(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 April 2012 (12.04.2012)

PCT

(10) International Publication Number
WO 2012/048140 A2

(51) International Patent Classification:
*H03M 3/00* (2006.01)

(21) International Application Number:
PCT/US2011/055147

(22) International Filing Date:
6 October 2011 (06.10.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/899,205 6 October 2010 (06.10.2010) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 12/899,205 (CON)
Filed on 6 October 2010 (06.10.2010)

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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(54) Title: PIPELINED CONTINUOUS-TIME SIGMA DELTA MODULATOR

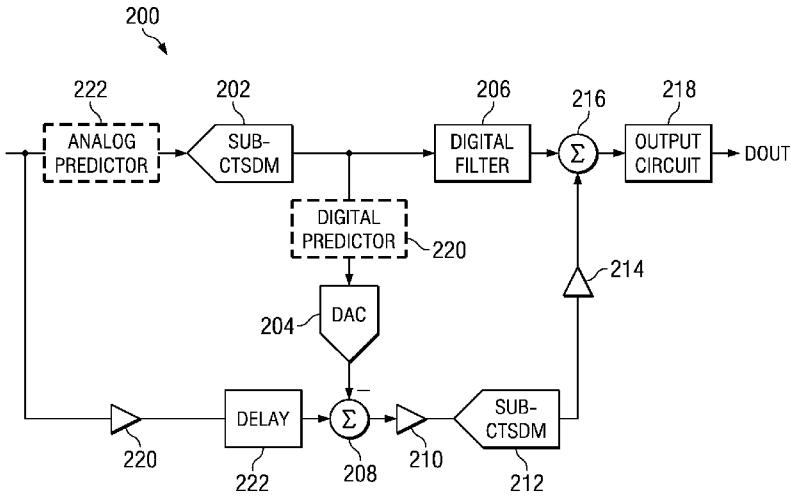


*FIG. 2*

(57) Abstract: A pipelined continuous-time (CT) sigma-delta modulators (SDM) is provided that has an architecture that is readily calibrated. The system includes a digital filter and other features that can be adjusted to account for input imbalance errors and well as quantization leakage noise. An example two-stage pipeline arrangement has CT SDMs (or sub-CT SDMs) 202 and 212, DAC 204, digital filter 206, amplifiers 220 and 210, digital gain circuit 214, summing circuits 208 and 216, output circuit 218, and an adjustable delay 222. CT SDM 202 may be a lower order modulator (i.e., order of 1 or 2), while CT SDM 212 may be a higher order modulator (i.e., order greater than 3) with aggressive noise shaping. Amplifier 210 also includes a filter.

WO 2012/048140 A2

**Declarations under Rule 4.17**:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

**Published**:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

# PIPELINED CONTINUOUS-TIME SIGMA DELTA MODULATOR

**[0001]** This relates generally to data converters and, more particularly, to continuous-time (CT) sigma-delta modulators (SDMs) or sigma-delta analog-to-digital converters (ADCs).

## BACKGROUND

**[0002]** In FIG. 1, the reference numeral 100 generally designates a pipelined discrete-time (DT) SDM. With a DT data converter, an analog input signal (such as signal AIN) is sampled by a sample-and-hold (S/H) circuit (such as S/H circuit 102) at discrete points in time or sampling instants, and the samples are converted to digital. Here, two SDM stages 104-1 and 104-2 are used in a pipeline configuration to perform the conversion for each of the samples. Each of stages 104-1 and 104-2 respectively comprise summing circuits 116-1/118-1 or 116-2/118-2, a delay 120-1 or 120-2, quantizer 122-1 or 122-2, digital low pass filter (LPF) 124-1 or 124-2, and digital-to-analog converter (DAC) 128-1 or 128-2. Additionally, stage 104-1 also includes digital filter 126. Between stages 104-1 and 104-2, there are several other components that enable stages 104-1 and 104-2 to operate as a pipeline; namely, these components are delay 108, summing circuit 110, amplifiers 112 and 114, analog LPF 113, and digital output circuit 106.

**[0003]** In operation, DT SDM 100 converts the analog input signal AIN to digital output signal DOUT. To accomplish this, a sample of the analog input signal AIN is provided to stage 104-1 (by S/H circuit 102), where the sample is converted to digital using conventional sigma-delta modulation. The same sample is provided to delay 108 so as to provide stage 104-1 with sufficient time to perform the data conversion. The difference analog representation of the data conversion (from DAC 128-1) and the sampled analog input signal AIN (from delay 108) or residue is determined by summing circuit 110. This residue is amplified and filtered by amplifiers 112 and 114 and analog LPF 113 and provided to stage 104-2. Stage 104-2 can then convert the residue to digital using conventional sigma-delta modulation. The digital output

circuit 106 then generates the digital output signal DOUT based the output from each pipeline 104-1 and 104-2.

**[0004]** This architecture, however, is incompatible with CT sigma-delta modulation. With DT sigma-delta modulation, the input to the stages (i.e., stages 104-1 and 104-2) is constant during conversion because the S/H circuit 102 holds the sampled analog input signal AIN. In contrast, an input to stages of a pipeline would be varying. Looking to DT SDM 100, it specifically employs a delay 108 so that stages 104-1 and 104-2 perform sigma-delta modulation on the same sample. If one were to remove the S/H circuit 102 so as to provide a continuously varying signal (i.e., analog input signal AIN) directly to stage 104-1 and delay 108, DT SDM 100 would not function.

**[0005]** Some other conventional circuits are disclosed in U.S. Patent Nos. 5,729,230; 6,788,232; 7,460,046; and 7,486,214.

SUMMARY

**[0006]** An example embodiment provides an apparatus including a first continuous-time (CT) sigma-delta modulator (SDM) that receives an analog input signal; a digital-to-analog converter (DAC) that is coupled to the first CT SDM; a first summing circuit that receives the analog input signal and that is coupled to the DAC, wherein the first summing circuit determines a difference between the analog input signal and an output from the DAC; an amplifier that is coupled to the summing circuit, wherein the amplifier has a first gain, and wherein the amplifier includes a filter; a second CT SDM that is coupled to the amplifier; a digital gain circuit that is coupled to the second CT SDM, wherein the digital gain circuit has a second gain, and wherein the second gain is substantially the inverse of the first gain, and wherein the amplifier, the second CTSDM, and the DAC collectively have a first transfer function; a digital filter that is coupled to the first CT SDM, wherein the digital filter has a second transfer function, wherein the second transfer function substantially matches the first transfer function; and a second summing circuit that is coupled to the digital filter and the digital gain circuit.

**[0007]** In accordance with an example embodiment, the DAC further comprises a first DAC having a third gain, and wherein the digital filter has a fourth gain, and wherein the second CT SDM further comprises: a third summing circuit that is coupled to the amplifier; an SDM filter that is coupled to the third summing circuit; a quantizer that is coupled to the SDM filter; and a second DAC that is coupled to the quantizer and the third summing circuit, wherein the

third summing circuit determines a difference between an output of the amplifier and an output of the second DAC, and wherein the second DAC has a fifth gain, and wherein the ratio of the third gain to the fifth gain is approximately equal to the fourth gain.

**[0008]** In accordance with an example embodiment, the SDM filter and the quantizer further comprise a first SDM filter and a first quantizer, and wherein the first CT SDM further comprises: a fourth summing circuit that receives the analog input signal; a second SDM filter that is coupled to the fourth summing circuit; a second quantizer that is coupled to the second SDM filter; and a second DAC that is coupled to the second quantizer and the fourth summing circuit, wherein the fourth summing circuit determines a difference between the analog input signal and an output of the second DAC.

**[0009]** In accordance with an example embodiment, the apparatus further comprises: an analog delay line that receives the analog input signal is coupled to the first summing circuit; and a digital predictor that is coupled between the first CT SDM and the first DAC.

**[0010]** In accordance with an example embodiment, the apparatus further comprises an analog predictor that receives the analog input signal and that is coupled to the fourth summing circuit.

**[0011]** In accordance with an example embodiment, the amplifier further comprises a first amplifier, and wherein the apparatus further comprises a second amplifier that is coupled to the first summing circuit and that receives the analog input signal.

**[0012]** In accordance with an example embodiment, the second amplifier has a third gain, and wherein the third gain is dimensioned to minimize an autocorrelation of an output of the second CT SDM.

**[0013]** In accordance with an example embodiment, the apparatus further comprises an output circuit that is coupled to the second circuit and that provides a digital output signal.

**[0014]** In accordance with an example embodiment, an apparatus is provided. The apparatus comprises an input terminal; a first stage of a pipeline including: a first CT SDM that is coupled to the input terminal; and a digital filter that is coupled to the first CT SDM, wherein the digital filter has a first transfer function; a second stage of a pipeline including: a first summing circuit that is coupled to the input terminal, wherein the first summing circuit is adapted to determine a difference; an amplifier that is coupled to the first summing circuit, wherein the amplifier has a first gain, and wherein the amplifier includes a filter; a second CT

SDM that is coupled to the first amplifier; and a digital gain circuit that is coupled to the second CT SDM, wherein the digital gain circuit has a second gain that is an inverse of the first gain; a DAC that is coupled between the first CT SDM and the first summing circuit, wherein the amplifier, the DAC, and the second CT SDM collectively have a second transfer function; and a second summing circuit that is coupled to each stage of the pipeline, wherein the first transfer function is adjusted to substantially match the second transfer function.

**[0015]** In accordance with an example embodiment, the DAC further comprises a first DAC having a third gain, and wherein the digital filter has a fourth gain, and wherein the second CT SDM further comprises: a third summing circuit that is coupled to the amplifier; an SDM filter that is coupled to the third summing circuit; a quantizer that is coupled to the SDM filter; and a second DAC that is coupled to the quantizer and the third summing circuit, wherein the third summing circuit determines a difference between an output of the amplifier and an output of the second DAC, and wherein the second DAC has a fifth gain, and wherein the ratio of the third gain to the fifth gain is approximately equal to the fourth gain.

**[0016]** In accordance with an example embodiment, the SDM filter and the quantizer further comprise a first SDM filter and a first quantizer, and wherein the first CT SDM further comprises: a fourth summing circuit that receives the analog input signal; a second SDM filter that is coupled to the fourth summing circuit; a second quantizer that is coupled to the second SDM filter; and a second DAC that is coupled to the second quantizer and the fourth summing circuit, wherein the fourth summing circuit determines a difference between the analog input signal and an output of the second DAC.

**[0017]** In accordance with an example embodiment, the amplifier further comprises a first amplifier, and wherein the apparatus further comprises a second amplifier that is coupled to the first summing circuit and that receives the analog input signal.

**[0018]** In accordance with an example embodiment, the second amplifier has a third gain, and wherein the third gain is adjusted by the controller to minimize an autocorrelation of an output of the second CT SDM.

**[0019]** In accordance with an example embodiment, the apparatus further comprises an output circuit that is coupled to the second circuit and that provides a digital output signal.

**[0020]** In accordance with an example embodiment, an apparatus is provided. The apparatus comprises an input terminal that receives an analog input signal; a first stage of a pipeline including: a first CT SDM including: a first summing circuit that is coupled to the input terminal so as to receive the analog input signal; a first SDM filter that is coupled to the first summing circuit; a first quantizer that is coupled to the first SDM filter; and a first DAC that is coupled to the first quantizer and the first summing circuit, wherein the first summing circuit determines a difference between the analog input signal and an output of the second DAC; and a digital filter that is coupled to the first CT SDM, wherein the digital filter has a first transfer function; a second stage of a pipeline including: a first amplifier that is coupled to the input terminal so as to receive the analog input signal, wherein the first amplifier has a first gain; a second summing circuit that is coupled to the first amplifier, wherein the second summing circuit is adapted to determine a difference; a second amplifier that is coupled to the second summing circuit, wherein the second amplifier has a second gain, wherein the second amplifier includes a filter; a second CT SDM having: a third summing circuit that is coupled to the second amplifier; a second SDM filter that is coupled to the third summing circuit; a second quantizer that is coupled to the second SDM filter; and a second DAC that is coupled to the second quantizer and the third summing circuit, wherein the third summing circuit determines a difference between an output of the second amplifier and an output of the second DAC; and a digital gain circuit that is coupled to the second CT SDM, wherein the third amplifier has a third gain that is an inverse of the second gain; a third DAC that is coupled between the first CT SDM and the second summing circuit, wherein the third DAC, the second CT SDM, and the second amplifier collectively have a second transfer function; a fourth summing circuit that is coupled to each stage of the pipeline, wherein the first transfer function is adjusted to substantially match the second transfer function, and wherein the first gain is adjusted to minimize an autocorrelation of an output of the second CT SDM, and wherein a gain of the digital filter to be approximately equal to a ratio of the gains of the second and third DACs; and an output circuit that is coupled to the fourth summing circuit and that provides a digital output signal.

**[0021]** In accordance with an example embodimen, a method for calibrating at least a portion of a pipelined continuous-time (CT) sigma-delta modulator (SDM) is provided, The CT SDM includes a first stage, a second stage, and a first digital-to-analog converter (DAC) coupled between the first and second stages, and a digital filter that is coupled to the first and second

stages, and wherein the second stage includes a second DAC. The method comprises determining a ratio of a gain of the first DAC to a gain of the second DAC; adjusting a gain of a digital filter to be approximately equal to the ratio of the gain of the first DAC to the gain of the second DAC; and adjusting the digital filter to maximize a cross-correlation between an output of the digital filter and the output of the second stage.

**[0022]** In accordance with an example embodiment, the method further comprises: disabling the first DAC, wherein the first DAC is located between a first stage and a second stage of the pipelined CT SDM; applying a predetermined input signal to the second stage while the first DAC is disabled; enabling the first DAC; disabling the second DAC within the second stage; and applying the predetermined input signal to the second stage while the using the first DAC as a feedback DAC for the second stage.

**[0023]** In accordance with an example embodiment, the method further comprises determining a gain of an amplifier located in the second stage that minimizes an autocorrelation of an output of the second stage.

**[0024]** In accordance with an example embodiment, a method for calibrating at least a portion of a pipelined CT SDM is provided. The method comprises disabling a first DAC, wherein the first DAC is located between the first stage and the second stage of the pipelined CT SDM; applying a predetermined input signal to the second stage while the first DAC is disabled; enabling the first DAC; disabling a second DAC within the second stage; applying the predetermined input signal to the second stage while the using the first DAC as a feedback DAC for the second stage; determining gains of the first and second DACs; and adjusting a gain of a digital filter to be a function of the gains of the first and second DACs.

**[0025]** In accordance with an example embodiment, the digital filter is coupled to the first and second stages.

**[0026]** In accordance with an example embodiment, the function is a ratio of the gains of the first and second DACs.

**[0027]** In accordance with an example embodimen, the method further comprises determining a gain of an amplifier located in the second stage that minimizes an autocorrelation of an output of the second stage.

**[0028]** In accordance with an example embodiment, the method further comprises adjusting the digital filter to maximize a cross-correlation between an output of the digital filter and the output of the second stage.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0029]** Example embodiments are described with reference to accompanying drawings, wherein:

**[0030]** FIG. 1 is a block diagram of a conventional pipelined DT SDM;

**[0031]** FIG. 2 is a block diagram of an example of a pipelined CT SDM in accordance with an example embodiment of the present invention; and

**[0032]** FIGS. 3 and 4 are block diagrams of examples of the sub-CT SDMs of FIG. 2.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

**[0033]** In FIGS. 2-4, an example of a pipelined CT SDM 200 in accordance with an example embodiment of the present invention can be seen. As an example, CT SDM 200 is a two-stage pipeline; however, CT SDM 200 can be scaled to include more stages. In this example, CT SDM 200 generally comprises CT SDMs (or sub-CT SDMs) 202 and 212, DAC 204, digital filter 206, amplifiers 220 and 210, digital gain circuit 214, summing circuits 208 and 216, output circuit 218, and an adjustable delay 222. CT SDM 202 (which can be seen in FIG. 3) generally comprises summing circuit 302, SDM filter 304, quantizer 306, and DAC 308, and CT SDM 212 generally comprises summing circuit 402, SDM filter 404, quantizer 405, and DAC 408. Also, CT SDM 202 can be a lower order modulator (i.e., order of 1 or 2), while CT SDM 212 can be a higher order modulator (i.e., order greater than 3) with aggressive noise shaping. Moreover, amplifier 210 also includes a filter. Amplifiers 220 and 210 can take on many forms, including but not limited to voltage-to-voltage amplifiers (i.e., operational amplifiers), voltage-to-current amplifiers with a current gain (i.e, transconductance amplifiers or variable resistors), current-to-voltage amplifiers (i.e., transimpedance amplifiers), or current-to-current amplifiers (i.e., current mode amplifiers having a topology that depends on the input signal AIN).

**[0034]** In order for CT SDM to function, CT SDM 200 is generally calibrated to compensate for system mismatches, but to make any calibrations, the sources of mismatch and error should be identified. Each of DACs 204, 308, and 408 each have gains of $g_4$, $g_1$, and $g_2$, while amplifiers 220 and 210 and digital gain circuit 214 have gains of $g_3$, $g_5$, and $g_6$. Gain $g_6$

can be adjusted to be approximately equal to be the inverse of gain $g_5$ (or $g_6=1/g_5$), which generally eliminates the effect of amplifiers 210. Alternatively, the gain $g_5$ can be 1 so as to use the filter incorporated therein. Additionally, each of SDM filters 304 and 306 include a gain of $1/g_1$ and $1/g_2$, respectively, to compensate for the gains of their respective DACs 308 and 408, and digital filter 206 has a gain of $g_F$ and a transfer function of $C_F(z)$. As a result, the output $Y_1(z)$ (which is in the frequency domain or z-domain) from CT SDMs 202 is

$$(1) \qquad Y_1(z) = \frac{S_1(z)X(z)}{g_1} + N_1(z)Q_1(z),$$

where, $S_1(z)$ is the Signal Transfer Function (STF) and $N_1(z)$ is the Noise Transfer Function (NTF) of an equivalent Discrete-Time Sigma Delta Modulator to which the CT SDM 200 is mapped for purposes of analysis using techniques well known to those skilled in the art, $Q_1(z)$ is the quantization error of the quantizer and X(z) is the discrete time equivalent of the continuous-time input. This leads to the output $Y_{1,N}(z)$ from digital filter 206 being:

$$(2) \qquad Y_{1,N}(z) = Y_1(z)g_F C_F(z) = \left(\frac{g_F}{g_1}\right)S_1(z)X(z)C_F(z) + g_F N_1(z)Q_1(z)C_F(z),$$

The input R(z) into CT SDM 212 is a combination of the output from amplifier 220 and output $Y_1(z)$ yielding:

$$(3) \qquad R(z) = g_3X(z) - g_4Y_1(z) = g_3X(z) - \left(\frac{g_4}{g_1}\right)S_1(z)X(z) - g_4N_1(z)Q_1(z).$$

Now using the same rationale applied to CT SDM 202 (because the structures of CT SDMs 202 and 212 are similar), the output $Y_2(z)$ for CT SDM 212 is:

$$(4) \qquad \begin{aligned} Y_2(z) &= \frac{S_2(z)R(z)}{g_2} + N_2(z)Q_2(z) \\ &= \left(\frac{g_3}{g_2}\right)S_2(z)X(z) - \left(\frac{g_4}{g_1g_2}\right)S_2(z)S_1(z)X(z) \\ &\quad - \left(\frac{g_4}{g_2}\right)S_2(z)N_1(z)Q_1(z) + N_2(z)Q_2(z) \end{aligned}$$

Thus, the output Y(z) of CT SDM 200 should be:

$$
\begin{aligned}
Y(z) &= Y_{1,N}(z) + Y_2(z) \\
&= \left(\frac{g_F}{g_1}\right) S_1(z) X(z) C_F(z) + N_2(z) Q_2(z) \\
&+ \left(\frac{g_3}{g_2}\right) S_2(z) X(z) - \left(\frac{g_4}{g_1 g_2}\right) S_2(z) S_1(z) X(z) \\
&+ g_F N_1(z) Q_1(z) C_F(z) - \left(\frac{g_4}{g_2}\right) S_2(z) N_1(z) Q_1(z)
\end{aligned} \tag{5}
$$

Equation (5) can then be reduced as follows:

$$
\begin{aligned}
Y(z) &= \left(\frac{g_F}{g_1}\right) S_1(z) X(z) C_F(z) + N_2(z) Q_2(z) \\
&+ \left(\frac{g_1 g_3 - g_4 S_1(z)}{g_1 g_2}\right) S_2(z) X(z) \\
&+ \left(g_F C_F(z) - \left(\frac{g_4}{g_2}\right) S_2(z)\right) N_1(z) Q_1(z)
\end{aligned} \tag{6}
$$

Therefore, it can be easily observed that output Y(z) is a combination of the desired output $Y_{DES}(z)$, the input phase imbalance $Y_{PI}(z)$, and the quantization noise leakage $Y_{QNL}(z)$, which are as follows:

$$
\begin{aligned}
Y_{DES}(z) &= \left(\frac{g_F}{g_1}\right) S_1(z) X(z) C_F(z) + N_2(z) Q_2(z) \\
Y_{PI}(z) &= \left(\frac{g_1 g_3 - g_4 S_1(z)}{g_1 g_2}\right) S_2(z) X(z) \\
Y_{QNL}(z) &= \left(g_F C_F(z) - \left(\frac{g_4}{g_2}\right) S_2(z)\right) N_1(z) Q_1(z)
\end{aligned} \tag{7}
$$

**[0035]** Looking first to the quantization noise leakage $Y_{QNL}(z)$, this error is related to the gains $g_4$, $g_2$, and $g_F$ and transfer functions $C_F(z)$ and $S_2(z)$. If one were to set the ratio of gains $g_4$ and $g_2$ to be approximately equal to gain $g_F$ ($\frac{g_4}{g_2} = g_F$), then a matching of the transfer functions $C_F(z)$ and $S_2(z)$ would result in elimination of this quantization noise leakage $Y_{QNL}(z)$. Since

gain $g_F$ and $C_F(z)$ transfer function is adjustable (as being part of digital filter 206), adjustment can be based on determinations of the gains $g_4$ and $g_2$ and transfer function.

**[0036]** To determine the gains $g_4$ and $g_2$, DACs 204 and 408 can be selectively deactivated. Initially, a test signal (of any magnitude) can be applied to the CT SDM 200 with DAC 204 in a deactivated state and the gain $g_3$ set to 1 so that the output $Y_2(z)$ of CT SDM 212 can be measured. Under these circumstances, the gain $g_4$ is effectively 0, allowing equation (4) to be reduced to become output $Y_{2C1}(z)$ as follows:

$$(8) \qquad Y_{2C1}(z) = \left(\frac{1}{g_2}\right) S_2(z)X(z) + N_2(z)Q_2(z)$$

Then, the same test signal can be applied to CT SDM 212 with DAC 408 in a deactivated state and with DAC 204 as a feedback DAC for CT SDM 212. This changes the output $Y_2(z)$ to become output $Y_{2C2}(z)$ as follows:

$$(9) \qquad Y_{2C2}(z) = \frac{1}{g_4} S_2(z)X(z) + N_2(z)Q_2(z)$$

Each of outputs $Y_{2C1}(z)$ and $Y_{2C2}(z)$ can be measured. By dividing the outputs $Y_{2C1}(z)$ and $Y_{2C2}(z)$ and noting that for a small band-width around the signal of interest the term $N_2(z)Q_2(z)$ is negligible yields:

$$(10) \qquad \frac{Y_{2C1}(z)}{Y_{2C2}(z)} = \frac{g_4}{g_2}$$

Thus, a simple analysis of the system (which depends on the structures of the SDM filter 404) can yield the ratio $g_4/g_2$. Typically, CT SDM 212 can be a higher order modulator (i.e., greater than 3) so the SDM filter 404 be, accordingly, a higher order filter. Gain $g_F$ can then be adjusted to be proximately equal to the ratio $g_4/g_2$.

**[0037]** With gain $g_F$ set, the transfer function $C_F(z)$ can be adjusted to substantially match the transfer function $S_2(z)$. To do this, an error function E that is a cross-correlation of an output $Y_{1,N}(z)$ of digital filter and output $Y_2(z)$ of CT SDM 212 is used, where error function E is as follows:

$$(11) \qquad E\{Y_{1,N}(k), Y_2(k)\} = (Y_{1,N} * Y_2)(k) = \sum \overline{Y}_{1,N}(i)Y_2(i+k)$$

This error function E is maximized when the transfer functions $C_F(z)$ and $S_2(z)$ are matched. Thus, digital filter 206 can be adjusted until the error function E is substantially maximized. Additionally, because the $Q_1(z)$ are common terms between outputs $Y_{1,N}(z)$ and $Y_2(z)$, digital filter 206 can be blindly adjusted or calibrated.

**[0038]** Now, turning to the gain imbalance, the output $Y_2(z)$ is generally comprised shaped of Q-noise $Y_{2Q}(z)$ and phase/gain imbalance $Y_{2PI}(z)$, which are as follows:

$$Y_{2PI}(z) = X(z)\left(g_3 - \left(\frac{g_4}{g_1}\right)S_1(z)\right)\left(\frac{S_2(z)}{g_2}\right)$$

(12)

$$Y_{2Q}(z) = N_2(z)Q_2(z) - \left(\frac{g_4}{g_2}\right)S_2(z)N_1(z)Q_1(z)$$

Because there can be a delay associated with amplifier 220 and DAC 204, gains $g_3$ and $g_4$ can be represented as $g_3A_d(z)$ and $g_4D_d(z)$, and from equation (11) above, it is clear that the following condition should substantially eliminate the gain imbalance $Y_{2PI}(z)$:

$$g_3A_d(z) - \left(\frac{g_4}{g_1}\right)D_d(z)S_1(z) = 0 \quad (13)$$

This would mean that the gain imbalance of $Y_{2PI}(z)$ would be substantially eliminated when the when the autocorrelation of $Y_2(z)$ (with gains $g_3$ and $g_4$ represented as $g_3A_d(z)$ and $g_4D_d(z)$) is approximately equal to zero. Thus, by adjusting delay 222 and the gain of 220, the gain imbalance $Y_{2PI}(z)$ cab be substantially eliminated.

**[0039]** Alternatively, the ratio $g_4/g_1$ can be determined by selectively deactivating DACs 204 and 408, similar to the method described above to determine the ratio $g_4/g_2$. Initially, a test signal (of any magnitude) can be applied to the CT SDM 200 with DAC 204 in a deactivated state and the gain $g_3$ set to the ratio $g_4/g_1$ so that the output $Y_2(z)$ of CT SDM 212 can be measured. Under these circumstances, equation (4) can be reduced to become output $Y_{2D1}(z)$ as follows:

$$Y_{2D1}(z) = \left(\frac{1}{g_1}\right)S_2(z)X(z) + N_2(z)Q_2(z) \quad (14)$$

Then, the same test signal can be applied to CT SDM 212 with DAC 408 in a deactivated state and with DAC 204 as a feedback DAC for CT SDM 212. This changes the output $Y_2(z)$ to

become output $Y_{2C2}(z)$ as denoted in equation (9) above. Each of outputs $Y_{2D1}(z)$ and $Y_{2C2}(z)$ can be measured. By dividing the outputs $Y_{2D1}(z)$ and $Y_{2C2}(z)$ and noting that, for a small band-width around the signal of interest, the term $N_2(z)Q_2(z)$ is negligible yields:

$$\frac{Y_{2D1}(z)}{Y_{2C2}(z)} = \frac{g_4}{g_1} \quad (15)$$

Thus, a simple analysis of the system (which depends on the structures of the SDM filter 404) can yield the ratio $g_4/g_1$. Thus, by adjusting gain $g_3$ to be approximately equal to the ratio $g_4/g_1$ with this foreground calibration scheme (as opposed to the background scheme described above), gain imbalance can be substantially eliminated.

**[0040]** To generally eliminate phase imbalance, either a digital predictor 220 or digital predictor with an analog delay line 222 can be employed. The tuning of either the digital predictor 220 or the analog delay line 222 can be done by minimizing the autocorrelation (similar to the scheme described above). For the digital predictor 220, for example, an analog delay line 222 can be introduced such that the delay through delay line 222 is greater than that through the CT SDM 202 so as to allow digital predictor 220 to be tuned such that the auto-correlation is minimized.

**[0041]** Those skilled in the art to which the invention relates will appreciate that modifications may be made to the described example embodiments and other embodiments realized within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a first continuous-time (CT) sigma-delta modulator (SDM) that receives an analog input signal;

a digital-to-analog converter (DAC) that is coupled to the first CT SDM;

a first summing circuit that receives the analog input signal and that is coupled to the DAC, wherein the first summing circuit determines a difference between the analog input signal and an output from the DAC;

an amplifier that is coupled to the summing circuit, wherein the amplifier has a first gain, and wherein the amplifier includes a filter;

a second CT SDM that is coupled to the amplifier;

a digital gain circuit that is coupled to the second CT SDM, wherein the digital gain circuit has a second gain, and wherein the second gain is substantially the inverse of the first gain, and wherein the amplifier, the second CTSDM, and the DAC collectively have a first transfer function;

a digital filter that is coupled to the first CT SDM, wherein the digital filter has a second transfer function, wherein the second transfer function substantially matches the first transfer function; and

a second summing circuit that is coupled to the digital filter and the digital gain circuit.

2. The apparatus of Claim 1, wherein the DAC further comprises a first DAC having a third gain, and wherein the digital filter has a fourth gain, and wherein the second CT SDM further comprises:

a third summing circuit that is coupled to the amplifier;

an SDM filter that is coupled to the third summing circuit;

a quantizer that is coupled to the SDM filter; and

a second DAC that is coupled to the quantizer and the third summing circuit, wherein the third summing circuit determines a difference between an output of the amplifier and an output

of the second DAC, and wherein the second DAC has a fifth gain, and wherein the ratio of the third gain to the fifth gain is approximately equal to the fourth gain.

3. The apparatus of Claim 2, wherein the SDM filter and the quantizer further comprise a first SDM filter and a first quantizer, and wherein the first CT SDM further comprises:

a fourth summing circuit that receives the analog input signal;

a second SDM filter that is coupled to the fourth summing circuit;

a second quantizer that is coupled to the second SDM filter; and

a second DAC that is coupled to the second quantizer and the fourth summing circuit, wherein the fourth summing circuit determines a difference between the analog input signal and an output of the second DAC.

4. The apparatus of Claim 1, wherein the apparatus further comprises:

an analog delay line that receives the analog input signal is coupled to the first summing circuit; and

a digital predictor that is coupled between the first CT SDM and the first DAC.

5. The apparatus of Claim 1, wherein the apparatus further comprises an analog predictor that receives the analog input signal and that is coupled to the fourth summing circuit.

6. The apparatus of Claim 1, wherein the amplifier further comprises a first amplifier, and wherein the apparatus further comprises a second amplifier that is coupled to the first summing circuit and that receives the analog input signal.

7. The apparatus of Claim 6, wherein the second amplifier has a third gain, and wherein the third gain is dimensioned to minimize an autocorrelation of an output of the second CT SDM.

8. The apparatus of Claim 7, wherein the apparatus further comprises an output circuit that is coupled to the second circuit and that provides a digital output signal.

9. An apparatus comprising:

an input terminal;

a first stage of a pipeline including:

a first CT SDM that is coupled to the input terminal; and

a digital filter that is coupled to the first CT SDM, wherein the digital filter has a first transfer function;

a second stage of a pipeline including:

a first summing circuit that is coupled to the input terminal, wherein the first summing circuit is adapted to determine a difference;

an amplifier that is coupled to the first summing circuit, wherein the amplifier has a first gain, and wherein the amplifier includes a filter;

a second CT SDM that is coupled to the first amplifier; and

a digital gain circuit that is coupled to the second CT SDM, wherein the digital gain circuit has a second gain that is an inverse of the first gain;

a DAC that is coupled between the first CT SDM and the first summing circuit, wherein the amplifier, the DAC, and the second CT SDM collectively have a second transfer function; and

a second summing circuit that is coupled to each stage of the pipeline, wherein the first transfer function is adjusted to substantially match the second transfer function.

10. The apparatus of Claim 9, wherein the DAC further comprises a first DAC having a third gain, and wherein the digital filter has a fourth gain, and wherein the second CT SDM further comprises:

a third summing circuit that is coupled to the amplifier;

an SDM filter that is coupled to the third summing circuit;

a quantizer that is coupled to the SDM filter; and

a second DAC that is coupled to the quantizer and the third summing circuit, wherein the third summing circuit determines a difference between an output of the amplifier and an output of the second DAC, and wherein the second DAC has a fifth gain, and wherein the ratio of the third gain to the fifth gain is approximately equal to the fourth gain.

11. The apparatus of Claim 10, wherein the SDM filter and the quantizer further comprise a first SDM filter and a first quantizer, and wherein the first CT SDM further comprises:

a fourth summing circuit that receives the analog input signal;

a second SDM filter that is coupled to the fourth summing circuit;

a second quantizer that is coupled to the second SDM filter; and

a second DAC that is coupled to the second quantizer and the fourth summing circuit, wherein the fourth summing circuit determines a difference between the analog input signal and an output of the second DAC.

12. The apparatus of Claim 11, wherein the apparatus further comprises:

an analog delay line that is coupled between the first summing circuit and the input terminal; and

a digital predictor that is coupled between the first CT SDM and the first DAC.

13. The apparatus of Claim 11, wherein the apparatus further comprises an analog predictor that receives the analog input signal and that is coupled to the fourth summing circuit.

14. The apparatus of Claim 9, wherein the amplifier further comprises a first amplifier, and wherein the apparatus further comprises a second amplifier that is coupled to the first summing circuit and that receives the analog input signal.

15. The apparatus of Claim 14, wherein the second amplifier has a third gain, and wherein the third gain is adjusted by the controller to minimize an autocorrelation of an output of the second CT SDM.

16. The apparatus of Claim 15, wherein the apparatus further comprises an output circuit that is coupled to the second circuit and that provides a digital output signal.

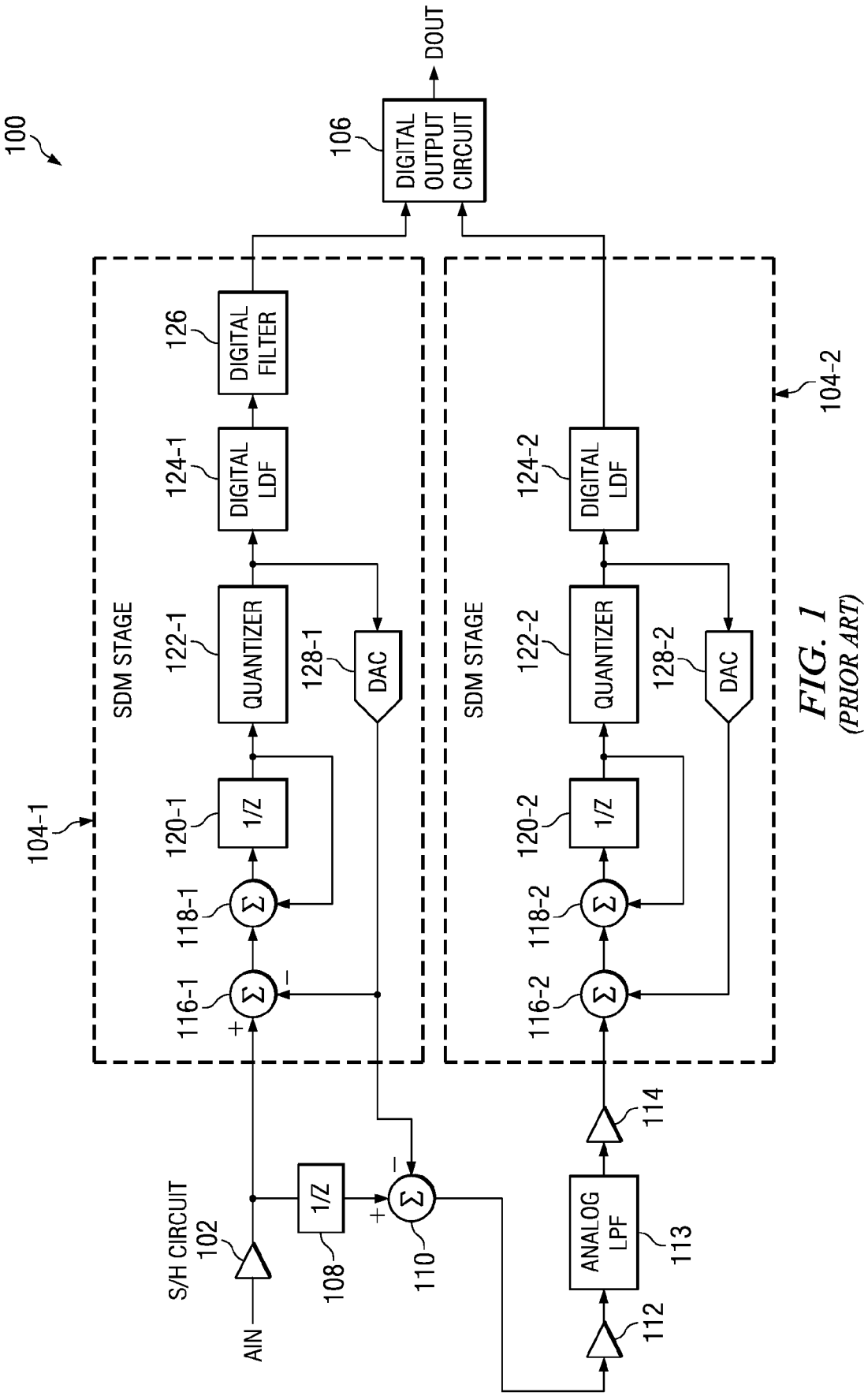


*FIG. 1*
*(PRIOR ART)*

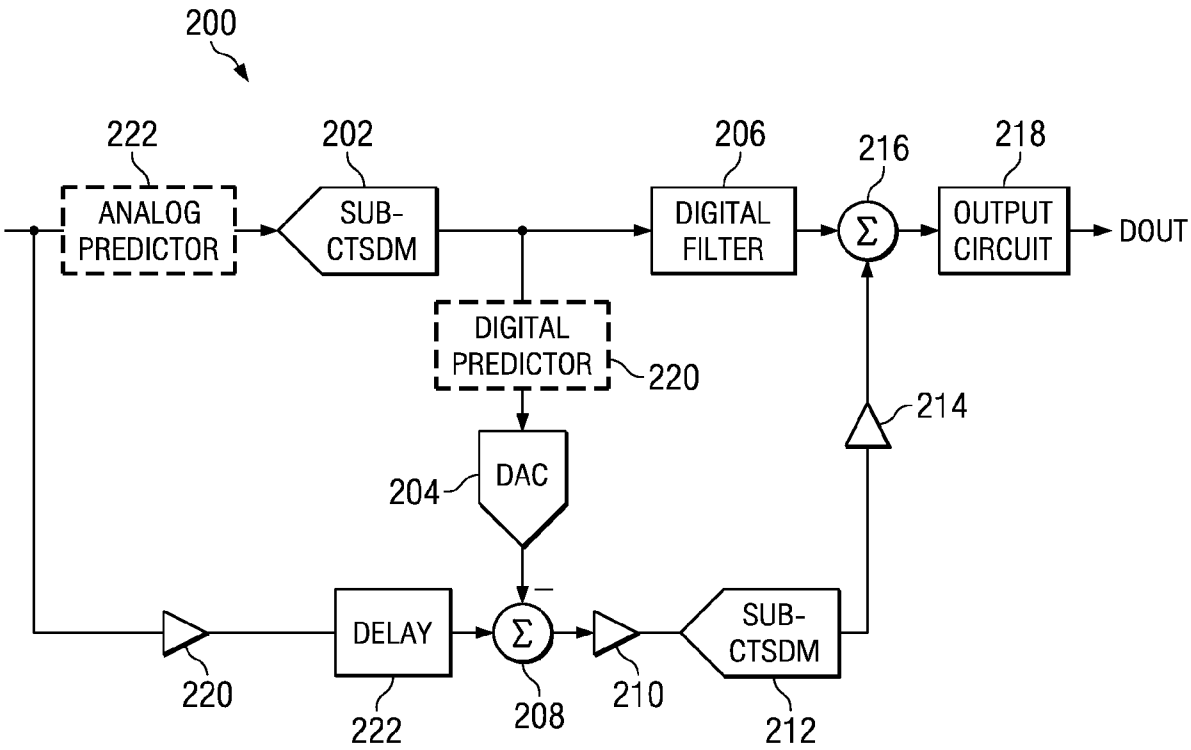


FIG. 2

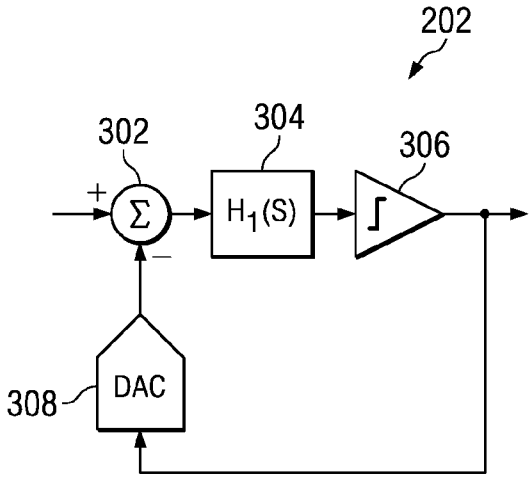


FIG. 3

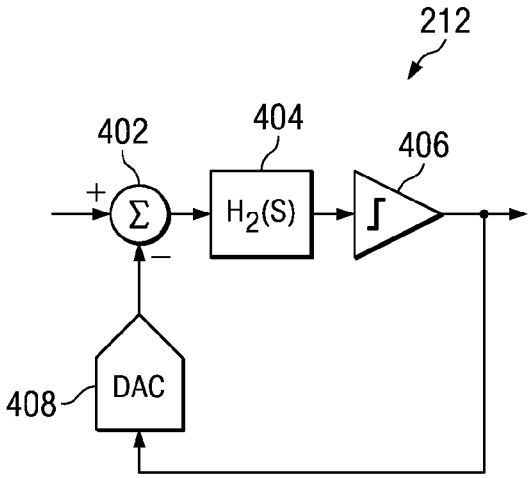


FIG. 4