Aug. 17, 1965 E. S. LEE III 3,201,605

MAGNETIC CORE FLUX COUNTER

Filed July 30, 1962 2 Sheets-Sheet 1

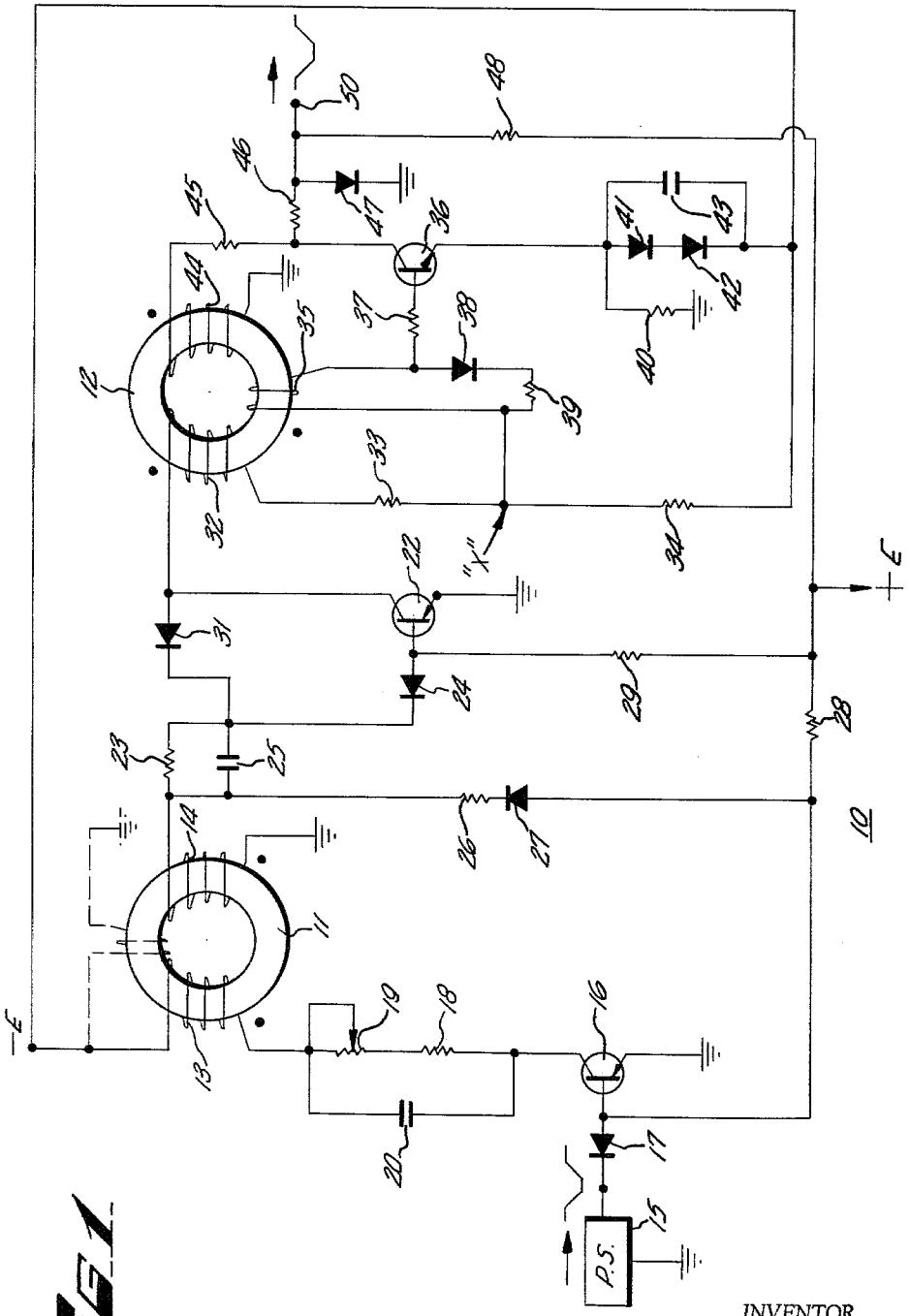


FIG 1

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MAGNETIC CORE FLUX COUNTER

Filed July 30, 1962 2 Sheets-Sheet 2

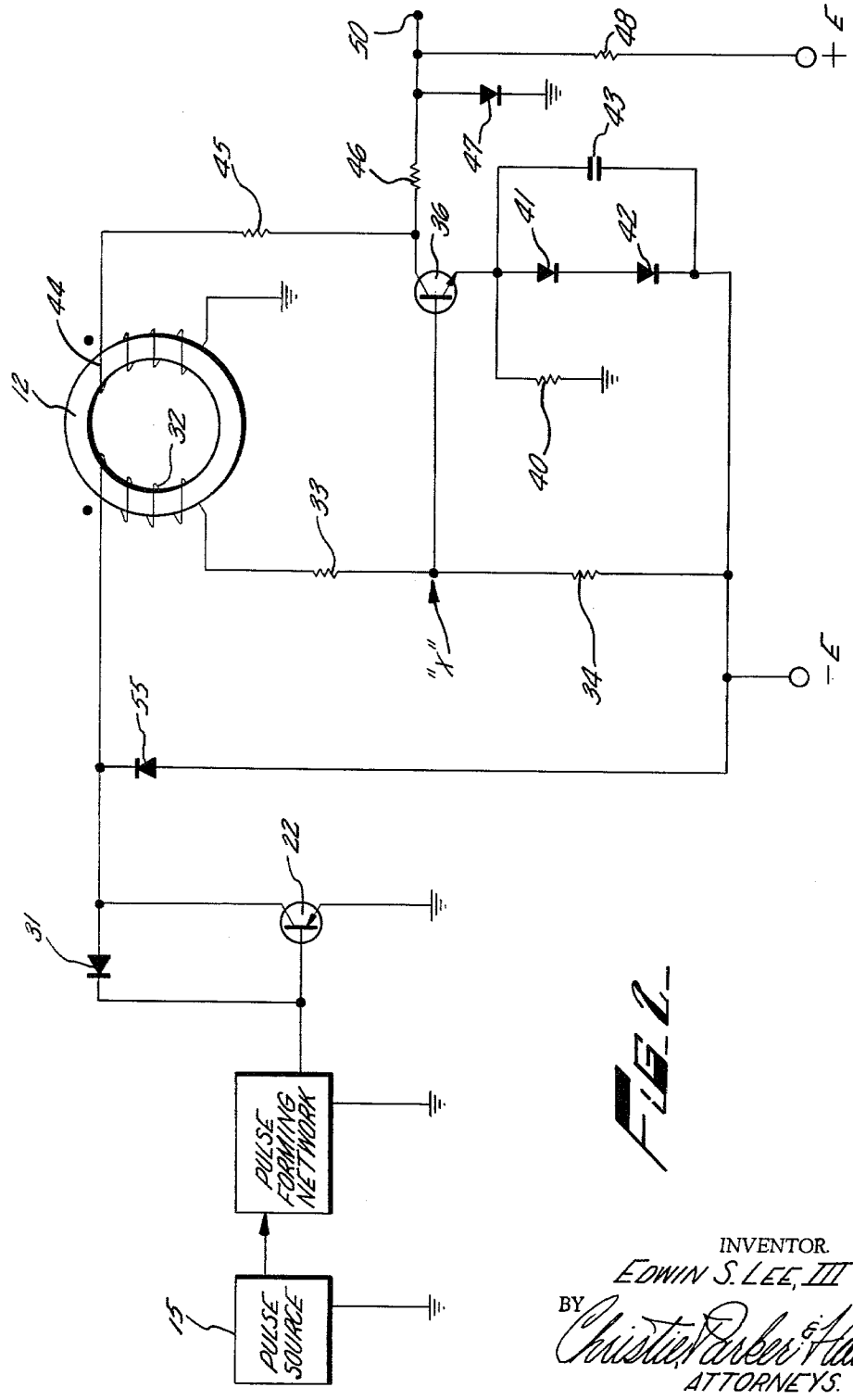


FIG 2

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3,201,605

MAGNETIC CORE FLUX COUNTER

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11 Claims. (Cl. 307—88.5)

This invention relates to a counter and, more particularly, to a magnetic core counter that counts by stepping a magnetic core along its hysteresis loop from one stable state to another stable state in a preselected plurality of increments or steps.

This invention is an improvement over the application of T. C. Chen and R. A. Tracy, entitled "Magnetic Device," and bearing Serial No. 498,257, filed on March 31, 1955, now abandoned in favor of continuation application Serial No. 221,399, filed on August 28, 1962, and now bearing Patent No. 3,102,239, granted on August 27, 1963, and assigned to the same assignee as this application.

The magnetic core counters described in the aforementioned co-pending patent application count input pulses and provide an output indication upon the application of a predetermined number of input pulses. The number of input pulses required to produce a single output pulse is a function of the number of pulses required to step a counting magnetic core from one stable magnetic state to another stable state along its hysteresis loop. The teachings of this co-pending application further indicate that the pulses applied to a counting core require that the pulses be quantized or have a constant voltage time product in order that each step up the hysteresis loop be substantially the same for producing the desired count. These quantized pulses may be generated by a quantizing magnetic core which produces an output pulse in switching from one stable state to the other stable state and which output pulse has been proportioned in terms of its voltage and time duration to cause the counting core to step along the hysteresis loop a desired increment in response thereto. This type of magnetic core counter has also been described in the literature and is commonly referred to as a "flux counter."

Various types of circuit configurations have been developed for generating and transferring the quantized pulses from a quantizing source to the counting core to provide the desired counting action. It has been found that although these circuits operate satisfactorily under controlled conditions they are sensitive to normal variations of the voltages from the power supplies and may cause the magnetic counters to provide erroneous counts. The changes in potential derived from the power sources effect both the quantizing cores and the counting core and, more particularly, effect the voltage-time product of the quantizing pulse to be counted applied to the count core. Therefore, the increment or the step that the count core is switched varies from the preselected increment and thereby may cause a change in the total number of steps or count of the count core. Furthermore, when semiconductor switching elements are utilized in combination with the quantizing magnetic core, it has been found that when the input pulses applied to the quantizing core and the semiconductor switch have a longer time duration than the output pulses, the semiconductor may exhibit a storage time that also effects the voltage-time product of the output pulse applied and, therefore, the correct operation of the counting core.

The present invention provides an improved magnetic core counter of the flux counting type in which the quantized pulses applied to the counting core are accurately generated even with normal variations in the power supply or voltages derived therefrom whereby a preselected

count is always correctly indicated. The magnetic core counter of the present invention is operable with normal power supply variations to provide a quantized pulse to the counting core having a constant voltage-time product by proportioning and arranging the circuit parameters associated with the switching windings to compensate for these changes whereby the counting core can be characterized as tracking the quantizing core. The counting circuit of the invention is also readily adjustable over a wide range of counts. Furthermore, the circuit parameters are arranged whereby the effect of storage time of the semiconductor devices is eliminated and the relative time durations of the input pulses to be counted and applied to the quantizing core and the output or quantizing pulses do not effect the counter operation.

Structurally, the invention comprises a quantizing magnetic core and a counting magnetic core each having a substantially rectangular hysteresis loop and at least an input and an output winding coupled to the core. A source of pulses to be counted is coupled to the input winding for the quantizing core by means of a normally non-conductive switching element, which may be a semiconductive element, having a variable impedance network coupled thereto. The output pulses from the quantizing core are coupled to the counting magnetic core by means including asymmetrical conducting circuit means coupled and arranged between the quantizing core output winding and the input winding for the counting core. The asymmetrical conducting means includes a normally non-conductive switching element that is rendered responsive only to a pulse to be counted and which switching element is also provided with an impedance network having a preselected value arranged with the input winding of the count core. These impedance means are proportioned relative to one another to allow the quantized pulses delivered to the counting core to be accurately defined and proportioned with power supply variations to produce the required count. The counting core is further arranged with a reset winding coupled thereto. The output and reset windings are arranged with a switching element and the impedance network to be normally in a non-conductive condition and adapted to be switched to a conductive condition to produce an output indication only when the count core switches into saturation and completes its count for automatically resetting the core.

These and other features of the present invention may be more fully appreciated when considered in the light of the following specification and drawings, in which:

FIG. 1 is a schematic circuit diagram of the magnetic counter embodying the invention; and

FIG. 2 is a schematic circuit diagram of another embodiment of the invention.

Now referring to FIG. 1 the magnetic counter **10** of the present invention will be described. The magnetic core counter comprises a quantizing magnetic core **11** and a counting magnetic core **12**. Each of the magnetic cores **11** and **12** has a substatnially rectangular hysteresis loop and, therefore, may be set at a plurality of stable magnetic states between the saturated conditions at the extreme ends of the loop. The quantizing magnetic core **11** has an input winding **13** inductively coupled thereto and an output winding **14** similarly arranged therewith. A source of pulses to be counted is represented in block form and identified as the pulse source **15** and which pulse source is coupled to the input winding **13** by circuit means including a switching element **16**. The switching element **16** is shown as a semiconductive switching element or a transistor having its output electrode connected through an impedance means or network to the input winding **13**.

Specifically, the base electrode for the switching ele-

ment **16** is coupled by means of a unilateral conductive device or diode to the pulse source **15** to allow only negative pulses to be applied to the input circuit of element **16**. The emitter electrode is connected directly to a point of reference potential or ground, as shown. The collector or output electrode of the switching element **16** is connected through a series of voltage dividing impedance elements comprising a resistance impedance element **18** connected to the output electrode of element **16** and to the manually variable resistive impedance element **19**. The remaining terminal of the resistive impedance element **19** is connected to one terminal of the input winding **13** while the other terminal of the input winding is connected to a point of negative potential, shown as —E. The impedance means further comprises a by-pass capacitor shown as the capacitor **20** connected in parallel circuit relationship with both of the impedance elements **18** and **19**. The base electrode of the switching element **16** is also connected to a point of positive potential, shown as the +E terminal of the power supply, through a dropping resistor **28**. The described arrangement of impedance elements is such as to normally maintain the switching element **16** in a non-conductive condition and to be rendered conductive in response to a negative pulse from the source **15**.

It should be noted that the provision of the impedances **18** and **19** in the collector circuit of the switching element **16** is an important feature of the invention. These impedances limit the collector current and thereby decrease the dissipation in the transistor. If no impedance or a small impedance was provided for the collector circuit, the collector current would rise to a very high value when the magnetic core **11** is saturated and the input pulse is still present or if the transistor has any storage time and a finite turn off time. Stated differently, these impedances compensate for any excessive conduction time of the switching element **16**.

The output winding **14** for the magnetic core **11** has one terminal connected directly to ground while the other terminal connected through circuit means with another switching element identified by the reference numeral **22**, and which element may be a semiconductive element of the same type as the switching element **16**. The emitter electrode of this switching element is connected directly to ground, while the base electrode is connected to a voltage dropping resistive impedance element **23** by means of an asymmetrical conducting element or diode **24**. The resistive element **23** is further arranged with a parallel by-pass capacitor **25**. A parallel circuit path from the output winding **14** is defined to the positive source of potential shown as the +E terminal by means of the resistive impedance element **26** arranged with a series diode **27** having its anode connected to one terminal of the resistor **28**. To this same end, a resistive impedance element **29** is coupled between the base electrode of the switching element **22** and the +E terminal as shown. The output or collector electrode of the switching element **22** is further shown provided with a diode **31** connected thereto and to the common junction of the diode **24** and the resistor **23**.

The output electrode for the switching element **22** is connected directly to an input winding **32** for the count core **12** for receiving the quantized pulses to be counted applied thereto. The remaining terminal of the input winding **32** is connected by means of a voltage dividing network comprising the series arranged resistive impedance elements **33** and **34**. The one terminal of the resistor **34** is connected to the negative terminal of the power supply source, shown as the —E terminal. A feedback winding **35** is also inductively coupled to the counting core **12** and has one terminal connected to the common junction between the resistive elements **33** and **34**, while the other terminal is connected to a further switching element **36** shown as a transistor having its base electrode connected thereto by means of a series

resistive impedance element **37**. The common junction between the resistor **37** and the feedback winding **35** is shown coupled to the anode of a diode **38** arranged in series with a further resistive impedance element **39** coupled to the common junction between the resistors **33** and **34** or the junction identified by the reference letter "X."

The emitter electrode for the switching element **36** is connected to a pair of parallel circuits. One of these circuits comprises a resistive element **40** having its opposite terminal connected to ground, while the other parallel circuit comprises the parallel combination of a pair of series connected diodes **41** and **42** arranged in parallel with a capacitor **43**. This latter parallel combination is connected directly to the negative terminal of the power source, —E. The output or collector electrode for the transistor **36** is shown coupled to an output windign **44** through a series resistor **45** and which output winding **44** has one terminal connected directly to ground and is inductively coupled to the count core **12**. The output electrode is also arranged with an output resistive element **46** and a parallel diode **47** having its cathode electrode connected directly to ground. The resistive impedance element **46** is also connected to the positive terminal of the power supply through the dropping resistor **48**. The output pulses from the counter **10** are derived by means of the output terminal identified by the reference numeral **50**.

It should be noted that in the preferred embodiment of the invention the switching elements **16**, **22**, and **36** are transistors and the transistor **36** is of the opposite conductivity type from the switching elements **16** and **22**, as illustrated.

As discussed hereinabove, the counting core **12** will be stepped between its stable states or points of negative and positive remanence in a predetermined plurality of discrete steps and will produce an output pulse only when the count core reaches one of the states of saturation. The pulses applied to the counting core **12**, and more specifically to the input winding **32** thereof, must be quantized input pulses to produce an output pulse only upon the application of a desired number of quantized pulses. The variable resistive impedance element **19** arranged in circuit relationship with the input winding **13** for the quantizing core **11** is adjusted to produce the number of quantized pulses for setting the base of the magnetic core counter **10**. To this end, the circuit will be described in accordance with the adjustment of the impedance element **19** for setting the counter **10** to produce an output pulse for every eight input pulses.

With the above structure in mind, the operation of the magnetic counter **10** will now be more fully described. It will be recognized that the switching elements **16**, **22**, and **36** are all normally arranged and the associated circuit parameters are proportioned to maintain them in a non-conductive condition. It will be further assumed that each of the magnetic cores **11** and **12** are arranged to be positioned at their negative points of remanence with the quantizing core **11** producing a pulse to be counted each time the core is switched from its negative state to its positive state of remanence only, while the counting core **12** produces an output pulse only after the counting core has reached its positive state of remanence and is being returned to its negative point of remanence. Specifically, it should be noted that a pulse to be counted is not coupled from the quantizing core **11** to the counting core **12** when the quantizing core **11** is switched from its positive remanence point to the negative remanence point. Also, no output pulses are produced from the count core **12** when the core switches from the negative point of remanence to the positive point, as well as during the times the core is being stepped along its hysteresis loop from negative to positive remanence.

Now assuming that a negative pulse is delivered from the pulse source **15** to the input circuit for the switching

element 16 and which negative pulse is proportioned to place the switching element 16 into a conductive condition in accordance with the time duration thereof. The conduction of the switching element 16 is further proportioned in terms of the windings for the input winding 13 to cause the magnetic core 11 to be switched from its negative to positive state of remanence. The switching of the quantizing core 11 therefore develops an output pulse in the output winding 14 which is coupled to the input circuit of the switching element 22 and the associated circuitry is further proportioned to cause the switching element 22 to be rendered conductive in response thereto for a specific length of time. The pulse provided at the output electrode for the switching element 22 is applied to the input winding 32 and is quantized (voltage×time) to cause the counting core 12 to be stepped along its hysteresis characteristic approximately one-eighth of the way in accordance with the assumed operating conditions. As a result of the stepping or switching of the counting core 12 along its hysteresis loop, it will be recognized that voltages will be induced in each of the windings 32, 35, and 44. Simultaneous with the generation of the voltages in the windings for the count core 12, the point "X" will be driven more positive than the negative potential at the emitter electrode for the switching element 36 which normally maintains the element non-conductive. The voltage developed across the feedback winding 35, however, maintains the potential of the base electrode for the switching element 36 more negative than the potential at the emitter electrode and, therefore, maintains the switching element 36 in its non-conductive condition during these stepping intervals. It will also be noted that during this interval the voltage developed across the output winding 44 tends to drive the output terminal in a positive direction but, due to the provision of the diode 47, is prevented from driving in this fashion and, therefore, under these conditions, no output pulse is derived from the output terminal 50.

This action then continues for each pulse delivered to the input winding 32. It should be noted that during the intervals between the delivery of the input pulses from the pulse source 15 the quantizing core 11 is reset as a result of the direct current circuit path provided by means of the direct current circuit path from the +E terminal of the power supply through the resistive impedance element 29, the diode 24, resistive element 23, and through the output winding 14 to ground. During the interval that the quantizing core 11 is being reset to its negative point of remanence, the voltage generated in the output winding 14 is of an opposite polarity from that previously generated and, therefore, does not render the switching element 22 conductive.

It will now be assumed that seven quantized pulses have been applied to the count core 12 and that the eighth pulse arrives at the input winding 32 to drive the count core into saturation. When the count core 12 is driven into saturation, the voltages normally developed across the windings 32, 35 and 44 will collapse. The current from the output or collector electrode of the switching element 22 will thereby increase due to the decreased impedance of the input winding 32 thereby driving the point "X" even more positive. Since the voltage across the feedback winding 35 has collapsed and this voltage previously prevented the conduction of the switching element 36, this element will now be rendered conductive in response to the saturated condition of the count core 12. The output or collector electrode for the switching element 36 then will be driven in a negative direction and, accordingly, drive the output winding 44. The energization of the output winding 44 will tend to reset the count core 12 and simultaneously will cause an increase in the drive for the base electrode of the switching element 36 due to the positive feedback between the windings 44 and 35. This then will be effective to completely reset the count core 12 to its point

of negative remanence and an output pulse will be provided at the output terminal 50. It should be noted that the count core 12 will be reset by this action without reference to when the conduction of the switching element 22 is terminated, or, stated differently, the time that the count core 12 is reset will not be dependent upon the time duration of the input pulses from the pulse source 15 and, therefore, the time that the switching element 22 is conductive.

The above described operation is the desired operation of the magnetic counter 10, however, it should be noted that an important aspect of the present invention is the ability of the count core 12 to track the quantizing core 13 with normal changes in the voltages provided by the power supply and yet provide a quantized pulse that provides the correct action. In particular, the flux counters of the prior art have been sensitive to the voltages provided by the power sources corresponding to the voltage derived at the —E terminal and thereby do not always produce correct counts. It should be recognized that since the quantized pulse is dependent upon the product of voltage and time being a constant for correct operation, that variations of the voltages from the terminal —E cause the pulses delivered to the count core 12 to vary from this constant. In accordance with the present invention the normal variations in the power supply are compensated for due to the provision of the impedance means arranged with each of the input windings 13 and 32 for the quantizing core 11 and count core 12 respectively. These impedance means are proportioned relative to one another whereby the normal changes in the voltages from the power supply are compensated for to produce the desired constant voltage-time product. To this end, if the voltage —E decreases, the parameters of the circuit are such that the output pulse from the switching element 22 exists for a longer time and its time-voltage product is the desired constant product whereby the quantized pulse delivered to the input winding 32 is correctly proportioned. To this same end, when the —E voltage increases, the time duration of the pulse from the switching element 22 decreases to produce the desired stepping action.

In a typical circuit of the invention, the impedance elements 33 and 34 may be on the order of 100 ohms each and the impedance element 18 has a value of 110 ohms. The variable impedance element may be on the order of 200 ohms. When utilizing impedance values in this range the negative supply source, —E, may be 12 volts and the circuit will provide the desired counting action with variations from 9 to 15 volts. To this same end, the positive supply source, +E, may be plus 20 volts and the circuit will accommodate variations in this source from 16 to 24 volts. These circuit parameters are employed with transistor switching elements wherein the switching elements 16 and 22 comprise 2N1384 transistors while the switching element 36 is a 2N1605 device.

It will be further noted that in the event sufficient current cannot be derived from the positive terminal of the voltage source through the winding 14 for resetting the quantizing core 11, a separate winding, as shown in dotted outline, may be provided for the quantizing core 11 connected between the negative terminal and ground and will be effective for resetting the core from its positive state of remanence to its negative state immediately after it has been switched.

Now referring to FIG. 2 another embodiment of the magnetic flux counter will be described. This embodiment is essentially the same as the previously described embodiment, but has been modified in that only two windings are required for the counting core 12.

The general organization of the modified flux counter of FIG. 2 is similar to that previously described and, accordingly, the circuitry has been simplified whereby a pulse forming network is shown coupled between the pulse source 15 and the switching element 22. It should be

appreciated that the pulse forming network may be similar to the quantizing core circuit organization described hereinabove and which quantized pulses appear at the collector electrode for the switching element 22 for application to the input winding 32 for the counting core 12. The input winding 32 is similarly arranged with an impedance network comprising the resistive impedance elements 33 and 34 connected to the negative terminal of the power supply, —E. The switching element 36 is shown as a semiconductive switching element having its base electrode directly connected to a point intermediate the resistive elements 33 and 34, or the point "X" as shown. The emitter electrode is connected through the same type of network as shown for the first embodiment to the negative terminal of the power source. The collector electrode is also shown arranged in a similar fashion as in the previous embodiment whereby the output pulses are derived from the output terminal 50. In addition, an asymmetrical conducting device or a diode 55 is connected to a point intermediate the collector electrode of the switching element 22 and the associated input terminal of the input winding 32. The asymmetrical conducting element 55 is poled whereby its anode electrode is connected to the negative terminal —E.

The operation of this embodiment then, as previously mentioned, is essentially the same as described hereinabove. With the application of each pulse from the pulse source 15 to the pulse forming network, a quantized pulse is derived therefrom which causes the switching element 22 to be rendered conductive and thereby the quantized pulse is applied to the input winding 32 for stepping the magnetic core 12 along its hysteresis loop. As in the previous embodiment, the switching element 36 is normally maintained in a non-conductive condition during the stepping of the magnetic core 12 along its hysteresis loop due to the relative impedance values of the resistive elements 33 and 34. To this end, the resistive impedance elements are proportioned for the purposes of this embodiment to have a ratio on the order of 4:1 and, in a typical application wherein voltages are the same as in the previous embodiment, the —E terminal is a 12 volt terminal, the resistive element 33 may have an impedance value on the order of 200 ohms, while the resistive element 34 has an impedance value of 50 ohms. Accordingly, with these resistance ratios the voltage drop across the input winding 32 is such as to maintain the switching element 36 in a non-conductive condition in much the same fashion as the holding winding functioned in the previous embodiment. Stated differently, the voltage drop across the resistive element 34 is not sufficient to cause the switching element 36 to be rendered conductive while the core is switched between remanence points of its hysteresis loop.

When the magnetic core 12 reaches its point of saturation, the impedance of the input winding 32 drops to a very low value whereby the voltage across the resistive element 34 rises and is effective to cause the switching element 36 to be rendered conductive. The conduction of the switching element 36 causes a current to flow through the output winding 44 for resetting the magnetic core 12 to its opposite stable state. With the resetting action of the magnetic core 12 initiated, the feedback action causes the non-dot terminal of the input winding 32 to be driven positive with respect to the dot terminal and, therefore, the switching element 36 is maintained in its conductive state despite the conduction or non-conduction of the switching element 22 due to the action of the asymmetrical conductive device 55. Under these conditions, then, the diode 55 will be rendered conductive when the switching element 22 is correspondingly rendered non-conductive to maintain the conduction of the switching element 36 for the appropriate time to allow the complete resetting of the magnetic core 12. The diode 55 further functions to clamp the dot terminal of the input winding 32 to —E or 12 volts to assure the necessary conduction of the switching element 36.

It should now be appreciated that the flux counter of the present invention allows the tolerances on the magnetic cores to be relaxed in terms of the flux provided by each core and the matching of the cores and the impedance elements to allow greater operating margin to provide more stable counting action. This circuit configuration further allows optimizing the time the counting core saturates.

What is claimed is:

1. A counter comprising a quantizing magnetic core having a substantially rectangular hysteresis loop and at least an input and an output winding coupled to the core, a source of pulses to be counted, first normally non-conductive switching means coupled to said source and arranged to be rendered conductively responsive thereto for coupling the pulses to said input winding, impedance means coupled between said switching means and said input winding, second normally non-conductive switching means arranged to be rendered conductive in response to the signal induced in said output winding in response to the switching of the magnetic core from one magnetic stable state to another magnetic stable state to thereby provide quantized output pulses to be counted, circuit means coupled and arranged between said output winding and said second switching means, a counting magnetic core having a substantially rectangular hysteresis loop and an input, output, and a feedback winding coupled to the core, said input winding being connected to said second switching means for receiving the quantized pulses therefrom to step the counting core along its hysteresis loop from one stable state to the other stable state in preselected increments in response to each quantized pulse, impedance means connected in series circuit relationship with the input winding for said counting core and receiving said quantized pulses, third normally non-conductive switching means coupled between one of the terminals of each said output and feedback windings, the other terminal of said feedback winding being connected to said latter mentioned impedance means to maintain said third switching means non-conductive during the intervals the count core is being stepped between stable states and to be rendered conductive in response to the switching of the count core to the other stable state and thereby cause the count core to be reset to said one state, and means coupled to said third switching means for providing an output pulse from the count core only during the switching thereof from said other stable state back to said one state.

2. A counter as defined in claim 1 wherein said first and last mentioned impedance means are coupled to a source of potential and are proportioned to cause the quantized pulses coupled to the input winding of the counting core to have a substantially constant voltage-time characteristic even with normal changes in the potential from the source.

3. A counter comprising a quantizing magnetic core having a substantially rectangular hysteresis loop and at least an input and an output winding coupled to the core, a source of pulses to be counted, first normally non-conductive semiconductor switching means coupled to said source and arranged to be rendered conductively responsive thereto for coupling the pulses to said input winding, impedance means including a variable resistive impedance element having a preselected impedance value coupled between said switching means and said input winding, second normally nonconductive semiconductor switching means arranged to be rendered conductive in response to the signal induced in said output winding in response to the switching of the magnetic core from one magnetic stable state to another magnetic stable state to thereby provide quantized output pulses to be counted, circuit means coupled and arranged between said output winding and said second switching means, a counting

magnetic core having a substantially rectangular hysteresis loop and an input, output, and a feedback winding coupled to the core, said input winding being connected to said second switching means for receiving the quantized pulses therefrom to step the counting core along its hysteresis loop from one stable state to the other stable state in preselected increments in response to each quantized pulse, resistive impedance means having a preselected impedance value relative to the impedance value of the first mentioned impedance means connected in series circuit relationship with the input winding for said counting core and receiving said quantized pulses, said first and latter mentioned impedance means being connected to the same terminal of a power source, third normally non-conductive semiconductor switching means coupled between one of the terminals of each of said output and feedback windings, the other terminal of said feedback winding being connected to said latter mentioned impedance means for maintaining said third switching means non-conductive during the intervals the count core is being stepped between stable states and to be rendered conductive in response to the switching of the count core to the other stable state and thereby cause the count core to be reset to said one state, and means coupled to said third switching means for providing an output pulse from the count core only during the switching thereof from said other stable state back to said one state.

4. A counter as defined in claim 3 wherein said variable impedance element is controllable for setting the total count of the counter and the third semiconductor switching element is of the opposite conductivity type from the first and second semiconductor switching elements.

5. A magnetic core counter comprising a quantizing magnetic core having a substantially rectangular hysteresis loop and at least an input and an output winding coupled to the core, a source of pulses to be counted, first normally non-conductive switching means having an input, output, and control electrode, the input-control electrode circuit of said switching means is coupled to said source and arranged to be conductively responsive thereto, impedance means having a preselected impedance value coupled to the output electrode of said switching means and said input winding for coupling the pulses to said input winding, second normally non-conductive switching means having an input, output, and control electrode, the input-control electrode circuit of said second switching means is coupled to said output winding and is rendered conductive in response to the signal induced in said output winding in response to the switching of the magnetic core from one magnetic stable state to another magnetic stable state to thereby provide quantized output pulses to be counted, circuit means coupled and arranged between said output winding and the input-control electrodes of said second switching means, said latter mentioned means being connected to a source of power for resetting the quantizing core from said another state to said one state during the intervals between the receipt of pulses from said source, a counting magnetic core having a substantially rectangular hysteresis loop and an input, output and a feedback winding coupled to the core, said input winding being connected to the output electrode of said second switching means for receiving the quantized pulses therefrom to step the counting core along its hysteresis loop from one stable state to the other stable state in preselected increments in response to each quantized pulse, impedance means having a preselected impedance value relative to the impedance value of the first mentioned impedance means connected in series circuit relationship with the input winding for said counting core and receiving said quantized pulses, said first and latter mentioned impedance means being connected to the same terminal of a power source whereby the variations thereof are compensated for to thereby couple a pulse of a constant voltage-time product to the input winding of said count core, third normally non-conductive switching means having input, output, and control electrodes, said output-control electrode circuit is coupled between one of the terminals of each of said output and feedback windings, the input electrode circuit of said third switching means being connected to said same terminal of the power source, the other terminal of said feedback winding being connected to said latter mentioned impedance means to maintain said third switching means non-conductive during the intervals the count core is being stepped between stable states and to be rendered conductive in response to the switching of the count core to the other stable state and thereby cause the count core to be reset to said one state, and means coupled to the output electrode of said third switching means for providing an output pulse from the count core only during the switching thereof from said other stable state back to said one state.

6. A magnetic core counter as defined in claim 5 wherein said switching elements are transistor switching elements and said first and last mentioned impedance means include resistive impedance elements and the first mentioned impedance means further includes a manually adjustable resistive impedance element.

7. A counter as defined in claim 6 wherein said first mentioned impedance means is proportioned to have an impedance value for compensating for any excessive conduction time of the first transistor switching means.

8. A counter comprising a quantizing magnetic core having a substantially rectangular hysteresis loop and at least an input and an output winding coupled to the core, a source of pulses to be counted, first normally non-conductive switching means coupled to said source and arranged to be rendered conductively responsive thereto for coupling the pulses to said input winding, impedance means having a preselected impedance value coupled between said switching means and said input winding, second normally non-conductive switching means arranged to be rendered conductive in response to the signal induced in said output winding in response to the switching of the magnetic core from one magnetic stable state to another magnetic stable state to thereby provide quantized output pulses to be counted, circuit means coupled and arranged between said output winding and said second switching means to render said switching means conductively responsive to said switching of the quantizing core only from said one state to said another state, a counting magnetic core having a substantially rectangular hysteresis loop and an input and output winding coupled to the core, said input winding being connected to said second switching means for receiving the quantized pulses therefrom to step the counting core along its hysteresis loop from one stable state to the other stable state in preselected increments in response to each quantized pulse, impedance means connected in series circuit relationship with the input winding for said counting core and receiving said quantized pulses, third normally non-conductive switching means coupled between one of the terminals of said output winding and said latter mentioned impedance means to maintain said third switching means non-conductive during the intervals the count core is being stepped between stable states and to be rendered conductive in response to the switching of the count core to the other stable state and thereby cause the count core to be reset to said one state, circuit means coupled to said input winding and responsive to the saturated condition of the core when it reaches its other stable state during the switching of the count core to the other stable state to aid in maintaining the third switching means conductive during the resetting thereof, and means coupled to said third switching means for providing an output pulse from the count core only during the switching thereof from said other stable state back to said one state.

9. A counter comprising a quantizing magnetic core having a substantially rectangular hysteresis loop and at least an input and an output winding coupled to the core,

a source of pulses to be counted, first normally non-conductive switching means coupled to said source and arranged to be rendered conductively responsive thereto for coupling the pulses to said input winding, impedance means having a preselected impedance value coupled between said switching means and said input winding, second normally non-conductive switching means arranged to be rendered conductive in response to the signal induced in said output winding in response to the switching of the magnetic core from one magnetic stable state to another magnetic stable state to thereby provide quantized output pulses to be counted, circuit means coupled and arranged between said output winding and said second switching means to render said switching means conductively responsive to said switching of the quantizing core only from said one state to said another state, a counting magnetic core having a substantially rectangular hysteresis loop and an input and output winding coupled to the core, said input winding being connected to said second switching means for receiving the quantized pulses therefrom to step the counting core along its hysteresis loop from one stable state to another stable state in preselected increments in response to each quantized pulse, asymmetrical conducting means connected to a point intermediate said input winding and said second switching means and arranged to be rendered conductive in response to the resetting of the counting core from said another stable state to the one stable state, impedance means connected in series circuit relationship with the input winding for said counting core and receiving said quantized pulses, third normally non-conductive switching means coupled between one of the terminals of said output winding and said latter mentioned impedance means to maintain said third switching means non-conductive during the intervals the count core is being stepped between stable states and to be rendered conductive in response to the switching of the count core to said another stable state and thereby cause the count core to be reset to said one state, and means coupled to said third switching means for providing an output pulse from the count core only during the switching thereof from said another stable state back to said one state.

10. A magnetic core counter comprising a quantizing magnetic core having a substantially rectangular hysteresis loop and at least an input and an output winding coupled to the core, a source of pulses to be counted, first normally non-conductive switching means having an input, output, and control electrode, the input-control electrode circuit of said switching means is coupled to said source and arranged to be conductively responsive thereto, impedance means having a preselected impedance value coupled to the output electrode of said switching means and said input winding for coupling the pulses to said input winding, second normally non-conductive switching means having an input, output, and control electrode, the input-control electrode circuit of said second switching means is arranged to be rendered conductive in response to the signal induced in said output winding in response to the switching of the magnetic core from one magnetic stable state to another magnetic stable state to thereby provide quantized output pulses to be counted, circuit means coupled and arranged between said output winding and said second switching means to render said switching means conductively responsive to said switching of the quantizing core only from said one state to said another state, said latter mentioned means being connected to a source of power for resetting the quantizing core from said another state to said one state during the intervals between the receipt of pulses from said source, a counting magnetic core having a substantially rectangular hysteresis loop and at least an input and an output winding coupled to the core, said input winding being connected to the output electrode of said second switching means for receiving the quantized pulses therefrom to step the counting core along its hysteresis loop from one stable state to another stable state in preselected increments in response to each quantized pulse, impedance means proportioned to have a preselected impedance value relative to the impedance value of the first mentioned impedance means connected in series circuit relationship with the input winding for said counting core and receiving said quantized pulses, said first and latter mentioned impedance means being connected to the same terminal of a power source whereby the variations thereof are compensated for to thereby couple a pulse of a constant voltage-time product to the input winding of said count core, third normally non-conductive switching means having input, output, and control electrodes, said output-control electrode circuit is coupled to one of the terminals of said output winding, the input-control electrode circuit of said third switching means being connected between said latter mentioned impedance means to maintain said third switching means non-conductive during the intervals the count core is being stepped between stable states and to be rendered conductive in response to the switching of the count core to said another stable state and said same terminal of the power source to thereby cause the count core to be reset to said one state, circuit means coupled to said input winding and responsive to the saturated condition of the core when it reaches said another stable state during the switching of the count core to the other stable state to be rendered conductive to aid in maintaining the third switching means conductive during the resetting thereof, and means coupled to the output electrode of said third switching means for providing an output pulse from the count core only during the switching thereof from said another stable state back to said one state.

11. A magnetic core counter as defined in claim **10** wherein said latter mentioned circuit means comprises an asymmetrical conductive element coupled between the output electrode of said second switching means and to said same terminal of the power source.

References Cited by the Examiner

UNITED STATES PATENTS

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ARTHUR GAUSS, *Primary Examiner.*

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,201,605 August 17, 1965

Edwin S. Lee III

It is hereby certified that error appears in the above numbered patent requiring correction and that the said Letters Patent should read as corrected below.

Column 10, lines 49 and 50, for "secand" read -- second --; column 12, line 42, for "other" read -- one ---.

Signed and sealed this 1st day of February 1966.

(SEAL)
Attest:

ERNEST W. SWIDER
Attesting Officer

EDWARD J. BRENNER
Commissioner of Patents