



(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

ADAPTIVE SLOPE COMPENSATION FOR CURRENT MODE SWITCHING POWER SUPPLY

5 FIELD OF THE INVENTION

This invention relates to slope compensation circuits for current mode switching power supplies, such as voltage regulators, and in particular to an adaptive slope compensation circuit.

BACKGROUND

10 A conventional current mode voltage regulator includes a current feedback loop and a voltage feedback loop for controlling the peak instantaneous current through a transistor switch for each switching cycle to regulate the output voltage. The duty cycle of the transistor switch is controlled by the feedback paths to regulate the voltage. It is well known that operating at a duty cycle near or above 50% can result in oscillations of
15 the duty cycle and output voltage in response to perturbations in the load or the input voltage. For example, in response to a perturbation, the duty cycle may continue to oscillate between two values in alternate switching cycles, referred to as a sub-harmonic oscillation.

Fig. 1 shows an example of a current mode voltage regulator without any slope
20 compensation. The solid waveform 6 represents the instantaneous inductor current at a duty cycle of about 70% when the regulator is operating properly. The transistor switch is turned on at the beginning of a switching cycle and turned off when the instantaneous inductor current crosses a current threshold I_{th} , set by an error amplifier receiving an output voltage feedback signal. If there is a perturbation in the load or input voltage, the
25 duty cycle reacts to the perturbation, which creates the dashed line instantaneous inductor current waveform 8. As seen, the duty cycle then fluctuates and may settle into an oscillation pattern where the duty cycle changes each switching cycle while trying to maintain the proper peak current. This creates significant ripple in the output voltage.

The typical current mode regulator includes a slope compensation circuit that
30 dampens such duty cycle oscillations. In one example, the current threshold (in the

voltage feedback path), used for determining when to turn the transistor switch off, is modulated by the same downward ramp signal for each switching cycle to provide slope compensation. Such a technique works but the slope compensation is fixed by the circuit designer, where the designer optimizes the slope compensation for a particular set of
5 likely off-chip components to be selected by the user and for a particular duty cycle. Therefore, even though the duty cycle perturbations may be eventually dampened, the number of switching cycles needed for the damping in actual operation is variable. Additionally, with fixed slope compensation, the load current perturbation may be such that the duty cycle perturbation is never damped or the duty cycle goes into an oscillating
10 pattern. This is a significant problem when a constant output voltage is important. If the slope compensation is higher than necessary, the behavior of the converter may exhibit characteristics of voltage mode control, hence voiding the advantages of current mode control.

In a similar type of slope compensation circuit, the instantaneous current feedback
15 signal, rather than the current threshold, is adjusted by a fixed upward slope compensation. Since the transistor switch shuts off when the rising instantaneous current signal crosses the current threshold, the slope compensation can either modulate the current threshold with a downward ramp or modulate the instantaneous current signal with an upward ramp.

20 Other types of slope compensation circuits may be adaptive and receive information from the regulator to adjust the slope compensation to be more optimal. However, such circuits tend to be complex and hence use up valuable chip area and power. In some examples, the adaptive slope compensation circuit requires a microprocessor.

25 What is needed is a compact adaptive slope compensation circuit that uses very little area and power yet adjusts the slope compensation so that perturbations in the duty cycle are damped within only one cycle or only a few cycles.

SUMMARY

In the preferred embodiment, an adaptive slope compensation circuit adjusts the
30 instantaneous current feedback signal of a current mode regulator.

A rising first ramp signal, independent of the instantaneous inductor current, is generated at the start of each switching cycle, where the first ramp signal always has the same slope. This first ramp signal, when used for slope compensation, may adequately damp any duty cycle perturbations, but the number of cycles needed for the damping
5 would be generally unpredictable (like the prior art) since the number of cycles needed for the damping depends on the external components (typically selected by the user for a particular application) and the duty cycle. When a highly stable output voltage is desired, such a relatively slow damping time may not be adequate.

This first ramp signal is then compensated by a compensation circuit to create a
10 compensated ramp signal. The compensation changes as the duty cycle changes and will be different for different external components (e.g., inductors, loads, etc.) selected by the user. As such, the compensation is adaptive.

The compensated ramp signal is then added to the actual instantaneous current feedback signal, to create a compensated current feedback signal, for application to a
15 comparator to determine when to turn off the transistor switch. A threshold level is applied to the other input of the comparator. The up-slope and down-slope of the compensated current feedback signal are detected for each switching cycle. The slope values are processed by simple circuits to generate subsequent compensated ramp signals for subsequent switching cycles.

20 The compensation circuit forces the compensated current feedback signal (applied to the comparator) to have an up-slope greater than the absolute value of its down-slope for duty cycles near and above 50%. (For duty cycles greater than 50%, the up-slope of the actual (uncompensated) inductor current is lower than the absolute value of its down-slope.) With these characteristics, there will be rapid dampening of any perturbation of
25 any duty cycle due to, for example, a load current change. Such damping can then occur within a single switching cycle after the load current perturbation.

In one embodiment, the circuit uses a differentiator, for generating up and down-slope values, and uses sample and hold circuits for providing the up and down slopes of the instantaneous current signal to downstream circuitry to generate the compensation
30 signal for the first ramp signal. An averaging circuit is used to average the slopes over one or a few switching cycles to smooth out the compensation of the first ramp signal.

In another embodiment, further compensation is added to the instantaneous current feedback signal to compensate for the small ripple in the threshold signal applied to the comparator. The small ripple is due to the ripple of the output voltage of the converter at the switching frequency. Such ripple in the threshold signal may induce instabilities and could further aggravate duty cycle perturbations. With such added compensation, any inaccuracy due to ripple in the threshold signal is compensated for, resulting in faster damping of duty cycle perturbations in the event of disturbances applied to the converter.

The circuitry used for the adaptive slope compensation circuit takes up less area than the prior art adaptive slope compensation circuits and uses less power.

Simulation results are shown.

Various other embodiments are described.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates an instantaneous inductor current in a current mode voltage regulator without any slope compensation, where an ideal waveform is shown in solid lines and a varying duty cycle waveform is shown in dashed lines due to a perturbation in the load or input voltage.

Fig. 2 illustrates one embodiment of the slope compensation circuit of the present invention within a current mode buck converter.

Figs. 3A-3H are examples of waveforms generated at various nodes in the circuit of Fig. 2 taken from a computer simulation.

Figs. 4A-4E illustrate simplified waveforms with annotations to help understand the functional circuit of Fig. 4F, where Fig. 4A is similar to Fig. 3A; Fig. 4B is similar to Fig. 3B; Fig. 4C is similar to Fig. 3H; Fig. 4D is similar to Fig. 3C; and Fig. 4E is similar to Fig. 3D (but inverted).

Fig. 4F illustrates a simplified circuit functionally showing the processing of the slope values identified in Fig. 4D to obtain the proper relationship between the up-slope and down-slope of the compensated inductor current signal.

Figs. 5A-5D are examples of waveforms generated, using computer simulation, at various nodes in the circuit of Fig. 2 in response to the load transient shown in Fig. 5A.

Fig. 6 illustrates a more general depiction of the slope compensation circuit applied to any type of current mode switching power supply, such as a boost or buck
5 voltage regulator.

Fig. 7 illustrates another embodiment of a slope compensation circuit where the “uncompensated” ramp signal is only generated while the transistor switch is on.

Figs. 8A-8D are similar to Figs. 4A-4D but are presented to show how the threshold voltage has a ripple, due to the output voltage having a ripple. The waveforms
10 are annotated to help understand the functional circuit of Fig. 8E.

Fig. 8E illustrates a simplified circuit functionally showing the processing of the slope values identified in Fig. 8D to obtain the proper relationship between the up-slope and down-slope of the compensated inductor current sense voltage while taking into account the ripple in the threshold voltage.

Fig. 9 illustrates the compensation waveform added to the inductor current sense voltage, where one waveform does not take into account the ripple in the threshold voltage and the other waveform takes into account the ripple in the threshold voltage.
15

Fig. 10 illustrates a converter circuit that is the same as that shown in Fig. 2 except a threshold voltage ripple compensation circuit has been added.

20 Elements that are the same or equivalent are labeled with the same numeral.

DETAILED DESCRIPTION

Fig. 2 is an actual simulation circuit diagram representing an embodiment of the slope compensation circuit being used with an otherwise conventional current mode buck voltage regulator. The nomenclature used in the actual simulated circuit will be used to
25 identify the various elements. The slope compensation portion 12 may be used with many other types of current mode switching circuits, including boost, buck-boost, current regulation, etc.

The overall regulator 14 receives an input voltage V_1 and outputs a regulated output voltage V_{out} . When the MOSFET M1 is turned on by the high Q output of the reset/set (RS) flip-flop A1, current flows through the low value sense resistor R5 and inductor L1 to charge the output capacitor C1 for delivering current to the load R7 at the regulated output voltage V_{out} . The instantaneous ramping current causes a voltage drop across the sense resistor R5, which is sensed by the differential amplifier E1. The current sense voltage (V_{sense}) of the amplifier E1 is thus proportional to the instantaneous inductor current i_L . Many other types of conventional current sensors may be used, including a sensor in the MOSFET M1 itself. Fig. 3A illustrates an example of the Q output of the RS flip-flop A1, and Fig. 3B illustrates an example of the current sense voltage V_{sense} output of the differential amplifier E1, corresponding to the instantaneous inductor L1 current. The voltage V_{sense} is then compensated by a controllable voltage source B1, in series with the voltage V_{sense} , whose voltage is determined by the slope compensation circuit 12. The compensated voltage ($V_{sense} + B1$ voltage) is then applied to an input of a comparator A2. The controllable voltage source B1 may be a voltage source in series between the amplifier E1 and the comparator A2 or may be an adder that adds the voltage V_{sense} to the B1 voltage. In either case, the B1 voltage is summed with the voltage V_{sense} .

The regulator's output voltage V_{out} is divided by a resistor divider (resistors R1 and R2) to provide a feedback voltage V_{fb} that is equal to a reference voltage V_2 when the desired level of the output voltage V_{out} is obtained. The regulator tries to keep V_{fb} equal to V_2 by adjusting a threshold voltage V_{th} , and hence the duty cycle of the MOSFET M1.

The feedback voltage V_{fb} and the reference voltage V_2 are applied to inputs of a transconductance error amplifier G1. A resistor/capacitor circuit (resistor R3 and capacitor C2) converts the current output of the error amplifier G1 to a threshold voltage V_{th} that is applied to the comparator A2. When V_{fb} equals V_2 , the output of the error amplifier G1 is zero current, so the threshold voltage V_{th} stays the same and the duty cycle does not change.

When the compensated voltage ($V_{sense} + B1$ voltage) is rising and crosses the threshold voltage V_{th} , the comparator A2 is tripped and outputs a short pulse, which

resets the RS flip-flop A1 and turns off the MOSFET M1 for the remainder of the switching cycle.

When the MOSFET M1 is off, the diode D1 become forward biased, and the ramping down inductor L1 current flows through the diode D1 and to the output capacitor C1 and load R7.

The clock signal CLK (a short pulse) then sets the RS flip-flop A1 at the beginning of the next cycle, and the process repeats. The CLK frequency may be, for example, 100kHz.

The slope compensation circuit 12 will now be described. The slope compensation circuit 12, along with other circuitry, generates the voltage generated by the voltage source B1 for summing with the voltage Visense to create the compensated current sense voltage ($V_{\text{sense}} + B1$ voltage).

A ramp generator 16 is triggered by a high CLK pulse (which also sets the RS flip-flop A1), which generates an up-ramping voltage Vramp at the same time that the instantaneous current through the inductor L1 is ramping up. The slope of the output of the ramp generator 16 is determined by the components used to create the ramp generator 16. The high CLK pulse (e.g., 10ns) briefly closes a switch S1 to discharge the capacitor C4 voltage to zero, followed by a current source I1 charging the capacitor C4 to create a ramping voltage (Vramp). Vramp will be modulated by a compensation signal, as discussed below, to create the B1 voltage.

An input of a differentiator circuit 20 is coupled to the compensated current sense voltage ($V_{\text{sense}} + B1$ voltage) for differentiating the compensated current sense voltage ($V_{\text{sense}} + B1$ voltage). The differentiator circuit 20 comprises a capacitor C7, a differential amplifier G2, and a feedback resistor R6. The output of the differentiator circuit 20 is a signal proportional to the slope of the compensated current sense voltage ($V_{\text{sense}} + B1$ voltage). The compensated current sense voltage ($V_{\text{sense}} + B1$ voltage) ramps up with a slope m_1 (Fig. 4B) when the MOSFET M1 is on and ramps down with a slope m_2 (Fig. 4B) when the MOSFET M1 is off.

The output of the differentiator circuit 20 is applied to the inverting input of a first sample and hold circuit A5 and applied to the non-inverting input of a second sample and

hold circuit A3. The first sample and hold circuit A5 is clocked by the Q output of the RS flip-flop A1, and the second sample and hold circuit A3 is oppositely clocked by the inverted Q output of the RS flip-flop A1. A driver A4 provides the clock signals to the sample and hold circuits A3 and A5. In the preferred embodiment, a slight delay in the
 5 clocking (e.g., 200nsec) is used to avoid any sampling of switching noise. Thus, the sample and hold circuit A5 outputs a voltage $V_{up-slope}$ corresponding to the up slope of the compensated current sense voltage ($V_{sense} + B1$ voltage), and the sample and hold circuit A3 outputs a voltage $V_{down-slope}$ corresponding to the down slope of the compensated current sense voltage ($V_{sense} + B1$ voltage). The polarity of $V_{up-slope}$ is
 10 reversed since the up slope signal is inverted by the sample and hold circuit A5.

Fig. 3D illustrates the up and down slope values applied to the sample and hold circuits A5 and A3 respectively. Fig. 3E illustrates the alternate clocking of the sample and hold circuits A5 and A3. Fig. 3F illustrates the absolute value held $V_{up-slope}$ and $V_{down-slope}$ signals that are output by the sample and hold circuits A5 and A3.

15 The voltage $V_{down-slope}$ is then subtracted from the voltage $V_{up-slope}$ (both have the same polarity) by a subtractor G3, which outputs a current proportional to the difference between the absolute values of the up slope and down slope of the compensated current sense voltage ($V_{sense} + B1$ voltage). The current is converted to a voltage by the voltage drop across the resistor R4 to generate the slope error voltage V_{se} .

20 Fig. 3F illustrates the voltage V_{se} resulting from the subtraction of the $V_{down-slope}$ from the $V_{up-slope}$.

The voltage V_{se} is applied to a transconductance amplifier G4. A constant DC offset voltage generated by a voltage source V4 is applied to another input of the amplifier G4 for subtracting the voltage V_{se} from the offset voltage and amplifying the
 25 difference. In one embodiment, the offset voltage is 30mV. In steady state operation, the output of the amplifier G4 is zero. The output of the amplifier G4 may be a positive or negative current depending on whether the voltage V_{se} is greater or less than the offset voltage.

The output of the amplifier G4 is a current corresponding somewhat to the
 30 difference between the up slope and down slope of the compensated current sense voltage ($V_{sense} + B1$ voltage). This current charges a capacitor C5 to a certain slope

compensation-compensation voltage V_{sc} . The small capacitor C5 (e.g., 100pF) serves to average the voltage V_{sc} over one or a few cycles. An example of the voltage V_{sc} waveform is shown in Fig. 3G. The adaptive value of V_{sc} ensures that the up-slope of the compensated current sense voltage ($V_{sense} + B1$ voltage) will always be greater than
 5 the absolute value of the down-slope of the compensated current sense voltage ($V_{sense} + B1$ voltage). This ensures rapid damping of any duty cycle perturbations.

The diode D2 ensures the value of V_{sc} does not go negative.

The offset voltage (e.g., 30mV), by the voltage source V4, causes the up-slope of the compensated current sense voltage ($V_{sense} + B1$ voltage) to be greater than the
 10 absolute value of its down-slope by the corresponding offset voltage amount. For example, if the up-slope corresponded to 100mV, the down-slope would correspond to 70mV. The voltages are proportional to the slope. A lower offset voltage would still work, but the perturbations in the duty cycle would take longer to settle.

For duty cycles below a certain value (somewhat below 50%), the voltage V_{se}
 15 will be sufficiently positive that the output of the amplifier G4 will be negative, and there will be no compensation of the voltage V_{sense} . This is because there is inherently good damping of duty cycle perturbations for duty cycles below 50%.

The voltage V_{ramp} (generated by the ramp generator 16) is multiplied by the voltage V_{sc} using a multiplier 24 to generate the B1 voltage ($V_{ramp} * V_{sc}$). The B1
 20 voltage is then added to the current sense voltage V_{sense} , as previously described, to compensate the voltage V_{sense} .

Fig. 3H shows the B1 voltage ($V_{ramp} * V_{sc}$). Fig. 3C shows the compensated current sense voltage ($V_{sense} + B1$ voltage) applied to the comparator A2, which is compared to the threshold voltage V_{th} .

25 Under these conditions, the slope compensation completely corrects for duty cycle perturbations on the next switching cycle or within just a few switching cycles. The slope compensation increases with the duty cycle near or above 50%, since the voltage V_{sc} becomes greater and greater (up to a limited value) as the up-slope of the voltage V_{sense} becomes less than the absolute value of the down-slope of the current sense voltage

Visense. As a result, there is no overcompensation at duty cycles near or above 50%, in contrast to prior art fixed slope compensation ramps.

Simulations have shown the circuit of Fig. 2 to damp duty cycle oscillations down to one cycle.

5 Many other techniques may be used to implement the present invention.

Figs. 4A-4E are simplified waveforms with annotations used for better explaining the functional circuit of Fig. 4F.

Fig. 4A illustrates a Q signal waveform output from the RS flip-flop A1 of Fig. 2. This particular pattern of the Q signals results in a ramping instantaneous inductor current
 10 corresponding to the voltage Visense output (Fig. 4B) from the amplifier E1. The up-slope has a sampled slope of m_1 (which can be considered as a voltage corresponding to the absolute value of the slope), and the down-slope has a sampled slope of m_2 . At duty cycles greater than 50%, the up-slope m_1 is less than the down-slope m_2 .

Based on the held slopes and the processing performed in Fig. 2, the voltage
 15 generated by the voltage source B1 is shown in Fig. 4C, with the up-slope having a slope of m_a .

Fig. 4D illustrates the sum of the voltage Visense and the output of the voltage source B1 (where the sum is applied to the comparator A2) and shows that the up-slope has a slope of m_1+m_a , and the down-slope has a slope of m_2-m_a . Fig. 4D also shows the
 20 voltage V_{th} applied to another input of the comparator A2. The slope compensation circuit 12 forces the up-slope of the combined voltages to always be greater than the down-slope for at least duty cycles near or above 50% to ensure any duty cycle perturbations are damped quickly. Below a 50% duty cycle of the MOSFET M1, the up-slope of the actual inductor current is naturally greater than the down-slope, so
 25 compensation is not needed.

Fig. 4E shows the corresponding slopes of the waveform of Fig. 4D after the differentiation and sample/hold of the differentiated signal. Note that the feedback forces (m_1+m_a) to be always be greater than $(|m_2|-m_a)$.

The functional performance of the slope compensation circuit of Fig. 2 is shown in Fig. 4F, where the adder 30, subtractors 32 and 34, amplifier 36, and the negative feedback connections cause the following to be true: $(m_1 + m_a) > (|m_2| - m_a)$. This ensures that the duty cycle will be damped within one or a few cycles of a perturbation.

5 Figs. 5A-5D show waveforms from a simulation of the circuit of Fig. 2 in response to a load perturbation.

Fig. 5A shows a large load current transient between 6.9A and about 3.3A, where the MOSFET M1 of Fig. 2 is switching at a duty cycle greater than 50%. Such a perturbation would normally cause a perturbation of the duty cycle.

10 Fig. 5B shows the resulting fluctuation of the voltage V_{sc} .

Fig. 5C shows the fluctuation in the inductor current in response to the load current perturbation.

Fig. 5D shows the rapid recovery of the output voltage V_{out} , where the duty cycle perturbation has been damped out at about the same time as the load current stabilized.

15 The slope compensation portion of the converter of Fig. 2 can be used in many other types of converters. Fig. 6 illustrates the slope compensation circuit 12 (generating V_{sc}) and the ramp generator 16 (generating V_{ramp}) connected to a multiplier 24, whose output controls the voltage source B1 to generate the value $V_{ramp} * V_{sc}$. This value is added to the V_{sense} signal and applied to an input of the comparator A2. The error
20 amplifier G1 receives the feedback voltage V_{fb} and the reference voltage V_{ref} (voltage V2 in Fig. 2), and the resulting signal is applied to the other input of the comparator A2. The output of the comparator A2 resets the RS flip-flop A1 for regulating the peak current of the MOSFET M1 or any other type of transistor switch. The duty cycle of the MOSFET M1 is controlled to achieve a regulated output signal, which in the example is a
25 regulated output voltage V_1 . An output current can instead be regulated by feeding back an output current signal.

Fig. 7 illustrates an alternative embodiment of the circuit of Fig. 2 where the ramp generator 16 is triggered by the Q output of the RS flip-flop A1 rather than the CLK signal. This results in a voltage V_{ramp} that ramps up when the MOSFET M1 is on and is

zero when the MOSFET M1 is off. This difference changes the voltage source B1 voltage to a value of $(0.2 \cdot V_{\text{ramp}} \cdot \max(0.5V \text{ or } V_{\text{sc}}))$. The fractional value of 0.2 is determined based on the particular circuitry used and can be determined by computer simulation.

- 5 In another embodiment, the voltage threshold signal from the error amplifier G1 is compensated by using a slope compensation signal that is opposite to the slope compensation signal of Fig. 4C. Such compensation is generated in basically the same way as described with respect to Fig. 2.

The feedback circuit for calculating slope compensation could additionally make
10 use of the voltage ripple on the threshold voltage V_{th} , applied to the comparator A2, to further improve the compensation. The threshold voltage V_{th} has some small ripple since the output voltage V_{out} has ripple at the switching frequency. The example waveform of Fig. 4D assumed that the threshold voltage V_{th} was constant, which may not be the case.

- Figs. 8A-8D illustrate waveforms where the threshold voltage V_{th} has ripple.
15 Figs. 8A-8C are identical to Figs. 4A-4C. Fig. 8D shows the ripple of the threshold voltage V_{th} greatly exaggerated. The actual ripple would also be smoother. The waveforms are annotated, where the up-slope of V_{sense} is m_1 (a voltage corresponding to the absolute value of the slope), the down-slope of V_{sense} is m_2 , the up-slope of the B1 voltage is m_a , and the up-slope of V_{th} is m_{vth} . The angle between V_{th} and the up-
20 slope of the compensated current sense voltage ($V_{\text{sense}} + \text{B1 voltage}$) is α , and the angle between V_{th} and the down-slope of the compensated current sense voltage ($V_{\text{sense}} + \text{B1 voltage}$) is β .

- The functional performance of the slope compensation circuit that performs the function of the circuit of Fig. 2, as well as takes into account the threshold voltage ripple,
25 is shown in Fig. 8E, where the adder 30, subtractors 32, 34, 38, amplifier 36, and the negative feedback connections cause the following to be true. Stability criteria for current mode control is $\alpha > \beta$, which translates to $(m_1 + m_a) > (|m_2| - m_a)$ if V_{th} is at a DC level. As the equivalent series resistance (ESR) of the output capacitor C1 is increased, or the capacitance is reduced, V_{th} exhibits a greater voltage ripple. Hence, additional
30 compensation by the B1 voltage (greater up-slope m_a) is needed. The circuit of Fig. 8E subtracts the m_{vth} up-slope from the output of the amplifier 36, which forces the feedback

loop to increase m_a . This further ensures that the duty cycle will be damped within one or a few cycles of a perturbation irrespective of the ripple in the threshold voltage V_{th} .

Fig. 9 illustrates waveforms obtained by computer simulation showing the B1 voltage (for compensating the voltage V_{sense}) generated by the circuit of Fig. 2 (waveform 50) compared with the B1 voltage generated by the circuit of Fig. 10 (waveform 52) which additionally uses the V_{th} voltage ripple in determining the B1 voltage. Note that the waveform 52 provides more compensation to V_{sense} due to the V_{th} ripple.

Fig. 10 shows the circuit of Fig. 2 augmented with a circuit that uses the threshold voltage V_{th} ripple to augment the B1 voltage. The circuit of Fig. 10 includes an additional differentiator circuit 56 and sample and hold circuit A6 to generate the slope m_{vth} (a voltage corresponding to the threshold voltage slope). The slope is then applied to the non-inverting input of the sample and hold circuit A5 as well as to the inverting input of the sample and hold circuit A3.

This effectively will reduce the voltage V_{se} and increase the voltage V_{sc} to increase the amount of compensation. The differentiator 56 is conventional and is formed of the differential amplifier E2, capacitors C6 and C5, resistor R8, and subtractor G5.

Many other circuit configurations may be used to carry out the inventive technique.

While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modifications that are within the true spirit and scope of this invention.

CLAIMS

What is claimed is:

1. A current mode switching converter comprising:
 - a transistor switch;
 - 5 an inductor configured to conduct a ramping inductor current as the transistor switch is turned on and off at a particular duty cycle;
 - a current sensor configured to convert the ramping inductor current to a corresponding current sense signal, the current sense signal having an up-slope portion with a first slope and having a down-slope portion with a second slope, 10 wherein, at duty cycles greater than 50%, the first slope is less than an absolute value of the second slope;
 - a ramp generator configured to generate a ramp voltage while the current sense signal has the first slope;
 - an adaptive slope compensation circuit configured to generate a 15 compensation voltage for the ramp voltage to create a compensated ramp voltage;
 - a combining circuit configured to sum the compensated ramp voltage with the current sense signal to create a compensated current sense signal;
 - a threshold voltage generator configured to generate a threshold voltage for determining a peak current through the inductor; and
 - 20 a comparator configured to receive the compensated current sense signal and the threshold voltage for determining when to turn off the transistor switch,
 - wherein the adaptive slope compensation circuit forces the compensated current sense signal to have an up-slope greater than an absolute value of its down-slope at least for duty cycles greater than 50%.
- 25 2. The converter of Claim 1 wherein the adaptive slope compensation circuit comprises:

a first differentiator circuit configured to convert the compensated current sense signal to a first up-slope voltage and a first down-slope voltage;

a first sample and hold circuit configured to sample and hold the first up-slope voltage;

5 a second sample and hold circuit configured to sample and hold the first down-slope voltage; and

a processing circuit coupled to output terminals of the first sample and hold circuit and the second sample and hold circuit, the processing circuit configured to process the first up-slope voltage and the first down-slope voltage to
10 derive a first compensation signal that compensates the ramp voltage to generate the compensated ramp voltage.

3. The converter of Claim 2 wherein the processing circuit comprises:

a first subtractor having inputs coupled to the output terminals of the first sample and hold circuit and the second sample and hold circuit, the first subtractor
15 configured to generate a first current across a first resistance to generate a first voltage; and

a transconductance amplifier having inputs coupled to receive the first voltage and an offset voltage, the amplifier being configured to generate a second current for charging and discharging a first capacitor to generate the compensation
20 voltage at the first capacitor to compensate the ramp voltage to create the compensated ramp voltage.

4. The converter of Claim 2 wherein the threshold voltage has ripple, the converter further comprising:

a second differentiator circuit configured to convert the threshold voltage
25 to a second up-slope voltage and a second down-slope voltage; and

a third sample and hold circuit configured to sample and hold the second up-slope voltage, wherein an output of the third sample and hold circuit is further

used to derive the compensation voltage for the ramp voltage to create the compensated ramp voltage.

5 5. The converter of Claim 4 wherein the output of the third sample and hold circuit is coupled to an input of the first sample and hold circuit for combining with the first up-slope voltage corresponding to an up-slope of the compensated current sense signal.

 6. The converter of Claim 2 further comprising:

 a reset/set flip-flop having a set input terminal coupled to receive a clock pulse and having an output terminal configured to generate an on-signal for the transistor switch when the reset/set flip-flop is set by the clock pulse,

 wherein the first sample and hold circuit is clocked by the clock pulse.

 7. The converter of Claim 6 wherein the first sample and hold circuit is clocked by a non-inverted clock pulse, and the second sample and hold circuit is clocked by an inverted clock pulse.

15 8. The converter of Claim 2 further comprising:

 a reset/set flip-flop having a set input terminal coupled to receive a clock pulse and having an output terminal configured to generate an on-signal for the transistor switch when the reset/set flip-flop is set by the clock pulse,

 wherein the first sample and hold circuit has a clock terminal coupled to the output terminal of the reset/set flip-flop so as to be clocked with the on-signal.

 9. The converter of Claim 8 wherein the first sample and hold circuit is clocked by a non-inverted on-signal, and the second sample and hold circuit is clocked by an inverted on-signal.

 10. The converter of Claim 1 wherein the adaptive slope compensation circuit is configured so that the compensation voltage increases as the duty cycle exceeds 50%.

 11. The converter of Claim 1 further comprising a multiplier coupled to the compensation voltage and the ramp voltage to generate the compensated ramp voltage.

12. The converter of Claim 1 wherein the converter comprises a current mode buck converter.

13. The converter of Claim 1 wherein the adaptive slope compensation circuit is configured to damp duty cycles perturbations in response to a load current perturbation
5 within one switching cycle after the load current perturbation has ceased.

14. The converter of Claim 1 wherein the adaptive slope compensation circuit is configured to damp duty cycles perturbations in response to a load current perturbation within two switching cycles after the load current perturbation has ceased.

15. The converter of Claim 1 wherein the adaptive slope compensation circuit
10 is configured to damp duty cycles perturbations in response to a load current perturbation within three switching cycles after the load current perturbation has ceased.

16. A method performed by a current mode switching converter comprising:

controlling a transistor switch at a duty cycle;

conducting a ramping inductor current, through an inductor, as the
15 transistor switch is turned on and off at the duty cycle;

converting the ramping inductor current to a corresponding current sense signal, by a current sensor, the current sense signal having an up-slope portion with a first slope and having a down-slope portion with a second slope, wherein, at duty cycles greater than 50%, the first slope is less than an absolute value of the
20 second slope;

generating a ramp voltage, by a ramp generator, while the current sense signal has the first slope;

generating a compensation voltage for the ramp voltage, by an adaptive slope compensation circuit, to create a compensated ramp voltage;

25 combining the compensated ramp voltage with the current sense signal to create a compensated current sense signal;

generating a threshold voltage for determining a peak current through the inductor; and

comparing the compensated current sense signal to the threshold voltage for determining when to turn off the transistor switch,

5 wherein the adaptive slope compensation circuit forces the compensated current sense signal to have an up-slope greater than an absolute value of its down-slope at least for duty cycles greater than 50%.

17. The method of Claim 16 wherein generating the compensation voltage for the ramp voltage by the adaptive slope compensation circuit comprises:

10 differentiating the compensated current sense signal, by a first differentiator circuit, to convert the compensated current sense signal to a first up-slope voltage and a first down-slope voltage;

 sampling and holding the first up-slope voltage by a first sample and hold circuit;

15 sampling and holding the first down-slope voltage by a second sample and hold circuit; and

 processing the first up-slope voltage and the first down-slope voltage to derive a first compensation signal that compensates the ramp voltage to generate the compensated ramp voltage.

20 18. The method of Claim 17 wherein the processing comprises:

 subtracting outputs of the first sample and hold circuit and the second sample and hold circuit, by a the first subtractor, to generate a first current across a first resistance to generate a first voltage; and

25 subtracting the first voltage from an offset voltage and amplifying the difference, by a transconductance amplifier, to generate a second current for charging and discharging a first capacitor to generate the compensation voltage at the first capacitor to compensate the ramp voltage to create the compensated ramp voltage.

19. The method of Claim 17 wherein the threshold voltage has ripple, the method further comprising:

converting the threshold voltage to a second up-slope voltage and a second down-slope voltage, by a second differentiator circuit; and

5 sampling and holding the second up-slope voltage, by a third sample and hold circuit, wherein an output of the third sample and hold circuit is further used to derive the compensation voltage for the ramp voltage to create the compensated ramp voltage.

20. The method of Claim 19 wherein the output of the third sample and hold
10 circuit is coupled to an input of the first sample and hold circuit for combining with the first up-slope voltage corresponding to an up-slope of the compensated current sense signal.

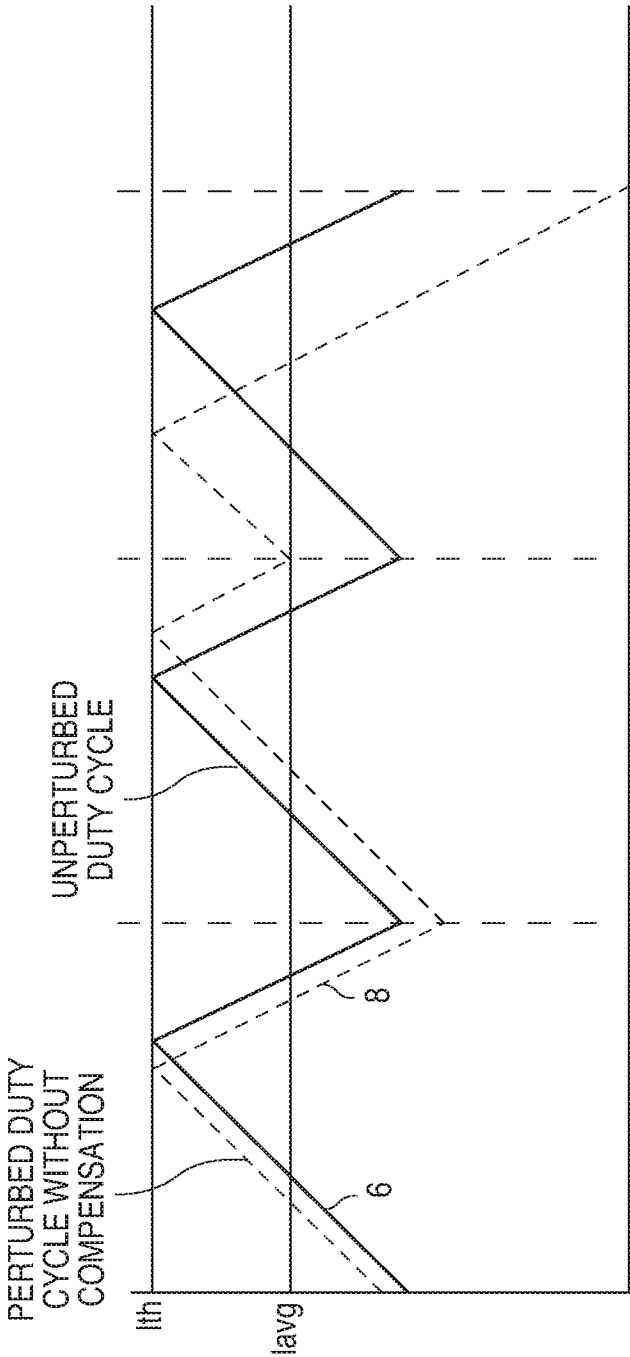
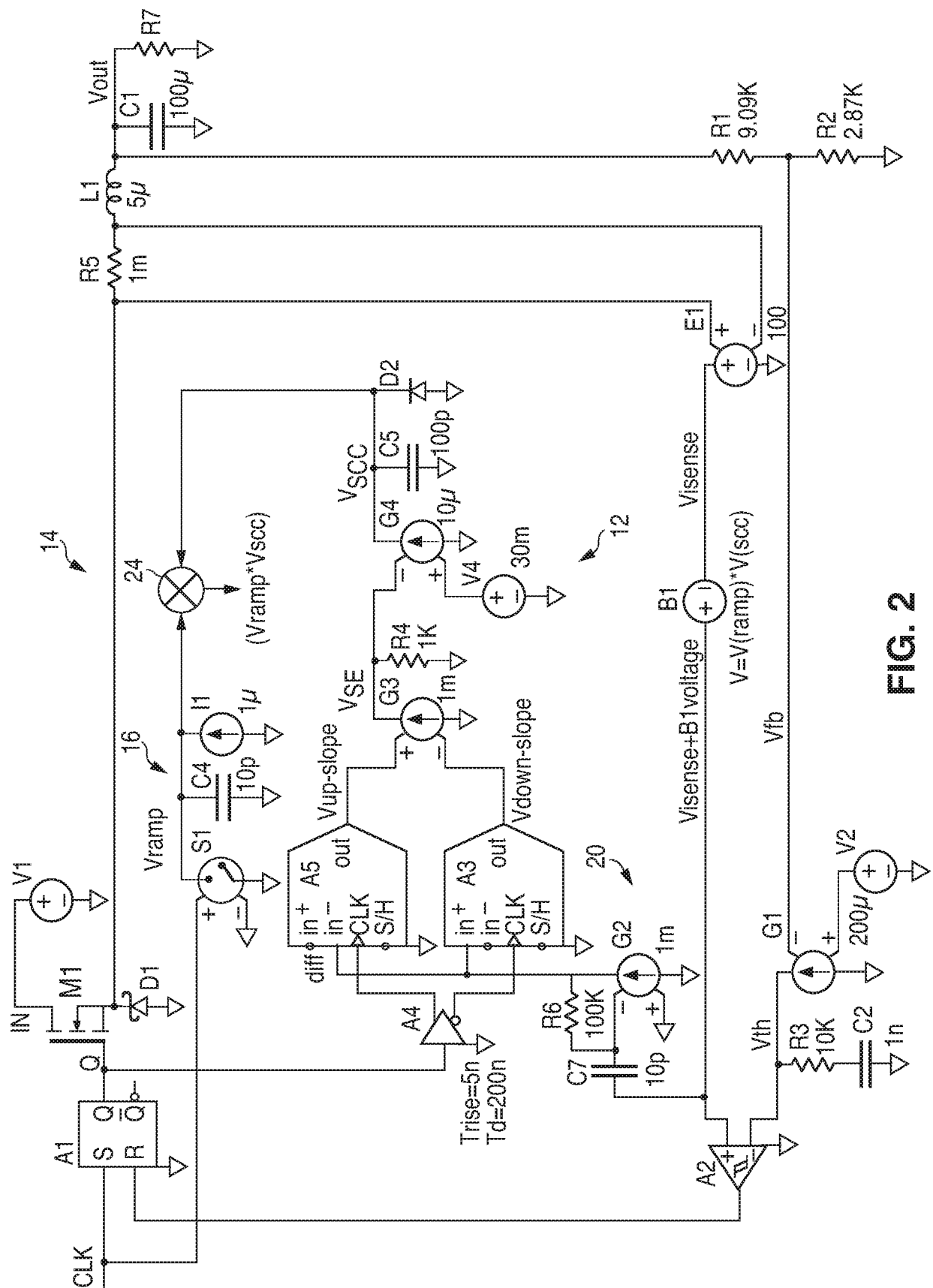


FIG. 1
(PRIOR ART)



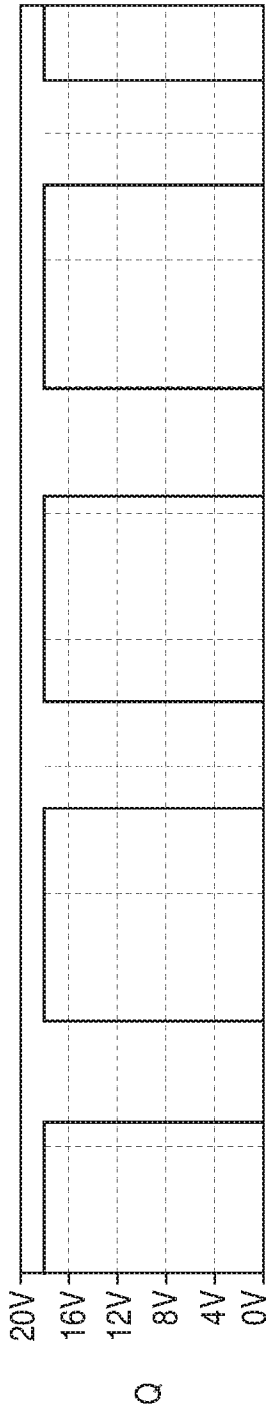


FIG. 3A

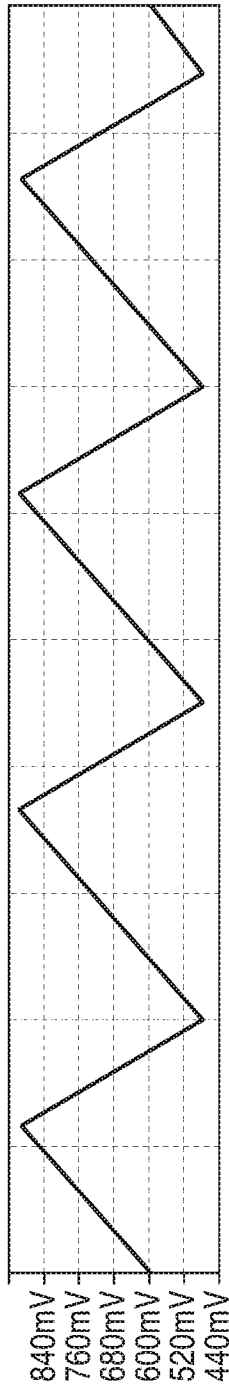


FIG. 3B

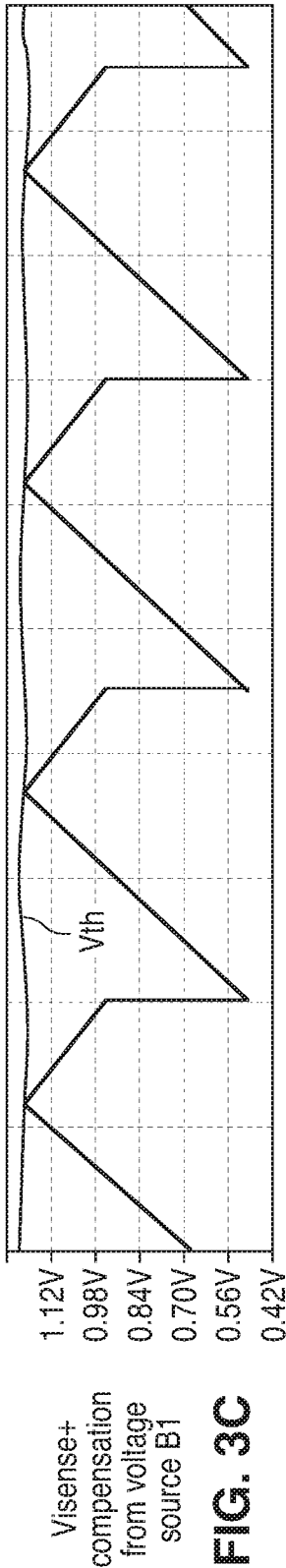


FIG. 3C

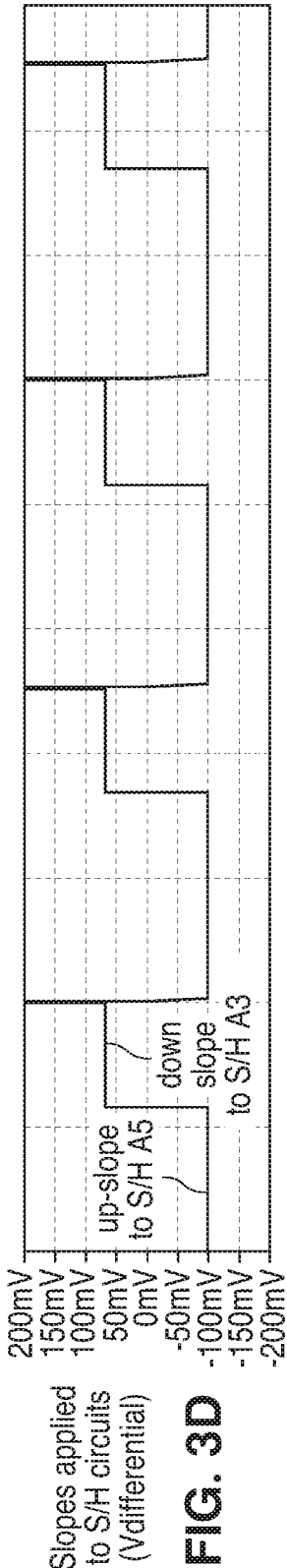
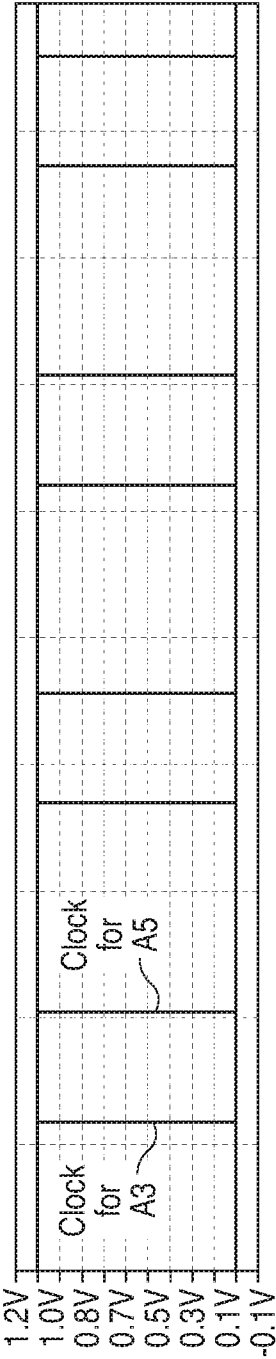
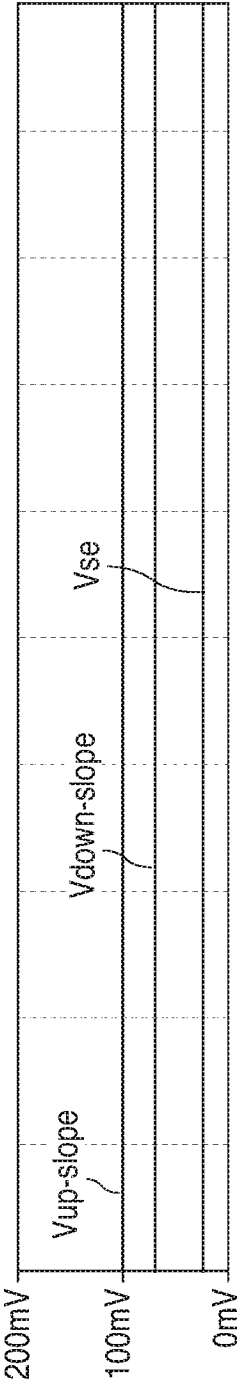


FIG. 3D



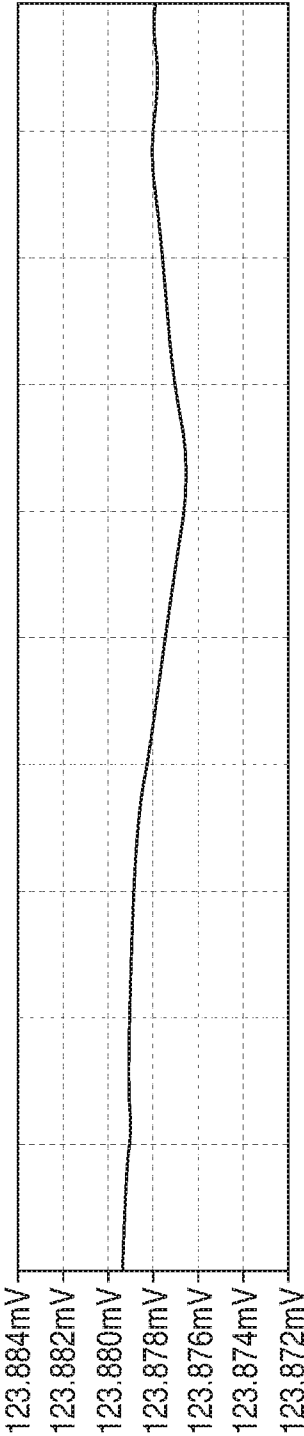
Sample and Hold
Clocking

FIG. 3E



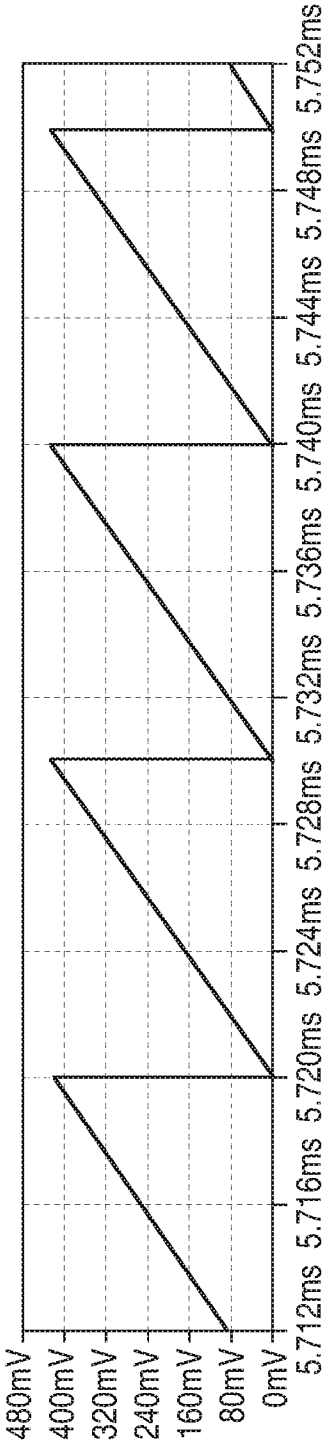
Held Slopes
and Vse

FIG. 3F



Vsc

FIG. 3G



B1 Voltage
(Vramp*Vsc)

FIG. 3H

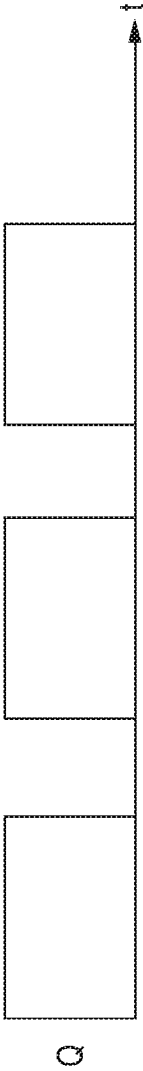


FIG. 4A

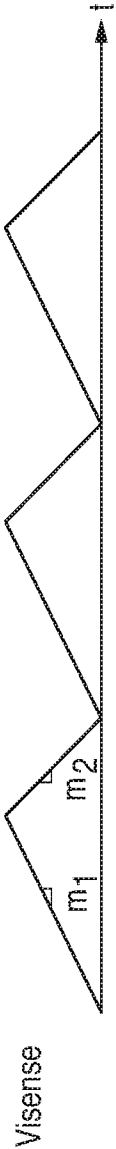


FIG. 4B

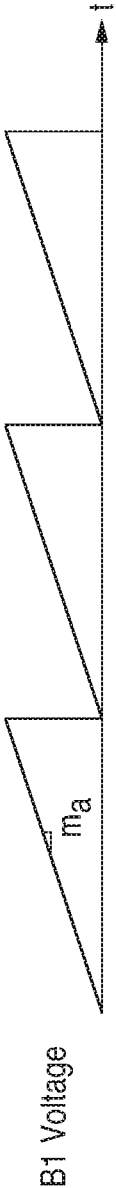


FIG. 4C

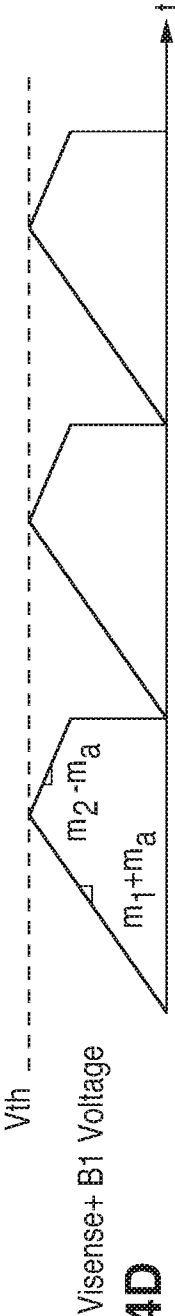


FIG. 4D

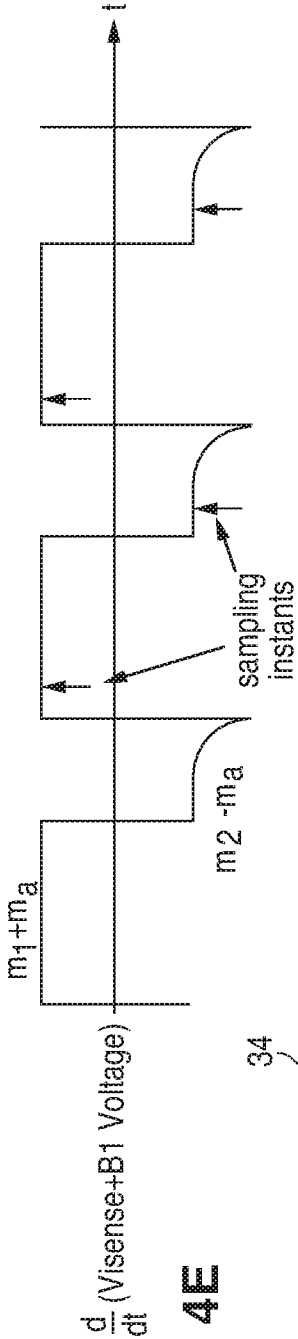


FIG. 4E

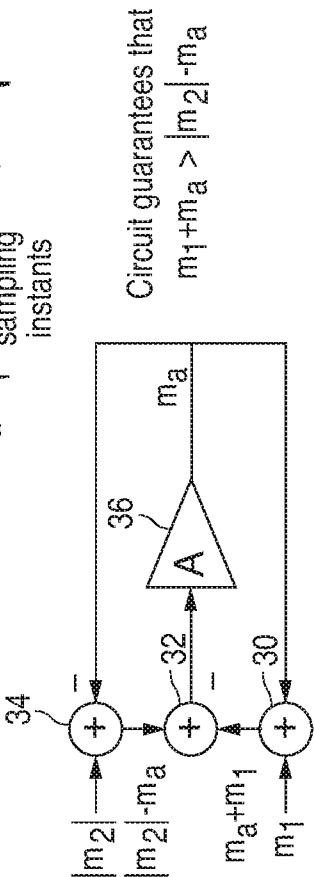


FIG. 4F

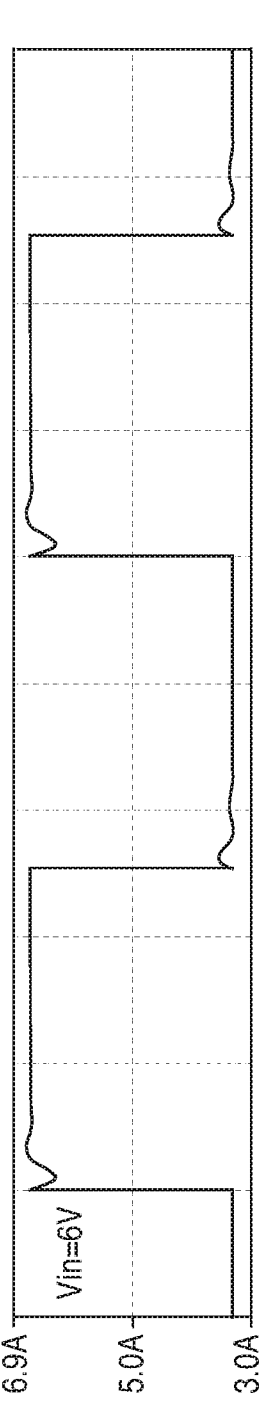


FIG. 5A

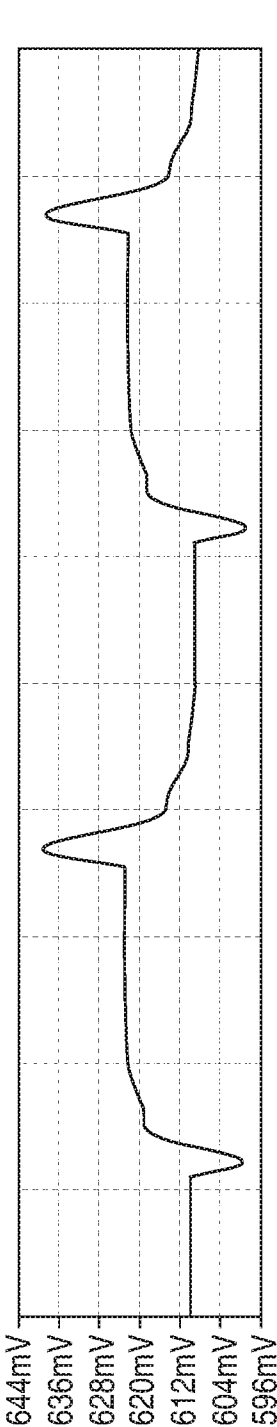


FIG. 5B

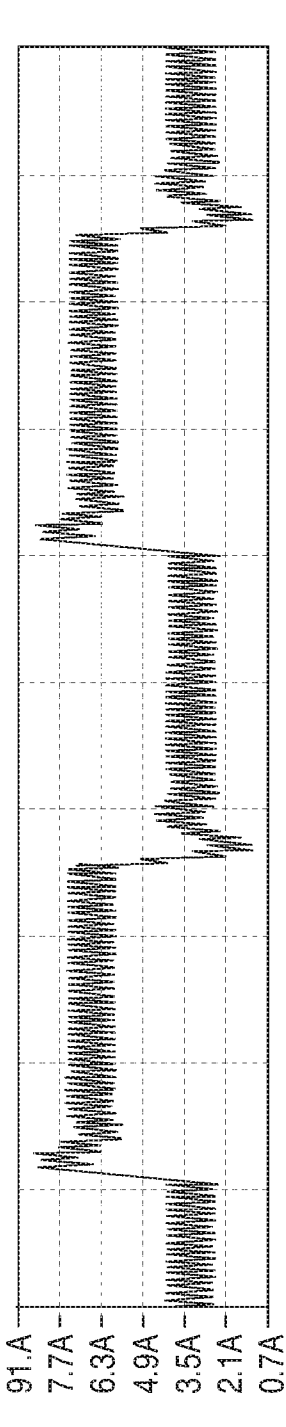


FIG. 5C

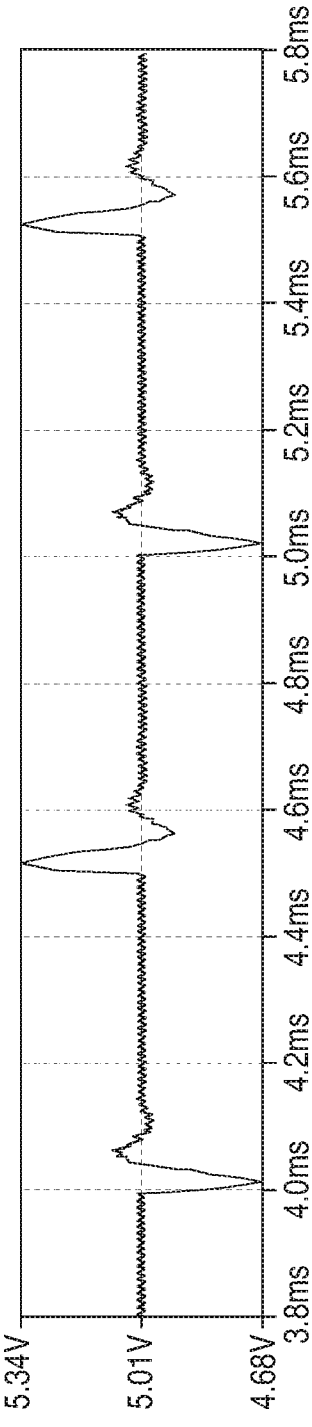
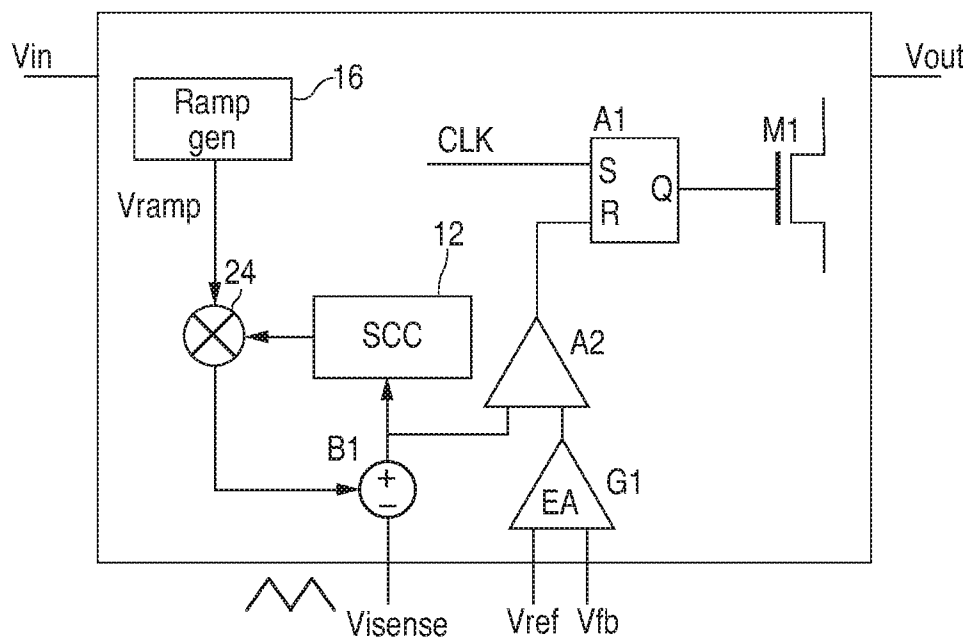
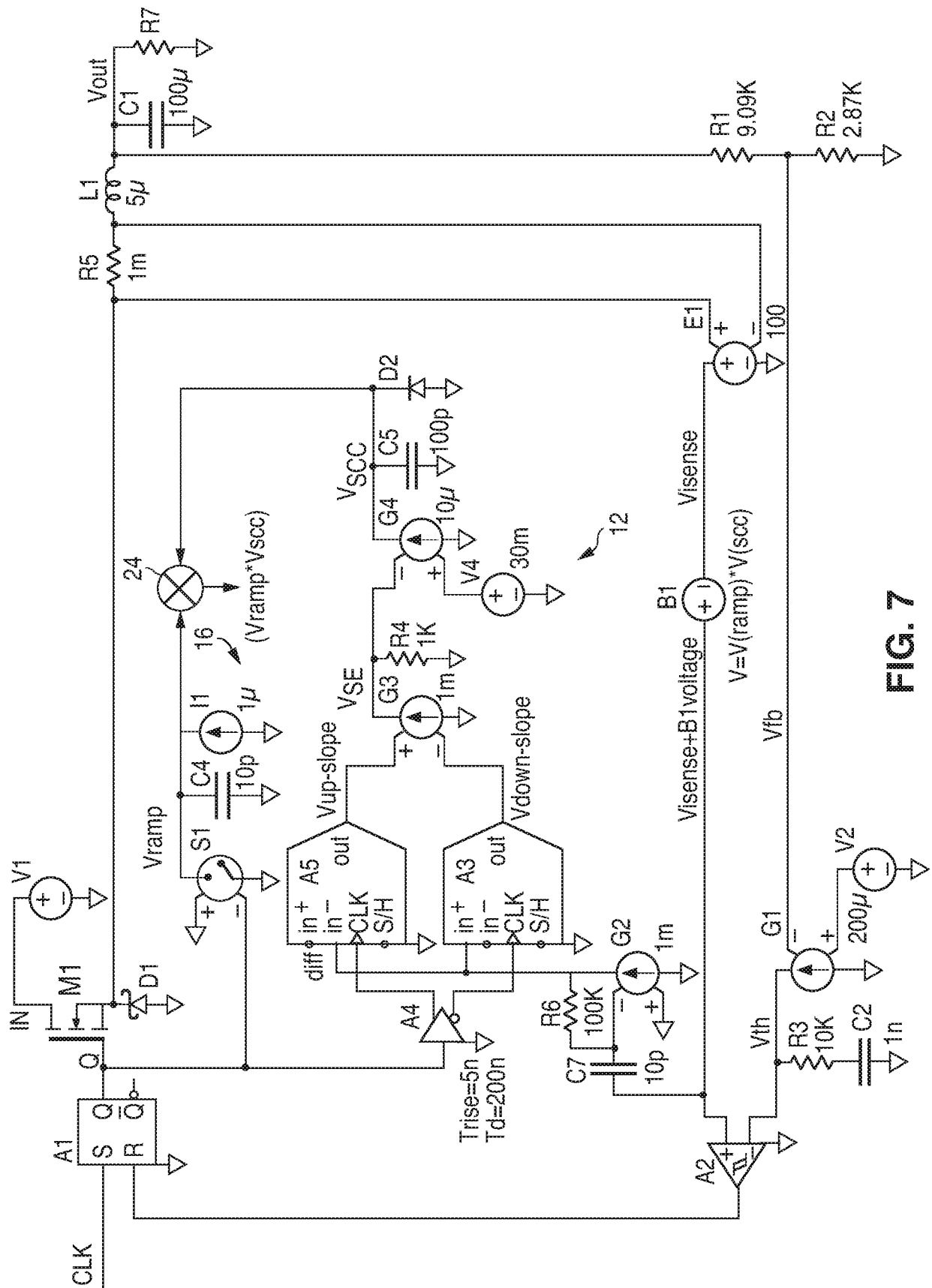


FIG. 5D

7/11

**FIG. 6**



75

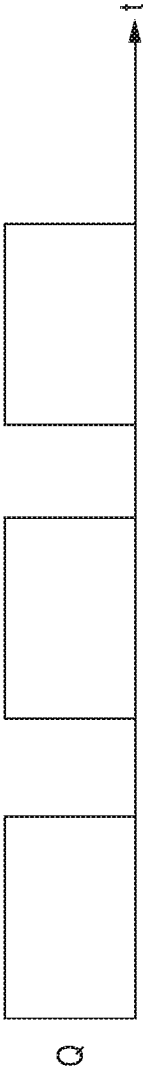


FIG. 8A

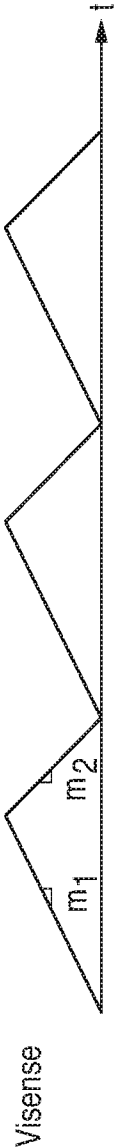


FIG. 8B

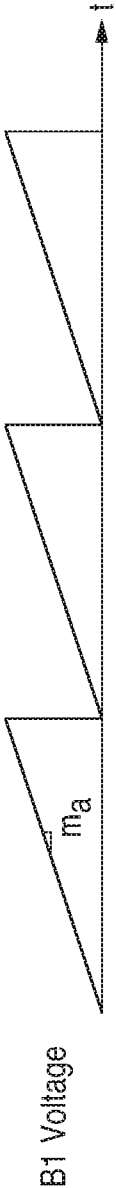


FIG. 8C

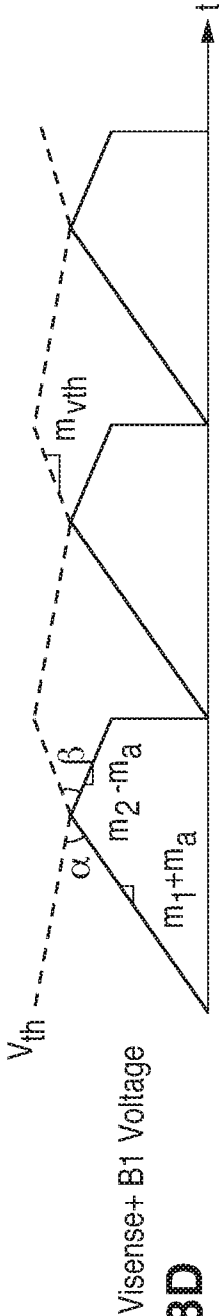


FIG. 8D

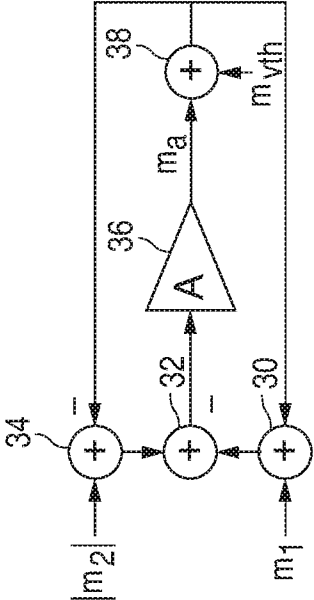


FIG. 8E

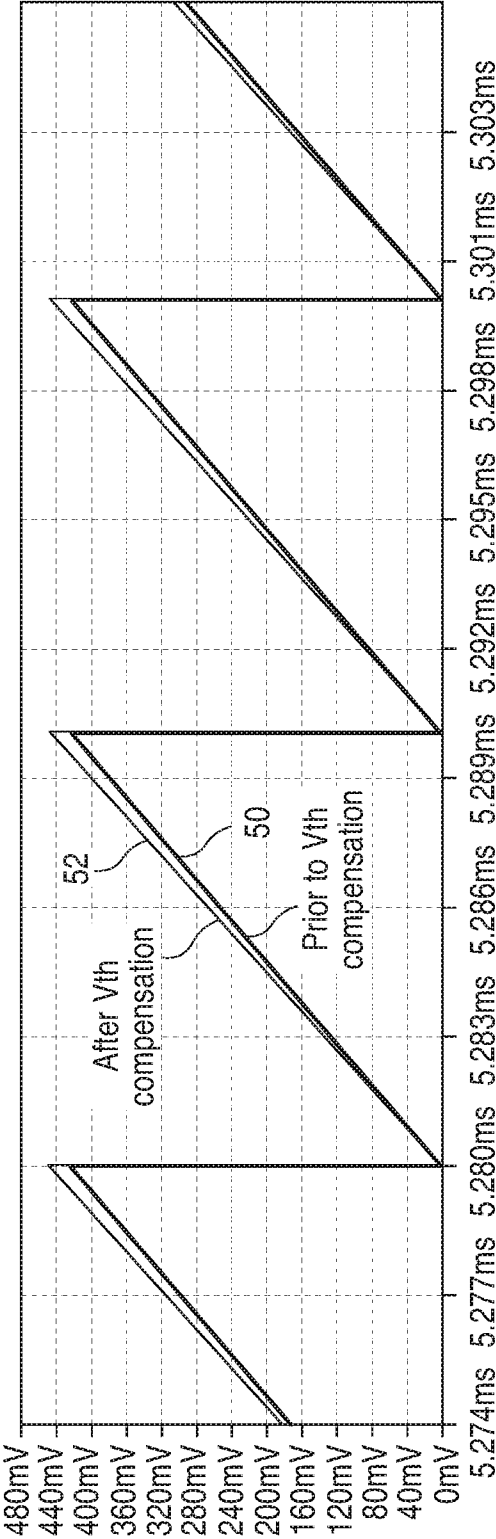
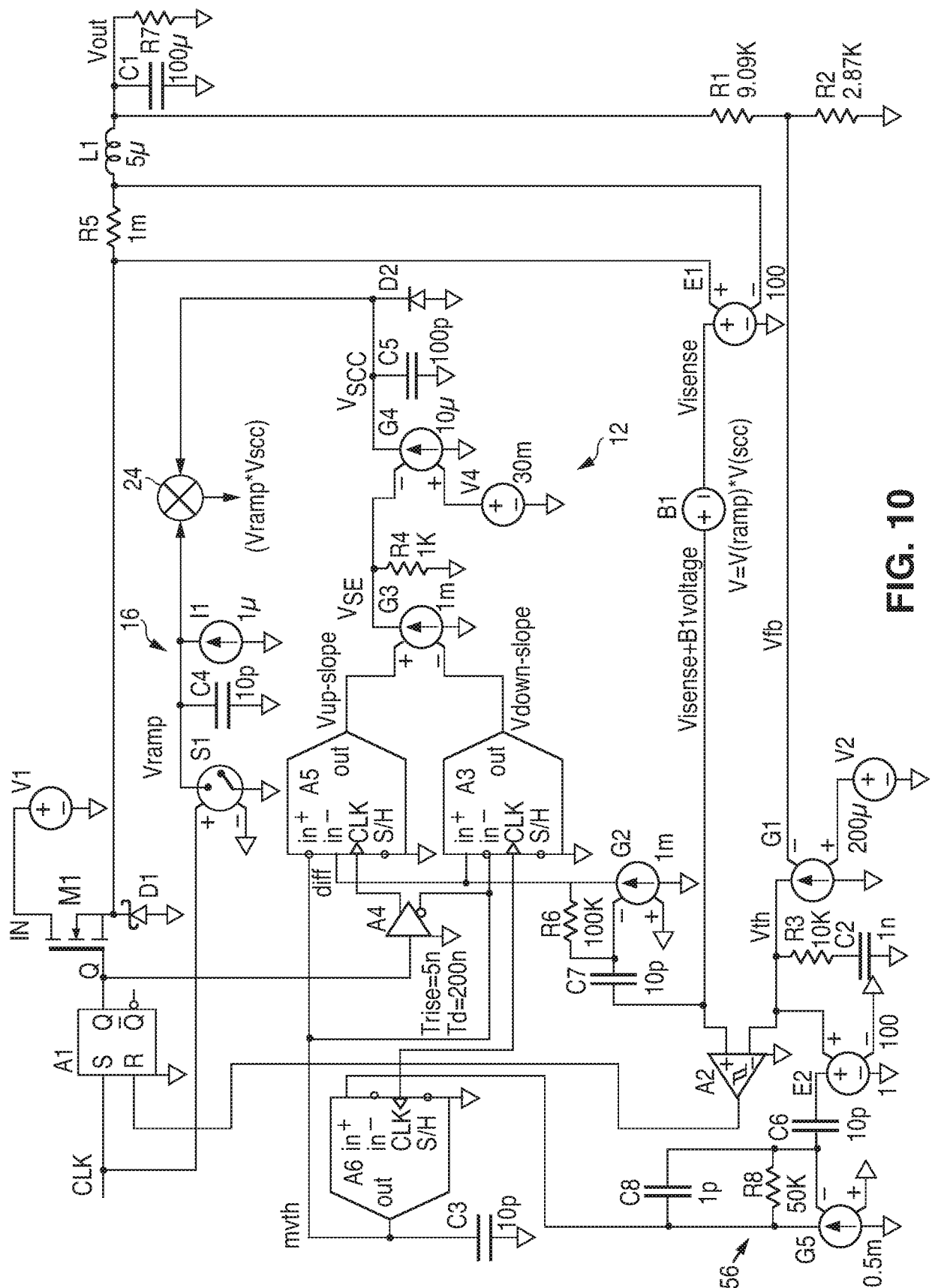


FIG. 9



OFFICIAL

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/015744

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/156
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016/006336 A1 (BENNETT PAUL THOMAS [US] ET AL) 7 January 2016 (2016-01-07) paragraph [0019] - paragraph [0021]; figures 1,2	1,10-16
A	----- US 2009/309557 A1 (MIYAMAE TORU [JP]) 17 December 2009 (2009-12-17) abstract; figures 1,3,4	1-20
A	----- DE 10 2007 028568 A1 (MEDIATEK INC [TW]) 10 April 2008 (2008-04-10) the whole document	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search

22 March 2018

Date of mailing of the international search report

29/03/2018

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Authorized officer

Gentili, Luigi

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2018/015744

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