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Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))
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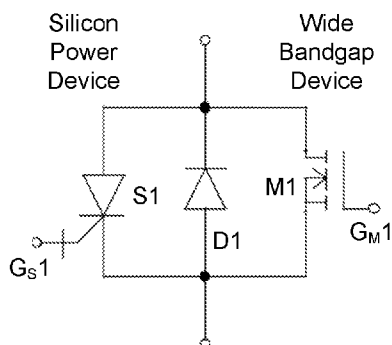


FIG. 1A

(57) Abstract: Various examples are provided related to operation of parallel semiconductors with different switching frequencies. In one example, a method of reducing conduction and switching losses in a high current switching circuit includes controlling two hybrid switches to conduct concurrently or alternately, each of the hybrid switches include a wide bandgap device and a silicon power device. Controlling of the silicon power device is at a first gate switching frequency and controlling of the wide bandgap device is at a second gate switching frequency, where the first gate switching frequency is lower than the second gate switching frequency. The silicon power device can be switched at a frequency of about 50 or 60 Hertz. The wide bandgap device can be switched at a frequency greater than 1 kHz.

WO 2025/042628 A1

## PARALLELING POWER SEMICONDUCTORS WITH DIFFERENT SWITCHING FREQUENCIES

### CROSS REFERENCE TO RELATED APPLICATIONS

**[0001]** This application claims priority to, and the benefit of, U.S. provisional application entitled "Paralleling Power Semiconductors With Different Switching Frequencies" having serial no. 63/533,757, filed August 21, 2023, which is hereby incorporated by reference in its entirety.

### BACKGROUND

**[0002]** Switching regulators and power converters such as inverters are much preferred because of the increased efficiency they can potentially provide by rapidly connecting and disconnecting the power input as needed to maintain the output voltage at a desired level. Thus, the period when a voltage drop occurs across the regulator or power converter will be limited to relatively short periods of time and overall efficiency can be improved. However, such switching is cyclic and some portions of the switching cycle may be less efficient than others due to the instantaneous conduction conditions in the regulator or power converter circuit. The amount of current passing through the regulator or power converter can vary widely over a single switching cycle and between switching cycles, depending on input voltage or output current.

### SUMMARY

**[0003]** Aspects of the present disclosure are related to operation of parallel semiconductors with different switching frequencies. In one aspect, among others, a method of reducing conduction and switching losses in a high current switching circuit comprises controlling two hybrid switches to conduct concurrently or alternately, wherein each of said hybrid switches comprise a wide bandgap device and a silicon power device, controlling of the silicon power device at a first gate switching frequency and controlling of the wide

bandgap device at a second gate switching frequency, where the first gate switching frequency is lower than the second gate switching frequency. In one or more aspects, the silicon power device can be switched at a frequency of about 50 or 60 Hertz. The wide bandgap device can be switched at a frequency greater than 1 kHz. The wide bandgap device can be switched at a frequency of about 20 kHz. In various aspects, the two hybrid switches can form a half-bridge circuit. Two additional hybrid switches can be controlled to conduct alternately in a full bridge circuit. The two hybrid switches can form a phase leg of a multi-phase power converter.

**[0004]** Other systems, methods, features, and advantages of the present disclosure will be or become apparent to one with skill in the art upon examination of the following drawings and detailed description. It is intended that all such additional systems, methods, features, and advantages be included within this description, be within the scope of the present disclosure, and be protected by the accompanying claims. In addition, all optional and preferred features and modifications of the described embodiments are usable in all aspects of the disclosure taught herein. Furthermore, the individual features of the dependent claims, as well as all optional and preferred features and modifications of the described embodiments are combinable and interchangeable with one another.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

**[0005]** Many aspects of the present disclosure can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present disclosure. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

**[0006]** FIGS. 1A-1D illustrate examples of hybrid switches, in accordance with various embodiments of the present disclosure.

**[0007]** FIG. 2 illustrates an example of an inverter circuit employing the hybrid switches of FIGS. 1A-1D, in accordance with various embodiments of the present disclosure.

**[0008]** FIG. 3 illustrates examples of currents of the produced using the hybrid switches of FIGS. 1A-1D, in accordance with various embodiments of the present disclosure.

**[0009]** FIGS. 4 and 5A-5B illustrate examples of full-bridge inverter and three-phase inverter circuits employing the hybrid switches of FIGS. 1A-1D, in accordance with various embodiments of the present disclosure.

**[0010]** FIG. 6 illustrates examples of currents of the produced using the hybrid switches in a three-phase inverter, in accordance with various embodiments of the present disclosure.

**[0011]** FIGS. 7A and 7B illustrate examples of three-phase inverter applications, in accordance with various embodiments of the present disclosure.

#### DETAILED DESCRIPTION

**[0012]** Disclosed herein are various examples related to operation of parallel semiconductors with different switching frequencies. Reference will now be made in detail to the description of the embodiments as illustrated in the drawings, wherein like reference numbers indicate like parts throughout the several views.

**[0013]** At light loads where conduction losses are reduced, the amount of power consumed by the rapid switching, referred to as switching losses, becomes a significant fraction of the total power consumption of the regulator or power converter. Switching losses can be substantially reduced by so-called hard switching or eliminated by so-called soft switching using wide bandgap semiconductor. Conversely, at heavy loads where high current is drawn through the regulator or power converter, conduction losses in the switches, generally wide bandgap MOSFETs since they are well-suited to operation in a hard-switching or soft-switching mode, tend to predominate because the conduction path in MOSFETs is substantially resistive. Conduction losses theoretically could be mitigated by placing a large number of MOSFETs in parallel to reduce currents in individual MOSFETs and thus reduce the voltage drop. However, such a parallel connection of many switches is not generally practical due to the cost of multiple switching devices. By operating a silicon power device connected in parallel with a wide bandgap device at a lower switching

frequency than the wide bandgap device, the switching loss and conduction loss can be significantly reduced since the switching frequency of the silicon power device is effectively reduced.

**[0014]** Referring to FIGS. 1A-1D, shown are schematic diagrams illustrating examples of hybrid switch arrangements in accordance with various embodiments of the present disclosure. The hybrid switch arrangements include a silicon power device S1 connected in parallel with a wide bandgap device M1. The silicon power device S1 can be, e.g., a silicon controlled rectifier (SCR) as shown in FIGS. 1A and 1C or an insulated-gate bipolar transistor (IGBT) as shown in FIG. 1B and 1D. The wide bandgap device M1 can be a metal oxide semiconductor field-effect transistor (MOSFET) device. For soft switching, the silicon power device S1 also has a diode D1 connected in parallel with the conduction terminals thereof as shown in FIGS. 1A and 1B. The wide bandgap device M1 also includes a similarly connected diode referred to as a body diode. Each transistor is controlled by a corresponding gate control signal  $G_{S1}$  or  $G_{M1}$  with the silicon power device S1 operated at a lower switching frequency than the wide bandgap device M1.

**[0015]** The silicon power device S1 operates at low switching frequency (for example, at an operational frequency of 60 Hz) and the wide bandgap device M1 operates at high switching frequency (for example, a frequency of 20 kHz). The silicon power device S1 is able to handle most currents at a low turn-on voltage with no severe switching losses. The wide bandgap device can operate at a high switching frequency (e.g., in a kilohertz frequency range) at low current. By paralleling the semiconductors with different switching frequencies, the overall conduction and switching losses can be reduced. At the same time, the system cost is reduced compared to systems only employing wide bandgap devices. The following table summarizes the advantages and benefits of the proposed configuration.

	Cost	Performance
Proposed hybrid switches with different switching frequencies (80% saving of Wide Bandgap Device)	Very Low	Very Good
Current State-of-the-Art (Wide Bandgap Device)	Expensive	Good
Classic State-of-the -Art (Low Speed Silicon Device)	Very Low	Not Good

**[0016]** Referring now to FIG. 2, shown is an example of an inverter circuit employing the hybrid switch of FIGS. 1A or 1B. It should be understood that examples of inverter circuits using the hybrid switches in other zero voltage switching inverters are considered to be within the scope of the present disclosure.

**[0017]** As illustrated in FIG. 2, the inverter circuit comprises two hybrid switches, which alternately connect the DC+ and DC- busses, which receive power from a power supply, battery or the like, generically illustrated as  $V_{dc}$  and  $C_{dc}$ , to a load. (The current return path from the load is not shown.) The upper hybrid switch comprises a wide bandgap device M1, a silicon power device S1, and optionally a diode D1 as described with respect to FIGS. 1A-1D. In a conventional hard-switching inverter, only IGBTs S1 and S2 and diodes D1 and D2 are used. IGBT S1 conducts the positive current, while diode D1 conducts the negative freewheeling current. Similarly, IGBT S2 conducts the negative current, while D2 conducts the positive freewheeling current. With added MOSFETs M1 and M2, the positive currents are shared between M1 and S1 and the negative currents are shared between M2 and S2 while the positive and negative freewheeling currents are shared between the diodes D1, D2 and the body diodes of the MOSFETs M1 and M2, respectively. Two gate signals control each hybrid switch: GS1 and GM1 for the upper switch and GS2 and GM2 for the lower switch. Voltage and current phase sensors can provide feedback for gate control. The low switching frequency can be controlled based on the voltage feedback and the high switching frequency can be controlled based on the current feedback.

**[0018]** The inverter circuit of FIG. 2 is perhaps the simplest and most generalized inverter circuit possible and its operation can be readily understood by those skilled in the art. Similarly, from the above discussion in connection with FIGS. 1A-1D, it can be understood that the reduction of voltage drop across the hybrid switches (compared with the conventional circuit in which only the IGBTs S1 and S2 are used) can significantly improve efficiency when any significant current is drawn by the load and particularly at light loads which will occur near the times when the on-state is reversed between switches.

**[0019]** FIG. 3 shows an example of the load current (top) supplied by switching the silicon power devices S1 and S2 at a lower switching frequency than the wide bandgap devices M1 and M2. The currents of the wide bandgap devices M1 and M2 (center) and the currents of the silicon power devices S1 and S2 produced by the switching scheme are also illustrated. Under full load conditions the inverter efficiency is approximately the same or effectively increased by using ultra-low voltage drop silicon devices, the hybrid switching scheme can provide a significant conduction and switching loss reduction/efficiency gain under lesser load conditions.

**[0020]** The hybrid switch is usable in virtually any soft-switching or hard-switching inverter, regulator or power converter. For example, FIG. 4 schematically shows a full-bridge resonant snubber inverter (RSI) circuit including hybrid switches in accordance with the disclosure. The full bridge operation is to have hybrid switches turning on and off simultaneously for the positive load current and hybrid switches turning on and off simultaneously for the negative load current. To achieve soft switching for hybrid switches, the resonant current relies on the turning on of auxiliary switch Sr1 which creates a positive current to discharge capacitors so that the hybrid switches can be turned on under zero voltage conditions. Similarly, for the negative current cycles, the negative resonant current relies on the turning on of auxiliary switch Sr2 to discharge capacitors to achieve soft switching for the hybrid switches. Voltage and current phase sensors can provide feedback for gate control. The low switching frequency can be controlled based on the voltage feedback and the high switching frequency can be controlled based on the current feedback.

**[0021]** FIG. 5A illustrates application of the hybrid switch in accordance with the disclosure in a three-phase inverter. FIG. 5B shows the three-phase inverter implemented with the hybrid switch of FIG. 1A. FIG. 6 shows an example of the load currents for the three phases (bottom) supplied by switching the silicon power devices S1-S6 at a lower switching frequency than the wide bandgap devices M1-M6. The currents of the wide bandgap devices and the currents of the silicon power devices produced by the switching scheme are also illustrated (top) with the DC bus voltage shown (middle). As can be seen in FIG. 6, the high-speed SiC devices M1-M6 only operate during 1/3 of grid cycle to significantly reduce the current stress and the associated conduction loss. The slow-speed silicon devices S1-S6 with very low voltage drop don't suffer high switching loss while achieving low conduction loss with low cost. This hybrid switching method can be applied to DC to AC and AC to DC conversion where the DC operates as a controlled power source and the AC is a three-phase voltage or current source. For example, the coordinated operation of all 12 devices in DC to AC conversion generates sinusoidal, three phase, low harmonic distortion AC current from a dynamic DC input current or voltage.

**[0022]** Control of the parallel devices operating at different switching frequencies for three-phase inverters or converters is illustrated in FIG. 6. The control scheme can be explained using time markers t1 through t5 for the two hybrid switches of phase A over a grid cycle T, as shown in FIG. 6. At time t1, slow-speed silicon device S1 is switched ON while devices S2 and M1-M2 are switched OFF. As seen in FIG. 6, time t1 corresponds to the cross-over of the phase A and C currents and the peak negative current for phase B. The current phase can lag, lead or be aligned with the voltage phase to meet the needs of the application. At time t2, operation of high-speed silicon devices M1-M2 is initiated while devices S1-S2 are switched OFF. As seen in FIG. 6, time t2 corresponds to the cross-over of the phase A and B currents and the peak negative current for phase C. The current phase can lag, lead or be aligned with the voltage phase to meet the needs of the application. The high frequency operation continues until time t3, where slow-speed silicon device S2 is switched ON while devices S1 and M1-M2 are switched OFF. As seen in FIG. 6, time t3

corresponds to the cross-over of the phase A and C currents and the peak positive current for phase B. The current phase can lag, lead or be aligned with the voltage phase to meet the needs of the application. At time t4, operation of high-speed silicon devices M1-M2 is initiated while devices S1-S2 are switched OFF. As seen in FIG. 6, time t4 corresponds to the cross-over of the phase A and B currents and the peak positive current for phase C. The current phase can lag, lead or be aligned with the voltage phase to meet the needs of the application. The grid cycle T is then repeated. The table below indicates the device states between the time markers over the grid cycle T.

Time Marker	% Grid Cycle	S1 (Si)	M1 (SiC)	S2 (Si)	M2 (SiC)
[t1, t2]	2/6	On	Off	Off	Off
[t2, t3]	1/6	Off	On/Off (High Freq.)	Off	Off/On (High Freq.)
[t3, t4]	2/6	Off	Off	On	Off
[t4, t5]	1/6	Off	On/Off (High Freq.)	Off	Off/On (High Freq.)

**[0023]** Phases B and C follow similar sequences. The slow switching silicon devices S1-S6 can operate at grid frequency and conduct the output current during 2/3 of the grid cycle. The high frequency switching silicon carbide devices M1-M6 conduct the current during 1/3 of grid cycle. High frequency switching of the three-phases covers all (3/3) of the grid cycles and drastically reduces the size, weight, and cost of the inductor chokes on the AC or grid side as shown in the circuit in the example of FIG. 5B.

**[0024]** FIGS. 7A and 7B show examples of three-phase inverter applications for photovoltaics (PV) or electric vehicle/battery storage, respectively. Voltage and current phase sensors can provide feedback for gate control. The low switching frequency can be controlled based on the voltage feedback and the high switching frequency can be controlled based on the current feedback.

**[0025]** It is seen that the hybrid switch in accordance with the basic principles of the disclosure facilitates design and operation of soft switching or hard-switching power

regulator and converters and power inverters while providing a significant improvement in light and/or heavy load efficiency in any such application. The hybrid switch can be embodied as discrete devices or a three (or four—for connecting an external delay or control) terminal switch package.

**[0026]** It should be emphasized that the above-described embodiments of the present disclosure are merely possible examples of implementations set forth for a clear understanding of the principles of the disclosure. Many variations and modifications may be made to the above-described embodiment(s) without departing substantially from the spirit and principles of the disclosure. All such modifications and variations are intended to be included herein within the scope of this disclosure and protected by the following claims.

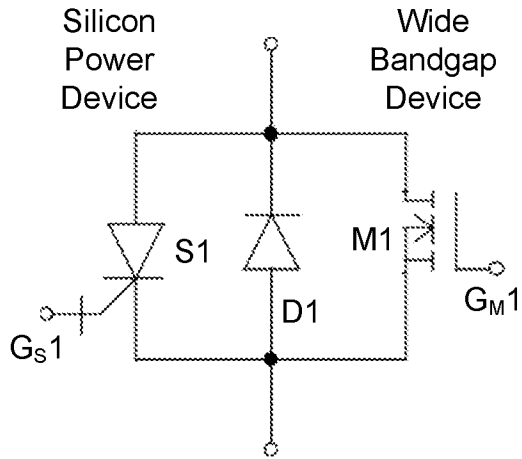
**[0027]** The term "substantially" is meant to permit deviations from the descriptive term that don't negatively impact the intended purpose. Descriptive terms are implicitly understood to be modified by the word substantially, even if the term is not explicitly modified by the word substantially.

**[0028]** It should be noted that ratios, concentrations, amounts, and other numerical data may be expressed herein in a range format. It is to be understood that such a range format is used for convenience and brevity, and thus, should be interpreted in a flexible manner to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. To illustrate, a concentration range of "about 0.1% to about 5%" should be interpreted to include not only the explicitly recited concentration of about 0.1 wt% to about 5 wt%, but also include individual concentrations (e.g., 1%, 2%, 3%, and 4%) and the sub-ranges (e.g., 0.5%, 1.1%, 2.2%, 3.3%, and 4.4%) within the indicated range. The term "about" can include traditional rounding according to significant figures of numerical values. In addition, the phrase "about 'x' to 'y'" includes "about 'x' to about 'y'".

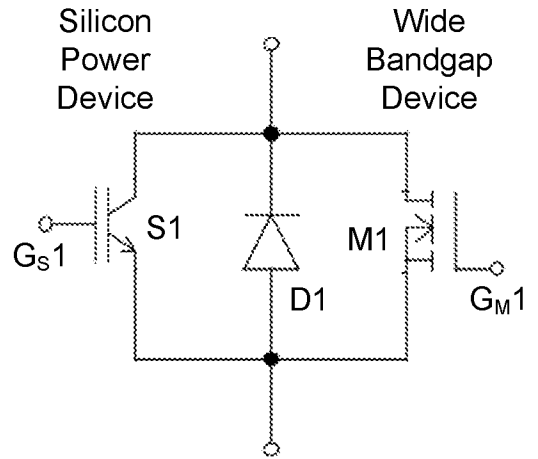
**CLAIMS**

Therefore, at least the following is claimed:

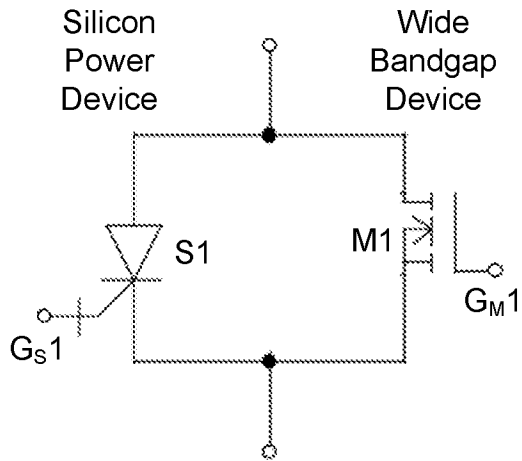
1. A method of reducing conduction and switching losses in a high current switching circuit, comprising:  
controlling two hybrid switches to conduct concurrently or alternately, wherein each of said hybrid switches comprise a wide bandgap device and a silicon power device, controlling of the silicon power device at a first gate switching frequency and controlling of the wide bandgap device at a second gate switching frequency, where the first gate switching frequency is lower than the second gate switching frequency.
2. The method of claim 1, wherein the silicon power device is switched at the first gate switching frequency of about 50 or 60 Hertz.
3. The method of claim 2, wherein the wide bandgap device is switched at the second switching frequency greater than 1 kHz.
4. The method of claim 3, wherein the wide bandgap device is switched at the second switching frequency of about 20 kHz.
5. The method of any of claims 1-4, wherein said two hybrid switches form a half-bridge circuit.
6. The method of any of claims 1-4, wherein two additional hybrid switches are controlled to conduct alternately in a full bridge circuit.
7. The method of any of claims 1-4, wherein said two hybrid switches form a phase leg of a multi-phase power converter.



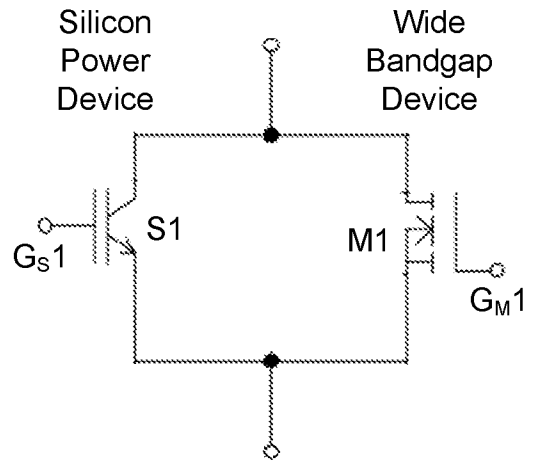
**FIG. 1A**



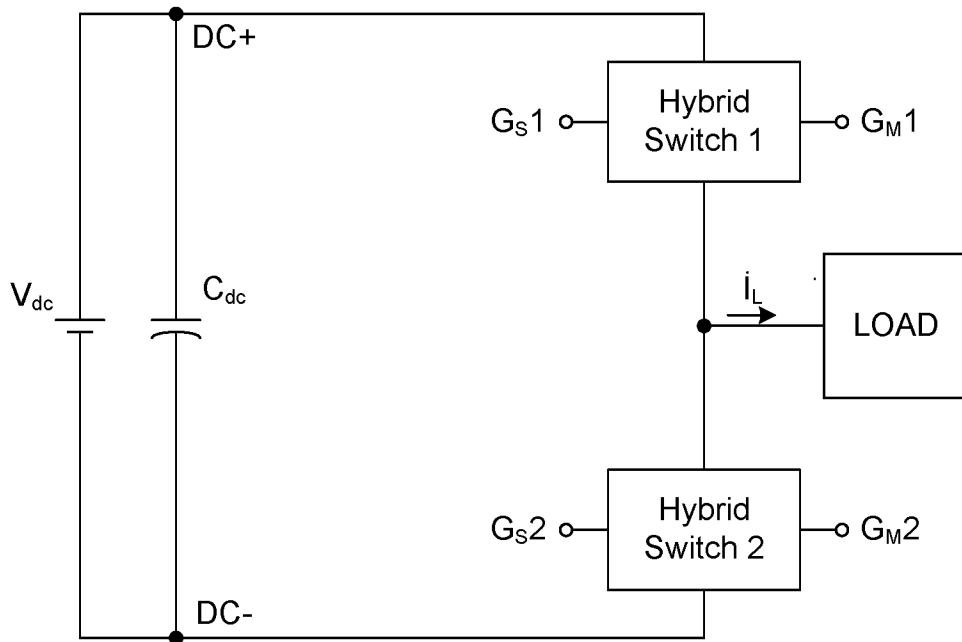
**FIG. 1B**



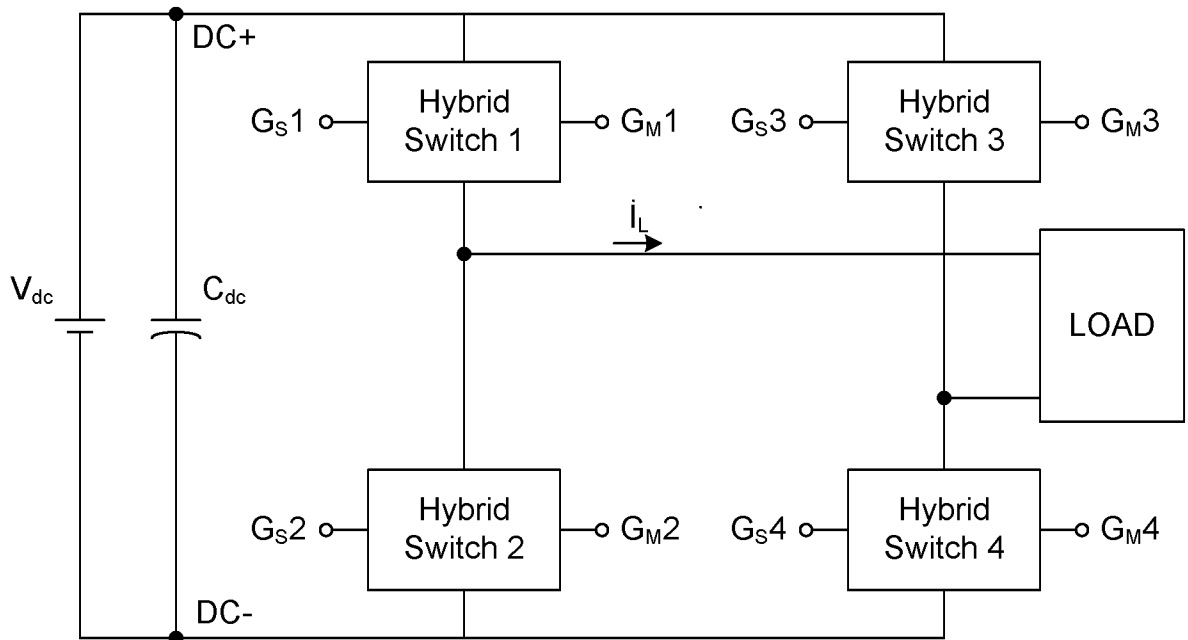
**FIG. 1C**



**FIG. 1D**



**FIG. 2**



**FIG. 4**

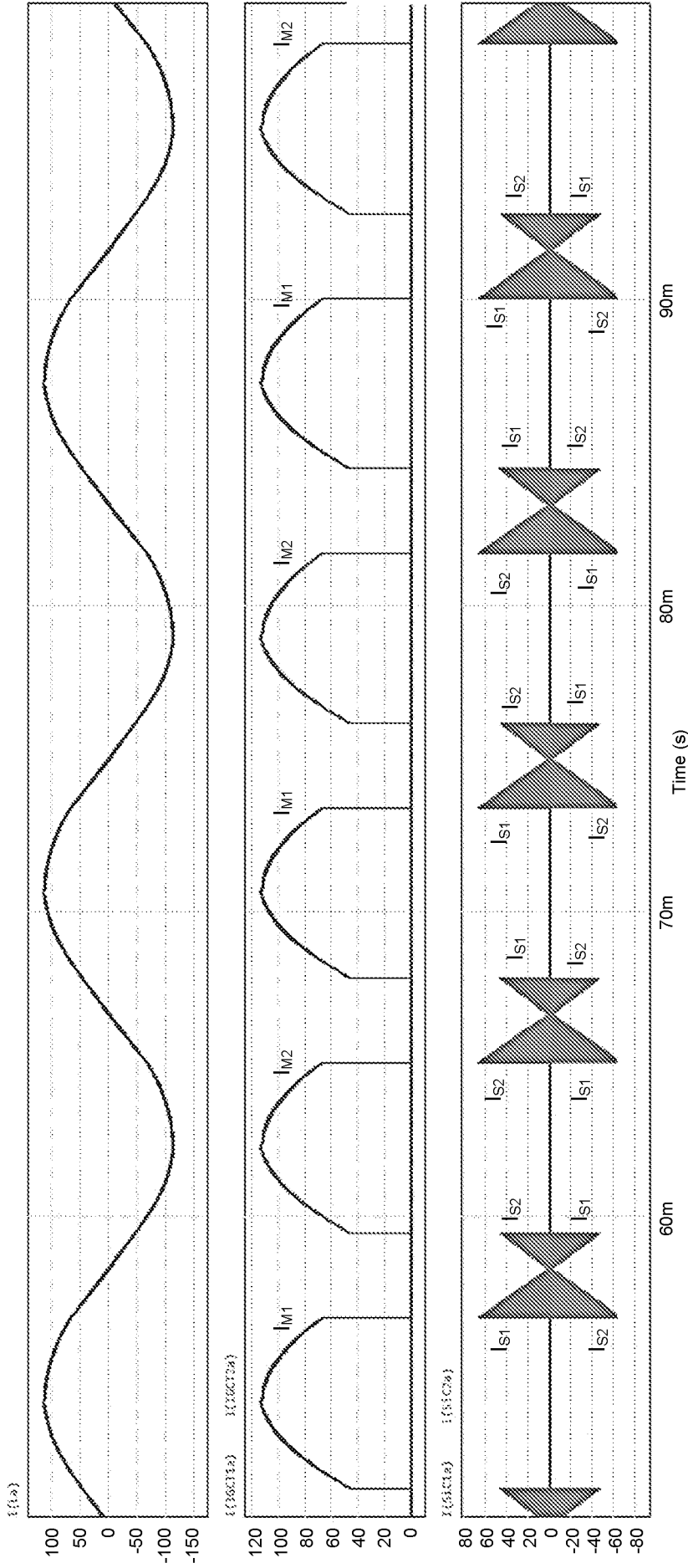


FIG. 3

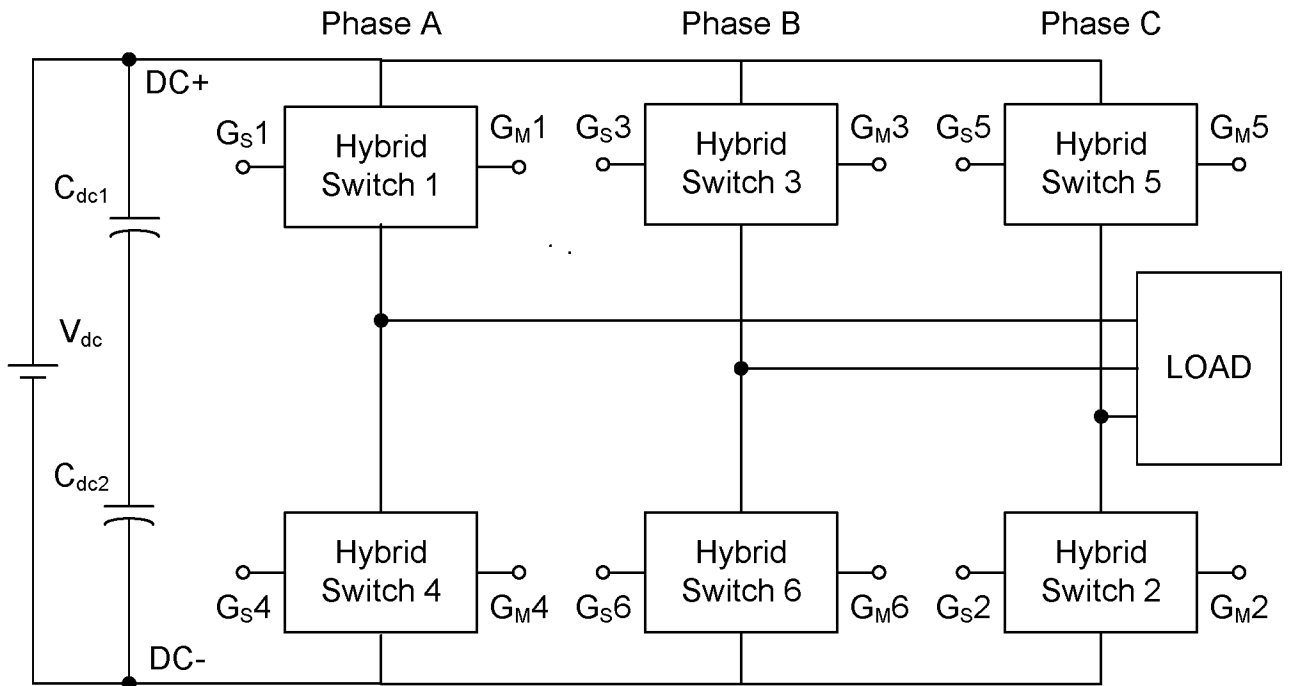


FIG. 5A

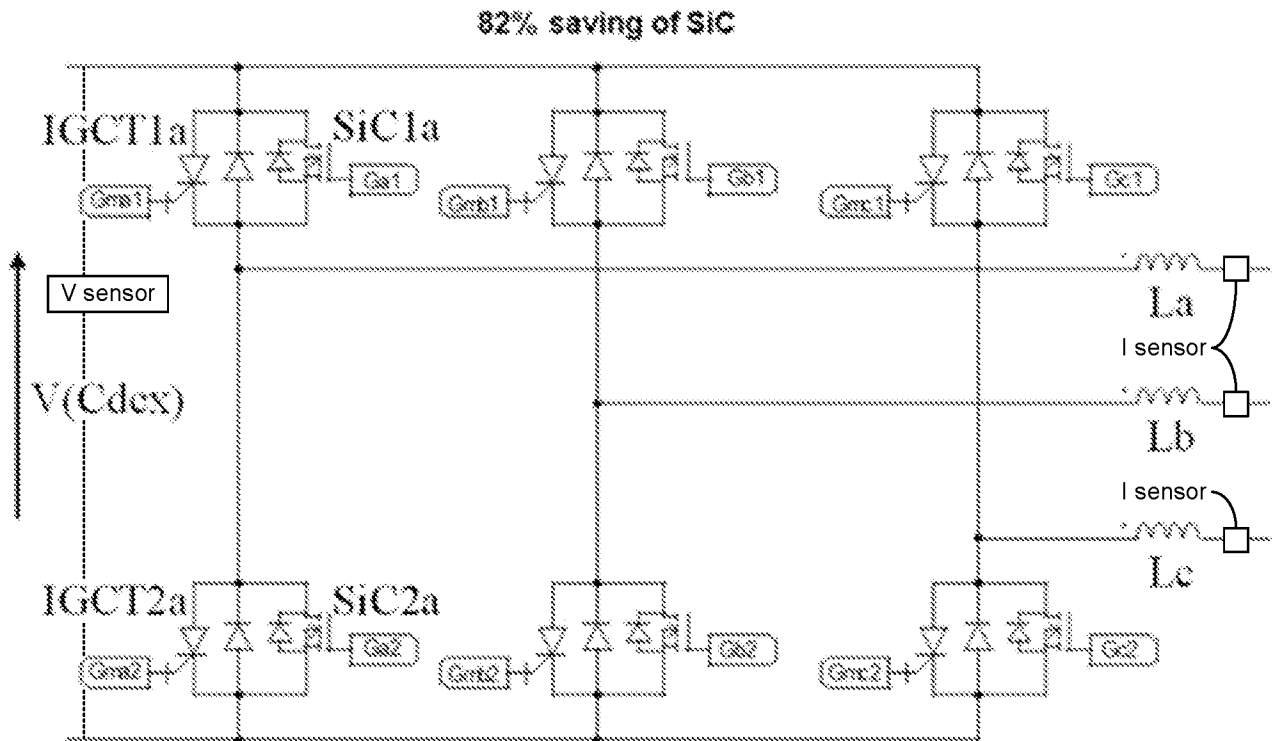


FIG. 5B

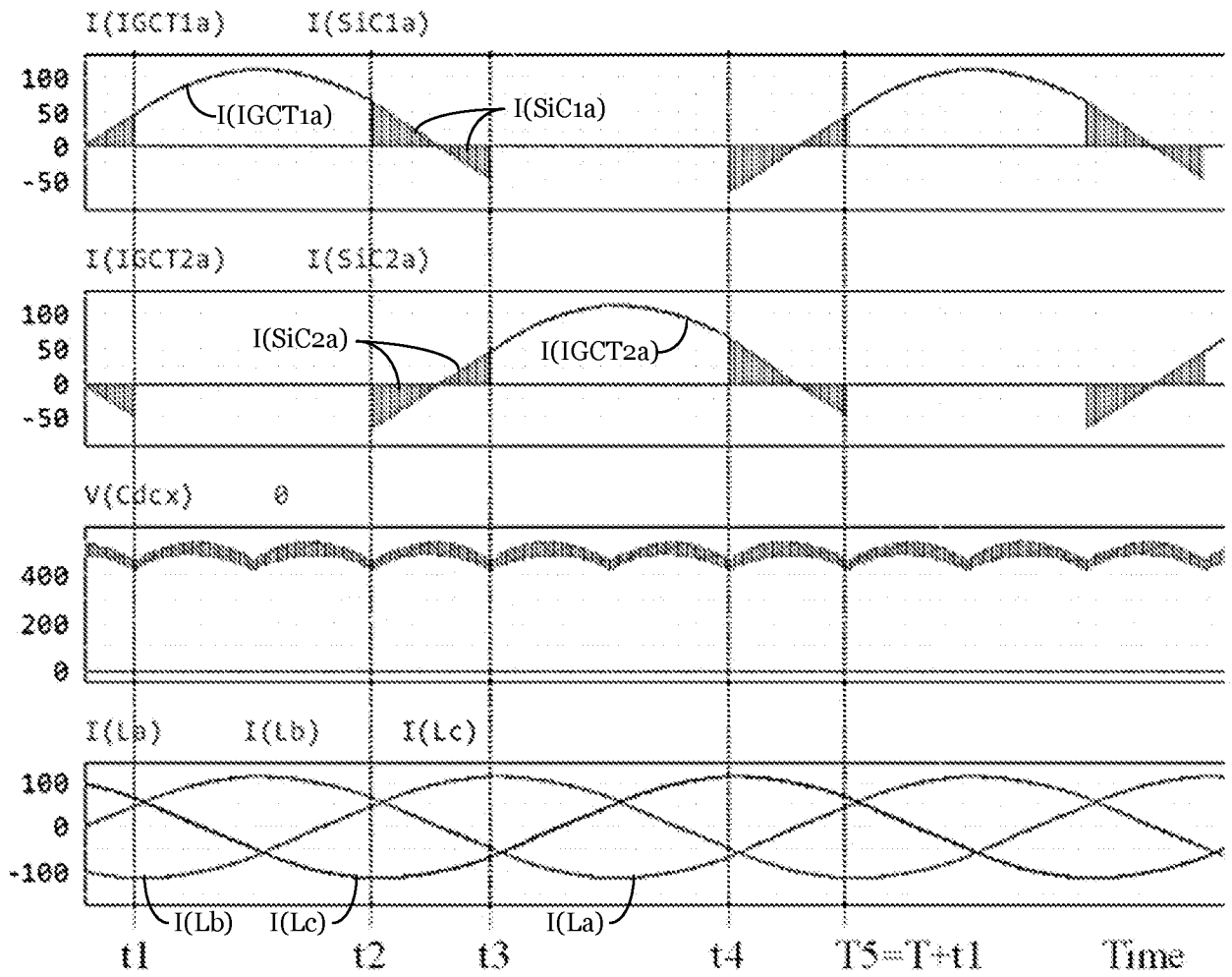
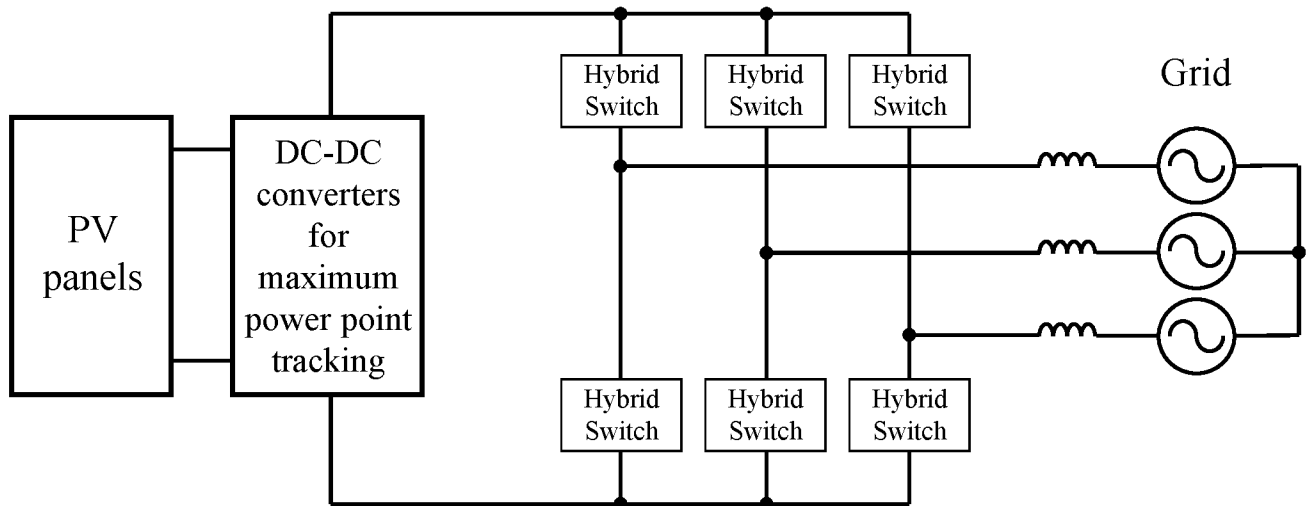
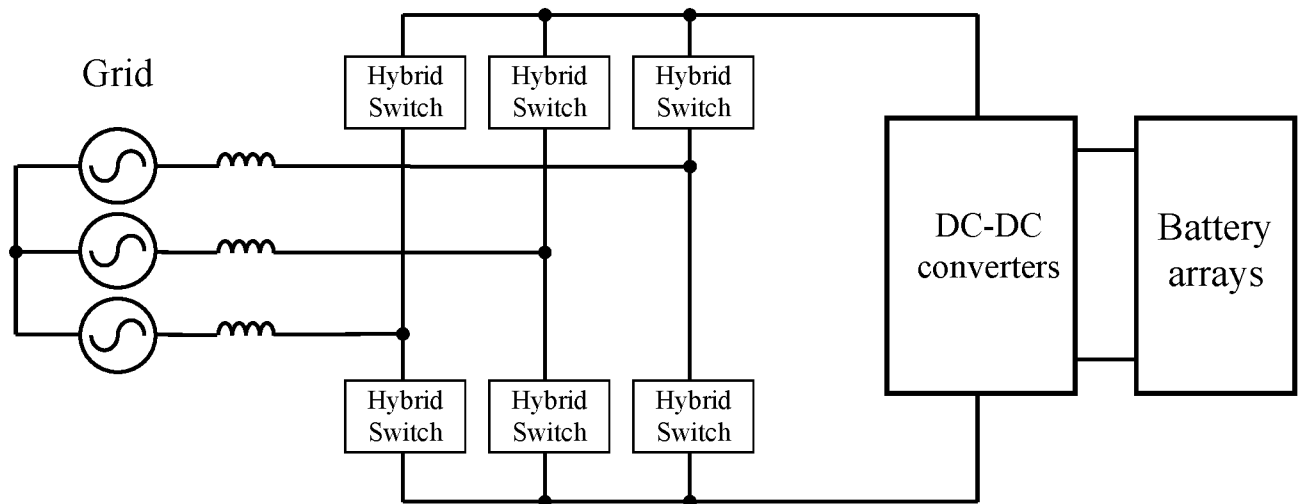


FIG. 6



**FIG. 7A**



**FIG. 7B**

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2024/042072

<b>A. CLASSIFICATION OF SUBJECT MATTER</b>		
IPC: <b>H03K 17/567</b> (2024.01); <b>H03K 17/12</b> (2024.01); <i>H03K 17/16</i> (2024.01); <i>H02M 1/00</i> (2024.01) CPC: <b>H03K 17/567</b> ; <b>H03K 17/127</b> ; <i>H02M 1/0054</i> ; <i>H03K 17/164</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b>		
Minimum documentation searched (classification system followed by classification symbols) See Search History Document		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched See Search History Document		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) See Search History Document		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 4064564 A1 (SIEMENS GAMESA RENEWABLE ENERGY INNOVATION & TECHNOLOGY S.L.) 28 September 2022 (28.09.2022) entire document	1-4
Y	entire document	5-7
Y	US 2012/0057387 A1 (LAI et al.) 08 March 2012 (08.03.2012) entire document	5-7
A	US 7,034,345 B2 (CHANG et al.) 25 April 2006 (25.04.2006) entire document	1-7
A	US 2016/0191046 A1 (EATON CORPORATION) 30 June 2016 (30.06.2016) entire document	1-7
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
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Date of the actual completion of the international search <b>12 September 2024 (12.09.2024)</b>		Date of mailing of the international search report <b>24 September 2024 (24.09.2024)</b>
Name and mailing address of the ISA/US <b>Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450</b> Facsimile No. <b>571-273-8300</b>		Authorized officer <b>MATOS TAINA</b> Telephone No. <b>571-272-4300</b>