United States Patent

McDonald

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[54] **SIGNAL CODING AND DECODING SYSTEM**

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[52] **U.S. Cl.**.....**325/32,** 178/22, 179/1.5 R, 179/1.5 S, 179/1.5 M, 179/1.5 E

[51] **Int. Cl.**.....**H04k 1/00**

[58] **Field of Search**.....325/32; 178/22; 179/1.5 R, 179/1.5 S, 1.5 M, 1.5 FS; 197/1.5 E

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[57] **ABSTRACT**

A first coded signal is developed from an input signal in a processor in a transmitter, and the resulting first coded signal is transmitted to a receiving unit which contains an identical processor. The output of the receiving processor is a second signal which is coupled with the first coded signal to a subtraction circuit wherein one of the first and second coded signals is subtracted from the other and the resulting difference signal is coupled through a high gain amplifier to the second processor. The output signal from the high gain amplifier is substantially the same as the original input signal. The processor can develop a coded signal by combining the input signal with one or more time delayed input signals as desired.

12 Claims, 7 Drawing Figures

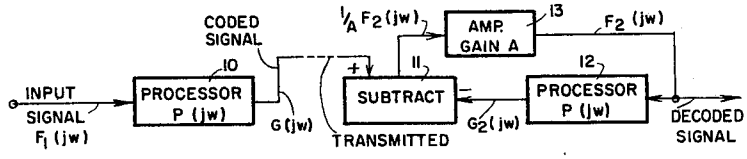


FIG. 1

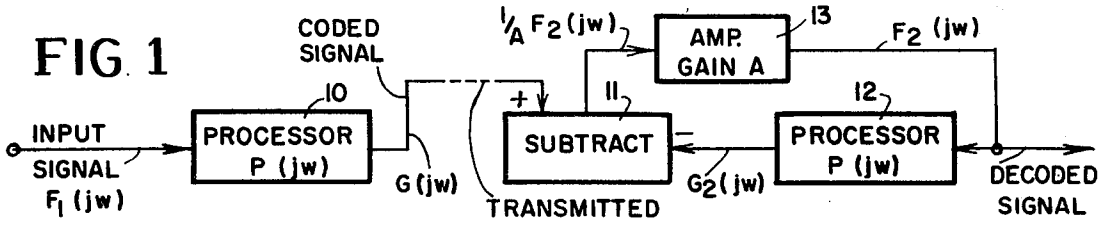


FIG. 2

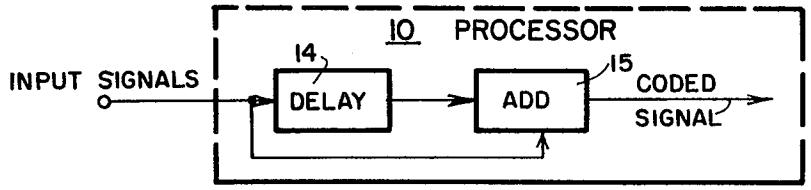
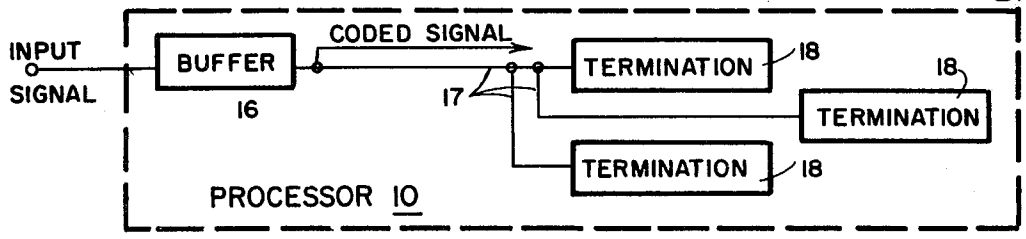


FIG. 3



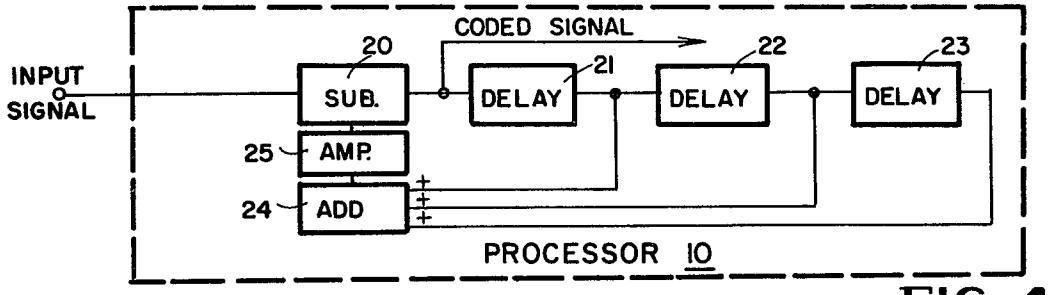


FIG. 4

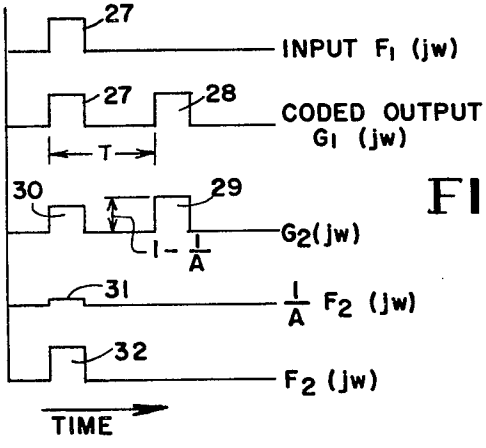


FIG. 5

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FIG. 7

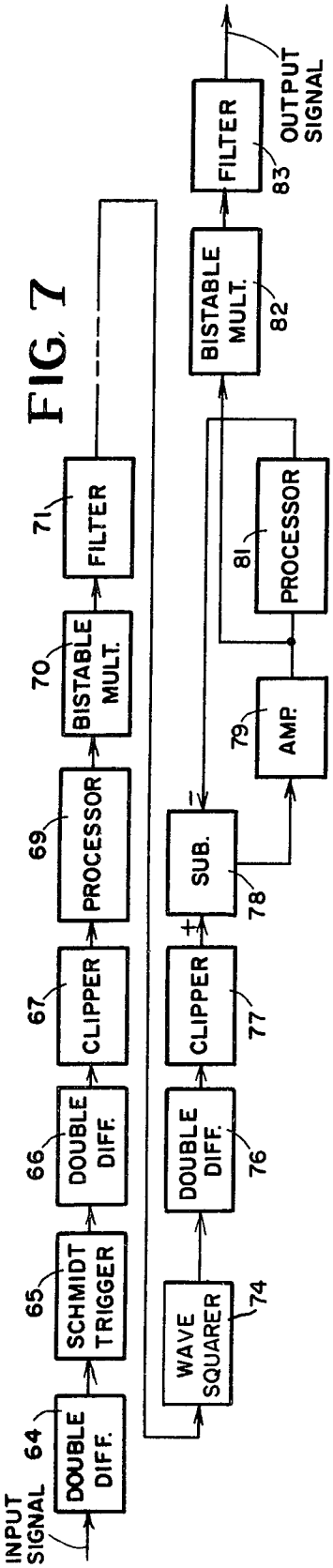
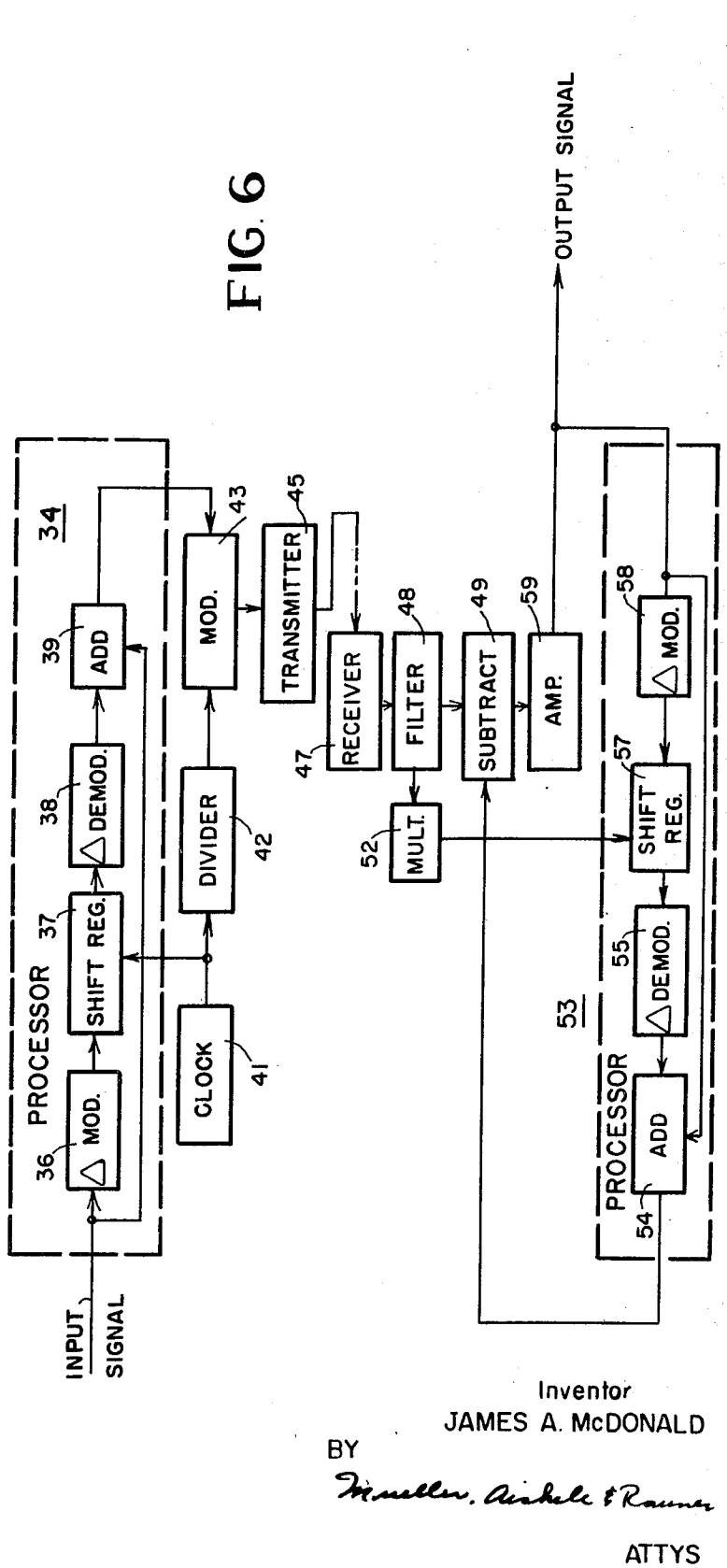


FIG. 6



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SIGNAL CODING AND DECODING SYSTEM

BACKGROUND OF THE INVENTION

In many present day communication systems it is desirable to have some degree of security as to the content of the messages transmitted so that unauthorized persons cannot use the information. This is particularly true in police work where persons can receive the messages merely by tuning a receiver to the proper frequency. Various systems have been developed for coding or scrambling the messages so that they are not easily understood. These systems give a degree of security dependent upon the complexity of the system used.

Systems which have reasonably good degree of security have been complex, expensive and bulky so that their use is limited only to those situations where this extra expense and complexity is warranted. Further, much of the coding is done by digital means so that a relatively high bandwidth is required. In the frequency bands available for two-way communications the spectrum is extremely limited and any coding scheme cannot be allowed to spread the bandwidth of the transmitted signals by a large amount or it will not be usable.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide an improved signal coding system.

Another object of this invention is to provide a signal coding system which is relatively simple and inexpensive.

Another object of this invention is to provide a signal coding system which does not increase the bandwidth of a transmitted signal appreciably.

In practicing this invention a first signal processor is provided which receives an input signal and produces a first coded or scrambled signal therefrom. The coded signal is transmitted through a communications channel to a receiving unit and applied to a subtracting circuit therein. A second signal processor, substantially identical with the first signal processor develops a second coded signal which is coupled to the subtraction circuit. One of the first and second coded signals is subtracted from the other coded signal and the resultant difference signal is coupled to a high gain amplifier. The output of the high gain amplifier is substantially the same as the input signal and is coupled to the second processor for coding thereby.

The signal processors can consist of a delay circuit for delaying the input signal and adding the delayed input signal to the input signal. More than one delayed signal can be used to code the signal as desired. The signal can be converted to a pulse-type of signal by, for example, a delta modulator and a shift register used as the delay. Also the signal can be reduced to a series of pulses representing zero crossings and the position of the zero crossings can be coded. The coded zero crossings can be converted to a coded signal by means of counters and filters.

The invention is illustrated in the drawings of which

FIG. 1 is a block diagram illustrating the operation of the system;

FIG. 2 is a block diagram showing the operation of a processor unit;

FIG. 3 is a block diagram showing the operation of another processor unit;

FIG. 4 is a block diagram showing the operation of yet another processor unit;

FIG. 5 is a set of curves illustrating the operation of the circuit of FIG. 1;

FIG. 6 is another embodiment of the invention in which a shift register is used as the delaying circuit; and

FIG. 7 is a block diagram of an embodiment of the circuit in which the zero crossings are coded.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. 1 there is shown a signal encoder and decoder having the features of this invention. An input signal which is to be coded or scrambled and which is represented by the Fourier transform $F_1(j\omega)$ is coupled to processor **10**. Processor **10** performs the operation $P(j\omega)$ on the input signal $F_1(j\omega)$ to develop a coded signal $G_1(j\omega)$. The coded or scrambled signal $G_1(j\omega)$ is transmitted by any desired means to the decoder and is coupled to a subtraction unit **11**. The other input to the subtraction unit is a coded signal $G_2(j\omega)$. One of the two signals $G_1(j\omega)$ and $G_2(j\omega)$ is subtracted from the other in the subtraction unit **11**, in this example $G_2(j\omega)$ is subtracted from $G_1(j\omega)$, to develop an output signal represented as $1/A\ F_2(j\omega)$.

The signal $1/A\ F_2(j\omega)$ is amplified in amplifier **13**, having a gain of A, to develop a signal $F_2(j\omega)$ which is coupled to processor **12**. Processor **12** is substantially identical to processor **10** and operates on the signal $F_2(j\omega)$ to produce the output signal $G_2(j\omega)$. The signal $F_2(j\omega)$ is substantially identical to the input signal $F_1(j\omega)$ with a very small error between the two signals. The magnitude of this error is dependent upon the gain of amplifier **13** so that the gain of this amplifier is made as large as possible consistent with the requirements of the system.

Referring to FIG. 1

let

$F_1(j)$ be the Fourier transform of the original signal

$P(j\omega)$ be the Fourier transform of processors **10** and **12**

$G_1(j)$ be the Fourier transform of the output of the encoder

$F_2(j)$ be the Fourier transform of the decoded signal

$G_2(j)$ be the Fourier transform of the output of processor **12**

then

$$G_1(j\omega)=F_1(j\omega)\,P(j\omega)$$
$$G_2(j\omega)=F_2(j\omega)\,P(j\omega)$$
$$1/A\,F_2(j\omega)=G_1(j\omega)-G_2(j\omega)$$
$$F_2(j\omega)=A[G_1(j\omega)-G_2(j\omega)]$$
$$F_2(j\omega)=A[F_1(j\omega)-F_2(j\omega)]\,P(j\omega)$$
$$F_2(j\omega)=A\,F_1(j\omega)\,P(j\omega)-A\,F_2(j\omega)\,P(j\omega)$$
$$F_2(j\omega)+A\,F_2(j\omega)\,P(j\omega)=A\,F_1(j\omega)\,P(j\omega)$$

Therefore

$$F_2(j\omega)=\frac{AF_1(j\omega)P(j\omega)}{1+AP(j\omega)}$$

if

$$A\,P(j\omega)\gg 1,\quad 1+A\,P(j\omega)\,A\,P(j\omega)$$

then

$$F_2(j\omega)=F_1(j\omega)$$

Referring to FIG. 2 there is shown a block diagram of a processor suitable for use as processor **10** or **12** of FIG. 1. In the processor of FIG. 2 an input signal is applied to a delay circuit **14** and the output of the delay

circuit is added to the input signal in adder 15 to develop a coded signal.

In FIG. 3 there is shown another processor useful in the system of FIG. 1. An input signal is applied to buffer unit 16. Signals at the output of buffer unit 16 are applied to transmission lines 17. Terminations 18 at the end of transmission lines 17 are selected to produce reflected waves when a signal is present at the output of buffer unit 16. The terminated transmission lines 17 act as the delay lines previously discussed by reflecting the signal at the output of buffer 16 back to the output of buffer 16 delayed in time. The reflected signals combine with the signal at the output of buffer unit 16 to produce the coded signal. Buffer 16 may have a source impedance or termination that will allow a portion of the reflected signal to be reflected back into the transmission line thereby further enhancing the coding.

The amplitude of a reflected wave is related to the transmission line length, transmission line termination, and frequency of input signal. The coded signal of processor 10 in FIG. 3 will, therefore, be time and frequency dependent. Changes in the coding may be accomplished by changing the terminations 18 or the length of transmission lines 17.

In FIG. 4 there is yet another processor which is useful in the system of FIG. 1. An input signal is applied to subtraction unit 20. Another signal is subtracted from the input signal to develop a coded signal. The coded signal is applied to delay lines 21, 22, 23 connected in series and the output of each delay line is coupled back to an adding circuit 24. The signals from each of the delay lines 21, 22 and 23 are added in adder 24 and the resulting signal is subtracted from the input signal in subtraction unit 20.

In order to provide the maximum possible delay, and, therefore, the greatest possible coding in processor 10 of FIG. 4, amplifier 25 may be inserted in processor 10. If the gain of the circuit consisting of subtractor 20, delay lines 21, 22 and 23, adding circuit 24, and amplifier 25, exceeds unity, processor 10 will oscillate. If the magnitude of the oscillation is controlled it will further enhance the coding of the signal when the signals are small in amplitude, however, excessive and continued oscillation will destroy the ability to decode the encoded signal. To prevent this occurrence and provide a controlled oscillation, amplifier 25, a non-linear amplifier of the compression type, is used to reduce the gain of the circuit below unity for signals exceeding a predetermined amplitude.

Referring to FIG. 5 there is shown a series of curves illustrating operation of the circuit of FIGS. 1 and 2. Assuming the input signal consists of a single pulse 27 having unity amplitude, a delayed pulse 28 is generated in the delay line 14 of FIG. 2 and added to the input signal so that the coded signal consists of pulses 27 and 28. Pulse 27 as it is coupled through subtractor 11, will be amplified by amplifier 13, and coupled through processor 12. The output of processor 12 is shown as pulses 29 and 30 with pulse 30 being slightly less than pulse 27. Because of the speed with which the circuit operates pulses 30 and 29 will be coupled to subtractor 11 substantially simultaneously with pulses 27 and 28. In the subtractor the resultant pulse when pulse 30 is subtracted from 27 is shown as pulse 31. This pulse is amplified in amplifier 13 to develop pulse 32, which is substantially the same as pulse 27 and therefore a decoded signal. The difference between pulses 32 and 27 will result in an error signal which can be made as small as the system requires by regulating the gain of amplifier 13.

In FIG. 6 there is shown another embodiment for obtaining the required delay. The input signal is changed into a series of pulses in a known manner by delta modulator 36. The pulses are fed into a shift register 37 and moved through the shift register by timing signals from clock 41. The output of shift register 37 is coupled to a delta demodulator 38 to develop the original signal delayed in time. The delayed signal is added to the original input signal in adder 39 and the resultant coded signal is coupled to a modulator 43. The timing signals from clock 41 are coupled to modulator 43 through a frequency divider 42 which changes the frequency of the timing signal to a value suitable for transmission. The modulation signal from modulator 43, consisting of the coded signal and the timing signal, is coupled to transmitter 35 for transmission to a receiver 47.

The signal received by receiver 47 is coupled to a filter 48 where the timing signal is separated from the coded signal. The timing signal is coupled to a frequency multiplier 52 where it is multiplied in frequency to the frequency of the original timing signal from clock 41. Multiplier 52 is coupled to shift register 57 to step the shift register in response to the timing signal. The coded signal from filter 48 is coupled to subtraction unit 49 in a manner similar to that shown in FIG. 1. The other signal applied to subtraction unit 49 comes from processor 53 and one of the two signals is subtracted from the other to form a difference signal which is amplified in amplifier 59. The output of amplifier 59 is the output signal and is substantially the same as the input signal to delta modulator 36. The output signal is also coupled to delta modulator 58 and the resulting series of pulses is coupled to shift register 57. The timing signal from multiplier 57 steps the series of pulses through the shift register 57 to achieve the delay and the resulting output is formed by delta demodulator 55, into the input signal to adder 54 delayed in time. The delayed signal from delta demodulator 55 is added to the input signal to delta modulator 58 in adder 54 and the resulting coded signal is coupled to subtraction unit 49.

The system of this invention may also be used to scramble the zero crossings of a signal as shown in FIG. 7. An input signal is differentiated twice in double differentiator 64 in order to improve the characteristics of the signal for proper transmission. The output of differentiator 64 is formed into a square wave signal by Schmitt trigger 65. The square wave signal is again differentiated twice in double differentiator 66 and clipped in clipper 67 so that narrow pulses, of a single polarity, representing the time position of the zero crossings are developed. The series of pulses is coupled to a processor 69 which operates in the manner of any of the previously described processors to develop a coded signal, with the coded signal representing the zero crossings. The coded or scrambled signal is then coupled to a bistable multivibrator 70 to develop a square wave output signal with the multivibrator being triggered by each pulse to shift to a different state. The

square wave output is filtered in filter 71 to remove the high frequency components and transmitted as desired.

The received signal is coupled through wave squarer 74 to double differentiator 76 to reproduce the scrambled pulses produced by processor 69, and clipped in clipper 77 to form a series of pulses of a single polarity representing each of the zero crossings. The series of pulses are coupled to subtraction unit 78.

Subtraction unit 78, amplifier 79 and processor 81 operate in a manner similar to the decoders described previously in the specification. The other input to subtraction unit 78 is the output signal from processor 81. One of the two input signals to subtraction unit 78 is subtracted from the other to form a difference signal which is amplified in amplifier 79 and coupled to processor 81. The output signal from amplifier 79 is also coupled to bistable multivibrator 82. Bistable multivibrator 82 is responsive to the series of pulses to form a square wave signal which is filtered in filter 83. The output signal from filter 83 is substantially the same as the input signal applied to the double differentiator 64.

I claim:

1. A system for coding and decoding an input signal including in combination, first signal processor means adapted to receive the input signal and develop therefrom a first coded signal, first subtraction means coupled through a communications channel to said first signal processor means, amplifying means coupled to said first subtraction means, second signal processor means substantially identical to said first signal processor means coupled to said amplifying means and being responsive to the output signal therefrom to develop a second coded signal, said first subtraction means further being coupled to said second signal processor means and acting to subtract one of said first and second coded signals from the other to develop a difference signal, said amplifying means acting to amplify said difference signal to develop an amplifying means output signal, said amplifying means output signal being substantially identical to said input signal.

2. The coding and decoding system of claim 1 wherein, each of said first and second signal processor means includes signal delay means adapted to receive the input signal and to develop a time delay input signal therefrom, signal adding means coupled to said signal delay means and adapted to receive the input signal, said signal adding means acting to add said input signal and said time delayed input signal to develop said first and second coded signal.

3. The coding and decoding system of claim 1 wherein each of said first and second signal processor means includes an input means adapted to receive the input signal, a plurality of transmission line means each having one end coupled to said input means, and termination means coupled to the other ends of said transmission line means, said transmission line means and said termination means reflecting a portion of the signal received from said input means back thereto to combine with said signals at said input means to develop said first and second coded signals.

4. The coding and decoding system of claim 3 wherein said input means reflects a portion of the signal reflected thereto by said transmission line means and said termination means.

5. The coding and decoding system of claim 1 wherein, each of said first and second signal processor means includes a plurality of signal delay means coupled in series and including a first signal delay means adapted to receive said coded signal, each of said plurality of signal delay means acting to delay the signals applied thereto to develop a plurality of time delayed coded signals, signal adding means coupled to each of said signal delay means and acting to add said plurality of time delayed coded signals and develop thereby a combined coded signal, second subtraction means adapted to receive the input signal and being coupled to said signal adding means and said first signal delay means, said second subtraction means acting to subtract one of said combined coded signal and the input signal from he other to develop said first and second coded signal.

6. The coding an decoding system of claim 5 further including amplification means coupled between said adding means and subtraction means to amplify said combined coded signal thereby providing an improved first and second coded signal.

7. The coding and decoding system of claim 6 wherein said amplification means is an amplifier of the compression type.

8. The coding and decoding system of claim 2 wherein, said signal delay means includes, pulse means for receiving the input signal and converting the same to a series of pulses representative of the input signal, shift register means coupled to said pulse means for receiving and storing said series of pulses, pulse demodulation means coupled to said shift register means and said signal adding means, said pulse demodulation means acting to demodulate said series of pulses to develop said time delayed input signal, said coding and decoding system further including, clock means coupled to said shift register means of said first signal processor means for applying a clock signal thereto to step said series of pulse signals therethrough, modulator means coupled to said first signal processor means and said clock means for combining said clock signal and said coded signal, transmission means coupled to said modulator means for transmitting said combined signal, and means for receiving said combined signal and including filter means acting to separate said clock signal and said coded signal, said filter means being coupled to said first subtraction means for applying said coded signal thereto and further being coupled to said shift register means of said second signal processor means for applying said clock signal thereto.

9. The coding and decoding system of claim 8 wherein, said pulse means is a delta modulator and said pulse demodulation means is a delta demodulator.

10. The coding and decoding system of claim 8, further including frequency divider means coupling said clock means to said modulator means for reducing the frequency of the clock signal applied thereto and frequency multiplier means coupling said filter means to said shift register means of said second signal processor means for increasing the frequency of the clock signal applied thereto to the original clock frequency.

11. A coding and decoding system for scrambling and unscrambling an input signal, including in combination, first means for receiving the input signal and

developing therefrom a first square wave signal representative of the input signal, first double differentiation and clipper means coupled to said first receiving means and responsive to said first square wave signal to develop a first pulse signal with all of the pulses therein being of one polarity and representative of each of the zero crossings of said first square wave signal, first signal processor means coupled to said first double differentiation and clipper means and acting to develop a first coded pulse signal, first bistable multivibrator means coupled to said first signal processor means and responsive to said first coded pulse signal to develop a second square wave signal therefrom, first filter means coupled to said first bistable multivibrator means for filtering said second square wave signal, to develop a band limited signal, transmission channel means coupled to said first filter means, second means coupled to said signal transmission channel means and being responsive to said band limited signal to develop therefrom a third square wave signal representative of said band limited signal, second double differentiation and clipper means responsive to said third square wave signal to develop a second pulse signal with all of the pulses therein being of one polarity and representative of each of the zero crossings of said third square wave signal, subtraction means coupled to said double differentiation and clipper means, second signal processor means substantially identical to said first signal processor means coupled to said subtraction means, and amplifying means coupling said subtraction means to said second signal processor means, said second signal processor means being responsive to the output signal from said amplifying means to develop a second coded pulse signal, said subtraction means acting to subtract one of said second pulse signal and said second coded pulse signal from the other to develop a difference signal, said amplifying means acting to amplify said difference signal to develop an amplifying means output signal, second bistable multivibrator means coupled to said amplifying means and being responsive to said amplifying means output signal to develop a fourth square wave signal therefrom and second filter means coupled to said second bistable multivibrator means for filtering said fourth square wave signal to develop an output signal therefrom substantially identical to said input signal.

12. The coding and decoding system of claim 11 wherein, each of said first and second signal processor means includes signal delay means adapted to receive the signal applied to said first and second signal processor means and to develop a time delayed applied signal therefrom, signal adding means adapted to receive the applied signal and coupled to said signal delay means, said signal adding means acting to add said applied signal and said time delayed applied signal to develop said first and second coded pulse signals.

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