

ELECTROMAGNETICALLY SHIELDED ELECTRONIC DEVICES AND RELATED SYSTEMS AND METHODS

Technical Field

[0001] Embodiments described herein relate generally to electromagnetically shielded electronic devices.

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Background

[0002] Electromagnetic interference (EMI) shielding for an electronic device package (e.g., a system-in-a-package (SiP)) can be created using a physical vapor deposition (PVD) process such as sputtering. For example, an
10 electrically conductive material can be deposited onto an exposed molded surface of the package (e.g., a mold compound such as an electronic grade epoxy) to create an EMI shield layer. For EMI shielding between components of the package, a trench can be made by a laser through the mold compound at a location between the components. The trench is then filled with a conductive
15 material prior to depositing the EMI layer material on the surface of the mold compound.

Brief Description of the Drawings

[0003] Invention features and advantages will be apparent from the detailed
20 description which follows, taken in conjunction with the accompanying drawings, which together illustrate, by way of example, various invention embodiments; and, wherein:

[0004] FIG. 1 illustrates an exemplary substrate having conductor pads and electronic components mounted thereon;

25 **[0005]** FIG. 2 illustrates an example of an insulating layer, such as a conformal insulating layer encapsulating conductor pads and electronic components on a substrate;

[0006] FIG. 3 illustrates an example of an insulating layer insulating layer

encapsulating conductor pads and electronic components on a substrate with openings formed to expose the conductor pads;

5 [0007] FIG. 4 illustrates an example of an electrically conductive or EMI layer formed on an insulating layer encapsulating electronic components on a substrate;

[0008] FIG. 5 illustrates an example of a device package with an encapsulation layer over an electrically conductive or EMI layer formed on an insulating layer encapsulating electronic components on a substrate;

10 [0009] FIG. 6 illustrates another example of a substrate having conductor pads and electronic components mounted thereon;

[0010] FIG. 7 illustrates an example of an insulating layer, such as a conformal insulating layer encapsulating electronic device components and conductor pads on a substrate;

15 [0011] FIG. 8 illustrates an example of an electrically conductive EMI layer formed on an insulating layer encapsulating electronic components on a substrate;

[0012] FIG. 9 illustrates an example of singulating or separating individual electronic device packages from one another;

20 [0013] FIG. 10 illustrates an example of singulating or separating individual electronic device packages with an encapsulation layer on an electrically conductive layer from one another;

[0014] FIG. 11 is a schematic illustration of an exemplary computing system.

25 [0015] Reference will now be made to exemplary invention embodiments and specific language will be used herein to describe the same. It will nevertheless be understood that no limitation of the technology scope or to specific invention embodiments is thereby intended.

Description of Embodiments

[0016] Before invention embodiments are disclosed and described, it is to be

understood that no limitation to the particular structures, process steps, or materials disclosed herein is intended, but also includes equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of
5 describing particular examples and is not intended to be limiting. The same reference numerals in different drawings represent the same element. Numbers provided in flow charts and processes are provided for clarity in illustrating steps and operations and do not necessarily indicate a particular order or sequence. Unless defined otherwise, all technical and scientific terms used herein have the
10 same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs.

[0017] As used in this specification and the appended claims, the singular forms “a,” “an” and “the” include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to “an electronic component” includes
15 a plurality of such electronic components.

[0018] In this disclosure, “comprises,” “comprising,” “containing” and “having” and the like can have the meaning ascribed to them in U.S. Patent law and can mean “includes,” “including,” and the like, and are generally interpreted to be open ended terms. The terms “consisting of” or “consists of” are closed terms,
20 and include only the components, structures, steps, or the like specifically listed in conjunction with such terms, as well as that which is in accordance with U.S. Patent law. “Consisting essentially of” or “consists essentially of” have the meaning generally ascribed to them by U.S. Patent law. In particular, such terms are generally closed terms, with the exception of allowing inclusion of
25 additional items, materials, components, steps, or elements, that do not materially affect the basic and novel characteristics or function of the item(s) used in connection therewith. For example, trace elements present in a composition, but not affecting the composition’s nature or characteristics would be permissible if present under the “consisting essentially of” language, even
30 though not expressly recited in a list of items following such terminology. When using an open ended term, like “comprising” or “including,” in this specification, it is understood that direct support should be afforded also to “consisting

essentially of” language as well as “consisting of” language as if stated explicitly and vice versa.

[0019] The terms “first,” “second,” “third,” “fourth,” and the like in the description and in the claims, if any, are used for distinguishing between similar elements
5 and not necessarily for describing a particular sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments described herein are, for example, capable of operation in sequences other than those illustrated or otherwise described herein. Similarly, if a method is described herein as
10 comprising a series of steps, the order of such steps as presented herein is not necessarily the only order in which such steps may be performed, and certain of the stated steps may possibly be omitted and/or certain other steps not described herein may possibly be added to the method.

[0020] The terms “left,” “right,” “front,” “back,” “top,” “bottom,” “over,” “under,”
15 and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments described herein are, for example, capable of operation in other orientations than those illustrated or otherwise
20 described herein. The term “coupled,” as used herein, is defined as directly or indirectly connected in an electrical or nonelectrical manner. Objects described herein as being “adjacent to” each other may be in physical contact with each other, in close proximity to each other, or in the same general region or area as each other, as appropriate for the context in which the phrase is used.
25 Occurrences of the phrase “in one embodiment,” or “in one aspect,” herein do not necessarily all refer to the same embodiment or aspect.

[0021] As used herein, the term “substantially” refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is “substantially” enclosed would
30 mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness

may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of “substantially” is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is “substantially free of” particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is “substantially free of” an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

[0022] As used herein, the term “about” is used to provide flexibility to a numerical range endpoint by providing that a given value may be “a little above” or “a little below” the endpoint.

[0023] As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

[0024] Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of “about 1 to about 5” should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values

such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

[0025] This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply
5 regardless of the breadth of the range or the characteristics being described.

[0026] Reference throughout this specification to “an example” means that a particular feature, structure, or characteristic described in connection with the example is included in at least one embodiment. Thus, appearances of the phrases “in an example” in various places throughout this specification are not
10 necessarily all referring to the same embodiment.

Example Embodiments

[0027] An initial overview of technology embodiments is provided below and specific technology embodiments are then described in further detail. This initial
15 summary is intended to aid readers in understanding the technology more quickly but is not intended to identify key or essential features of the technology nor is it intended to limit the scope of the claimed subject matter.

[0028] Current processes for electromagnetically shielding electronic devices in an electronic device package have certain drawbacks. In particular, laser
20 trenching through a thick layer of epoxy mold compound in order to expose electrical pads is a time consuming process. In addition, a minimum aspect ratio of 1.0 for the mold compound thickness and the spacing between components is required for laser trenching. The thickness of the mold compound therefore puts limitations on the minimum spacing between
25 components.

[0029] Certain invention embodiments provide methods of making an electronic device package with reduces or minimized time as compared to currently used processes, thereby reducing cost. Another advantage is the ability to reduce or minimize spacing between components, thus reducing package size. Such
30 methods can include: providing a substrate having a conductor pad and an

electronic component; encapsulating the electronic component on the substrate with an insulating layer; exposing the conductor pad; and forming an electrically conductive EMI layer on the insulating layer and in contact with the conductor pad. Such methods can further include coating the EMI layer with an
5 encapsulation layer or outer encapsulation layer. Such methods can apply to any technology that utilizes EMI shielding of components, including EMI shielding between components or for groups of components.

[0030] Referring to FIGS. 1-5, an exemplary method of making an electromagnetically shielded electronic device package is illustrated. In
10 particular, the electronic device package in this example will include EMI shielding about one or more electronic components, such as those found in a SiP, where a variety of closely spaced components are to be individually shielded from one another. The method can include providing or obtaining a substrate 110 having one or more conductor pads 112a-d (e.g., grounding
15 pads) and one or more electronic components 120-122 mounted on the substrate 110, as illustrated in FIG. 1. The electronic components 120-122 can comprise dies, processors, chips, packaged components and other devices, including as passives, etc. The electronic components 120-122 can be mounted on the substrate 110 in any suitable manner. Some electronic
20 components, as represented by the electronic components 121, 122, can have underfill 123, 124 applied to flip chip bonded dies.

[0031] The method can also include forming an insulating layer, such as a conformal insulating layer 130 on the substrate 110 and electronic components 120-122, as illustrated in FIG. 2. The conformal insulating layer 130 can be
25 formed about the electronic components 120-122 such that the insulating layer 130 conforms to the electronic components 120-122. The conformal insulating layer 130 can be formed of any suitable material (e.g., a dielectric material). In some embodiments, the conformal insulating layer 130 can be a thin layer from about 10 nm to about 100 μm thick, which may vary depending on the technique
30 or process utilized to form the layer 130. For example, the conformal insulating layer 130 can be very thin, for example about 10 nm thick when using a spray

process to form the layer 130, or about 50 μm when using a dispense or print approach to form the layer 130. The thickness of the conformal insulating layer 130 can therefore depend on filler size or type and the technique utilized to form the layer 130 (e.g., deposition by spraying, printing, dispensing, and/or lamination). In addition, the thickness of the conformal insulating layer 130 can depend on the gap or spacing (e.g., the lateral distance) in between the electronic components 120-122. In other words, the conformal insulating layer 130 should fit between adjacent electronic components that are to be shielded from one another. Thus, the thickness of the conformal insulating layer 130 will be thinner than the gap or spacing between such electronic components. In general, a thinner layer 130 may be more desirable to ensure that each of the electronic components 120-122 can be compartmentally shielded. On the other hand, the conformal insulating layer 130 should be formed to cover the electronic components 120-122 without pinholes in order to avoid a bridge between the electronic components 120-122 and the conformal insulating layer 130. As the thickness of the insulating layer 130 decreases, the process time required to manufacture the electronic device package also decreases. Reducing the thickness of the insulating layer 130 can also provide for reduced spacing between the electronic components 120, 121 and between the electronic components 121, 122, which can reduce the size of the electronic device package containing such components.

[0032] The conformal insulating layer 130 can conform individually to one or more of the electronic components 120-122. Although the conformal insulating layers in the figures are illustrated as having linear and/or planar outer surfaces, it should be recognized that outer surfaces of conformal insulating layers can have any suitable configuration, such as curved and/or angled surfaces, to conform to one or more electronic components. Exposed surfaces of the electronic devices 120-122 and the substrate 110 can be conformally coated with an insulating (e.g., a dielectric) material by any suitable technique, such as using a deposition process (e.g., atomization or sputtering), a spraying process, a printing process, a lamination process, a molding process, etc. Such processes of forming the conformal insulating layer 130 can result in the

conductor pads 112a-d being covered by the conformal insulating layer 130.

[0033] Thus, the method can further include exposing the conductor pads 112a-d, as illustrated in FIG. 3, to facilitate electrically coupling EMI shielding to the conductor pads 112a-d. The conductor pads 112a-d can be exposed by

5 forming openings 113a-d through the conformal insulating layer 130 to the conductor pads 112a-d, respectively. The openings 113a-d can be of any suitable configuration (e.g., a trench, a slot, a via, a hole, etc.) to facilitate electrically coupling EMI shielding with the conductor pads 112a-d. Such openings 113a-d can be formed through the thin conformal insulating layer 130

10 to the conductor pads 112a-d by any suitable technique, such as excimer laser ablation, laser assisted chemical etching, ion milling through a mask, etc. By reducing or minimizing the thickness of the insulating layer 130, the amount of material removed to form the openings 113a-d can also be reduced or minimized, thereby reducing or minimizing the process time required to

15 manufacture the electronic device package. In other words, conformal coating of the thin insulating layer 130 of material can facilitate the use of excimer laser ablation or other suitable technique for exposing the conductor pads 112a-d through the thin insulating layer 130, which can reduce the process time for exposure of the conductor pads 112a-d when compared to a typical process of

20 UV/IR laser ablation through thick mold material over a ground pad. In one aspect, use of a reduced projection excimer laser can facilitate the formation of small openings, such as about 10 μm wide trenches. Excimer laser ablation patterning of thin insulating layer 130 can make a trench width or a via hole diameter smaller than with deep trench laser drilling through thick epoxy mold

25 compound, typically utilized to create shielding partitions between on-board components. This can facilitate a reduction in spacing between the electrical components 120-122 and in the size of the conductor pads 112a-d, which can lead to a size reduction of a SiP package foot print. The thin conformal layer 130 can also provide for a reduction in package thickness. In addition, excimer

30 laser ablation using a photomask can be employed to simultaneously form multiple openings. For example, multiple trenches and/or vias for closely spaced electrical components can be made at the same time using a

photomask assisted excimer laser ablation process. Utilizing photomask assisted excimer laser ablation can provide for very fast fabrication of multiple openings (e.g., trenches and/or vias) simultaneously when compared to the typical UV/IR laser ablation for one electrical component at a time. Utilizing
5 laser assisted chemical etching or ion milling through a mask to expose the conductor pads 112a-d may provide similar benefits and advantages.

[0034] With the conductor pads 112a-d exposed, an electrically conductive or electromagnetic interference (EMI) layer 140 can be formed on the insulating layer 130, as illustrated in FIG. 4, for an electromagnetic shield associated with
10 the substrate 110. The electrically conductive layer 140 can be in contact with, or make a connection to, the conductor pads 112a-d by extending through the openings 113a-d. The electrically conductive material and the layer 140 thickness can be of any suitable type and thickness to form a conformal shielding overcoat. In one aspect, the electrically conductive material and
15 thickness can be defined by electrical conductivity, magnetic permeability, and/or EMI shielding requirements. The electrically conductive layer 140 can be formed by any suitable technique, such as a deposition process (e.g., atomization or sputtering), a plating process, a spraying process, a printing process, a lamination process, a molding process, etc. Conformal coating of
20 electrically conductive layer 140 material can also provide for a reduction in thickness of the electronic device package.

[0035] In one aspect, due to the insulating layer 130 conforming about the electrical components 120-122, the electrically conductive layer 140 can be formed about the electronic components 120-122 individually. The conformal
25 insulating layer 130 can also facilitate a plurality of electrically conductive layer portions 141a-b, 142a-b to be disposed between electrical components, in contrast to a single electrical conductor-filled trench between components resulting from the typical UV/IR laser ablation process. For example, the electrically conductive layer portions 141a-b can be disposed between the
30 electrical components 120, 121, and the electrically conductive layer portions 142a-b can be disposed between the electrical components 121, 122. The

electrically conductive layer 140 can be connected to the conductor pad 112b between the electrical components 120, 121, and to the conductor pad 112c between the electrical components 121, 122. In addition, by forming the electrically conductive layer 140 about the electrical components 120-122 at the same time (e.g., by a deposition process), the side portions 141a-b, 142a-b of the electrically conductive layer 140 can be integrally formed with top portions of the electrically conductive layer 140, in contrast to the separately formed electrical conductor-filled trench and electrical conductor deposited on a mold compound surface as a result of the typical process. For example, the side portion 141a can be integrally formed with a top portion 143a, the side portions 141b, 142a can be integrally formed with a top portion 143b, and the side portion 142b can be integrally formed with a top portion 143c. Although the side portions (e.g., side portions 141a-b, 142a-b) of the electrically conductive layer 140 are illustrated as being oriented perpendicular to the top surface of the substrate 110, one or more side portions of the electrically conductive layer 140 can be oriented at a non-perpendicular angle relative to the top surface of the substrate. In some aspects, the electrically conductive layer can be a continuous layer of a single material extending across the entire electronic device package, and can be formed as such.

[0036] With the electrically conductive layer 140 in place, an electronic device package 100 can be singulated or physically separated from other packages into individual packages. The electronic device package 100 can also be prepared for electrically coupling with another component (e.g., a motherboard), such as by attaching solder balls (not shown) on a back side 111 of the electronic device package.

[0037] In one aspect, the method can optionally include forming an encapsulation layer 150 (i.e. an outer layer, top layer, or protective layer) on the electrically conductive layer 140, as illustrated in FIG. 5, to protect the electrically conductive layer 140 and other components of an electronic device package. The encapsulation layer 150 can be formed by any suitable technique (e.g., transfer or compression molding) using any suitable encapsulation material, such as a molding compound (e.g., an electronic grade epoxy). In one

aspect, due to the conformal insulating and electrically conductive layers 130, 140 about the electrical components 120-122, the portions of the encapsulation layer 150 can be disposed between electrical components. For example, an encapsulation layer portion 151 can be disposed between the electrical components 120, 121, and an encapsulation layer portion 152 can be disposed between the electrical components 121, 122.

[0038] With the encapsulation layer 150 in place, an electronic device package 100' can be singulated or physically separated from other packages into individual packages. The electronic device package 100' can also be prepared for electrically coupling with another component (e.g., a motherboard), such as by attaching solder balls (not shown) on a back side 111 of the electronic device package.

[0039] FIGS. 6-10 illustrate a method of making an electromagnetically shielded electronic device package in accordance with another example of the present disclosure. In particular, the package in this example will include EMI shielding about one or more electronic components at the unit or strip level (e.g., containing multiple units). The method can include providing or obtaining a substrate 210 having one or more conductor pads 212a-b, 212a'-b' and one or more electronic components 220, 221, 220', 221' mounted on the substrate 210, as illustrated in FIG. 6. The electronic components 220, 221 form a first group of electronic components and the electronic components 220', 221' can form a second group of electronic components associated with respective first and second portions 214, 214' of the substrate 210. The conductor pads 212a-b, 212a'-b' are exposed at a surface 215 of the substrate 210.

[0040] The method can also include forming insulating layers, such as conformal insulating layers 230, 230' on the substrate 210 and electronic components 220, 221, 220', 221', as illustrated in FIG. 7. The conformal insulating layer 230 can be formed about the electronic components 220, 221, 220', 221' such that the insulating layer 230 conforms to the first group of electronic components 220, 221, and the insulating layer 230' conforms to the second group of electronic components 220', 221'. The conformal insulating

layers 230, 230' can be formed by any suitable technique, such as a deposition process (e.g., atomization or sputtering), a spraying process, a printing process, a lamination process, a molding process, etc. FIG. 7 illustrates forming the conformal insulating layers 230, 230' by molding an insulating material. In this example, a mold chase 260 can be used in a molding process, such as a transfer or compression molding process to apply the conformal insulating layers 230, 230' about the electronic components 220, 221, 220', 221'.

[0041] The method can further include exposing the conductor pads 212a-b, 212a'-b' to facilitate electrically coupling EMI shielding to the conductor pads 212a-b, 212a'-b'. The conductor pads 212a-b, 212a'-b' can be exposed by masking the conductor pads such that the conformal insulating layers 230, 230' are prevented from contacting at least a portion of the conductor pads 212a-b, 212a'-b'. As illustrated in FIG. 7, the conductor pads 212a-b, 212a'-b' can be masked by covering the conductor pads 212a-b, 212a'-b' with the mold chase 260. Thus, a mold process can be utilized to apply an insulating material around the electronic components 220, 221, 220', 221' but not completely covering the conductor pads 212a-b, 212a'-b' at the surface 215 of the substrate 210. The amount and degree to which the conductor pad is covered can be adjusted by utilizing an appropriate mold chase. In one example, the conductor pad can be free of, such as completely free of insulator material following application of the insulating material around the electronic components. In another example, the conductor pad can be partially covered. In a further example the conductor pad can have at least 10% of its surface exposed. In another example, the conductor pad can have 15% to 95% of its surface exposed. With at least some portion of each of the conductor pads 212a-b, 212a'-b' remaining exposed, there is no need to remove insulating layer 230 material to provide access for an EMI shielding connection. Thus, the process time required to manufacture the electronic device package can be reduced due to the absence of a material removal process to expose the conductor pads.

[0042] In one aspect, a mold process can be employed where the conductor pads 212a-b, 212a'-b' are completely covered by insulating material (i.e., a thin

layer) at the surface of the substrate 210. In this case, the conductor pads 212a-b, 212a'-b' can be exposed as in the example discussed above with regard to FIGS. 1-5 (e.g., laser ablation).

[0043] With the conductor pads 212a-b, 212a'-b' exposed, the method can include forming electrically conductive or electromagnetic interference (EMI) layers 240, 240' on the insulating layers 230, 230', respectively, as illustrated in FIG. 8, for electromagnetic shields associated with the substrate 210. The electrically conductive layers 240, 240' can be in contact with, or make a connection to, the conductor pads 212a-b, 212a'-b'. For example, the electrically conductive layer 240 can be in contact with the conductor pads 212a-b, and the electrically conductive layer 240' can be in contact with the conductor pads 212a'-b'. The electrically conductive layers 240, 240' can be formed by any suitable technique, such using a deposition process (e.g., atomization or sputtering), a plating process, a spraying process, a printing process, a lamination process, a molding process, etc. FIG. 8 illustrates forming the electrically conductive layers 240, 240' by molding an electrically conductive material. In this example, a mold chase 262 can be used in a transfer or compression molding process to form the electrically conductive layers 240, 240' on the insulating layers 230, 230' about the electronic components 220, 221, 220', 221'. Conformal coating of the electrically conductive material layer 240, 240' can provide for a reduction in thickness of an electronic device package.

[0044] In addition, by forming the electrically conductive layers 240, 240' on the insulating layers 230, 230' and about the electronic components 220, 221, 220', 221' at the same time (e.g., by a molding process), the side portions 241a-b, 241a'-b' of the electrically conductive layers 240, 240' can be integrally formed with top portions of the electrically conductive layers 240, 240', respectively. For example, the side portions 241a-b can be integrally formed with a top portion 243, and the side portions 241a'-b' can be integrally formed with a top portion 243'. Although the side portions side portions 241a-b, 241a'-b' of the electrically conductive layers 240, 240' are illustrated as being oriented perpendicular to the top surface of the substrate 210, one or more of the side

portions 241a-b, 241a'-b' can be oriented at a non-perpendicular angle relative to the top surface of the substrate.

[0045] With the electrically conductive layer 240 in place, electronic device packages 200, 200' can be singulated or separated from one another into individual packages, as illustrated in FIG. 9. For example, the first and second portions 214, 214' of the substrate 210 can be separated to form the electronic device packages 200, 200'. The substrate 210 can be separated in any suitable manner, such as sawing with a saw blade 270. The electronic device packages 200, 200' can also be prepared for electrically coupling with another component (e.g., a motherboard), such as by attaching solder balls (not shown) on back sides 211, 211' of the packages.

[0046] In one aspect, the method can optionally include forming an encapsulation (i.e. a top, outer, or protective) layer 250 on the electrically conductive layers 240, 240', as illustrated in FIG. 10, to protect the electrically conductive layers 240, 240' and other components of electronic device packages 201, 201'. The encapsulation layer 250 can be formed by any suitable technique (e.g., transfer or compression molding) using any suitable encapsulation material, such as a molding compound (e.g., an electronic grade epoxy). In this example, a portion of the encapsulation layer 250 is in contact with the substrate 210 (e.g., the top surface of the substrate).

[0047] With the encapsulation layer 250 in place, the electronic device packages 201, 201' can be singulated or separated from one another into individual packages, as illustrated in FIG. 10. For example, the first and second portions 214, 214' of the substrate 210 and the encapsulation layer 250 can be separated to form the electronic device packages 201, 201'. The substrate 210 and the encapsulation layer 250 can be separated in any suitable manner, such as sawing with the saw blade 270. The electronic device packages 201, 201' can be prepared for electrically coupling with another component (e.g., a motherboard), such as by attaching solder balls (not shown) on back sides 211, 211' of the packages.

[0048] Thus, in one embodiment an electronic device package with a single die

or multiple dies can made at the strip level, where the formation of the conformal insulating layer, the electrically conductive layer, and the (optional) encapsulation layer can be made using sequential molding processes as an alternative to making such packages using a laser ablation process, which may
5 be used to expose conductor pads.

[0049] In one aspect, illustrated in FIG. 11, an electronic device package 300 as disclosed herein can form part of a computing system 302. The computing system 302 can include a motherboard 380, as well as a processor 381, a memory device 382, a radio 383, a heat sink 384, a port 385, a slot, or any
10 other suitable device, which can be operably coupled to the motherboard 380. The computing system 302 can comprise any type of computing system, such as a desktop computer, a laptop computer, a tablet computer, a smartphone, a server, etc.

15 Examples

[0050] The following examples pertain to further embodiments.

[0051] In one example a method of making an electronic device package is provided, comprising: providing a substrate having a conductor pad and an electronic component; forming a conformal insulating layer on the substrate and
20 electronic component, wherein the conformal insulating layer conforms to the electronic component; exposing the conductor pad, or at least a portion of the conductor pad; and forming an electrically conductive electromagnetic interference (EMI) layer on the insulating layer and in contact with the conductor pad.

[0052] In one example of a method of making an electronic device package, exposing the conductor pad comprises forming an opening through the conformal insulating layer to the conductor pad, wherein the electrically conductive layer extends into the opening in contact with the conductor pad.

[0053] In one example of a method of making an electronic device package,
30 forming an opening through the conformal insulating layer comprises ablating the

conformal insulating layer with a laser.

[0054] In one example of a method of making an electronic device package, exposing the conductor pad comprises masking the conductor pad such that the conformal insulating layer is prevented from contacting at least a portion of the conductor pad.

[0055] In one example of a method of making an electronic device package, masking the conductor pad comprises covering the conductor pad with a mold chase, wherein forming the conformal insulating layer comprises molding an insulating material.

[0056] In one example of a method of making an electronic device package, the electronic component comprises a first electronic component and a second electronic component.

[0057] In one example of a method of making an electronic device package, the conformal insulating layer conforms individually to at least one of the first electronic component and the second electronic component.

[0058] In one example of a method of making an electronic device package, the first electronic component and the second electronic component form a group of electronic components, and the conformal insulating layer conforms to the group of electronic components.

[0059] In one example of a method of making an electronic device package, a plurality of conductive layer portions is disposed between the first and second electronic components.

[0060] In one example of a method of making an electronic device package, the electrically conductive layer is formed about the first and second electronic components individually.

[0061] In one example of a method of making an electronic device package, forming a conformal insulating layer comprises depositing an insulating material.

[0062] In one example of a method of making an electronic device package, depositing the insulating material comprises atomizing the insulating material.

[0063] In one example of a method of making an electronic device package, forming a conformal insulating layer comprises molding an insulating material.

[0064] In one example of a method of making an electronic device package, forming the electrically conductive layer comprises depositing an electrically conductive material.

5 **[0065]** In one example of a method of making an electronic device package, depositing the electrically conductive material comprises at least one of atomizing, printing, sputtering, and plating the electrically conductive material.

[0066] In one example of a method of making an electronic device package, forming the electrically conductive layer comprises molding an electrically conductive material.

10 **[0067]** In one example of a method of making an electronic device package, the method further comprises forming an encapsulation layer on the electrically conductive layer.

15 **[0068]** In one example of a method of making an electronic device package, the electronic component comprises a first electronic component and a second electronic component, wherein at least a portion of the encapsulation layer is disposed between the first electronic component and the second electronic component.

[0069] In one example of a method of making an electronic device package, portion of the encapsulation layer is in contact with the substrate.

20 **[0070]** In one example of a method of making an electronic device package, forming an encapsulation layer comprises molding an encapsulation material.

[0071] In one example of a method of making an electronic device package, the encapsulation material comprises an epoxy.

25 **[0072]** In one example of a method of making an electronic device package, the electronic component comprises a first electronic component and a second electronic component associated with respective first and second portions of the substrate, the method further comprising separating the first and second portions of the substrate to form first and second electronic device packages.

30 **[0073]** In one example of a method of making an electronic device package, separating the first and second portions of the substrate comprises cutting the substrate.

[0074] In one example of a method of making an electronic device package, a

side portion of the electrically conductive layer is integrally formed with a top portion of the electrically conductive layer.

5 **[0075]** In one example of a method of making an electronic device package, a side portion of the electrically conductive layer is oriented at a non-perpendicular angle relative to a top surface of the substrate.

10 **[0076]** In one example, there is provided a method of electromagnetically shielding an electronic device package comprising: forming a conformal insulating layer about an electronic component mounted on a substrate, wherein the conformal insulating layer conforms to the electronic component; and forming an electrically conductive layer on the insulating layer and in contact with a conductor pad on the substrate for an electromagnetic shield associated with the substrate.

15 **[0077]** In one example of a method of electromagnetically shielding an electronic device package, the conductor pad is covered by the conformal insulating layer, the method further comprising forming an opening through the conformal insulating layer to the conductor pad, wherein the electrically conductive layer extends into the opening in contact with the conductor pad.

20 **[0078]** In one example of a method of electromagnetically shielding an electronic device package, forming the opening through the conformal insulating layer comprises ablating the conformal insulating layer with a laser.

25 **[0079]** In one example of a method of electromagnetically shielding an electronic device package, the method further comprises masking the conductor pad such that the conformal insulating layer is prevented from contacting at least a portion of the conductor pad.

30 **[0080]** In one example of a method of electromagnetically shielding an electronic device package, masking the conductor pad comprises covering the conductor pad with a mold chase, wherein forming the conformal insulating layer comprises molding an insulating material.

30 **[0081]** In one example of a method of electromagnetically shielding an electronic device package, the electronic component comprises a first electronic component and a second electronic component.

[0082] In one example of a method of electromagnetically shielding an electronic device package, the conformal insulating layer conforms individually to at least one of the first electronic component and the second electronic component.

5 **[0083]** In one example of a method of electromagnetically shielding an electronic device package, the first electronic component and the second electronic component form a group of electronic components, and the conformal insulating layer conforms to the group of electronic components.

10 **[0084]** In one example of a method of electromagnetically shielding an electronic device package, a plurality of conductive layer portions is disposed between the first and second electronic components.

[0085] In one example of a method of electromagnetically shielding an electronic device package, the electrically conductive layer is formed about the first and second electronic components individually.

15 **[0086]** In one example of a method of electromagnetically shielding an electronic device package, forming the conformal insulating layer comprises depositing an insulating material.

[0087] In one example of a method of electromagnetically shielding an electronic device package, depositing the insulating material comprises atomizing the insulating material.

20 **[0088]** In one example of a method of electromagnetically shielding an electronic device package, forming the conformal insulating layer comprises molding an insulating material.

25 **[0089]** In one example of a method of electromagnetically shielding an electronic device package, forming the electrically conductive layer comprises depositing an electrically conductive material.

[0090] In one example of a method of electromagnetically shielding an electronic device package, depositing the electrically conductive material comprises at least one of atomizing, printing, sputtering, and plating the electrically conductive material.

30 **[0091]** In one example of a method of electromagnetically shielding an

electronic device package, forming the electrically conductive layer comprises molding an electrically conductive material.

5 **[0092]** In one example of a method of electromagnetically shielding an electronic device package, the method further comprises forming an encapsulation layer on the electrically conductive layer.

10 **[0093]** In one example of a method of electromagnetically shielding an electronic device package, the electronic component comprises a first electronic component and a second electronic component, wherein at least a portion of the encapsulation layer is disposed between the first electronic component and the second electronic component.

[0094] In one example of a method of electromagnetically shielding an electronic device package, a portion of the encapsulation layer is in contact with the substrate.

15 **[0095]** In one example of a method of electromagnetically shielding an electronic device package, forming the encapsulation layer comprises molding an encapsulation material.

[0096] In one example of a method of electromagnetically shielding an electronic device package, the encapsulation material comprises an epoxy.

20 **[0097]** In one example of a method of electromagnetically shielding an electronic device package, the electronic component comprises a first electronic component and a second electronic component associated with respective first and second portions of the substrate, method further comprising separating the first and second portions of the substrate to form first and second electronic device packages.

25 **[0098]** In one example of a method of electromagnetically shielding an electronic device package, separating the first and second portions of the substrate comprises cutting the substrate.

[0099] In one example of a method of electromagnetically shielding an electronic device package, a side portion of the electrically conductive layer is integrally formed with a top portion of the electrically conductive layer.

30 **[00100]** In one example of a method of electromagnetically shielding an

electronic device package, a side portion of the electrically conductive layer is oriented at a non-perpendicular angle relative to a top surface of the substrate.

[00101] In one example there is provided, an electronic device package comprising: a substrate having a conductor pad; an electronic component
5 coupled to the substrate; a conformal insulating layer on the electronic component and the substrate, wherein the conformal insulating layer conforms to the electronic component; and an electrically conductive electromagnetic interference (EMI) layer on the insulating layer and in contact with the conductor pad.

10 **[00102]** In one example of an electronic device package, the electronic component comprises a first electronic component and a second electronic component.

[00103] In one example of an electronic device package, the conformal insulating layer conforms individually to at least one of the first electronic component or
15 the second electronic component.

[00104] In one example of an electronic device package, the first electronic component and the second electronic component form a group of electronic components and the conformal insulating layer conforms to the group of electronic components.

20 **[00105]** In one example of an electronic device package, a plurality of conductive layer portions is disposed between the first and second electronic components.

[00106] In one example of an electronic device package, the electrically conductive layer is formed about the first and second electronic components
25 individually.

[00107] In one example of an electronic device package, the electronic device package further comprises an encapsulation layer on the electrically conductive layer.

[00108] In one example of an electronic device package, the electronic component comprises a first electronic component and a second electronic component,
30 wherein at least a portion of the encapsulation layer is disposed between the first electronic component and the second electronic component.

[00109] In one example of an electronic device package, a portion of the encapsulation layer is in contact with the substrate.

[00110] In one example of an electronic device package, the encapsulation layer comprises an epoxy.

5 **[00111]** In one example of an electronic device package, a side portion of the electrically conductive layer is integrally formed with a top portion of the electrically conductive layer.

[00112] In one example of an electronic device package, a side portion of the electrically conductive layer is oriented at a non-perpendicular angle relative to a top
10 surface of the substrate.

[00113] In one example there is provided, a computing system comprising a motherboard and an electronic device package as recited herein coupled thereto.

[00114] In one example of a computing system, the computing system
15 comprises a desktop computer, a laptop computer, a tablet computer, a smartphone, a server, or a combination thereof.

[00115] In one example of a computing system, the computing system further comprises a processor, a memory device, a heat sink, a radio, a slot, a port, or a combination thereof operably coupled to the motherboard.

20 **[00116]** Circuitry used in electronic components or devices (e.g. a die) of an electronic device package can include hardware, firmware, program code, executable code, computer instructions, and/or software. Electronic components and devices can include a non-transitory computer readable storage medium which can be a computer readable storage medium that does
25 not include signal. In the case of program code execution on programmable computers, the computing devices recited herein may include a processor, a storage medium readable by the processor (including volatile and non-volatile memory and/or storage elements), at least one input device, and at least one output device. Volatile and non-volatile memory and/or storage elements may
30 be a RAM, EPROM, flash drive, optical drive, magnetic hard drive, solid state drive, or other medium for storing electronic data. Node and wireless devices

may also include a transceiver module, a counter module, a processing module, and/or a clock module or timer module. One or more programs that may implement or utilize any techniques described herein may use an application programming interface (API), reusable controls, and the like. Such programs
5 may be implemented in a high level procedural or object oriented programming language to communicate with a computer system. However, the program(s) may be implemented in assembly or machine language, if desired. In any case, the language may be a compiled or interpreted language, and combined with hardware implementations.

10 **[00117]** Furthermore, the described features, structures, or characteristics may be combined in any suitable manner in one or more embodiments. In this description, numerous specific details are provided, such as examples of layouts, distances, network examples, etc. One skilled in the relevant art will recognize, however, that many variations are possible without one or more of
15 the specific details, or with other methods, components, layouts, measurements, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail but are considered well within the scope of the disclosure.

[00118] While the forgoing examples are illustrative of the specific embodiments
20 in one or more particular applications, it will be apparent to those of ordinary skill in the art that numerous modifications in form, usage and details of implementation can be made without departing from the principles and concepts articulated herein. Accordingly, no limitation is intended thereby.

Claims

What is claimed is:

1. A method of making an electronic device package, comprising:
5 providing a substrate having a conductor pad and an electronic component;
forming a conformal insulating layer on the substrate and electronic component, wherein the conformal insulating layer conforms to the electronic component;
10 exposing the conductor pad; and
forming an electrically conductive electromagnetic interference (EMI) layer on the insulating layer and in contact with the conductor pad.
2. The method of claim 1, wherein exposing the conductor pad comprises
15 forming an opening through the conformal insulating layer to the conductor pad, and wherein the electrically conductive layer extends into the opening in contact with the conductor pad.
3. The method of claim 2, wherein forming an opening through the
20 conformal insulating layer comprises ablating the conformal insulating layer with a laser.
4. The method of claim 1, wherein exposing the conductor pad comprises
masking the conductor pad such that the conformal insulating layer is prevented
25 from contacting at least a portion of the conductor pad.
5. The method of claim 3, wherein masking the conductor pad comprises
covering the conductor pad with a mold chase, and wherein forming the
conformal insulating layer comprises molding an insulating material.
30
6. The method of claim 1, wherein the electronic component comprises a first electronic component and a second electronic component.

7. The method of claim 6, wherein the conformal insulating layer conforms individually to at least one of the first electronic component and the second electronic component.

5

8. The method of claim 6, wherein the first electronic component and the second electronic component form a group of electronic components, and the conformal insulating layer conforms to the group of electronic components.

10 9. The method of claim 6, wherein a plurality of conductive layer portions is disposed between the first and second electronic components.

10. The method of claim 9, wherein the electrically conductive layer is formed about the first and second electronic components individually.

15

11. The method of claim 1, wherein forming a conformal insulating layer comprises depositing an insulating material.

12. The method of claim 11, wherein depositing the insulating material
20 comprises atomizing the insulating material.

13. The method of claim 1, wherein forming a conformal insulating layer comprises molding an insulating material.

25 14. The method of claim 1, wherein forming the electrically conductive layer comprises depositing an electrically conductive material.

15. The method of claim 14, wherein depositing the electrically conductive material comprises at least one of atomizing, printing, sputtering, and plating the
30 electrically conductive material.

16. The method of claim 1, wherein forming the electrically conductive layer comprises molding an electrically conductive material.
17. The method of claim 1, further comprising forming an encapsulation layer
5 on the electrically conductive layer.
18. The method of claim 17, wherein the electronic component comprises a first electronic component and a second electronic component, and wherein at least a portion of the encapsulation layer is disposed between the first electronic
10 component and the second electronic component.
19. The method of claim 17, wherein a portion of the encapsulation layer is in contact with the substrate.
- 15 20. The method of claim 17, wherein forming an encapsulation layer comprises molding an encapsulation material.
21. The method of claim 20, wherein the encapsulation material comprises an epoxy.
20
22. The method of claim 1, wherein the electronic component comprises a first electronic component and a second electronic component associated with respective first and second portions of the substrate, and further comprising separating the first and second portions of the substrate to form first and second
25 electronic device packages.
23. The method of claim 22, wherein separating the first and second portions of the substrate comprises cutting the substrate.
- 30 24. The method of claim 1, wherein a side portion of the electrically conductive layer is integrally formed with a top portion of the electrically conductive layer.

25. The method of claim 1, wherein a side portion of the electrically conductive layer is oriented at a non-perpendicular angle relative to a top surface of the substrate.

5

26. A method of electromagnetically shielding an electronic device package, comprising:

forming a conformal insulating layer about an electronic component mounted on a substrate, wherein the conformal insulating layer conforms to the electronic component; and
10 forming an electrically conductive layer on the insulating layer and in contact with a conductor pad on the substrate for an electromagnetic shield associated with the substrate.

15 27. The method of claim 26, wherein the conductor pad is covered by the conformal insulating layer, and further comprising forming an opening through the conformal insulating layer to the conductor pad, wherein the electrically conductive layer extends into the opening in contact with the conductor pad.

20 28. The method of claim 27, wherein forming the opening through the conformal insulating layer comprises ablating the conformal insulating layer with a laser.

29. The method of claim 26, further comprising masking the conductor pad such that the conformal insulating layer is prevented from contacting at least a portion of the conductor pad.
25

30. The method of claim 29, wherein masking the conductor pad comprises covering the conductor pad with a mold chase, and wherein forming the conformal insulating layer comprises molding an insulating material.
30

31. The method of claim 26, wherein the electronic component comprises a first electronic component and a second electronic component.

32. The method of claim 31, wherein the conformal insulating layer conforms individually to at least one of the first electronic component and the second electronic component.

33. The method of claim 31, wherein the first electronic component and the second electronic component form a group of electronic components, and the conformal insulating layer conforms to the group of electronic components.

34. The method of claim 31, wherein a plurality of conductive layer portions is disposed between the first and second electronic components.

35. The method of claim 34, wherein the electrically conductive layer is formed about the first and second electronic components individually.

36. The method of claim 26, wherein forming the conformal insulating layer comprises depositing an insulating material.

37. The method of claim 36, wherein depositing the insulating material comprises atomizing the insulating material.

38. The method of claim 26, wherein forming the conformal insulating layer comprises molding an insulating material.

39. The method of claim 26, wherein forming the electrically conductive layer comprises depositing an electrically conductive material.

40. The method of claim 39, wherein depositing the electrically conductive material comprises at least one of atomizing, printing, sputtering, and plating the electrically conductive material.

41. The method of claim 26, wherein forming the electrically conductive layer comprises molding an electrically conductive material.

5 42. The method of claim 26, further comprising forming an encapsulation layer on the electrically conductive layer.

43. The method of claim 42, wherein the electronic component comprises a first electronic component and a second electronic component, and wherein at
10 least a portion of the encapsulation layer is disposed between the first electronic component and the second electronic component.

44. The method of claim 42, wherein a portion of the encapsulation layer is in contact with the substrate.

15

45. The method of claim 42, wherein forming the encapsulation layer comprises molding an encapsulation material.

46. The method of claim 45, wherein the encapsulation material comprises
20 an epoxy.

47. The method of claim 26, wherein the electronic component comprises a first electronic component and a second electronic component associated with respective first and second portions of the substrate, and further comprising
25 separating the first and second portions of the substrate to form first and second electronic device packages.

48. The method of claim 47, wherein separating the first and second portions of the substrate comprises cutting the substrate.

30

49. The method of claim 26, wherein a side portion of the electrically conductive layer is integrally formed with a top portion of the electrically conductive layer.

5 50. The method of claim 26, wherein a side portion of the electrically conductive layer is oriented at a non-perpendicular angle relative to a top surface of the substrate.

51. An electronic device package, comprising:
10 a substrate having a conductor pad;
an electronic component coupled to the substrate;
a conformal insulating layer on the electronic component and the substrate, wherein the conformal insulating layer conforms to the electronic component; and
15 an electrically conductive electromagnetic interference (EMI) layer on the insulating layer and in contact with the conductor pad.

52. The electronic device package of claim 51, wherein the electronic component comprises a first electronic component and a second electronic
20 component.

53. The electronic device package of claim 52, wherein the conformal insulating layer conforms individually to at least one of the first electronic component or the second electronic component.
25

54. The electronic device package of claim 52, wherein the first electronic component and the second electronic component form a group of electronic components and the conformal insulating layer conforms to the group of electronic components.
30

55. The electronic device package of claim 52, wherein a plurality of conductive layer portions is disposed between the first and second electronic components.

5 56. The electronic device package of claim 55, wherein the electrically conductive layer is formed about the first and second electronic components individually.

57. The electronic device package of claim 51, further comprising an
10 encapsulation layer on the electrically conductive layer.

58. The electronic device package of claim 57, wherein the electronic component comprises a first electronic component and a second electronic component, and wherein at least a portion of the encapsulation layer is
15 disposed between the first electronic component and the second electronic component.

59. The electronic device package of claim 57, wherein a portion of the encapsulation layer is in contact with the substrate.
20

60. The electronic device package of claim 59, wherein the encapsulation layer comprises an epoxy.

61. The electronic device package of claim 51, wherein a side portion of the
25 electrically conductive layer is integrally formed with a top portion of the electrically conductive layer.

62. The electronic device package of claim 51, wherein a side portion of the electrically conductive layer is oriented at a non-perpendicular angle relative to
30 a top surface of the substrate.

63. A computing system, comprising:

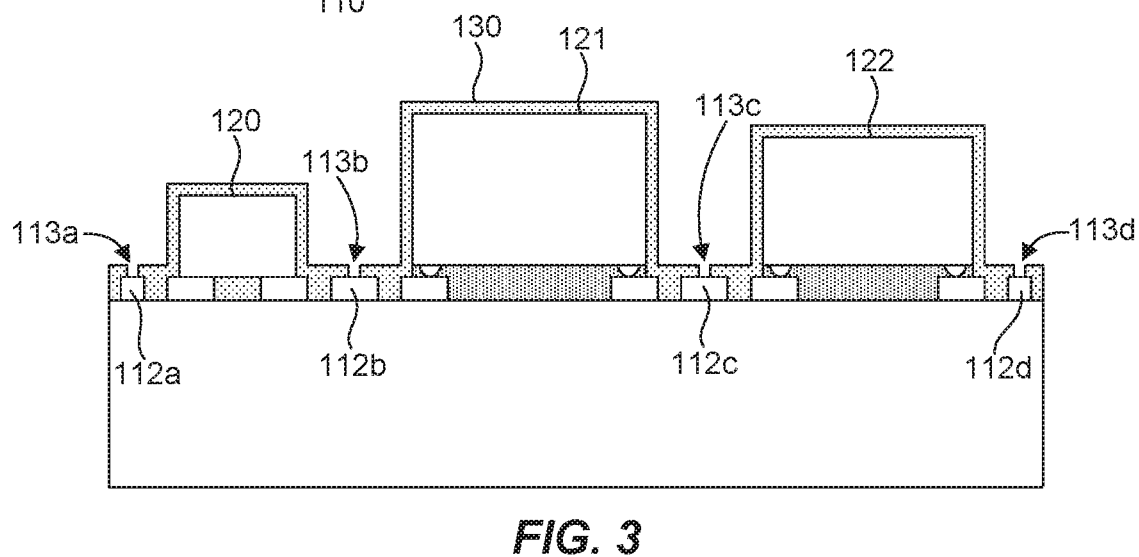
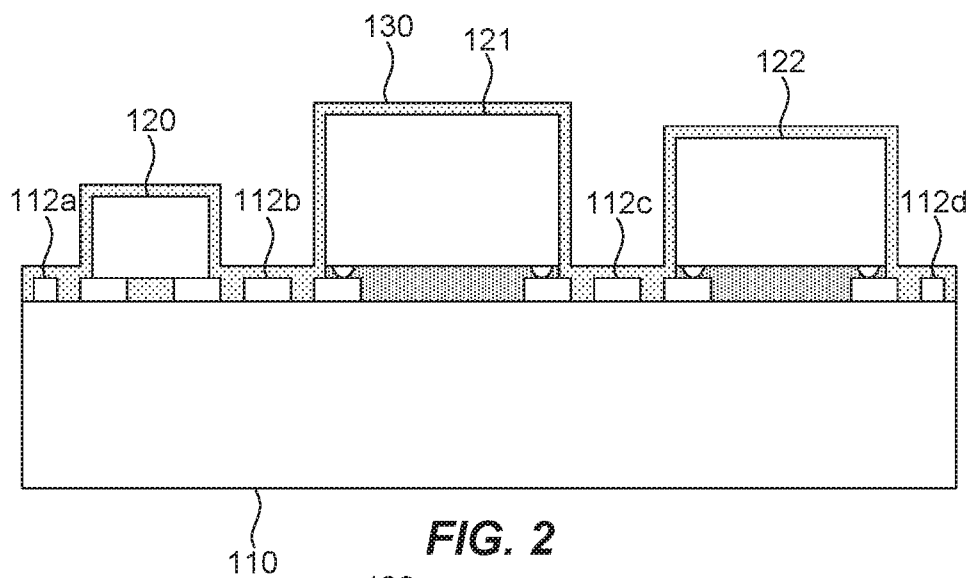
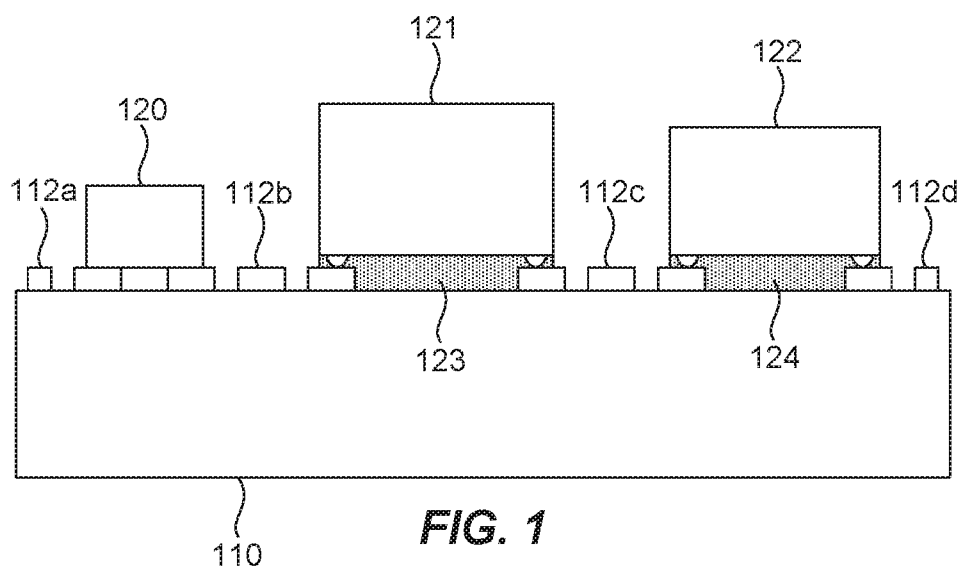
a motherboard; and

an electronic device package as recited in any of claims 51-62 coupled thereto.

64. The system of claim 63, wherein the computing system comprises a
5 desktop computer, a laptop computer, a tablet computer, a smartphone, a
server, or a combination thereof.

65. The system of claim 63, further comprising a processor, a memory
device, a heat sink, a radio, a slot, a port, or a combination thereof operably
10 coupled to the motherboard.

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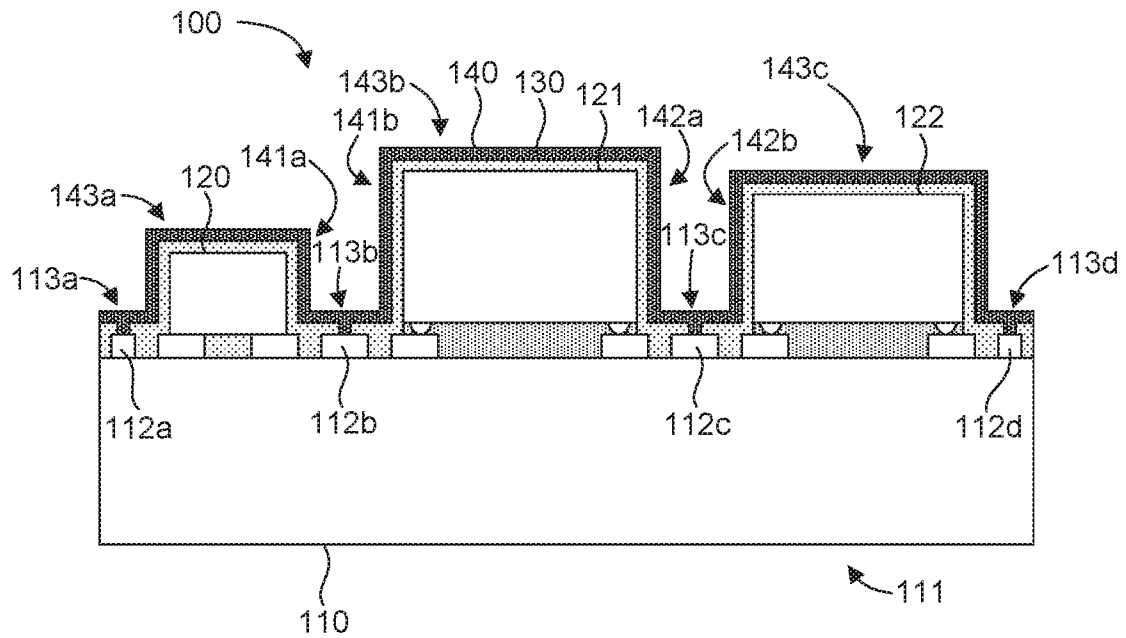


FIG. 4

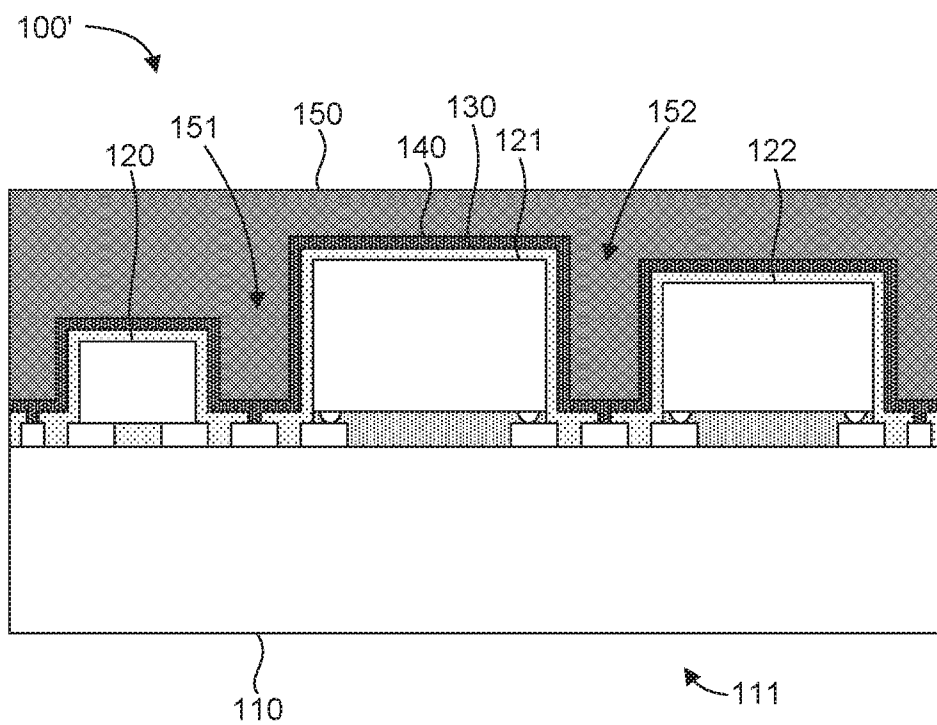


FIG. 5

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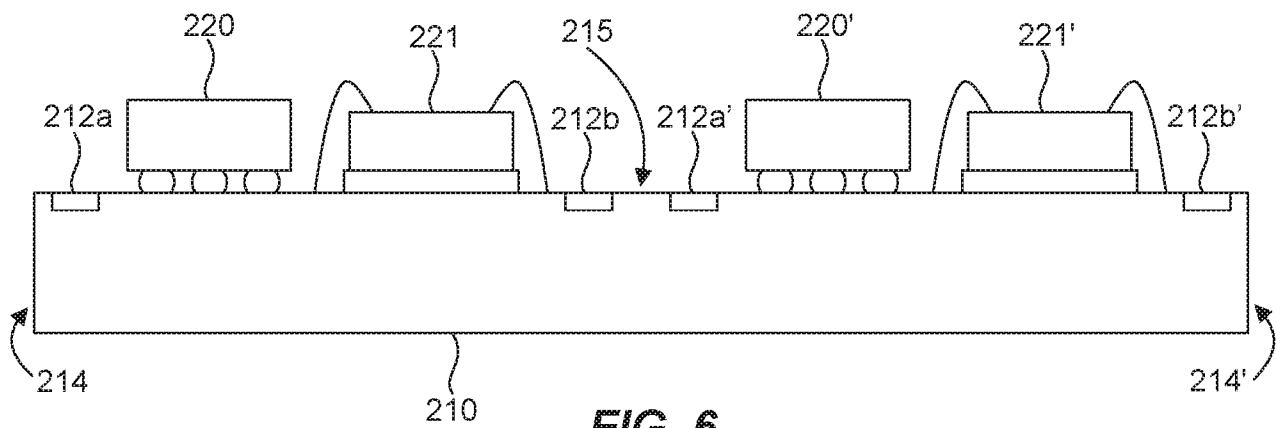


FIG. 6

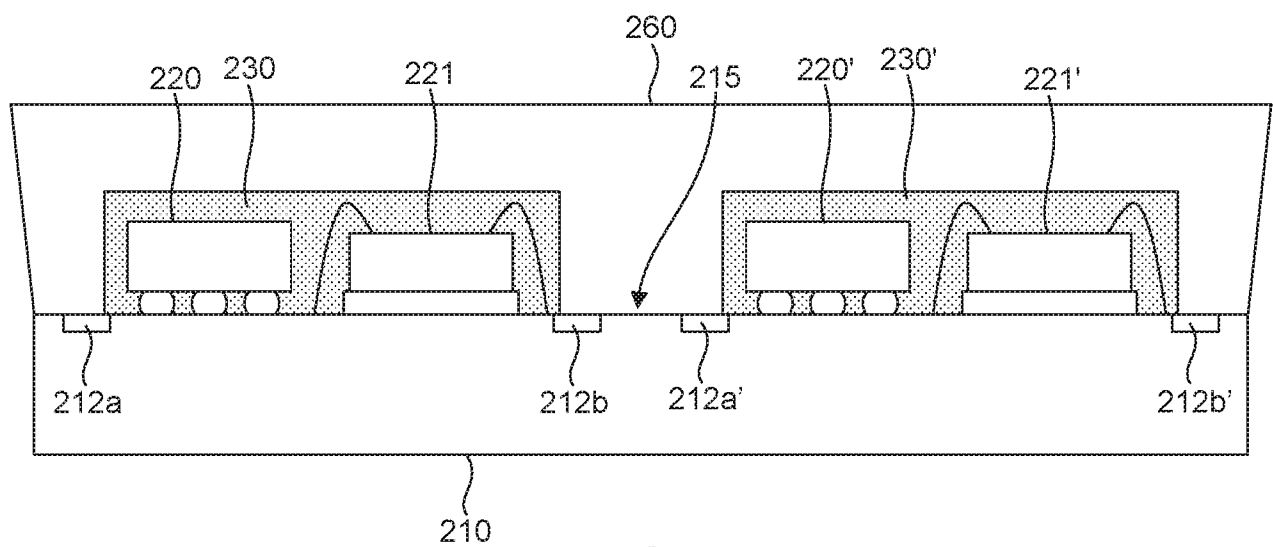


FIG. 7

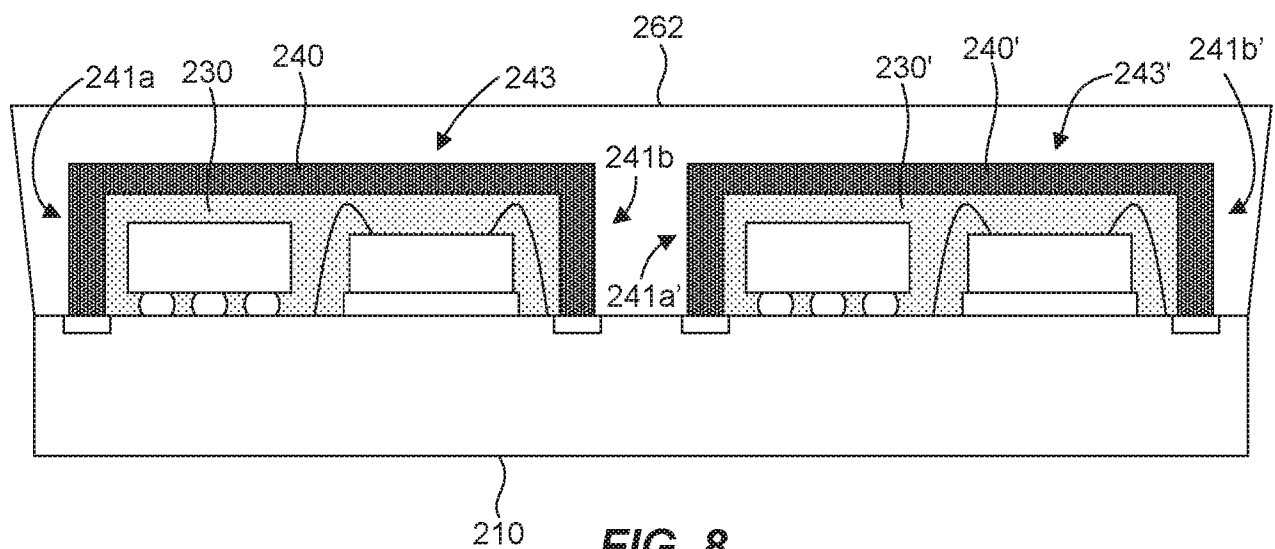
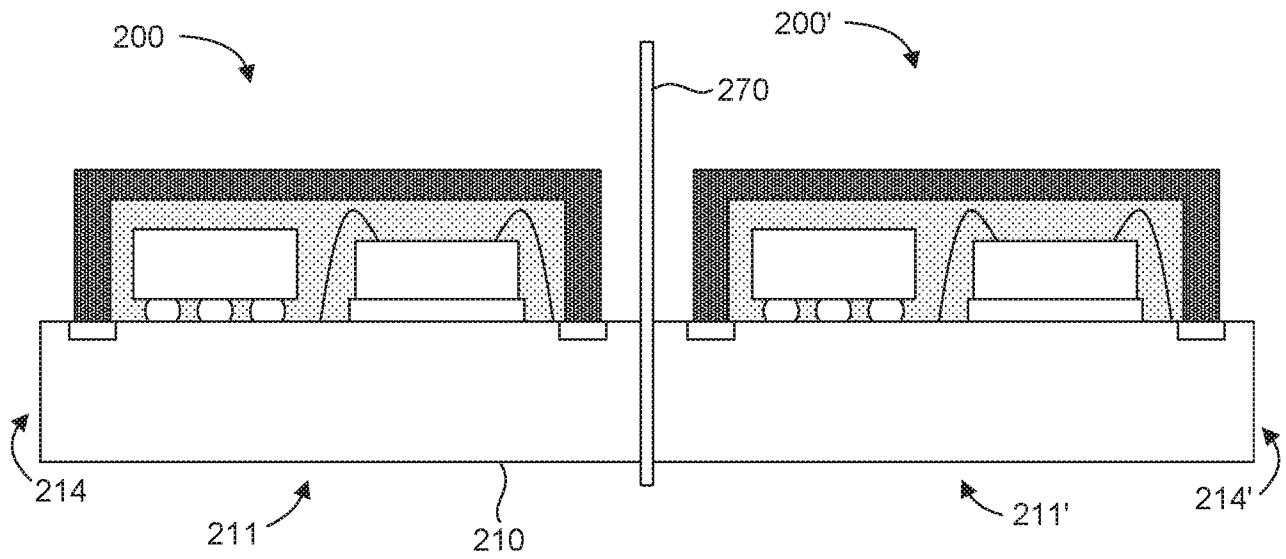
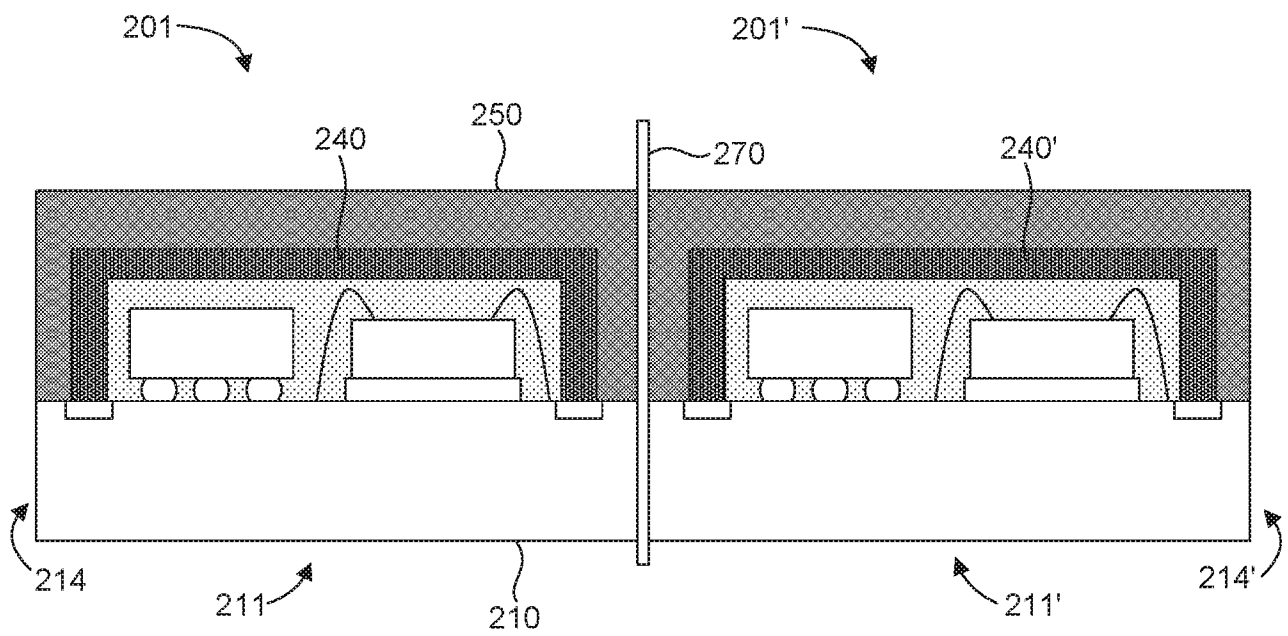
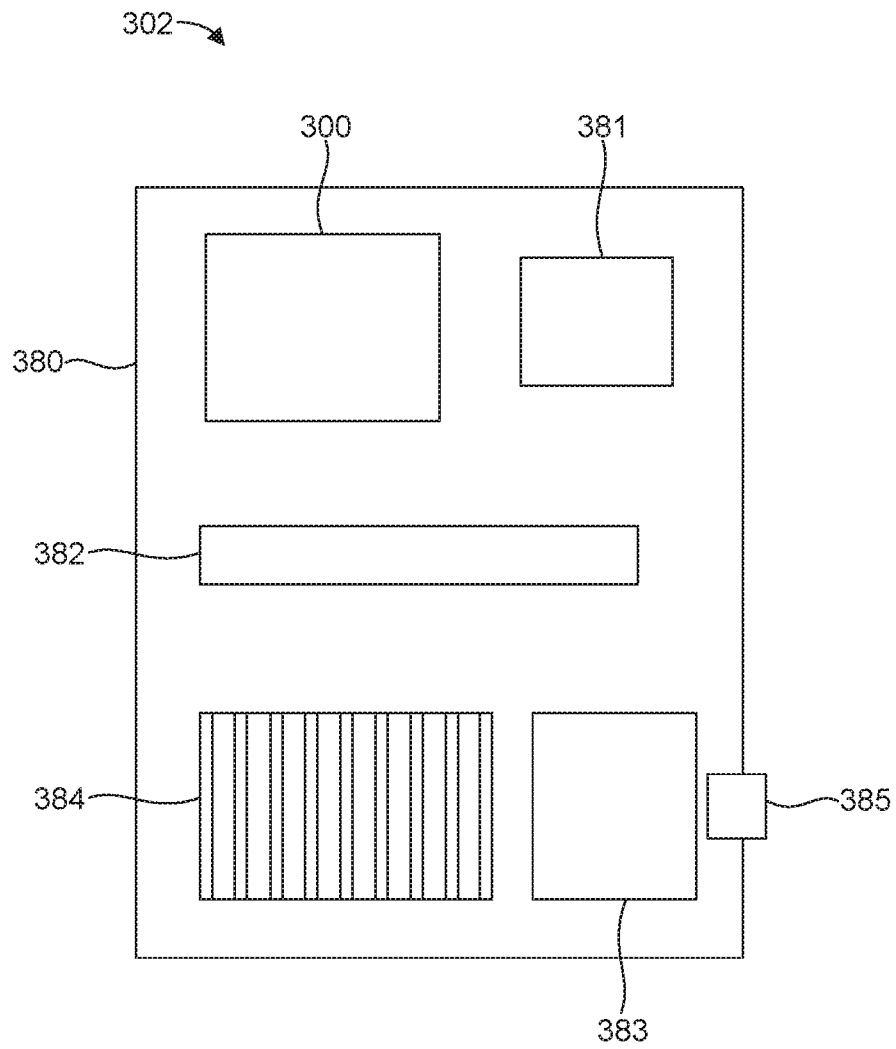


FIG. 8

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**FIG. 9****FIG. 10**

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**FIG. 11**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/063733

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-5, 22, 23, 26-30, 47, 48, 51, 63-65

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/063733

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/552 H01L21/56 H05K9/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2010/069786 A1 (ST MICROELECTRONICS GRENoble [FR]; COFFY ROMAIN [FR]; SAUTY JEAN-FRANC) 24 June 2010 (2010-06-24) page 5, line 6 - page 6, line 17; figure 4 page 1, line 1 - page 5, line 5; figures 1-3 -----	1-4,22, 23, 26-29, 47,48, 51,63-65
X	US 2006/113642 A1 (KAJIKI ATSUNORI [JP] ET AL) 1 June 2006 (2006-06-01) paragraph [0036] - paragraph [0060]; figures 3-14 ----- -/--	1,4,5, 26,29, 30,51

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 February 2017

Date of mailing of the international search report

25/04/2017

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Le Gallo, Thomas

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/063733

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2008/027888 A2 (TEXAS INSTRUMENTS INC [US]; SALZMAN JAMES F [US]) 6 March 2008 (2008-03-06) page 2, line 17 - page 8, line 27; figures 1-6 -----	1,2,4, 26,27, 29,51

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2016/063733

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2010069786 A1	24-06-2010	FR 2940588 A1 US 2012020039 A1 WO 2010069786 A1	25-06-2010 26-01-2012 24-06-2010
US 2006113642 A1	01-06-2006	JP 4494175 B2 JP 2006156798 A KR 20060060550 A TW 200620618 A US 2006113642 A1	30-06-2010 15-06-2006 05-06-2006 16-06-2006 01-06-2006
WO 2008027888 A2	06-03-2008	US 2008055878 A1 WO 2008027888 A2	06-03-2008 06-03-2008

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-5, 22, 23, 26-30, 47, 48, 51, 63-65

directed to methods of exposing the conductor pad, to methods of separating the substrate to form a plurality of electronic device packages and to a computing system including an electronic device package with an EMI layer

1.1. claims: 2-5, 27-30

directed to methods of exposing the conductor pad

1.2. claims: 22, 23, 47, 48

directed to methods of separating the substrate to form a plurality of electronic device packages

1.3. claims: 63-65

directed to a computing system including an electronic device package with an EMI layer

2. claims: 6-10, 31-35, 52-56

directed to an electronic package comprising two electronic components

3. claims: 11-13, 36-38

directed to methods of forming the conformal insulating layer

4. claims: 14-16, 24, 25, 39-41, 49, 50, 61, 62

directed to the electrically conductive material

5. claims: 17-21, 42-46, 57-60

directed to an encapsulation layer on the electrically conductive layer
