



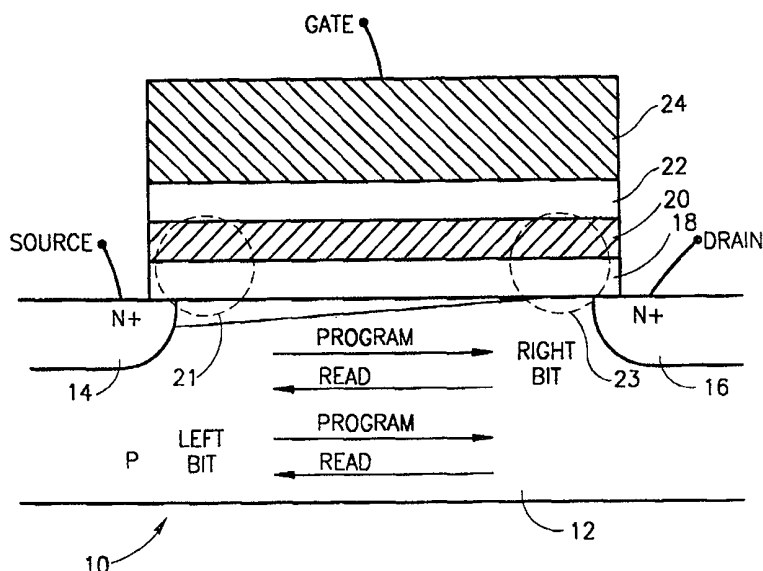
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(21) International Application Number: PCT/IL98/00363 (22) International Filing Date: 2 August 1998 (02.08.98) (30) Priority Data: 08/905,286 1 August 1997 (01.08.97) US (71) Applicant (for all designated States except US): SAIFUN SEMICONDUCTORS LTD. [IL/IL]; Bet HaSofer, Hamelacha Street 65, 42504 Industrial Area South Netanya (IL). (72) Inventor; and (75) Inventor/Applicant (for US only): EITAN, Boaz [IL/IL]; Achi Dakar Street 4, 43259 Ra'anana (IL). (74) Agent: EITAN, PEARL, LATZER & COHEN-ZEDEK; Lumir House, Maskit Street 22, 46733 Herzelia (IL).		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i> (88) Date of publication of the international search report: 8 April 1999 (08.04.99)

(54) Title: TWO BIT EEPROM USING ASYMMETRICAL CHARGE TRAPPING

(57) Abstract

A non-volatile electrically erasable programmable read only memory (EEPROM) capable of storing two bits of information having a nonconducting charge trapping dielectric, such as silicon nitride (20), sandwiched between two silicon dioxide layers (18, 22) acting as electrical insulators is disclosed. The invention includes a method of programming, reading and erasing the two bit EEPROM device. The nonconducting dielectric layer functions as an electrical charge trapping medium. A conducting gate electrode (24) is placed over the upper silicon dioxide layer (22). A left and right bit are stored in physically different areas of the charge trapping layer, near left and right regions of the memory cell, respectively. Each bit of the memory device is programmed in the conventional manner, using hot electron programming, by applying programming voltages to the gate and to either the left or the right region while the other region is grounded.



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INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : HO1L 29/788, 29/792

US CL : 257/317, 324

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/317, 324

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P, L	US 5,768,192 (EITAN) 16 June 1998 (16/06/98), see entire document.	1-68
A,P	US 5,654,568 (NAKAO) 05 August 1997 (05/08/97), see entire document, especially Figure 6E.	1-68



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