COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

DECLARATION IN SUPPORT OF CONVENTION OR NON-CONVENTION APPLICATION FOR A PATENT

Insert title of invention.

In support of the Application made for a patent for an invention entitled: "DEBRIS DETECTOR"

Insert full name(s) and address(es) of declarant(s) being the applicant(s) or person(s) authorized to sign on behalf of an applicant company.

I, Arthur B. PELL
~~We~~ of COULTER ELECTRONICS, INC,
of 590 West 20th Street, Hialeah,
Florida 33010, United States of America.

Cross out whichever of paragraphs 1(a) or 1(b) does not apply

1(a) relates to application made by individual(s)
1(b) relates to application made by company; insert name of applicant company.

do solemnly and sincerely declare as follows :-

~~1. (a) I am the applicant for the patent~~

or (b) I am authorized by

COULTER ELECTRONICS, INC

the applicant..... for the patent to make this declaration on its behalf.

Cross out whichever of paragraphs 2(a) or 2(b) does not apply

2(a) relates to application made by inventor(s)
2(b) relates to application made by company(s) or person(s) who are not inventor(s); insert full name(s) and address(es) of inventor.

~~2. (a) I am/We are the actual inventor..... of the invention~~

or (b) Ermi ROOS of 7400 Miami Lakes Drive, Miami Lakes, Florida 33014; and Wallace H. COULTER of 910 Quail Avenue, Miami Springs, Florida 33166, both of United States of America

are the actual inventors..... of the invention and the facts upon which the applicant.....
is entitled to make the application are as follows :-

State manner in which applicant(s) derive title from inventor(s)

The actual inventors assigned the invention to the said applicant.

Cross out paragraphs 3 and 4 for non-convention applications. For convention applications, insert basic country(s) followed by date(s) and basic applicant(s).

3. The basic application..... as defined by Section 141 of the Act was made
in United States of America on the 3rd October 1986
by Ermi ROOS and Wallace H. COULTER
in ..... on the .....
by .....
in ..... on the .....
by .....

4 The basic application..... referred to in paragraph 3 of this Declaration was/were the first application..... made in a Convention country in respect of the invention the subject of the application.

Insert place and date of signature.

Declared at Hialeah, Florida, U.S.A. this 28th day of April, 1988.

Signature of declarant(s) (no attestation required)

COULTER ELECTRONICS, INC.
by Arthur B. Pell
Arthur B. Pell, Assistant Secretary/Treasurer

Note Initial all alterations.

DAVIES & COLLISON, MELBOURNE and CANBERRA.

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(71) Applicant(s)
COULTER ELECTRONICS, INC.

(72) Inventor(s)
ERMI ROOS; WALLACE H. COULTER

(74) Attorney or Agent
DAVIES & COLLISON, MELBOURNE

(56) Prior Art Documents
US 3259842
US 4326230

(57) Claim

1. A debris detector for a particle detector of the type having a small orifice separating two chambers, with a constant current applied through said orifice, and in which particles and debris suspended in a liquid are passed through said small orifice, whereby each particle or debris passing through said orifice causes a voltage pulse across said orifice and debris lodging in or against said orifice causes a d.c. voltage shift across said orifice, and said particle detector further having sensing means to sense the voltage across said orifice, said sensing means further including capacitance means coupling said sensing means to said orifice, said debris detector being characterized by means for integrating the output of said sensing means; and means for determining if the integrated sensing means output exceeds a certain value Vref after a certain delay time.

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(71) Applicant: COULTER ELECTRONICS, INC. [US/US]; 590 West 20th Street, Hialeah, FL 33010 (US).

(72) Inventors: ROOS, Ermi ; 7400 Miami Lakes Drive, Miami Lakes, FL 33014 (US). COULTER, Wallace, H. ; 910 Quail Avenue, Miami Springs, FL 33166 (US).

(74) Agent: HIBNICK, Gerald, R.; Coulter Electronics, Inc., 590 West 20th Street, Hialeah, FL 33010 (US).

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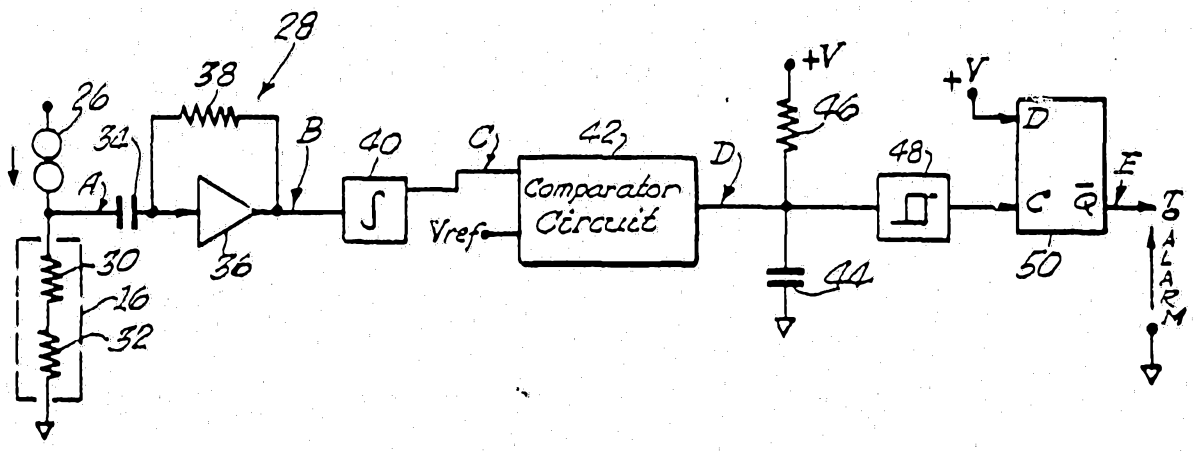

(57) Abstract

In a debris detector for a particle counter (10), a particle (18), or transient debris passing through the sensing orifice (16) causes a voltage pulse occurs (fig. 3A). When debris lodges in or against the orifice (16) of the particle detector (10), a d.c. voltage shift occurs. The voltage at the orifice (16) is capacitively (34) coupled to an amplifier (36) and the output of the amplifier (36) is provided to an integrator (40). The integrated voltage (Fig. 3C) is applied to a comparator (42) to provide an output signal (Fig. 3D) whenever the integrated voltage (Fig. 3C) exceeds a reference voltage (Vref). The comparator (42) output signal (Fig. 3D) is provided to a delay circuit (44, 46) having a delay related to the time required for a particle (18) to pass through the orifice (16). If the comparator (42) signal (Fig. 3D) remains after the delay time, a debris alarm signal (Fig. 3E) is provided.

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This invention relates to a debris detector and more particularly to such a detector for use in a particle counter such as a blood cell counter, for detecting and providing an alarm signal whenever debris becomes lodged against or in the orifice through which the particles pass.

Blood cell counters of the general type now known as the COULTER COUNTER (R) analyzer were first described in the U.S. Patent 2,656,508 which was granted October 20, 1953 in the name of Wallace H. Coulter. According to the principle taught by Coulter in the aforementioned patent, a fluid containing blood cells suspended therein, such as diluted whole blood, is passed through a small opening, or orifice, from one fluid containing chamber to another fluid containing chamber. An electrode positioned in each of the chambers is coupled to a current source, so that a constant current flows through the orifice from one chamber to the other. As blood cells pass through the orifice, the electrical resistance within the orifice increases with a corresponding increase in the voltage across the orifice due to the constant current. Sensing means coupled to the two electrodes sense the voltage pulse increase due to the passage of a particle through the orifice, thereby detecting such particle. By utilizing appropriate counter means and volume control means, the number of particles, such as red blood cells, within a defined volume, can be determined. The change in resistance in the orifice due to the presence of a particle is approximately proportional to the volume of the particle. Thus, the COULTER COUNTER analyzer is capable of determining the mean particle volume of, as well as the number of particles in, a sample being measured.

One of the problems which always has been present in any blood cell counter of the type described above is that debris, such as blood clots or other contaminants placed in the specimen under test from the ambient, can lodge against or within the orifice, thereby preventing the free and

natural flow of the cells through the orifice. Other debris within the specimen may be so small that it passes through the orifice, causing no permanent problem. Such small debris is referred to herein as transient debris and sufficient care can be taken so that the number of transient debris particles passing through the orifice is negligible compared to desired particles. Thus, the transient debris, if counted as particles, causes negligible effect on the final result.

Many attempts have been made in the past to provide a detector to indicate that the orifice of the COULTER (R) type particle counter has become clogged by debris lodged in or against the orifice. For example, in U.S. Patent 3,259,842 in the name of Wallace H. Coulter et. al., a debris detector is described which measures the height and width of the pulses detected by the COULTER particle detector apparatus. This debris detector makes use of the fact that debris generally has a resistance greater than the resistance of a normal blood cell. Further, the duration of the pulse detected for a debris particle or lodged debris generally exceeds the duration of a normal cell. This is because a cell passes through the orifice in less time than debris, because the cell is smaller.

A second type debris detector is disclosed in U.S. Patent 3,259,891, in the name of Wallace H. Coulter et. al., and utilizes similar larger resistance and pulse width for debris versus predictably known lower resistance and pulse time for normal particles passing through the orifice. In the debris alarm detector of U.S. Patent 3,259,891 the magnitude of the voltage sensed is first detected and, for pulses exceeding a certain threshold voltage amplitude, the duration of the pulse is also measured. If the duration exceeds a certain value, then the debris alarm is sounded. The problem with this type of detection is that transient debris and many large particles are detected as debris, merely because of their large size and long duration their pulse.

Several problems exist with the technique in the debris alarm described in U.S. Patent 3,259,891 First, the debris alarm of the prior art is unable to differentiate easily between debris which lodges in or against the orifice and large cells or transient debris which passes through the orifice causing negligible effect on the ultimate result. Further, in the prior art device the waveform shape becomes critical in detecting the debris. This is particularly true of the rise time of the pulse which results when debris becomes lodged in or against the orifice. In order to compensate for the relatively slow rise time of the leading edge of the debris pulse, the prior art device used a lower threshold voltage setting than was optimally desirable. This, in turn, resulted in many false alarms of debris being detected, particularly when the debris was transient debris which passed through the orifice. Further, the prior art device had difficulty in differentiating in many instances between large pulses due to large cells or debris, again leading to many false negatives alarms.

Attempts to overcome many of the limitations of the prior art debris detectors described in the aforementioned patent have been made. For example, in U.S. Patent 4,412,175 in the name of Franklin D. Maynarez, bad pulses are detected based on the techniques of the aforementioned prior art patents to W. H. Coulter, et. al. and ratioing techniques are utilized to determine when the number of bad pulses exceeds certain predetermined unacceptable levels. By utilizing the improvements such as in the Maynarez patent, some of the shortcomings of the prior art detectors can be overcome. Another example of improvements in debris alarms of the prior art is shown in U.S. Patent 4,450,435 in the name of Bobby D. James. In the James Patent, sophisticated comparator means are utilized for comparing the number of good pulses and bad pulses and for alarming when the number of bad pulses exceeds certain predetermined

relative per cents. Even with these techniques, false negatives are obtained when the sample under test contains many large cells.

Rather than relying on ratioing and group comparison techniques of the prior art, it would be preferable to be able to utilize the debris alarm circuitry itself directly to provide an indication when debris becomes lodged in the particle counter orifice. This will result in an alarm when troublesome debris is detected, rather than requiring a wait until after the proper ratios or comparisons have been made. Such a wait causes a substantial number of improper particles having been counted. Further, by detecting the debris when it initially becomes lodged, samples may be saved and evasive action taken immediately.

In accordance with one aspect of this invention, there is provided a debris detector for a particle detector of the type having a small orifice separating two chambers, with a constant current applied through said orifice, and in which particles and debris suspended in a liquid are passed through said small orifice, whereby each particle or debris passing through said orifice causes a voltage pulse across said orifice and debris lodging in or against said orifice causes a d.c. voltage shift across said orifice, and said particle detector further having sensing means to sense the voltage across said orifice, said sensing means further including capacitance means coupling said sensing means to said orifice, said debris detector being characterized by means for integrating the output of said sensing means; and means for determining if the integrated sensing means output exceeds a certain value Vref after a certain delay time.

By way of example, illustrative embodiments of the invention now will be described with reference to the accompanying drawings, in which:

Figure 1 shows a general schematic representation of the prior art COULTER type particle sensing apparatus;

Figure 2 shows a block diagram of the subject invention used to detect debris lodged in or against the orifice of the apparatus shown in Figure 1;

Figure 3 shows diagrams useful in understanding the general operation of the invention subject matter shown in Figure 2;

Figure 4 shows logic circuitry which has been added to the block diagram shown in Figure 2 to inhibit its operability during certain special periods;

Figure 5 shows a more detailed circuit diagram of the block diagram shown in Figure 4;

Figure 6 shows yet a more detailed diagram of a certain portion of the circuit shown in Figure 5 relating to the operation of the delay function; and

Figure 7 is a series of waveforms useful in understanding the operation of the circuit shown in Figure 6.

Referring now to Figure 1, the traditional schematic presentation of a COULTER type particle sensing apparatus 10, typical of the prior art, is shown. The apparatus 10 includes a first fluid holding container 12 and a second fluid holding container 14. A small aperture, orifice or opening 16 is fabricated in container 14 to allow particles 18, suspended in a fluid 20, to pass from the container 12 into the container 14. A pair of electrodes 22 and 24 are respectably positioned within the fluid 20 of each of containers 12 and 14; and a current source 26 is coupled between the electrodes 22 and 24, so that a constant current flows from electrode 22 to electrode 24 through orifice 16. In addition, sensing, sizing and counting circuit 28, well known in the prior art, is connected to each of electrodes 22 and 24 to provide the detection, size and count of the number of particles 18 passing through orifice 16. This count is generally taken during the controlled provision of a predetermined amount of fluid 20 through orifice 16.

The apparatus of Figure 1 works extremely well, except when a particle of debris becomes lodged in or against orifice 16. This either causes the particles 18 to cease or slow down in passing through orifice 16, at least for the period of time that the debris is lodged in or against orifice 16, or it causes particles to be improperly sized because of constriction in the orifice volume. It is important to be able to detect this occurrence of debris lodging in or against orifice 16 in order to stop the count and provide an alarm notifying the operator of apparatus 10 that the count or particle volume then occurring is an error and that corrective action must be taken. However, care must be taken to be sure that the debris detected is lodged debris, rather than large cells or transient debris which passes through orifice 16 and thereby does not prevent a significant number of particles 18 from passing through orifice 16. The only harm which results from a piece of transient debris passing through orifice 16 is that the particle count may be increased by one, and/or that the mean particle volume is changed slightly. However, the amount of error from other portions of apparatus 10 is greater than the error which will result in the total count or mean particle volume if transient debris is sensed as if particles. This, of course, assumes that normal care is used in preparing the solution placed in container 12, which contains the particles 18 to be detected, so that debris is minimized.

Referring now to Figure 2, orifice 16 is shown schematically as a pair of series coupled resistors 30 and 32. Resistor 30 is the normal resistance in orifice 16 due to the electrolyte fluid 20 normally within aperture 16. Resistor 32 represents a transient resistance which comes and goes as a particle 18 passes through aperture 16. With current source 26 coupled in series with resistors 30 and 32, the voltage across resistors 30 and 32 increases due to

the presence of a particle 18 being within aperture 16 which causes a corresponding increase in resistance of resistor 32.

The junction between current source 26 and resistor 30 is coupled through a coupling capacitor 34 to the input of an operational amplifier 36. Amplifier 36, together with feedback resistor 38 and other resistors (not shown) normally associated with an operational amplifier to cause significant gain, represent the first stage of the preamplifier of the sensing portion of circuit 28 shown in Figure 1. It should be understood that the additional stages of the preamplifier, as well as the post amplifier, generally are included as part of circuit 28, but are not shown in Figure 2 because they form no part of the subject invention.

The output from amplifier 36, the first stage preamplifier, is applied as an input to an integrator circuit 40. Integrator circuit 40 provides a voltage at its output which is the mathematical integral of the voltage applied to its input. Integrator circuit 40 can include an operational amplifier with a feedback capacitor and is shown in more detail hereafter in Figure 5. The output from integrator circuit 40 is provided as the data input to a comparator circuit 42. A reference voltage, Vref, also is provided to a second input of comparator circuit 42. The output from comparator circuit 42 is normally a positive voltage whenever the voltage provided at the data input from integrator 40 exceeds the value of the reference voltage Vref. However, the output of comparator 42 is coupled to the junction of one end of each of a capacitor 44 and a resistor 46; the other end of resistor 46 is coupled to a source of positive voltage +V and the other end of capacitor 44 is coupled to ground. When the output of comparator circuit 42 is low, due to the data signal from integrator 40 being less than Vref, the output transistor (not shown) included within comparator 42 is conductive to ground and capacitor 44 discharges

therethrough. However, when the voltage provided from integrator 40 to comparator 42 exceeds Vref, capacitor 44 begins charging, with a time constant determined by the values of resistor 46 and capacitor 44.

The junction of resistor 46 and capacitor 44 is coupled as one input to a threshold circuit 48, such as a Schmitt trigger circuit. When the value of the voltage stored by capacitor 44 exceeds threshold value of threshold circuit 48, which may be 1.6 volts for example, the output of circuit 48 changes states. The output from threshold circuit 48 is provided to the clock input (C) of a flip-flop circuit 50 and the leading edge of the threshold circuit 48 pulse forces the Q bar output of flip-flop 50 to a low value, that is, to the logic value opposite to the logic value of the signal applied to its data input (D). This results in a positive to negative voltage appearing at the Q bar output of flip-flop 50. This signal is used to trigger a debris detected visual and/or audible alarm (not shown), thereby alerting the operator to take appropriate action.

Referring now to Figure 3, a series of waveforms labeled A-E are shown. Corresponding letters A-E are shown in Figure 2 to indicate which portion of the circuit the waveforms A-E represent. Waveform A is the voltage pulses provided by detecting the change in voltage due to the presence or absence of transient resistor 32 due to the corresponding presence or absence of a particle 18 passing through orifice 16. As can be seen, the first voltage pulse is a relatively low signal and manifests a normal blood cell passing through orifice 16. The second pulse in waveform A represents either a larger blood cell, or transient debris, either of which have a higher resistance that results in a higher voltage. However, because the large cell or transient debris passes through orifice 16, the pulse has only a slightly longer than normal pulse width. The third portion of waveform A represents a piece of debris which has become lodged in or against, and

thereby blocks, orifice 16. This results in a high voltage being sensed for a long duration. In effect, the result is a d.c. voltage shift for the voltage sensed.

Waveform B of Figure 3 shows the output of operational amplifier 36, which as previously mentioned, is the first stage of the preamplifier of circuit 28 shown in Figure 1. Waveform B shows the effects of capacitor 34 being included between aperture 16 and the first stage of the preamplifier. As can be seen, the first pulse in Waveform B increases at a slower rate than the corresponding A waveform pulse, because capacitor 34 becomes charged and subtracts its voltage from the A waveform pulse. It is well known that the voltage across a capacitor cannot instantaneously change. Thus, when the trailing edge of the first pulse occurs, a negative undershoot 52 in the voltage provided from the output of amplifier 36 results. The amplitude of this negative undershoot is approximately equal to the amount the rising edge of the pulse has been depressed by the charging of capacitor 34. The second pulse in waveform B is substantially identical to the shape of the first pulse of waveform B, except that its magnitude is larger, due to the larger pulse being detected. However, again, an undershoot 52 is present in the second pulse in waveform B.

For any value of capacitor 34, the area above undershoot 52 is equal to the area below the positive going portion 53 of the first and second pulses in Waveform B. Thus, the average voltage passing through amplifier 36 is zero for the first and second pulses shown in Waveform B.

It should be recalled from the description of waveform A that the third pulse rises to a steady d.c. voltage and remains at that d.c. voltage value due to the debris becoming lodged in or against orifice 16. The third pulse of waveform B reflects this constant voltage by the absence of any undershoot 52. The value of the output of operational amplifier 36 for the third pulse thus rises to

a peak value and thereafter decays from the peak value to zero. Thus, the average value of the voltage through amplifier 36 for the third pulse is no longer zero.

Referring now to waveform C of Figure 3, the first and second pulses are similarly shaped and different only in amplitude. Both rise and fall back to zero due to the integration of the positive portion 53 and undershoot portion 52 of the first and second pulses of waveform B. However, the third pulse of waveform C increases to a value at which it generally remains. Again, this is because the integration of the third pulse in waveform B does not include any undershoot to bring the integral thereof back to zero.

Waveform C, as indicated in Figure 2, is applied to the input of comparator circuit 42, which also has the voltage Vref applied thereto. Voltage Vref is shown as a dashed line in waveform C and is above the first pulse and through the second pulse and third pulse of waveform C.

Referring now to waveform D of Figure 3, it is seen that since the first pulse of waveform C was below the Vref threshold, there is no corresponding first pulse in waveform D. The pulse of waveform D corresponding to the second pulse of waveform C, however, exists for the period of time that the second pulse of waveform C was above the threshold Vref value. However, this is a relatively short time due to the short duration of the second pulse detected at Waveform A. Since the waveform D pulses represent the voltage stored by capacitor 44, the waveform D pulses only begin increasing when the waveform C pulses exceed the comparator Vref voltage and capacitor 44 is being charged. Thereafter, capacitor 44 discharges through the grounded output of comparator circuit 42. Thus, there is no pulse in waveform D corresponding to the first pulse in waveform C and the pulse of waveform D corresponding to the second pulse of waveform C never exceeds the threshold voltage Vth. The third pulse of waveform C, however, remains above the Vref value, so capacitor 44 continues to be charged

until it exceeds the threshold voltage Vth of threshold circuit 48. This is shown by the dashed lines labeled Vth in waveform D.

Referring now to waveform E of Figure 3, as soon as the last pulse of waveform D exceeds the Vth value, an output appears from circuit 48, triggering flip-flop 50 and causing the voltage E to change state. This will be interpreted by circuitry (not shown) to cause an audible and/or visual alarm to occur, manifesting to the operator of apparatus 10 that a debris blockage has been detected.

Referring now to Figure 4, an enhanced embodiment of the subject invention is shown. The circuit in Figure 4 includes means to inhibit the operation during the critical times of the start-up of apparatus 10, or the detection of the filling of a chamber containing fluid 20. This chamber (not shown) can be one used for determining hemoglobin in a blood sample. Hemoglobin is measured by techniques independent of the COULTER principle. When the chamber used for measuring hemoglobin has filled, the fluid 20, mixed with a chemically treated blood sample, strikes an electrode that is positioned at the location the liquid would reach when the chamber is filled. A second electrode is at the bottom of the chamber. When the liquid touches the level sensing electrode, circuitry (not shown) detects the liquid level by sensing electrical continuity between the sensing electrode and the bottom electrode. This continuity detection is accomplished by current flow between the electrodes. This current flow causes interference at the orifice 16 that is similar to debris being lodged against or in the orifice. Both the start up and filling of the chamber can cause transient voltages to be provided at the input side of capacitor 34, and hence to amplifier 36, which may appear as permanent blockages due to debris, but in fact are due to nonpermanent transient voltages resulting from either the application of power to

apparatus 10 or the flow of electrical current resulting from detection of the filling of a chamber containing fluid 20.

In Figure 4, like components, with respect to Figure 2, have been given like numerical designations and the operation thereof is similar to that described with respect to Figure 2. Of the components shown in Figure 2, only integrator 40 is shown in more detail as including a feedback capacitor 54, an operational amplifier 55 and an input resistor 56 . This, as is well known in the art, is a conventional integrator circuit.

The additional circuitry added in Figure 4 includes a level detector 57 and a start detector 58. Both are well known in the art and are shown only in block form in Figure 4. Level detector 57 provides a voltage whenever the level of the fluid 20 in the hemoglobin chamber reaches a prescribed level. When the fluid reaches the prescribed level in that chamber (not shown), the level is detected by current flow caused by continuity produced when the fluid reaches the level sensing electrode. This current could be detected as a d.c. level shift not always indistinguishable from a similar d.c. level shift as a result of blocking debris. Start detector 58, on the other hand, monitors when voltage is first applied to apparatus 10. Such application results in a significant d.c. voltage shift through orifice 16, which again could be detected as lodged debris causing a d.c. voltage shift in orifice 16. The output voltage from level detector 57 is a pulse of approximately 100 milliseconds duration and the output voltage of start detector 58 is a pulse of approximately one second duration which, as will be explained hereafter, inhibits the operation of the detector circuit.

The output of level detector 57 and the output of start detector 58 are both applied as the two inputs to a NAND gate 60. In addition, the outputs of level detector 57 and start detector 58 are applied as the two inputs to a NAND gate 62. The output from NAND gate 60 is provided to the

noninverting input of a driver circuit 64 and the inverting input of a driver circuit 66. The inverting input of driver circuit 64 and the noninverting input of driver circuit 66 are coupled to a source of positive voltage +V. The output of driver circuit 64 is coupled to the gate of a field effect transistor (FET) transistor 68. The channel electrodes of transistor 68 are coupled between operational amplifier 36 and the input to operational amplifier 55 within integrator circuit 40 through the input resistor 56. The output of driver circuit 66 is coupled to the gate electrode of an FET transistor 70, which has one channel electrode coupled to the junction between resistor 56 and the input to operational amplifier 55 and the other channel electrode coupled to the anode of a diode 72, the cathode of which is coupled to ground. In addition, the other channel electrode of FET transistor 70 is coupled to the output of operational amplifier 55 and to the cathode of a diode 74, the anode of which is coupled to ground.

Capacitor 54 is coupled between the input and output of operational amplifier 55, and thus, is coupled in the same manner as the channel electrodes of transistor 70. Whenever either level detector 57 or start detector 58 detects a respective level change or voltage application, a signal is provided through NAND gate 60 and driver circuit 64 to render FET transistor 68 nonconductive and FET transistor 70 conductive. This occurs for the approximately 100 millisecond period following level detector 57, or the one second period following start detector 58 detecting one of the critical conditions. During this period, capacitor 54 is discharged through now conductive FET transistor 70. At the same time, voltage is prevented from being applied to the input of integrator 40 by nonconductive FET transistor 68. After the 100 millisecond or one second duration of the pulses provided by one of detectors 57 and 58, the normal condition of transistor 68 being conductive and transistor 70 being nonconductive is returned and operation proceeds as previously explained.

In addition, the outputs from detectors 57 and 58 are applied through NAND gate 62 to disable a NAND gate 76 from passing any signals provided thereto from threshold circuit 48. Because of the inclusion of NAND gate 76, it is necessary to provide an inverter 78, in order to have the proper polarity to trigger flip-flop 50 by providing a pulse to the clock (C) input thereof.

Referring now to Figure 5, a more detailed schematic diagram of the circuit shown in Figure 4 is shown. Where like components are shown, they have been given like numerical designations with respect to the circuits shown in Figures 4 and 5. Elements 26 through 38 (even numbers only) and FET transistor 68 are connected as previously described with respect to Figure 4. The substrate electrode of transistor 68 is coupled to a source of voltage +V2, which can be 15 volts d.c. The previously mentioned voltage +V can be five volts d.c. The other channel electrode of transistor 68 is coupled through resistor 56 to the inverting input of operational amplifier 55. One channel electrode of transistor 70 is connected to the inverting input of operational amplifier 55 and the other channel electrode of transistor 70 is connected to the output of operational amplifier 55. The substrate electrode of transistor 70 is connected to a source of voltage +V2. Capacitor 54 is coupled between the output and the inverting input of operational amplifier 55. A resistor 82 is coupled in parallel with capacitor 54 and serves to discharge capacitor 54 after a debris alarm has sounded and to prevent the debris alarm from responding to very slowly varying d.c. level shifts at the orifice 16, which are not caused by debris. The anode of diode 72 is connected to the output of operational amplifier 55 and the cathode of diode 72 is connected to ground. The cathode of diode 74 is connected to the output of operational amplifier 55 and the anode of diode 74 is connected to ground. Connected in this manner, diodes 72 and 74 limit the voltage excursion of the output of operational amplifier 55.

The noninverting input of amplifier 55 is coupled to ground. The numbers at the connections of some of the components shown in Figure 5 are pin numbers of the particular components used. A list of the components used is given hereafter. Offset voltage control input, pin 1, of amplifier 55 is coupled through a potentiometer 84 to offset voltage control input, pin 5, of amplifier 55. Potentiometer 84 is used to set the offset voltage of operational amplifier 55. Negative d.c. power supply input, pin 4, of amplifier 55 is coupled through a resistor 86 to -V2 volts, which can be -15 volts, through a capacitor 88 to ground and through a capacitor 90 to positive d.c. power supply input, pin 7. The junction between capacitor 90 and positive d.c. power supply input, pin 7, is coupled through a resistor 92 to voltage V2. Resistors 86 and 92 and capacitors 88 and 90 provide for d.c. power supply bypassing of amplifier 55.

The output from amplifier 55 is coupled through a resistor 94 to the noninverting input of a comparator 96, which forms the principal component of the comparator circuit 42 shown in Figures 2 and 4. The reference voltage is applied to the inverting input of comparator 96 and is provided by the inverting input being coupled through a resistor 98 to voltage V2 and through a resistor 100 to ground. Negative d.c. power supply input, pin 4, of comparator 96 is coupled through a resistor 102 to voltage -V2 and through a capacitor 104 to ground. The junction between negative d.c. power supply input, pin 4, and capacitor 104 is also coupled through a capacitor 106 to positive d.c. power supply input, pin 8. Positive d.c. power supply input, pin 8, also is coupled through a resistor 108 to +V2 voltage. Resistors 102 and 108, and capacitors 104 and 106 provide for d.c. power supply bypassing for comparator 96. The output from comparator 96 is coupled through a resistor 110 back to the input thereof. Resistor 110 provides hysteresis for comparator 96, thus stabilizing its operation when the noninverting

voltage is near the reference voltage. Connected in this manner, comparator circuit 42 provides a positive voltage at its output whenever the voltage at the non-inverting input exceeds the threshold voltage, for example, 0.36 volts. Thus, whenever the output from integrator 40 applied through resistor 94 is above 0.36 volts, the output of comparator 96 becomes a positive voltage.

The voltage from the output of comparator 96 is provided through a resistor 112 to the junction between resistor 46 and capacitor 44. As previously mentioned, this junction also is coupled to threshold circuit 48, which consists of two Schmitt trigger circuits 114 and 116, both of which invert the signal applied thereto.

Level detector 57 includes means (not shown) for detecting if a chamber containing fluid 20 has filled, for providing a trigger signal (LEVEL) to a monostable multivibrator 118. Similarly, means to detect the application of power to apparatus 10 causes a trigger signal (START) to be provided to a monostable multivibrator 120. Both multivibrators 118 and 120 have associated time constant setting components (not shown) which cause either a 100 millisecond or a one second low voltage pulse to be provided at the outputs thereof upon application to either one of the LEVEL or START signals.

The output of NAND gate 60 is coupled through a resistor 122 to the noninverting input of a driver amplifier 124, which is a comparator. The inverting input of amplifier 124 is coupled through a resistor 126 to ground and also through a resistor 128 to voltage +V. Resistors 126 and 128, and voltage +V provide a reference voltage for driver amplifier (or comparator) 124. The output of driver amplifier 124 is coupled through a resistor 130 back to the noninverting input thereof. Resistor 130 provides hysteresis for driver amplifier 124 in order to stabilize amplifier 124 if its non-inverting input voltage is near its threshold voltage. The output of

amplifier 124 also is coupled through a resistor 132 to +V2 and to the gate electrode of transistor 68. Resistor 132 is a pull-up resistor for the output of amplifier 124.

The output from NAND gate 60 also is coupled through a resistor 134 to the inverting input of a driver amplifier 136. The noninverting input to amplifier 136 is coupled through a resistor 138 to ground, a resistor 140 to voltage +V and a resistor 142 to the output of amplifier 136. Resistors 138 and 140 (with voltage +V) provide a threshold voltage for amplifier (or comparator) 136, and resistor 142 provides hysteresis for amplifier 136. The positive d.c. power supply input, pin 3, of amplifier 136 is coupled through a resistor 143 to voltage V2 and through a capacitor 144 to negative d.c. power supply input, pin 12. Negative d.c. power supply input, pin 12, also is coupled through a resistor 146 to voltage -V2 and through capacitor 148 to ground. Resistors 143 and 146, and capacitors 144 and 148 are used to provide d.c. power supply bypassing for amplifier 136. In the particular configuration described here, amplifiers 124 and 136 are contained in the same integrated circuit, and therefore use the same power supply inputs. The output of amplifier 136 is coupled through a resistor 150 to voltage +V2 and to the gate electrode of transistor 70. Resistor 150 is a pull-up resistor for the output of amplifier 136.

Further additions to the circuit shown in Figure 5 include the provision of an inverter 152 between the output of NAND gate 62 and the input of NAND gate 76. Inverter 152 converts NAND gate 62 into an AND gate. In addition, the positive voltage applied to the data (D) input of flip-flop 50 is applied through a resistor 155 and also is applied to the preset input thereof. A RESET signal, which may be provided from an operator controlled switch on the device 10 operator's panel, is provided to the reset input of flip-flop 50.

The following circuit components have been assigned the following values in order to operate in the manner previously described with respect to Figures 2 and 4:

Resistors(ohms)

38--200K
46--10K
80--49.9K (1%)
82--1.0M
84--100K
86--47
92--47
94--2.49K(1%)
98--10K(1%)
100--249(1%)
102--47
108--47
110--249K(1%)
112--100
122--4.7K
126--1.5K
128--3.3K
130--100K
132--10K
134--4.7K
138--1.5K
140--3.3K
142--100K
143--47
146--47
150--10K
155--3.3K

Capacitors(microfarads)

34--.22
44--3.3
54--1.2
88--.01
90--.01
104--.01
106--.01
144--.01
148--.01

Amplifiers and Comparators

55--AD542
96--LM311
124--LM339
136--LM339

Other Components

50--74LS74
60--74LS00
62--74LS00
68--3N163
70--3N163
72--IN4148
74--IN4148
76--74LS00
78--74LS00
114--74LS14
116--74LS14
118--74LS221
120--74LS221
152--74LS14

Referring now to Figure 6, the operation of resistor 46 and capacitor 44 in conjunction with the output of amplifier 96 and Schmitt Trigger circuit 114 now will be described. Reference also will be made to the waveforms of Figure 7 for assistance in understanding the operation of the circuit shown in Figure 6. Comparator 96 includes an output transistor 154, which is rendered conductive by a positive voltage signal applied to the base thereof when the voltage at the noninverting input is less than the voltage at the inverting input. This allows capacitor 44 to discharge through resistor 112 and conductive transistor 154, so that no voltage is held by capacitor 44. Under this situation, Schmitt Trigger circuit 114 provides a logic high output.

Once the signal from integrator 40 applied to the noninverting input of amplifier 96 exceeds the reference voltage at the inverting input, as determined by resistors 98 and 100, the signal provided to the base of transistor 154 falls to a low value, thereby rendering transistor 154 nonconductive. This is shown by the waveform F in Figure 7. Waveform C of Figure 7 is the same signal C indicated earlier in Figure 3. Once transistor 154 becomes nonconductive by signal F going from a high value to a low value, capacitor 44 begins charging to a value determined by the voltage applied to the other side of resistor 46. This voltage can be 5 volts. The time that is required for capacitor 44 to charge to the full voltage is determined by the time constant of resistor 46 and capacitor 44. These values should be selected together with the voltage applied to the other side of resistor 46 so that the time required for capacitor 44 to charge to 1.6 volts, which is the threshold voltage of Schmitt Trigger 114, will be approximately 3.86 milliseconds. This is sufficient time to allow large particles and transient debris to pass through orifice 16, but a small enough time to detect actual blocking debris within or against orifice 16. Once Schmitt Trigger 114 is triggered by capacitor 44 being charged to

1.6 volts or more, the output thereof, which is waveform G of Figure 7, becomes a low value, thereby resulting in a debris alarm occurring, as previously explained.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A debris detector for a particle detector of the type having a small orifice separating two chambers, with a constant current applied through said orifice, and in which particles and debris suspended in a liquid are passed through said small orifice, whereby each particle or debris passing through said orifice causes a voltage pulse across said orifice and debris lodging in or against said orifice causes a d.c. voltage shift across said orifice, and said particle detector further having sensing means to sense the voltage across said orifice, said sensing means further including capacitance means coupling said sensing means to said orifice, said debris detector being characterized by means for integrating the output of said sensing means; and means for determining if the integrated sensing means output exceeds a certain value Vref after a certain delay time.

2. A debris detector according to claim 1 wherein said capacitance means maintains a zero average value voltage at the output of said sensing means for voltage pulses detected due to particles and debris passing through said orifice further characterized in that the output of said means for integrating is a pulse voltage for each particle and debris passing through said orifice and a step voltage for debris lodging in or against said orifice.

3. A debris detector according to claims 1 or 2 wherein said capacitance means causes an undershoot of the voltage at the falling edge of each voltage pulse sensed further characterized in that the output of said means for integrating is a pulse voltage for each particle and debris passing through said orifice and a step voltage for debris lodging in or against said orifice.

4. A debris detector according to claim 3 further characterized in that said means for determining includes

voltage comparator means for providing an output signal in response to the integrating means output signal remaining above a certain reference value Vref for said certain delay time after initially being above said certain reference value Vref.

5. A debris detector according to claim 1 further characterized in that said integrating means provides a voltage at its output related to the integral of said sensing means output voltage; and in that said means for determining includes: voltage comparator means having one input (+) coupled to said integrating means output and a second input (-) coupled to a source of reference voltage +V2, and an output at which normally appears a voltage pulse having a leading edge whenever the voltage at said integrating means output exceeds said reference voltage +V2; second capacitance means, including a charge path therefore, coupled to said comparator means output for being charged to above a threshold value Vth during said certain delay time following said voltage at said integrating means output exceeding said reference voltage +V2; and threshold sensing means for sensing said second capacitance means being charged to a value exceeding said threshold value Vth and for providing a signal manifesting the detection of lodged debris.

6. A debris detector according to claim 5 further characterized in that said second capacitance means discharges whenever said voltage applied to said first input of said comparator means is below said reference voltage Vref.

7. A debris detector according to claims 5 or 6 further characterized in that said charge path for said second capacitance means includes a resistance, the value of said second capacitance means and said resistance being selected to determine said certain delay time.

8. A debris detector according to claims 1, 5 or 6 further characterized in that said debris detector further includes means for inhibiting said debris detector for a fixed time following the application of current to said orifice.

9. A debris detector according to claim 8 further characterized in that said means for integrating includes a capacitor and said means for inhibiting discharges said integrating means capacitor.

10. A debris detector according to claim 9 further characterized in that said charge path for said second capacitance means includes a resistance, the value of said second capacitance means and said resistance being selected to determine said certain delay time.

11. A debris detector substantially as hereinbefore described with reference to the accompanying drawings.

DATED this 11th day of May, 1990.

COULTER ELECTRONICS, INC.
By its Patent Attorneys
DAVIES & COLLISON

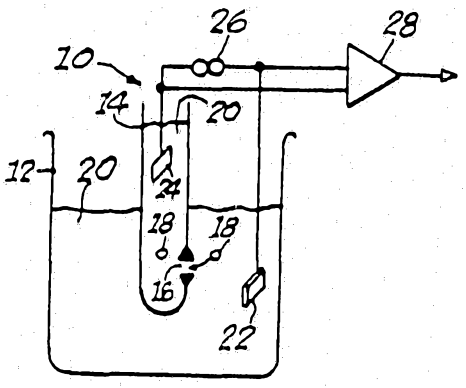


Fig. 1.

Fig. 3.

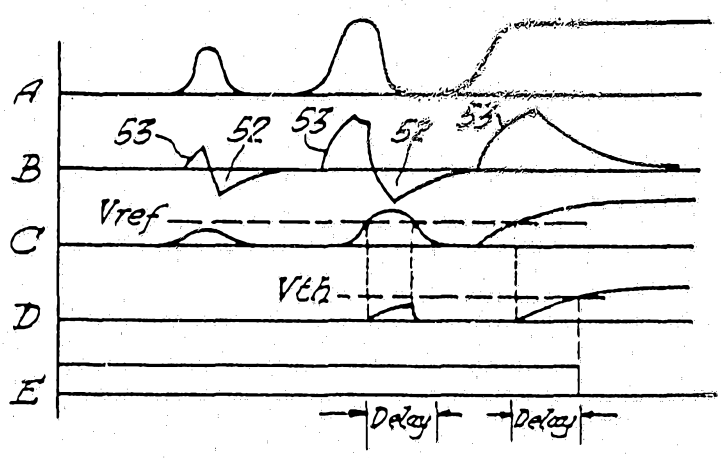
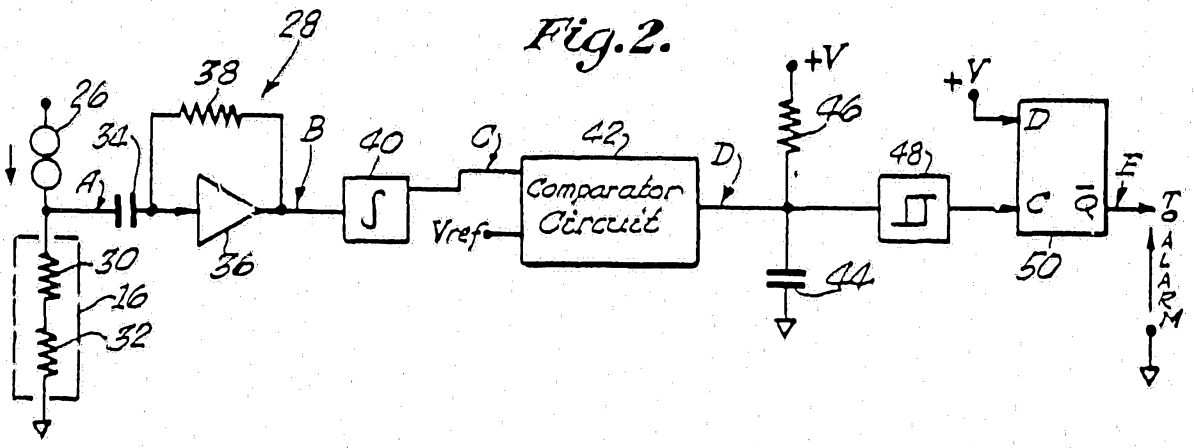


Fig. 2.



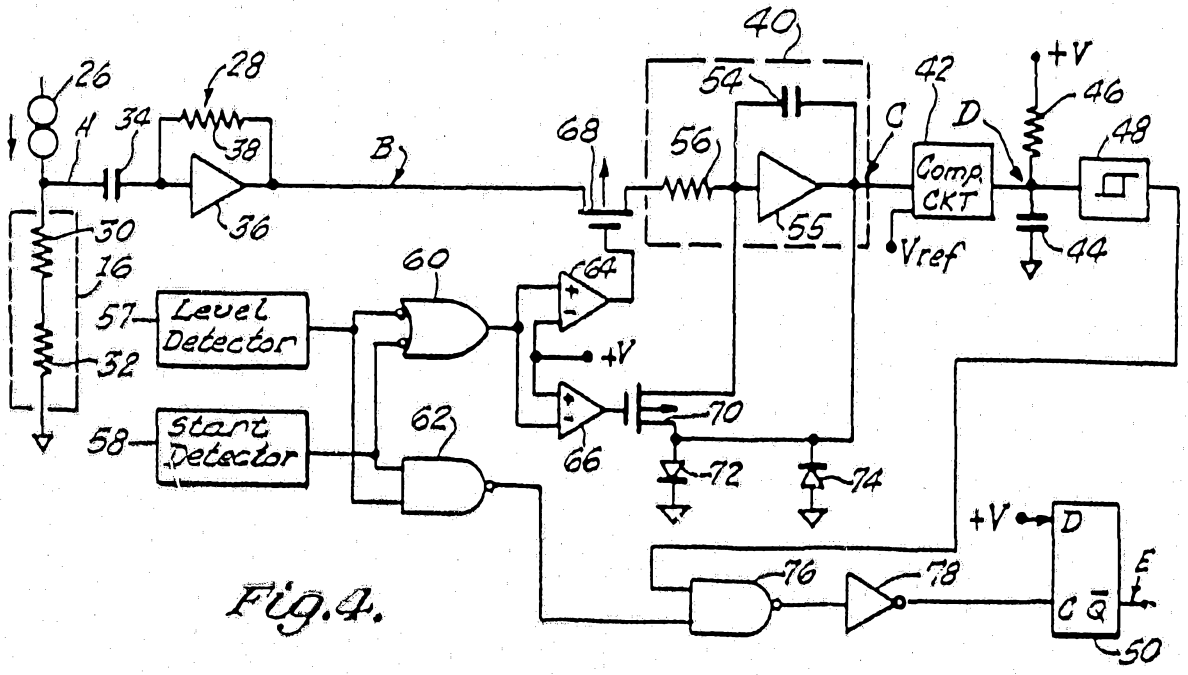


Fig. 4.

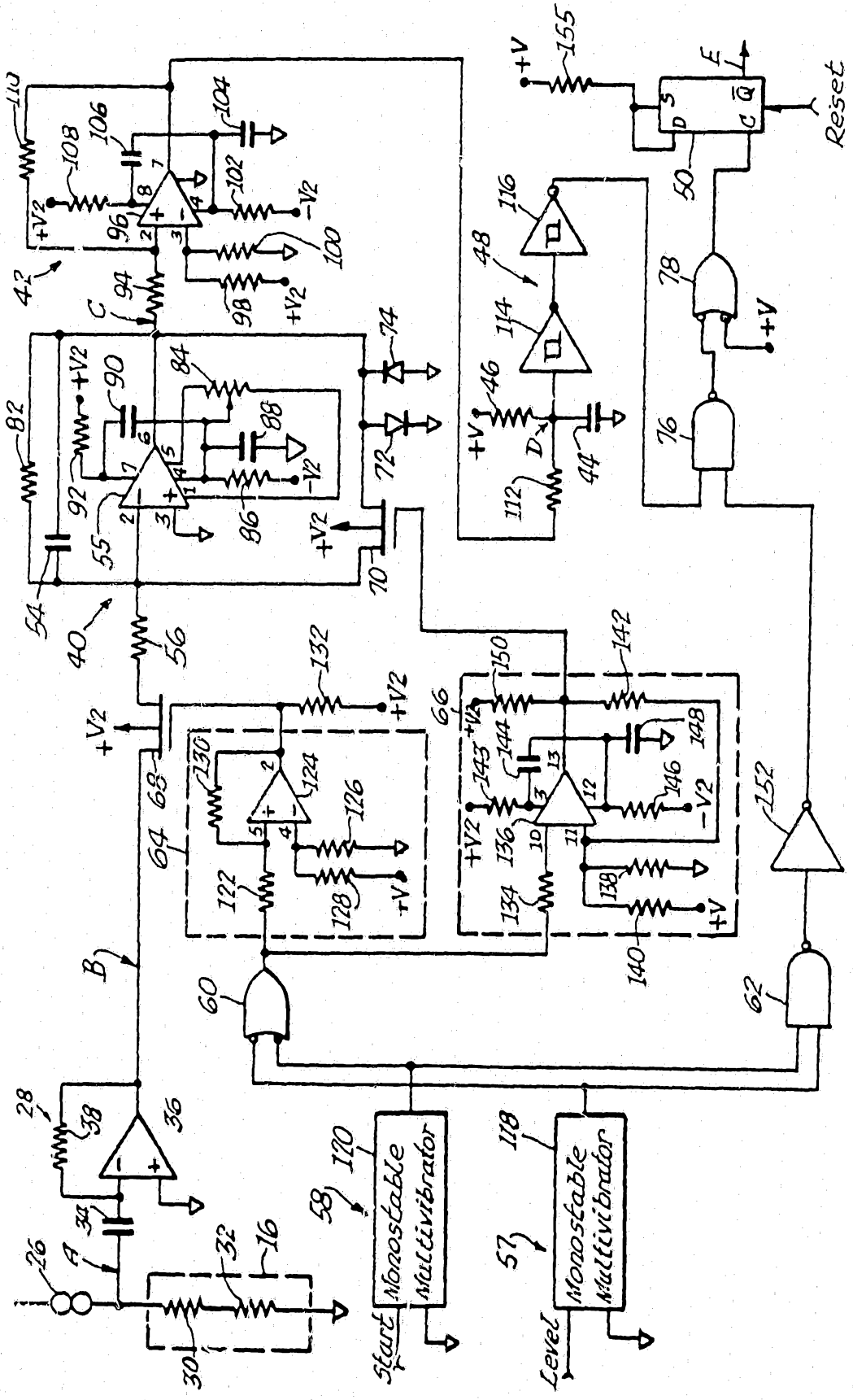

Monostable Multivibrator
Start
Monostable Multivibrator
Level
Reset
+V
+V2
-V2

Fig. 5.

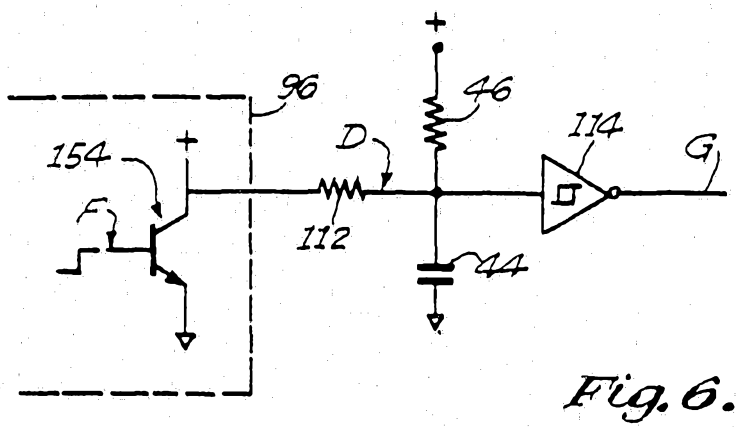


Fig. 6.

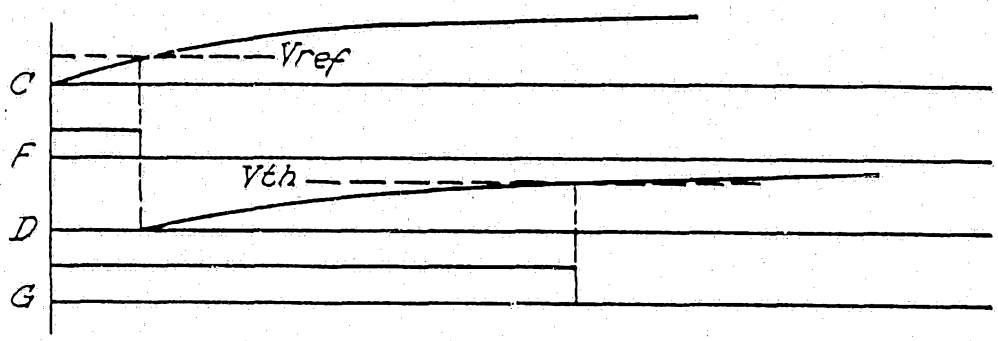


Fig. 7.

INTERNATIONAL SEARCH REPORT

International Application No PCT/US87/02537

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (4): G01N 27/00

U.S. CL. 324/71.1 71.4; 377/12

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	324/71.1, 71.4, 438, 439, 450 377/12, 30 361/89, 94, 110

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	US, A, 3,259,842 (W H COULTER) 05 July 1966 See entire document.	1-10
A	US, A, 3,938,038 (COULTER ELECTRONICS, INC), 02 February 1976, See entire document.	1-10
A	US, A, 3,978,374 (SOCIETE ANONYME DES ATELIERS DE SECHERON), 31 August 1976, See entire document.	1-10
A	US, A, 3,987,391 (COULTER ELECTRONICS, INC) 19 October 1976, See figure 1.	1-10
Y	US, A, 4,326,230 (SEIMENS AKTIENGESELLSCHAFT) 20 April 1982, See entire document.	1-10
A	US, A, 4,412,175 (COULTER ELECTRONICS, INC) 25 October 1983, See Figures 1-5.	2,3
A	US, A, 4,558,310 (RAYMOND MCALLISE) 10 December 1985 See Figures 1, 2, 3, 7, 8.	1-10
A	US, A 4,590,533 (MITSBISHI DENKI KABUSHIKI KAISHA) 20 May 1986, See entire document.	1-10

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
28 January 1988	10 FEB 1988
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	Jonathan Wysocki

See notes on accompanying sheet

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A,P	US, A, 4,680,552 (ERMA OPTICAL WORKS LTD, ULYAC SERVICE CORPORATION), 14 July 1987 See entire document.	1-10

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers , because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers , because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.