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(54) **Title**: RECEIVER FOR MULTI-WIRE COMMUNICATION WITH REDUCED INPUT CAPACITANCE

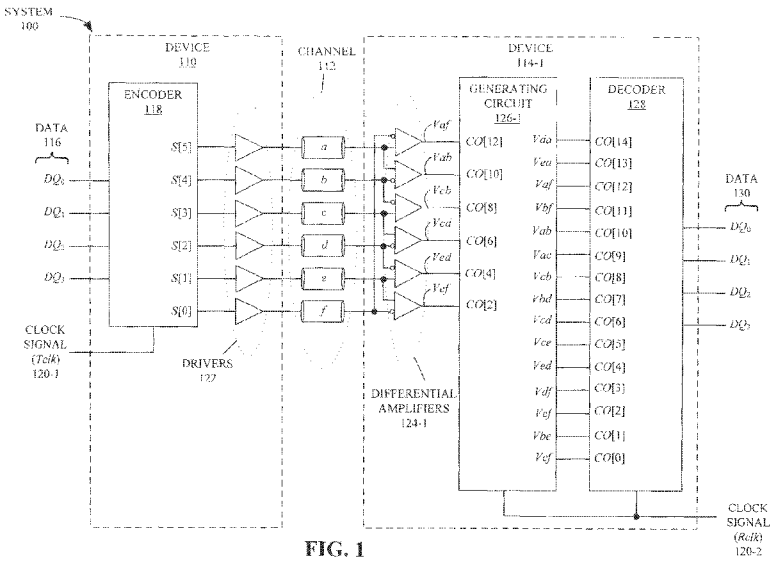

FIG. 1

(57) **Abstract**: Embodiments of a device that receives and decodes a series of parallel symbol sets over a series of time intervals is described. In this device, symbols in a respective parallel symbol set are received on nodes. Each node receives a respective symbol, which can have one of two possible logical values (*e.g.*, a logic 0 or a logic 1). Differential amplifiers in the device provide primary comparison results, each of which compares symbols received on pairs of the links, and generation circuits in the device provide secondary comparison results from the primary comparison results. A decoder in the device decodes a respective parallel symbol set from the primary and secondary comparison results to recover encoded data.

WO 2009/086078 A4

AMENDED CLAIMS
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What is claimed is:

1. An integrated circuit comprising:

input nodes to receive a series of parallel symbol sets over a series of time intervals;

comparison circuits, each comparison circuit having at least a first input terminal, coupled to a respective input node, and a comparison-circuit output node to provide primary comparison results;

generation circuits, each generation circuit having second and third input terminals, coupled to at least a respective pair of the comparison-circuit output nodes, and a generation-circuit output node to provide secondary comparison results, wherein the primary comparison results and the secondary comparison results produce a set of determinate logical values and a set of indeterminate logical values; and

a decoder having decoder input terminals coupled to the comparison-circuit output nodes and the generation-circuit output nodes, the decoder to decode the symbol sets from the determinate logical values of the primary comparison results and the secondary comparison results.

2. The integrated circuit of claim 1, wherein the comparison circuits include differential amplifiers and the primary comparison results are relative to a reference voltage.

3. The integrated circuit of claim 1, wherein the comparison circuits include single-ended amplifiers and each of the primary comparison results is relative to an internal reference voltage of a respective single-ended amplifier.

4. The integrated circuit of claim 1, wherein each comparison circuit has the first input terminal and a fourth input terminal, coupled to respective ones of a pair of the input nodes.

5. The integrated circuit of claim 4, wherein the comparison circuits include differential amplifiers.

6. The integrated circuit of claim 1, wherein the generation circuits include differential amplifiers.

7. The integrated circuit of claim 1, wherein the combination of the comparison circuits and the generation circuits provide comparisons for all pairs of symbols a respective symbol set received on the input nodes.

8. The integrated circuit of claim 1, wherein there are M symbols in each symbol set; and wherein there are less than $M(M-1)/2$ comparison circuits.

9. The integrated circuit of claim 1, wherein there are M symbols in each symbol set; and wherein there are $M(M-1)/2$ comparisons in the combination of the primary comparison results and the secondary comparison results.

10. The integrated circuit of claim 1, wherein the symbols in each symbol set include a first symbol type representative of a logic zero and a second symbol type representative of a logic one.

11. The integrated circuit of claim 10, wherein there are equal numbers of the first symbol type and the second symbol type in each symbol set.

12. The integrated circuit of claim 1, wherein the integrated circuit is to communicate information during inter-chip or intra-chip communication.

13. The integrated circuit of claim 1, wherein the integrated circuit includes a memory controller or a dynamic random access memory (*DRAM*).

14. The integrated circuit of claim 1, wherein the generating circuit includes a sample-and-hold circuit.

15. An integrated circuit comprising:

input nodes to receive a series of parallel symbol sets over a series of time intervals;

comparison circuits, each comparison circuit having at least a first input terminal, coupled to a respective input node, and a comparison-circuit output node to provide primary comparison results;

generation circuits, each generation circuit having second and third input terminals, coupled to at least a respective pair of the comparison-circuit output nodes, and a generation-circuit output node to provide secondary comparison results, wherein the primary comparison results and the secondary comparison results produce a set of determinate logical values and a set of indeterminate logical values; and

means for decoding the symbol sets from the determinate logical values of the primary comparison results and the secondary comparison results.

16. A system, comprising an integrated circuit that includes:

input nodes to receive a series of parallel symbol sets over a series of time intervals;

comparison circuits, each comparison circuit having at least a first input terminal, coupled to a respective input node, and a comparison-circuit output node to provide primary comparison results;

generation circuits, each generation circuit having second and third input terminals, coupled to at least a respective pair of the comparison-circuit output nodes, and a generation-circuit output node to provide secondary comparison results, wherein the primary comparison results and the secondary comparison results produce a set of determinate logical values and a set of indeterminate logical values; and

a decoder having decoder input terminals coupled to the comparison-circuit output nodes and the generation-circuit output nodes, the decoder to decode the symbol sets from the determinate logical values of the primary comparison results and the secondary comparison results.

17. A method for communicating information, the method comprising:

receiving a series of parallel symbol sets over a series of time intervals, the symbols in each symbol set received on respective nodes, and for each of the symbol sets:

comparing symbols on the nodes to determine primary comparison results; and

generating secondary comparison results from the primary comparison results, wherein the primary comparison results and the secondary comparison results produce a set of determinate logical values and a set of indeterminate logical values; and

decoding the respective symbol set from the determinate logical values of the primary comparison results and the secondary comparison results.

18. The method of claim 17, wherein the primary comparison results are relative to a reference voltage.

19. The method of claim 17, wherein each comparison result is for symbols received on a respective pair of the input nodes.

20. The method of claim 17, wherein the combination of the primary comparison results and the secondary comparison results provide comparisons for all pairs of symbols in the respective symbol set received on the input nodes.

21. The method of claim 17, wherein there are M symbols in each symbol set; and wherein there are less than $M(M\text{-}1)/2$ primary comparison results.

22. The method of claim 17, wherein there are M symbols in each symbol set; and wherein there are $M(M\text{-}1)/2$ comparisons in the combination of the primary comparison results and the secondary comparison results.

23. An integrated circuit comprising:

input nodes to receive a series of parallel symbol sets over a series of time intervals;

comparison circuits, each comparison circuit having at least a first input terminal, coupled to a respective input node, and a comparison-circuit output node to provide comparison results, each comparison corresponding to a respective one of three analog values, wherein two of the three analog values are determinate logical values and the third analog value is an indeterminate logical value;

a decoder having decoder input terminals coupled to the comparison-circuit output nodes, the decoder to decode the symbol sets from the determinate logical values of the comparison results.

24. The integrated circuit of claim 23, wherein there are M symbols in each symbol set; and

wherein there are less than $M(M\text{-}1)/2$ comparison results.

25. An integrated circuit comprising:

input nodes to receive a series of parallel symbol sets over a series of time intervals;

comparison circuits, each comparison circuit having a first input terminal, coupled to a respective input node, a second input terminal, coupled to a common node, and a comparison-circuit output node to provide comparison results, wherein the common node is coupled to and partially terminates the input nodes, and wherein the comparison results produce a set of determinate logical values and a set of indeterminate logical values; and

a decoder having decoder input terminals coupled to the comparison-circuit output

nodes, the decoder to decode the symbol sets from the determinate logical values of the comparison results.

26. The integrated circuit of claim 25, wherein the common node is coupled to a reference voltage.

27. The integrated circuit of claim 26, wherein the reference voltage is adjustable.

28. The integrated circuit of claim 25, further comprising a low-pass filter coupled to the common node.

29. The integrated circuit of claim 25, wherein the common node includes a virtual ground.

30. A system, comprising an integrated circuit that includes:

input nodes to receive a series of parallel symbol sets over a series of time intervals;

comparison circuits, each comparison circuit having a first input terminal, coupled to a respective input node, a second input terminal, coupled to a common node, and a comparison-circuit output node to provide comparison results, wherein the common node is coupled to and partially terminates the input nodes, wherein the comparison results produce a set of determinate logical values and a set of indeterminate logical values; and

a decoder having decoder input terminals coupled to the comparison-circuit output nodes, the decoder to decode the symbol sets from the determinate logical values of the comparison results.

31. A method for communicating information, the method comprising:

coupling input nodes to a common node, which partially terminates the input nodes;

receiving a series of parallel symbol sets over a series of time intervals, the symbols in each symbol set received on respective input nodes, and for each of the symbol sets:

comparing symbols on the nodes to a reference voltage to determine comparison result, wherein the comparison results produce a set of determinate logical values and a set of indeterminate logical values s; and

decoding a respective symbol set from the determinate logical values of the comparison results.

Statement Explaining Amendment to PCT/US2008/087639 under Article 19(1)

Applicants herewith have amended the claims via replacement claim sheets to more particularly point out the novel features of the present invention. Reference D1 (US 6,278,740 B1) and D2 (US 6,734,811 B1) do not show the invention of any of Applicants' claims.

In this regard, Applicants' claims do not merely relate to a vector signaling decoder that decodes an M symbol vector into an $N < M$ symbol vector via pure Boolean logic. Such a vector signaling decoder requires relatively complex circuitry. Applicants' invention relates to a novel circuit that decodes an M symbol vector in a manner not addressed by any of the cited art.

With reference to Applicants' disclosed embodiments and Figures, FIG. 1 shows a decoder 128 which includes a set of differential amplifiers 124-1 and generating circuit 126-1 that produce comparison results for link pairs of a data channel 112. A comparison result corresponds to an analog output of a differential amplifier (e.g., signal *Vda*), which has its positive and negative input terminals coupled to two channel links (e.g., channel links *d* and *a*, respectively). Specifically, the comparison results can have one of three analog output values: a negative voltage (denoted by '-1'), a positive voltage (denoted by '1'), and an intermediate voltage (e.g., 0 Volts, denoted by '0').

FIG. 3A shows the symbol sets produced for the comparison results after analog-to-digital conversion (i.e., symbol sets CO[14:0]). A negative analog voltage is interpreted as a logic zero value (denoted by '0'), a positive analog voltage is interpreted as a logic one value (denoted by '1'), and an intermediate analog voltage produces an indeterminate logic value (which can be a logic zero or a logic one, denoted by '*x*') that is not used to determine the decoded data. Conventional decoders, on the other hand use additional combinational logic (e.g., majority voting logic) to first determine the encoded symbol vector from a set of comparison results that include indeterminate values, and then use the encoded symbol vector to determine the decoded data. For example, cited reference D1 employs majority logic to determine the logical state of a channel link from a set of determinate and indeterminate comparison results, and then uses this logical state information (i.e., an encoded codeword) to determine the decoded data.

With the present invention, the determinate values (i.e., the non-*x* values) in the symbol sets CO[14:0] provide sufficient information to uniquely identify each codeword. Each encoded codeword produces a set of comparison results that includes at least one assuredly different result for each of the other sets of comparisons. Decoder 128 can thus resolve each codeword, and consequently the encoded data, despite the indeterminate values of a subset of the comparisons. Therefore, decoder 128 can resolve each codeword, without using the indeterminate logic values and without using a majority logic, to produce the decoded data. Because the determinate values of the comparison results are sufficient for identifying each codeword, some of Applicants' embodiments and some of Applicants' detailed claims relate to generation circuits that produce a set of determinate results and a set of indeterminate results, such that the determinate results provide sufficient information for decoding the received parallel symbol sets.

Applicants believe that the claims, both as amended and previous to amendment, present the invention in a manner not taught by the cited art.

STATEMENT UNDER ARTICLE 19 (1)