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AKIMOTO

(54) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

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H01L 21/336 (2006.01)

(52) **U.S. Cl.** **438/104**; 438/151; 257/E21.411

(57) **ABSTRACT**

To provide a semiconductor device in which a defect or fault is not generated and a manufacturing method thereof even if a ZnO semiconductor film is used and a ZnO film to which an n-type or p-type impurity is added is used for a source electrode and a drain electrode. The semiconductor device includes a gate insulating film formed by using a silicon oxide film or a silicon oxynitride film over a gate electrode, an Al film or an Al alloy film over the gate insulating film, a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film, and a ZnO semiconductor film over the ZnO film to which an n-type or p-type impurity is added and the gate insulating film.

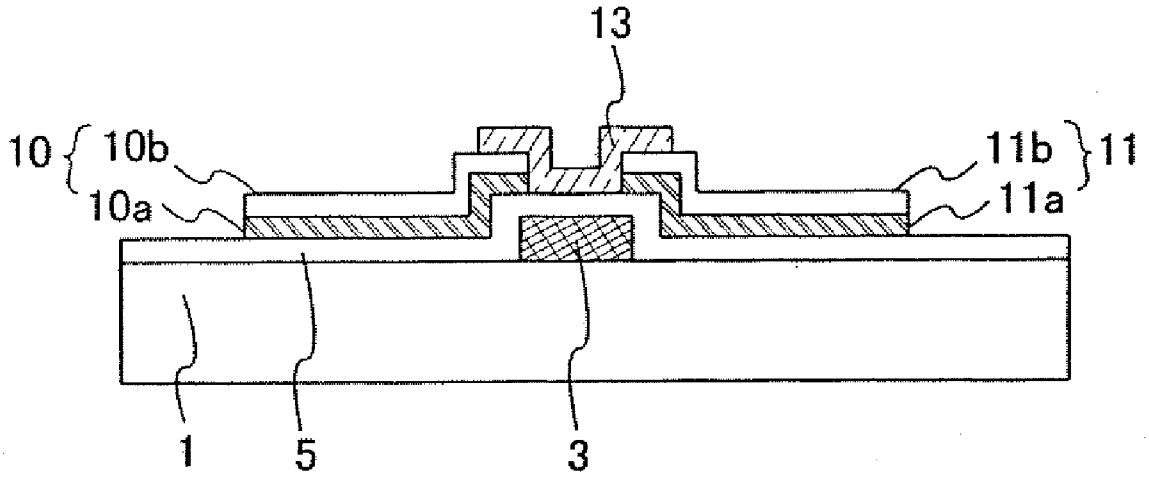

FIG. 1A

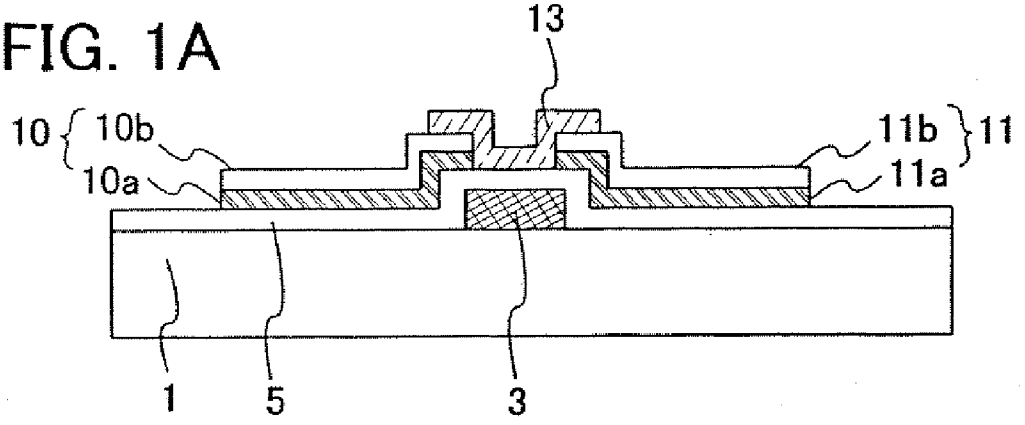

FIG. 1B

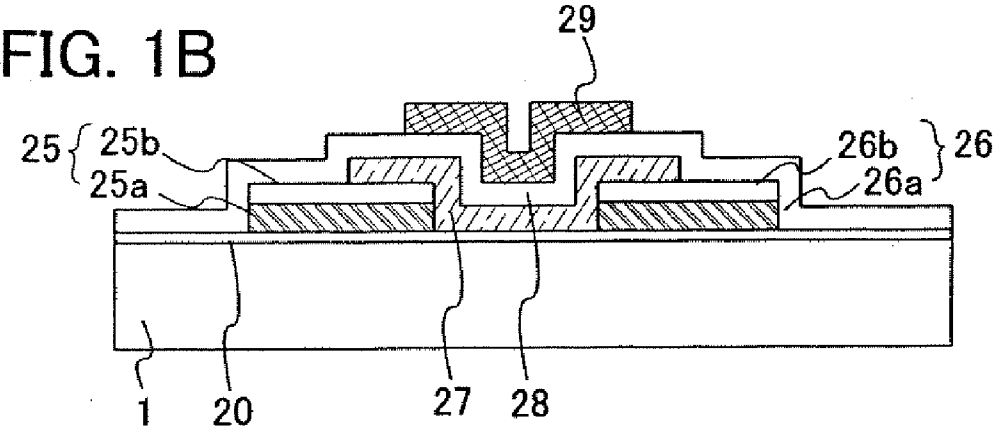

FIG. 2A

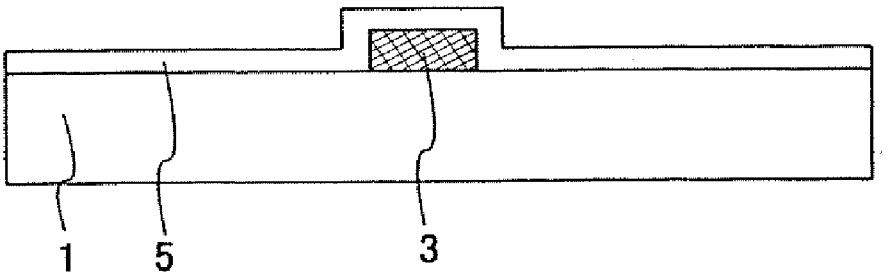

FIG. 2B

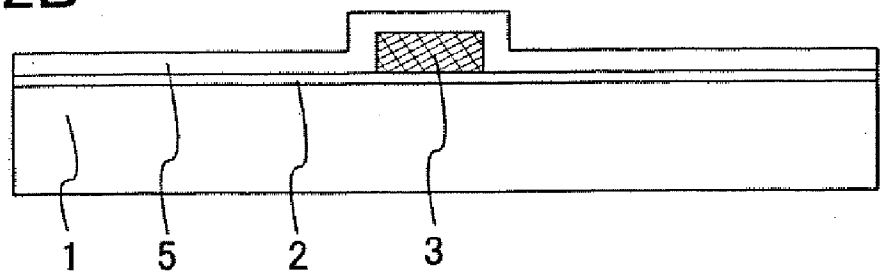

FIG. 2C

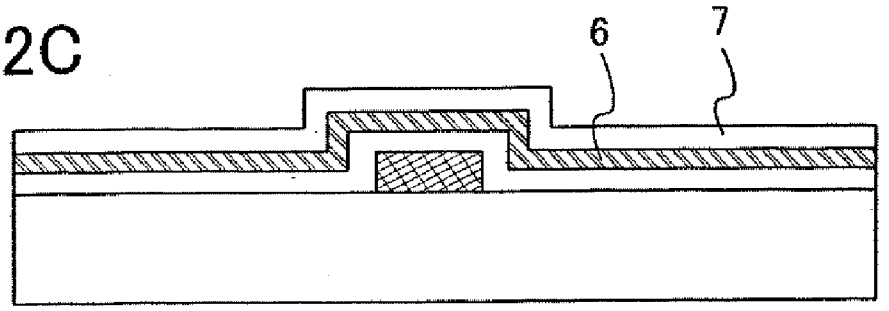

FIG. 2D

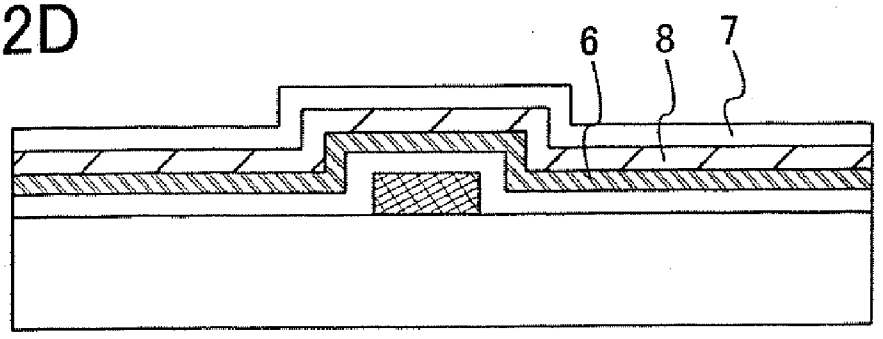

FIG. 3A

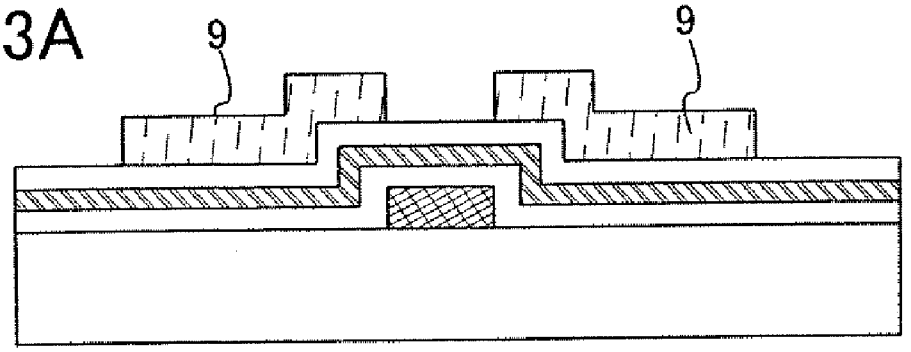

FIG. 3B

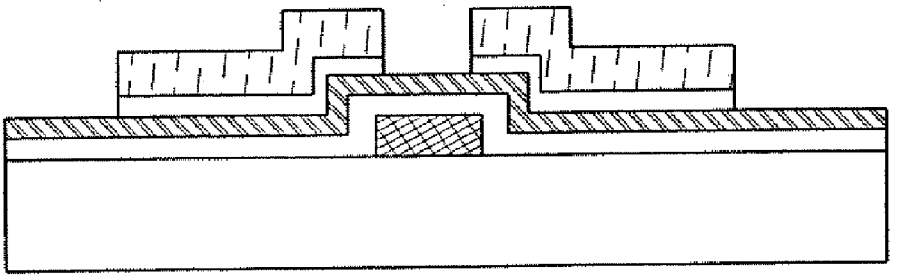

FIG. 3C

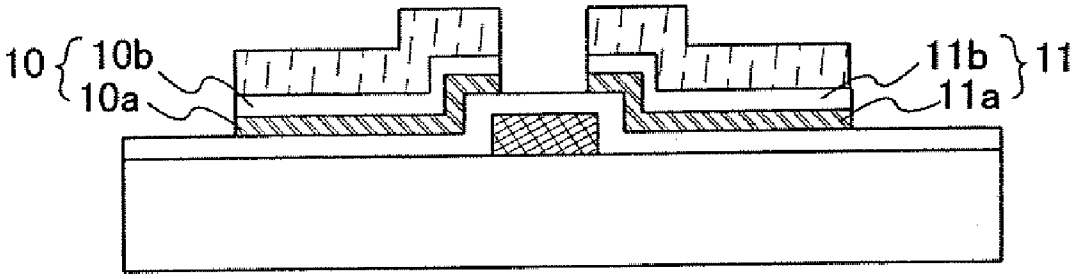

FIG. 3D

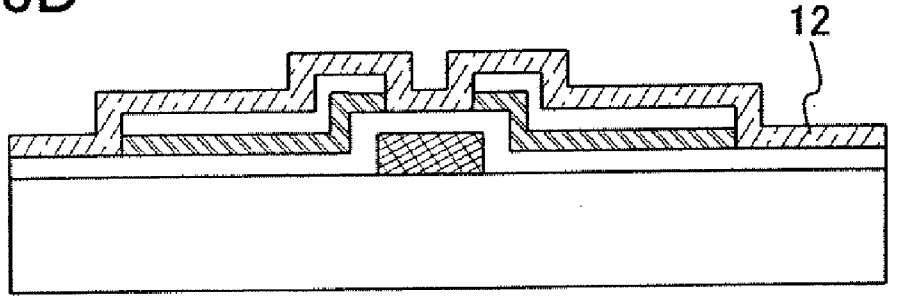

FIG. 4A

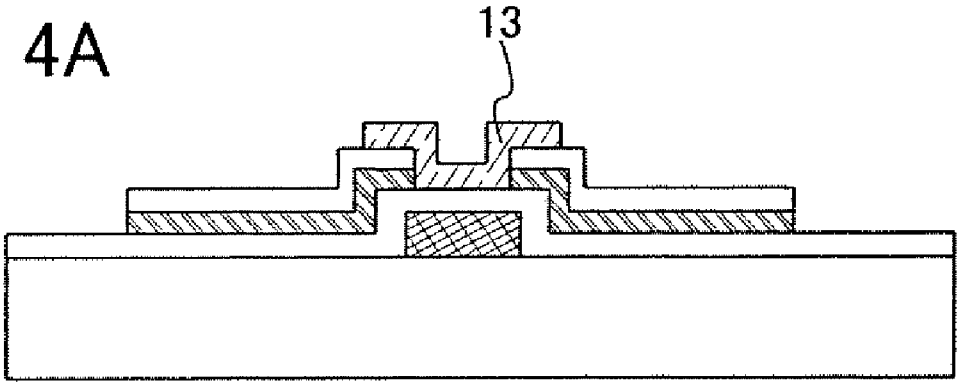

FIG. 4B

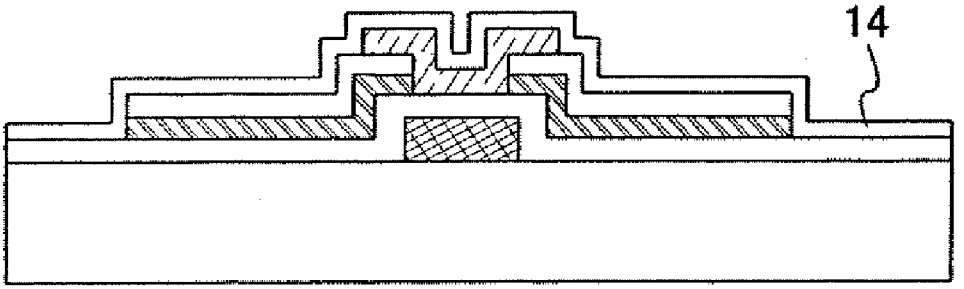

FIG. 5A

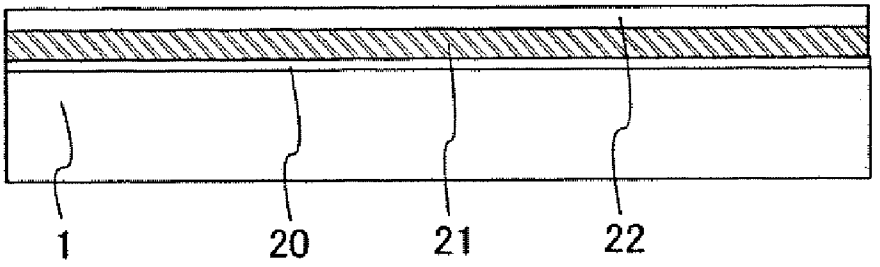

FIG. 5B

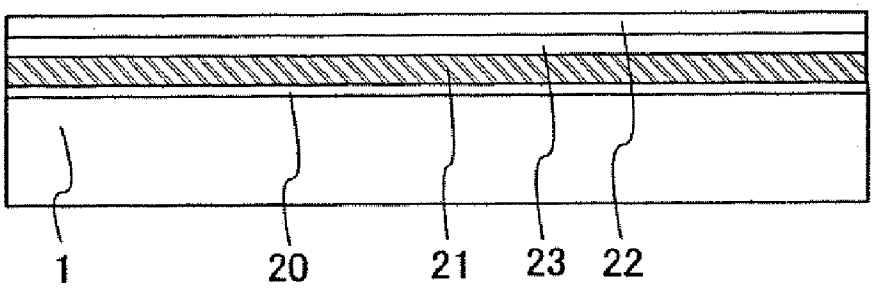

FIG. 5C

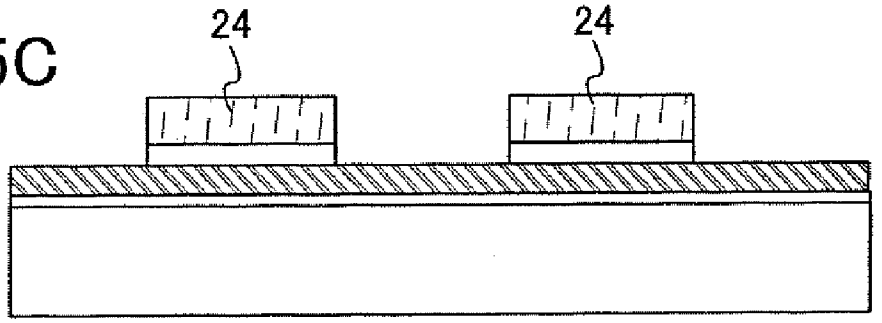

FIG. 5D

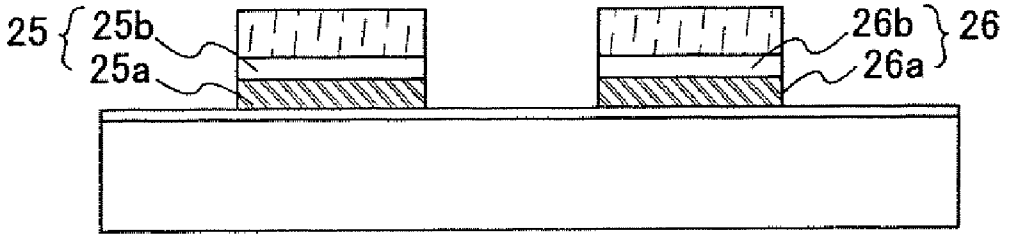

FIG. 6A

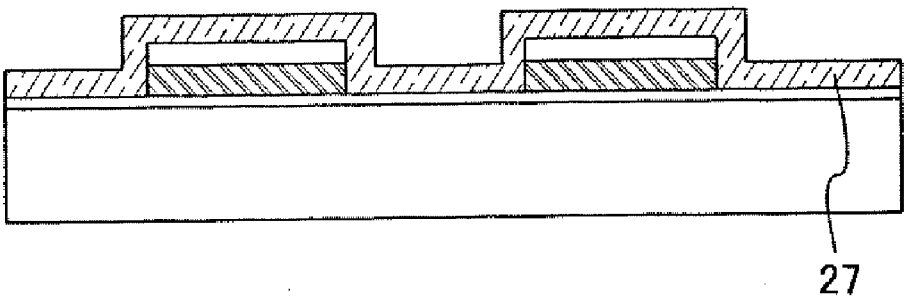

FIG. 6B

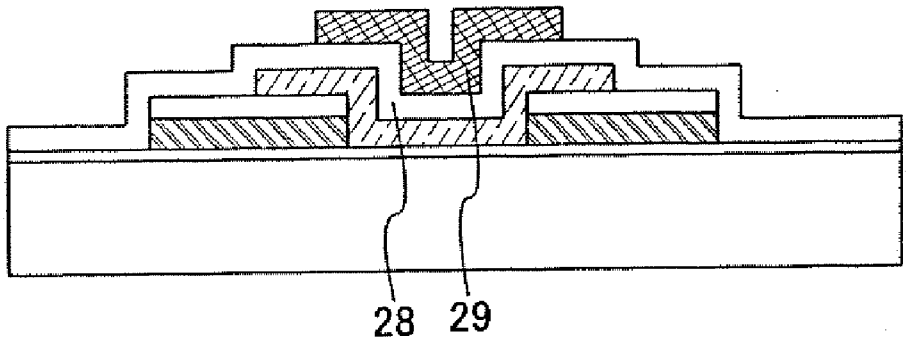

FIG. 6C

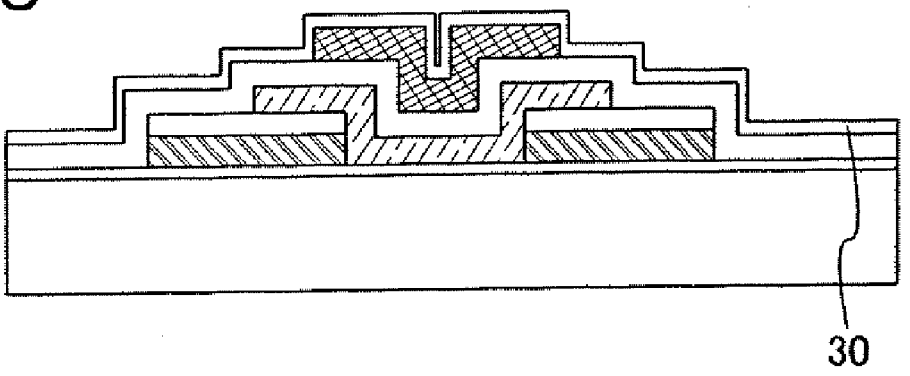

FIG. 7A

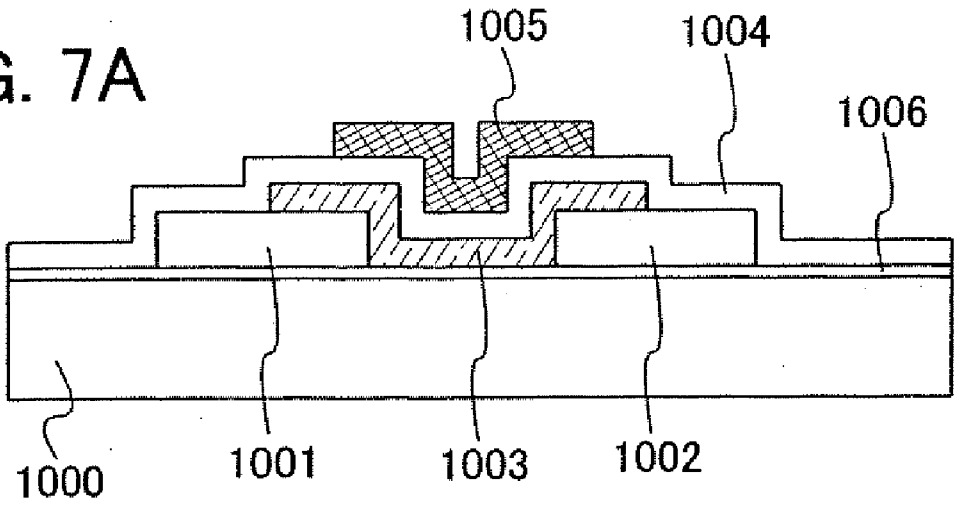
1005
1004
1006
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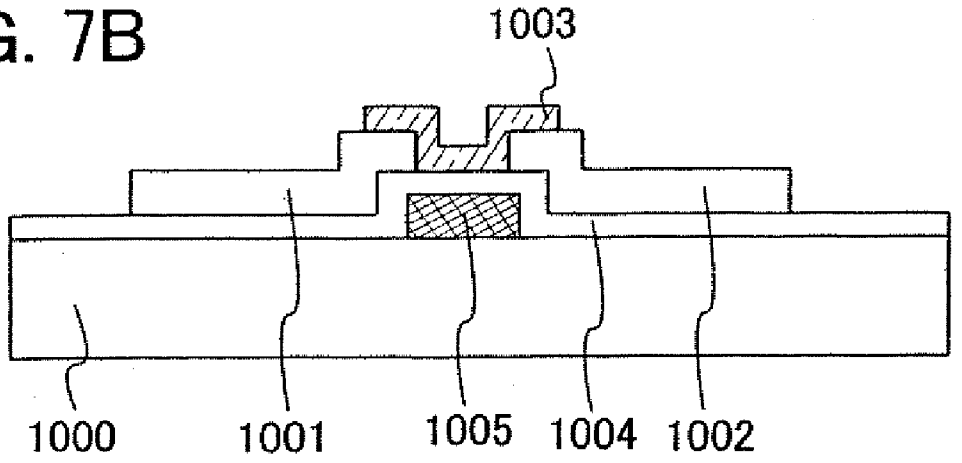
FIG. 7B


1003
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1001
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FIG. 8A

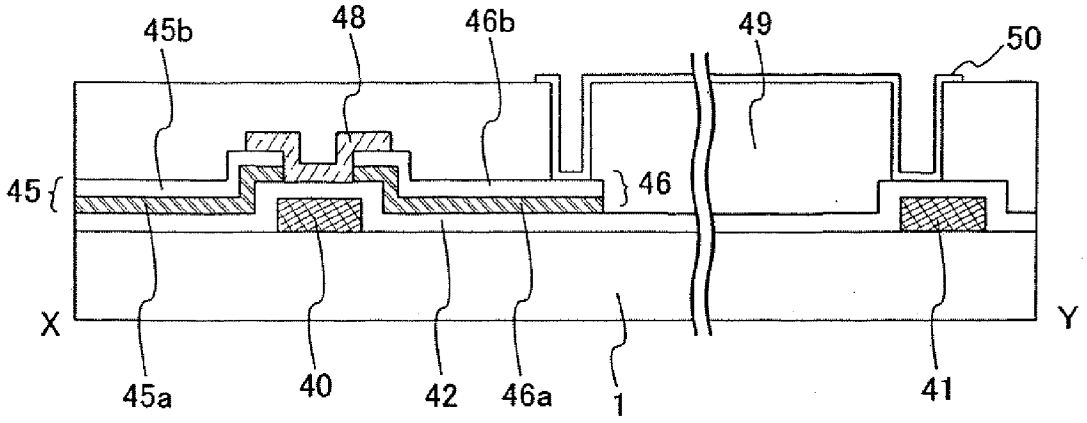

FIG. 8B

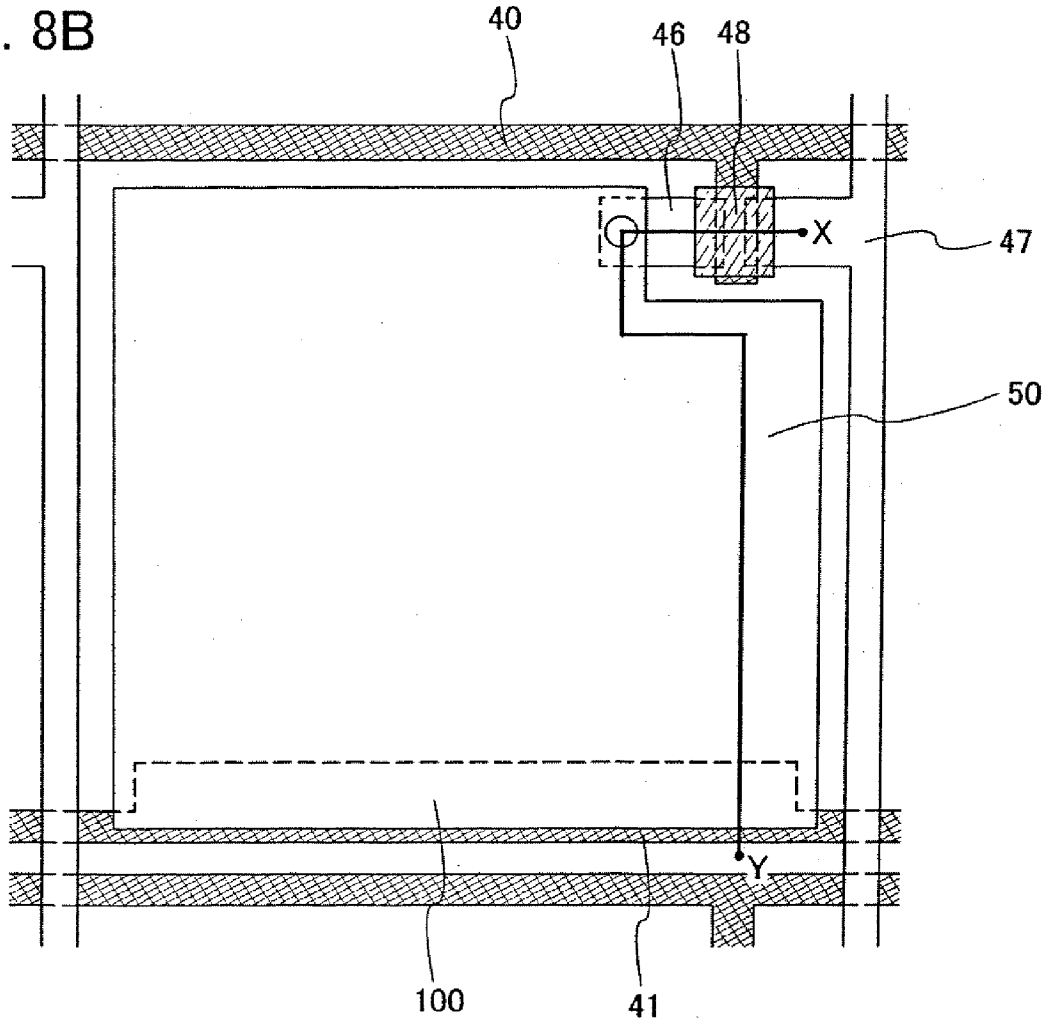

FIG. 9A

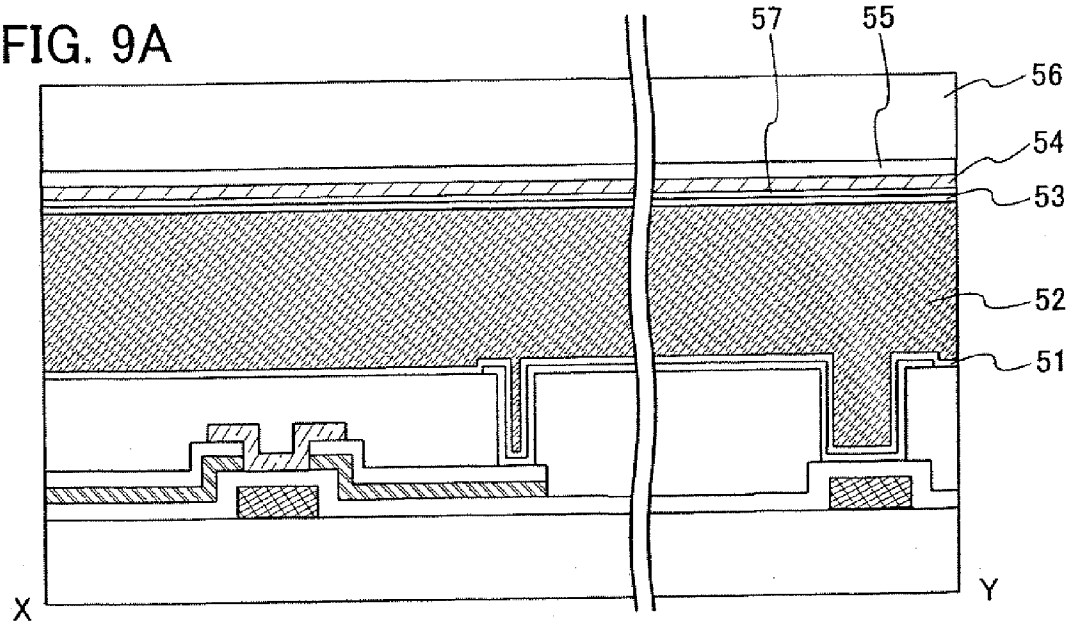
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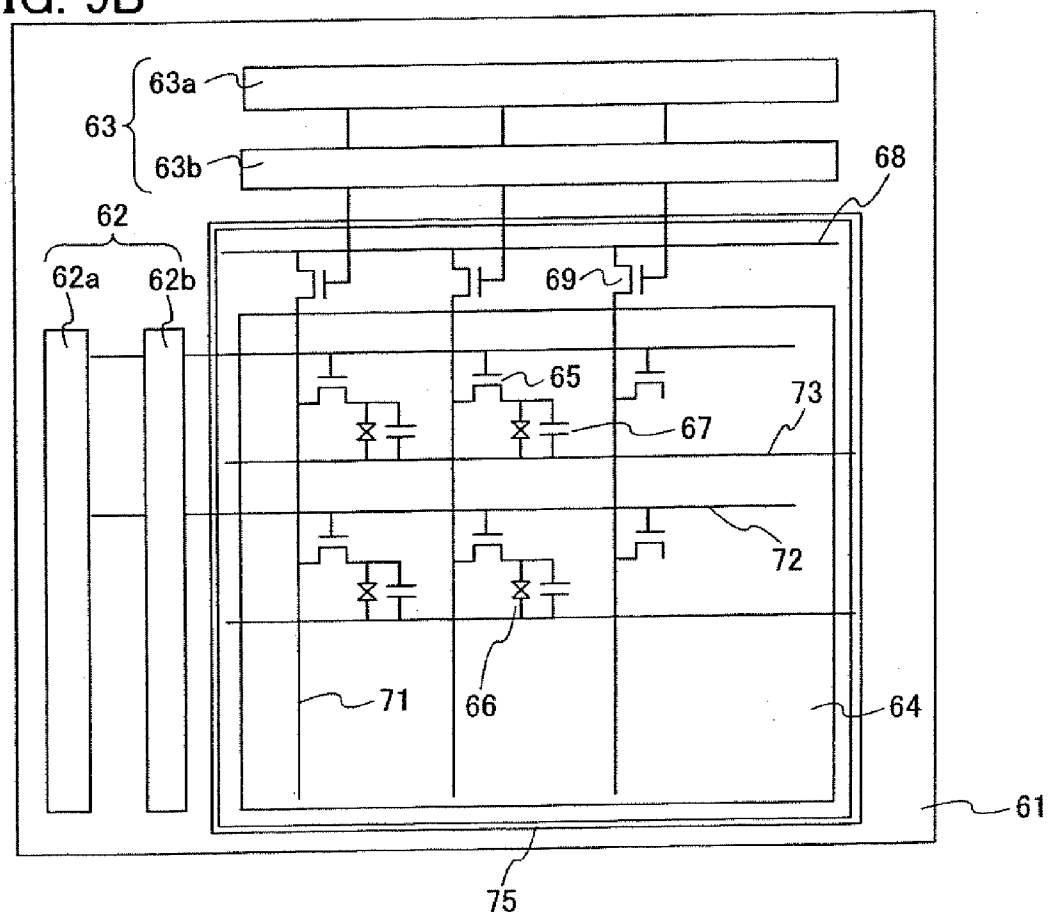
FIG. 9B


63
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63b
62
62a
62b
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FIG. 10A

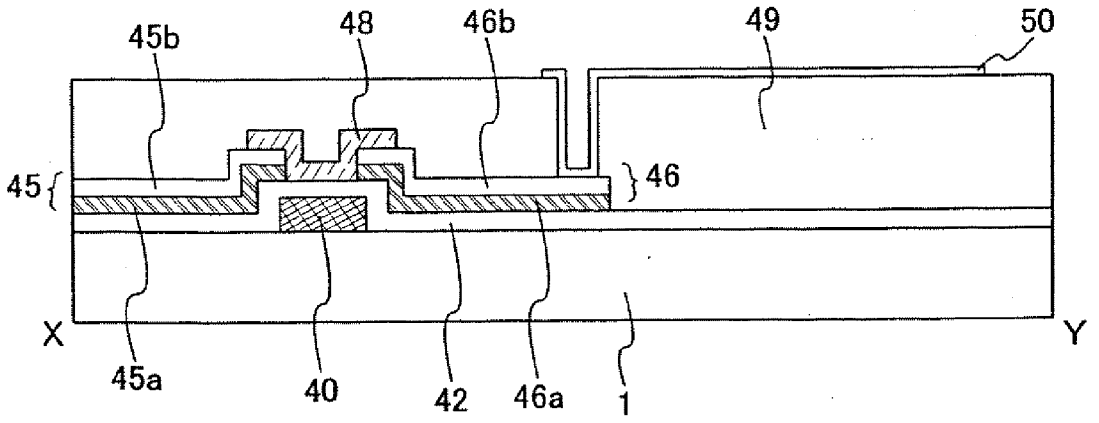

FIG. 10B

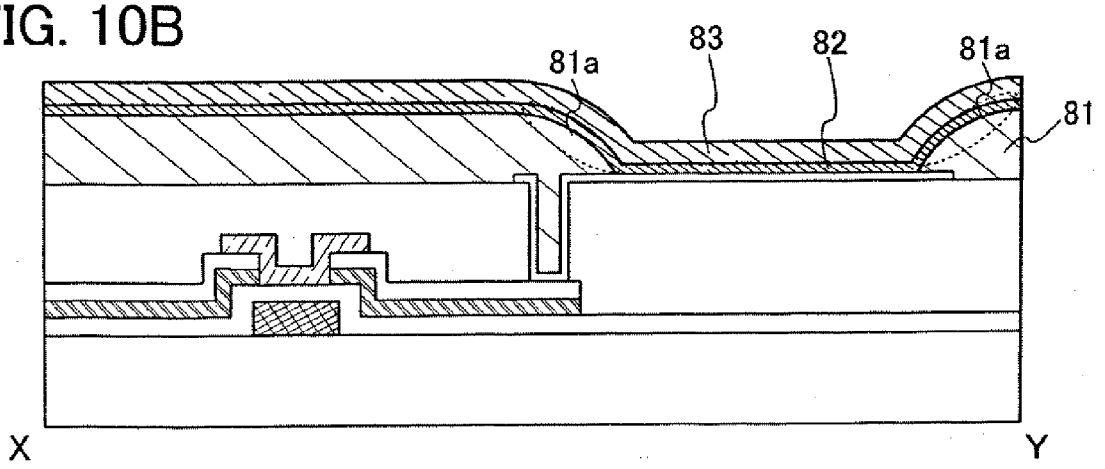

FIG. 11A

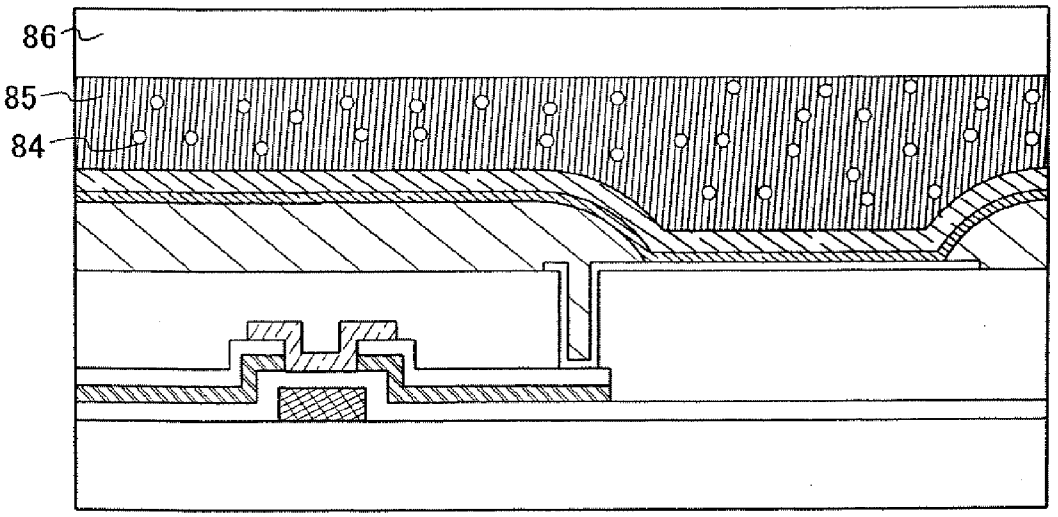

FIG. 11B

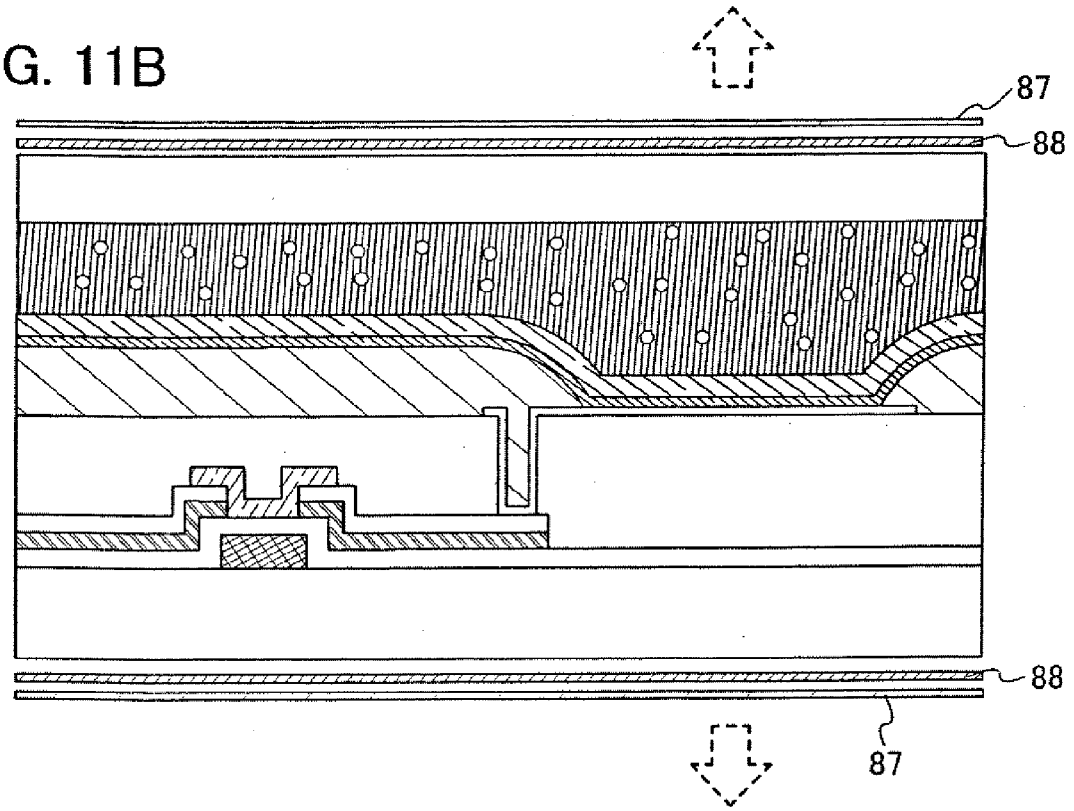

FIG. 12A

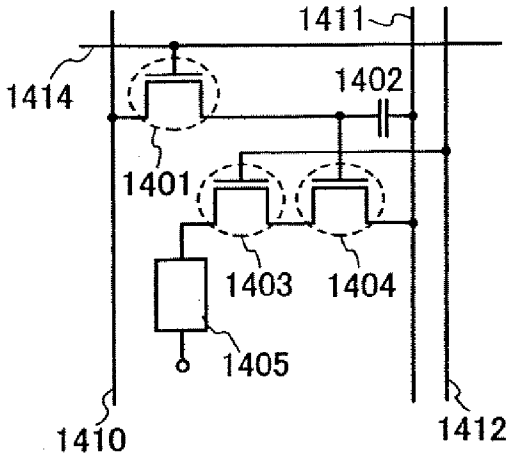

FIG. 12B

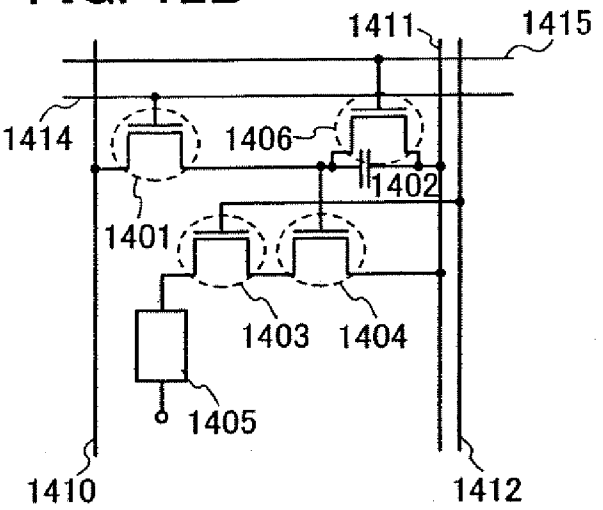

FIG. 12C

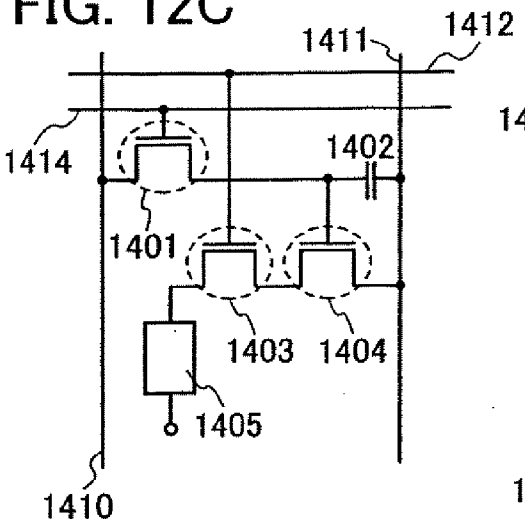

FIG. 12D

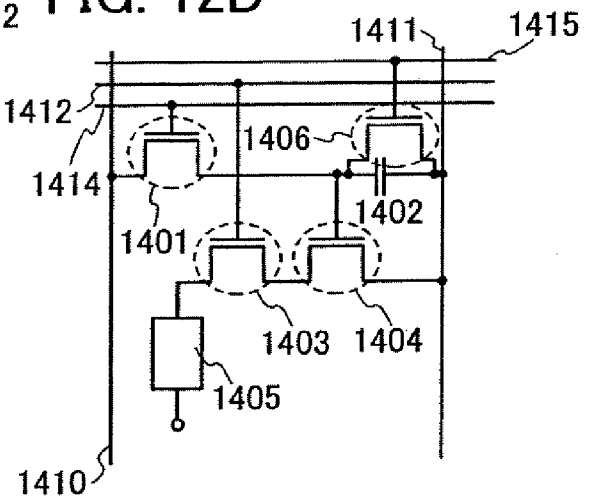

FIG. 12E

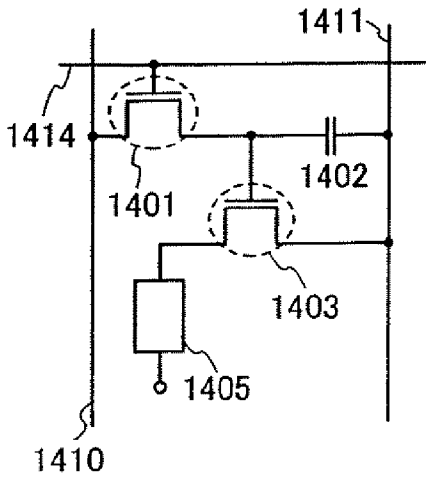

FIG. 12F

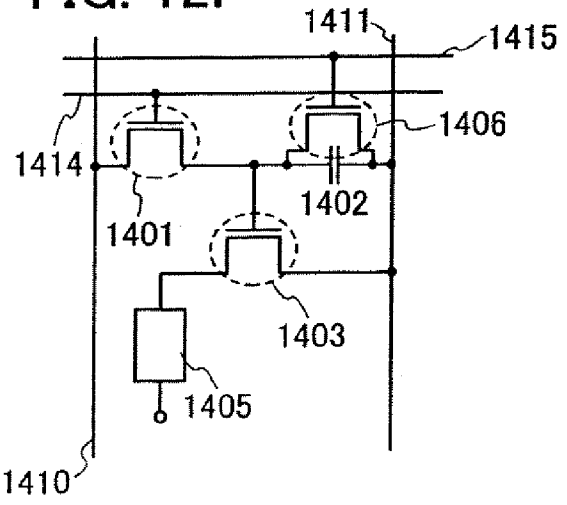

FIG. 13

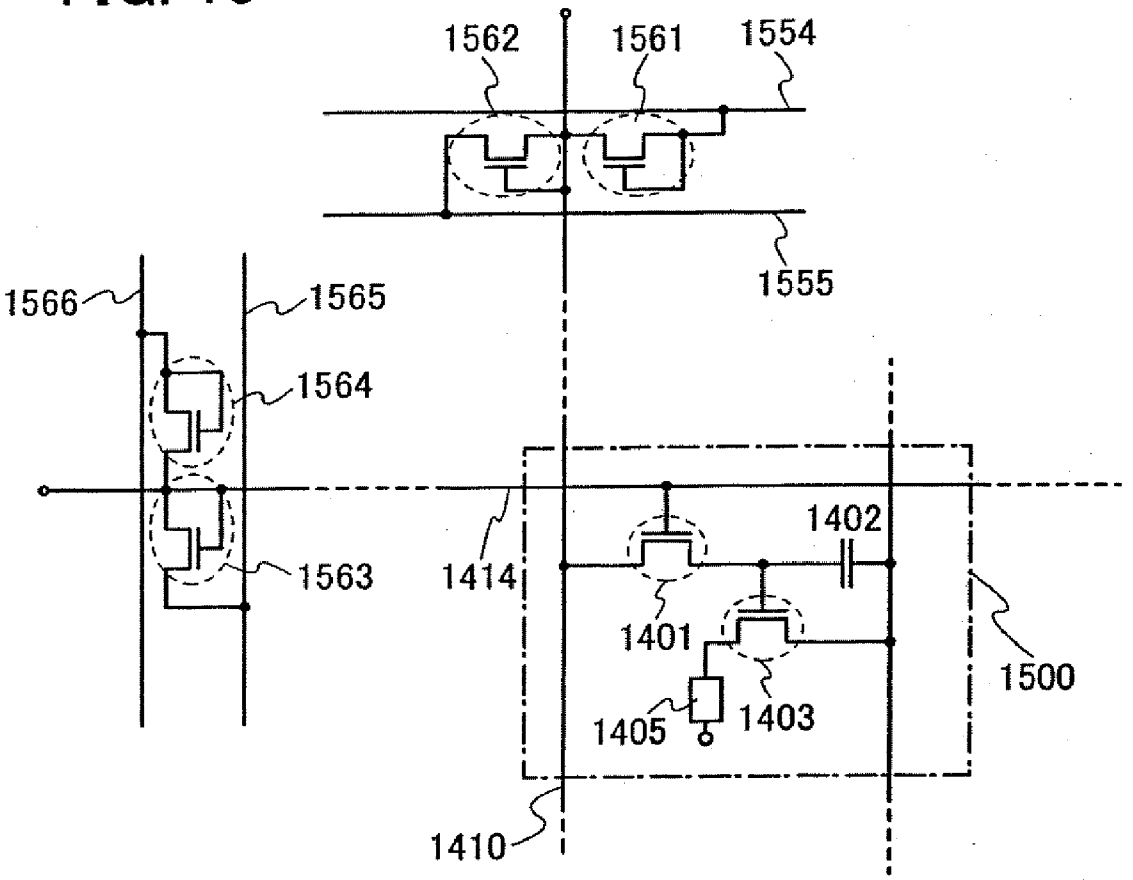
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FIG. 14A

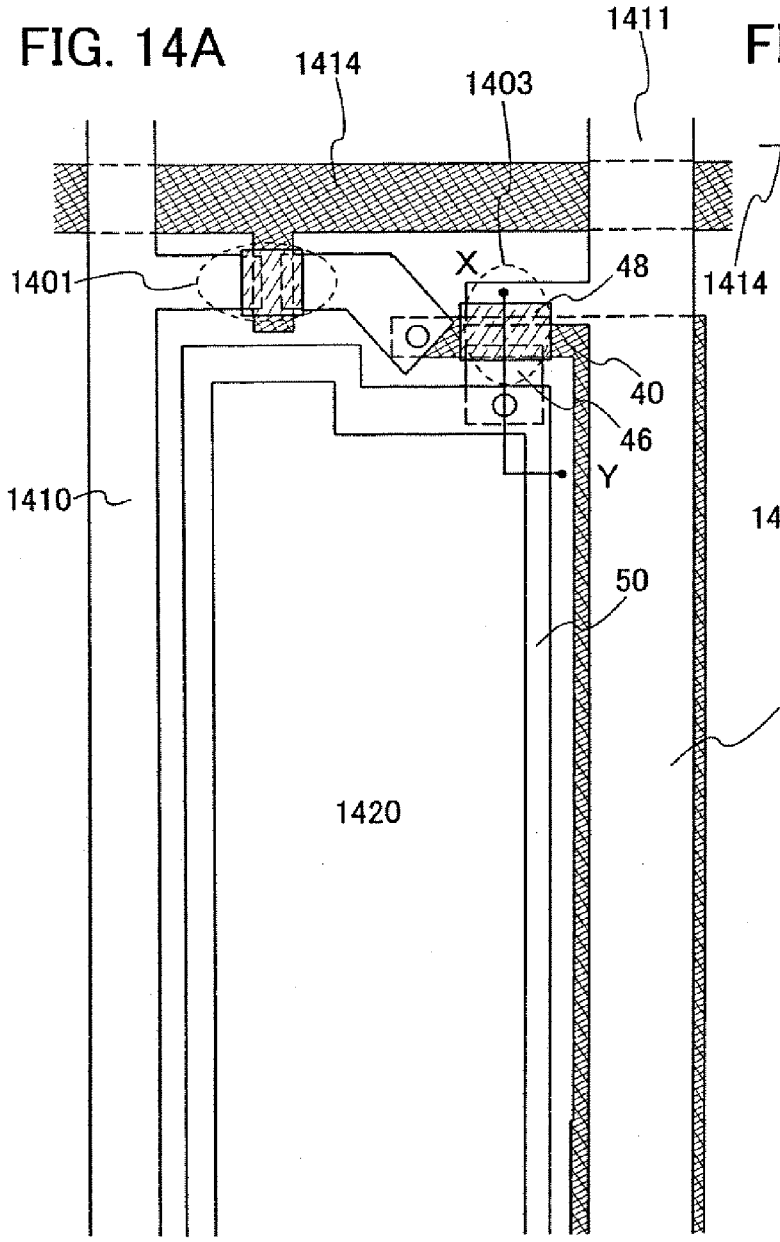


FIG. 14B

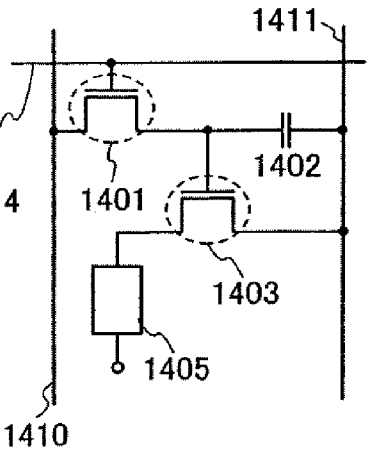


FIG. 15A

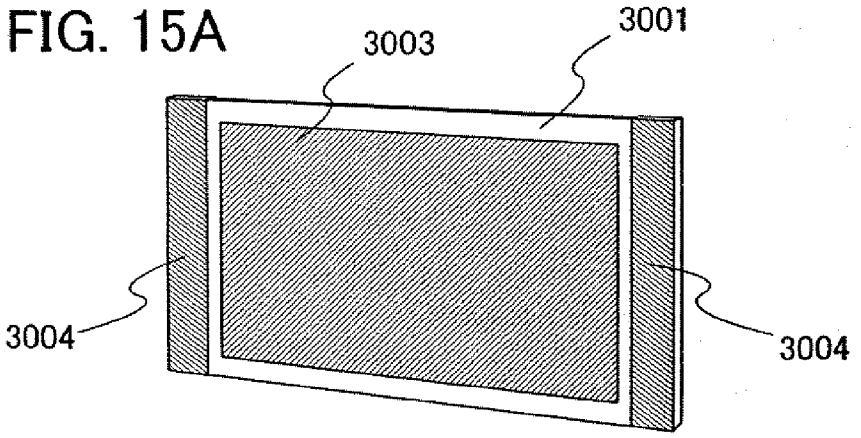


FIG. 15B

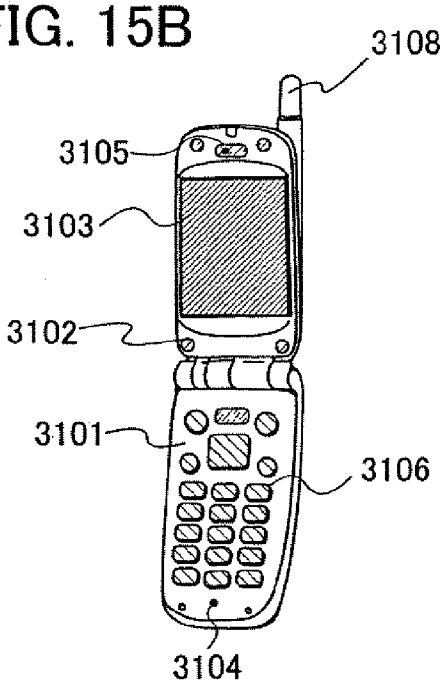


FIG. 15C

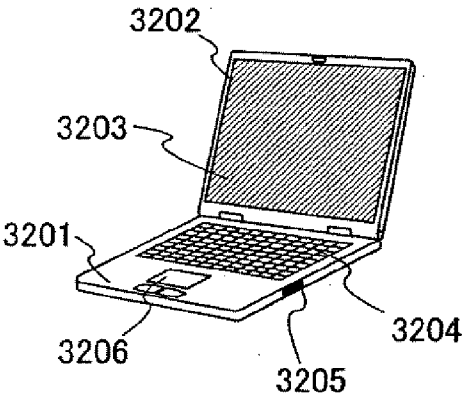


FIG. 15D

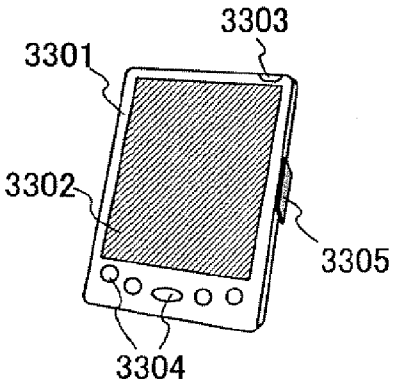


FIG. 15E

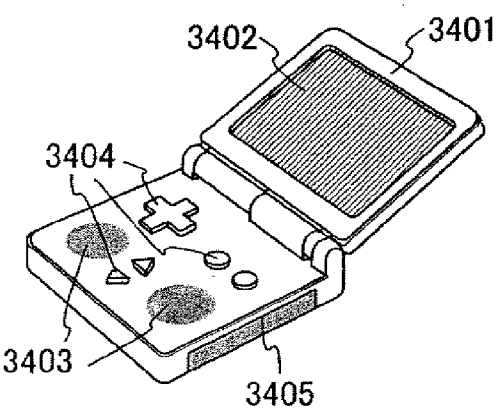
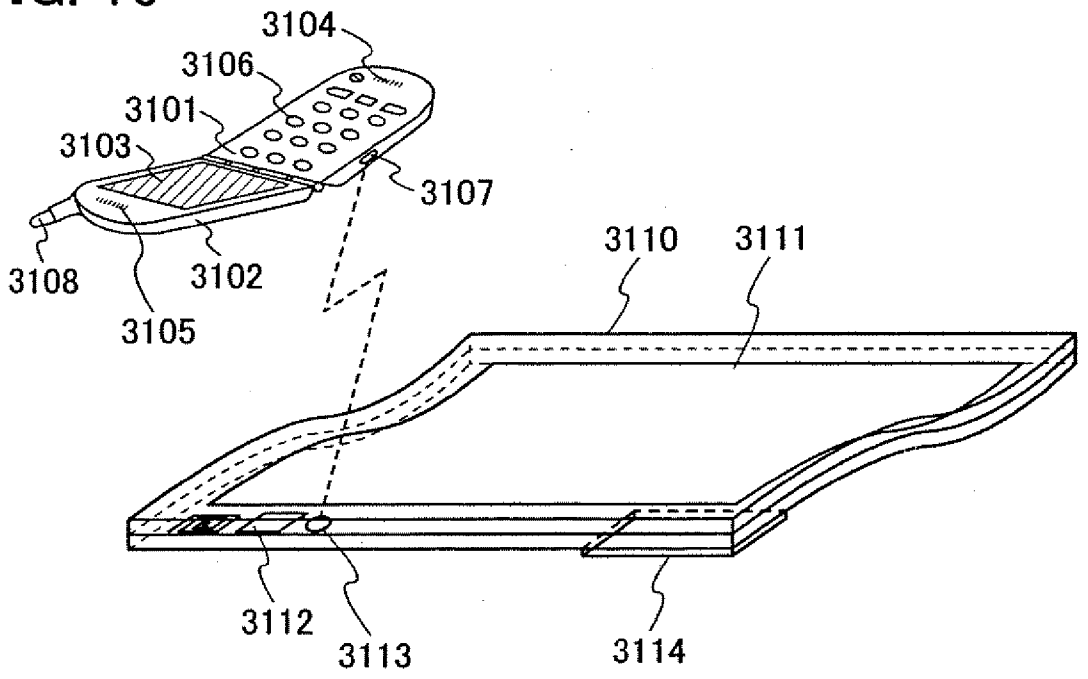


FIG. 16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SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device using ZnO (Zinc Oxide) and a manufacturing method thereof.

BACKGROUND ART

[0002] A semiconductor device used for a display panel of a liquid crystal display device or an EL (Electroluminescent) display device, for example, a semiconductor portion of a TFT (Thin Film Transistor), is generally formed by using a-Si (amorphous silicon) or poly-Si (polycrystalline silicon).

[0003] Si (silicon) does not have a large band gap (for example, single-crystalline Si is 1.1 eV), and absorbs visible light. By irradiation with the light, electrons and holes (carriers) are formed in Si. If a Si film is used for a channel formation region of a TFT, a carrier is generated in the channel formation region by irradiation with the light even in an OFF state. Then, current flows between a source region and a drain region. The current which flows in an OFF state is called "OFF-leak current". If the current value is high, a display panel does not operate normally. Consequently, a light shielding film is formed so as not to irradiate the Si film with light. However, a process becomes complex when the light shielding film is formed, because a deposition step, a photolithography step, and an etching step are required.

[0004] To solve the problem, an attention is paid to a transparent transistor using zinc oxide (ZnO) which is a semiconductor having a larger band gap of 3.4 eV than that of Si. Concerning such a transparent transistor, the band gap is larger than light energy in a visible light band and the visible light is not absorbed. Consequently, it has an advantage that the OFF-leak current does not increase if irradiated with light.

[0005] A semiconductor device using ZnO for the channel formation region is disclosed in Reference 1, for example. The structure of the semiconductor device using ZnO is described referring to FIG. **7**A.

[0006] A semiconductor device in FIG. **7**A has a source electrode **1001** and a drain electrode **1002**, a ZnO layer **1003** arranged so as to be contacted with the source electrode **1001** and the drain electrode **1002**, and a gate insulating layer **1004** stacked over the ZnO layer **1003** and a gate electrode **1005** over an insulating substrate **1000** such as a glass substrate.

[0007] For the source electrode **1001** and the drain electrode **1002**, a conductive ZnO is used. The conductive ZnO is doped with one of the following: B (boron), Al (aluminum), Ga (gallium), In (indium), or Tl (thallium), which are III group elements; F (fluorine), Cl (chlorine), Br (bromine), or I (iodine), which are VII group elements; Li (lithium), Na (sodium), K (potassium), Rb (rubidium), or Cs (caesium), which are I group elements; and N (nitrogen), P (phosphorus), As (arsenic), Sb (antimony), or Bi (bismuth), which are V group elements.

[Reference 1] Japanese Published Patent Application No. 2000-150900

DISCLOSURE OF INVENTION

[0008] According to the examination by the present inventor, it was revealed that the substrate **1000** is etched in some cases when the source electrode **1001** and the drain electrode **1002** of the top gate semiconductor device shown in FIG. **7**A is formed by etching. Even in the case of forming a base film **1006** formed by using a silicon oxide film or a silicon oxynitride film on the substrate **1000**, the surface of the substrate **1000** is exposed in some cases when the base film is etched. In addition, in the case of a bottom gate semiconductor device shown in FIG. **7**B, it is revealed that a gate insulating film **1004** formed by using a silicon oxide film or a silicon oxynitride film is etched when a source electrode **1001** and a drain electrode **1002** are formed by etching.

[0009] It the case of the top gate semiconductor device, when the glass substrate **1000** or the base film **1006** formed by using a silicon oxide film or a silicon oxynitride film is etched, an impurity such as sodium is diffused into a semiconductor film **1003** from the substrate **1000**, so that characteristics are deteriorated.

[0010] In the case of the bottom gate semiconductor device (FIG. **7**B), if the gate insulating film **1004** is etched when the source electrode **1001** and the drain electrode **1002** are formed by etching, the characteristics are not stable and causes a fault.

[0011] In consideration of the above situation, it is an object of the present invention to provide a semiconductor device in which a defect or a fault is not generated and a manufacturing method thereof even if a ZnO semiconductor film is used for the channel formation region, and a ZnO film to which an n-type or p-type impurity is added is used for the source electrode and the drain electrode.

[0012] An aspect of a semiconductor device of this invention has an Al film or an Al alloy film over a silicon oxide film or a silicon oxynitride film, and a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film. "A silicon oxide film", "a silicon oxynitride film", "an Al film", "an Al alloy film" and "a ZnO film" in this specification means a film containing silicon oxide, a film containing silicon oxynitride, a film containing Al, a film containing Al alloy, a film containing ZnO, respectively.

[0013] An aspect of a semiconductor device of this invention has a gate insulating film formed by using a silicon oxide film or a silicon oxynitride film over a gate electrode, an Al film or an Al alloy film over the gate insulating film, a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film, and a ZnO semiconductor film over the ZnO film to which an n-type or p-type impurity is added and the gate insulating film.

[0014] An aspect of a semiconductor device of this invention has an Al film or an Al alloy film over a silicon oxide film or a silicon oxynitride film, a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film, a ZnO semiconductor film over the silicon oxide film or the silicon oxynitride film and the ZnO film to which an n-type or p-type impurity is added, a gate insulating film over the ZnO semiconductor film, and a gate electrode over the gate insulating film.

[0015] An aspect of a manufacturing method of a semiconductor device of this invention has the steps of: forming a silicon oxide film or a silicon oxynitride film; forming an Al film or an Al alloy film over the silicon oxide film or the silicon oxynitride film; forming a ZnO film to which an n-type or p-type impurity is added over the Al film or the Al alloy film, wherein the ZnO film to which an n-type or p-type impurity is added is etched to have an island-like shape by a first etching, and the Al film or the Al alloy film is etched to have an island-like shape by a second etching.

[0016] An aspect of a manufacturing method of a semiconductor device of this invention, wherein a ZnO semiconductor film is formed over the ZnO film to which an n-type or p-type impurity is added, and the silicon oxide film or the silicon oxynitride film after the second etching.

[0017] In the case of the bottom gate semiconductor device, a gate insulating film formed by using the silicon oxide film or the silicon oxynitride film is formed over the gate electrode after forming a gate electrode.

[0018] In the case of the top gate semiconductor device, a gate insulating film is formed and a gate electrode is formed after the ZnO semiconductor film is formed.

[0019] A first etching of this invention may be wet etching.

[0020] A first etching of this invention may be wet etching using buffered fluoric acid.

[0021] A first etching of this invention may be dry etching.

[0022] A first etching of this invention may be dry etching using CH_4 (methane) gas

[0023] A second etching of this invention may be wet etching.

[0024] A second etching of this invention may be wet etching using developing solution for a photoresist.

[0025] A second etching of this invention may be wet etching using an organic alkaline solution.

[0026] A second etching of this invention may be wet etching using TMAH (tetramethylammonium hydroxide).

[0027] An aspect of a semiconductor device of this invention has a gate electrode, a gate insulating film over the gate electrode, a first film comprising metal material over the gate insulating film, a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the first film, and a third film comprising the transparent semiconductor material over the second film and the gate insulating film.

[0028] An aspect of a semiconductor device of this invention has an insulating film over a substrate, a first film comprising a metal material over the insulating film, a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the metal film, a third film comprising the transparent semiconductor material over the insulating film and the second film, a gate insulating film over the third film, and a gate electrode over the gate insulating film.

[0029] An aspect of a manufacturing method of a semiconductor device of this invention has the steps of: forming an insulating film over a substrate, forming a first film comprising a metal material over the insulating film, forming a second film comprising a transparent semiconductor material and an n-type or p-type impurity over the first film, etching the second film, and etching the first film.

[0030] An aspect of a manufacturing method of a semiconductor device of this invention has the steps of: forming a gate electrode over a substrate, forming a gate insulating film over the gate electrode, forming a first film comprising a metal material over the gate insulating film, forming a second film comprising a transparent semiconductor material and an n-type or p-type impurity over second film, etching the second film, and etching the first film.

[0031] In the top gate semiconductor device, a base film formed by using a glass substrate, a silicon oxide film or a silicon oxynitride film is not etched, and an impurity such as sodium is not diffused from a substrate into a semiconductor film so that its characteristics are not deteriorated.

[0032] In the bottom gate semiconductor device, the gate insulating film is not etched and its characteristics do not become unstable.

[0033] Since Al is used for a part of the source electrode and drain electrode, low resistance of a wire can be obtained.

BRIEF DESCRIPTION OF DRAWINGS

[0034] In the accompanying drawings:

[0035] FIGS. **1**A and **1**B show semiconductor devices of this invention;

[0036] FIGS. **2**A to **2**D show manufacturing steps of a semiconductor device of this invention;

[0037] FIGS. **3**A to **3**D show manufacturing steps of a semiconductor device of this invention;

[0038] FIGS. **4**A and **4**B show manufacturing steps of a semiconductor device of this invention;

[0039] FIGS. **5**A to **5**D show manufacturing steps of a semiconductor device of this invention;

[0040] FIGS. **6**A to **6**C show manufacturing steps of a semiconductor device of this invention;

[0041] FIGS. **7**A and **7**B show conventional examples;

[0042] FIGS. **8**A and **8**B show a manufacturing step of a liquid crystal display device;

[0043] FIGS. **9**A and **9**B show manufacturing steps of a liquid crystal display device;

[0044] FIGS. **10**A and **10**B show manufacturing steps of a light-emitting device;

[0045] FIGS. **11**A and **11**B show manufacturing steps of a light-emitting device;

[0046] FIGS. **12**A to **12**F each show an equivalent circuit of a light-emitting device;

[0047] FIG. **13** shows an equivalent circuit of a light-emitting device;

[0048] FIG. **14**A illustrates a top front view of a pixel portion and FIG. **14**B illustrates an equivalent circuit of a light-emitting device;

[0049] FIGS. **15**A to **15**E each show an example of an electronic apparatus to which this invention is applied; and

[0050] FIG. **16** shows an example of electronic apparatuses to which this invention is applied.

[0051] The embodiments of this invention will be described hereinafter referring to the accompanying drawings. Note that this invention is not limited to the description below, and it is easily understood by those skilled in the art that the embodiments and details herein disclosed can be modified in various ways without departing from the purpose and the scope of the invention. Therefore, this invention should not be interpreted as being limited to the description of the embodiments to be given below.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiment 1

[0052] Here, a bottom gate semiconductor device is described.

[0053] FIG. **1**A is a cross-sectional view in which one example of the embodiment of this invention is shown. In FIG. **1**A, numeral reference **1** denotes a substrate, **3** denotes a gate electrode, **5** denotes a gate insulating film, **10** denotes a source electrode, **10***a* denotes a first conductive film, **10***b* denotes a second conductive film, **11** denotes a drain electrode, **11***a* denotes a first conductive film, **11***b* denotes a second conductive film, and **13** denotes a semiconductor film.

An insulating film for passivation or planarization may be formed over the semiconductor film **13**.

[0054] The gate electrode **3** is formed over the substrate **1**, the gate insulating film **5** is formed over the gate electrode **3**, and the source electrode **10** and the drain electrode **11** are formed over the gate insulating film **5**. The source electrode **10** is formed of a layered film having the first conductive film **10***a* and the second conductive film **10***b*, and the drain electrode **11** is formed of a layered film having the first conductive film **11***a* and the second conductive film **11***b*. A third conductive film may be formed between the first conductive film **10***a* and the second conductive film **10***b*, or between the first conductive film **11***a* and the second conductive film **11***b*. The source electrode **10** and the drain electrode **11** may be each formed so as to overlap partially with the gate electrode **3** through the gate insulating film **5**. The semiconductor film **13** is formed over the source electrode **10** and the drain electrode **11** over the gate insulating film **5**.

[0055] Hereinafter, each structure is described.

[0056] (1) Substrate

[0057] The following can be used for forming a substrate: a substrate formed by using a glass substrate; an insulating material such as alumina; and a plastic substrate which can resist a processing temperature in post-steps; and the like. In the case of using a plastic substrate for the substrate **1**, the following can be used: PC (polycarbonate); PES (polyethersulfone); PET (polyethylene terephthalate); PEN (polyethylene naphthalate); or the like. In the case of the plastic substrate, an inorganic layer or an organic layer may be provided as a gas barrier layer over the surface. In the case where a prominence due to dust or the like which is generated on the substrate in the manufacturing process of the plastic substrate, the substrate may be used after polishing it with CMP or the like to make its surface planarized. An insulating film such as silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy) (X>Y), and silicon nitride oxide (SiNxOy) (X>Y) may be formed over the substrate **1** for preventing an impurity or the like from diffusing from the substrate side.

[0058] (2) Gate Electrode

[0059] A gate electrode can be formed by using an Al (aluminum) film, a W (tungsten) film, a Mo (molybdenum) film, a Ta (tantalum) film, a Cu (copper) film, a Ti (titanium) film, an alloy material containing the elements as a main component (for example, an Al alloy film, a MoW (molybdenum tungsten) alloy film), or the like. A semiconductor film represented by a polycrystalline silicon film doped with an impurity element such as P (phosphourus) may be used. The gate electrode **3** may be a single layer or a layered film in which two or more layers are stacked.

[0060] (3) Gate Insulating Film

[0061] The gate insulating film **5** is formed by using an insulating film containing silicon as a main component, for example, silicon oxide film, and silicon oxynitride film. In addition, it may be a single layer or a layered film.

[0062] (4) Source Electrode and Drain Electrode

[0063] The source electrode **10** is formed with a layered film of the first conductive film **10***a* and the second conductive film **10***b*, and the drain electrode **11** is formed with a layered film of the first conductive film **11***a* and the second conductive film **11***b*.

[0064] As the first conductive film, an Al film, an Al alloy film such as an AlNi (aluminum nickel) film, and an AlNd (neodymium aluminum) film can be used. As the second conductive film, ZnO (zinc oxide) to which a p-type or n-type impurity of B (boron), Al (aluminum), Ga (gallium), P (phosphorus), or As (arsenic) is added can be used. A metal film such as a Ti film may be provided as a third conductive film between the first conductive film and the second conductive film.

[0065] (5) Semiconductor Film

[0066] A ZnO film is used as a semiconductor film. Since the source electrode and the drain electrode contacted with the semiconductor film have the ZnO film to which a p-type or n-type impurity is added, they can be easily connected with the semiconductor film.

[0067] (6) Insulating Film

[0068] An insulating film such as a passivation film and a planarization film may be formed over the semiconductor film **13**, although not shown. Silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy) (x>y), silicon nitride oxide (SiNxOy) (x>y), a SOG (spin-on-glass) film, or an organic resin film of acryl, or a layered film of those can be used.

[0069] In the bottom gate semiconductor device, a gate insulating film is not etched in manufacturing process, and characteristics do not become unstable. Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

Embodiment 2

[0070] Here, a top gate semiconductor device is described.

[0071] FIG. **1**B is a cross-sectional view showing one example of an embodiment of this invention. In FIG. **1**B, numeral reference **1** denotes a substrate, **20** denotes an insulating film, **25** denotes a source electrode, **25***a* denotes a first conductive film, **25***b* denotes a second conductive film, **26** denotes a drain electrode, **26***a* denotes a first conductive film, **26***b* denotes a second conductive film, **27** denotes a semiconductor film, **28** denotes a gate insulating film, and **29** denotes a gate electrode. An insulating film for passivation or planarization may be formed over the gate electrode.

[0072] The insulating film **20** is formed on the substrate **1**, and the source electrode **25** and the drain electrode **26** are formed over the insulating film **20**. The source electrode **25** is formed with a layered film of the first conductive film **25***a* and the second conductive film **25***b*, and the drain electrode **26** is formed with a layered film of the first conductive film **26***a* and the second conductive film **26***b*. A third conductive film may be formed between the first conductive film **25***a* and the second conductive film **25***b*, or between the first conductive film **26***a* and the second conductive film **26***b*. The semiconductor film **27** is formed over the source electrode **25** and the drain electrode **26** over the insulating film **20**, the gate insulating film **28** is formed over the semiconductor film **27**, and the gate electrode **29** is formed over the gate insulating film **28**. The gate electrode **29** may be formed so as to partially overlap with the source electrode and the drain electrode with the gate insulating film **28** and the semiconductor film **27** interposed therebetween.

[0073] Here, each structure is described.

[0074] For the substrate, the source electrode, the drain electrode, the semiconductor film, and the gate electrode, the same ones described in Embodiment 1 can be used.

[0075] (1) Insulating Film Over Substrate

[0076] An silicon oxide film or a silicon oxynitride film is formed as the insulating film **20** for preventing an impurity or

the like from diffusing from the substrate side over the substrate **1**. In addition, it may be a single layer or a layered film.

[0077] (2) Gate Insulating Film

[0078] The gate insulating film **28** is formed by using an insulating film containing silicon as a main component, for example, a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, and a silicon nitride film. In addition, it may be a single layer or a layered film.

[0079] (3) Insulating Film Over Gate Electrode

[0080] An interlayer insulating film such as a passivation film and a planarization film may be formed over the gate electrode **29**, although not shown. A SiO_x film, a SiNx film, a SiON film, SiNO film, an SOG (spin-on-glass) film, and an organic resin film of acrylic or a layered film of those can be used.

[0081] In the top gate semiconductor device, the substrate or the base film formed by using a silicon oxide film or a silicon oxynitride film is not etched, so that an impurity such as sodium is not diffused into the semiconductor film from the substrate and the characteristics are not deteriorated. Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

Embodiment 3

[0082] A manufacturing method of the bottom gate semiconductor device is described, in which a silicon oxide film or a silicon oxynitride film is formed as a gate insulating film over the gate electrode, an Al film or an Al alloy film is formed as a first conductive film, and a ZnO film to which an n-type or p-type impurity is added is formed as a second conductive film, and then, the second conductive film is etched to have an island-like shape by a first etching and the first conductive film is etched to have an island-like shape by a second etching to form source and drain electrodes, and a ZnO semiconductor film is formed.

[0083] As shown in FIG. **2**A, a gate electrode **3** is formed. The thickness of the gate electrode may be 10 to 200 nm over a substrate **1**. The substrate **1** may be formed by using the material shown in Embodiment 1. Here, a glass substrate is used.

[0084] An insulating film **2** containing silicon oxide (SiOx), silicon nitride (SiNx), silicon oxynitride (SiOxNy) (x>y), silicon nitride oxide (SiNxOy) (x>y), or the like may be formed with a thickness of 10 to 200 nm by CVD or sputtering so as to prevent impurity or the like from diffusing from the substrate side (FIG. **2**B).

[0085] The insulating film **2** may be formed by processing the surface of the substrate **1** with high density plasma. For example, the high density plasma can be generated using a microwave of 2.45 GHz, and it is only required that electron density ranges from 1×10^{11} to $1\times10^{13}/cm^3$, and electron temperature is 2 eV or less. Such high density plasma has a low kinetic energy of active species and a film with fewer defects can be formed with less damage caused by plasma compared to a conventional plasma treatment.

[0086] The surface of the substrate **1** can be nitrided by the high density plasma treatment under a nitriding atmosphere such as an atmosphere containing nitrogen and a noble gas, an atmosphere containing nitrogen, hydrogen and a noble gas, and an atmosphere containing ammonia and a noble gas. In the case where a glass substrate is used as the substrate **1** subjected to a nitriding treatment by the high density plasma, as a nitride film formed over the surface of the substrate **1**, the insulating film **2** containing silicon nitride as a main component can be formed. The insulating film **2** may be formed by using a plurality of layers in which a silicon oxide film or a silicon oxynitride film is formed by plasma CVD over the nitride film.

[0087] In addition, a nitride film can be formed by nitriding over the surface of the insulating film **2** with high density plasma similarly.

[0088] The nitride film formed by nitriding with high density plasma can suppress diffusion of impurity from the substrate **1**.

[0089] The gate electrode **3** can be formed by using materials shown in Embodiment 1. Here, an AlNd (aluminum neodymium) film is formed by sputtering using an AlNd target and processed into an island-like shape. A photolithography method is used for processing the film into an island-like shape, and dry etching or wet etching is used.

[0090] After cleaning the surface of the gate electrode **3** and the surface of the substrate **1** or the insulating film **2**, a gate insulating film **5** is formed with a thickness of 10 to 200 nm using a known CVD or sputtering over the gate electrode **3** (FIGS. **2**A and **2**B). The surface cleaning step and the formation step of the gate insulating film **5** may be carried out continuously without being exposed to air. In the case where an Al film is used for the gate electrode **3**, when the gate insulating film **5** is formed at a high temperature, a hillock is generated in some cases. Thus, it is preferable to form the film at a low temperature of 500° C. or less, preferably 350° C. or less.

[0091] The gate insulating film **5** can be formed by using the material shown in Embodiment 1. Here, a silicon oxide film is formed. Note that the insulating film **2** is omitted in the drawings below.

[0092] A first conductive film **6** for source and drain electrodes is formed with a thickness of 10 to 200 nm on the gate insulating film **5**. The first conductive film **6** can be formed by using the material shown in Embodiment 1. Here, an AlNi (aluminum nickel) film or an AlNd film is used. The first conductive film **6** can be formed by sputtering using an AlNi target or an AlNd target. After forming the gate insulating film **5**, the first conductive film **6** may be formed continuously without being exposed to the air.

[0093] A second conductive film **7** is formed with a thickness of 10 to 200 nm on the first conductive film **6** (FIG. **2**C). The second conductive film **7** can be formed by using the material shown in Embodiment 1. Here, ZnO (zinc oxide) to which an impurity such as Al or Ga is added is used. Consequently, an ohmic contact can be easily created between the second conductive film **7** and a ZnO film which is formed as a semiconductor layer later. The second conductive film **7** can be formed by sputtering. For example, the following methods can be used for adding Al or Ga: sputtering using a ZnO target to which 1 to 10 weight % of Al or Ga is added; or sputtering in which an Al or Ga chip is mounted on a ZnO target at 200 to 300° C.

[0094] After forming the first conductive film **6**, the second conductive film **7** may be formed continuously without being exposed to the air. Therefore, formation from the gate insulating film **5** to the second conductive film **7** may be continuously carried out without being exposed to air.

[0095] A third conductive film **8** may be formed with a thickness of 10 to 200 nm between the first conductive film **6** and the second conductive film **7** (FIG. **2**D). A contact resistance is occasionally increased between the first conductive film **6** and the second conductive film **7** depending on a heat

treatment temperature in a manufacturing process. However, the contact resistance can be reduced between the first conductive film **6** and the second conductive film **7** by forming the third conductive film **8**. The third conductive film **8** can be formed by using a metal film such as a Ti film which is formed by sputtering or the like.

[0096] A resist mask **9** is formed over the second conductive film **7**, and the second conductive film **7** is etched (FIGS. **3**A and **3**B). In the case of using wet etching, buffered fluoric acid (in which HF (hydrofluoric acid) and NH_4F (ammonium fluoride) are mixed), for example, solution with a ratio of $HF:NH_4F$ (weight ratio)=1:100 to 1:10 is used.

[0097] In the case of using dry etching, anisotropic plasma etching using CH_4 gas can be used.

[0098] Under the second conductive film **7**, the first conductive film **6** is formed. Thus, the first conductive film **6** serves as an etching stopper when the second conductive film **7** is etched. Consequently, source and drain electrodes can be formed without damaging the gate insulating film **5** in etching.

[0099] A part of the first conductive film **6** may be etched when the second conductive film **7** is etched. However, attention is required to be paid so as not to totally etch the first conductive film **6** because the gate insulating film is damaged if the first conductive film **6** is totally etched.

[0100] Next, a source electrode **10** and a drain electrode **11** are formed by etching the first conductive film **6** using the resist mask **9** (FIG. **3**C). In this invention, the first conductive film **6** is etched using an organic alkaline solution represented by TMAH (tetramethylammonium hydroxide), which is a developer for a photoresist.

[0101] In the case of using an AlNi film for the first conductive film **6** and TMAH for etching solution, the etching ratio is approximately 300 nm/min at 30° C. On the other hand, the second conductive film **7** or the gate insulating film **5** to which the above-mentioned material is used is not etched with TMAH. Consequently, the source electrode **10** and the drain electrode **11** can be formed without damaging the gate insulating film **5**. Further, the island-like shaped second conductive films **10***b* and **11***b* are not reduced in size. In this invention, the first conductive film **6** can be etched using a developer which is used when a resist mask is formed without using a special etching solution. Consequently, cost is reduced and efficiency is increased.

[0102] The resist mask **9** is removed after forming the source electrode **10** and the drain electrode **11**.

[0103] A ZnO film is formed as a semiconductor film **12** with a thickness of 20 to 200 nm by sputtering over the source electrode **10**, the drain electrode **11**, and the gate insulating film **5** (FIG. **3**D). For example, the film can be formed by sputtering using a ZnO target with a flow ratio of oxygen/argon ranging from 30 to 20, at 200 to 300° C.

[0104] The semiconductor film **12** is etched by a photolithography method to form an island-like shaped semiconductor film **13** (FIG. **4**A). A wet etching method using a buffered fluoric acid or anisotropic dry etching method using CH_4 gas can be used.

[0105] Zno is commonly used in the semiconductor film **12** and the second conductive films **10***b* and **11***b*, and it is difficult to obtain a sufficient etching selectivity. However, since the second conductive film **7** is required to be formed in a portion in contact with the semiconductor film **12**, the second conductive film **7** may be etched in a portion out of contact with the semiconductor film **12**, for example, a wire portion. In the above-mentioned etching method, the second conductive films **10***b* and **11***b* may be etched, but the first conductive films **10***a* and **11***a* are not etched. Consequently, the first conductive films **10***a* and **11***a* serve as wires, and the electrical connection with the semiconductor device is ensured.

[0106] An insulating film **14** is formed with a thickness of 50 nm to 1 μm over a semiconductor film **13** by CVD or sputtering (FIG. **4**B). An insulating film containing silicon as a main component can be formed as the insulating film **14**. An organic resin film or the like may be stacked over the insulating film containing silicon. The insulating film **14** functions as a planarization film or a passivation film. Since Al is included in the source electrode **10** and the drain electrode **11**, a hillock is occasionally generated when the insulating film **14** is formed at high temperature. Thus, it is preferably formed at low temperature, 500° C. or less, preferably 350° C. or less.

[0107] Contact holes are formed in the insulating film **14**, and conductive films in contact with the gate electrode **3**, the source electrode **10**, and the drain electrode **11** are provided if necessary.

[0108] According to this invention, a semiconductor device can be formed without damaging the gate insulating film. An Al alloy film such as an AlNi film is used as the first conductive film, thereby achieving lower resistance of the wire.

Embodiment 4

[0109] Here, a manufacturing method of a top gate semiconductor device is described, in which an Al film or an Al alloy film is formed as a first conductive film on a silicon oxide film or a silicon oxynitride film, and a ZnO film to which an n-type or p-type impurity is added is formed as a second conductive film, and then, the second conductive film is formed to have an island-like shape by a first etching, the first conductive film is formed to have an island-like shape by a second etching to form source and drain electrodes, a ZnO semiconductor film is formed, a gate insulating film is formed, and a gate electrode is formed. Note that it is needless to say that materials and methods for manufacture described in Embodiments 1 to 3 can be applied to those used for the present embodiment.

[0110] As shown in FIG. **5**A, a silicon oxide (SiOx) film is formed as an insulating film **20** over a substrate **1** with a thickness of 10 to 200 nm by CVD or sputtering. The insulating film **20** prevents impurity or the like from diffusing from the substrate **1** side.

[0111] A first conductive film **21** for the source and drain electrodes is formed with a thickness of 10 to 200 nm by sputtering or evaporation over the insulating film **20**. An Al alloy film such as AlNi (aluminum nickel) film which is shown in Embodiment 1 can be used as the first conductive film **21**. After forming the insulating film **20**, the first conductive film **21** may be formed continuously without being exposed to the air.

[0112] A second conductive film **22** is formed with a thickness of 10 to 200 nm by sputtering on the first conductive film **21** (FIG. **5**A). As the second conductive film **22**, ZnO (zinc oxide) to which a p-type or n-type impurity such as B (boron), Al (aluminum), Ga (gallium), P (phosphourus), or As (arsenic) is added can be used. After forming the first conductive film **21**, the second conductive film **22** may be formed continuously without being exposed to the air. Therefore, the

steps of forming the insulating film **20** to the second conductive film **22** may be carried out continuously without being exposed to the air.

[0113] A metal film such as a Ti film may be formed as a third conductive film **23** with a thickness of 10 to 200 nm by sputtering between the first conductive film **21** and the second conductive film **22** in order to reduce the contact resistance between the first conductive film **21** and the second conductive film **22** (FIG. **5**B).

[0114] A resist mask **24** is formed over the second conductive film **22**, and the second conductive film **22** is etched (FIG. **5**C). Wet etching using buffered fluoric acid or dry etching using CH_4 gas can be used as an etching method.

[0115] The first conductive film **21** is formed under the second conductive film **22**. Therefore, the first conductive film **21** serves as an etching stopper when the second conductive film **22** is etched. Thus, the source and drain electrodes can be formed without exposing the substrate **1** by etching the insulating film **20**.

[0116] When the second conductive film **22** is etched, a part of the first conductive film **21** may be etched. Note that if all of the first conductive film **21** is etched, the insulating film **20** is etched and the substrate **1** is exposed, which would cause diffusion of impurity included in the substrate **1**.

[0117] The first conductive film **21** is etched to form the source electrode **25** and the drain electrode **26** (FIG. **5**D). Wet etching using a developer for a photoresist, TMAH is used as an etching method. Thus, the source electrode **25** and the drain electrode **26** can be formed without etching the insulating film **20**. Further, the sizes of the island-like shaped second conductive films **25***b* and **26***b* are not reduced because the ZnO film is not etched by TMAH. Etching can be performed with a developer which is used in formation of a resist mask without a special etching solution for the first conductive film **21**, which leads to cost reduction and improvement in efficiency.

[0118] After forming the source electrode **25** and the drain electrode **26**, the resist mask **24** is removed.

[0119] A ZnO film is formed with a thickness of 20 to 200 nm by sputtering as the semiconductor film **27** over the source electrode **25**, the drain electrode **26**, and the insulating film **20** (FIG. **6**A).

[0120] The semiconductor film **27** is etched by a photolithography method to make an island-like shaped semiconductor film **27**. Wet etching using buffered fluoric acid or dry etching using CH_4 gas can be used as an etching method.

[0121] ZnO is commonly used for the semiconductor film **27** and the second conductive films **25***b* and **26***b*, and it is difficult to obtain a high etching selectivity. However, the second conductive film may be etched in the portion out of contact with the semiconductor film **27**, specially the wire portion, because the second conductive film **22** may be formed in the source and drain electrode portions, which is the same as Embodiment 3.

[0122] A gate insulating film **28** is formed with a thickness of 10 to 200 nm by CVD or sputtering over the semiconductor film **27** (FIG. **6**B). The semiconductor film **27** may be subjected to a high density plasma treatment shown in the above-mentioned Embodiment to form a gate insulating film. The surface of the semiconductor film **27** can be nitrided by the high density plasma treatment under a nitriding atmosphere such as an atmosphere containing nitrogen and a noble gas; an atmosphere containing nitrogen, hydrogen, and a noble gas; and an atmosphere containing ammonia and a noble gas.

[0123] The gate insulating film **28** may be formed by using an insulating film containing silicon as a main component, for example, a silicon oxide film, a silicon oxynitride film, a silicon nitride film, and a silicon nitride oxide film. In addition, it may be a single layer or a layered film.

[0124] A gate electrode **29** is formed over the gate insulating film **28** (FIG. **6**B). The gate electrode **29** can be formed by using the material shown in the above-mentioned embodiment, and may be a single layer or a layered film including two or more layers. A known CVD sputtering, evaporation, or the like can be employed as a method for film formation. Dry etching or wet etching method can be used for processing the gate electrode **29** into an island-like shape with a photolithography method.

[0125] An insulating film **30** is formed with a thickness of 50 nm to 1 μm by CVD or sputtering over the gate electrode **29** and the gate insulating film **28** (FIG. **6**C). The insulating film **30** can be formed by using an insulating film containing silicon. An organic resin film or the like may be stacked over the insulating film containing silicon. The insulating film **30** functions as a planarization film or a passivation film. Since Al is included in the source electrode **25** and the drain electrode **26**, a hillock is occasionally generated when the gate insulating film **28**, the gate electrode **29**, and the insulating film **30** are formed at a high temperature. Thus, they are preferably formed at a low temperature, at 500° C. or less, preferably 350° C. or less.

[0126] As described above, this invention can prevent an impurity from diffusing due to an exposure of the substrate **1**. An Al alloy film such as an AlNi film is used as the first conductive film, thereby achieving lower resistance of a wire.

Embodiment 5

[0127] Here, a description is made of a method of manufacturing a liquid crystal display device using a bottom gate semiconductor device which is shown in Embodiments 1 and 3 referring to FIGS. **8**A and **8**B and **9**A and **9**B. Note that it is needless to say that the top gate semiconductor device which is shown in Embodiments 2 and 4 can be applied. FIGS. **8**A and **9**A show cross-sectional views taken along line X-Y in FIG. **8**B.

[0128] A gate wire **40** and an auxiliary capacitor wire **41** are formed over a glass substrate or a plastic substrate **1**. An AlNd film is formed by sputtering, and then, formed by known photolithography method and etching.

[0129] A gate insulating film **42** formed by using a silicon oxide film or a silicon oxynitride film is formed by CVD or sputtering.

[0130] An AlNi film is formed as a first conductive film by sputtering over the gate insulating film **42**. The first conductive film forms a source electrode **45***a*, a drain electrode **46***a* and a source wire **47** later.

[0131] A ZnO (zinc oxide) film to which Al is added is formed as a second conductive film by sputtering over the first conductive film. The second conductive film forms a source electrode **45***b*, a drain electrode **46***b*, and a source wire **47** later.

[0132] A resist mask is formed in a region which is to be a source electrode portion, a drain electrode portion, and a source wire portion, over the second conductive film (not shown in the figure). Then, the second conductive film is etched. Here, etching is performed using buffered fluoric acid and a solution of $HF:NH_4F=1:100$ (weight ratio).

[0133] Next, the first conductive film is etched using TMAH solution to form the source electrode **45***a*, the drain electrode **46***a*, and the source wire **47**. After that, the resist mask is removed. Then, the source electrode **45**, the drain electrode **46**, and the source wire **47** can be formed without damaging the gate insulating film **42**. In addition, since the ZnO film is not etched by TMAH, the size of the island-like shaped second conductive film is not reduced. Further, since an AlNi film is used for the first conductive film, the resistance of the source wire can be reduced.

[0134] Next, a semiconductor film **48** is formed. A ZnO film is formed by sputtering, and then, the semiconductor film **48** is formed from the ZnO film by a photolithography method and etching. Wet etching using buffered fluoric acid is used as etching. The portion of the second conductive film out of contact with the semiconductor film **48** may be partially removed here, because the first conductive film is formed in a portion to be a wire.

[0135] An insulating film **49** is formed by CVD, sputtering, coating, or the like over the semiconductor film **48**. The insulating film **49** can be formed by using a layered film having an insulating film containing silicon, an organic resin film, or the like. The insulating film **49** may be a film which makes the unevenness of the surface planarized.

[0136] A contact hole leading to the drain electrode **46** and a contact hole for the auxiliary capacitor are formed in the insulating film **49** using a photolithography method and an etching method.

[0137] A transparent conductive film is formed by sputtering, and then, a pixel electrode **50** is formed using a photolithography method and etching. For example, ITO (Indium Tin Oxide), ITSO (Indium Tin Oxide containing silicon oxide), or IZO (Indium Zinc Oxide) may be used.

[0138] In the case of a reflective liquid crystal display device, a light reflective metal material such as Ag (silver), Au (gold), Cu (copper), W (tungsten), or Al (aluminum) is formed instead of a transparent electrode.

[0139] The portion where the pixel electrode **50** and the auxiliary capacitor wire **41** are overlapped forms an auxiliary capacitor **100** which is formed of the pixel electrode **50**, the gate insulating film **42**, and the auxiliary capacitor wire **41** (FIGS. **8**A and **8**B).

[0140] A corner of a bent portion or a portion where width changes may be smoothed and rounded in a wire and an electrode. A shape of a chamfered corner can be realized by using a photomask pattern manufactured using a pattern of photomask. This will have advantages described below. When dry etching using plasma is performed, generation of fine particles due to abnormal discharge can be suppressed by chamfering a projecting portion. Even though the fine particles are generated, the fine particles can be prevented from accumulating at the corner at the time of cleaning, and the fine particles can be washed away by chamfering a concave portion. Thus, a problem of fine particles or dust in the manufacturing process can be solved and the yield can be improved.

[0141] An alignment film **51** is formed so as to cover the pixel electrode **50**. The alignment film is formed by a droplet discharge method, printing, or the like. After forming the alignment film, rubbing is conducted.

[0142] A color filter **55** is formed by using a colored layer and a light-shielding layer (black matrix), and a protective insulating film **54** is formed on an opposing substrate **56**. A transparent electrode **57** is formed, and an alignment film **53** is formed on the protective insulating film **54** (FIG. **9**A). The alignment film is subjected to a rubbing process.

[0143] Next, a closed pattern **75** of a sealant is formed by a droplet discharge method (FIG. **9**B). A region surrounded by the sealant is filled with liquid crystal composition **52** (FIG. **9**A).

[0144] After dropping the liquid crystal composition **52** in the closed pattern **75**, the opposing substrate **56** and a substrate **1** in which a semiconductor device is formed are attached to each other. When the liquid crystal composition **52** is filled, the following alternative may be adopted: a seal pattern having an opening portion is provided on the substrate **1**; the opposing substrate **56** and the substrate **1** are attached to each other; then, liquid crystal is injected using capillary action.

[0145] As an alignment mode of the liquid crystal composition **52**, TN mode in which the alignment of liquid crystal molecules is twisted at 90° from the side of light incidence to the side of light emission, FLC mode, IPS mode, or the like can be used. Note that an electrode pattern is different from one shown in FIG. **8**B and is a comb-like shape in the case of the IPS mode.

[0146] Polarizing plates are attached to both of the opposing substrate **56** and the substrate **1** on which the semiconductor device is formed. In addition, an optical film can be attached if required.

[0147] The distance between the opposing substrate **56** and the substrate **1** on which the semiconductor device is formed may be kept by dispersing spherical spacers or forming a columnar spacer formed of a resin, or by mixing fillers in the sealant. The aforementioned columnar spacer is formed of an organic resin material containing at least one of acrylic, polyimide, polyimide amide, or epoxy as a main component, or an inorganic material having one of silicon oxide, silicon nitride and silicon oxide containing nitrogen, or a layered film thereof.

[0148] Then, an FPC (Flexible Printed Circuit) is attached to the substrate **1** with an anisotropic conductive layer interposed therebetween using a known technique.

[0149] A peripheral driver circuit may be formed over the substrate. A plane exemplary diagram is shown in FIG. **9**B.

[0150] A gate wire driver circuit **62**, a source wire driver circuit **63**, and an active matrix portion **64** are formed over a substrate **61** formed of glass or the like. The gate wire driver circuit **62** is constituted from at least a shift register **62***a* and a buffer **62***b*. The source wire driver circuit **63** is constituted from at least a shift register **63***a*, a buffer **63***b*, and an analog switch **69** which samples video signals transmitted via video lines **68**. A plurality of gate wires **72** extended from the gate wire driver circuit **62** is arranged in parallel with each other in the active matrix portion **64**. A plurality of source wires **71** extended from the source wire driver circuit **63** is arranged orthogonally to the gate wires **72**. In addition, an auxiliary capacitor wire **73** is arranged in parallel with the gate wires **72**. In addition, a semiconductor device **65**, a liquid crystal portion **66**, and an auxiliary capacitor **67** are provided in a region surrounded by the gate wire **72**, the source wires **71**, and the auxiliary capacitor wire **73**.

[0151] The gate wire driver circuit **62**, the source wire driver circuit **63**, and the analog switch **69** are provided with a semiconductor device manufactured by the same manufacturing method as the semiconductor device **65** to have a similar structure.

[0152] In the semiconductor device **65**, a gate electrode is connected to the gate wire **72**, and the source electrode is connected to the source wire **71**. A liquid crystal portion **66** is formed by introducing a liquid crystal to be sealed between a pixel electrode connected to the drain electrode of the semiconductor device **65** and an opposing electrode over the opposing substrate. The auxiliary capacitor wire **73** is connected to an electrode having the same potential as the opposing electrode.

[0153] In the aforementioned liquid crystal display device, the gate insulating film is not etched and the characteristics do not become unstable, and thus, high reliability is realized. In the case of using a top gate semiconductor device, a glass substrate or a base film formed by using, a silicon oxide film or a silicon oxynitride film is not etched, so that impurity such as sodium is not diffused into a semiconductor film from the substrate and the characteristics are not deteriorated, and thus, high reliability can be realized.

[0154] Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

Embodiment 6

[0155] Here, a description is made of a method for manufacturing a light-emitting device with using the bottom gate semiconductor device shown in Embodiments 1 and 3 referring to FIGS. **10**A and **10**B and **11**A and **11**B. Note that it is needless to say that the semiconductor device of Embodiments 2 and 4 can be applied.

[0156] The semiconductor device is manufactured based on the description of the aforementioned embodiment, and formation to the stage shown in FIG. **10**A is carried out. Note that the same parts as those of the above embodiments are denoted by the same reference numerals.

[0157] In the EL display device, the pixel electrode **50** functions as an anode or a cathode. As the material for the pixel electrode **50**, the following can be employed: a conductive metal such as aluminum (Al), silver (Ag), gold (Au), platinum (Pt), nickel (Ni), tungsten (W), chromium (Cr), molybdenum (Mo), iron (Fe), cobalt (Co), copper (Cu), palladium (Pd), lithium (Li), caesium (Cs), magnesium (Mg), calcium (Ca), strontium (Sr), or titanium (Ti); an alloy such as aluminum-silicon (Al—Si), aluminum-titanium (Al—Ti), or aluminum-silicon-copper (Al—Si—Cu); nitride of a metal material such as titanium nitride (TiN); a metal compound such as ITO, ITO containing silicon, or IZO.

[0158] An electrode from which light emitted from an EL layer is extracted is only required to be formed by using a light-transmitting conductive film, and a very thin film of metal such as Al or Ag may be used as well as a metal compound such as ITO, ITO containing silicon, or IZO.

[0159] When light-emission is extracted from an electrode which is opposed to the pixel electrode **50**, a highly reflective material (Al, Ag, or the like) can be used for the pixel electrode **50**. In this embodiment, ITSO, which means ITO containing silicon, is used as the pixel electrode **50** (FIG. **10**A).

[0160] Next, an insulating film formed by using an organic material or an inorganic material is formed so as to cover the insulating film **49** and the pixel electrode **50**. Then, the insulating film is processed to expose the pixel electrode **50** partially, thereby forming partition walls **81**. As the material of the partition walls **81**, a photosensitive organic material (such as acrylic or polyimide) is preferable. Alternatively, a non-photosensitive organic material or inorganic material may also be used. Further, the partition walls **81** may be used as a black matrix by coloring the partition walls **81** black in such a way that a black pigment or dye such as titanium black or carbon nitride is dispersed into the material of the partition wall **81** with the use of a dispersant. It is desirable that the partitions wall **81** have a tapered shape and those end surfaces **81***a* toward the pixel electrode have curvatures changing continuously (FIG. **10**B).

[0161] Next, a layer **82** including a light-emitting substance is formed, and an opposing electrode **83** which covers the layer **82** including a light-emitting substance is formed. Then, a light-emitting element with the layer **82** including a light-emitting substance interposed between the pixel electrode **50** and the opposing electrode **83** can be manufactured, and light-emission can be obtained by applying a voltage between the opposing electrode **83** and the pixel electrode **50**.

[0162] As an electrode material used for forming the opposing electrode **83**, a material similar to one which can be used for the pixel electrode can be used. In this embodiment, aluminum is used for a second electrode.

[0163] The layer **82** including a light-emitting substance is formed by evaporation, ink-jet, spin coating, dip coating, roll-to-roll method, sputtering, or the like.

[0164] In the case of an organic electroluminescent display device, the layer **82** including a light-emitting substance may be a layered film of layers having functions of hole transportation, hole injection, electron transportation, electron injection, or light-emission, respectively, or a single layer of a light-emitting layer. As a layer including a light-emitting substance, a single layer or a layered film of an organic compound may be used.

[0165] A hole injecting layer is provided between an anode and a hole transporting layer. As the hole injecting layer, a mixed layer of an organic compound and a metal oxide can be used. This prevents short circuit between the pixel electrode **50** and the opposing electrode **83** due to unevenness which is formed on the surface of the pixel electrode **50** or a foreign substance which is left on the surface of the electrode. The thickness of the mixed layer is preferably 60 nm or more, more preferably 120 nm or more. Since increase in thickness of a film does not cause increase in driving voltage, the thickness of the film can be selected such that the influence of the unevenness or foreign substance can be covered sufficiently. Thus, a dark spot is not generated, and driving voltage or power consumption is not increased in the light-emitting device manufactured by this invention.

[0166] An oxide or a nitride of transition metal is preferable as a metal oxide, concretely, zirconium oxide, hafnium oxide, vanadium oxide, niobium oxide, tantalum oxide, chromium oxide, molybdenum oxide, tungsten oxide, titanium oxide, manganese oxide, and rhenium oxide.

[0167] As an organic compound, the following can be employed: an organic material having an arylamino group such as 4,4'-bis[N-(1-napthyl)-N-phenylamino]biphenyl (NPB), 4,4'-bis[N-(3-methylphenyl]-N-phenylamino]biphenyl (TPD), 4,4',4"-tris(N,N-diphenylamino)triphenylamine (TDATA), 4,4',4"-tris[N-(3-methylphenyl)-N-phenylamino] triphenylamine (MTDATA), 4,4'-bis{N-[4-(N,N-di-m-tolylamino)phenyl]-N-phenylamino}biphenyl (DNTPD), 1,3,5-tris[N,N-di(m-tolyl)amino]benzene (m-MTDAB), and 4,4',4"-tris(N-carbazolyl) triphenylamine (TCTA); phthalocyanine (H_2Pc); copper phthalocyanine (CuPc); vanadyl phthalocyanine (VOPc); or the like.

[0168] The hole transporting layer is provided between the anode and a light-emitting layer, or between the hole injecting

layer and the light-emitting layer when the hole injecting layer is provided. The hole transporting layer is formed by using a layer which has an excellent property of transporting a hole, for example, a layer formed by using a compound of aromatic amine (that is, having a benzene ring-nitrogen bond) such as NPB, TPD, TDATA, MTDATA, and BSPB. The substances mentioned here have the hole mobility of 1×10^{-6} to 10 cm^2/Vs mainly. Note that a substance having higher transporting property of holes than electrons may be used as well as the materials. Note that the hole transporting layer may be formed by not only a single layer but also a layered film in which two or more layers formed from the above mentioned substances are stacked.

[0169] The light-emitting layer is provided between the anode and the cathode, or between the hole transporting layer and the electron transporting layer when the hole transporting layer and the electron transporting layer are provided. There is no particular limitation on the light-emitting layer; however, a layer serving as the light-emitting layer has two modes roughly. One is a host-guest type layer which includes a dispersed light-emitting substance in a layer formed of a material (host material) having a larger energy gap than an energy gap of a light-emitting substance (dopant material) which becomes a luminescent center, while the other is a layer in which a light-emitting layer is made of a light-emitting substance only. The former is preferable, because concentration quenching hardly occurs. As the light-emitting substance to be a luminescent center, the following can be employed: 4-dicyanomethylene-2-methyl-6-(1,1,7,7-tetramethyljulolidyl-9-enyl)-4H-pyran (DCJT); 4-dicyanomethylene-2-t-butyl-6-(1,1,7,7-tetramethyljulolidine-9-enyl)-4H-pyran; periflanthene; 2,5-dicyano-1,4-bis(10-methoxy-1,1,7,7-tetramethyljulolidine-9-enyl)benzene; N,N'-dimethylquinacridone (DMQd); coumarin 6; coumarin 545T; tris(8-quinolinolato)aluminum (Alq_3); 9,9'-bianthryl; 9,10-diphenylanthracene (DPA); 9,10-bis(2-naphthyl)anthracene (DNA); 2,5,8,11-tetra-t-butylperylene (TBP); PtOEP; $Ir(ppy)_3$; $Btp_2Ir(acac)$; FIrpic; or the like. As the base material to be a host material in the case of forming the layer in which the light-emitting substance is diffused, the following can be used: an anthracene derivative such as 9,10-di(2-naphtyl)-2-tert-butylanthracene (t-BuDNA); a carbazole derivative such as 4,4'-bis(N-carbazolyl)biphenyl (CBP); or a metal complex such as tris(8-quinolinolato)aluminum (Alq_3), tris(4-methyl-8-quinolinolato)aluminum ($Almq_3$); bis(10-hydroxybenzo[h]-quinolinato)beryllium ($BeBq_2$); bis(2-methyl-8-quinolinolato)-4-phenylphenolato-aluminum (BAlq); bis[2-(2-hydroxyphenyl)pyridinato]zinc ($Znpp_2$); or bis[2-(2-hydroxyphenyl)benzoxazolate]zinc (ZnBOX). As the material which can constitute the light-emitting layer only with a light-emitting substance, tris(8-quinolinolato)aluminum (Alq_3), 9,10-bis(2-naphtyl)anthracene (DNA), bis(2-methyl-8-quinolinolato)-4-phenylphenolato-aluminum (BAlq), or the like can be used.

[0170] An electron transporting layer is provided between the light-emitting layer and the cathode, or between the light-emitting layer and an electron injecting layer when the electron injecting layer is provided. The electron transporting layer is a layer having an excellent electron transporting property, and for example, a layer formed using a metal complex having a quinoline skeleton or a benzoquinoline skeleton such as tris(8-quinolinolato)aluminum (Alq_3), tris(5-methyl-8-quinolinolato)aluminum ($Almq_3$), bis(10-hydroxybenzo[h]-quinolinato)beryllium ($BeBq_2$), and bis(2-methyl-8-quinolinolato)-4-phenylphenolato-aluminum (BAlq). In addition, a metal complex having an oxazole ligand or a thiazole ligand such as bis[2-(2-hydroxyphenyl)-benzoxazolato]zinc ($Zn(BOX)_2$), bis[2-(2-hydroxyphenyl)-benzothiazolato]zinc ($Zn(BTZ)_2$), or the like can be used. In addition to the metal complexes, 2-(4-biphenylyl)-5-(4-tert-butylphenyl)-1,3,4-oxadiazole (PBD); 1,3-bis[5-(p-tert-butylphenyl)-1,3,4-oxadiazole-2-yl]benzene (OXD-7); 3-(4-tert-butylphenyl)-4-phenyl-5-(4-biphenylyl)-1,2,4-triazole (TAZ); 3-(4-tert-butylphenyl)-4-(4-ethylphenyl)-5-(4-biphenylyl)-1,2,4-triazole (p-EtTAZ); bathophenanthroline (BPhen); bathocuproine (BCP); or the like can be used. These substances mentioned here mainly have the electron mobility of 1×10^{-6} to 10 cm^2/Vs. Note that other substance may be used for the electron transporting layer so long as it has a higher electron transporting property than a hole transporting property. Further, the electron transporting layer may be formed by not only a single layer but also a layered film in which two or more layers made from the above mentioned substances are stacked.

[0171] The electron injecting layer is provided between the cathode and the electron transporting layer. As the electron injecting layer, a compound of alkali metal or alkaline earth metal such as lithium fluoride (LiF), cesium fluoride (CsF), or calcium fluoride (CaF_2) can be employed. In addition to that, a layer formed by using an electron transporting substance which contains alkali metal or alkaline earth metal, for example, Alq_3 containing magnesium (Mg) or the like can be used.

[0172] In the case of an inorganic electroluminescent display device, one in which a fluorescent substance particles are diffused in dispersing agent for the layer **82** including a light-emitting substance can be used.

[0173] A fluorescent substance in which a donor impurity such as Cl (chlorine), I (iodine), or Al (aluminum) is added with Cu (copper) in ZnS can be used.

[0174] As the dispersing agent, the following can be employed: a polymer having a relatively high dielectric constant such as cyanoethyl cellulose based resin, polyethylene based resin, polypropylene based resin, polystyrene based resin, silicone resin, epoxy resin, vinylidene fluoride resin, or the like. The dielectric constant can be adjusted by mixing the resin and minute particles having high dielectric constant such as $BaTiO_3$ (barium titanate) or $SrTiO_3$ (strontium titanate). As a diffusing means, an ultrasonic diffusing machine or the like can be used.

[0175] A dielectric layer may be provided between the layer **82** including a light-emitting substance and one of the electrodes. For the dielectric layer, a highly dielectric and insulating material which has a high dielectric breakdown voltage is employed. One is selected from a metal oxide or nitride, for example, TiO_2, $BaTiO_3$, $SrTiO_3$ $PbTiO_3$, $KNbO_3$, $PbNbO_3$, Ta_2O_3, $BaTa_2O_6$, $LiTaO_3$, Y_2O_3, Al_2O_3, ZrO_2, AlON, ZnS, or the like. Those may be disposed as a uniform film or a film having a particle structure.

[0176] In the case of an inorganic electroluminescent display device, a double-insulating structure in which a light-emitting layer is interposed between insulating layers may be employed. The light-emitting layer can be formed by using a II-VI compound such as Mn (manganese) or ZnO (zinc sulfide) containing a rare earth element, and the insulating layer can be formed by using oxide or nitride such as Si_3N_4, SiO_2, Al_2O_3, or TiO_2.

[0177] A silicon oxide film containing nitrogen is formed as a passivation film over the opposing electrode **83** by plasma CVD (not shown). In the case of using a silicon oxide film containing nitrogen, the following can be used: a silicon oxynitride film formed by using SiH_4, N_2O, and NH_3 by plasma CVD; a silicon oxynitride film formed by using SiH_4, and N_2O; or a silicon oxynitride film formed by using a gas in which SiH_4 and N_2O is diluted with Ar.

[0178] A silicon oxide nitride hydride film manufactured from SiH_4, N_2O, and H_2 may be employed as a passivation film. Note that a passivation film is not limited to the aforementioned substance. Another insulating film containing silicon as a main component can be also used. In addition, a layered film structure may be employed as well as a single layer structure. Further, a multilayer film of a carbon nitride film and a silicon nitride film or a multilayer film of a styrene polymer can be used. A silicon nitride film or a diamond-like carbon film may be formed.

[0179] Then, a display portion is sealed to protect a light-emitting element from a material such as water which promotes deterioration. In the case of using an opposing substrate for sealing, the opposing substrate is attached by using an insulating sealant so as to expose an external connection portion. A space between the opposing substrate and an element substrate may be filled with an inert gas such as dry nitrogen, or the opposing substrate may be attached by applying a sealant to the pixel portion entirely. It is preferable to use an ultraviolet curing resin or the like as the sealant. A drying agent or particles for keeping the gap between the substrates constant may be mixed in the sealant. Then, the light-emitting device is completed by attaching a flexible wire board to the external connection portion.

[0180] One example of a structure of the light-emitting device manufactured as described above is shown referring to FIGS. **11**A and **11**B. Note that portions having the same functions are sometimes denoted by the same reference numerals even though they have different shapes, and the explanations are occasionally omitted.

[0181] FIG. **11**A shows a structure in which the pixel electrode **50** is formed using a light transmitting conductive film, and light generated in the layer **82** including a light-emitting substance is emitted toward a substrate **1**. Further, reference numeral **86** denotes an opposing substrate. This opposing substrate is firmly attached to the substrate **1** using a sealant or the like after forming a light emitting element. A space between the opposing substrate **86** and the element is filled with resin **85** having a light-transmitting property or the like to seal the light emitting element. Accordingly, the light emitting element can be prevented from being deteriorated by moisture or the like. Preferably, the resin **85** has a hygroscopic property. More preferably, a drying agent **84** with a high light-transmitting property is dispersed in the resin **85** to prevent the adverse influence of moisture.

[0182] FIG. **11**B shows a structure in which both the pixel electrode **50** and an opposing substrate **83** are formed by using conductive films having light-transmitting property. Accordingly, light can be emitted toward both the substrate **1** and the opposing substrate **86** as shown by an arrow of dotted lines. In this structure, by providing polarizing plates **88** outside of the substrate **1** and the opposing substrate **86**, a screen can be prevented from being transparent, thereby improving visibility. Protection films **87** are preferably provided outside of the polarizing plates **88**.

[0183] The light-emitting device of this invention having a display function may employ either an analog video signal or a digital video signal. If a digital video signal is used, the video signal may use either a voltage or a current.

[0184] When the light-emitting element emits light, a video signal to be inputted to a pixel may have either a constant voltage or a constant current. When a video signal has a constant voltage, a constant voltage is applied to a light-emitting element or a constant current flows through the light-emitting element.

[0185] Also, when a video signal has a constant current, a constant voltage is applied to a light-emitting element or a constant current flows through the light-emitting element. A driving method where a constant voltage is applied to a light-emitting element is called a constant voltage drive. Meanwhile, a driving method where a constant current flows through a light-emitting element is called a constant current drive. In the constant current drive, constant current flows regardless of change in resistance of a light emitting element. The light emitting display device according to this invention and the driving method thereof may use any one of the aforementioned methods.

[0186] In the light-emitting device, a gate insulating film is not etched, and the characteristics of the light-emitting element is not unstable so that its reliability is high. In the case of using a top gate semiconductor device, since a glass substrate or a base film formed by using, a silicon oxide film or a silicon oxynitride film is not etched, impurity such as sodium which deteriorates characteristics is not diffused from the substrate into the semiconductor film so that high reliability is obtained.

[0187] Al is used for a part of the source electrode and the drain electrode, thereby achieving lower resistance of a wire.

[0188] A pixel circuit and a protective circuit included in a panel and module, and operation thereof are shown referring to FIGS. **12**A to **12**F and **13** or the like. FIGS. **10**A and **10**B and **11**A and **11**B each show a cross-sectional view of a driving TFT **1403** of the semiconductor device. A switching TFT **1401**, a current control TFT **1404**, and an eraser TFT **1406** may be manufactured at the same time of the driving TFT **1403**, and may have the same structure as the driving TFT **1403**.

[0189] A pixel shown in FIG. **12**A includes a signal line **1410** and power source lines **1411** and **1412** arranged in a column direction and a scan line **1414** arranged in a row direction. The pixel further includes a switching TFT **1401**, the driving TFT **1403**, the current control TFT **1404**, an auxiliary capacitor **1402**, and a light-emitting element **1405**.

[0190] A pixel shown in FIG. **12**C has the same structure as one in FIG. **12**A except for that the gate electrode of the driving TFT **1403** is connected to the power source line **1412** provided in the row direction. In other words, the pixels shown in FIGS. **12**A and **12**C have the same equivalent circuit diagram. However, a power source line formed in the case of arranging the power source line **1412** in the column direction (FIG. **12**A) is formed by using a conductive layer in a different layer from a layer in which a power source line is formed by using a conductive layer in the case of arranging the power source line **1412** in the row direction (FIG. **12**C). Here, attention is paid to a wire connected to the gate electrode of the driving TFT **1403**, and the structure is shown separately in FIGS. **12**A and **12**C in order to show that these wires are manufactured with different layers.

[0191] As a feature of the pixels shown in FIGS. **12**A and **12**C, the driving TFT **1403** and the current control TFT **1404** are connected serially within the pixel, and it is preferable to set the channel length L (**1403**) and the channel width W (**1403**) of the driving TFT **1403**, and the channel length L (**1404**) and the channel width W (**1404**) of the current control TFT **1404** so as to satisfy L (**1403**)/W (**1403**):L (**1404**)/W (**1404**)=5 to 6000:1.

[0192] The driving TFT **1403** operates in a saturation region and serves to control the current value of the current flowing into the light-emitting element **1405**. The current control TFT **1404** operates in a linear region and serves to control the current supplied to the light-emitting element **1405**. Both the TFTs preferably have the same conductivity type in the manufacturing process, and the TFTs are n-channel type TFTs in this embodiment. The driving TFT **1403** may be either an enhancement mode TFT or a depletion mode TFT. Since the current control TFT **1404** operates in the linear region in the light-emitting device having the above structure, slight fluctuation of Vgs of the current control TFT **1404** does not affect the current value of the light-emitting element **1405**. That is to say, the current value of the light-emitting element **1405** can be determined by the driving TFT **1403** operating in the saturation region. With the above structure, the variation of the luminance of the light-emitting element due to the variation of the characteristics of the TFT can be remedied, thereby providing a light-emitting device having improved image quality.

[0193] In each pixel shown in FIGS. **12**A to **12**D, the switching TFT **1401** is to control the input of the video signal to the pixel, and the video signal is inputted into the pixel when the switching TFT **1401** is turned on. Then, the voltage of the video signal is held in the auxiliary capacitor **1402**. Although FIGS. **12**A and **12**C show the structure in which the auxiliary capacitor **1402** is provided, this invention is not limited thereto. When the gate capacitance and the like can serve as a capacitor holding the video signal, the auxiliary capacitor **1402** is not necessarily provided.

[0194] A pixel shown in FIG. **12**B has the same pixel structure as that in FIG. **12**A except for that a TFT **1406** and a scan line **1415** are added. In the same way, a pixel shown in FIG. **12**D has the same pixel structure as that in FIG. **12**C expect for that the TFT **1406** and the scan line **1415** are added.

[0195] ON and OFF of the TFT **1406** is controlled by the additionally provided scan line **1415**. When the TFT **1406** is turned on, the charge held in the auxiliary capacitor **1402** is discharged, thereby turning off the current control TFT **1404**. In other words, by the provision of the TFT **1406**, a state can be produced compellingly in which the current does not flow into the light-emitting element **1405**. For this reason, the TFT **1406** can be referred to as an eraser TFT. Consequently, in the structures shown in FIGS. **12**B and **12**D, a lighting period can be started at the same time as or just after the start of a writing period before the writing of the signal into all the pixels; therefore the duty ratio can be increased.

[0196] In a pixel shown in FIG. **12**E, the signal line **1410** and the power source line **1411** are arranged in the column direction, and the scan line **1414** is arranged in the row direction. Further, the pixel includes the switching TFT **1401**, the driving TFT **1403**, the auxiliary capacitor **1402**, and the light-emitting element **1405**. A pixel shown in FIG. **12**F has the same pixel structure as that shown in FIG. **12**E except for that the TFT **1406** and the scan line **1415** are added. In the structure shown in FIG. **12**F, the duty ratio can also be increased by the provision of the TFT **1406**.

[0197] Such an active matrix light-emitting device can be driven at low voltage when the pixel density increases, because the TFTs are provided in respective pixels. Therefore, it is considered that the active matrix light-emitting device is advantageous.

[0198] Although this embodiment described the active matrix light-emitting device in which the respective TFTs are provided in respective pixels, a passive matrix light-emitting device can also be formed. Since the TFTs are not provided in respective pixels in the passive matrix light-emitting device, high aperture ratio can be obtained. In the case of a light-emitting device in which light is emitted to both sides of the light emission stack, the transmissivity of the passive matrix light-emitting device is increased.

[0199] Subsequently, a case will be described in which a diode is provided as a protective circuit on the scan line and the signal line with the use of an equivalent circuit shown in FIG. **12**E.

[0200] In FIG. **13**, the switching TFT **1401**, the driving TFT **1403**, the auxiliary capacitor **1402**, and the light-emitting element **1405** are provided in a pixel area **1500**. Diodes **1561** and **1562** are provided on the signal line **1410**. In the similar way to the switching TFT **1401** and the driving TFT **1403**, the diodes **1561** and **1562** are manufactured based on the above embodiments, and have a gate electrode, a semiconductor layer, a source electrode, a drain electrode, and the like. The diodes **1561** and **1562** are operated as diodes by connecting the gate electrode with the drain electrode or the source electrode.

[0201] Common potential lines **1554** and **1555** connecting to the diodes **1561** and **1562** are formed by using the same layer as the gate electrode. Therefore, in order to connect the common potential lines **1554** and **1555** with the source electrode or the drain electrode of the diode, it is necessary to form a contact hole in the gate insulating layer.

[0202] Diodes **1563** and **1564** provided on the scan line **1414** have a similar structure. Further, common potential lines **1565** and **1566** has the similar structure.

[0203] In this manner, protection diodes can be simultaneously formed in an input stage according to this invention. Further, the positions of the protection diodes are not limited to this, and they can be provided between a driver circuit and a pixel.

[0204] A top view of a pixel portion in the case of using an equivalent circuit shown in FIG. **12**E is described in FIG. **14**A. In addition, the same equivalent circuit as that in FIG. **12**E is shown in FIG. **14**B. Each semiconductor device shown in FIGS. **10**A, **10**B, **11**A, and **11**B is corresponds to each driving TFT **1403**. FIGS. **10**A, **10**B, **11**A and **11**B show cross-sectional views taken along line X-Y in FIGS. **14**A and **14**B. The power source line **1411**, the signal line **1410**, and the source electrode and the drain electrode of the switching TFT **1401** are formed by using the first conductive film, and the source electrode and the drain electrode of the driving TFT **1403** are formed by using the second conductive film.

[0205] The switching TFT **1401** is manufactured by the same method as the driving TFT **1403**. The drain electrode of the switching TFT **1401** and a gate electrode **40** of the driving TFT **1403** are connected electrically with each other through a contact hole formed in an insulating film in the same layer as the gate insulating film **42**.

[0206] The auxiliary capacitor **1402** is formed by using a portion where the gate electrode of the driving TFT **1403** is extended, the power source line **1411**, and an insulating film in the same layer as the gate insulating film **42**.

[0207] A light-emitting region **1420** is formed in an opening portion of a partition wall **81**. The partition wall **81** is formed in the vicinity of the light-emitting region **1420**, although it is not shown. The corner portion of the light-emitting region **1420** may be rounded. By making the corner portion of the opening portion of the partition wall **81** rounded, the corner portion of the light-emitting region **1420** can be rounded. When dry etching using plasma is performed to process the partition wall **81**, generation of fine particles due to abnormal discharge can be suppressed by making the corner portion rounded.

[0208] This embodiment can be combined with a suitable structure of the above embodiments as appropriate.

Embodiment 7

[0209] As an electronic device having semiconductor devices according to this invention mounted with modules shown as examples in the above embodiments, a camera such as a video camera or a digital camera; a goggle type display (a head mounted display); a navigation system; an audio reproducing device (e.g., a car audio component); a computer; a game machine; a portable information terminal (e.g., a mobile computer, a cellular phone, a portable game machine, an electronic book, or the like); an image reproducing device equipped with a recording medium (specifically, a device which can reproduce the content of a recording medium such as a digital versatile disc (DVD) and which has a display for displaying an image stored therein); and the like can be given. Specific examples of these electronic appliances are shown in FIGS. **15**A to **15**E, and FIG. **16**.

[0210] FIG. **15**A shows a monitor for a television receiver or a personal computer, or the like, including a housing **3001**, a display area **3003**, speakers **3004**, and the like. An active matrix display device is provided in the display area **3003**. Each pixel of the display area **3003** includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a television with less characteristic deterioration can be obtained.

[0211] FIG. **15**B shows a cellular phone, including a main body **3101**, a housing **3102**, a display area **3103**, an audio input portion **3104**, an audio output portion **3105**, operation keys **3106**, an antenna **3108**, and the like. An active matrix display device is provided in the display area **3103**. Each pixel of the display area **3103** includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a cellular phone with less characteristic deterioration can be obtained.

[0212] FIG. **15**C shows a computer, including a main body **3201**, a housing **3202**, a display area **3203**, a keyboard **3204**, an external connection port **3205**, a pointing mouse **3206**, and the like. An active matrix display device is provided in the display area **3203**. Each pixel of the display area **3203** includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a computer with less characteristic deterioration can be obtained.

[0213] FIG. **15**D shows a mobile computer, including a main body **3301**, a display area **3302**, a switch **3303**, operation keys **3304**, an infrared port **3305**, and the like. An active matrix display device is provided in the display area **3302**. Each pixel of the display area **3302** includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a mobile computer with less characteristic deterioration can be obtained.

[0214] FIG. **15**E shows a portable game machine, including a housing **3401**, a display area **3402**, speakers **3403**, operation keys **3404**, a recording medium insert portion **3405**, and the like. An active matrix display device is provided in the display area **3402**. Each pixel of the display area **3402** includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a portable game machine with less characteristic deterioration can be obtained.

[0215] FIG. **16** shows a flexible display, including a main body **3110**, a pixel area **3111**, a driver IC **3112**, a receiving device **3113**, a film buttery **3114**, and the like. The receiving device can receive a signal from an infrared communication port **3107** of the above described cellular phone. An active matrix display device is provided in the pixel area **3111**. Each pixel of the pixel area **3111** includes a semiconductor device manufactured in accordance with this invention. By using the semiconductor device of this invention with this structure, a flexible display with less characteristic deterioration can be obtained.

[0216] As set forth above, the application range of this invention is extremely wide, and this invention can be applied to electronic devices in all fields.

[0217] The present application is based on Japanese Patent Application serial No. 2005-329806 filed on Nov. 15, 2005 in Japanese Patent Office, the entire contents of which are hereby incorporated by reference.

What is claimed is:

1. A method of manufacturing a semiconductor device including a channel formation region and a gate insulating film adjacent to the channel formation region, the method comprising:

forming the gate insulating film by using a microwave,

wherein the channel formation region comprises an oxide semiconductor material.

2. The method according to claim **1** wherein the microwave has a frequency of 2.45 GHz.

3. The method according to claim **1** wherein the semiconductor device is a top gate semiconductor device in which the gate insulating film is formed over the channel formation region.

4. The method according to claim **1** wherein the gate insulating film comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, and silicon nitride oxide.

5. The method according to claim **1** wherein the oxide semiconductor material includes zinc oxide.

6. A method of manufacturing a semiconductor device including a channel formation region and a gate insulating film adjacent to the channel formation region, the method comprising:

forming the gate insulating film by using a plasma having an electron density from 1×10^{11} to $1\times10^{13}/cm^3$,

wherein the channel formation region comprises an oxide semiconductor material.

7. The method according to claim 6 wherein the semiconductor device is a top gate semiconductor device in which the gate insulating film is formed over the channel formation region.

8. The method according to claim 6 wherein the gate insulating film comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, and silicon nitride oxide.

9. The method according to claim 6 wherein the oxide semiconductor material includes zinc oxide.

10. A method of manufacturing a semiconductor device including a channel formation region and a gate insulating film adjacent to the channel formation region, the method comprising:

forming the gate insulating film by using a plasma having an electron temperature 2 eV or less,

wherein the channel formation region comprises an oxide semiconductor material.

11. The method according to claim 10 wherein the semiconductor device is a top gate semiconductor device in which the gate insulating film is formed over the channel formation region.

12. The method according to claim 10 wherein the gate insulating film comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, and silicon nitride oxide.

13. The method according to claim 10 wherein the oxide semiconductor material includes zinc oxide.

14. A method of manufacturing a semiconductor device including a channel formation region and a gate insulating film adjacent to the channel formation region, the method comprising:

forming the gate insulating film by using a plasma generated by using a microwave, the plasma having an electron density from 1×10^{11} to $1\times10^{13}/cm^3$,

wherein the channel formation region comprises an oxide semiconductor material.

15. The method according to claim 10 wherein the semiconductor device is a top gate semiconductor device in which the gate insulating film is formed over the channel formation region.

16. The method according to claim 10 wherein the gate insulating film comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, and silicon nitride oxide.

17. The method according to claim 10 wherein the oxide semiconductor material includes zinc oxide.

18. A method of manufacturing a semiconductor device including a channel formation region and a gate insulating film adjacent to the channel formation region, the method comprising:

forming the gate insulating film by using a plasma generated by using a microwave, the plasma having an electron temperature 2 eV or less,

wherein the channel formation region comprises an oxide semiconductor material.

19. The method according to claim 18 wherein the semiconductor device is a top gate semiconductor device in which the gate insulating film is formed over the channel formation region.

20. The method according to claim 18 wherein the gate insulating film comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, and silicon nitride oxide.

21. The method according to claim 18 wherein the oxide semiconductor material includes zinc oxide.

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