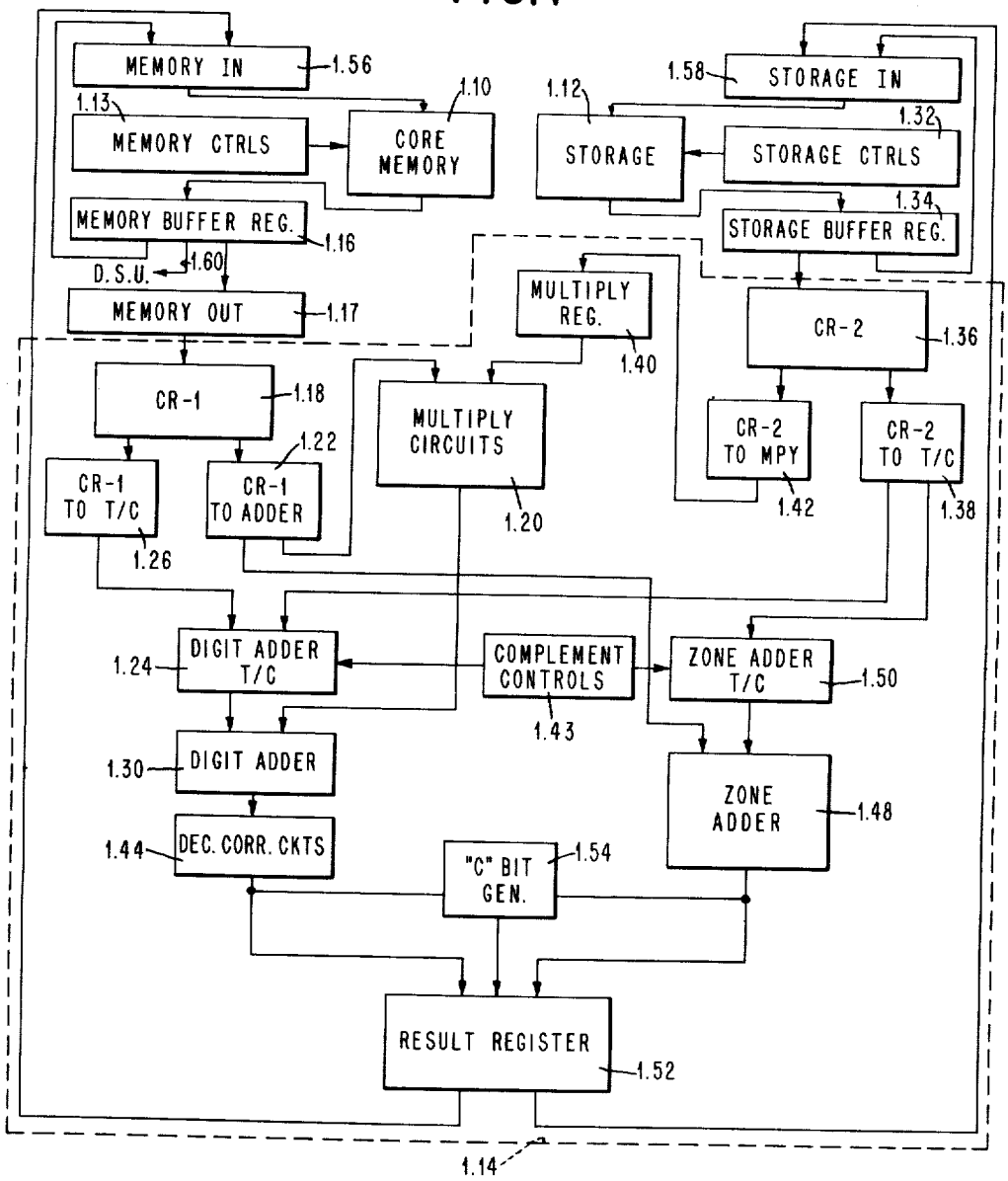
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OVERLAP MODE CONTROL

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FIG. 1



INVENTORS
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ATTORNEY

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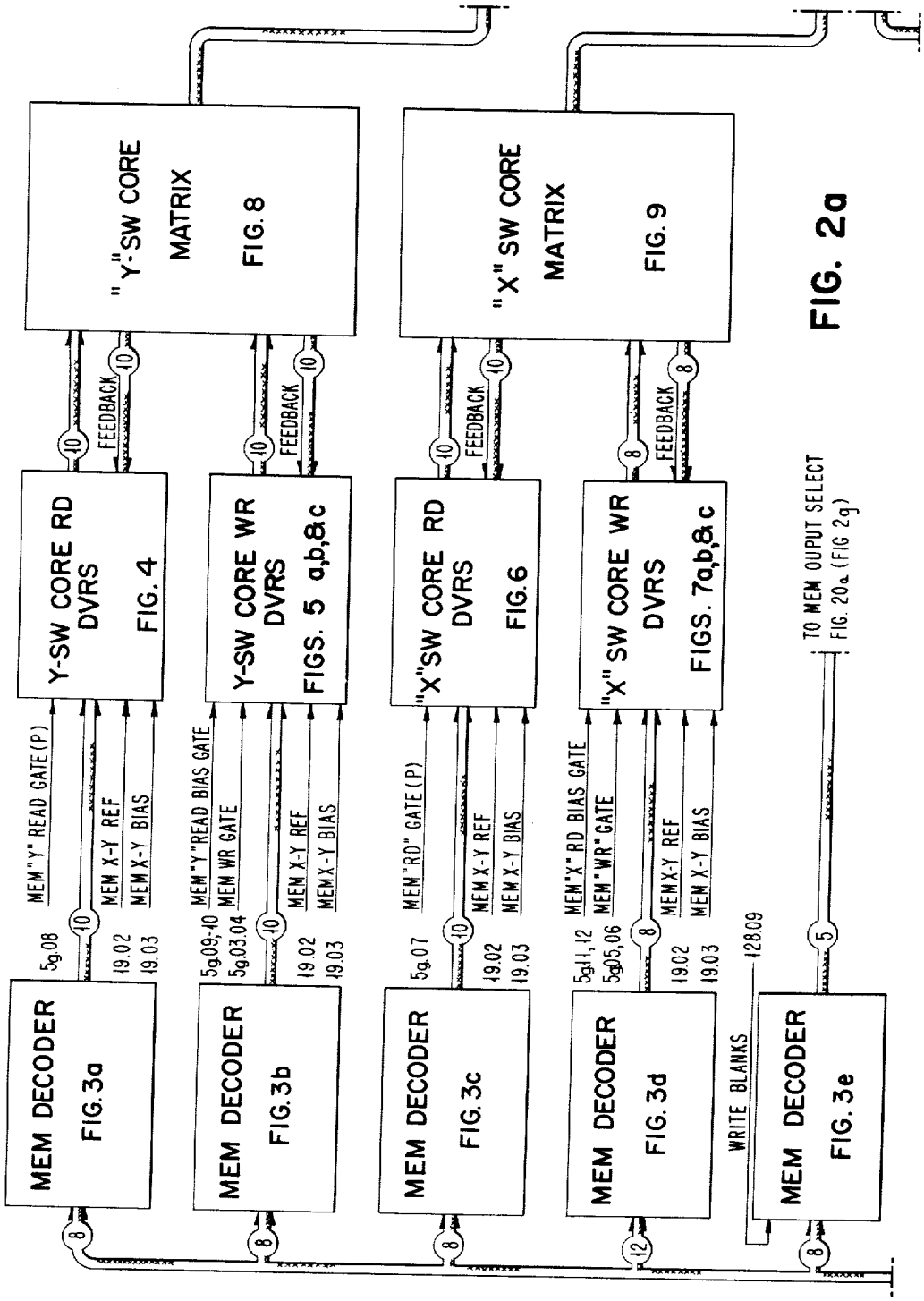
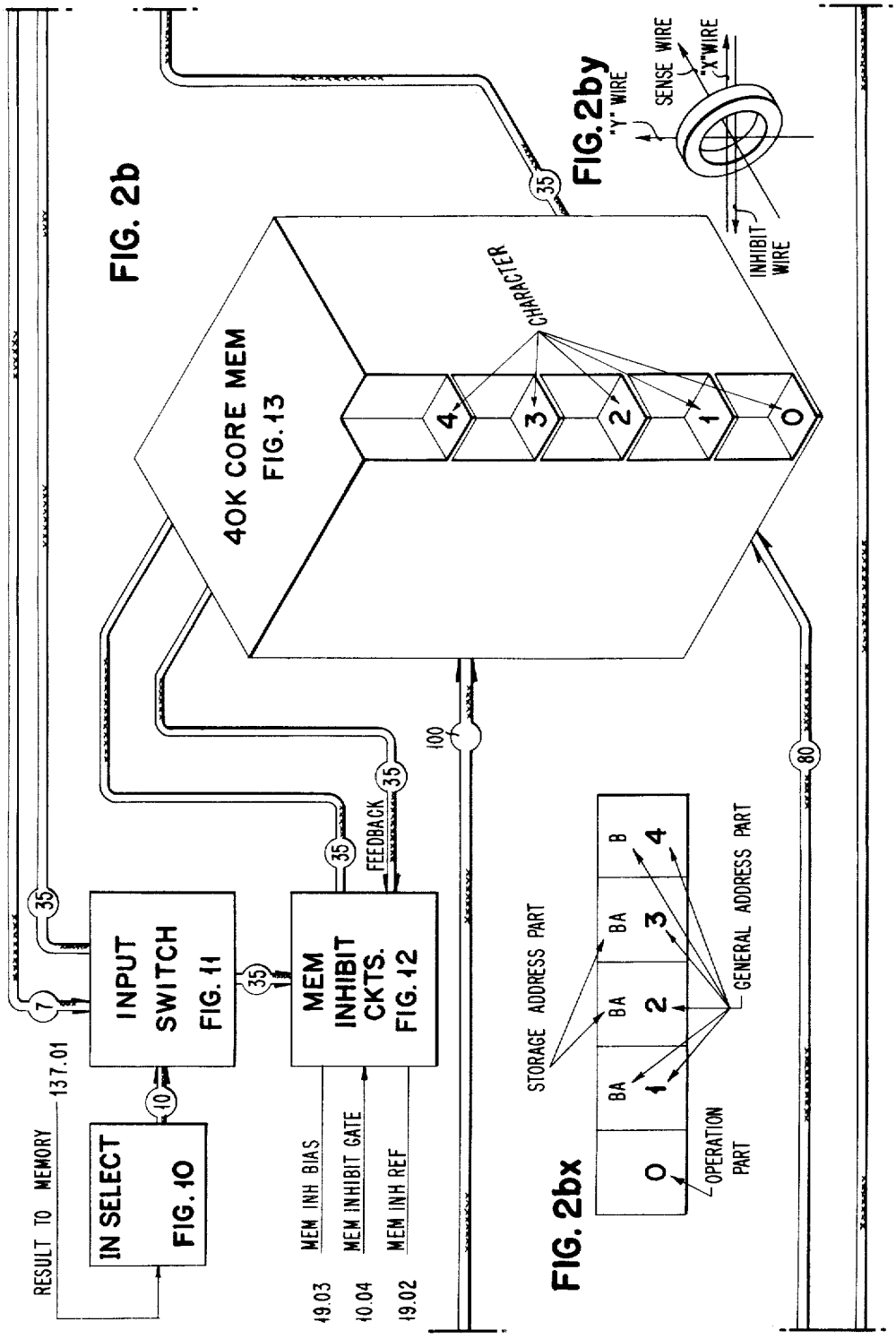


FIG. 2a


FIG. 2b
FIG. 2by
SENSE WIRE
"Y" WIRE
"X" WIRE
INHIBIT WIRE
CHARACTER
40K CORE MEM FIG. 13
4
3
2
1
0
35
100
80
7
10
FEEDBACK
INPUT SWITCH FIG. 11
MEM INHIBIT CKTS. FIG. 12
IN SELECT FIG. 10
RESULT TO MEMORY
137.01
MEM INH BIAS
MEM INHIBIT GATE
MEM INH REF
19.03
10.04
19.02
FIG. 2bx
STORAGE ADDRESS PART
GENERAL ADDRESS PART
OPERATION PART
BA
B
0
1
2
3
4

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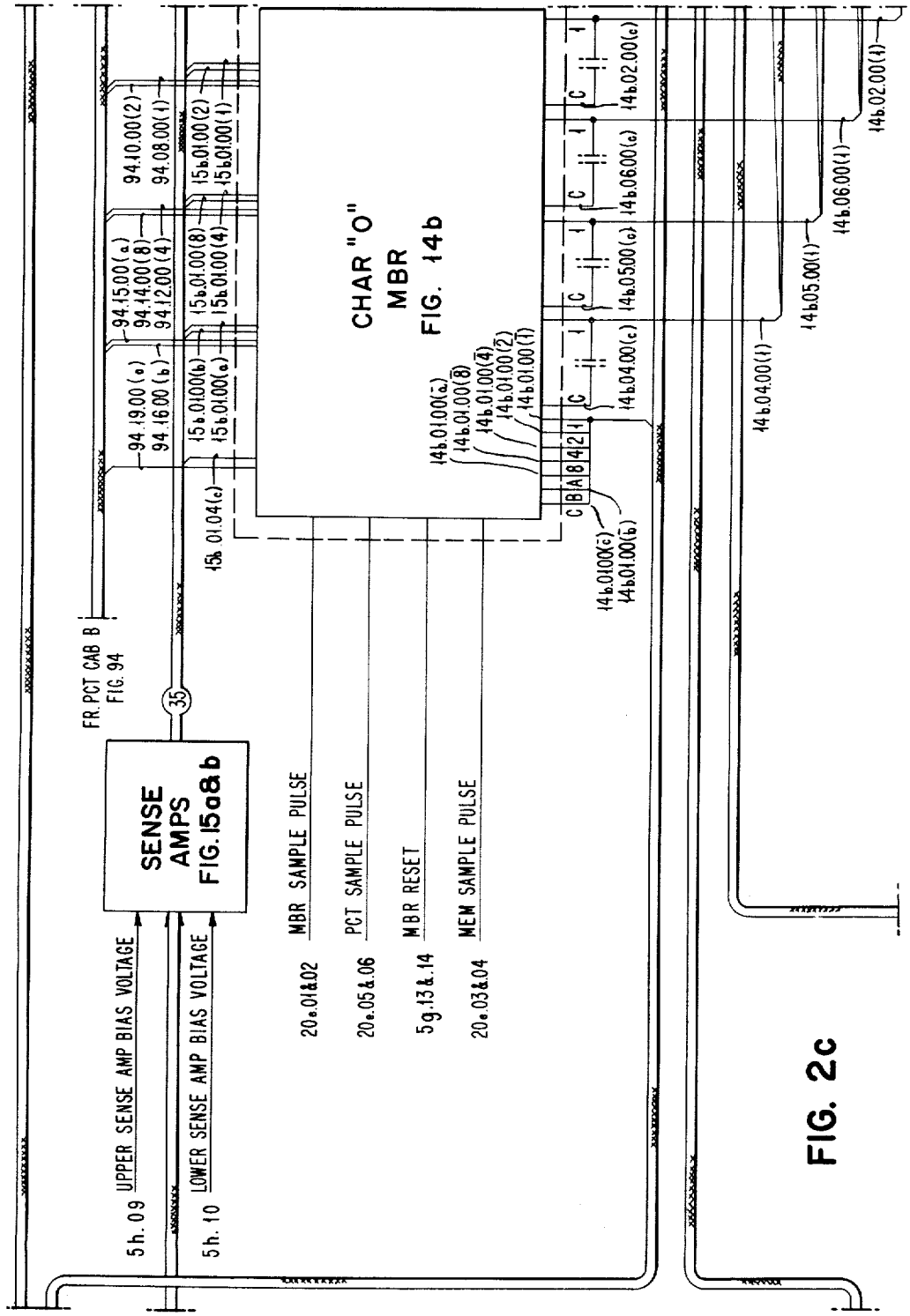
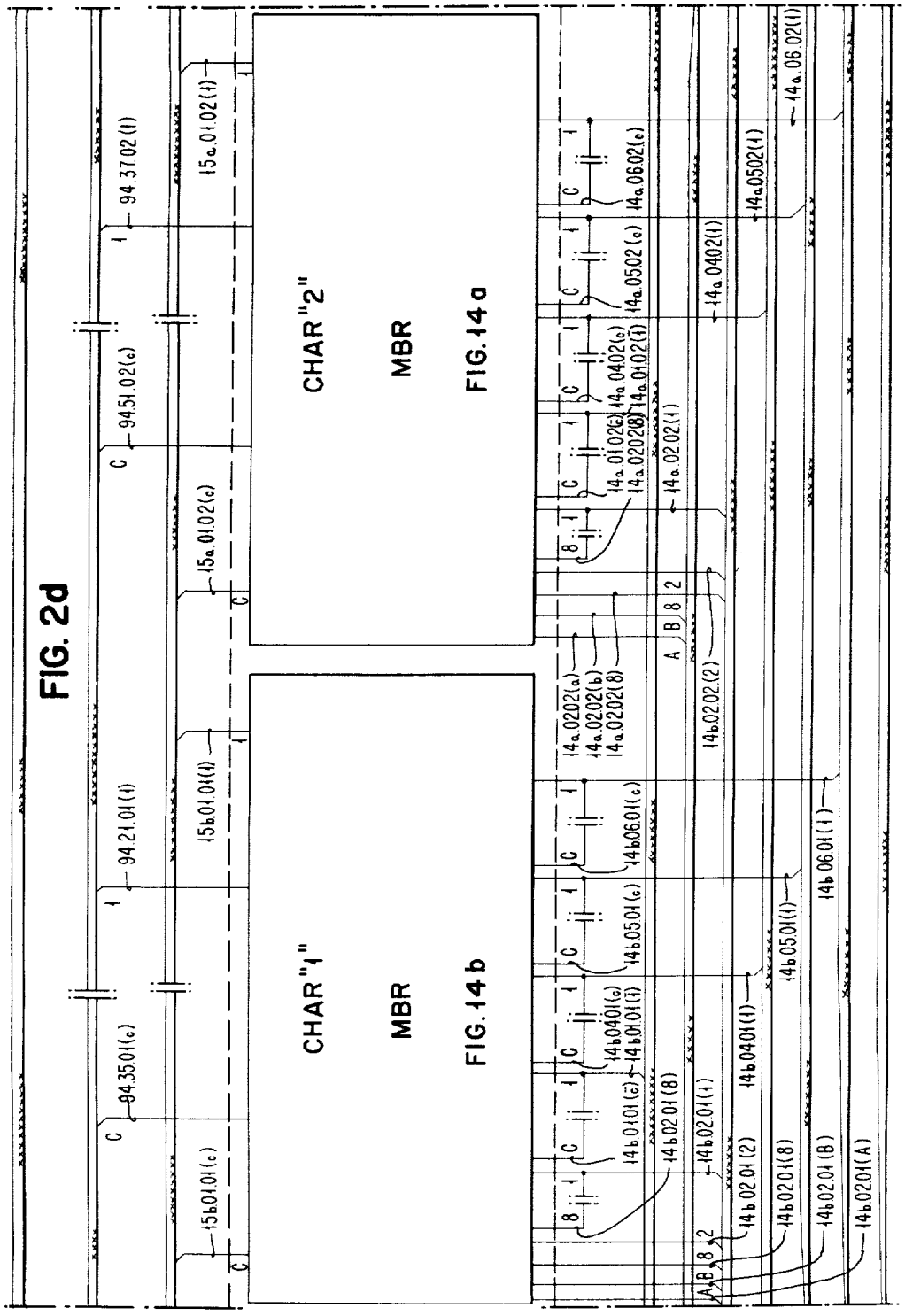


FIG. 2c

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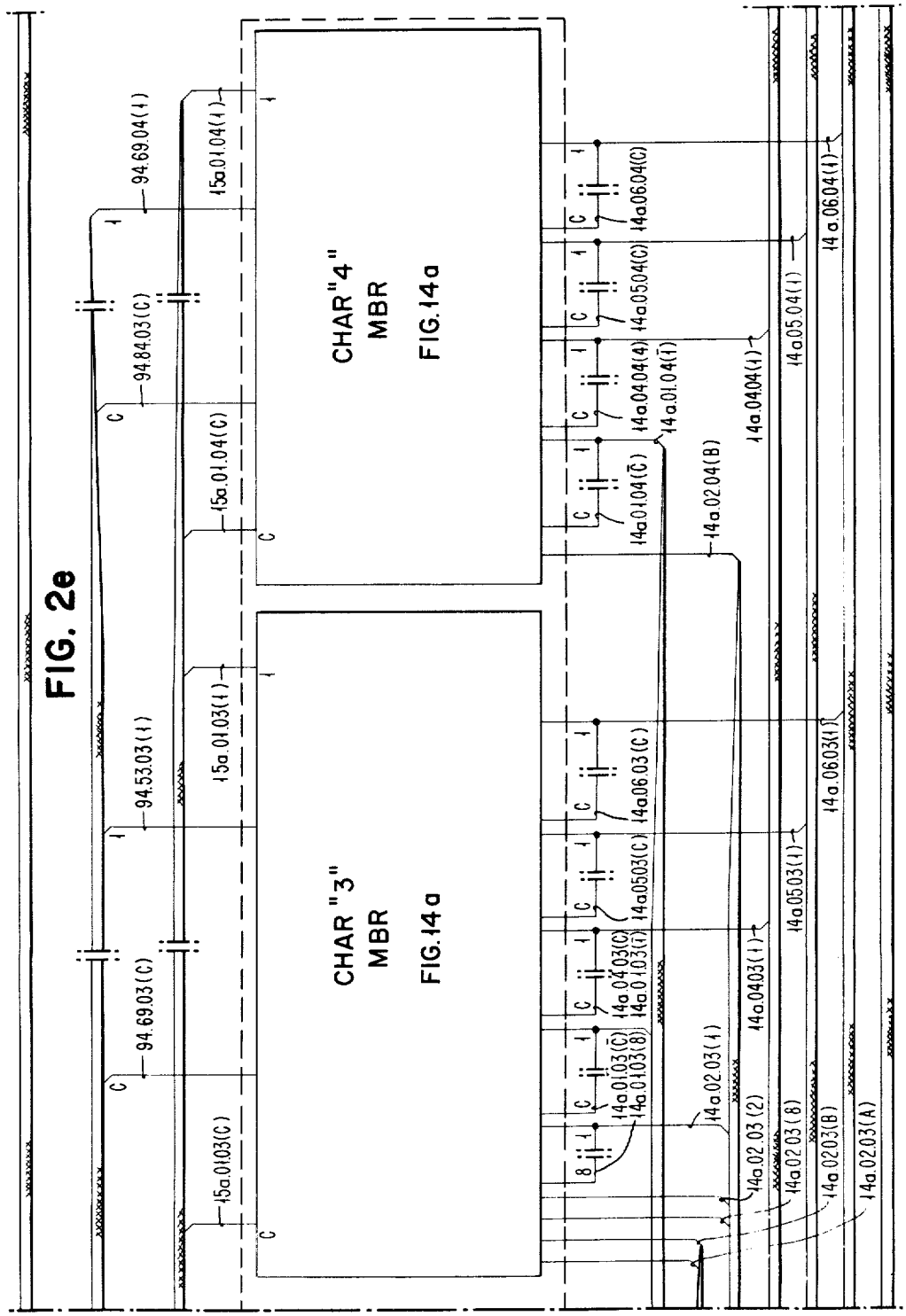

FIG. 2e
CHAR "4" MBR FIG. 14a
CHAR "3" MBR FIG. 14a
94.69.04(1)
15a.01.04(1)
94.84.03(C)
15a.01.04(C)
94.53.03(1)
15a.01.03(1)
94.69.03(C)
15a.01.03(C)
14a.06.04(C)
14a.05.04(C)
14a.04.04(4)
14a.01.04(1)
14a.01.04(C)
14a.02.04(B)
14a.04.04(1)
14a.05.04(1)
14a.06.04(1)
14a.06.03(C)
14a.05.03(C)
14a.04.03(C)
14a.01.03(1)
14a.01.03(C)
14a.01.03(B)
14a.02.03(1)
14a.04.03(1)
14a.05.03(1)
14a.06.03(1)
14a.02.03(2)
14a.02.03(8)
14a.02.03(B)
14a.02.03(A)

FIG. 2f

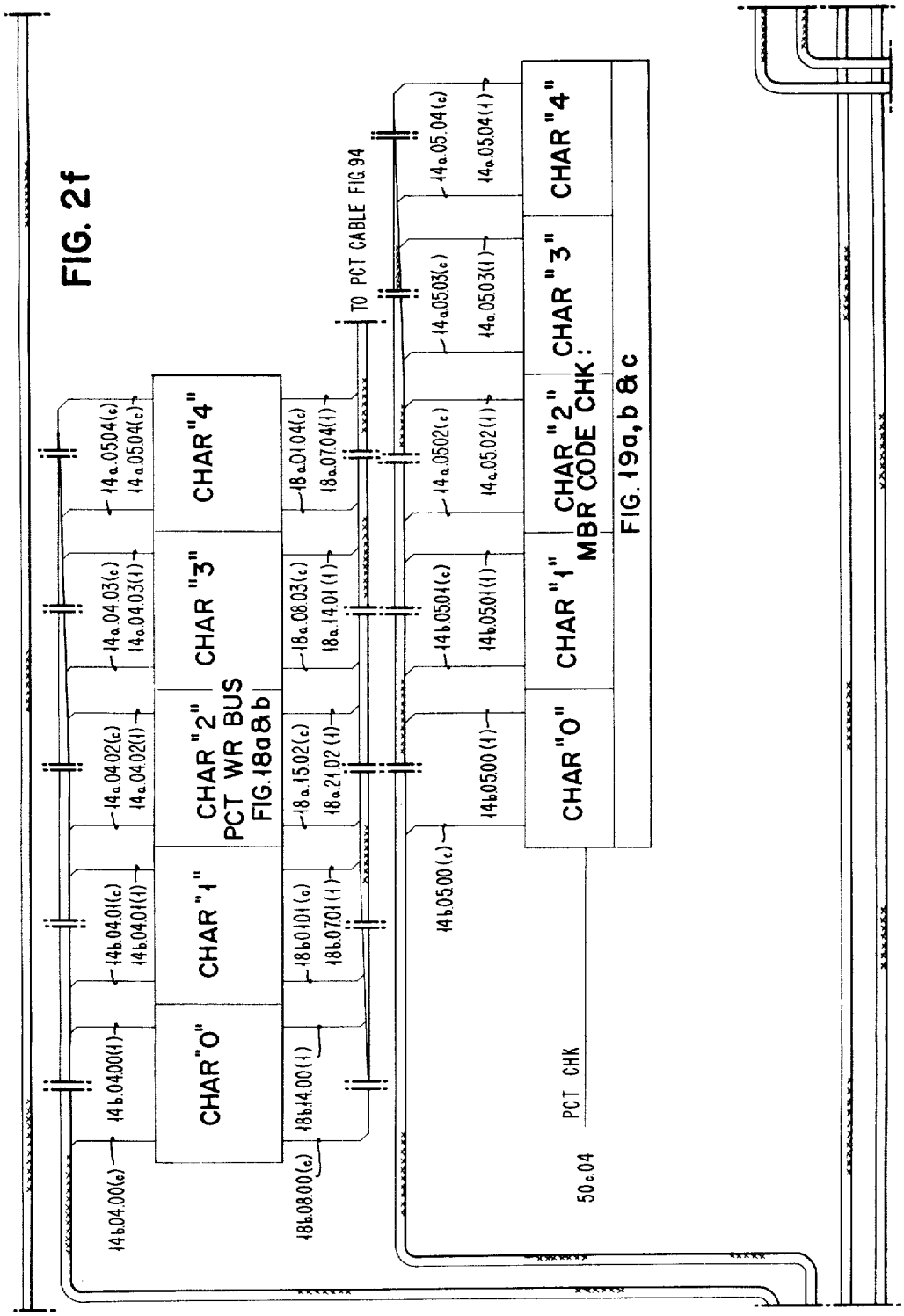
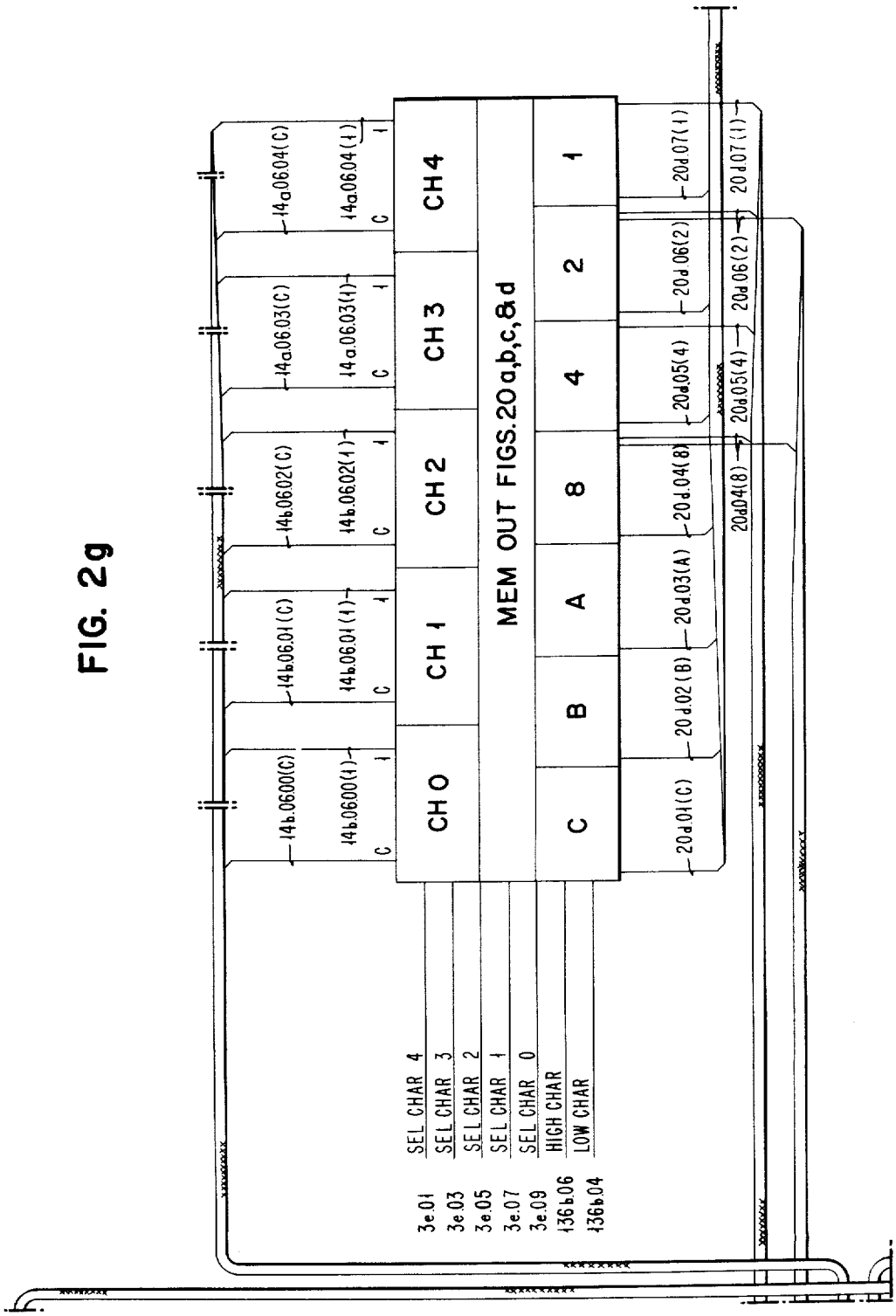

CHAR "0"
CHAR "1"
CHAR "2"
CHAR "3"
CHAR "4"
PCT WR BUS
FIG. 18a & b
TO PCT CABLE FIG. 94
CHAR "0"
CHAR "1"
CHAR "2"
CHAR "3"
CHAR "4"
MBR CODE CHK:
FIG. 19a, b & c
PCT CHK
50c.04

FIG. 2g


CH 0
CH 1
CH 2
CH 3
CH 4
MEM OUT FIGS. 20a,b,c,&d
C
B
A
8
4
2
1
14b.06.00(C)
14b.06.00(1)
14b.06.01(C)
14b.06.01(1)
14b.06.02(C)
14b.06.02(1)
14a.06.03(C)
14a.06.03(1)
14a.06.04(C)
14a.06.04(1)
20d.01(C)
20d.02(B)
20d.03(A)
20d.04(8)
20d.05(4)
20d.06(2)
20d.07(1)
SEL CHAR 4
SEL CHAR 3
SEL CHAR 2
SEL CHAR 1
SEL CHAR 0
HIGH CHAR
LOW CHAR
3e.01
3e.03
3e.05
3e.07
3e.09
136b.06
136b.04

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FIG. 2h

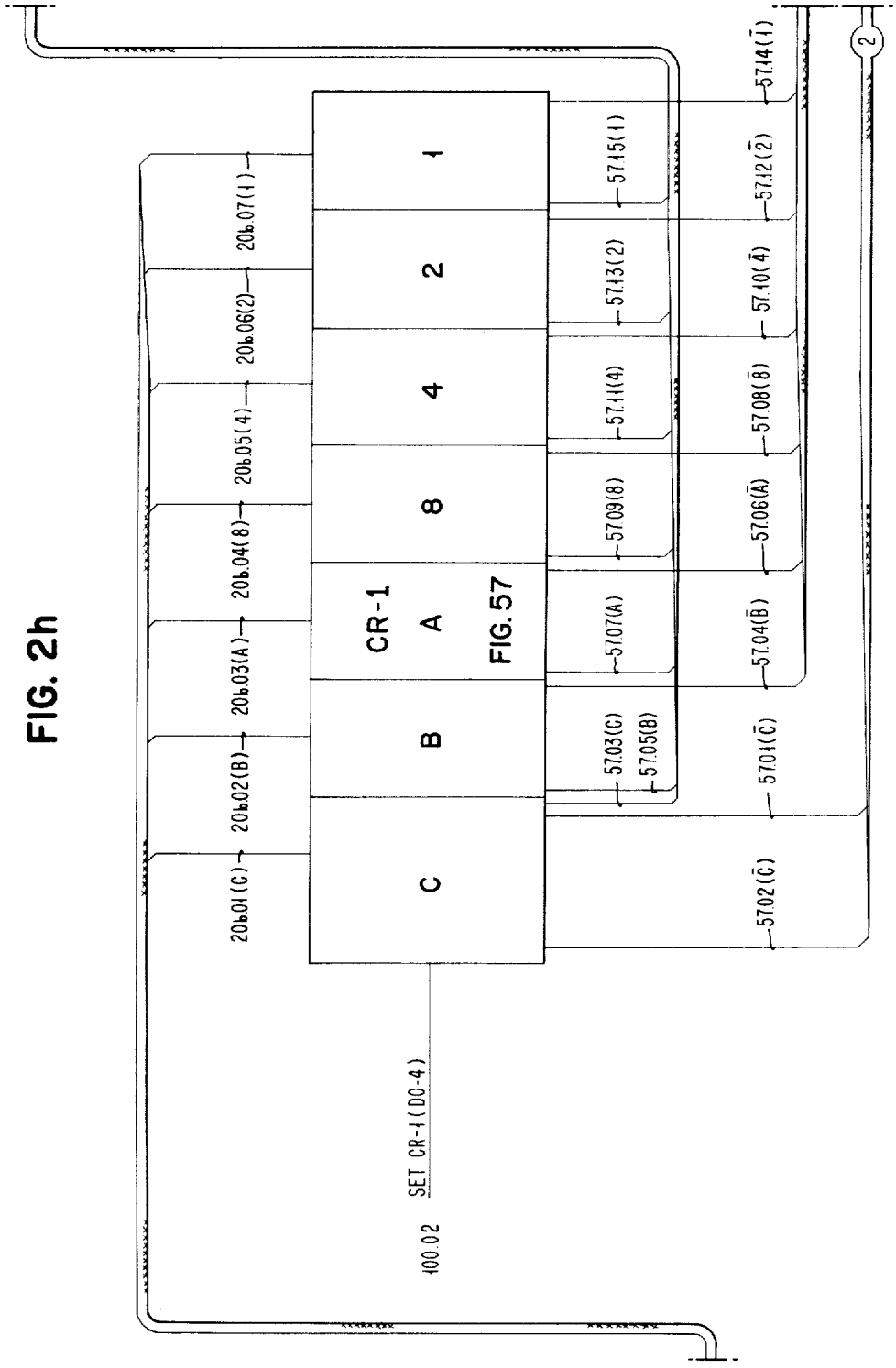


FIG. 2i

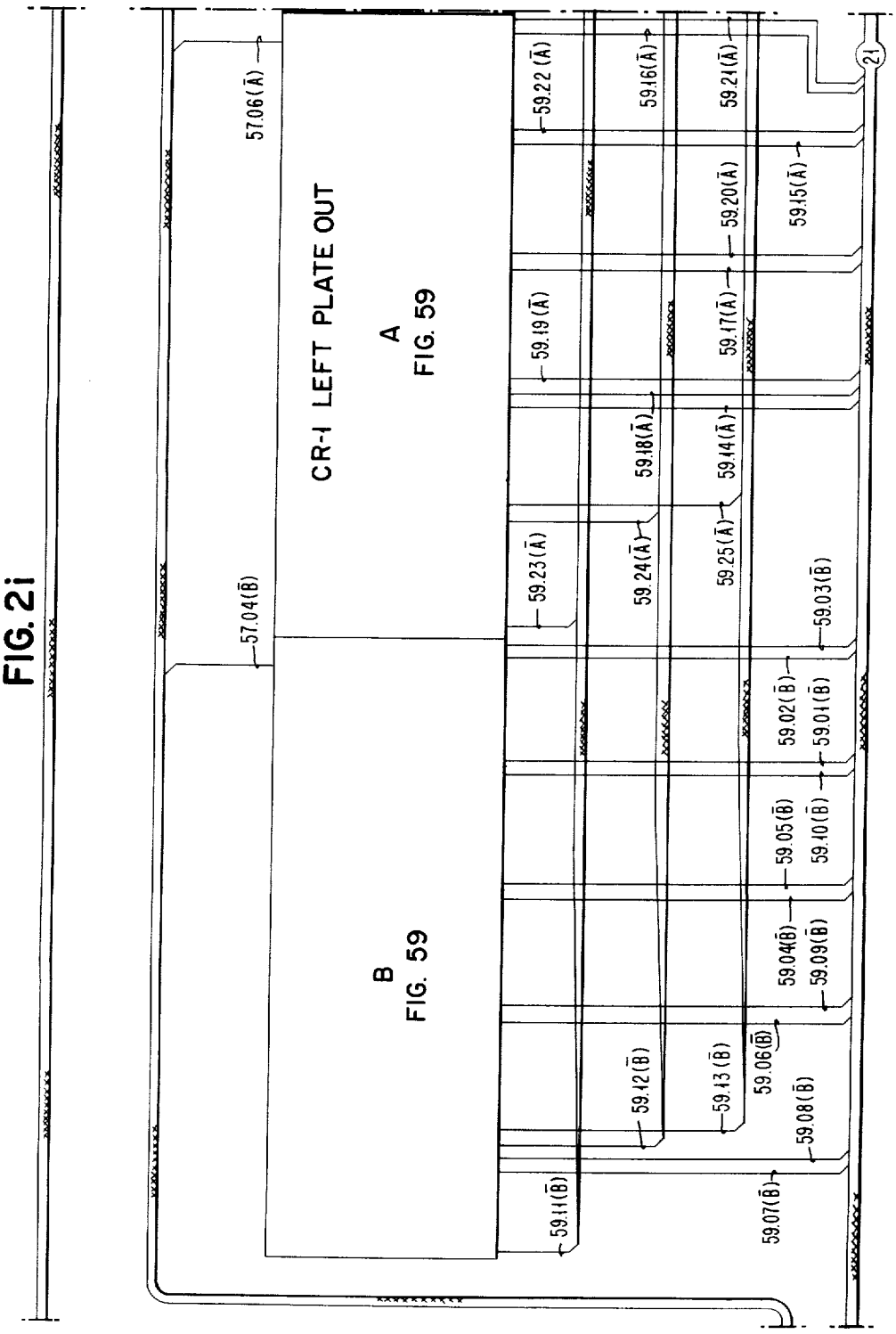
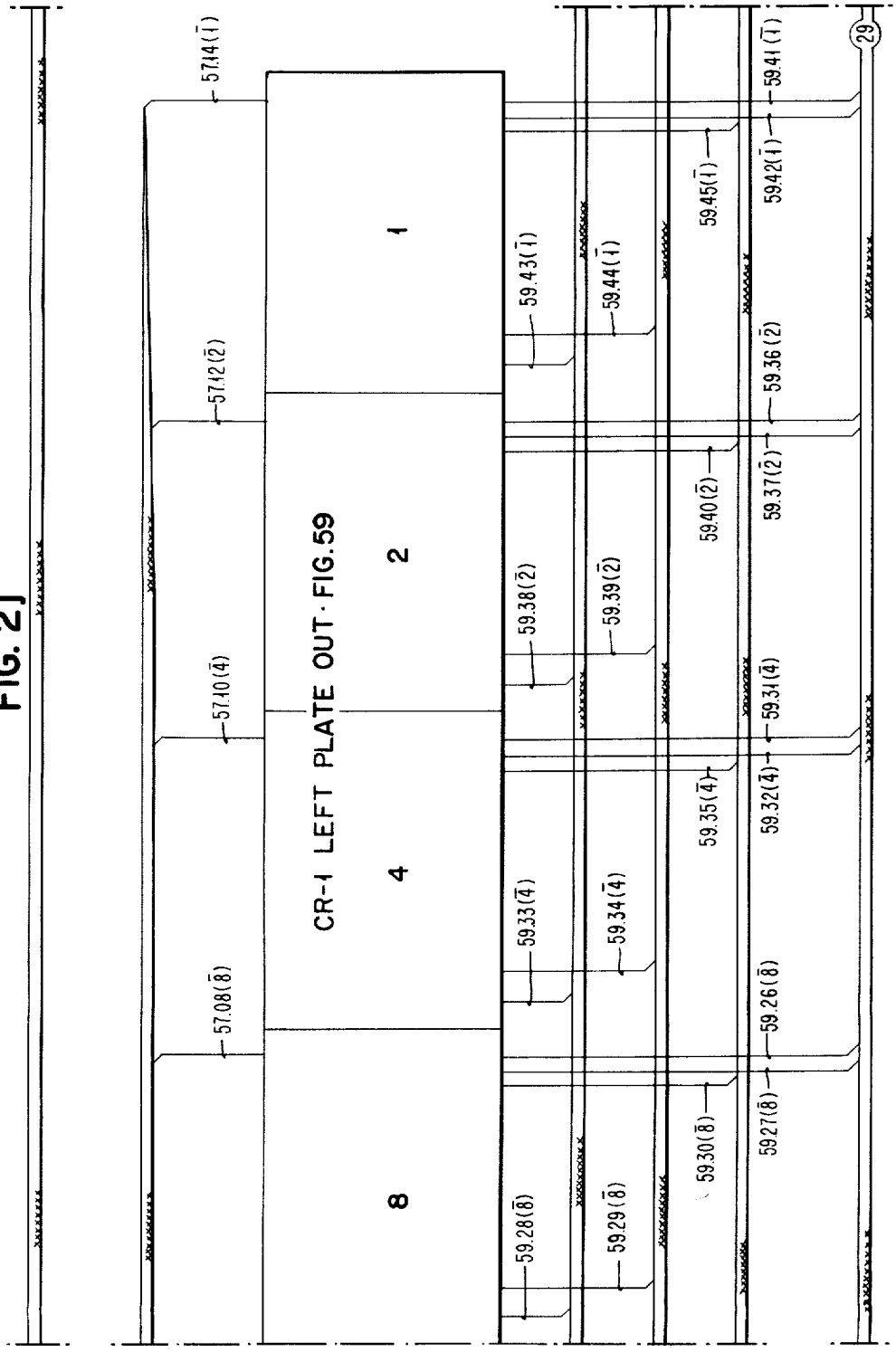

CR-1 LEFT PLATE OUT
A
FIG. 59
B
FIG. 59
57.06(Ā)
57.04(B̄)
59.22 (Ā)
59.16(Ā)
59.21(Ā)
59.20(Ā)
59.15(Ā)
59.19 (Ā)
59.17(Ā)
59.18(Ā)
59.14(Ā)
59.23 (Ā)
59.24(Ā)
59.25(Ā)
59.03(B̄)
59.02(B̄)
59.01(B̄)
59.05(B̄)
59.10(B̄)
59.04(B̄)
59.09(B̄)
59.12(B̄)
59.13 (B̄)
59.06(B̄)
59.08(B̄)
59.11(B̄)
59.07(B̄)
21

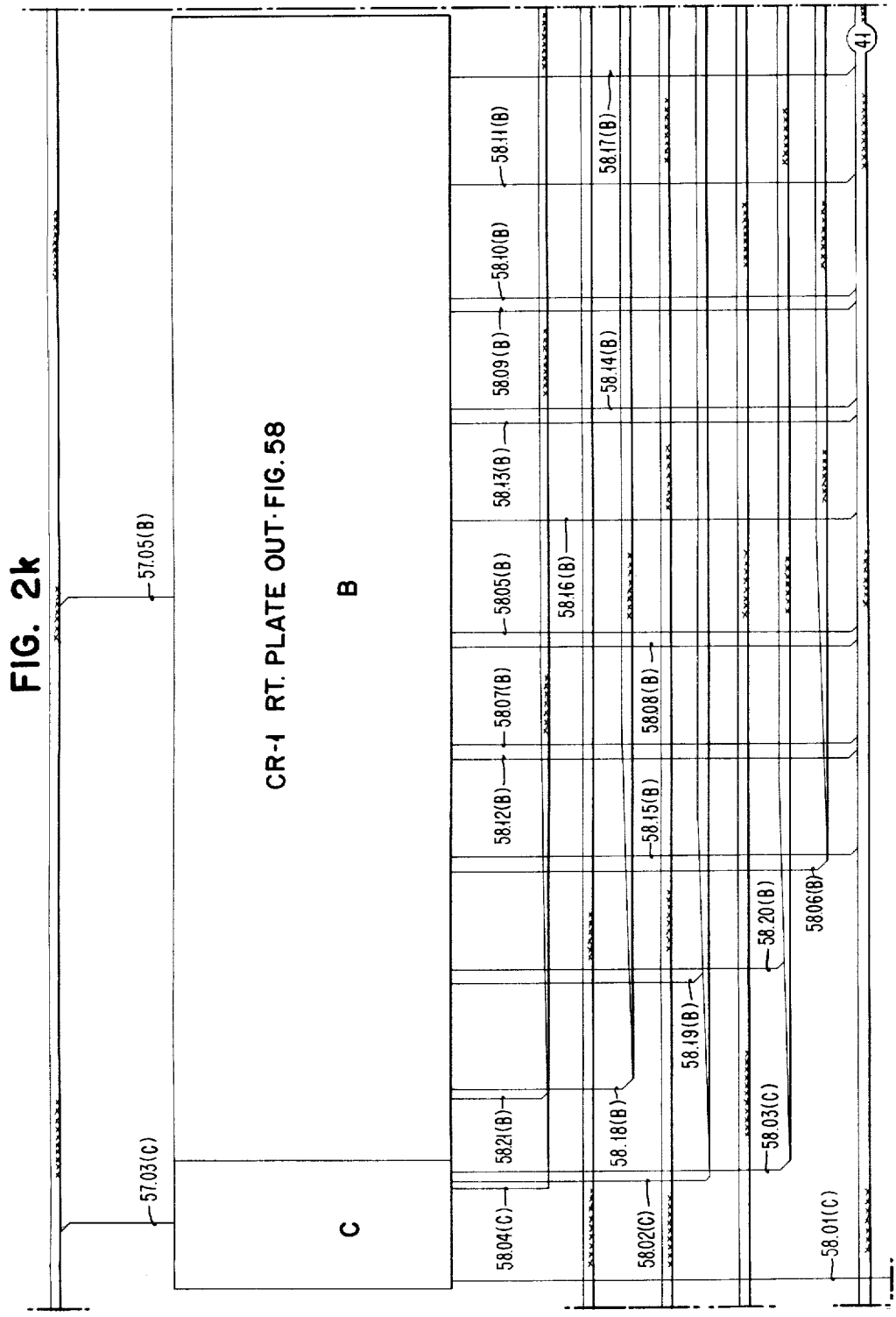
FIG. 2j


CR-1 LEFT PLATE OUT · FIG.59
1
2
4
8
57.14(1̄)
57.12(2̄)
57.10(4̄)
57.08(8̄)
59.43(1̄)
59.44(1̄)
59.45(1̄)
59.41(1̄)
59.42(1̄)
59.36(2̄)
59.38(2̄)
59.39(2̄)
59.40(2̄)
59.37(2̄)
59.33(4̄)
59.34(4̄)
59.35(4̄)
59.31(4̄)
59.32(4̄)
59.28(8̄)
59.29(8̄)
59.30(8̄)
59.26(8̄)
59.27(8̄)
29

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FIG. 21

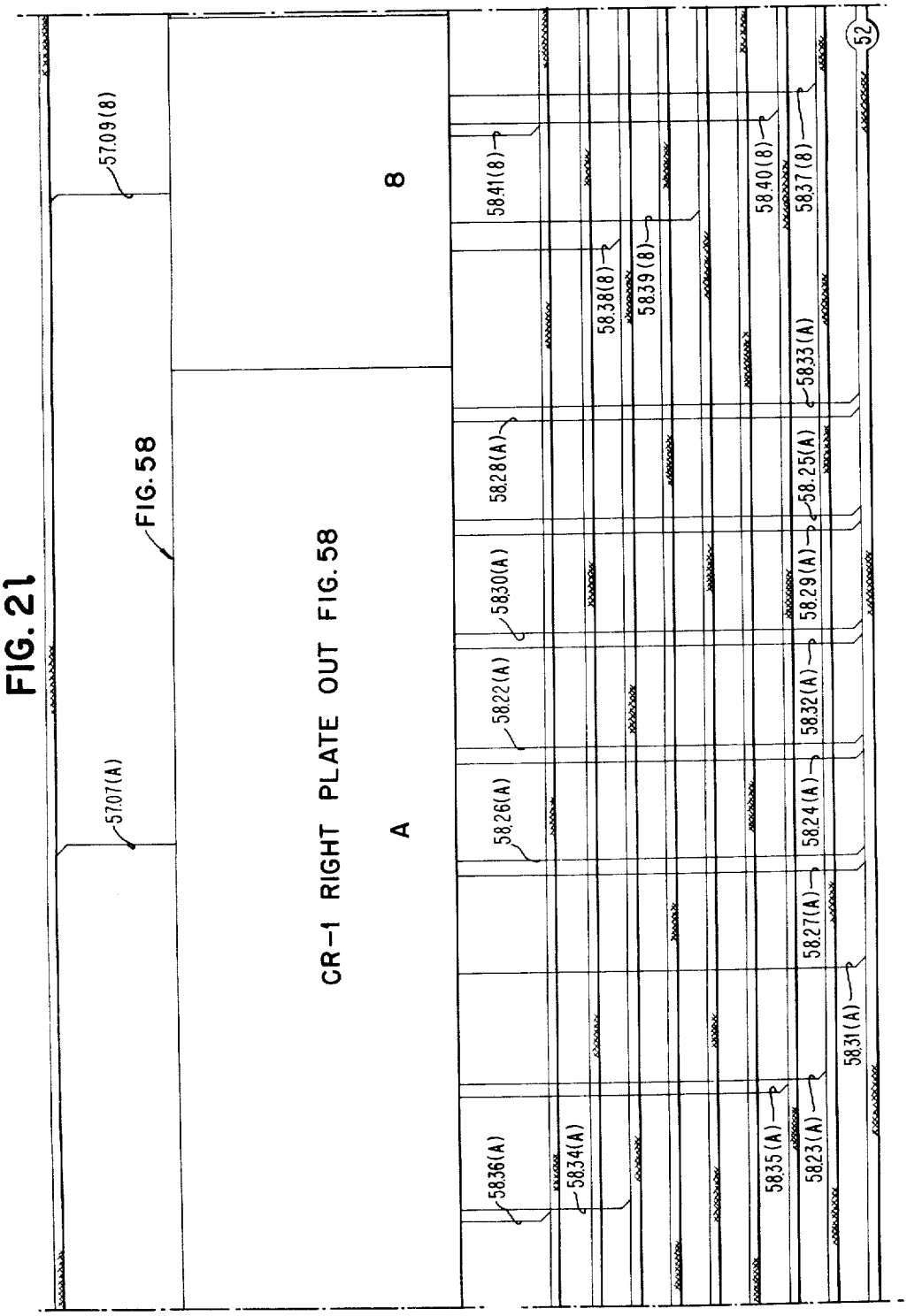


FIG. 2m

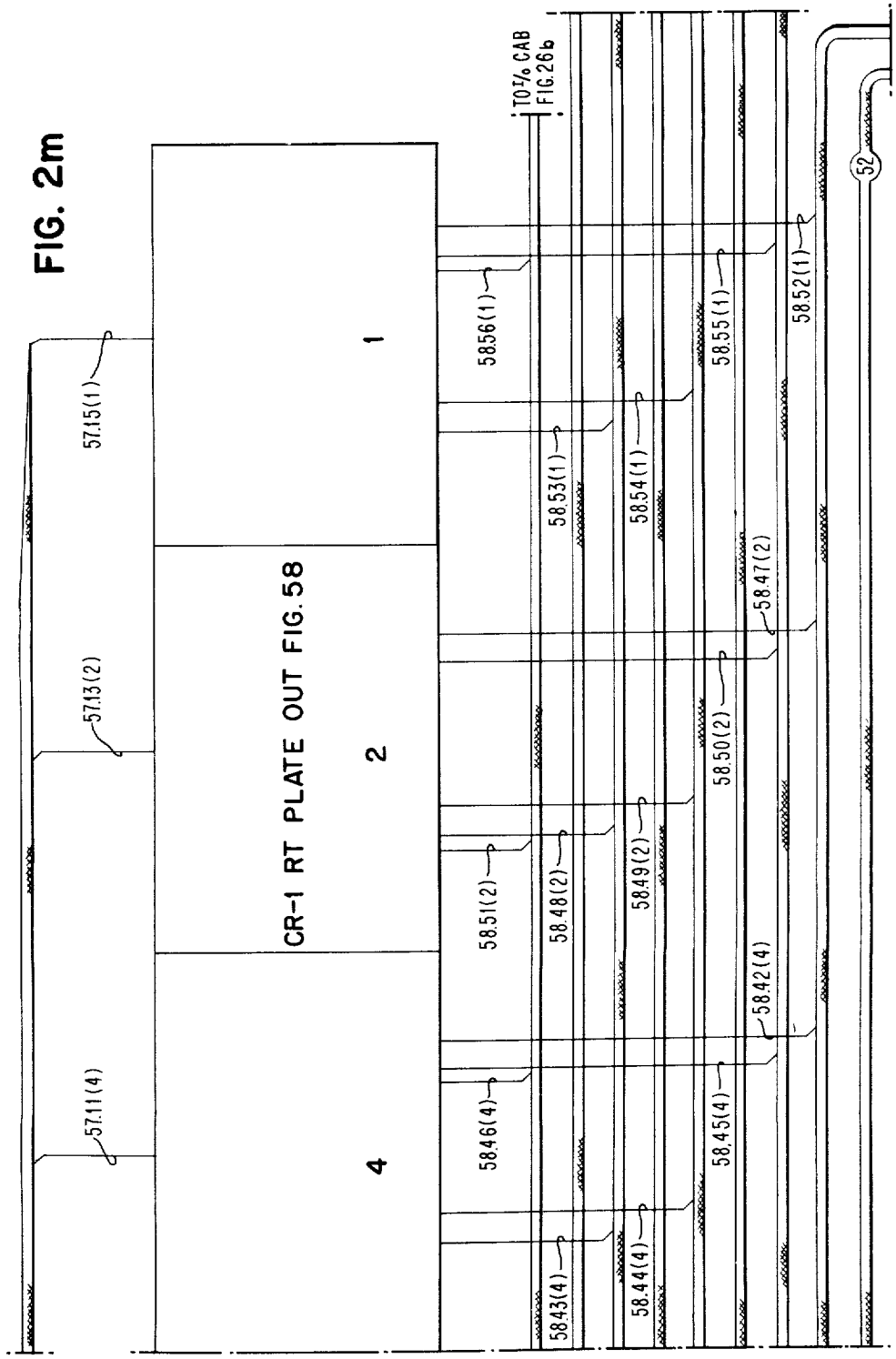
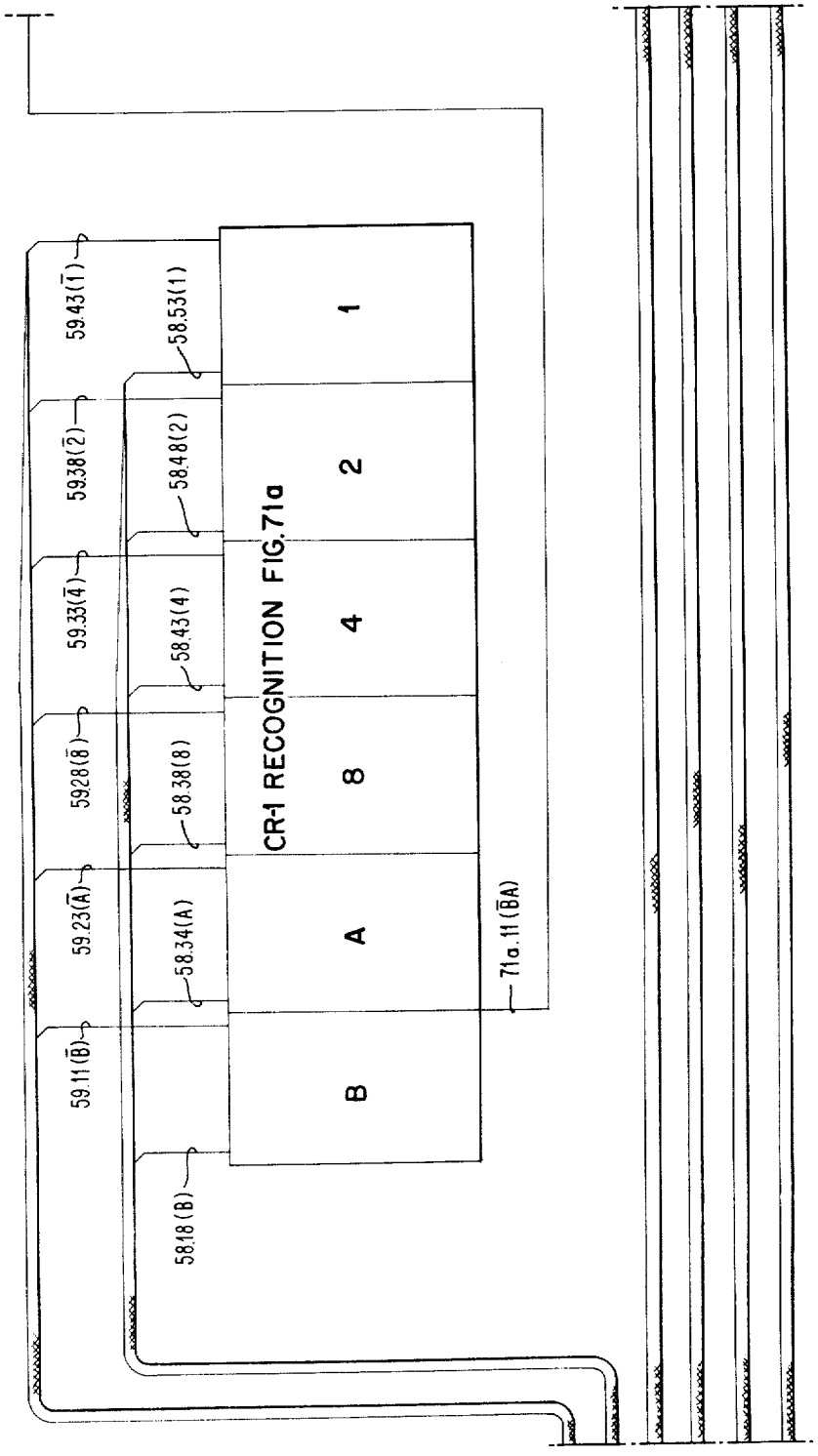

TO 1/0 CAB FIG. 26b
CR-1 RT PLATE OUT FIG. 58
1
2
4
57.15(1)
57.13(2)
57.11(4)
58.56(1)
58.53(1)
58.54(1)
58.55(1)
58.52(1)
58.47(2)
58.50(2)
58.51(2)
58.48(2)
58.49(2)
58.42(4)
58.46(4)
58.45(4)
58.43(4)
58.44(4)
52

FIG. 2n


59.43(1̄)
58.53(1)
59.38(2̄)
58.48(2)
59.33(4̄)
58.43(4)
59.28(8̄)
58.38(8)
59.23(Ā)
58.34(A)
59.11(B̄)
58.18(B)
CR-1 RECOGNITION FIG.71a
1
2
4
8
A
B
71a.11(B̄A)

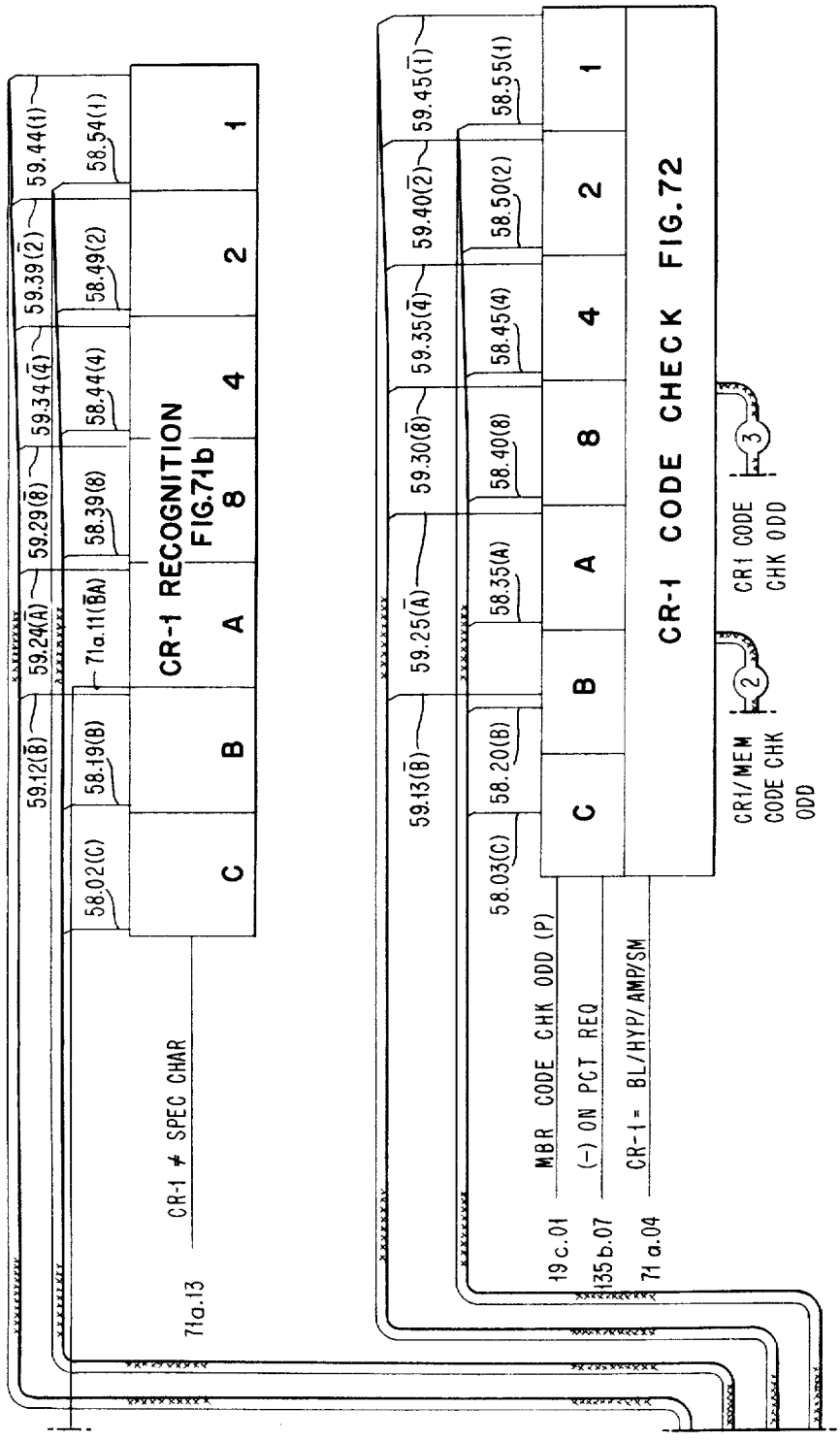

CR-1 RECOGNITION
FIG.71b
C
B
A
8
4
2
1
CR-1 ≠ SPEC CHAR
71a.13
58.02(C)
58.19(B)
71a.11(BA)
58.39(8)
58.44(4)
58.49(2)
58.54(1)
59.12(B̄)
59.24(Ā)
59.29(8̄)
59.34(4̄)
59.39(2̄)
59.44(1̄)
CR-1 CODE CHECK FIG.72
58.03(C)
58.20(B)
58.35(A)
58.40(8)
58.45(4)
58.50(2)
58.55(1)
59.13(B̄)
59.25(Ā)
59.30(8̄)
59.35(4̄)
59.40(2̄)
59.45(1̄)
MBR CODE CHK ODD (P)
19 c.01
(-) ON PCT REQ
135 b.07
CR-1= BL/HYP/AMP/SM
71 a.04
CR1/MEM CODE CHK ODD
CR1 CODE CHK ODD
2
3

FIG. 20

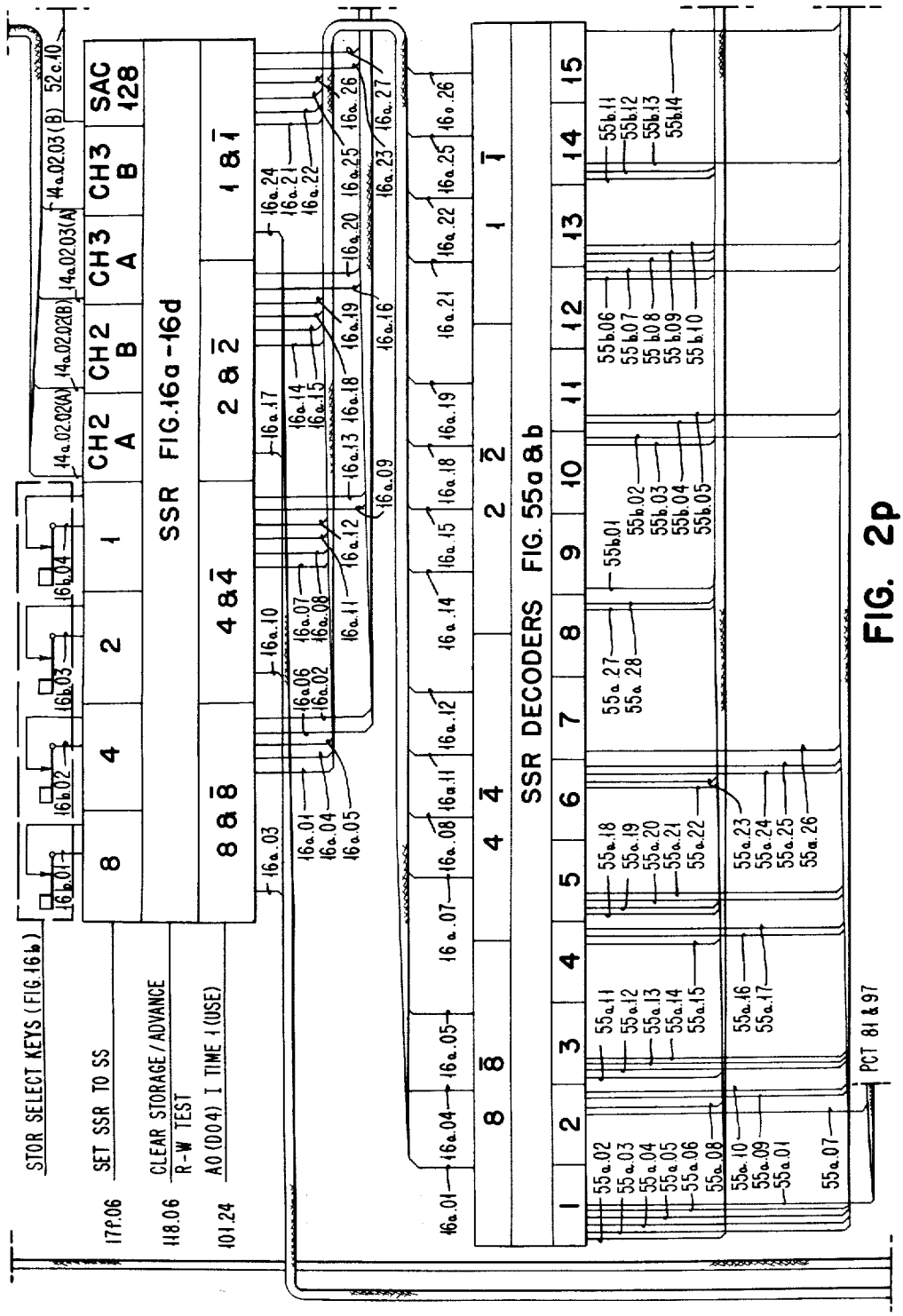

STOR SELECT KEYS (FIG.16b)
17P.06 SET SSR TO SS
118.06 CLEAR STORAGE / ADVANCE
R-W TEST
101.24 A0 (004) I TIME 1 (USE)
SSR FIG.16a-16d
CH2 A
CH2 B
CH3 A
CH3 B
SAC 128
SSR DECODERS FIG. 55a & b
PCT 81 & 97

FIG. 2p

FIG. 2q

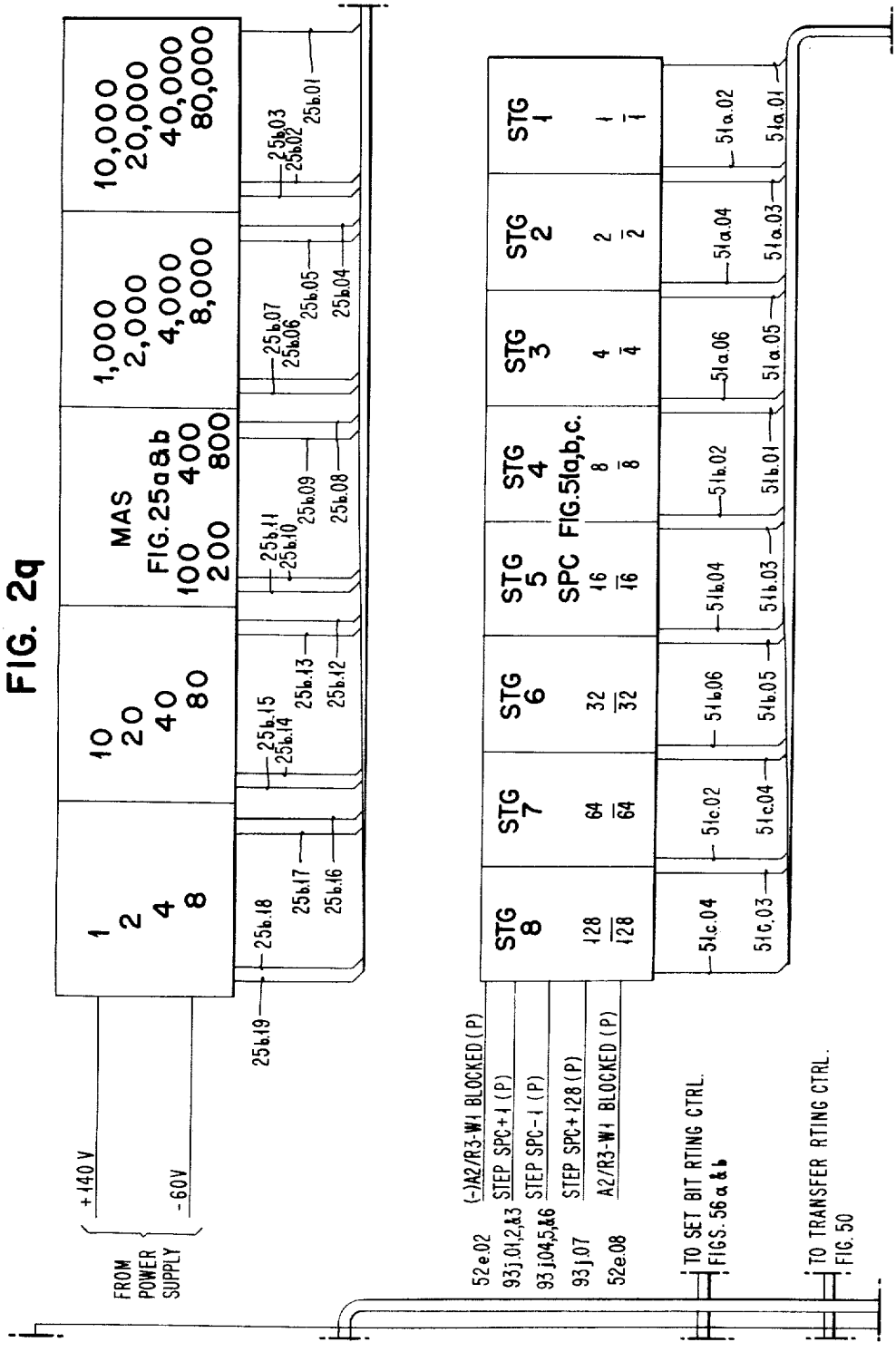
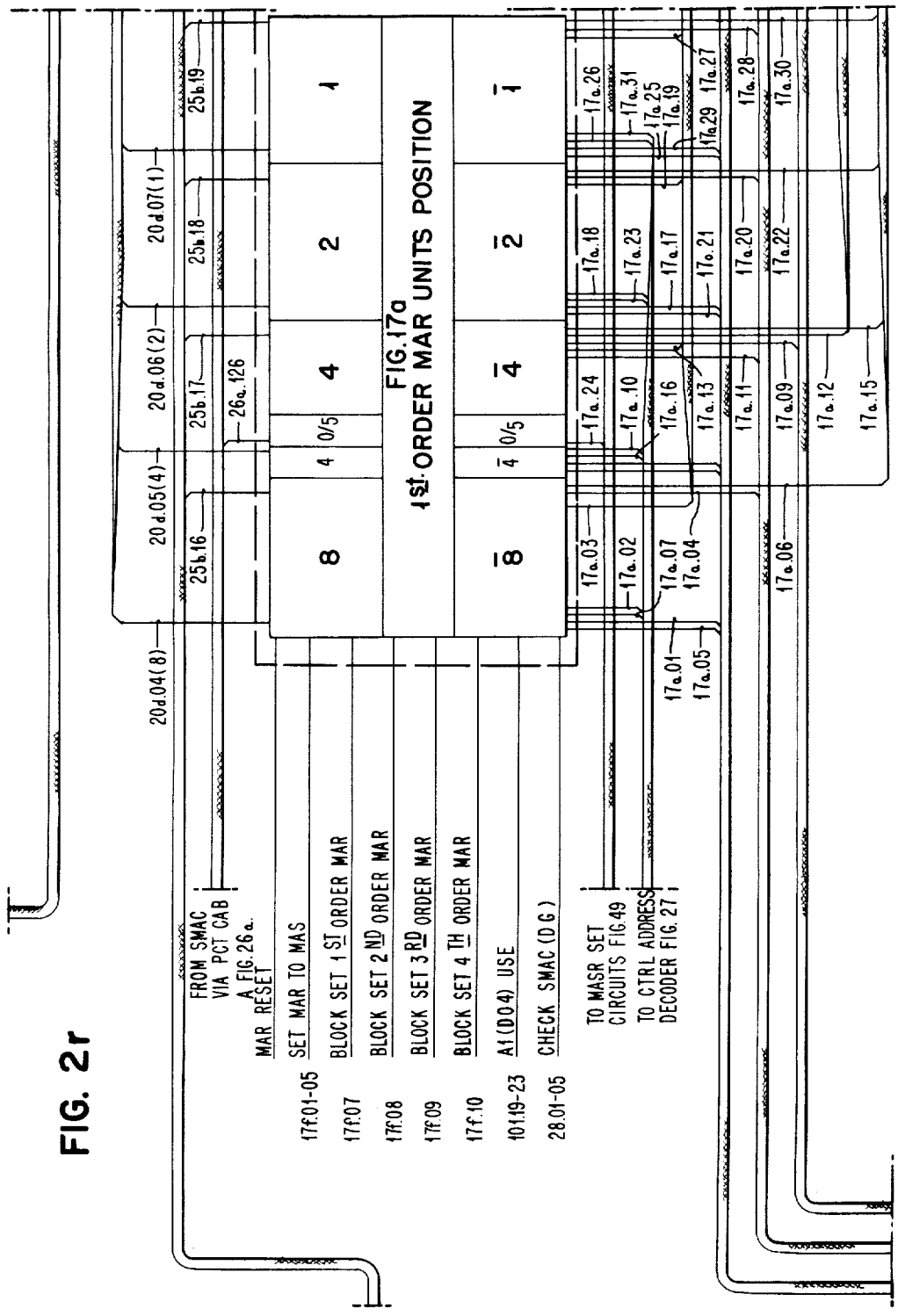

1 2 4 8
10 20 40 80
MAS FIG. 25a&b 100 200 400 800
1,000 2,000 4,000 8,000
10,000 20,000 40,000 80,000
25b.01 25b.02 25b.03 25b.04 25b.05 25b.06 25b.07 25b.08 25b.09 25b.10 25b.11 25b.12 25b.13 25b.14 25b.15 25b.16 25b.17 25b.18 25b.19
STG 8 STG 7 STG 6 STG 5 STG 4 STG 3 STG 2 STG 1
SPC FIG.51a,b,c.
128 64 32 16 8 4 2 1
51a.01 51a.02 51a.03 51a.04 51a.05 51a.06
51b.01 51b.02 51b.03 51b.04 51b.05 51b.06
51c.01 51c.02 51c.03 51c.04
+140 V
-60V
FROM POWER SUPPLY
52e.02 (-)A2/R3-W1 BLOCKED (P)
93j.01,2,&3 STEP SPC+1 (P)
93j.04,5,&6 STEP SPC-1 (P)
93j.07 STEP SPC+128 (P)
52e.08 A2/R3-W1 BLOCKED (P)
TO SET BIT RTING CTRL. FIGS. 56a & b
TO TRANSFER RTING CTRL. FIG. 50

FIG. 2r


FIG.17a
1ST ORDER MAR UNITS POSITION
8
4
2
1
0/5
FROM SMAC VIA PCT CAB A FIG.26a.
MAR RESET
SET MAR TO MAS
BLOCK SET 1 ST ORDER MAR
BLOCK SET 2 ND ORDER MAR
BLOCK SET 3 RD ORDER MAR
BLOCK SET 4 TH ORDER MAR
A1(004) USE
CHECK SMAC (D G)
TO MASR SET CIRCUITS FIG.49
TO CTRL ADDRESS DECODER FIG. 27
17f.01-05
17f.07
17f.08
17f.09
17f.10
10.19-23
28.01-05
20d.04(8)
20d.05(4)
20d.06(2)
20d.07(1)
25b.16
25b.17
25b.18
25b.19
26a.126
17a.01
17a.02
17a.03
17a.04
17a.05
17a.06
17a.07
17a.09
17a.10
17a.11
17a.12
17a.13
17a.15
17a.16
17a.17
17a.18
17a.19
17a.20
17a.21
17a.22
17a.23
17a.24
17a.25
17a.26
17a.27
17a.28
17a.29
17a.30
17a.31

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FIG. 2s

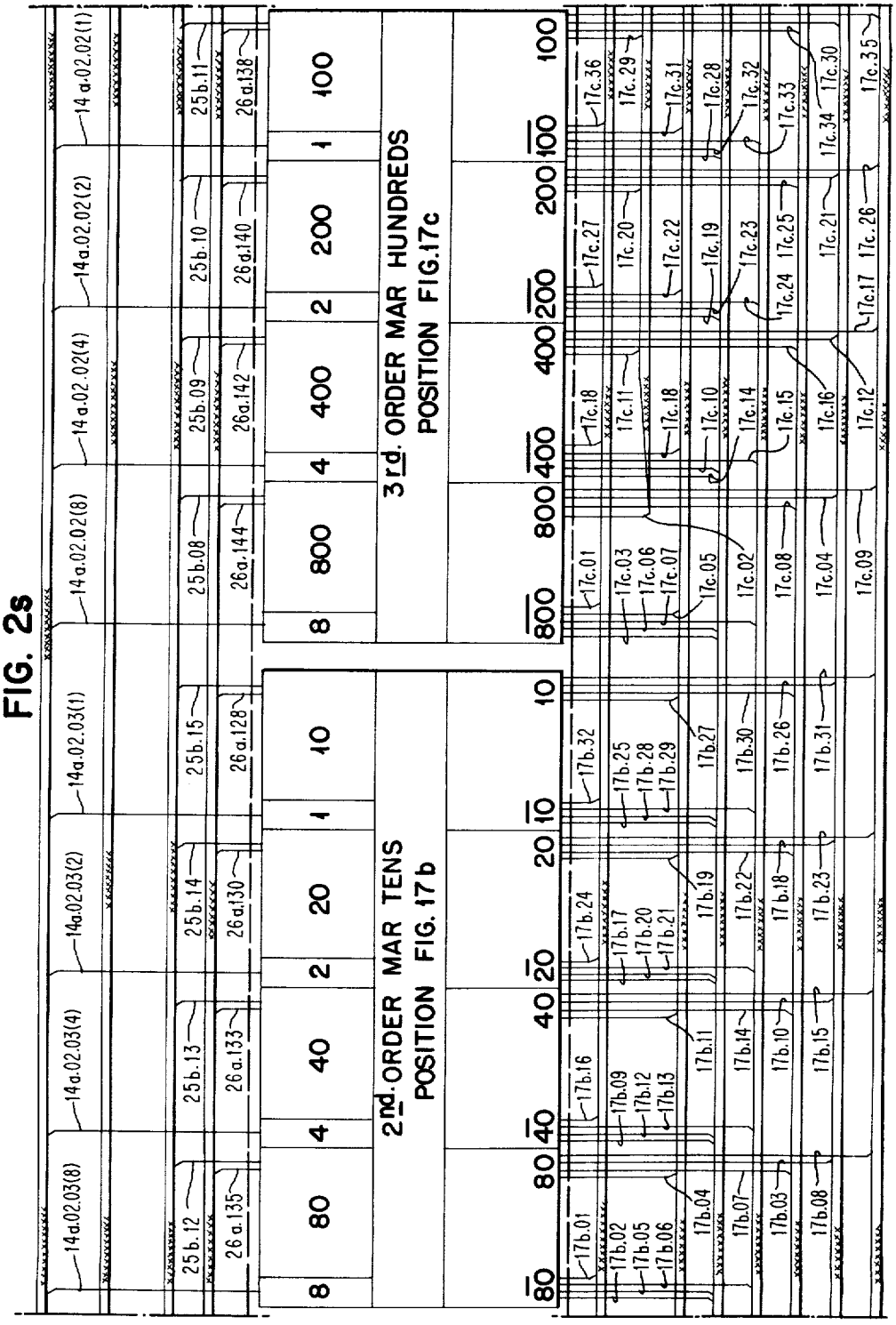


FIG. 21

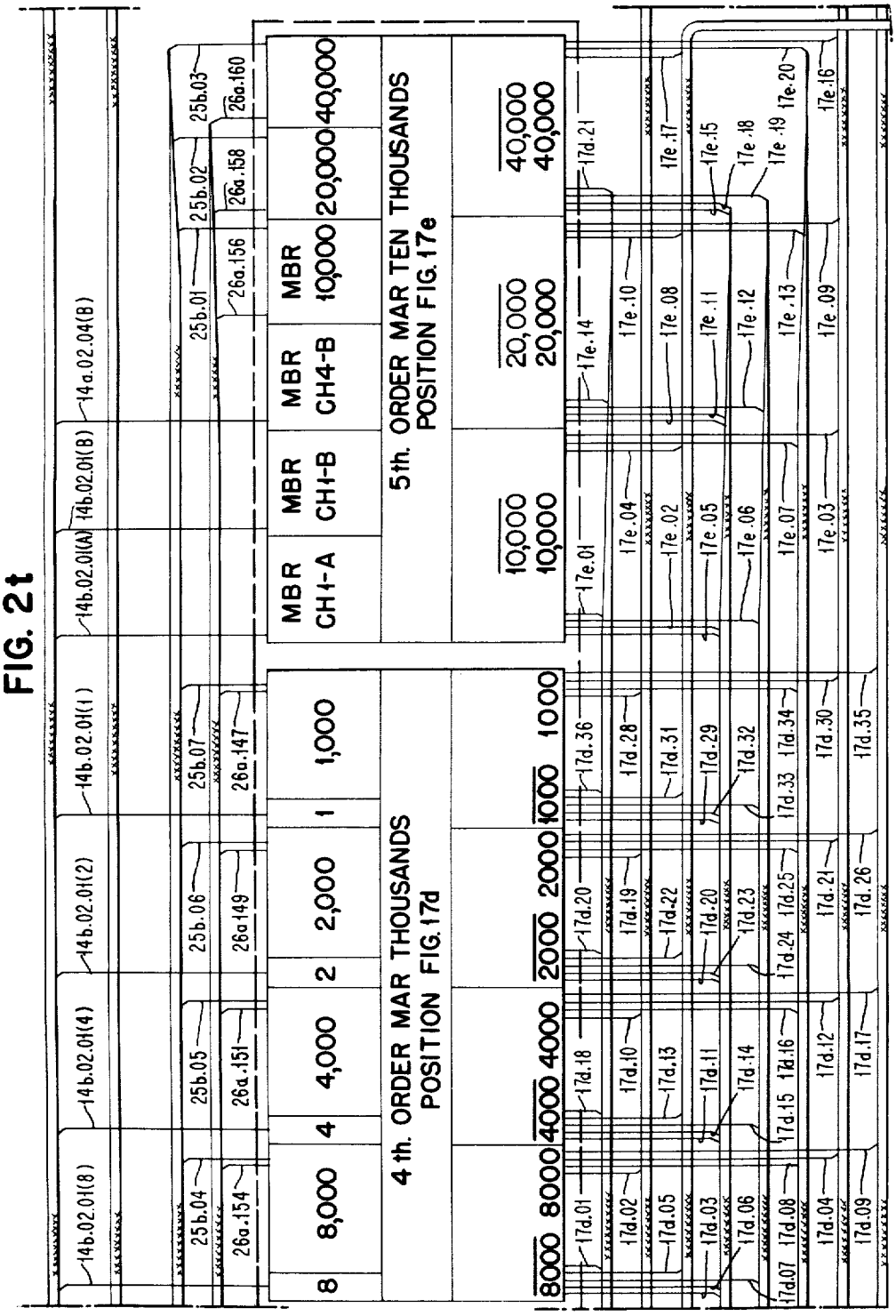
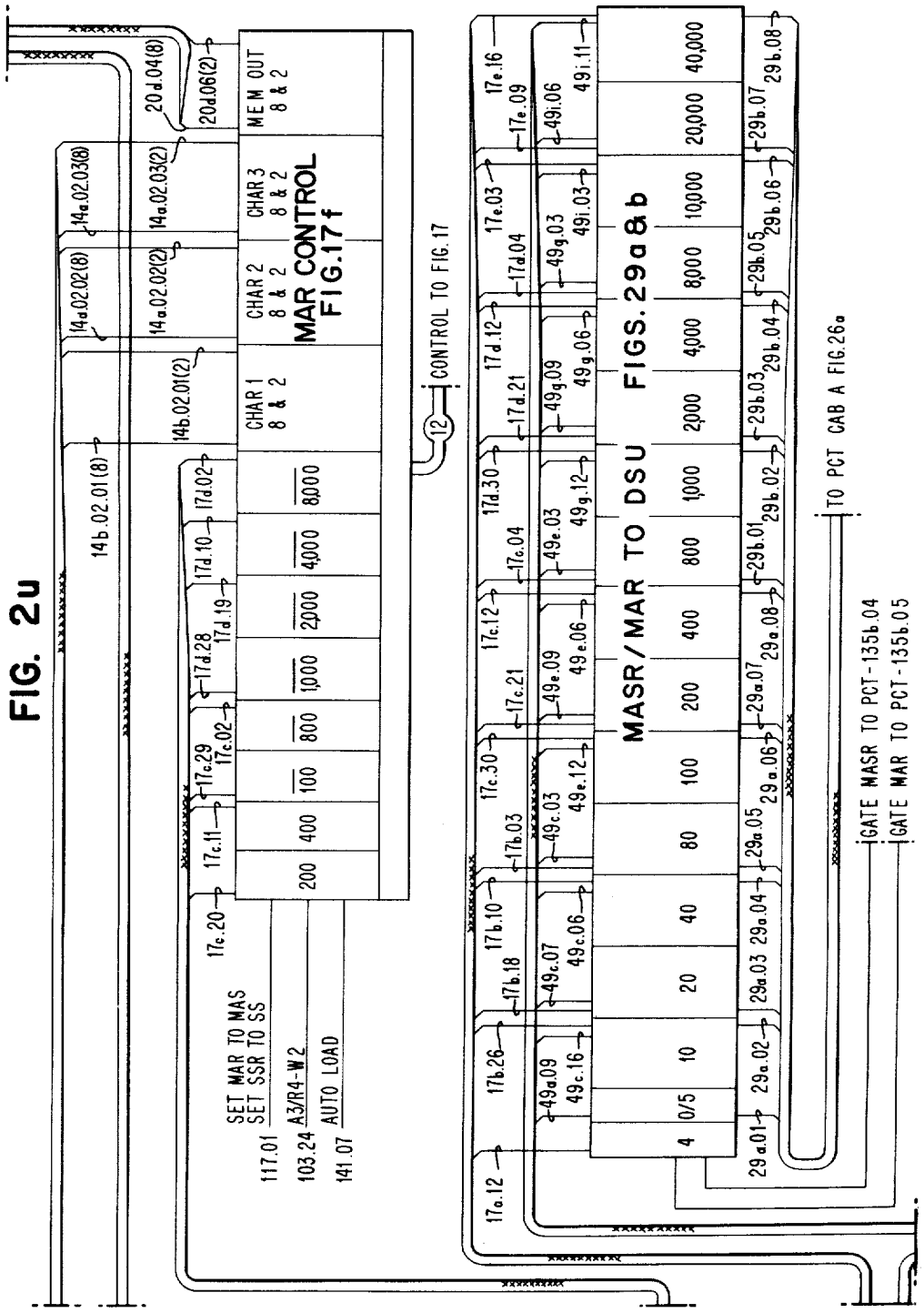

14b.02.01(8)
14b.02.01(4)
14b.02.01(2)
14b.02.01(1)
14b.02.01(A)
14b.02.01(B)
14a.02.04(B)
25b.04
25b.05
25b.06
25b.07
25b.01
25b.02
25b.03
26a.154
26a.151
26a.149
26a.147
26a.156
26a.158
26a.160
8
8,000
4
4,000
2
2,000
1
1,000
4th. ORDER MAR THOUSANDS POSITION FIG. 17d
MBR CH1-A
MBR CH1-B
MBR CH4-B
MBR 10,000
20,000
40,000
5th. ORDER MAR TEN THOUSANDS POSITION FIG. 17e
8000 8000
4000 4000
2000 2000
1000 1000
10,000 10,000
20,000 20,000
40,000 40,000
17d.01 17d.02 17d.03 17d.04 17d.05 17d.06 17d.07 17d.08 17d.09 17d.10 17d.11 17d.12 17d.13 17d.14 17d.15 17d.16 17d.17 17d.18 17d.19 17d.20 17d.21 17d.22 17d.23 17d.24 17d.25 17d.26 17d.28 17d.29 17d.30 17d.31 17d.32 17d.33 17d.34 17d.35 17d.36
17e.01 17e.02 17e.03 17e.04 17e.05 17e.06 17e.07 17e.08 17e.09 17e.10 17e.11 17e.12 17e.13 17e.14 17e.15 17e.16 17e.17 17e.18 17e.19 17e.20 17d.21

FIG. 2u

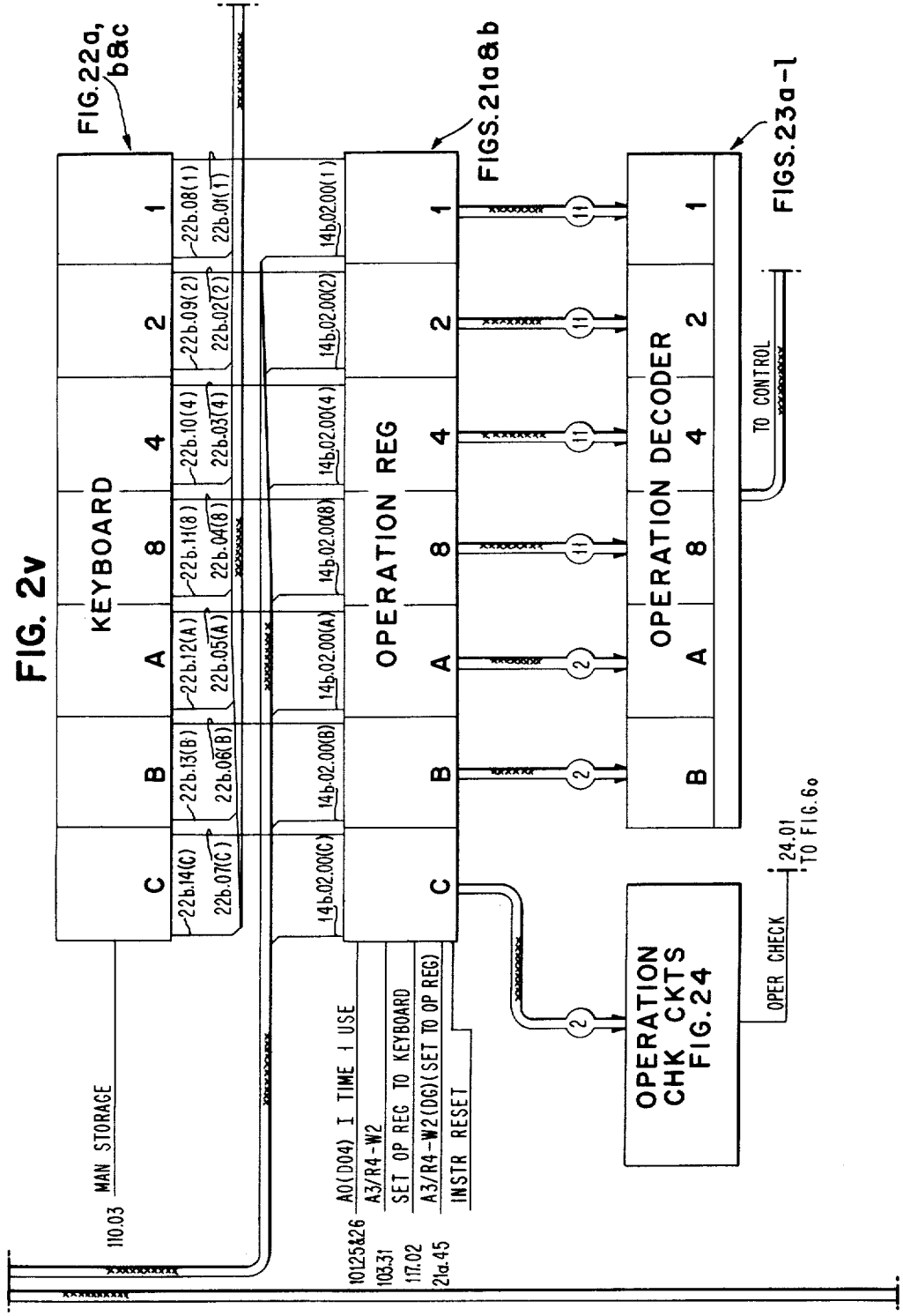

MAR CONTROL FIG.17f
MASR/MAR TO DSU FIGS. 29a & b
CONTROL TO FIG. 17
TO PCT CAB A FIG. 26a
GATE MASR TO PCT-135b.04
GATE MAR TO PCT-135b.05
SET MAR TO MAS
SET SSR TO SS
A3/R4-W2
AUTO LOAD
CHAR 1 & 2
CHAR 2 & 2
CHAR 3 & 2
MEM OUT & 2
200
400
100
800
1000
2000
4000
8000
4
0/5
10
20
40
80
100
200
400
800
1,000
2,000
4,000
8,000
10,000
20,000
40,000

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FIG. 2v



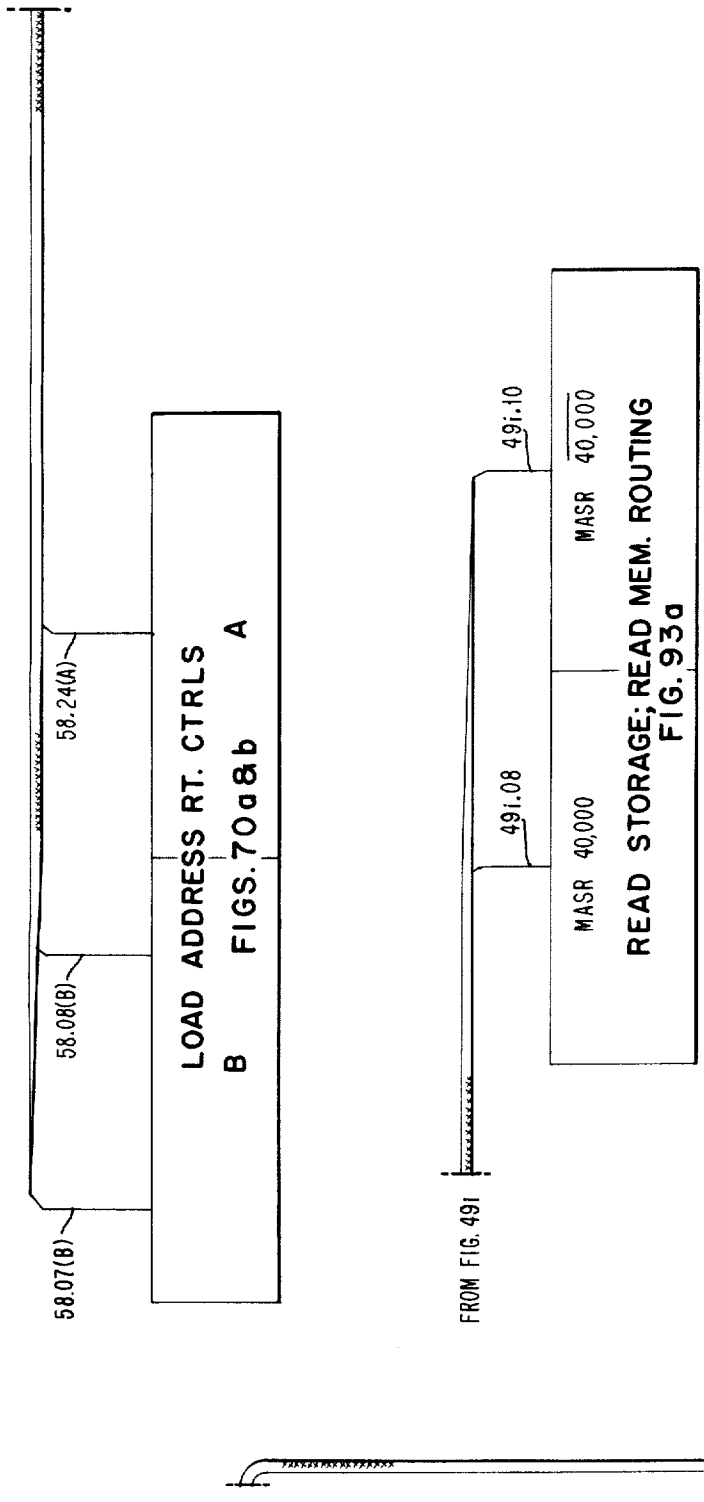

58.07(B)
58.08(B)
58.24(A)
LOAD ADDRESS RT. CTRLS
B FIGS. 70a&b A
FROM FIG. 49i
49i.08
MASR 40,000
49i.10
MASR 40,000
READ STORAGE; READ MEM. ROUTING
FIG. 93a

FIG. 2w

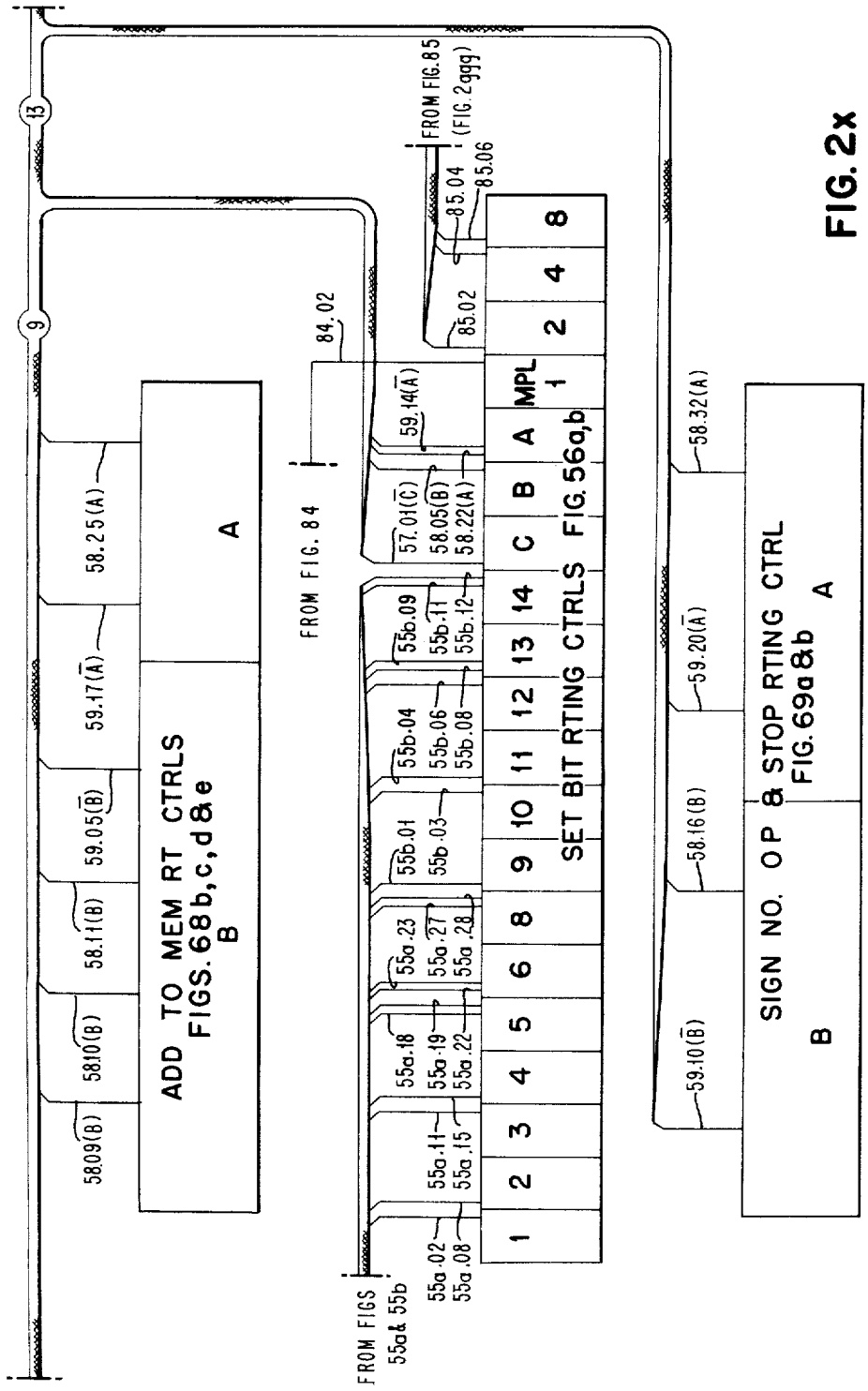

FROM FIG. 85 (FIG. 2qqq)
85.04
85.06
85.02
84.02
FROM FIG. 84
59.14(Ā)
57.01(C̄)
58.05(B̄)
58.22(A)
55b.09
55b.11
55b.12
55b.04
55b.06
55b.08
55b.01
55b.03
55a.23
55a.27
55a.28
55a.18
55a.19
55a.22
55a.11
55a.15
55a.02
55a.08
FROM FIGS 55a & 55b
SET BIT RTING CTRLS FIG. 56a,b
1 2 3 4 5 6 8 9 10 11 12 13 14 C B A MPL 1 2 4 8
ADD TO MEM RT CTRLS FIGS. 68b,c,d & e
B
A
58.25(A)
59.17(Ā)
59.05(B̄)
58.11(B)
58.10(B)
58.09(B)
SIGN NO. OP & STOP RTING CTRL FIG. 69a & b
B
A
58.32(A)
59.20(Ā)
58.16(B)
59.10(B̄)
13
9

FIG. 2x

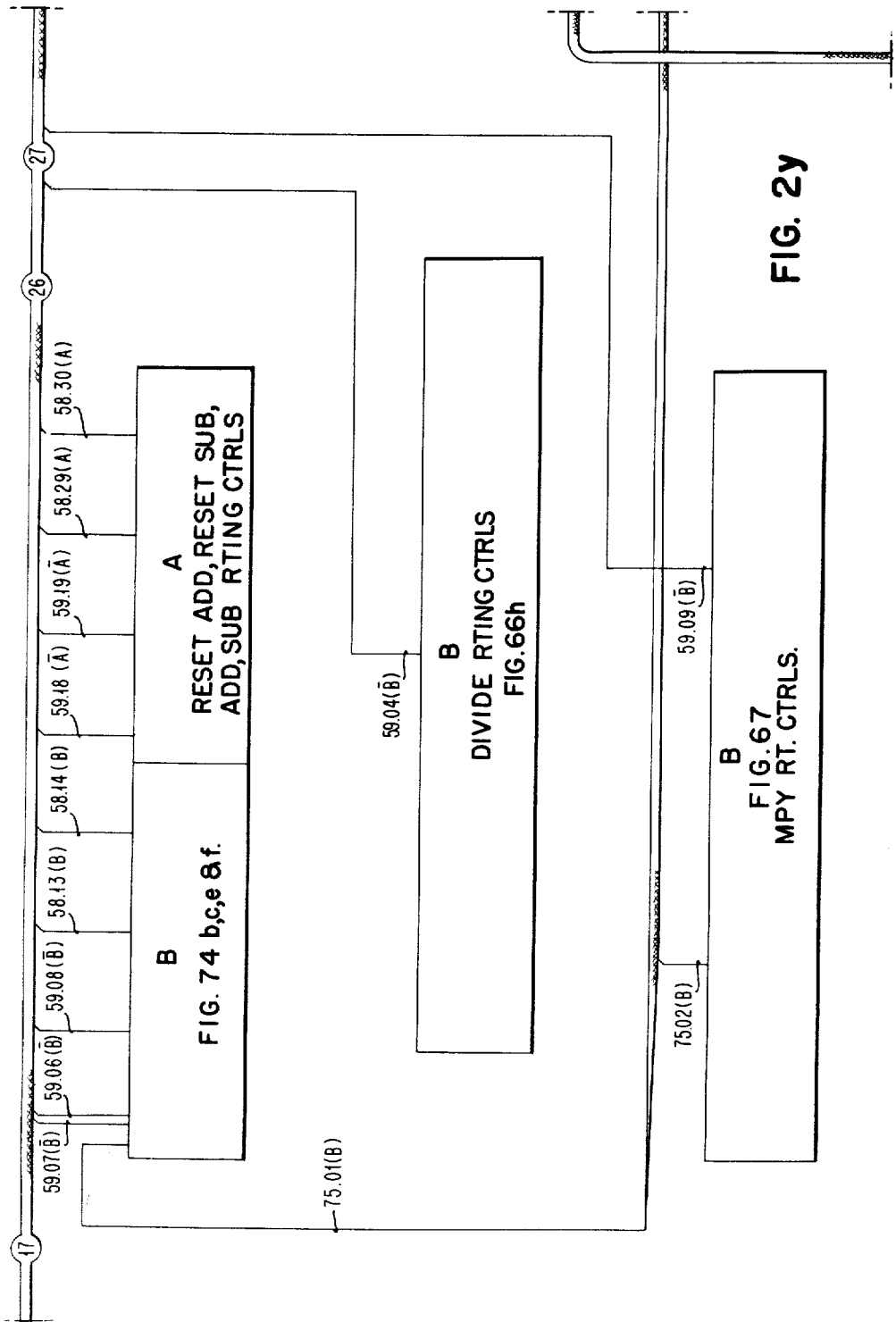
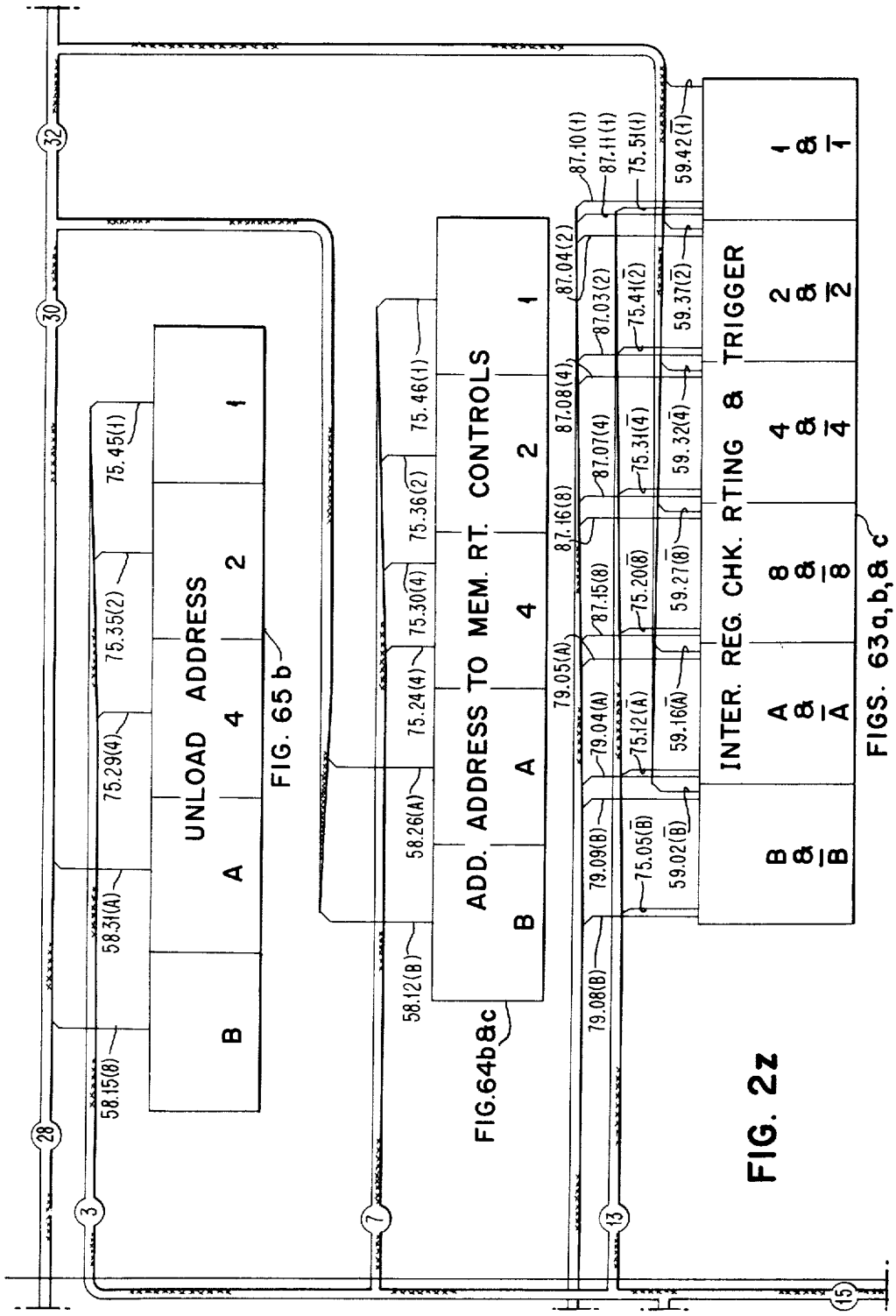

27
26
17
58.30(A)
58.29(A)
59.19(Ā)
59.18(Ā)
58.14(B)
58.13(B)
59.08(B̄)
59.06(B̄)
59.07(B̄)
A
RESET ADD, RESET SUB, ADD, SUB RTING CTRLS
B
FIG. 74 b,c,e & f.
75.01(B)
59.04(B̄)
B
DIVIDE RTING CTRLS
FIG. 66h
59.09(B̄)
75.02(B)
B
FIG. 67
MPY RT. CTRLS.

FIG. 2y


UNLOAD ADDRESS
A
B
4
2
1
ADD. ADDRESS TO MEM. RT. CONTROLS
A
B
4
2
1
INTER. REG. CHK. RTING & TRIGGER
A & Ā
B & B̄
8 & 8̄
4 & 4̄
2 & 2̄
1 & 1̄
75.45(1)
75.35(2)
75.29(4)
58.31(A)
58.15(8)
75.46(1)
75.36(2)
75.30(4)
75.24(4)
58.26(A)
58.12(B)
87.10(1)
87.11(1)
75.51(1)
59.42(1̄)
87.04(2)
87.03(2)
75.41(2̄)
59.37(2̄)
87.08(4)
87.07(4)
75.31(4̄)
59.32(4̄)
87.16(8)
87.15(8)
75.20(8̄)
59.27(8̄)
79.05(A)
79.04(A)
75.12(Ā)
59.16(Ā)
79.09(B)
75.05(B̄)
59.02(B̄)
79.08(B)
FIG. 65 b
FIG.64b&c
FIGS. 63a,b,& c
FIG. 2z
32
30
28
3
7
13
15

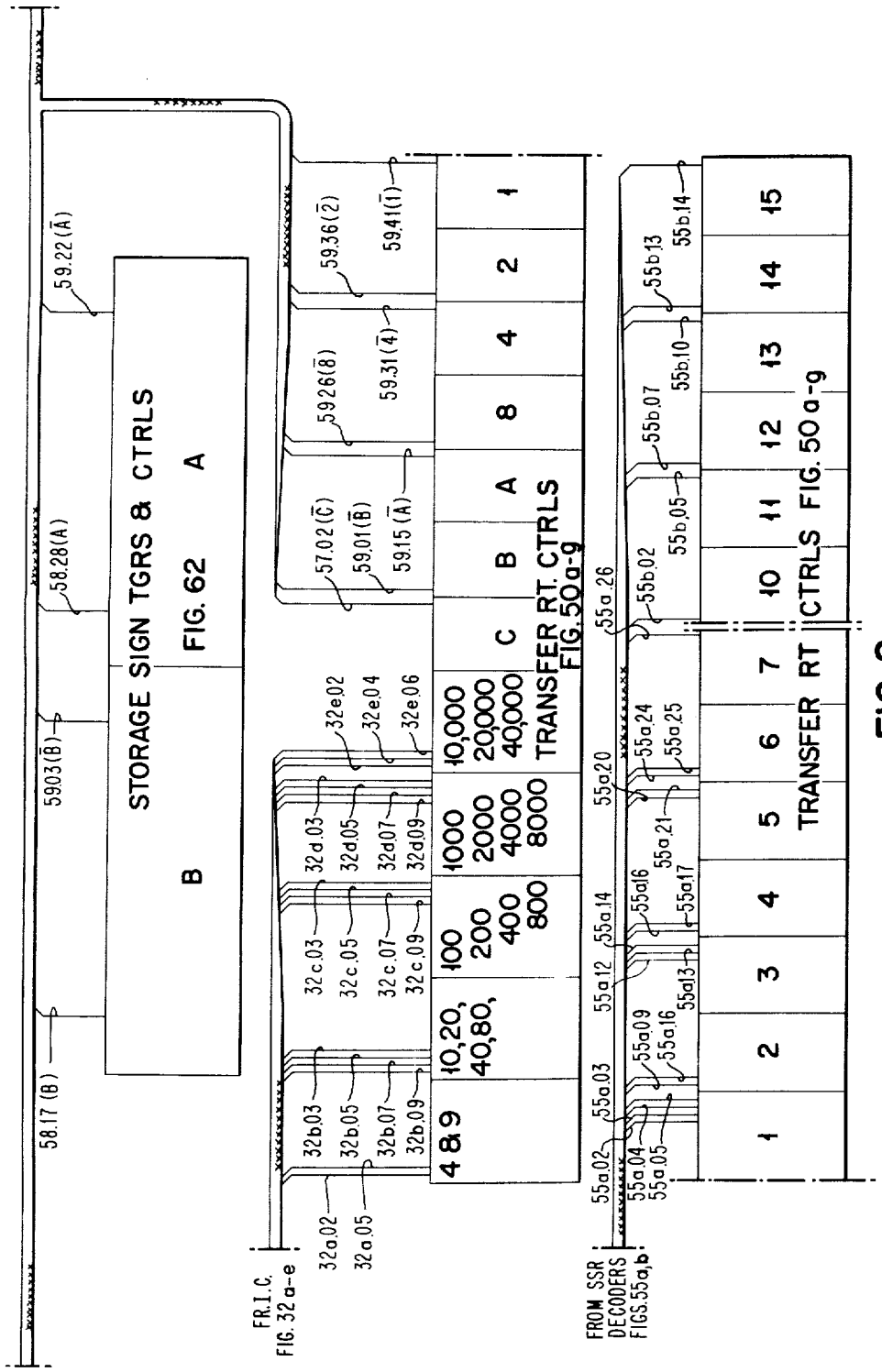

STORAGE SIGN TGRS & CTRLS
A
B
FIG. 62
59.22(Ā)
58.28(A)
5903(B̄)
58.17 (B)
59.41(1̄)
59.36(2̄)
59.31(4̄)
59.26(8̄)
59.15 (Ā)
59.01(B̄)
57.02(C̄)
TRANSFER RT. CTRLS FIG. 50a-g
1 2 4 8 A B C
10,000 20,000 40,000
1000 2000 4000 8000
100 200 400 800
10,20, 40,80,
4 8 9
32e.02 32e.04 32e.06
32d.03 32d.05 32d.07 32d.09
32c.03 32c.05 32c.07 32c.09
32b.03 32b.05 32b.07 32b.09
32a.02 32a.05
FR.I.C. FIG. 32a-e
55a.26 55a.20 55a.14 55a.12 55a.03 55a.02
55a.24 55a.25 55a.21 55a16 55a17 55a13 55a.09 55a.16 55a.04 55a.05
FROM SSR DECODERS FIGS. 55a,b
55b.14 55b13 55b.10 55b.07 55b.05 55b.02
1 2 3 4 5 6 7 10 11 12 13 14 15
TRANSFER RT CTRLS FIG. 50a-g

FIG. 2aa

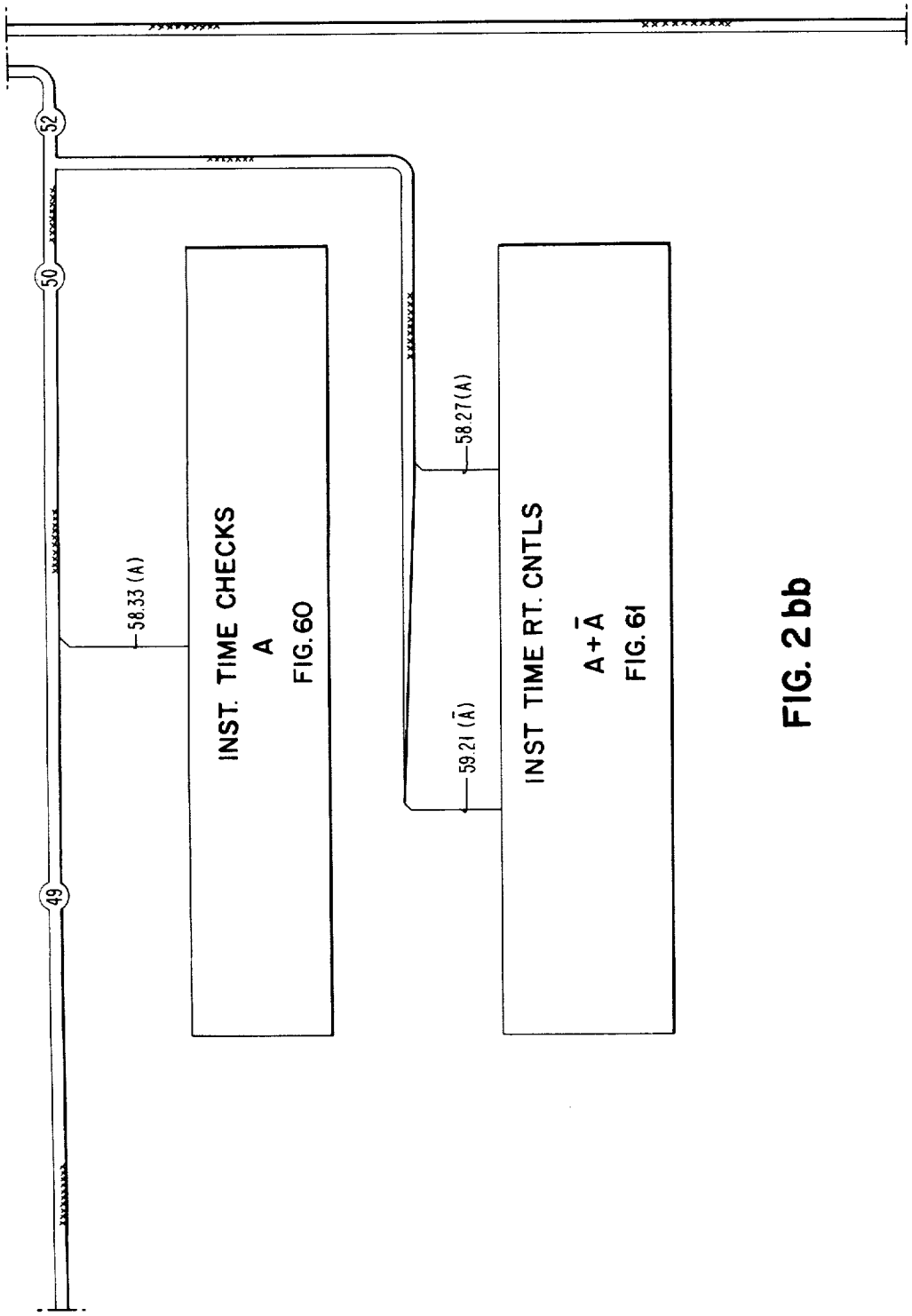

52
50
49
58.33 (A)
INST. TIME CHECKS
A
FIG. 60
58.27 (A)
59.21 (Ā)
INST TIME RT. CNTLS
A+Ā
FIG. 61

FIG. 2bb

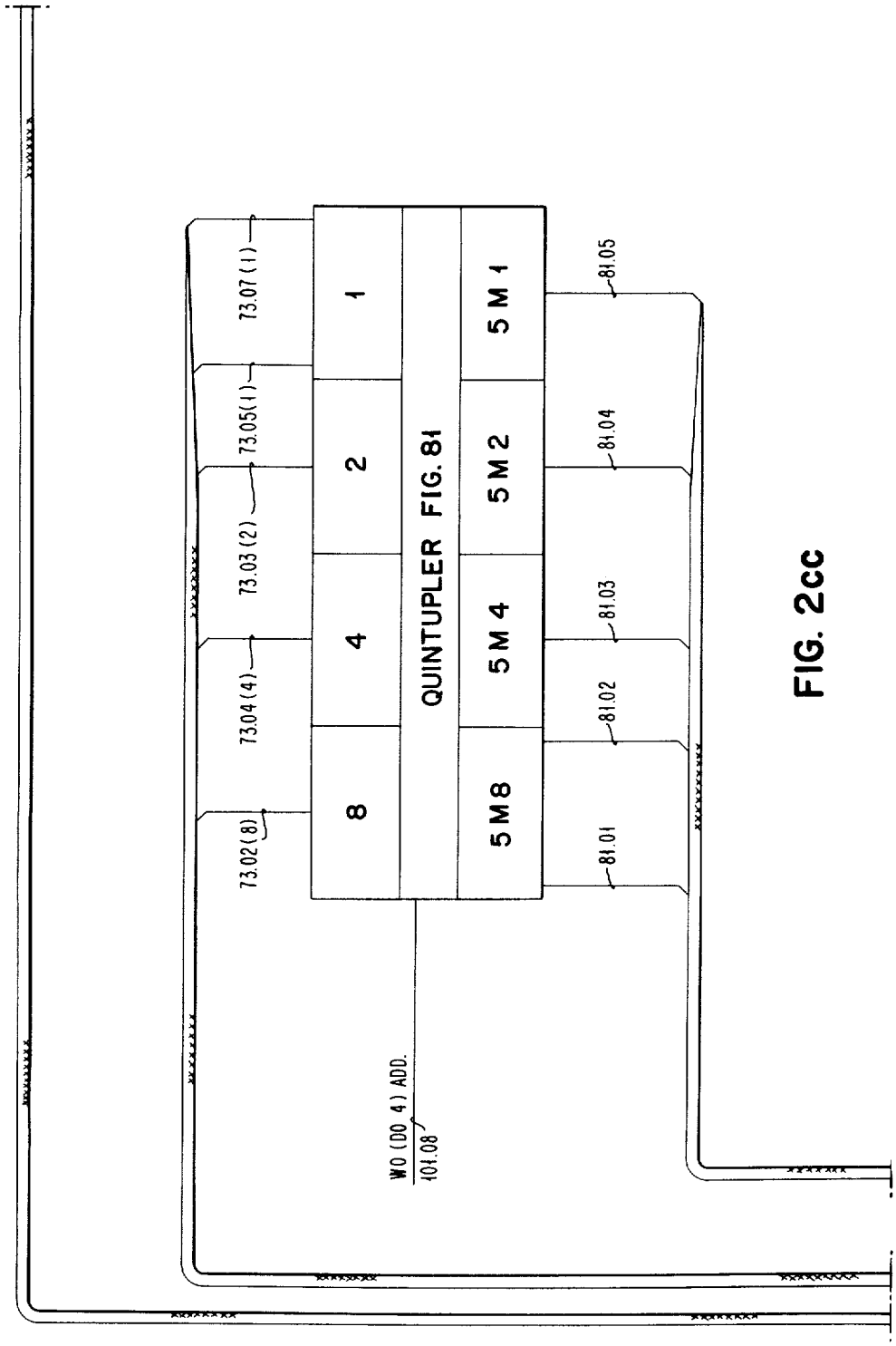

QUINTUPLER FIG. 81
1
2
4
8
5M1
5M2
5M4
5M8
73.07(1)
73.05(1)
73.03(2)
73.04(4)
73.02(8)
81.05
81.04
81.03
81.02
81.01
WO (DO 4) ADD.
101.08

FIG. 2cc

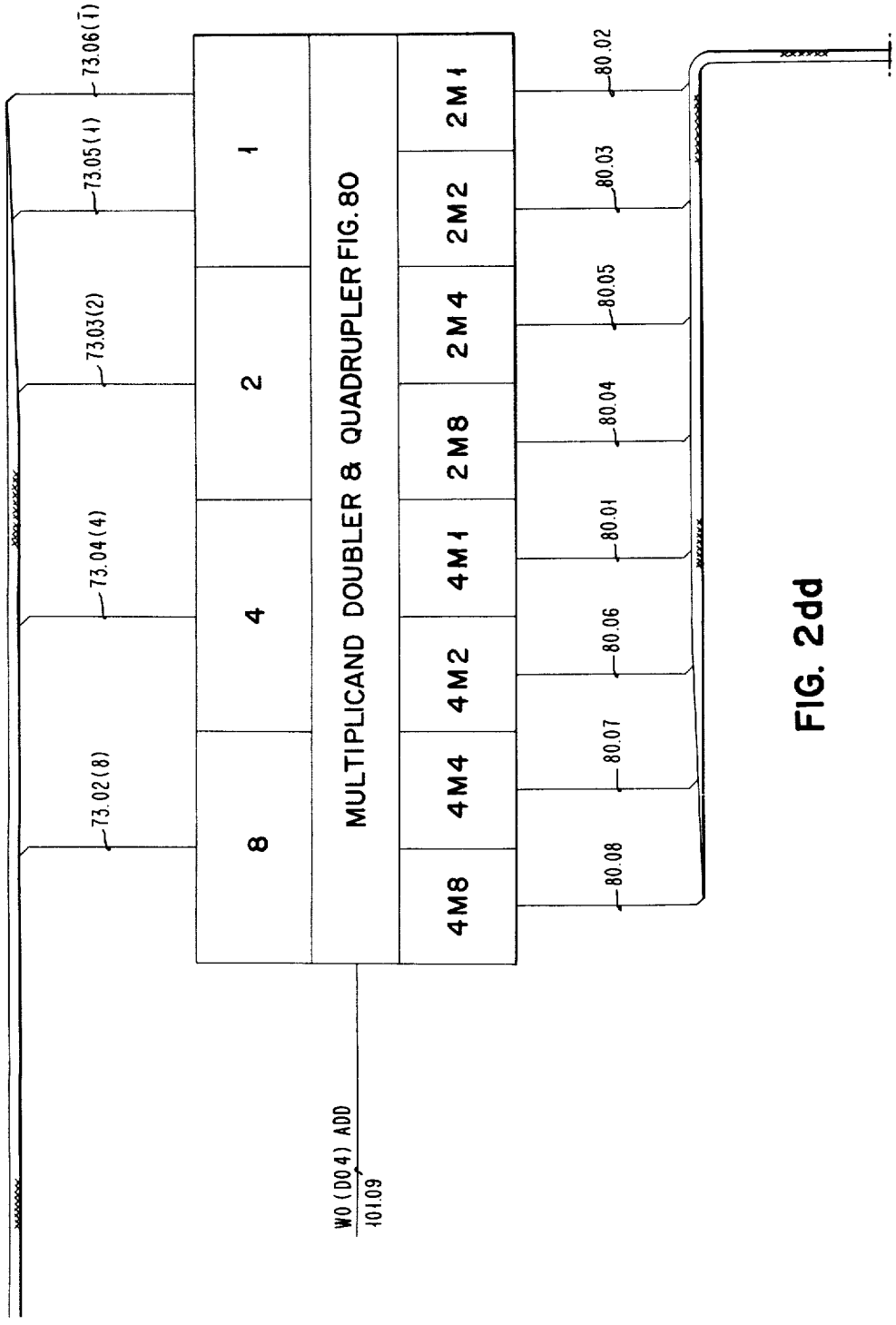
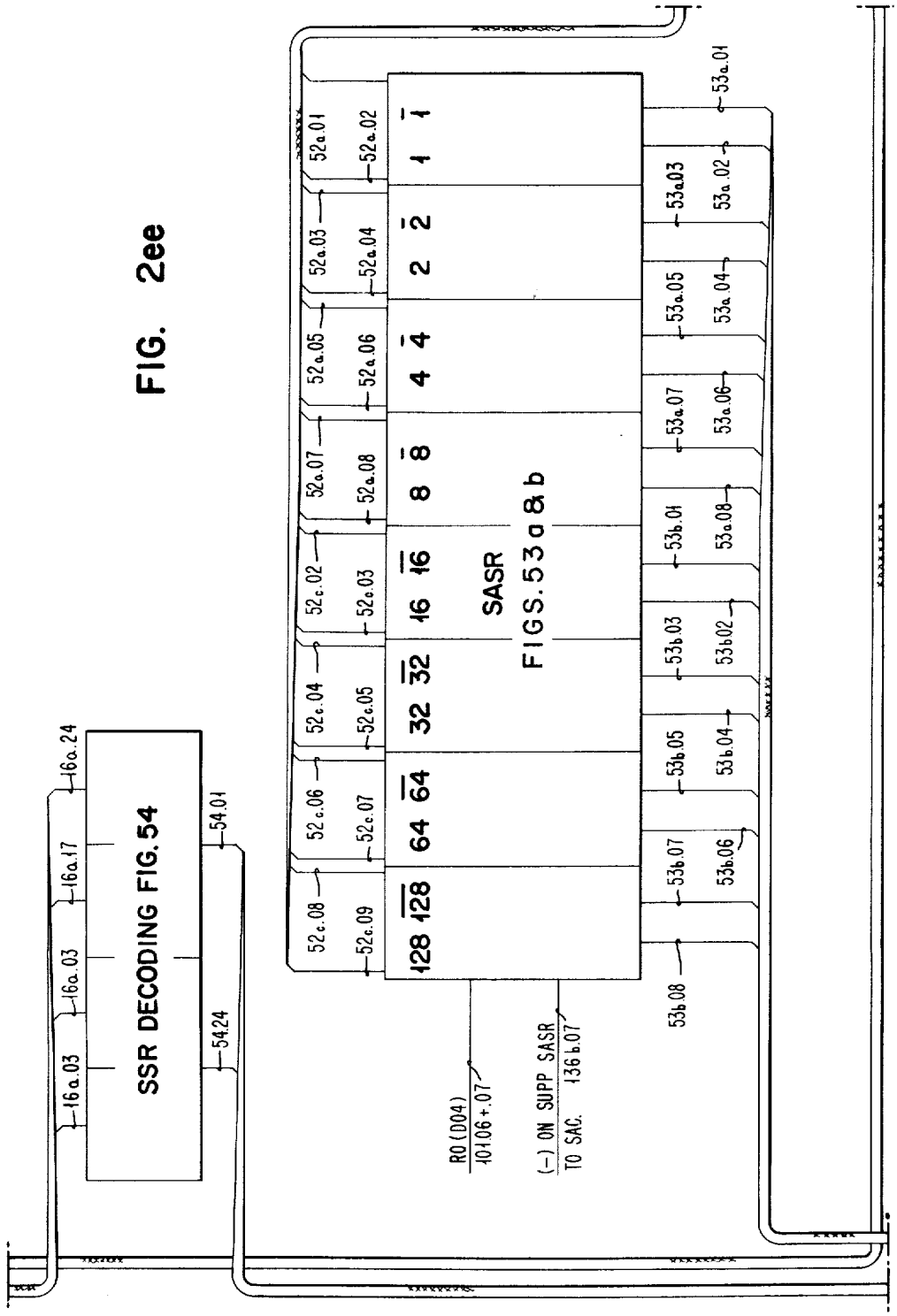

73.06(1)
73.05(1)
73.03(2)
73.04(4)
73.02(8)
1
2
4
8
MULTIPLICAND DOUBLER & QUADRUPLER FIG. 80
2M1
2M2
2M4
2M8
4M1
4M2
4M4
4M8
80.02
80.03
80.05
80.04
80.01
80.06
80.07
80.08
WO(004) ADD
101.09

FIG. 2dd

FIG. 2ee


SSR DECODING FIG. 54
16a.24
16a.17
16a.03
16a.03
54.01
54.24
SASR
FIGS. 53a & b
1 1
2 2
4 4
8 8
16 16
32 32
64 64
128 128
52a.01
52a.02
52a.03
52a.04
52a.05
52a.06
52a.07
52a.08
52a.02
52a.03
52a.04
52a.05
52a.06
52a.07
52a.08
52a.09
53a.01
53a.02
53a.03
53a.04
53a.05
53a.06
53a.07
53a.08
53b.01
53b02
53b.03
53b.04
53b.05
53b.06
53b.07
53b.08
RO(D04)
10106+.07
(-) ON SUPP SASR
TO SAC. 136b.07

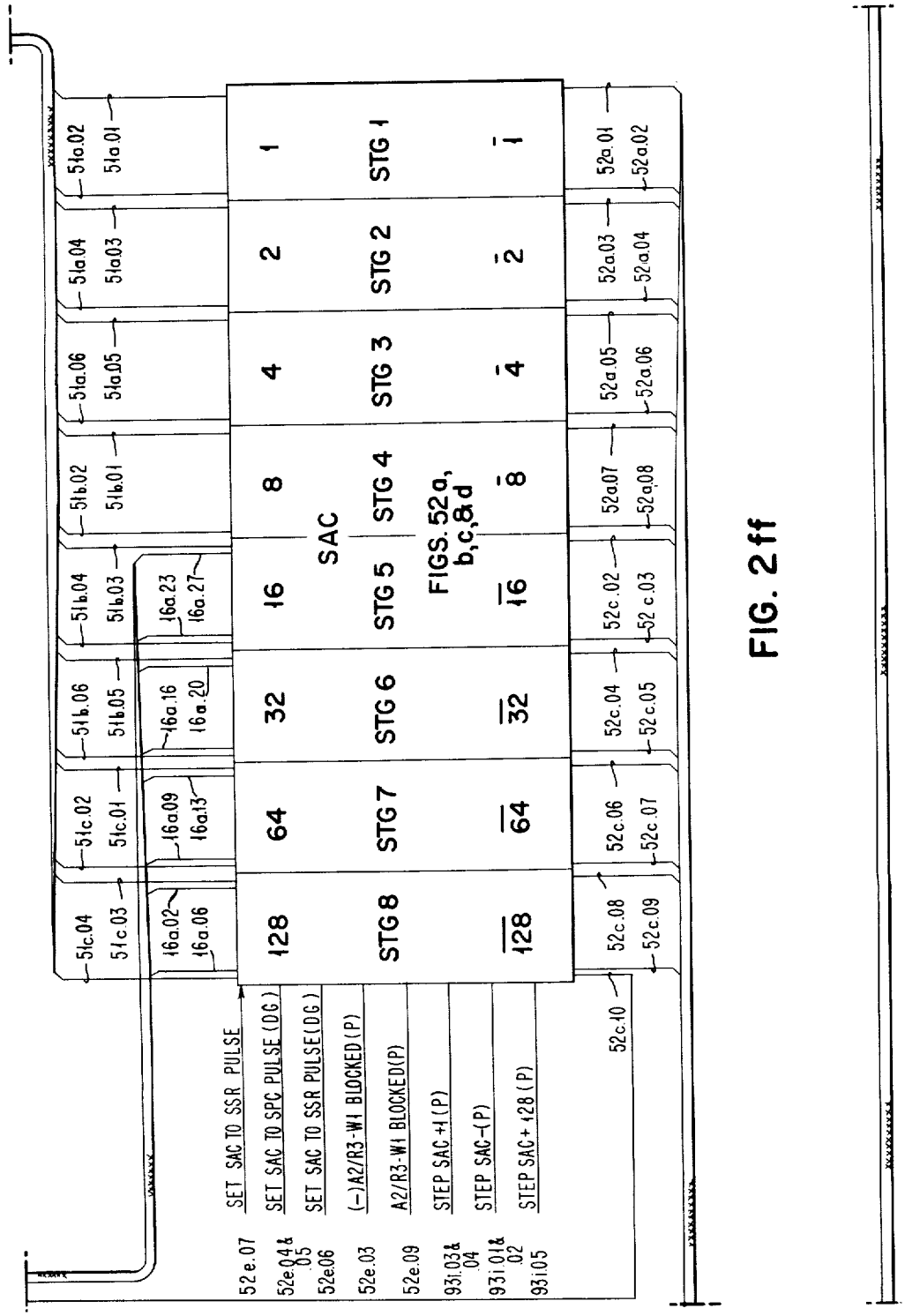

SAC
FIGS. 52a, b,c,&d
STG 1
STG 2
STG 3
STG 4
STG 5
STG 6
STG 7
STG 8
1
2
4
8
16
32
64
128
SET SAC TO SSR PULSE
SET SAC TO SPC PULSE (DG)
SET SAC TO SSR PULSE(DG)
(-)A2/R3-W1 BLOCKED(P)
A2/R3-W1 BLOCKED(P)
STEP SAC+1(P)
STEP SAC-(P)
STEP SAC+128(P)

FIG. 2ff

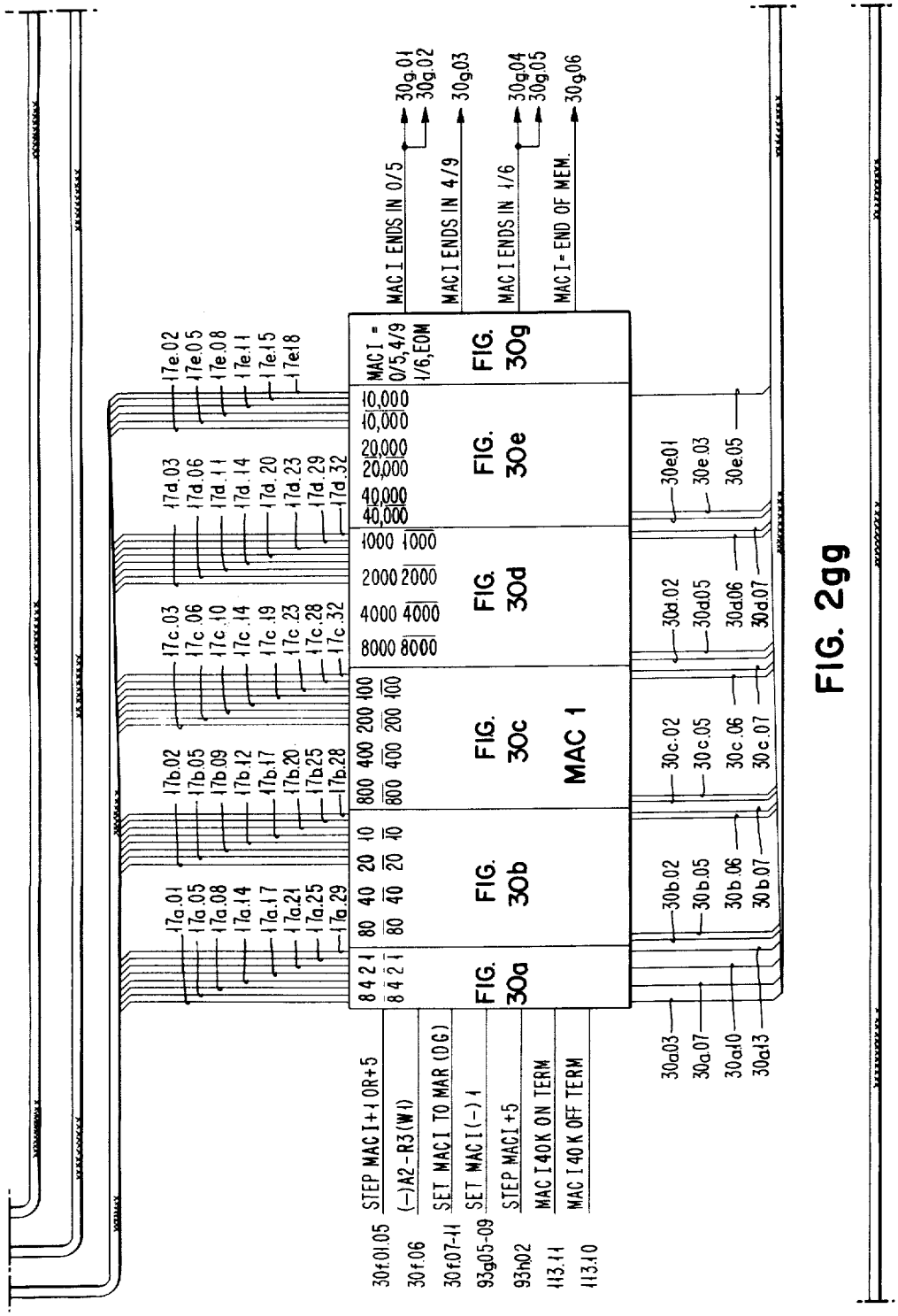

MAC I ENDS IN 0/5
MAC I ENDS IN 4/9
MAC I ENDS IN 1/6
MAC I = END OF MEM.
MAC I = 0/5,4/9 1/6,EOM
FIG. 30g
FIG. 30e
FIG. 30d
FIG. 30c
FIG. 30b
FIG. 30a
MAC 1
STEP MAC I+1 OR+5
(-)A2-R3 (W1)
SET MAC I TO MAR (OC)
SET MAC I(-)1
STEP MAC I+5
MAC I 40 K ON TERM
MAC I 40 K OFF TERM

FIG. 2gg

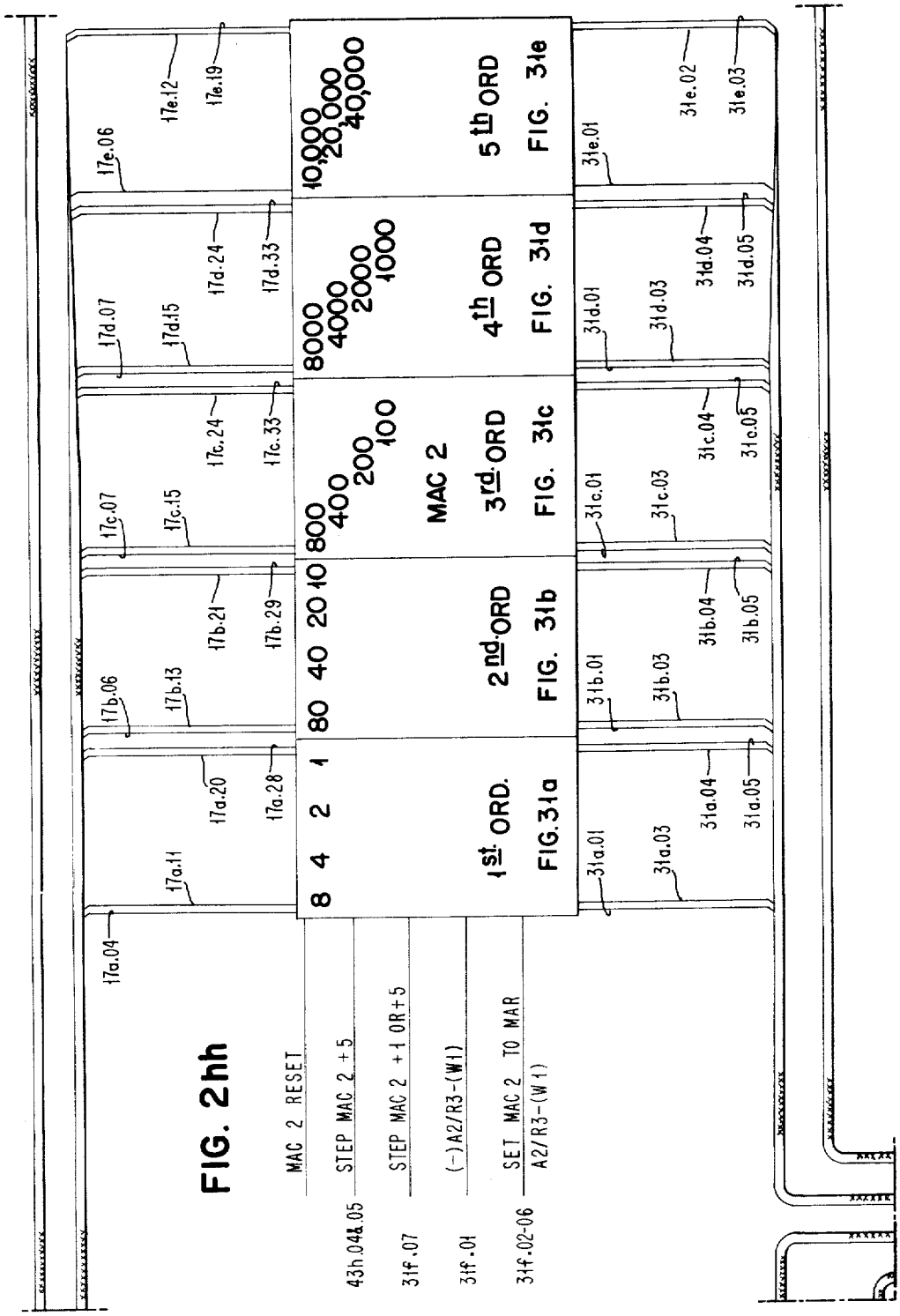

8 4 2 1
80 40 20 10
800 400 200 100
8000 4000 2000 1000
10,000 20,000 40,000
1st ORD. FIG. 31a
2nd ORD FIG. 31b
MAC 2
3rd ORD FIG. 31c
4th ORD FIG. 31d
5th ORD FIG. 31e
MAC 2 RESET
STEP MAC 2 +5
STEP MAC 2 +1 OR+5
(-)A2/R3-(W1)
SET MAC 2 TO MAR
A2/R3-(W1)
43h.04&.05
31f.07
31f.01
31f.02-06
17a.04
17a.11
17a.20
17a.28
17b.06
17b.13
17b.21
17b.29
17c.07
17c.15
17c.24
17c.33
17d.07
17d.15
17d.24
17d.33
17e.06
17e.12
17e.19
31a.01
31a.03
31a.04
31a.05
31b.01
31b.03
31b.04
31b.05
31c.01
31c.03
31c.04
31c.05
31d.01
31d.03
31d.04
31d.05
31e.01
31e.02
31e.03

FIG. 2hh

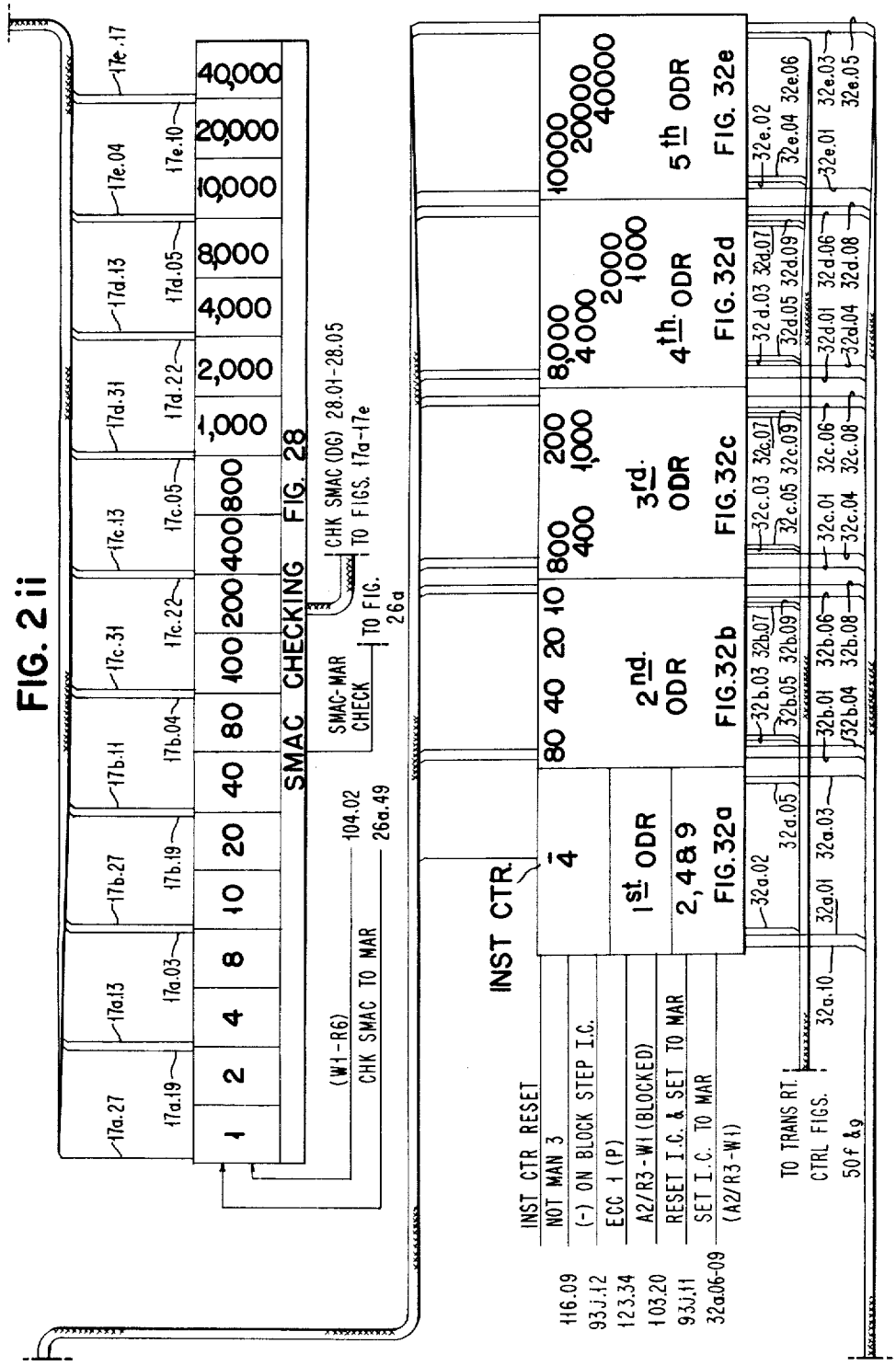

FIG. 2ii
SMAC CHECKING FIG. 28
1 2 4 8 10 20 40 80 100 200 400 800 1,000 2,000 4,000 8,000 10,000 20,000 40,000
17a.27 17a.19 17a.13 17a.03 17b.27 17b.19 17b.11 17b.04 17c.31 17c.22 17c.13 17c.05 17d.31 17d.22 17d.13 17d.05 17e.04 17e.10 17e.17
(W1-RG)
CHK SMAC TO MAR
104.02
26a.49
SMAC-MAR CHECK
CHK SMAC (DG) 28.01-28.05
TO FIGS. 17a-17e
TO FIG. 26a
INST CTR.
INST CTR RESET
NOT MAN 3
(-) ON BLOCK STEP I.C.
ECC 1 (P)
A2/R3-W1 (BLOCKED)
RESET I.C. & SET TO MAR
SET I.C. TO MAR
(A2/R3-W1)
116.09
93J.12
123.34
103.20
93J.11
32a.06-09
4
1st ODR
2,4&9
FIG. 32a
80 40 20 10
800 400
200 1,000
8,000 4,000 2,000 1000
10000 20000 40000
2nd. ODR
3rd. ODR
4th. ODR
5th ODR
FIG. 32b
FIG. 32c
FIG. 32d
FIG. 32e
32a.02 32a.05 32a.10 32a.01 32a.03
32b.03 32b.07 32b.05 32b.09 32b.01 32b.06 32b.04 32b.08
32c.03 32c.07 32c.05 32c.09 32c.01 32c.06 32c.04 32c.08
32d.03 32d.07 32d.05 32d.09 32d.01 32d.06 32d.04 32d.08
32e.02 32e.04 32e.06 32e.01 32e.03 32e.05
TO TRANS RT.
CTRL FIGS.
50f &9

FIG. 2jj

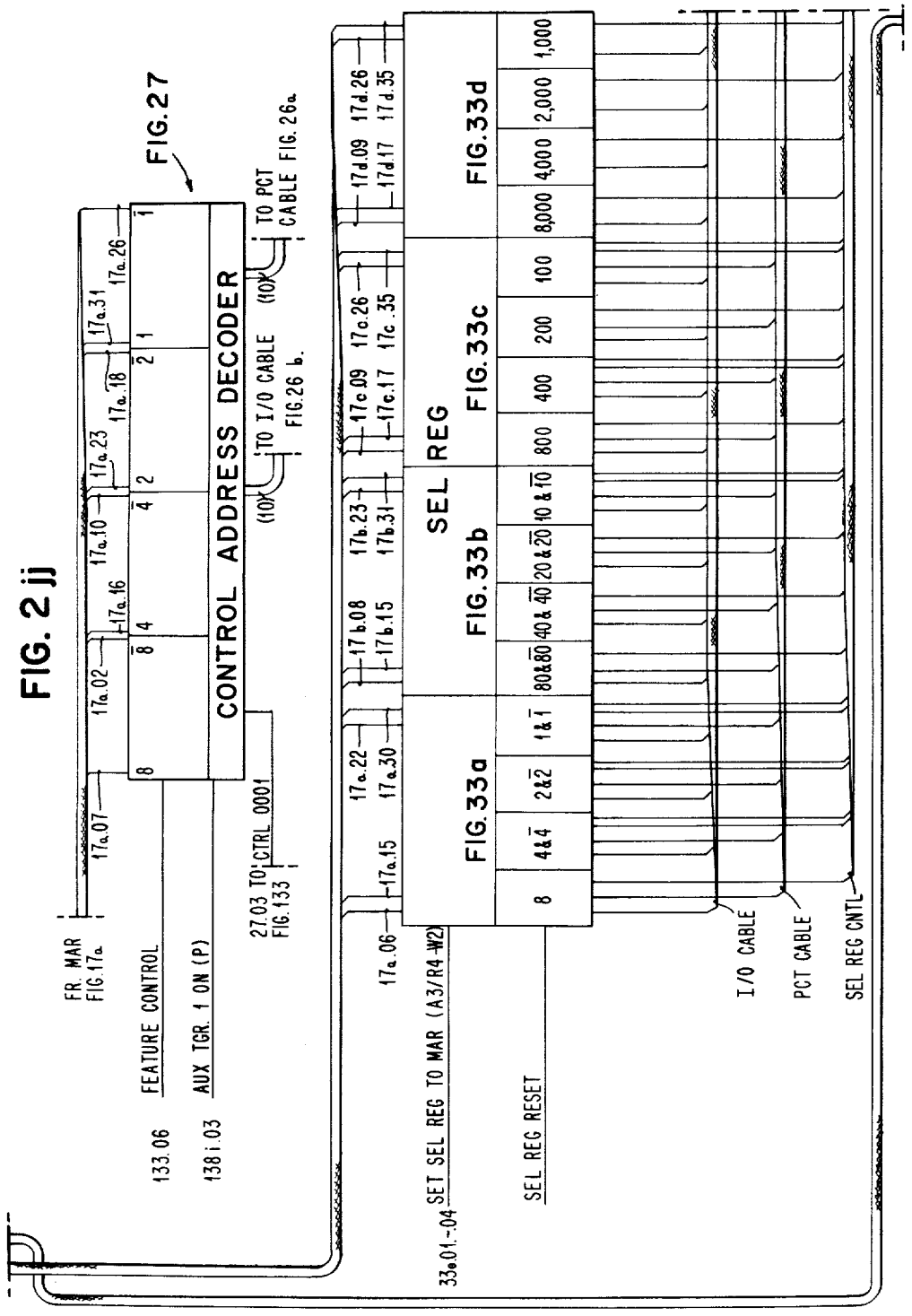

FIG.27
CONTROL ADDRESS DECODER
FIG.33a
FIG.33b
SEL REG
FIG.33c
FIG.33d
TO PCT CABLE FIG.26a
TO I/O CABLE (10X) FIG.26 b.
FR. MAR FIG.17a
FEATURE CONTROL
AUX TGR. 1 ON (P)
CTRL 0001
27.03 TO FIG.133
SET SEL REG TO MAR (A3/R4 W2)
SEL REG RESET
I/O CABLE
PCT CABLE
SEL REG CNTL

FIG. 2kk

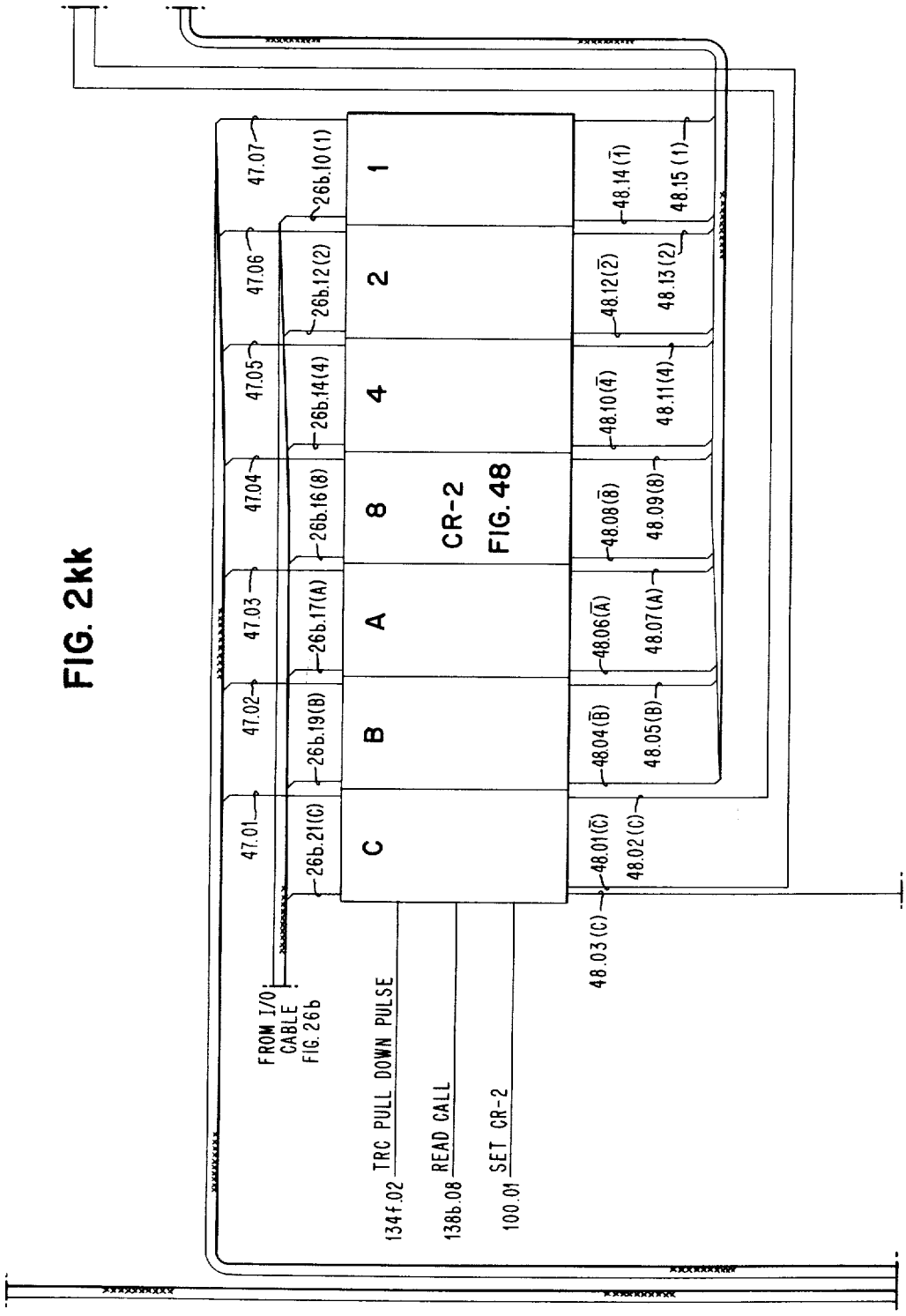

CR-2
FIG. 48
1
2
4
8
A
B
C
47.07
47.06
47.05
47.04
47.03
47.02
47.01
26b.10(1)
26b.12(2)
26b.14(4)
26b.16(8)
26b.17(A)
26b.19(B)
26b.21(C)
48.14(1̄)
48.12(2̄)
48.10(4̄)
48.08(8̄)
48.06(Ā)
48.04(B̄)
48.01(C̄)
48.15(1)
48.13(2)
48.11(4)
48.09(8)
48.07(A)
48.05(B)
48.02(C)
48.03(C)
FROM I/O CABLE FIG. 26b
134f.02 TRC PULL DOWN PULSE
138b.08 READ CALL
100.01 SET CR-2

FIG. 211

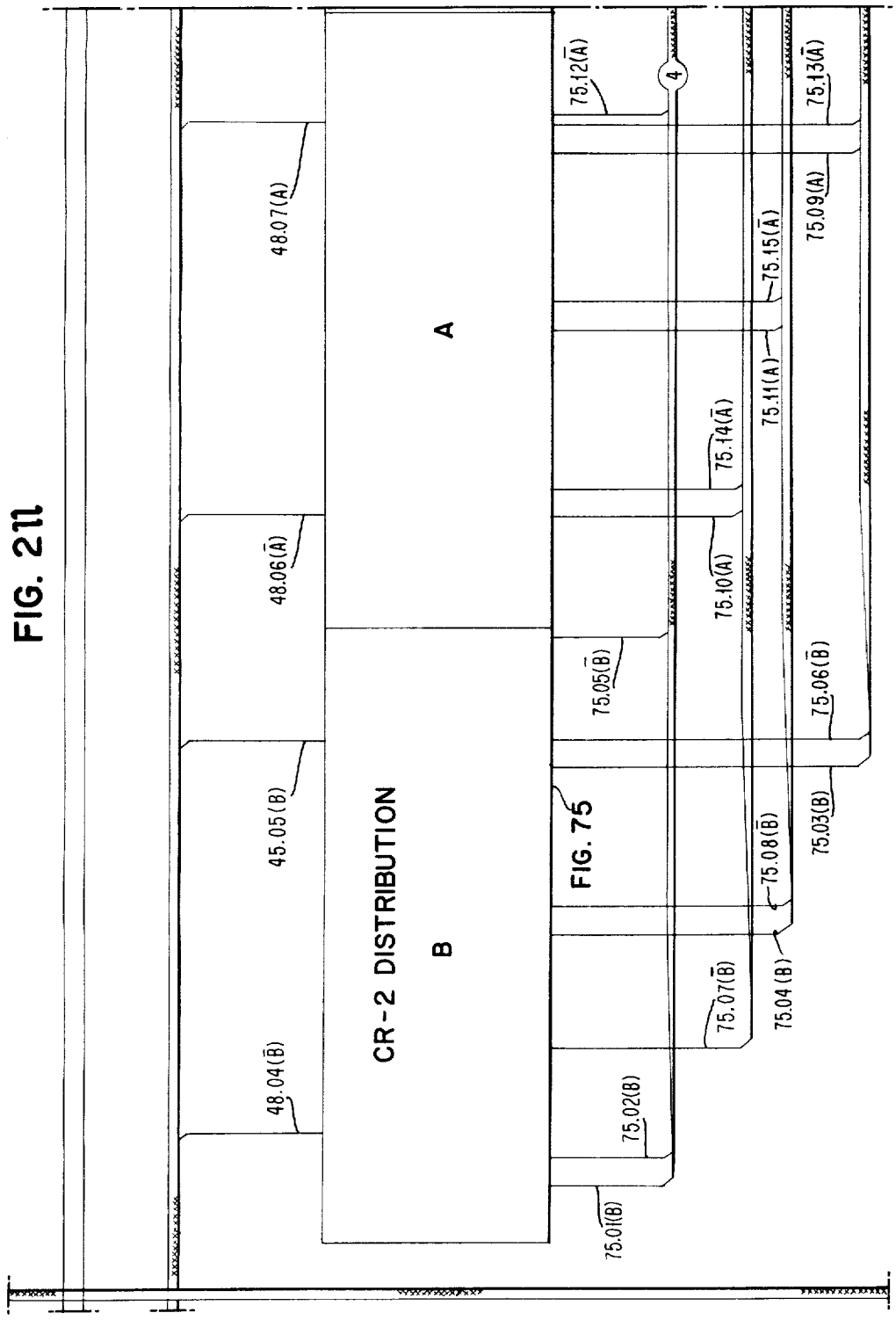
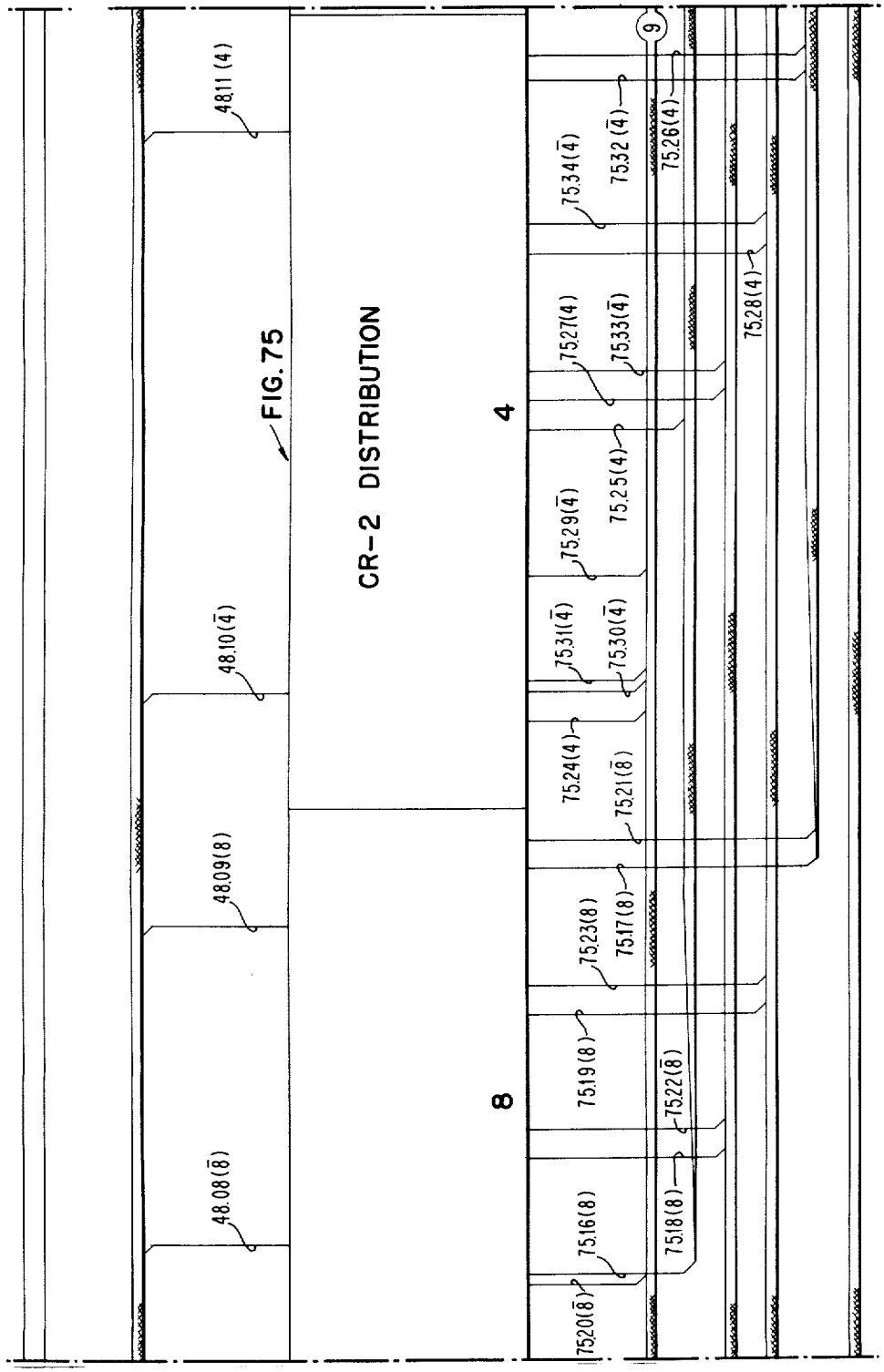

48.07(A)
48.06(Ā)
45.05(B)
48.04(B̄)
A
CR-2 DISTRIBUTION
B
FIG. 75
75.12(Ā)
4
75.13(Ā)
75.09(A)
75.15(Ā)
75.11(A)
75.14(Ā)
75.10(A)
75.05(B̄)
75.06(B̄)
75.03(B)
75.08(B̄)
75.04(B)
75.07(B̄)
75.02(B)
75.01(B)

FIG. 2mm

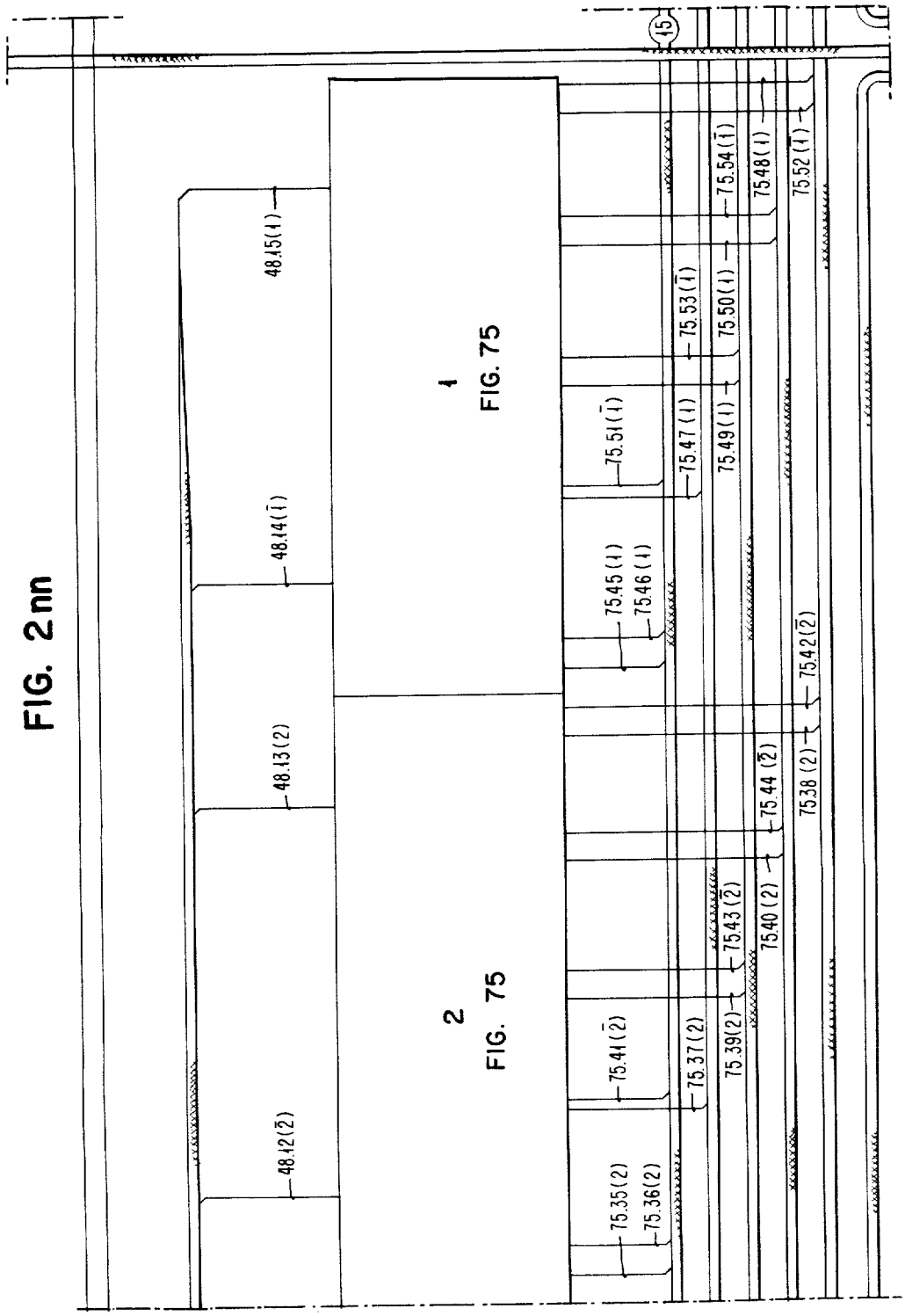

FIG. 75
CR-2 DISTRIBUTION
4
8
9
48.11(4)
48.10(4̄)
48.09(8)
48.08(8̄)
75.16(8)
75.17(8)
75.18(8)
75.19(8)
75.20(8̄)
75.21(8̄)
75.22(8̄)
75.23(8)
75.24(4)
75.25(4)
75.26(4)
75.27(4)
75.28(4)
75.29(4̄)
75.30(4̄)
75.31(4̄)
75.32(4̄)
75.33(4̄)
75.34(4̄)

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FIG. 2nn



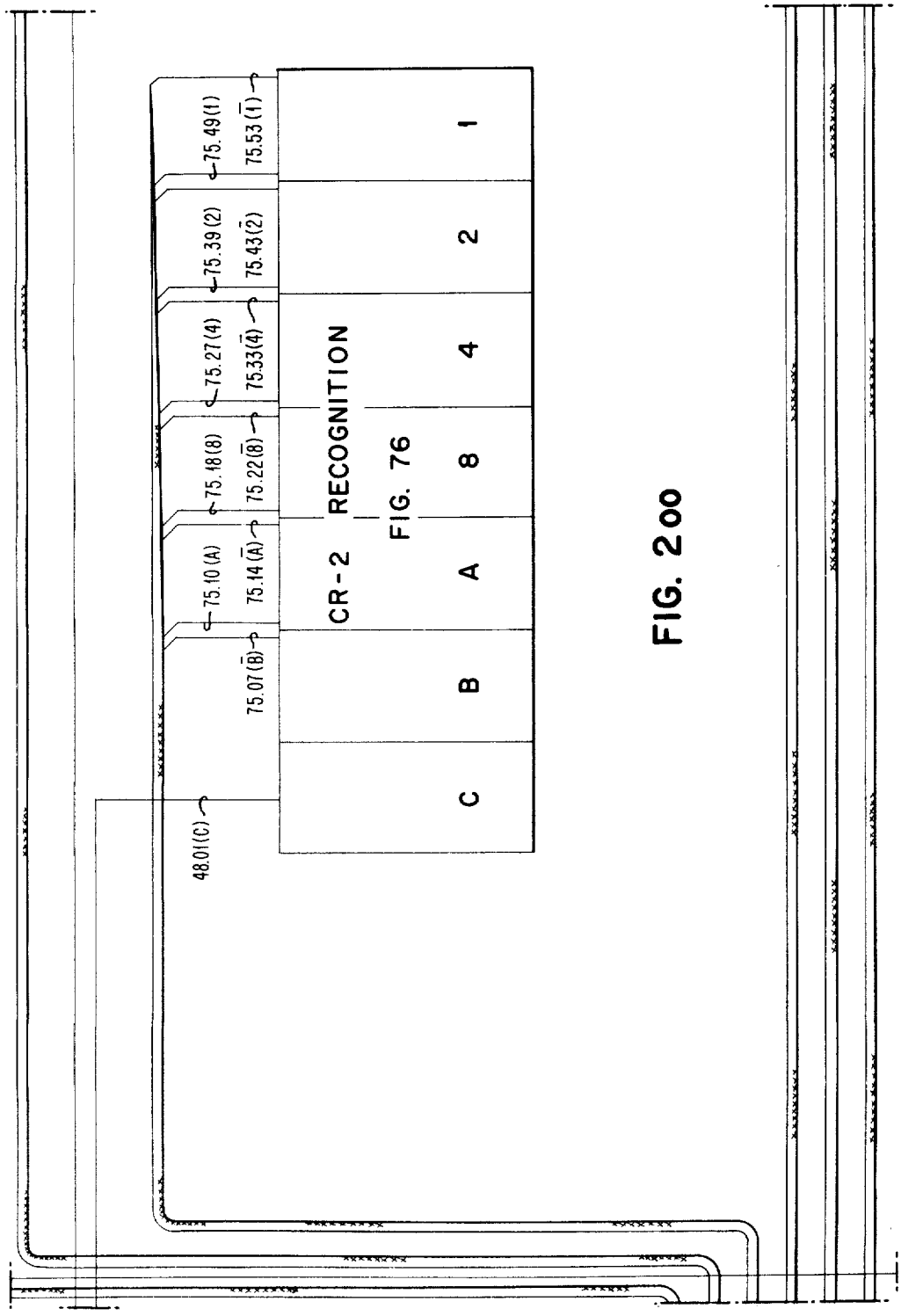

75.49(1)
75.53(1)
75.39(2)
75.43(2)
75.27(4)
75.33(4)
75.18(8)
75.22(8)
75.10(A)
75.14(A)
75.07(B)
48.01(C)
CR-2 RECOGNITION
FIG. 76
1
2
4
8
A
B
C

FIG. 200

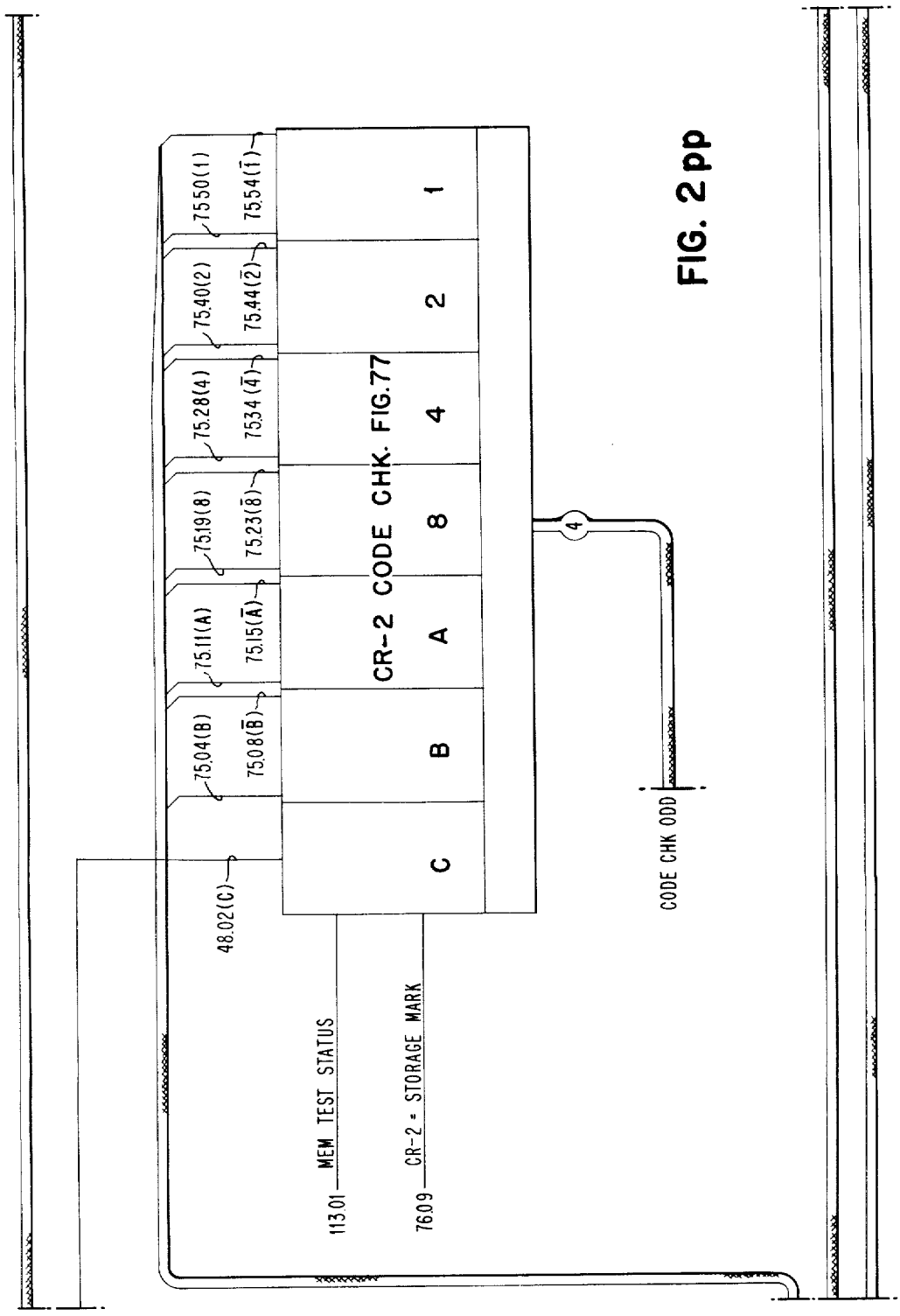

CR-2 CODE CHK. FIG.77
75.50(1)
75.54(1̄)
75.40(2)
75.44(2̄)
75.28(4)
75.34(4̄)
75.19(8)
75.23(8̄)
75.11(A)
75.15(Ā)
75.04(B)
75.08(B̄)
48.02(C)
1
2
4
8
A
B
C
4
CODE CHK ODD
MEM TEST STATUS
113.01
CR-2 = STORAGE MARK
76.09

FIG. 2pp

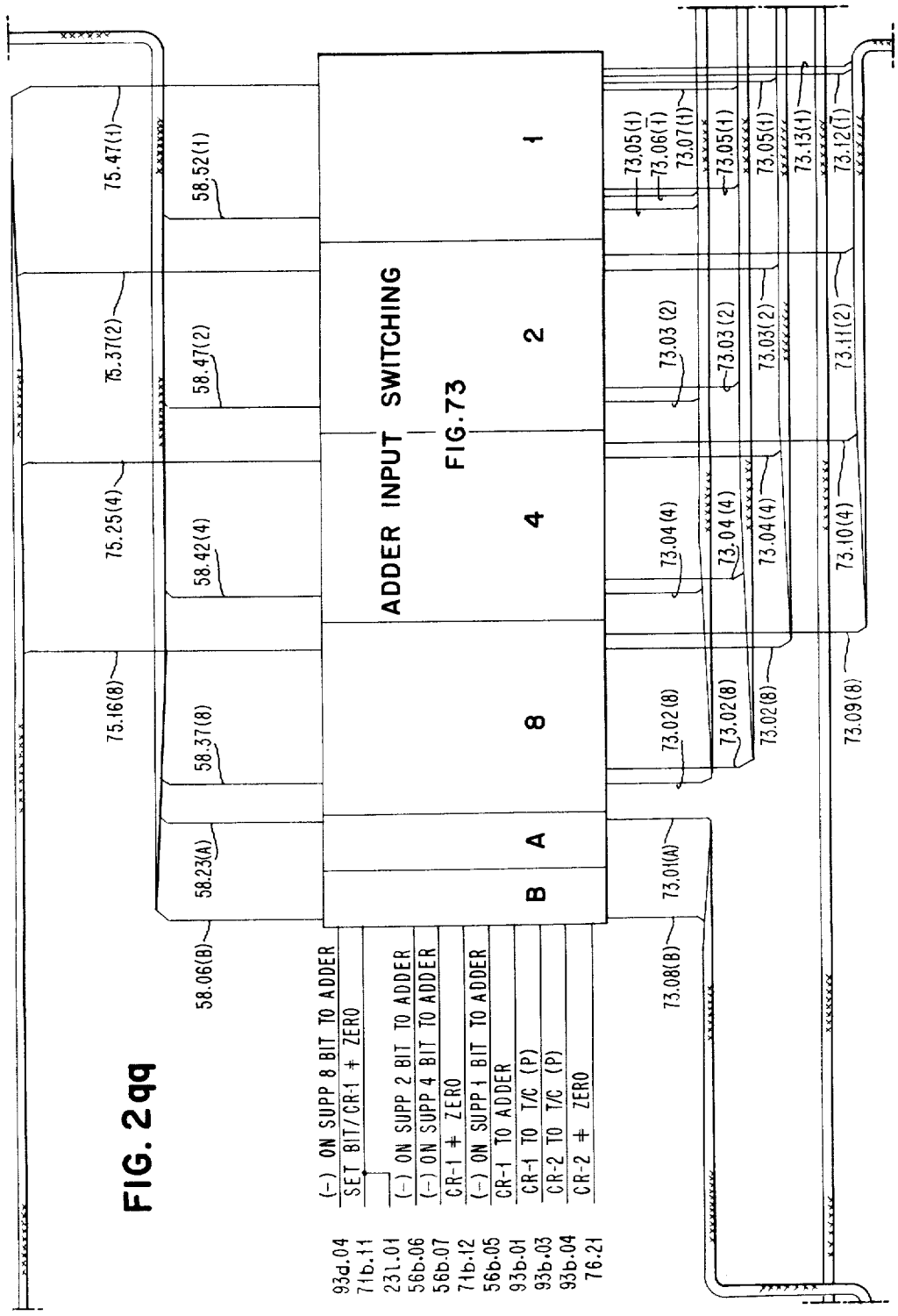
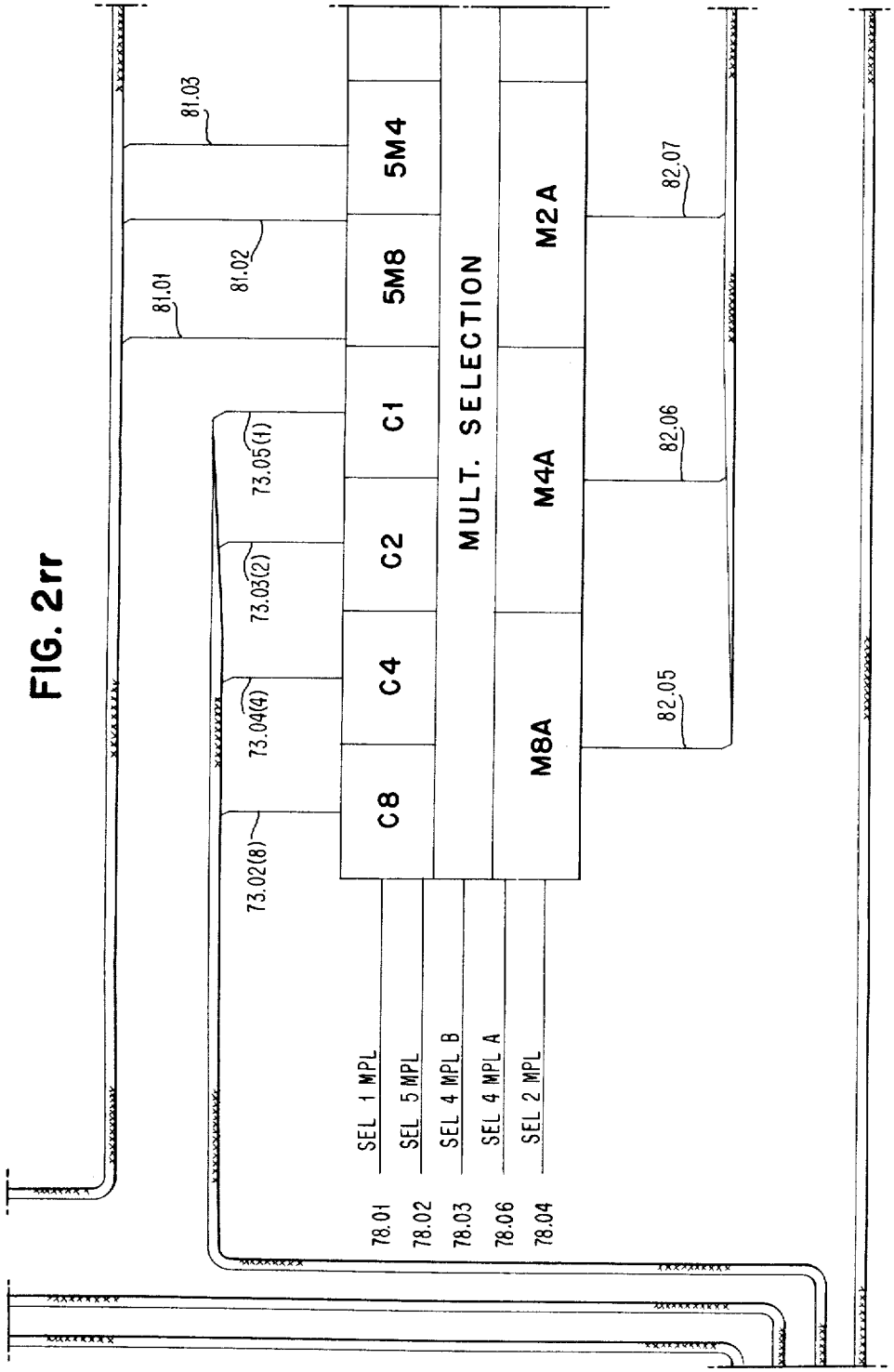

ADDER INPUT SWITCHING
FIG. 73
1
2
4
8
A
B
75.47(1)
58.52(1)
75.37(2)
58.47(2)
75.25(4)
58.42(4)
75.16(8)
58.37(8)
58.23(A)
58.06(B)
73.05(1)
73.06(1)
73.07(1)
73.03(2)
73.04(4)
73.02(8)
73.01(A)
73.08(B)
73.13(1)
73.12(1)
73.11(2)
73.10(4)
73.09(8)
(-) ON SUPP 8 BIT TO ADDER
SET BIT/CR-1 + ZERO
(-) ON SUPP 2 BIT TO ADDER
(-) ON SUPP 4 BIT TO ADDER
CR-1 + ZERO
(-) ON SUPP 1 BIT TO ADDER
CR-1 TO ADDER
CR-1 TO T/C (P)
CR-2 TO T/C (P)
CR-2 + ZERO
93d.04
71b.11
231.01
56b.06
56b.07
71b.12
56b.05
93b.01
93b.03
93b.04
76.21

FIG. 2qq

FIG. 2rr


81.03
81.02
81.01
73.05(1)
73.03(2)
73.04(4)
73.02(8)
5M4
5M8
C1
C2
C4
C8
MULT. SELECTION
M2A
M4A
M8A
82.07
82.06
82.05
SEL 1 MPL
SEL 5 MPL
SEL 4 MPL B
SEL 4 MPL A
SEL 2 MPL
78.01
78.02
78.03
78.06
78.04

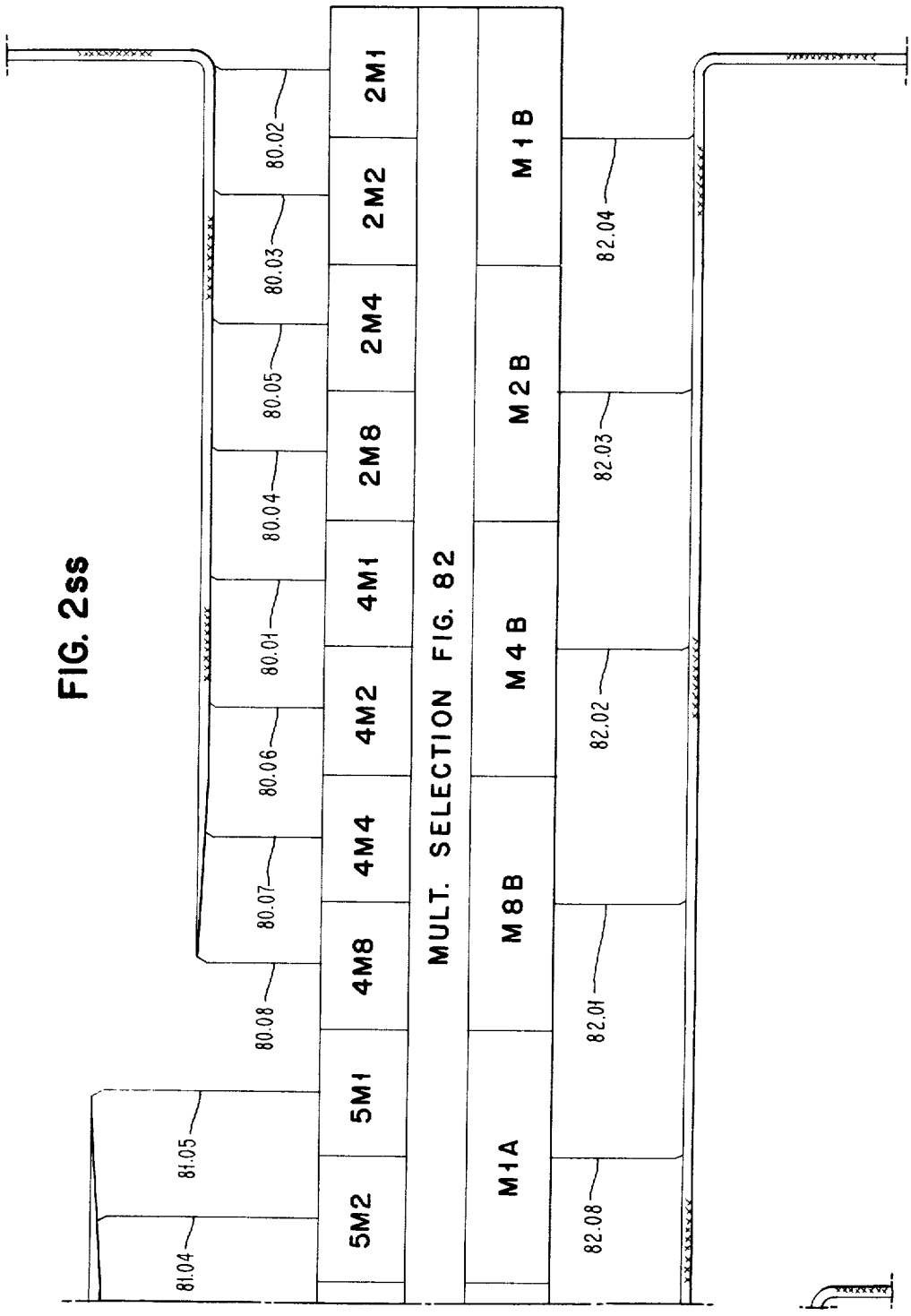

2M1
2M2
2M4
2M8
4M1
4M2
4M4
4M8
5M1
5M2
MULT. SELECTION FIG. 82
M1B
M2B
M4B
M8B
M1A
80.02
80.03
80.05
80.04
80.01
80.06
80.07
80.08
81.05
81.04
82.04
82.03
82.02
82.01
82.08

FIG. 2ss

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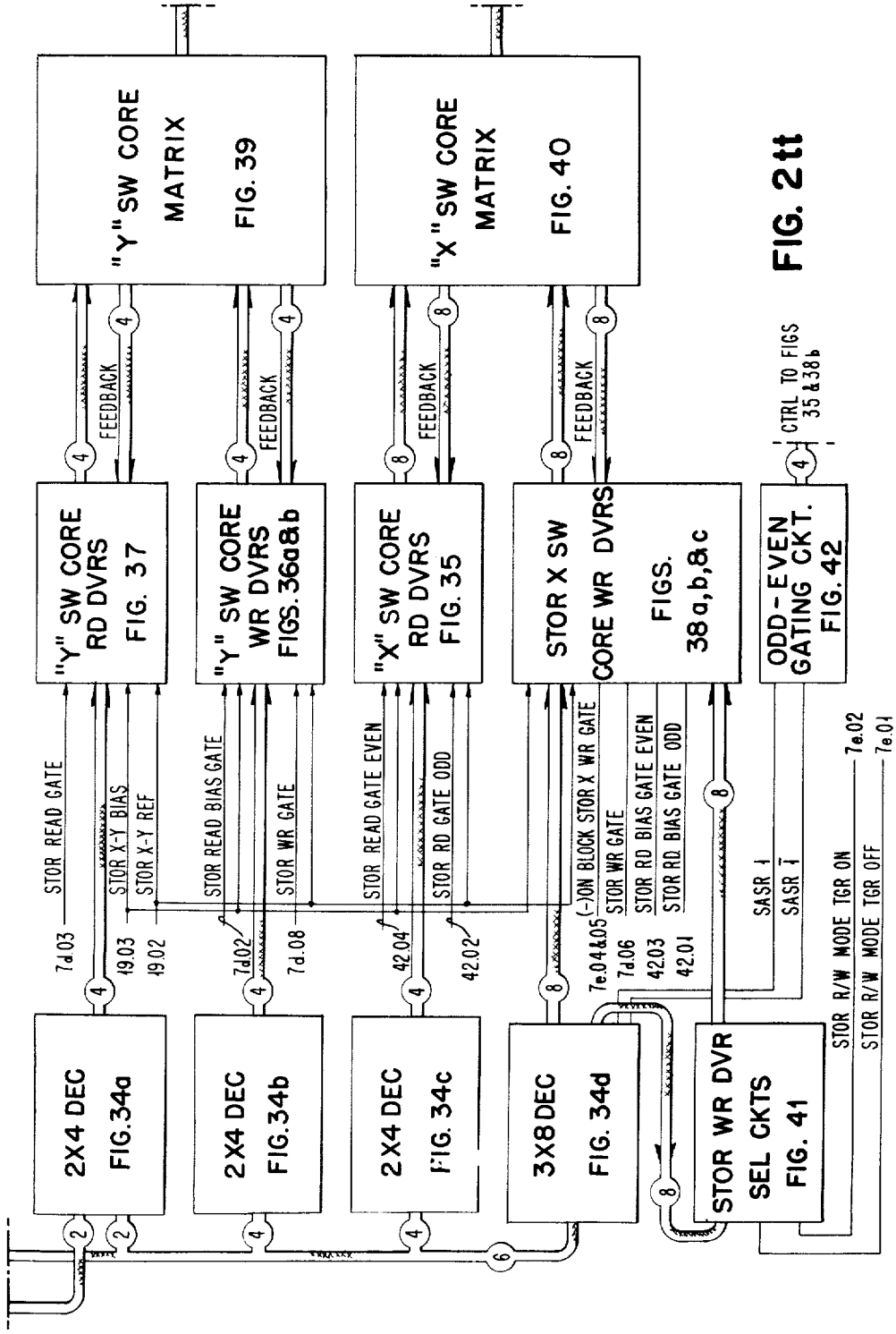


FIG. 2tt

FIG. 2uu

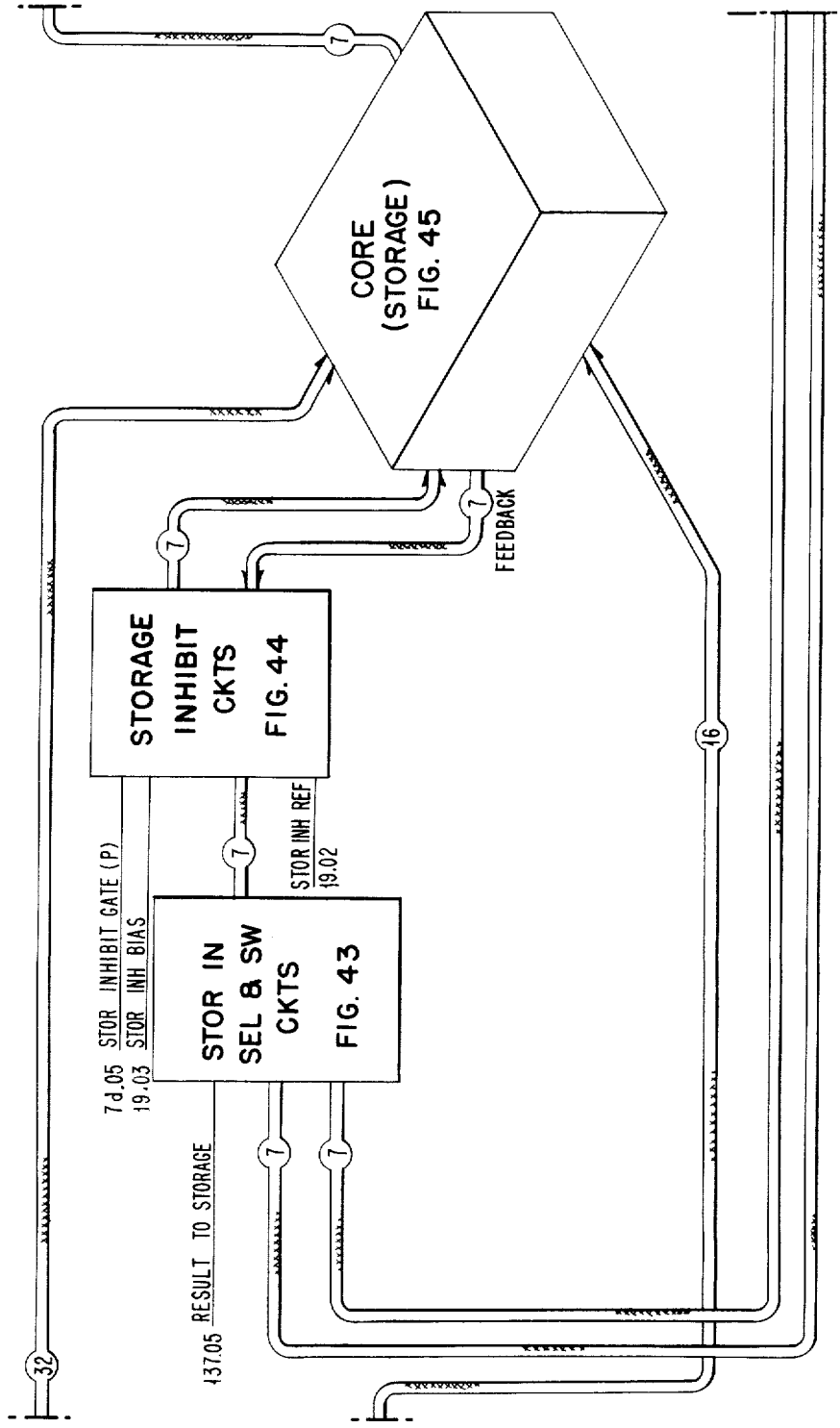
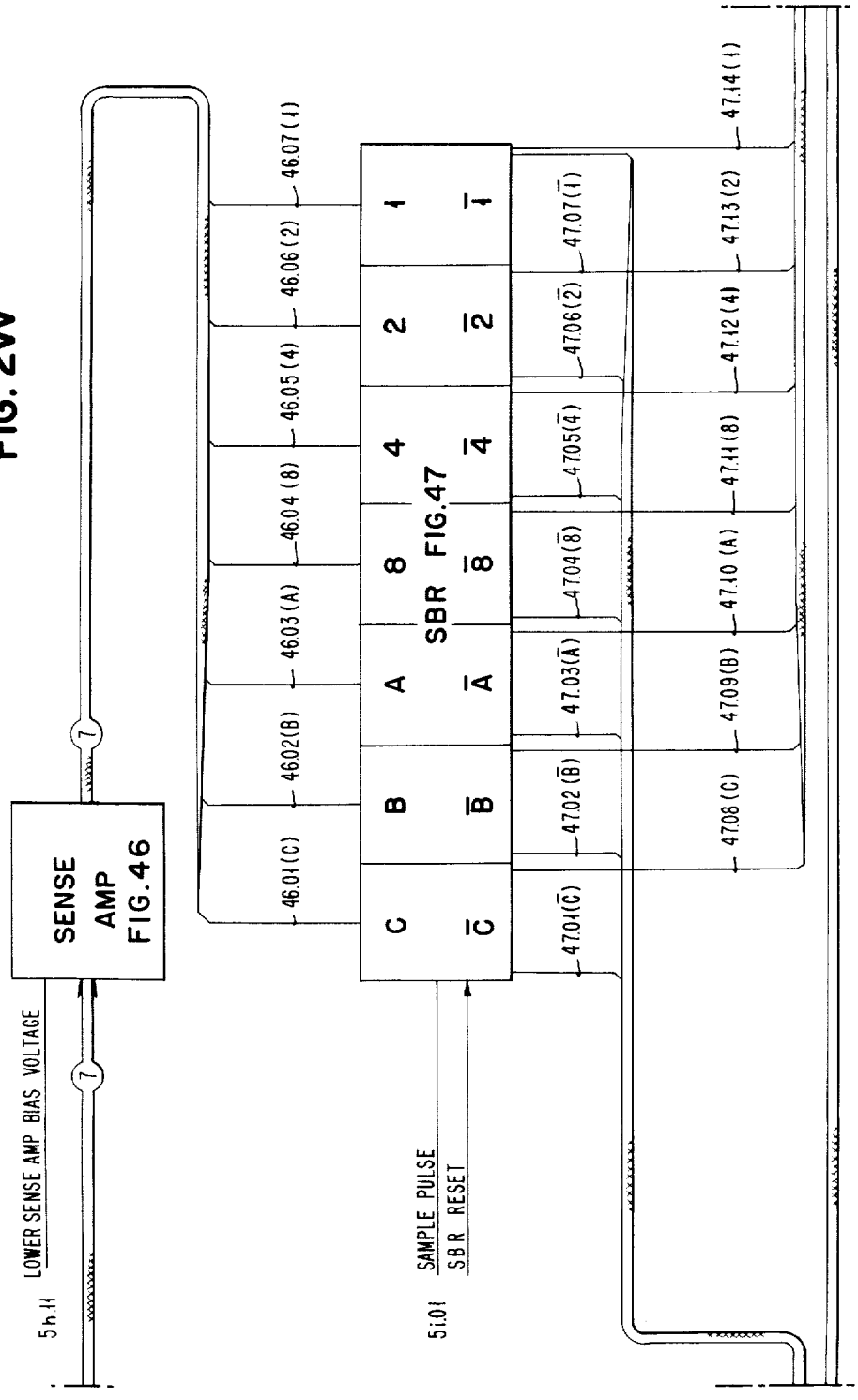

CORE (STORAGE) FIG. 45
STORAGE INHIBIT CKTS FIG. 44
STOR IN SEL & SW CKTS FIG. 43
FEEDBACK
STOR INH REF 19.02
7d.05 STOR INHIBIT GATE (P)
19.03 STOR INH BIAS
137.05 RESULT TO STORAGE
7
16
32

FIG. 2vv


SENSE AMP FIG.46
LOWER SENSE AMP BIAS VOLTAGE
5h.11
SAMPLE PULSE
SBR RESET
5i.01
SBR FIG.47
C B A 8 4 2 1
C̄ B̄ Ā 8̄ 4̄ 2̄ 1̄
46.01(C)
46.02(B)
46.03(A)
46.04(8)
46.05(4)
46.06(2)
46.07(1)
47.01(C̄)
47.02(B̄)
47.03(Ā)
47.04(8̄)
47.05(4̄)
47.06(2̄)
47.07(1̄)
47.08(C)
47.09(B)
47.10(A)
47.11(8)
47.12(4)
47.13(2)
47.14(1)

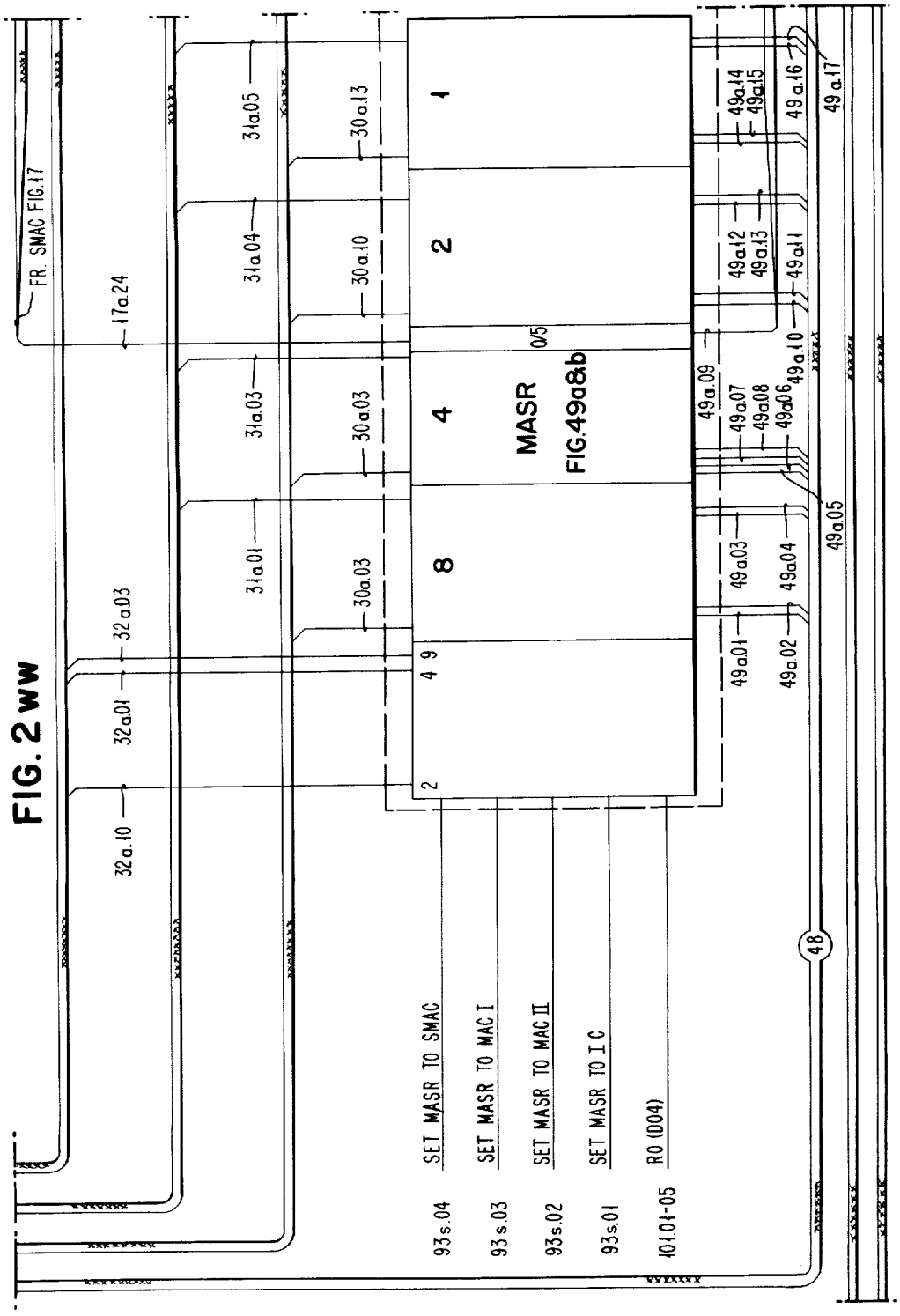
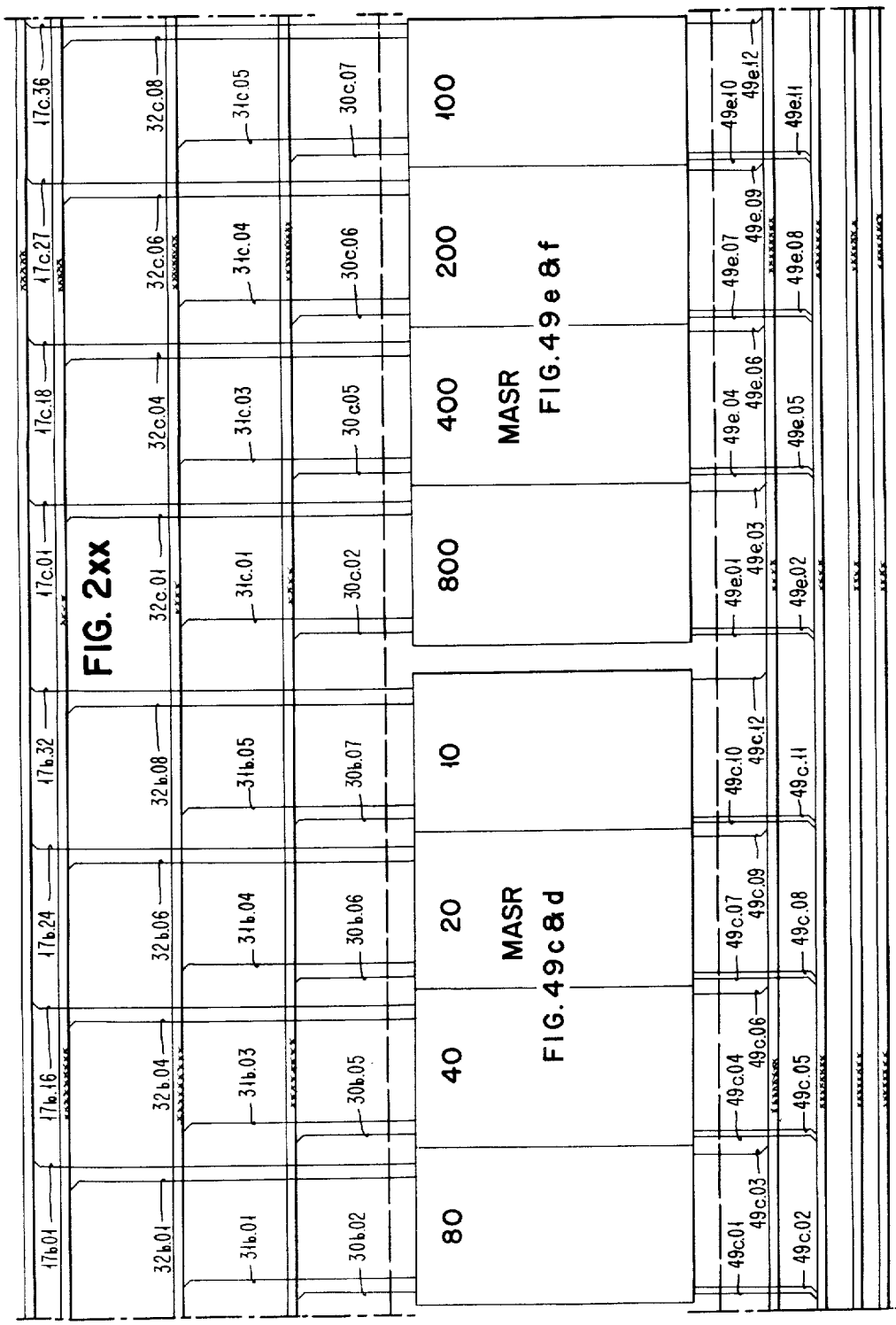

FR. SMAC FIG.17
17a.24
31a.05
31a.04
31a.03
31a.01
30a.13
30a.10
30a.03
30a.03
32a.03
32a.01
32a.10
1
2
4
8
4 9
2
MASR
FIG.49a8b
0/5
49a.14
49a.15
49a.16
49a.17
49a.12
49a.13
49a.11
49a.10
49a.09
49a.07
49a.08
49a.06
49a.05
49a.03
49a.04
49a.01
49a.02
48
SET MASR TO SMAC
SET MASR TO MAC I
SET MASR TO MAC II
SET MASR TO I C
RO (004)
93s.04
93s.03
93s.02
93s.01
10101-05

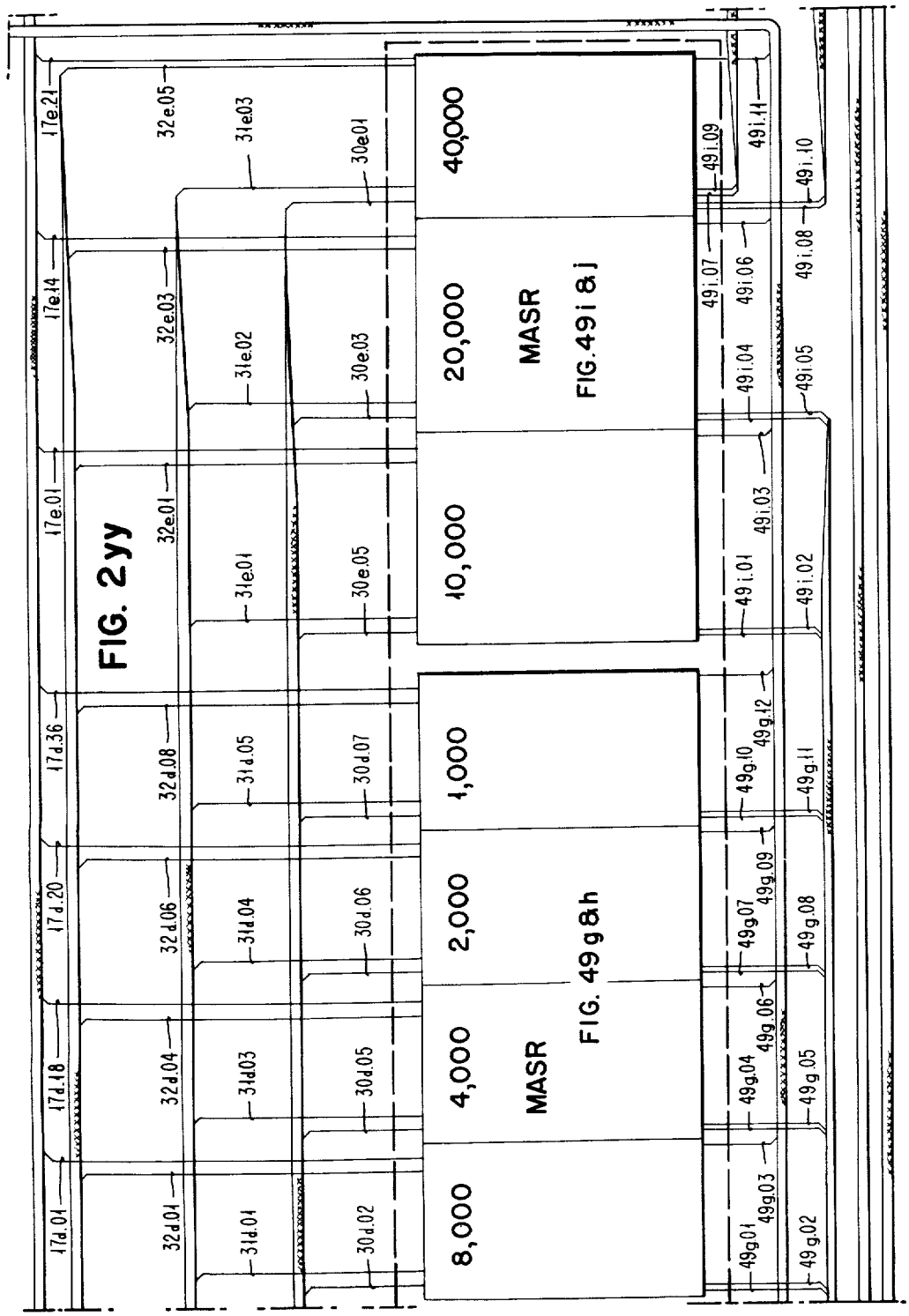
FIG. 2ww

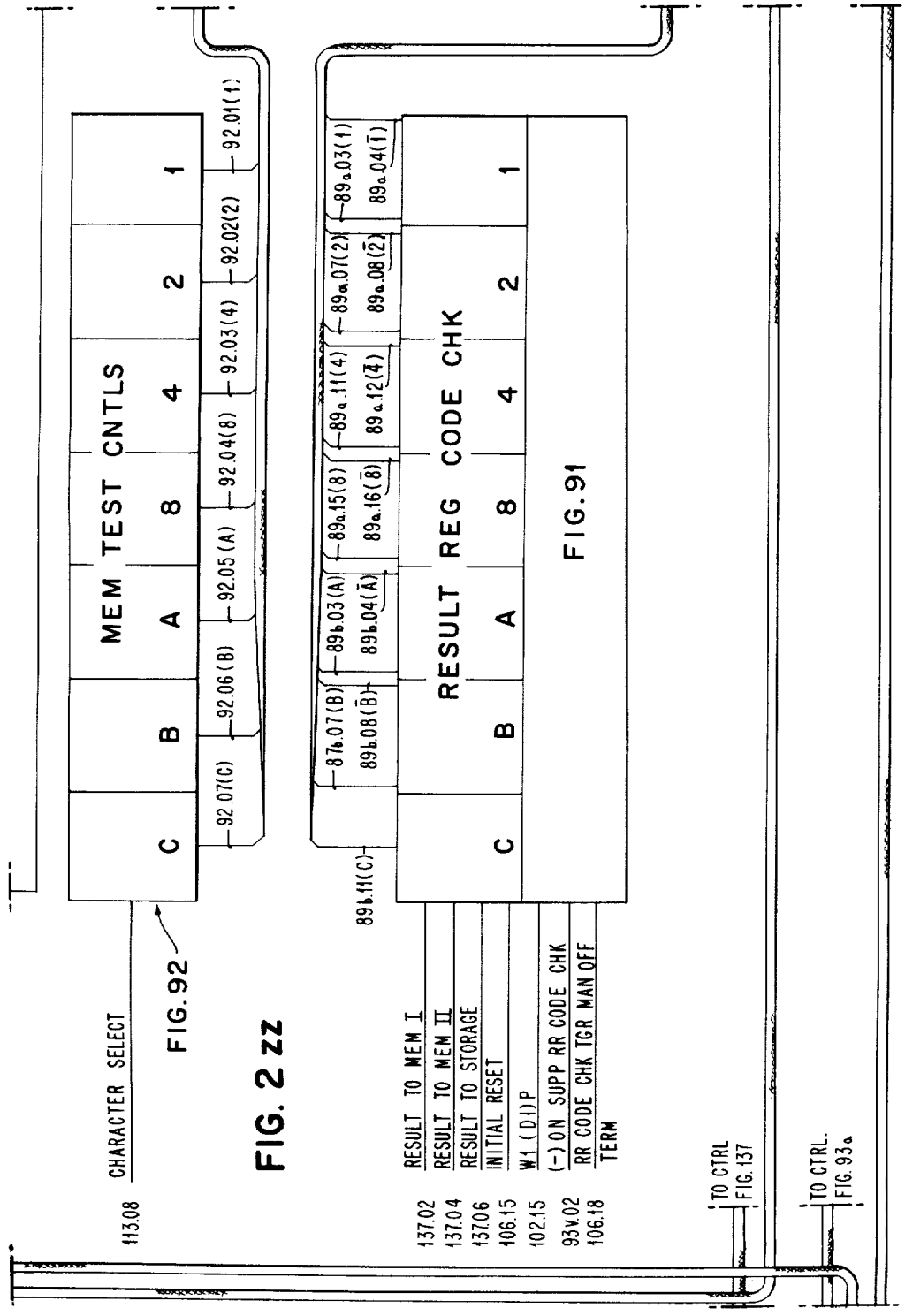
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FIG. 2yy
40,000
20,000
10,000
MASR
FIG. 49i & j
1,000
2,000
4,000
8,000
MASR
FIG. 49g & h
17e.21
17e.14
17e.01
17d.36
17d.20
17d.18
17d.01
32e.05
32e.03
32e.01
32d.08
32d.06
32d.04
32d.01
31e.03
31e.02
31e.04
31d.05
31d.04
31d.03
31d.01
30e.04
30e.03
30e.05
30d.07
30d.06
30d.05
30d.02
49i.09
49i.11
49i.10
49i.07
49i.06
49i.08
49i.04
49i.05
49i.01
49i.03
49i.02
49g.10
49g.12
49g.11
49g.07
49g.09
49g.08
49g.04
49g.06
49g.05
49g.01
49g.03
49g.02


MEM TEST CNTLS
C
B
A
8
4
2
1
92.07(C)
92.06(B)
92.05(A)
92.04(8)
92.03(4)
92.02(2)
92.01(1)
RESULT REG CODE CHK
89b.11(C)
89b.08(B̄)
89b.07(B)
89b.04(Ā)
89b.03(A)
89a.16(8̄)
89a.15(8)
89a.12(4̄)
89a.11(4)
89a.08(2̄)
89a.07(2)
89a.04(1̄)
89a.03(1)
FIG. 92
FIG. 91
FIG. 2zz
113.08 CHARACTER SELECT
137.02 RESULT TO MEM I
137.04 RESULT TO MEM II
137.06 RESULT TO STORAGE
106.15 INITIAL RESET
102.15 W1 (D1)P
93v.02 (-) ON SUPP RR CODE CHK
106.18 RR CODE CHK TGR MAN OFF
TERM
TO CTRL FIG. 137
TO CTRL. FIG. 93a

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OVERLAP MODE CONTROL

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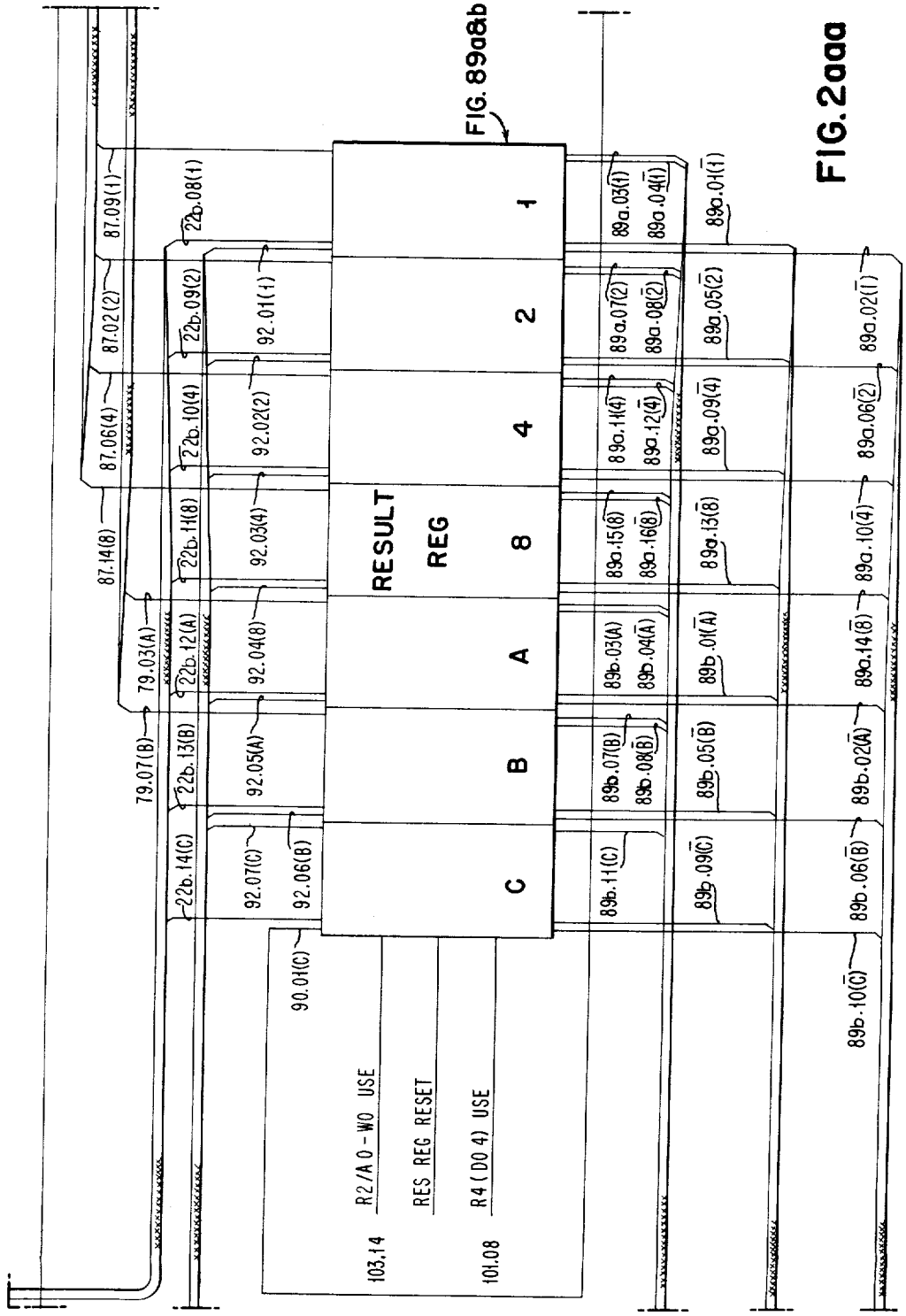


FIG. 2aa

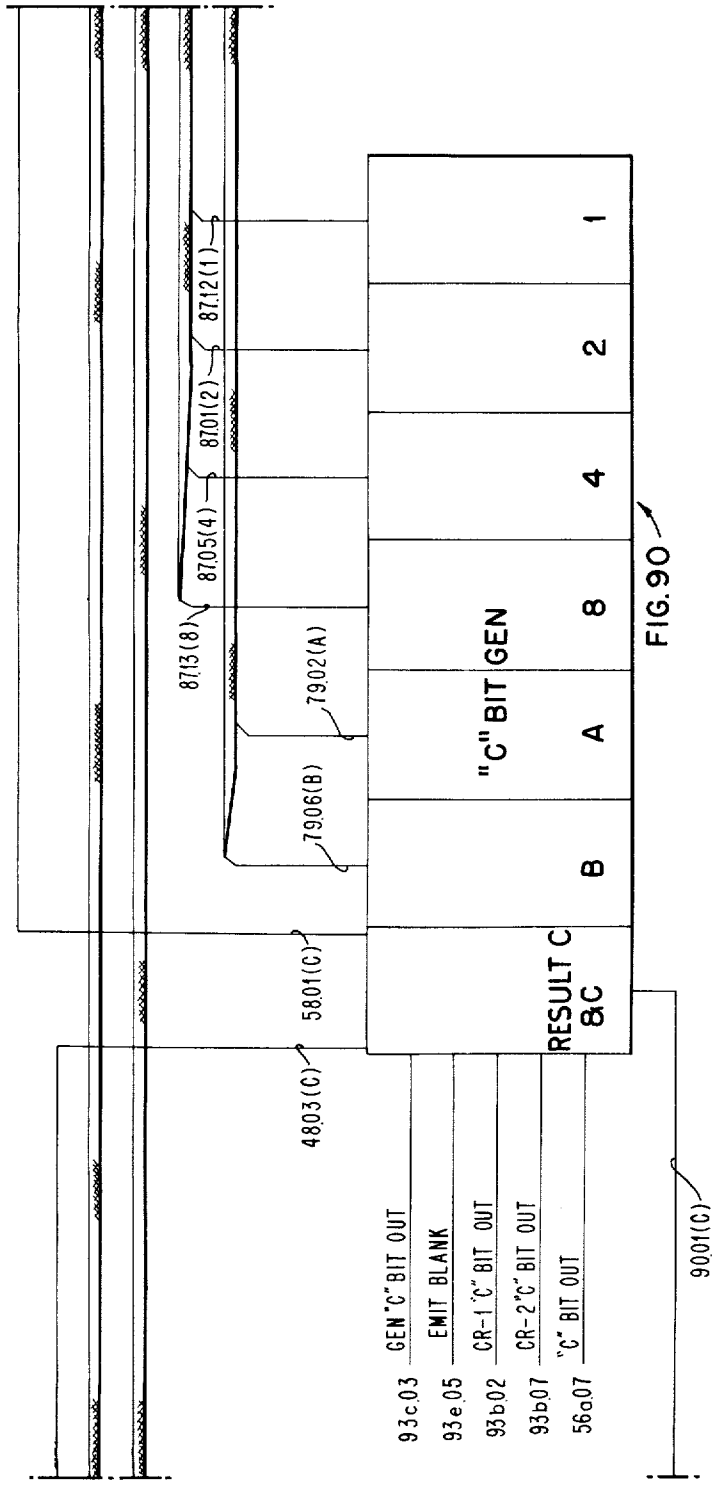

87.13(8)
87.05(4)
87.01(2)
87.12(1)
79.02(A)
79.06(B)
58.01(C)
48.03(C)
"C" BIT GEN
8
4
2
1
A
B
RESULT C
&C
FIG. 90
GEN "C" BIT OUT
EMIT BLANK
CR-1 "C" BIT OUT
CR-2 "C" BIT OUT
"C" BIT OUT
93c.03
93e.05
93b.02
93b.07
56a.07
90.01(C)

FIG. 2bbb

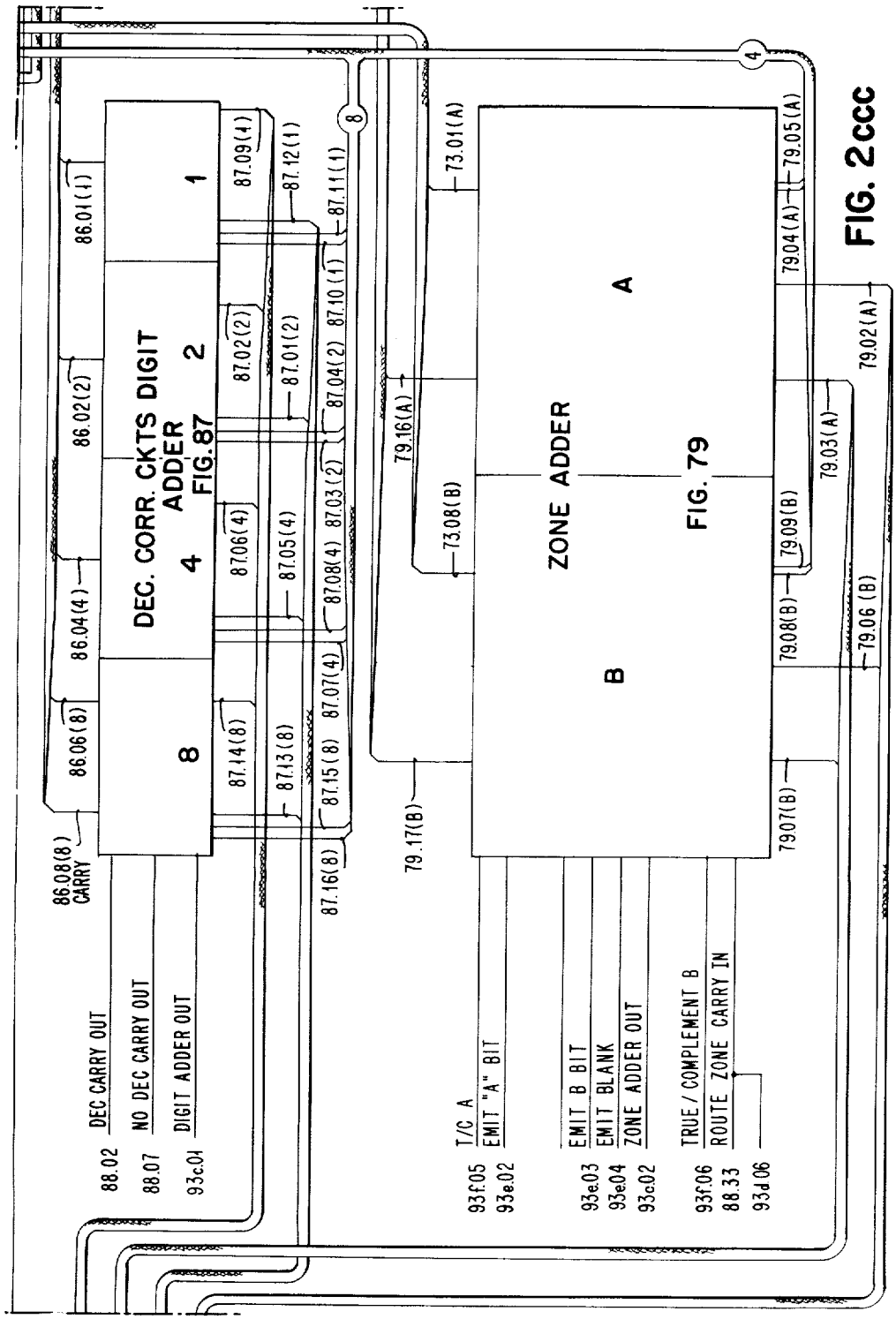

DEC. CORR. CKTS DIGIT ADDER FIG.87
8
4
2
1
ZONE ADDER
A
B
FIG. 79
86.08(8) CARRY
86.06(8)
86.04(4)
86.02(2)
86.01(1)
87.14(8)
87.13(8)
87.15(8)
87.16(8)
87.07(4)
87.08(4)
87.06(4)
87.05(4)
87.03(2)
87.04(2)
87.02(2)
87.01(2)
87.09(4)
87.12(1)
87.11(1)
87.10(1)
79.16(A)
79.17(B)
73.08(B)
73.01(A)
79.07(B)
79.08(B)
79.09(B)
79.04(A)
79.05(A)
79.03(A)
79.02(A)
79.06(B)
88.02 DEC CARRY OUT
88.07 NO DEC CARRY OUT
93c.01 DIGIT ADDER OUT
93f.05 T/C A
93e.02 EMIT "A" BIT
93e.03 EMIT B BIT
93e.04 EMIT BLANK
93c.02 ZONE ADDER OUT
93f.06 TRUE / COMPLEMENT B
88.33 ROUTE ZONE CARRY IN
93d.06

FIG. 2ccc

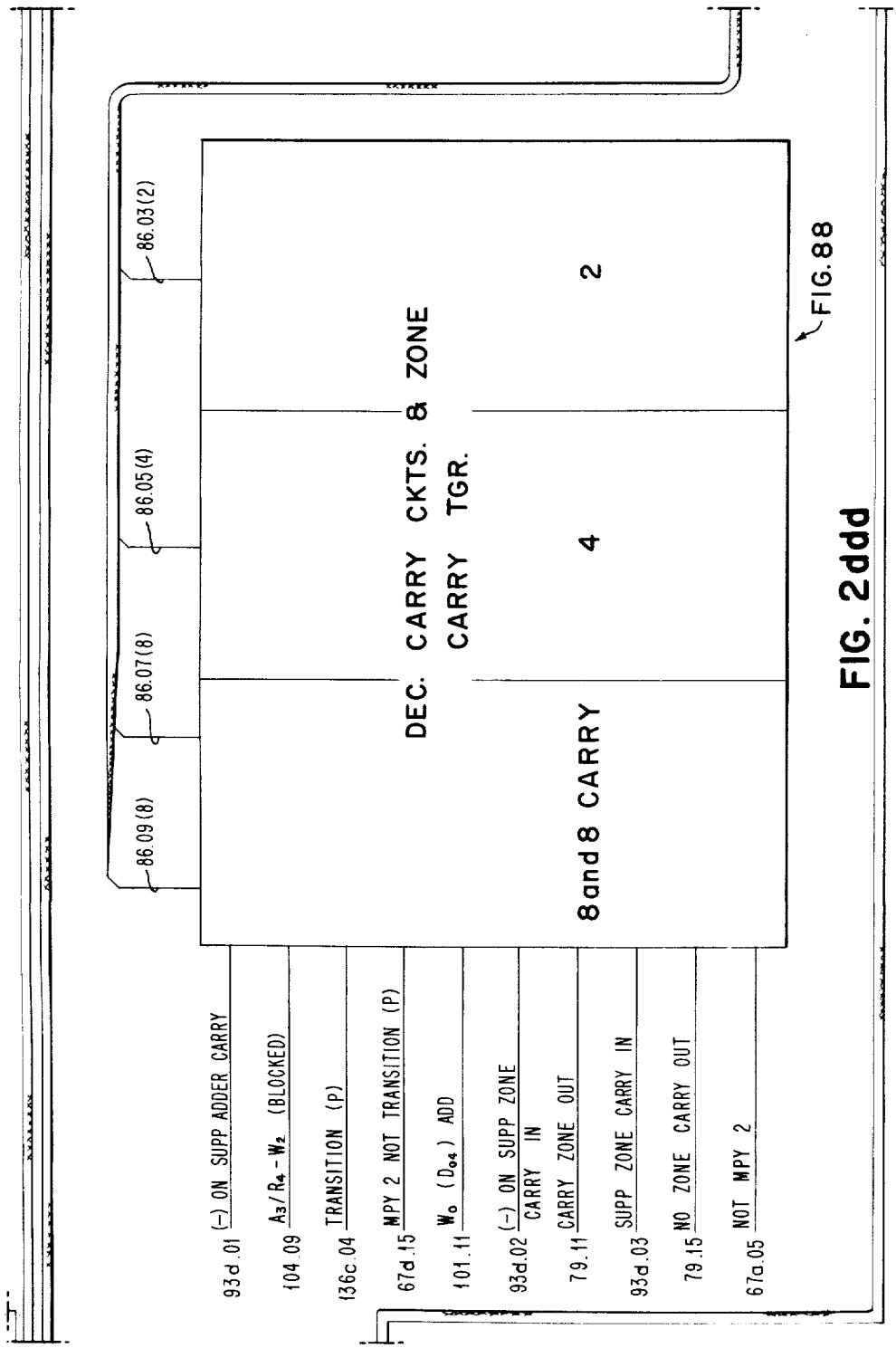


FIG. 88

FIG. 2ddd

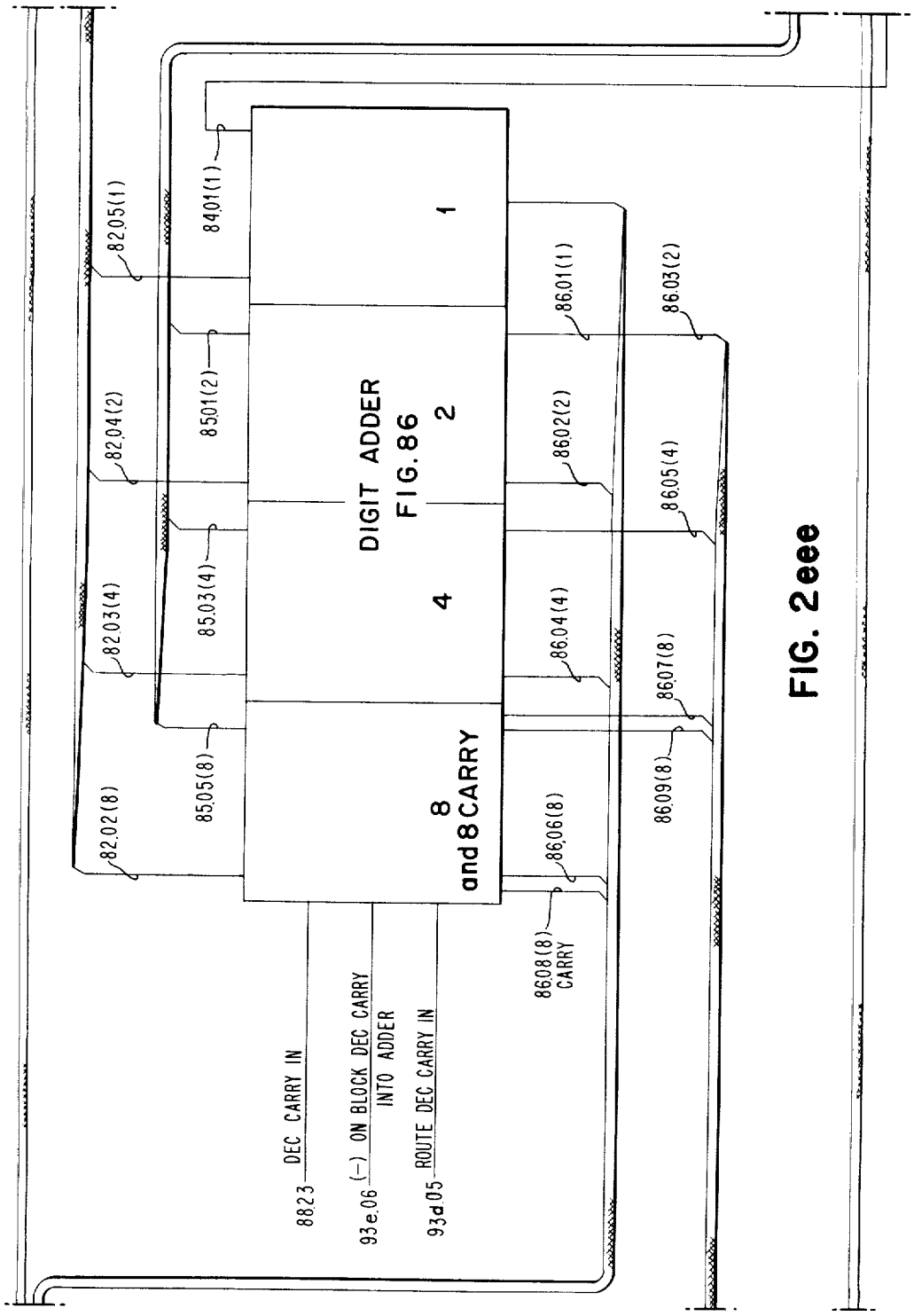
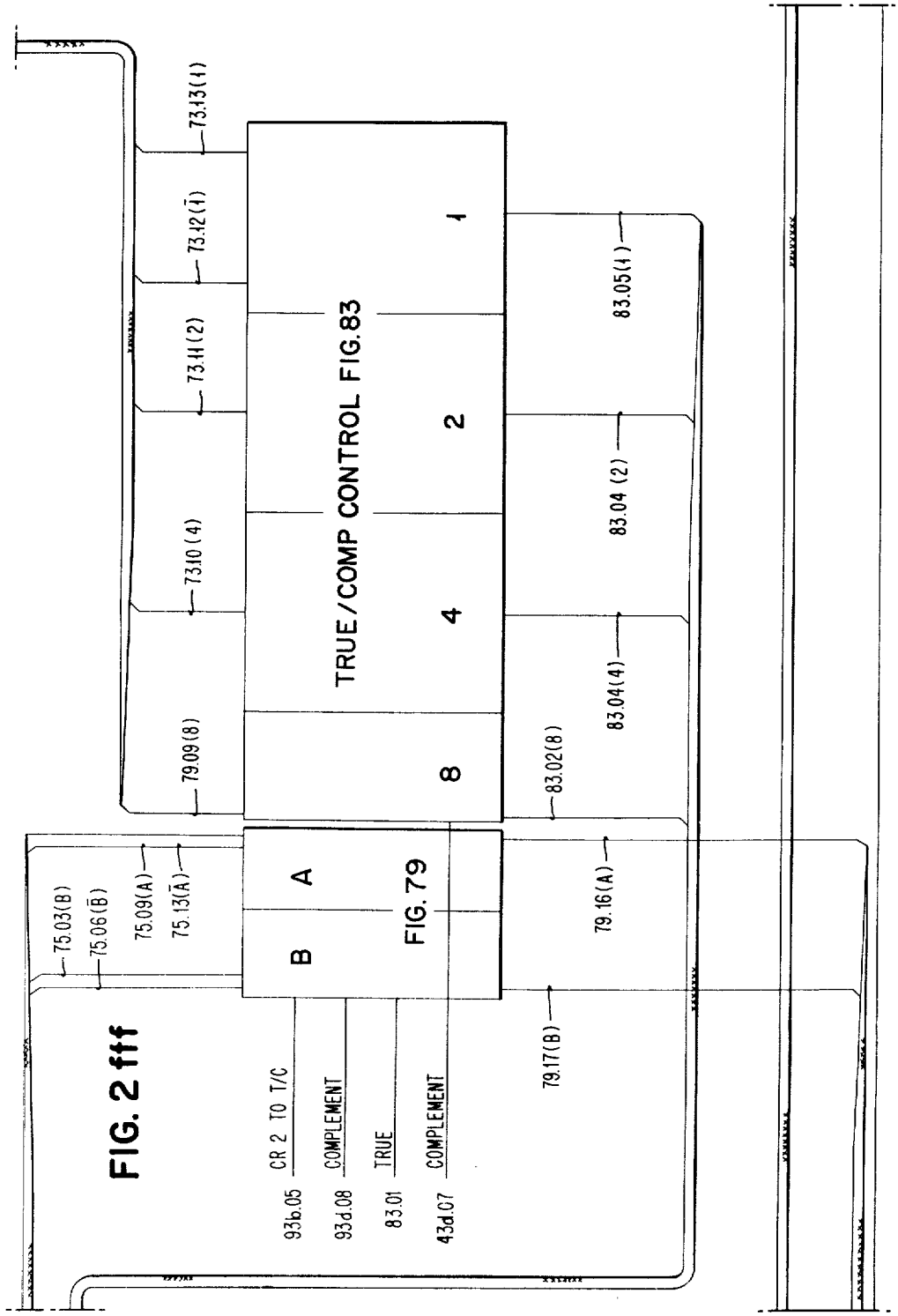

DIGIT ADDER
FIG. 86
1
2
4
8 and 8 CARRY
84.01(1)
82.05(1)
85.01(2)
82.04(2)
85.03(4)
82.03(4)
85.05(8)
82.02(8)
86.01(1)
86.03(2)
86.02(2)
86.05(4)
86.04(4)
86.07(8)
86.09(8)
86.06(8)
86.08(8) CARRY
8823 DEC CARRY IN
93e.06 (-) ON BLOCK DEC CARRY INTO ADDER
93d.05 ROUTE DEC CARRY IN

FIG. 2ee


73.13(1)
73.12(1)
73.11(2)
73.10(4)
79.09(8)
TRUE/COMP CONTROL FIG.83
1
2
4
8
83.05(1)
83.04(2)
83.04(4)
83.02(8)
79.16(A)
79.17(B)
75.03(B)
75.06(B)
75.09(A)
75.13(A)
A
B
FIG. 79
CR 2 TO T/C
COMPLEMENT
TRUE
COMPLEMENT
93b.05
93d.08
83.01
43d.07
FIG. 2 fff

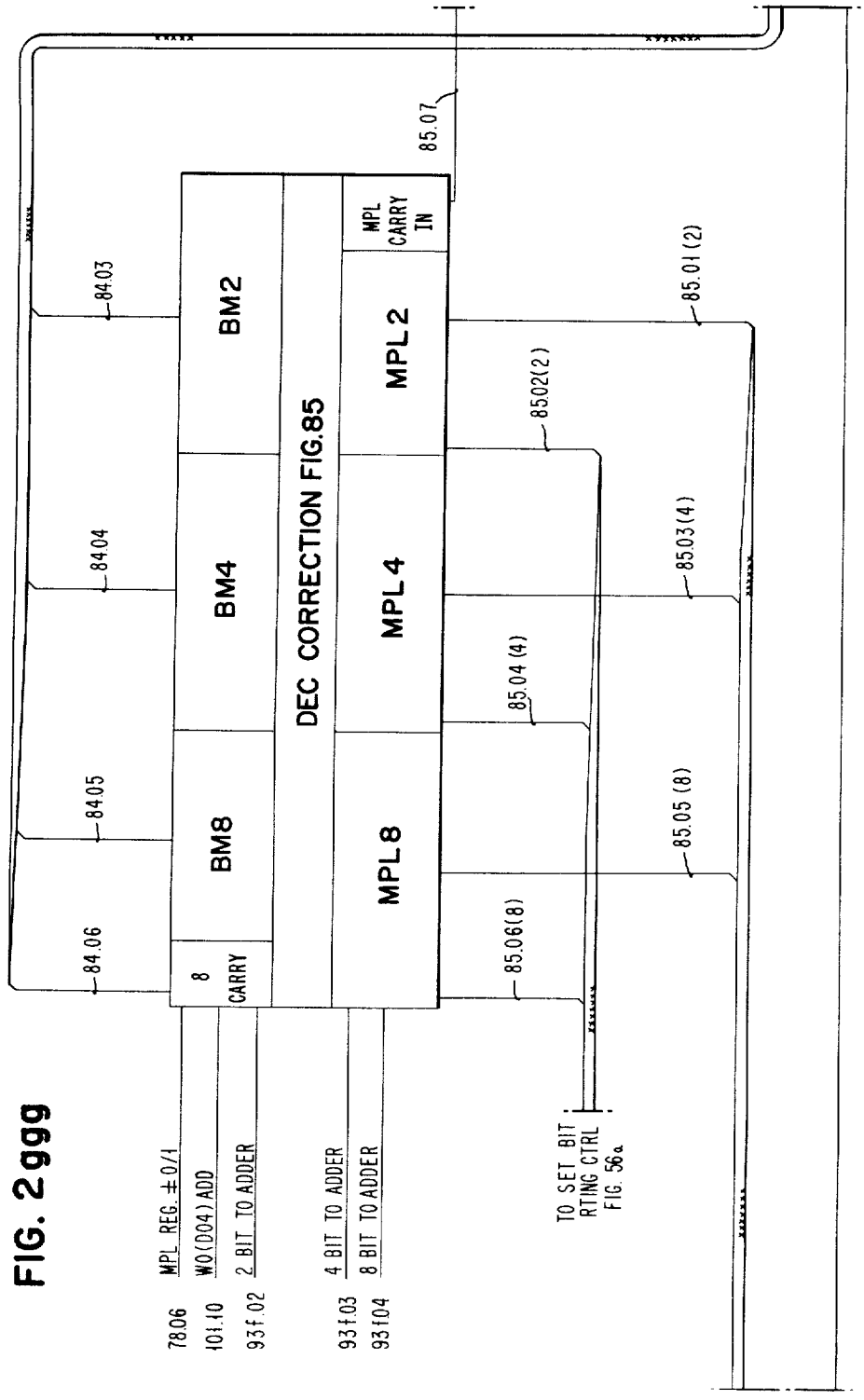

85.07
84.03
84.04
84.05
84.06
BM2
BM4
BM8
8 CARRY
DEC CORRECTION FIG.85
MPL CARRY IN
MPL 2
MPL 4
MPL 8
85.01(2)
8502(2)
85.03(4)
85.04(4)
85.05(8)
85.06(8)
TO SET BIT RTING CTRL FIG. 56a
MPL REG. ± 0/1
W0(004) ADD
2 BIT TO ADDER
4 BIT TO ADDER
8 BIT TO ADDER
78.06
101.10
934.02
934.03
934.04

FIG. 2ggg

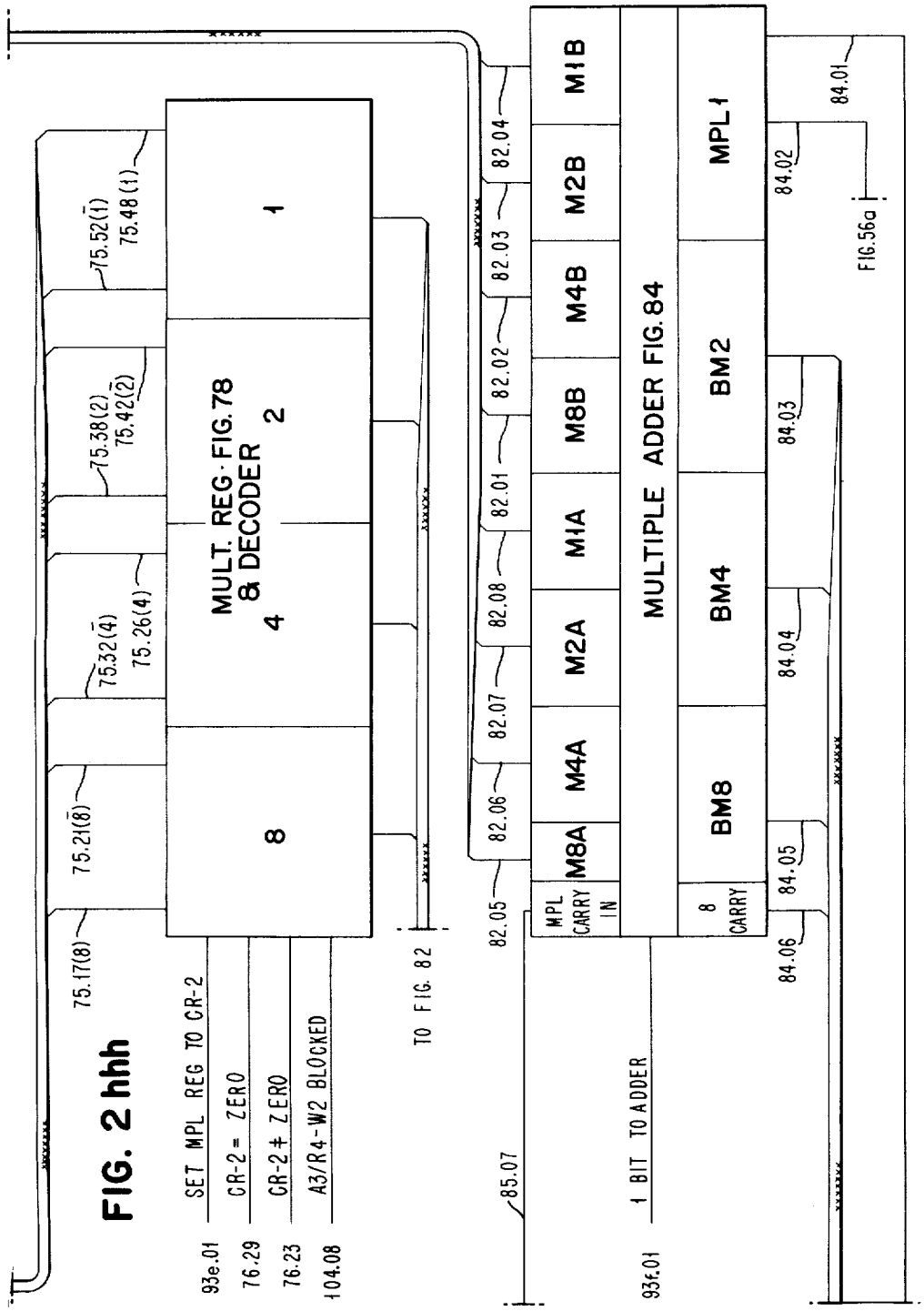

MULT. REG. FIG. 78
& DECODER
8
4
2
1
75.17(8)
75.21(8)
75.32(4)
75.26(4)
75.38(2)
75.42(2)
75.52(1)
75.48(1)
SET MPL REG TO CR-2
CR-2 = ZERO
CR-2 ± ZERO
A3/R4-W2 BLOCKED
93e.01
76.29
76.23
104.08
TO FIG. 82
82.05
82.06
82.07
82.08
82.01
82.02
82.03
82.04
MPL CARRY IN
M8A
M4A
M2A
M1A
M8B
M4B
M2B
M1B
MULTIPLE ADDER FIG. 84
8 CARRY
BM8
BM4
BM2
MPL 1
84.01
84.02
84.03
84.04
84.05
84.06
FIG. 56a
85.07
1 BIT TO ADDER
93f.01

FIG. 2 hhh

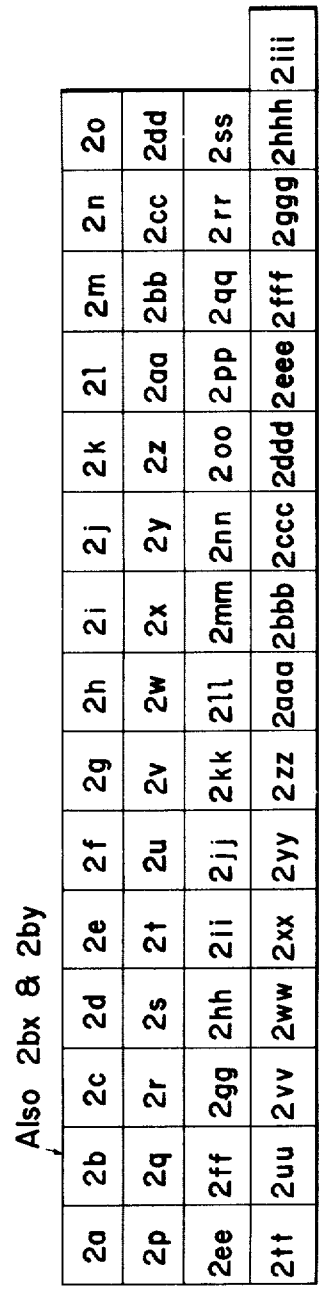

Also 2bx & 2by
2a 2b 2c 2d 2e 2f 2g 2h 2i 2j 2k 2l 2m 2n 2o
2p 2q 2r 2s 2t 2u 2v 2w 2x 2y 2z 2aa 2bb 2cc 2dd
2ee 2ff 2gg 2hh 2ii 2jj 2kk 2ll 2mm 2nn 2oo 2pp 2qq 2rr 2ss
2tt 2uu 2vv 2ww 2xx 2yy 2zz 2aaa 2bbb 2ccc 2ddd 2eee 2fff 2ggg 2hhh 2iii

FIG. 2iii

FIG. 3a MEM. 4 X 10 DECODER 1000 ORDER

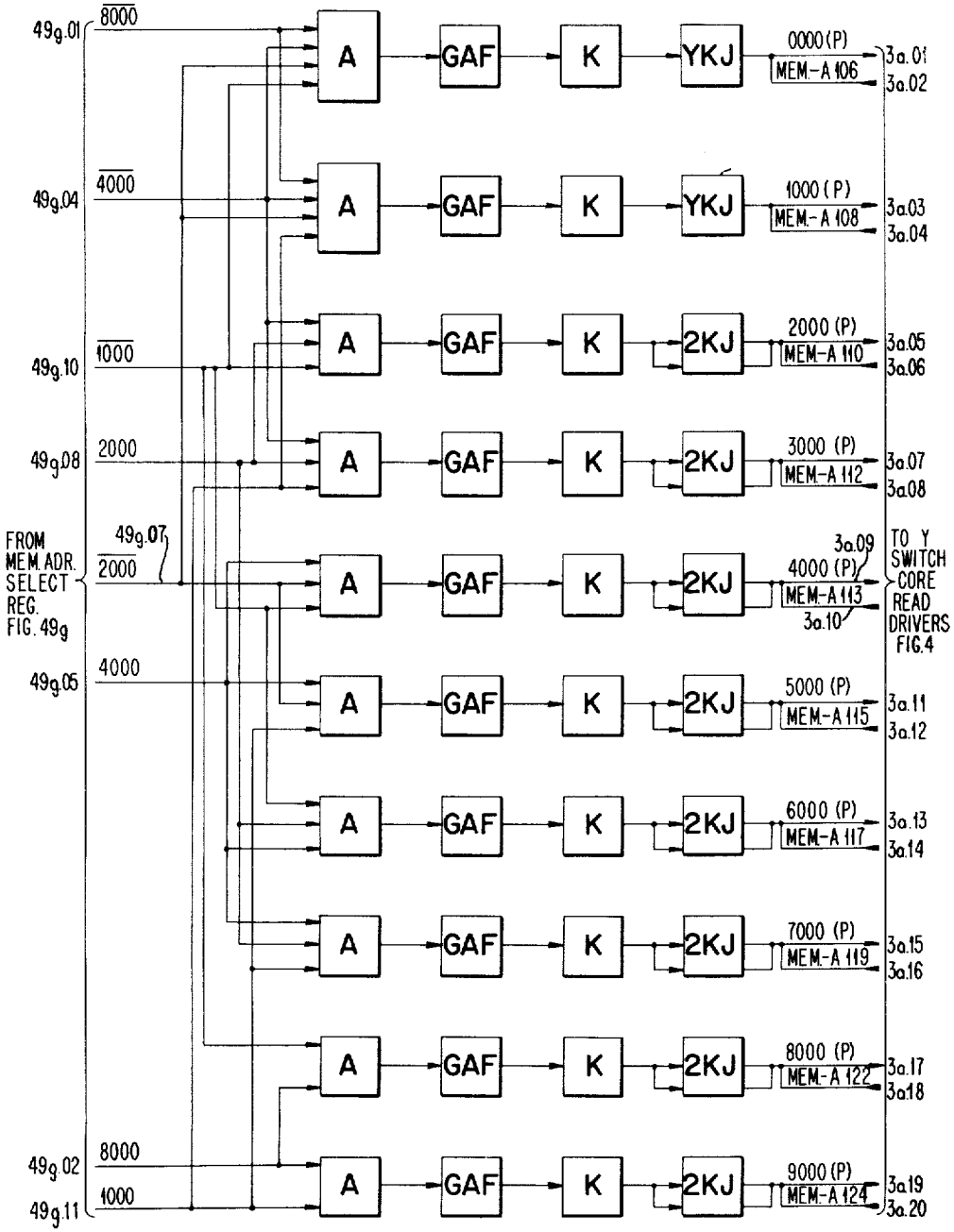


FIG. 3b

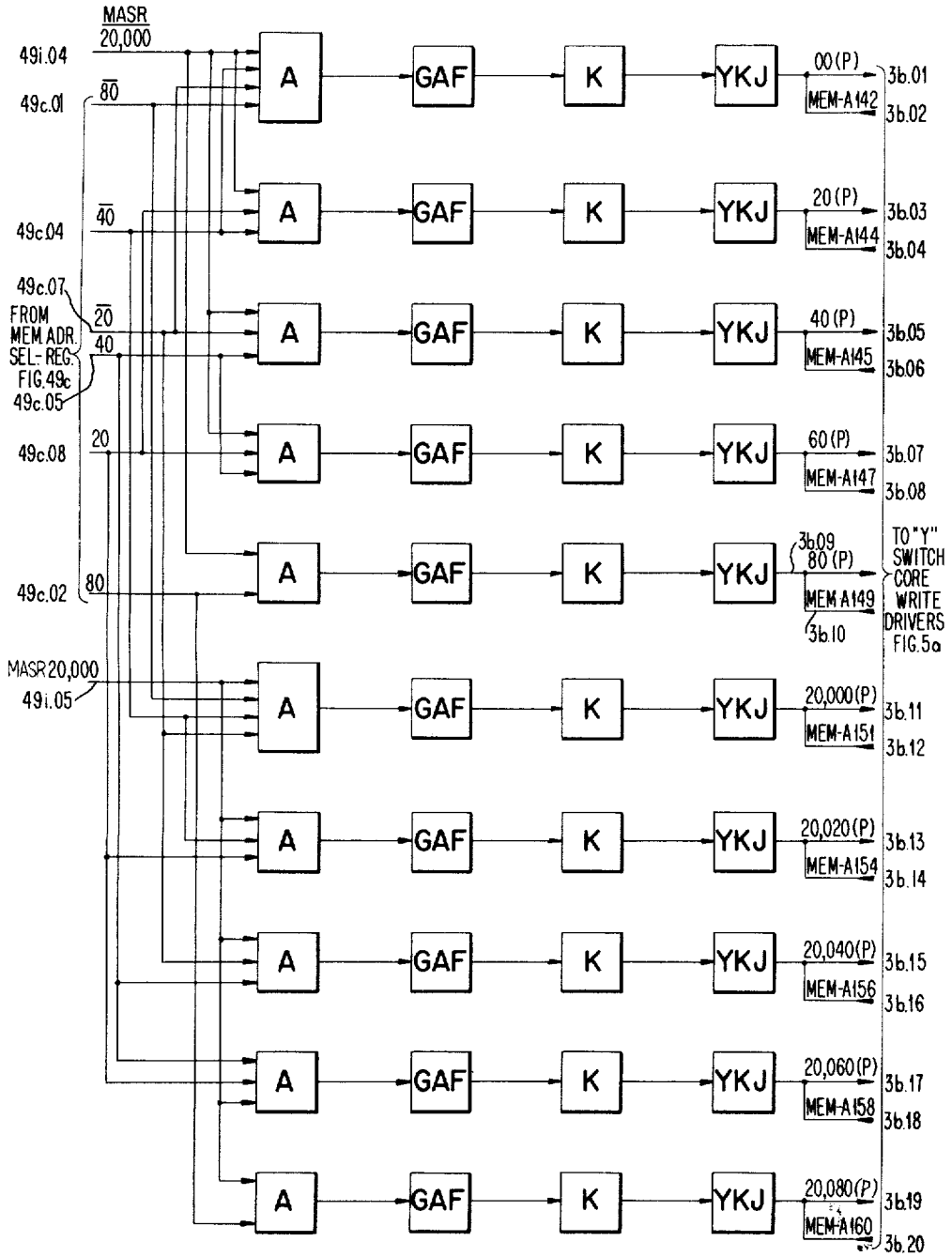
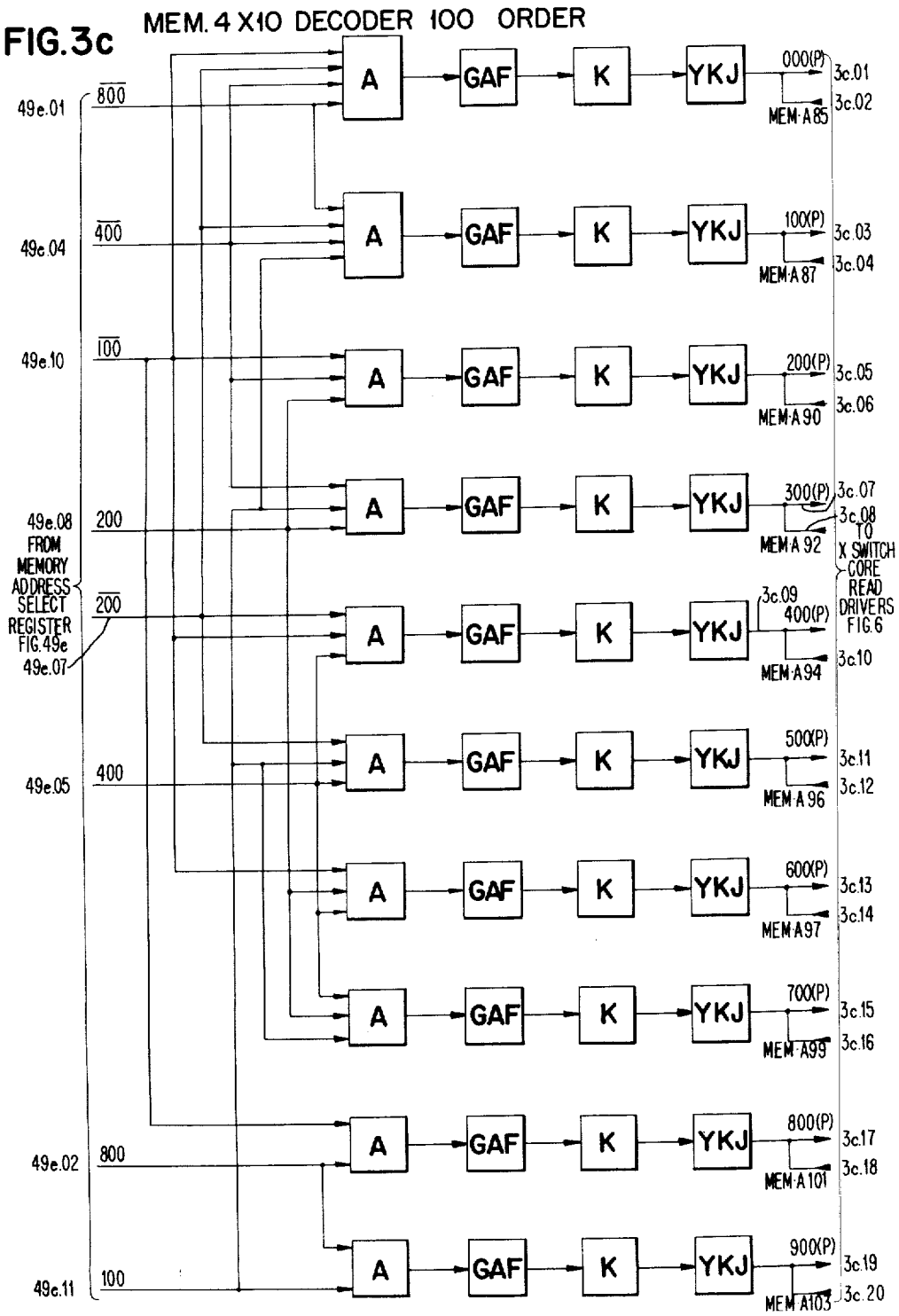

MEM. 4X10 DECODER
MASR 20,000
49i.04
49c.01
80
40
49c.04
49c.07
FROM MEM ADR. SEL-REG. FIG. 49c
49c.05
20
40
49c.08
49c.02
80
MASR 20,000
49i.05
A
GAF
K
YKJ
00(P)
MEM-A142
3b.01
3b.02
20(P)
MEM-A144
3b.03
3b.04
40(P)
MEM-A145
3b.05
3b.06
60(P)
MEM-A147
3b.07
3b.08
3b.09
80(P)
MEM A149
3b.10
TO "Y" SWITCH CORE WRITE DRIVERS FIG. 5a
20,000(P)
MEM-A151
3b.11
3b.12
20,020(P)
MEM-A154
3b.13
3b.14
20,040(P)
MEM-A156
3b.15
3b.16
20,060(P)
MEM-A158
3b.17
3b.18
20,080(P)
MEM-A160
3b.19
3b.20

FIG.3c


MEM. 4 X10 DECODER 100 ORDER
49e.01
800
49e.04
400
49e.10
100
49e.08
200
FROM MEMORY ADDRESS SELECT REGISTER FIG.49e
49e.07
200
49e.05
400
49e.02
800
49e.11
100
A
GAF
K
YKJ
000(P)
MEM·A85
100(P)
MEM·A87
200(P)
MEM·A90
300(P)
MEM·A92
400(P)
MEM·A94
500(P)
MEM·A96
600(P)
MEM·A97
700(P)
MEM·A99
800(P)
MEM·A101
900(P)
MEM·A103
3c.01
3c.02
3c.03
3c.04
3c.05
3c.06
3c.07
3c.08
TO X SWITCH CORE READ DRIVERS FIG.6
3c.09
3c.10
3c.11
3c.12
3c.13
3c.14
3c.15
3c.16
3c.17
3c.18
3c.19
3c.20

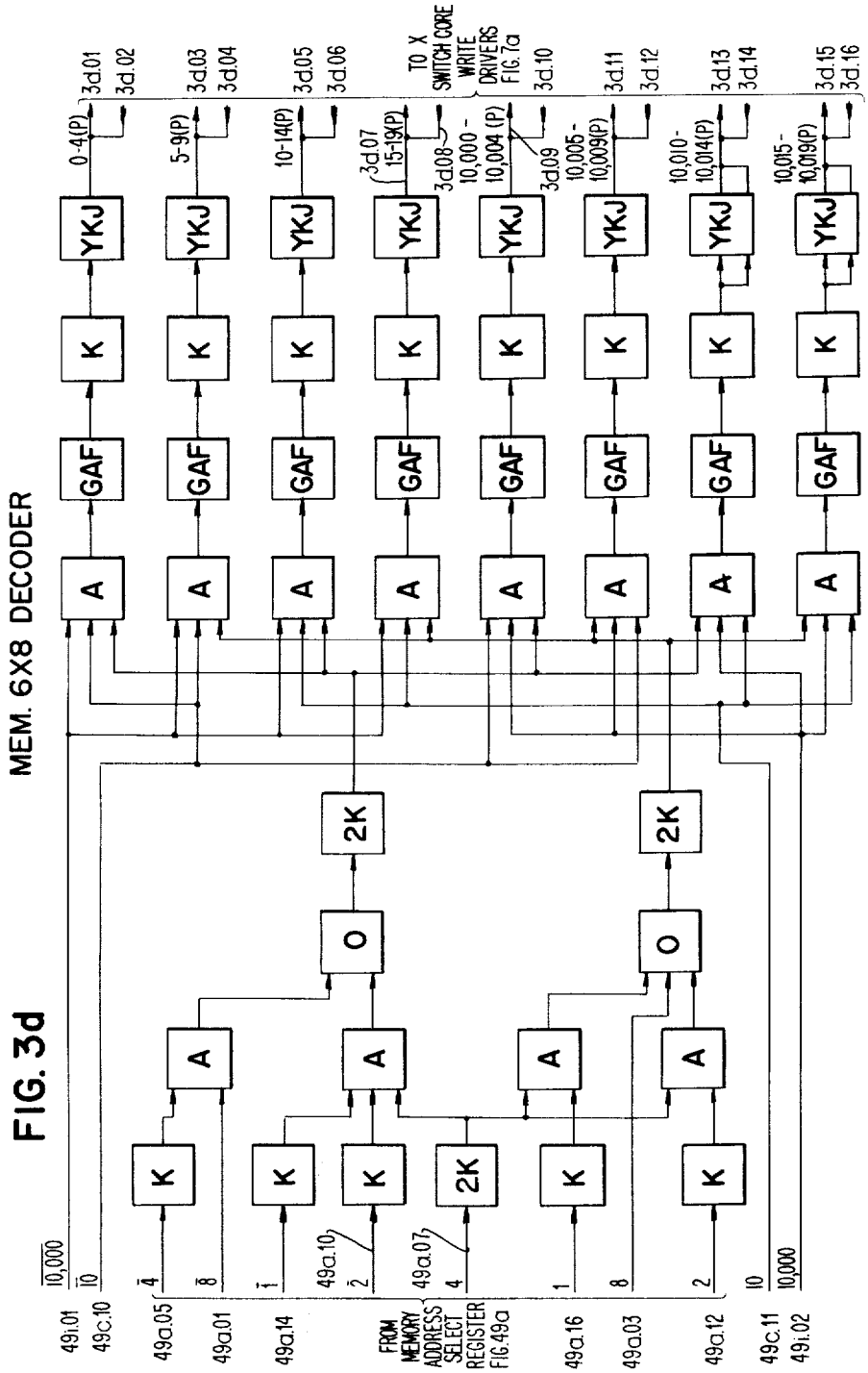
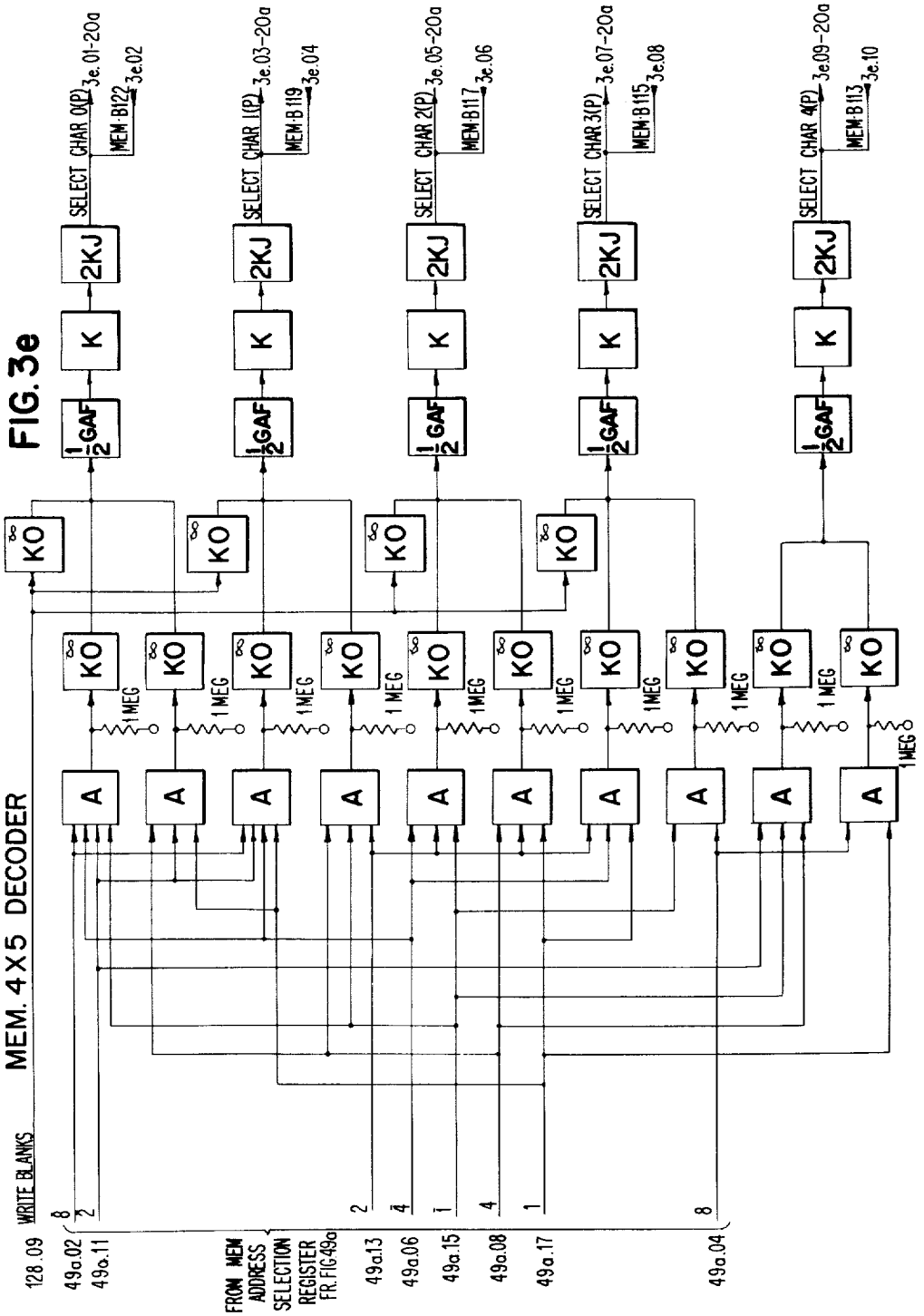

MEM. 6X8 DECODER
TO X SWITCH CORE WRITE DRIVERS FIG. 7a
0-4(P)
5-9(P)
10-14(P)
15-19(P)
10,000 - 10,004 (P)
10,005 - 10,009(P)
10,010 - 10,014(P)
10,015 - 10,019(P)
3d.01
3d.02
3d.03
3d.04
3d.05
3d.06
3d.07
3d.08
3d.09
3d.10
3d.11
3d.12
3d.13
3d.14
3d.15
3d.16
YKJ
K
GAF
A
2K
O
FROM MEMORY ADDRESS SELECT REGISTER FIG. 49a
49i.01
49c.10
49a.05
49a.01
49a.14
49a.10
49a.07
49a.16
49a.03
49a.12
49c.11
49i.02
10,000
10

FIG. 3d

FIG. 3e


MEM. 4X5 DECODER
WRITE BLANKS
128.09
49a.02
49a.11
FROM MEM ADDRESS SELECTION REGISTER FR. FIG 49a
49a.13
49a.06
49a.15
49a.08
49a.17
49a.04
SELECT CHAR 0(P)
SELECT CHAR 1(P)
SELECT CHAR 2(P)
SELECT CHAR 3(P)
SELECT CHAR 4(P)
MEM B122
MEM B119
MEM B117
MEM B115
MEM B113
1 MEG
KO
A
K
2KJ
GAF

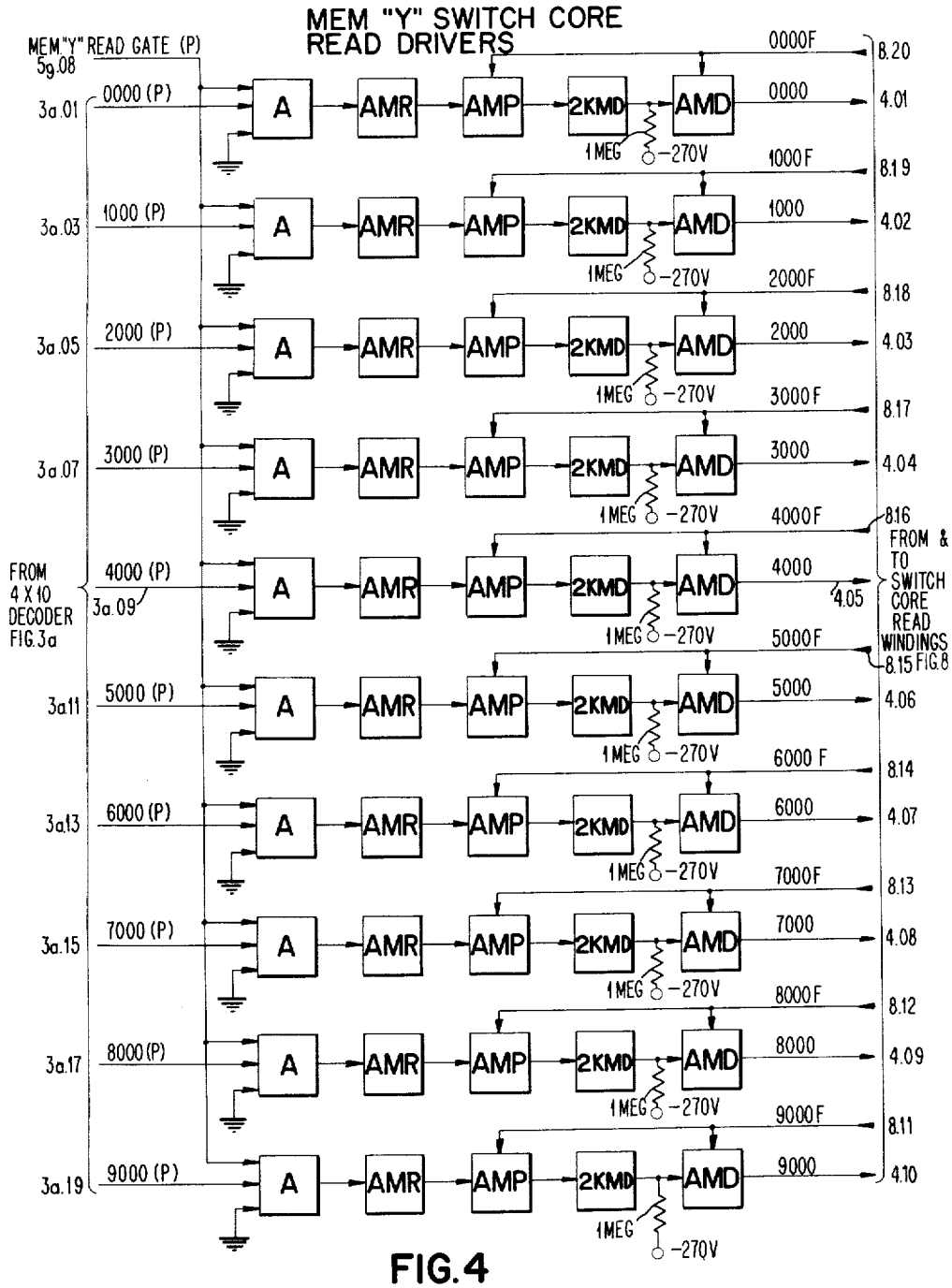
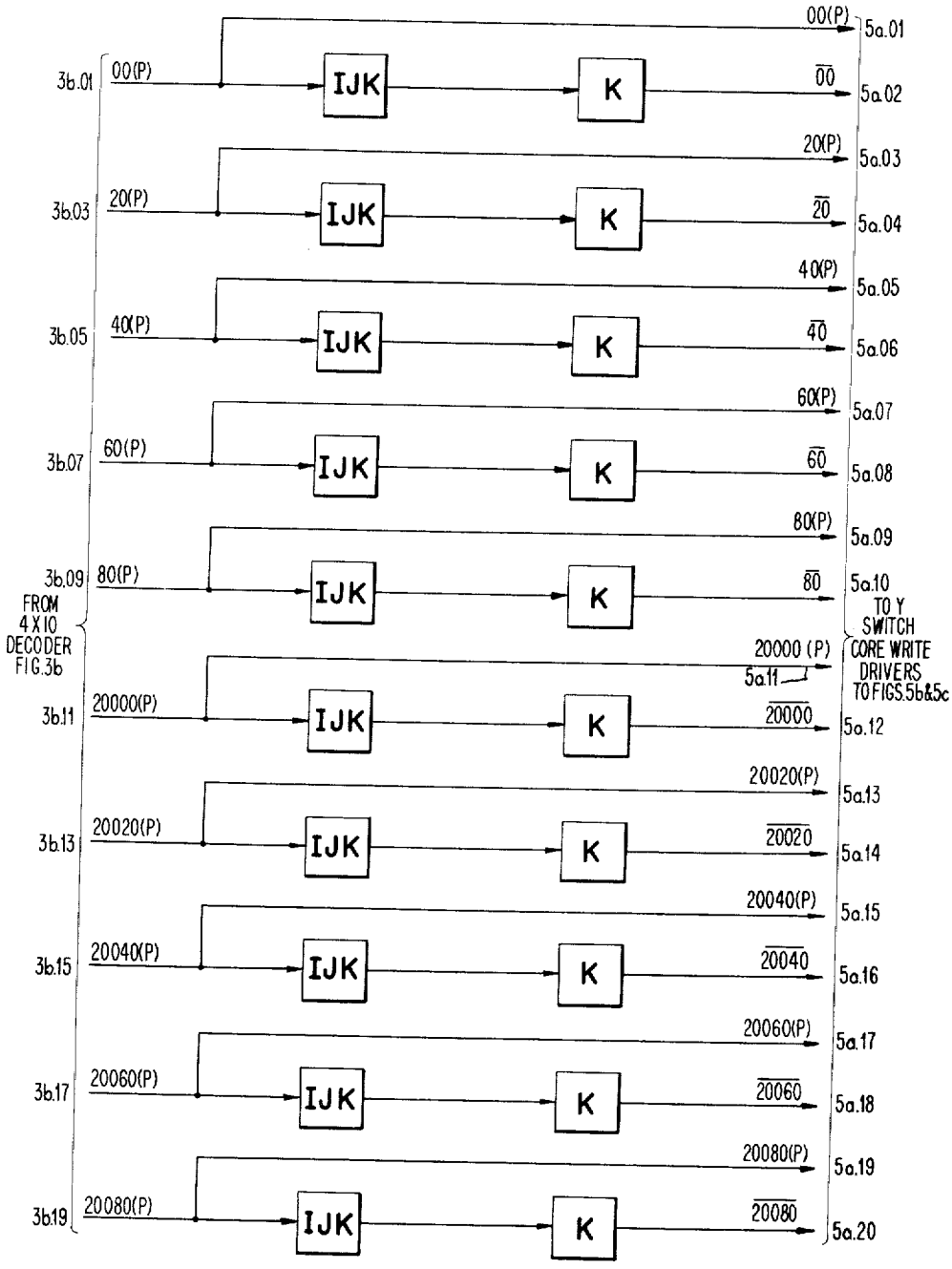

MEM "Y" SWITCH CORE READ DRIVERS
MEM "Y" READ GATE (P) 5g.08
0000F
8.20
3a.01
0000 (P)
A
AMR
AMP
2KMD
AMD
0000
4.01
1MEG
-270V
1000F
8.19
3a.03
1000 (P)
1000
4.02
2000F
8.18
3a.05
2000 (P)
2000
4.03
3000F
8.17
3a.07
3000 (P)
3000
4.04
4000F
8.16
FROM & TO SWITCH CORE READ WINDINGS 8.15 FIG.8
FROM 4 X 10 DECODER FIG.3a
4000 (P)
3a.09
4000
4.05
5000F
3a.11
5000 (P)
5000
4.06
6000 F
8.14
3a.13
6000 (P)
6000
4.07
7000F
8.13
3a.15
7000 (P)
7000
4.08
8000F
8.12
3a.17
8000 (P)
8000
4.09
9000F
8.11
3a.19
9000 (P)
9000
4.10

FIG.4

FIG.5a

4 X 10 DECODER OUTPUT INVERTERS



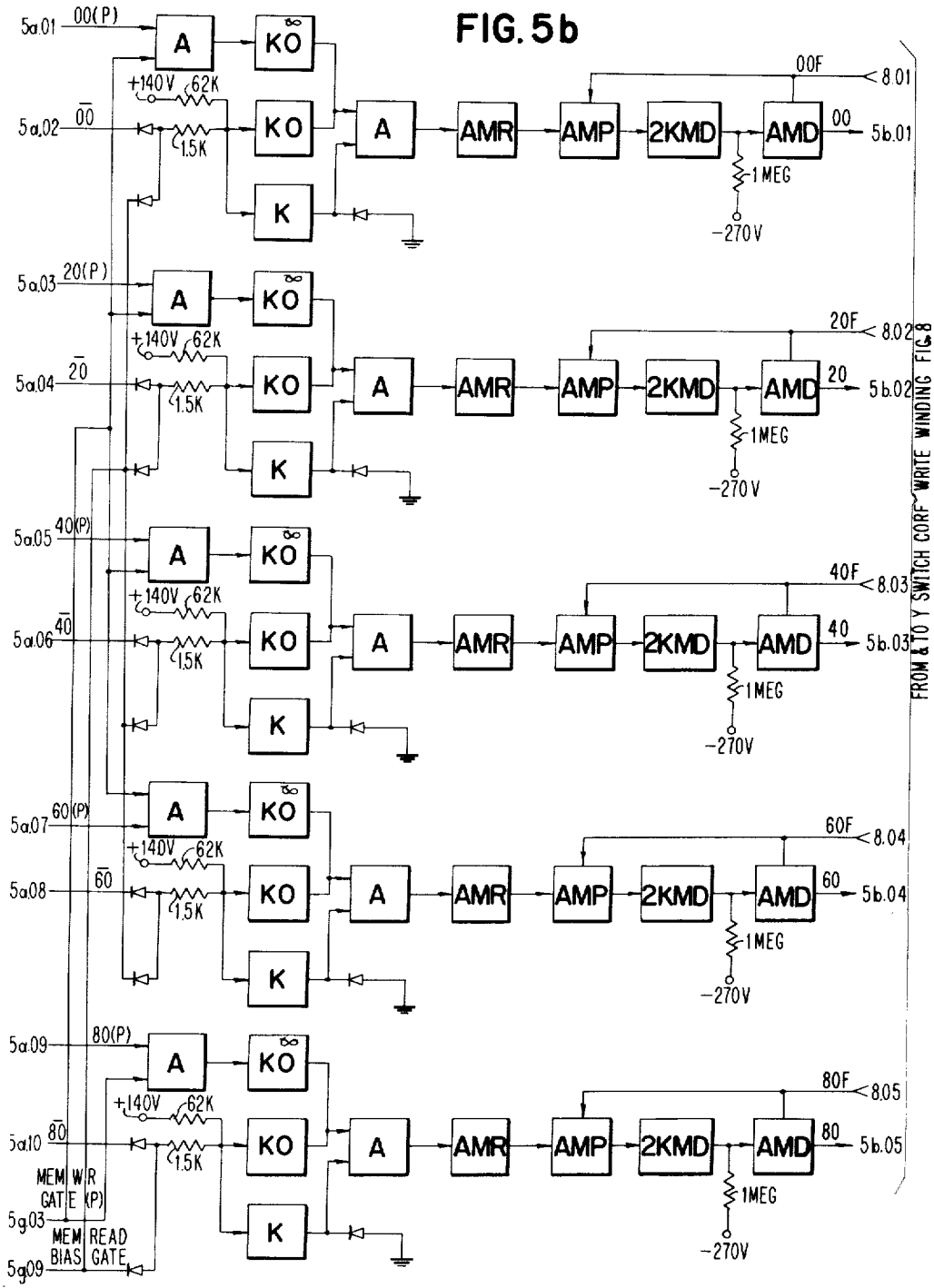
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MEM Y SWITCH CORE WRITE DRIVERS

FIG. 5b



MEM Y SWITCH CORE WRITE DRIVERS

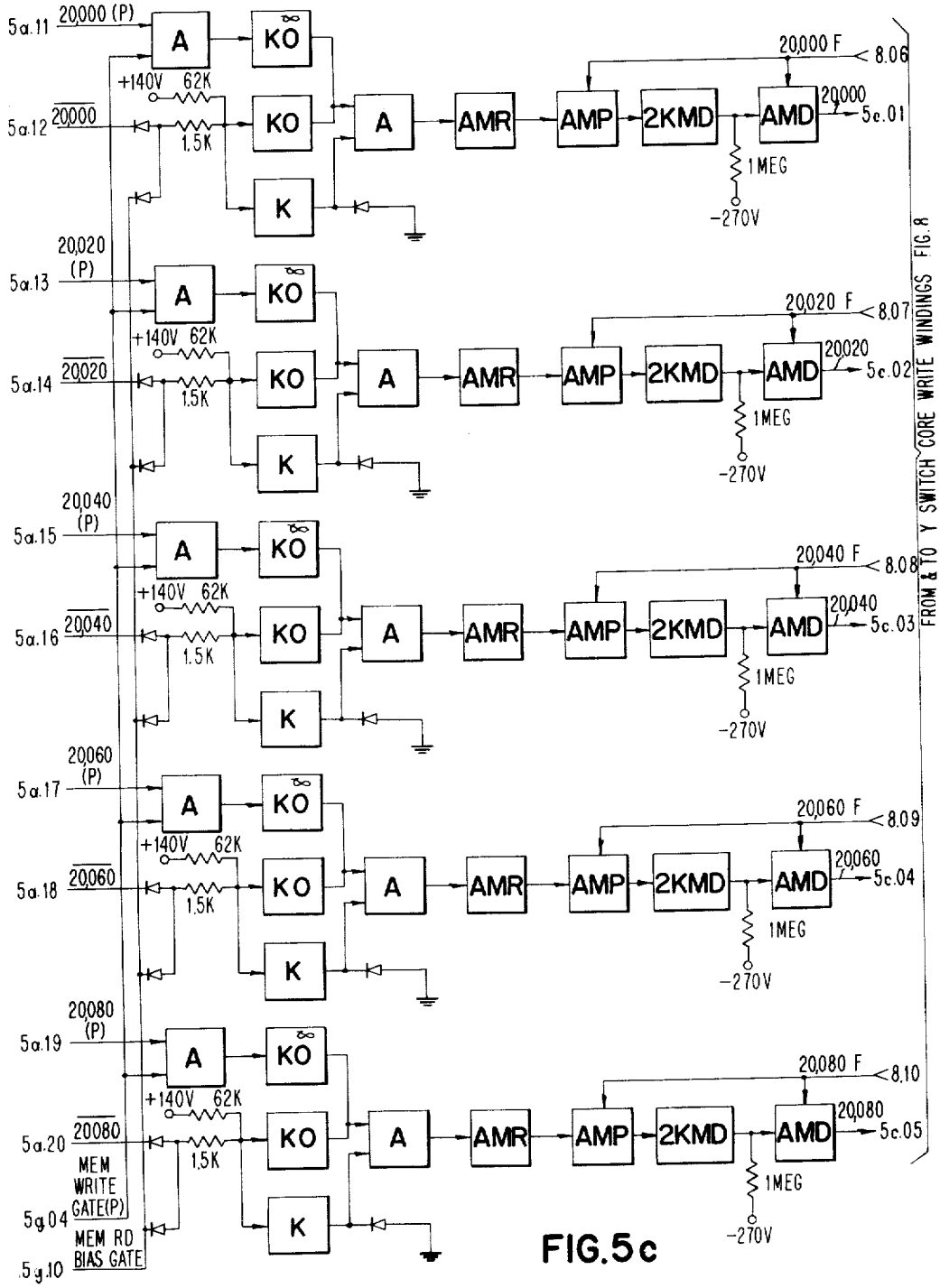
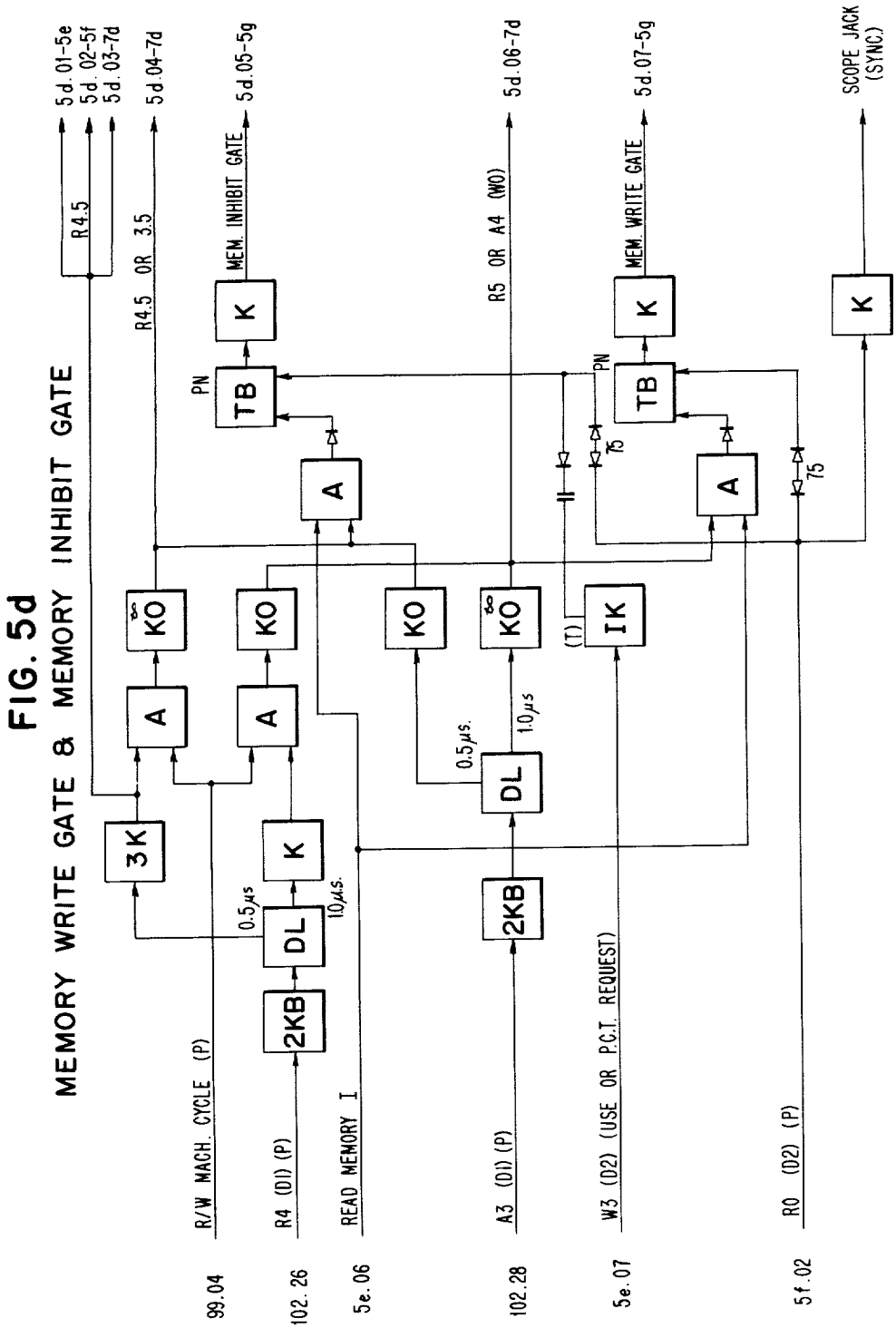


FIG. 5c


MEMORY WRITE GATE & MEMORY INHIBIT GATE
5d.01-5e
5d.02-5f
5d.03-7d
5d.04-7d
5d.05-5g
5d.06-7d
5d.07-5g
SCOPE JACK (SYNC.)
R4.5
R4.5 OR 3.5
MEM. INHIBIT GATE
R5 OR A4 (WO)
MEM. WRITE GATE
PN
TB
K
A
KO
3K
DL
2KB
IK
0.5μs.
1.0μs.
75
(T)
R/W MACH. CYCLE (P)
R4 (D1) (P)
READ MEMORY I
A3 (D1) (P)
W3 (D2) (USE OR P.C.T. REQUEST)
R0 (D2) (P)
99.04
102.26
5e.06
102.28
5e.07
5f.02
-12 CLAMP 5h.04

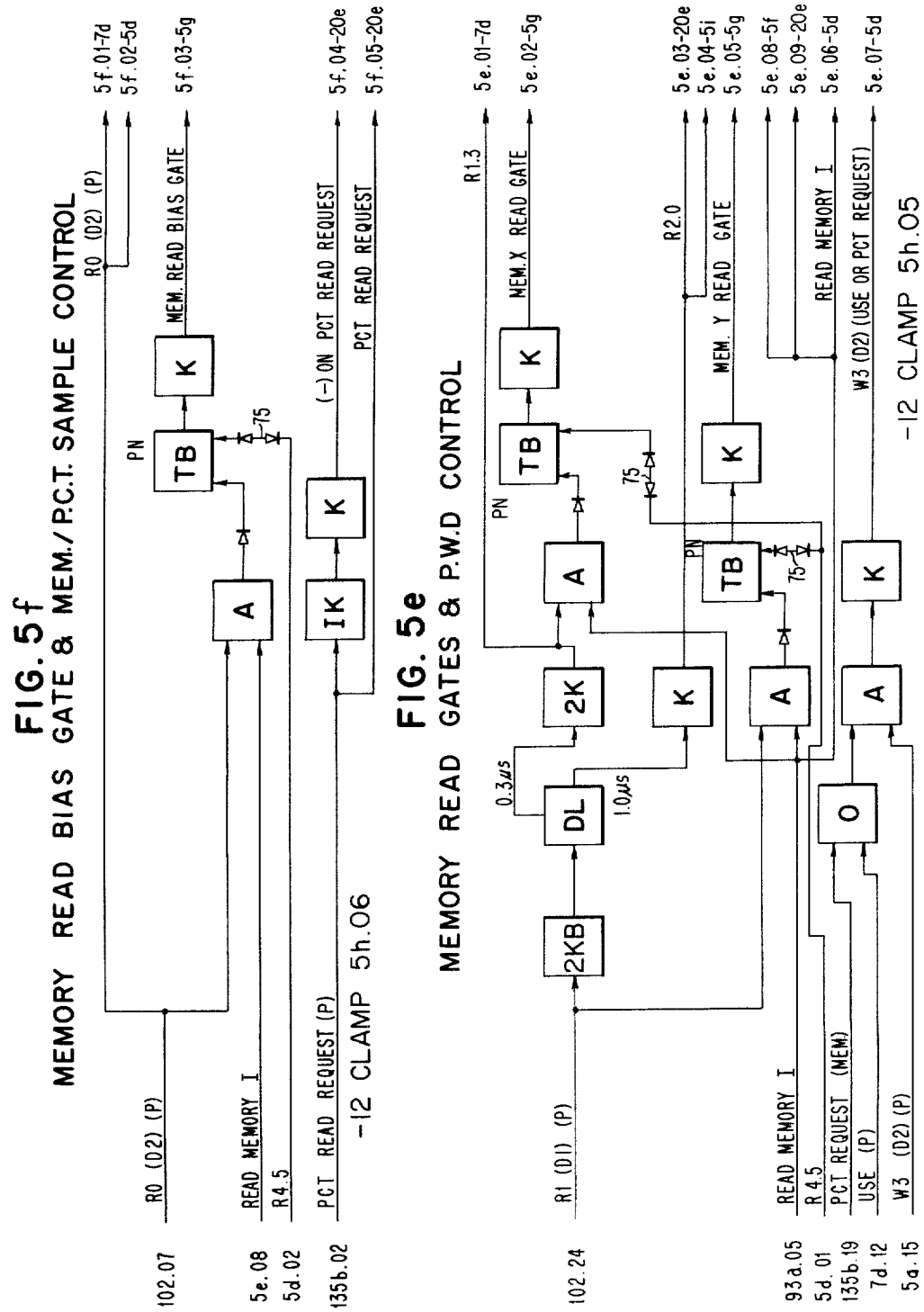

FIG. 5f
MEMORY READ BIAS GATE & MEM./P.C.T. SAMPLE CONTROL
R0 (02) (P)
5f.01-7d
5f.02-5d
5f.03-5g
MEM. READ BIAS GATE
K
TB
PN
75
A
IK
(-) ON PCT READ REQUEST
PCT READ REQUEST
5f.04-20e
5f.05-20e
102.07
5e.08
5d.02
135b.02
R0 (02) (P)
READ MEMORY I
R4.5
PCT READ REQUEST (P)
-12 CLAMP 5h.06
FIG. 5e
MEMORY READ GATES & P.W.D CONTROL
R1.3
5e.01-7d
5e.02-5g
MEM.X READ GATE
2K
2KB
DL
0.3μs
1.0μs
R2.0
5e.03-20e
5e.04-5i
5e.05-5g
MEM. Y READ GATE
5e.08-5f
5e.09-20e
5e.06-5d
READ MEMORY I
5e.07-5d
W3 (D2) (USE OR PCT REQUEST)
-12 CLAMP 5h.05
O
R1 (01) (P)
READ MEMORY I
R4.5
PCT REQUEST (MEM)
USE (P)
W3 (D2) (P)
102.24
93a.05
5d.01
135b.19
7d.12
5a.15

FIG. 5g

MEMORY GATE POWERING & M.B.R. RESET

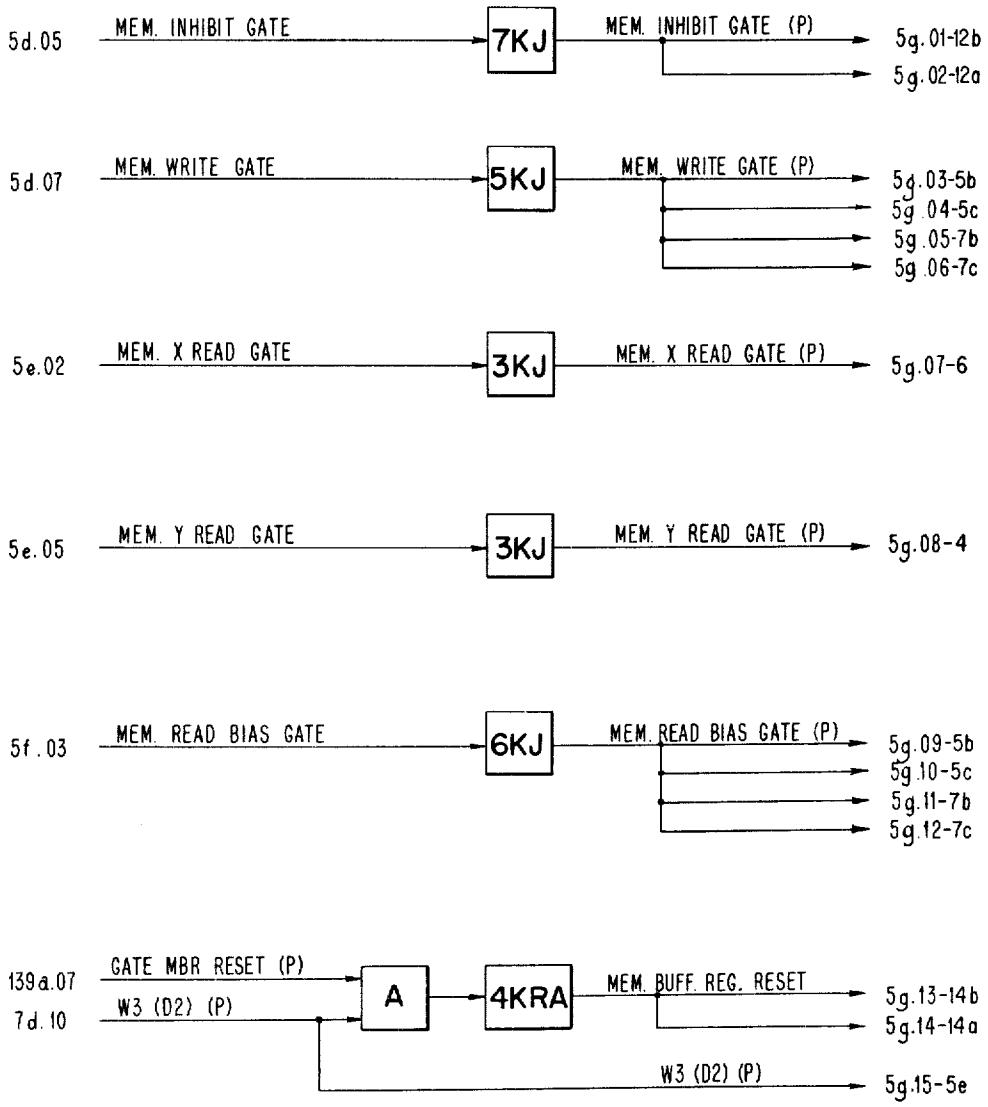


FIG. 5h
MEMORY CLAMPS & SENSE AMP. BIAS VOLTAGE

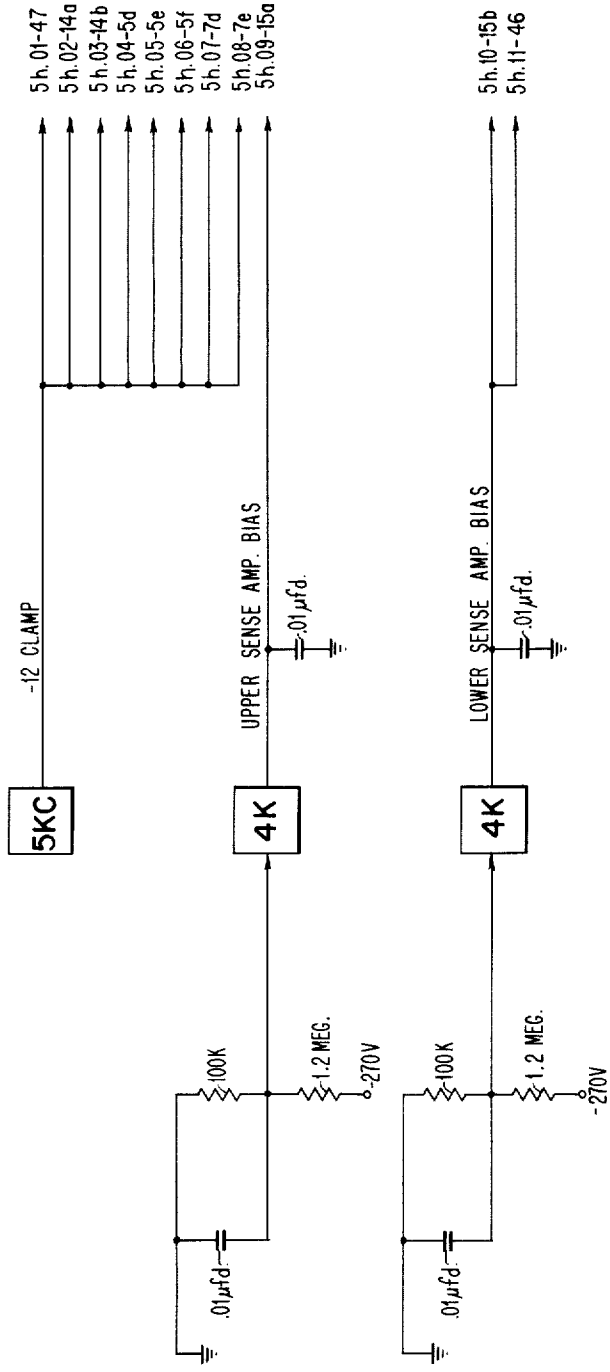


FIG. 5i
STORAGE SAMPLE PULSE GENERATOR

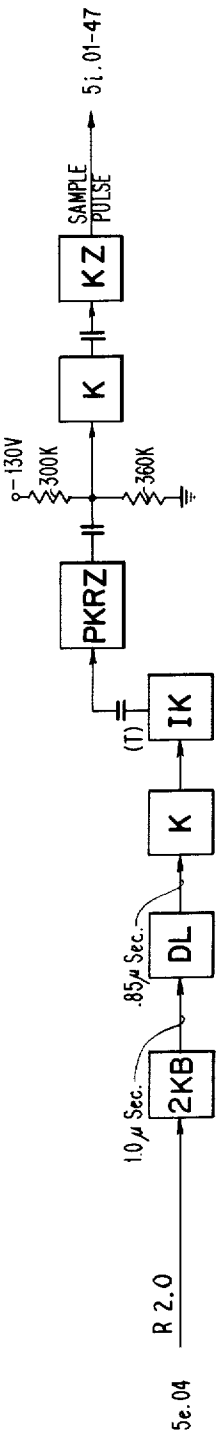


FIG.6

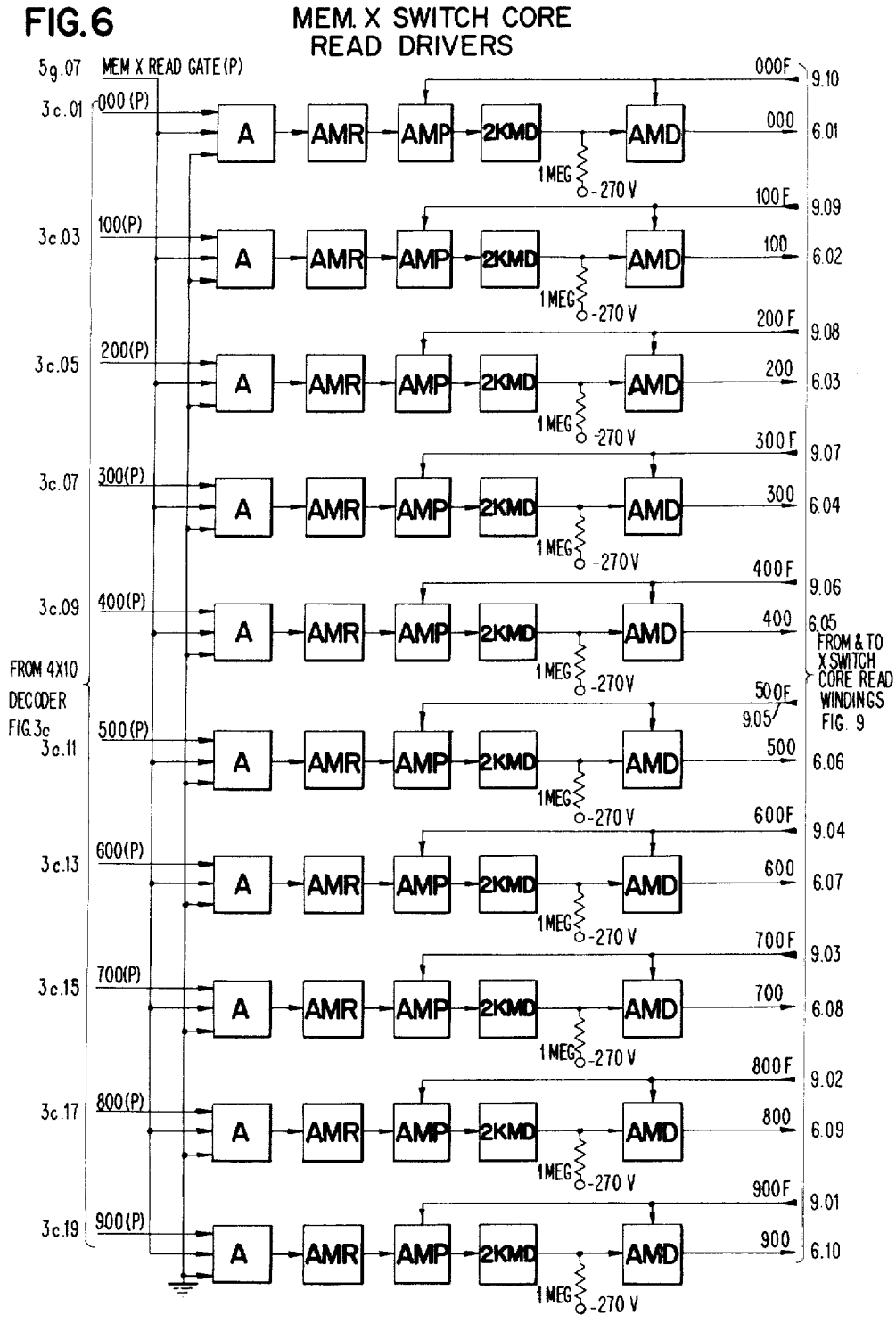
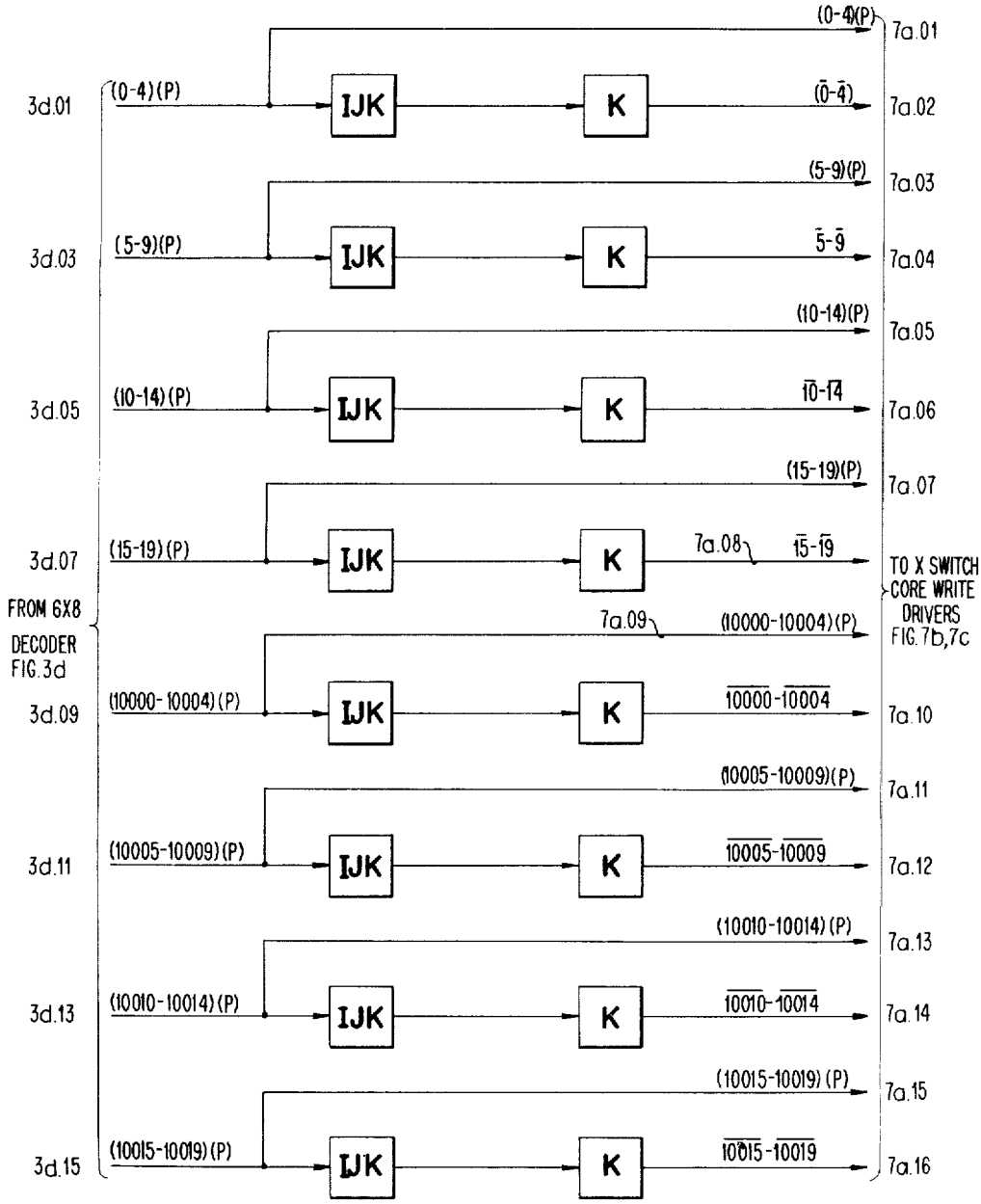

MEM. X SWITCH CORE READ DRIVERS
5g.07 MEM X READ GATE (P)
3c.01 000 (P)
3c.03 100(P)
3c.05 200(P)
3c.07 300(P)
3c.09 400(P)
FROM 4X10 DECODER FIG.3c
3c.11 500(P)
3c.13 600(P)
3c.15 700(P)
3c.17 800(P)
3c.19 900(P)
A
AMR
AMP
2KMD
AMD
1 MEG
-270 V
000F 9.10
000 6.01
100F 9.09
100 6.02
200F 9.08
200 6.03
300F 9.07
300 6.04
400F 9.06
400 6.05
500F 9.05
500 6.06
600F 9.04
600 6.07
700F 9.03
700 6.08
800F 9.02
800 6.09
900F 9.01
900 6.10
FROM & TO X SWITCH CORE READ WINDINGS FIG. 9

FIG. 7a

6 X 8 DECODER OUTPUT INVERTERS



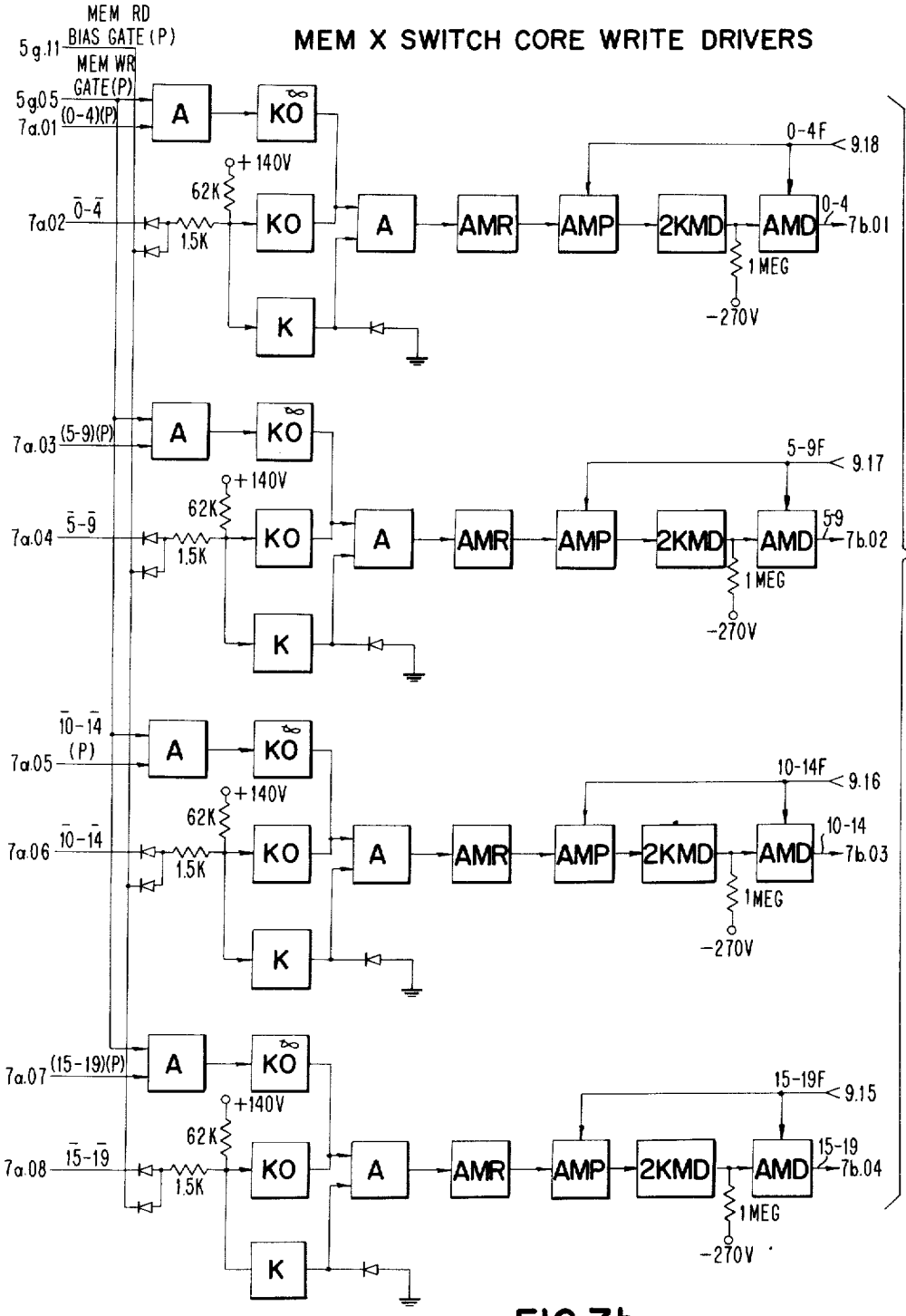

MEM X SWITCH CORE WRITE DRIVERS
MEM RD BIAS GATE (P)
5g.11
MEM WR GATE (P)
5g.05
(0-4)(P)
7a.01
7a.02 0-4
7a.03 (5-9)(P)
7a.04 5-9
7a.05 10-14 (P)
7a.06 10-14
7a.07 (15-19)(P)
7a.08 15-19
A
KO
K
+140V
62K
1.5K
AMR
AMP
2KMD
AMD
1 MEG
-270V
0-4F 9.18
0-4 7b.01
5-9F 9.17
5-9 7b.02
10-14F 9.16
10-14 7b.03
15-19F 9.15
15-19 7b.04
FROM & TO X SWITCH CORE WRITE WINDINGS FIG 9

FIG. 7b

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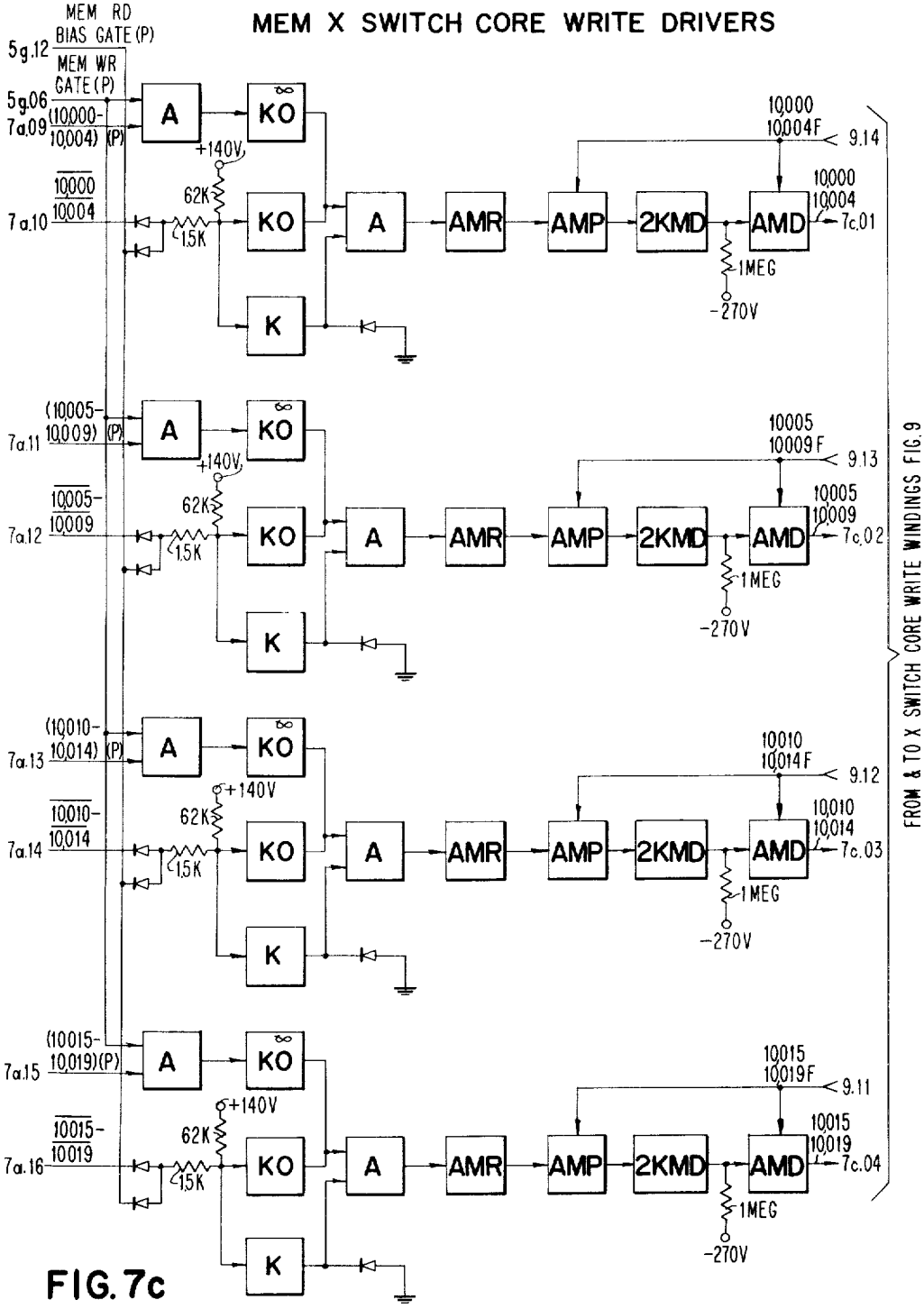


FIG. 7c

FIG. 7d

STOR. READ BIAS GT, READ GT., INHIBIT GT., WRITE GT. & BUFF REG. RESET

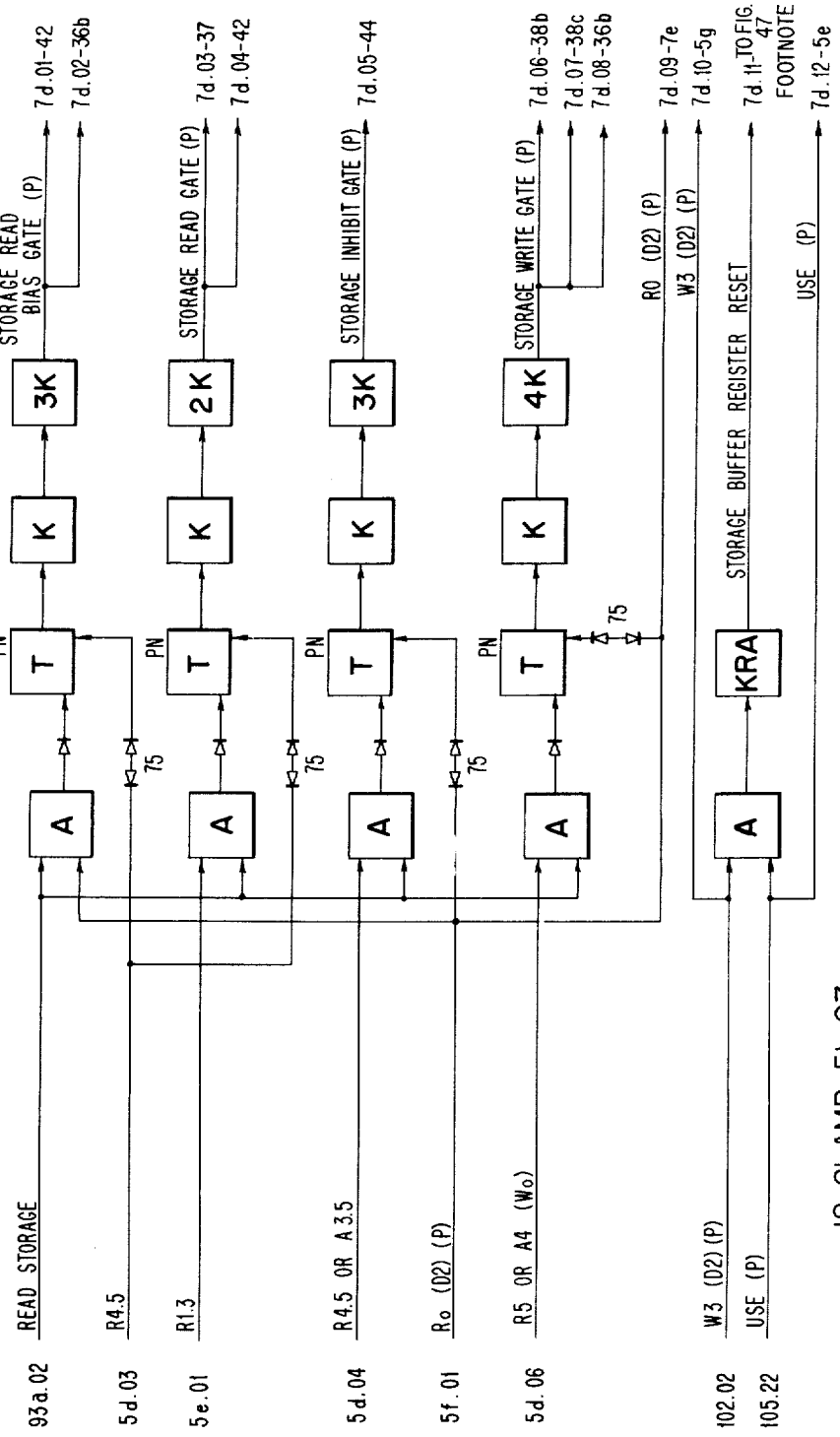
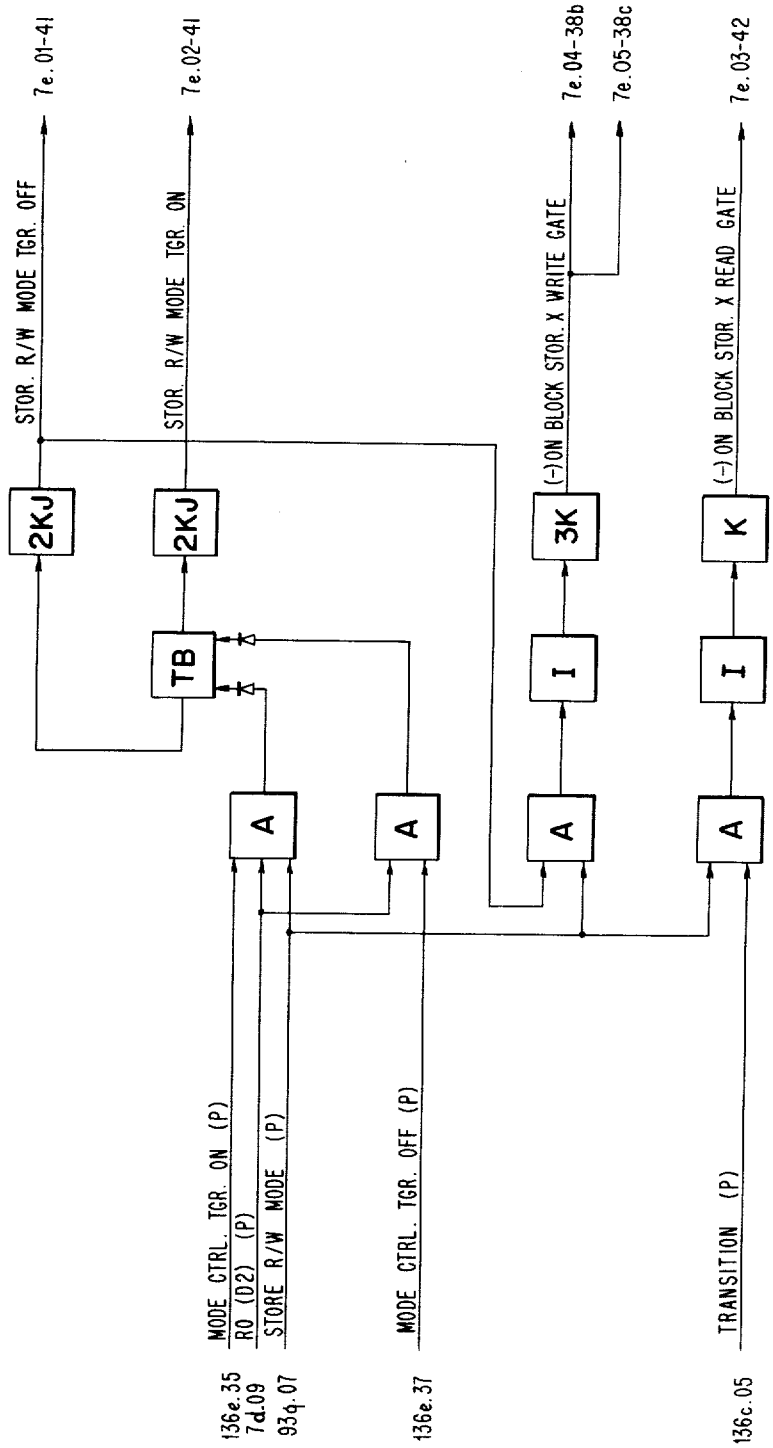


FIG. 7e
STORAGE R/W MODE CTRL.



-12 CLAMP 5h.08

FIG.8 Y SWITCH CORE MATRIX

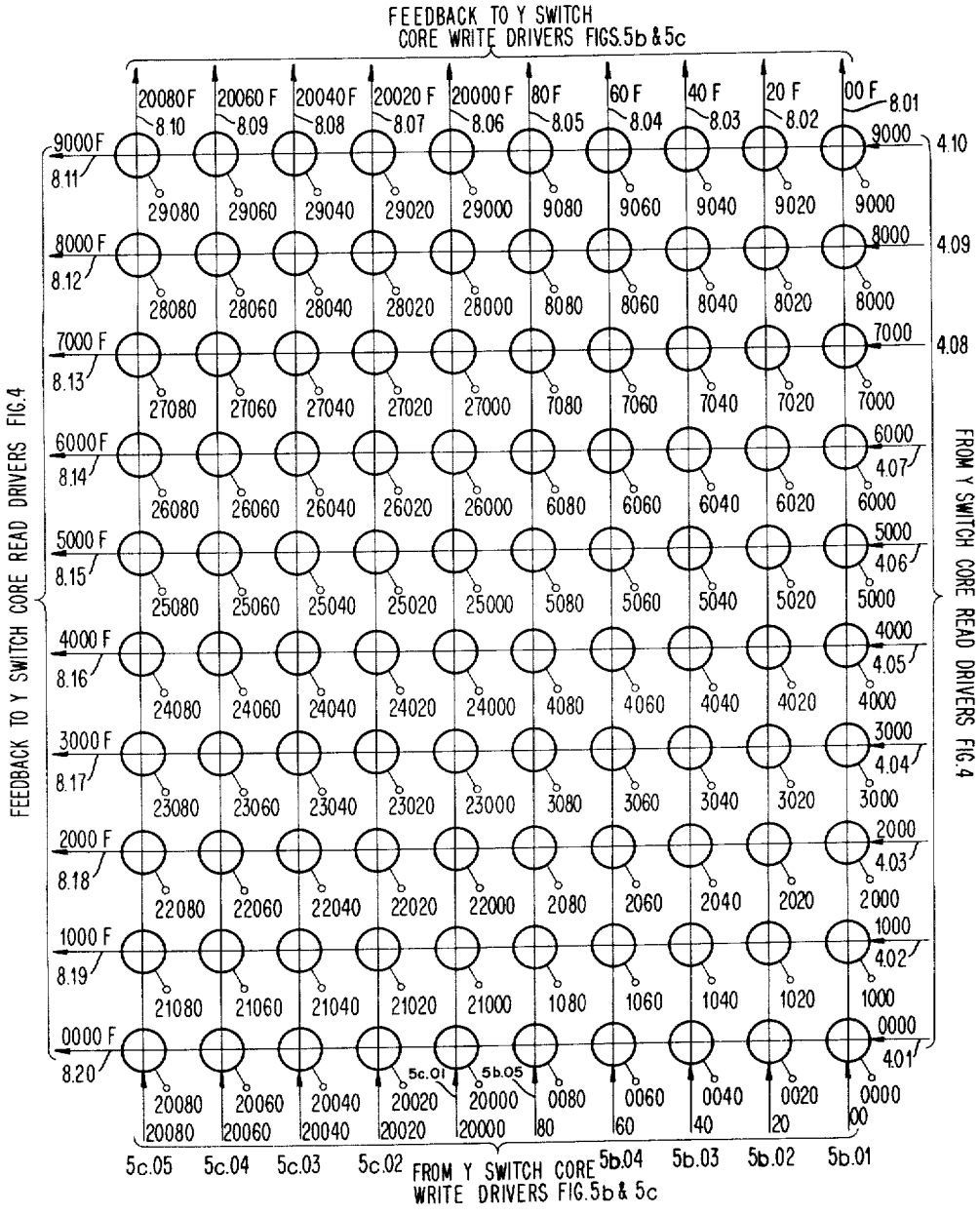


FIG.9

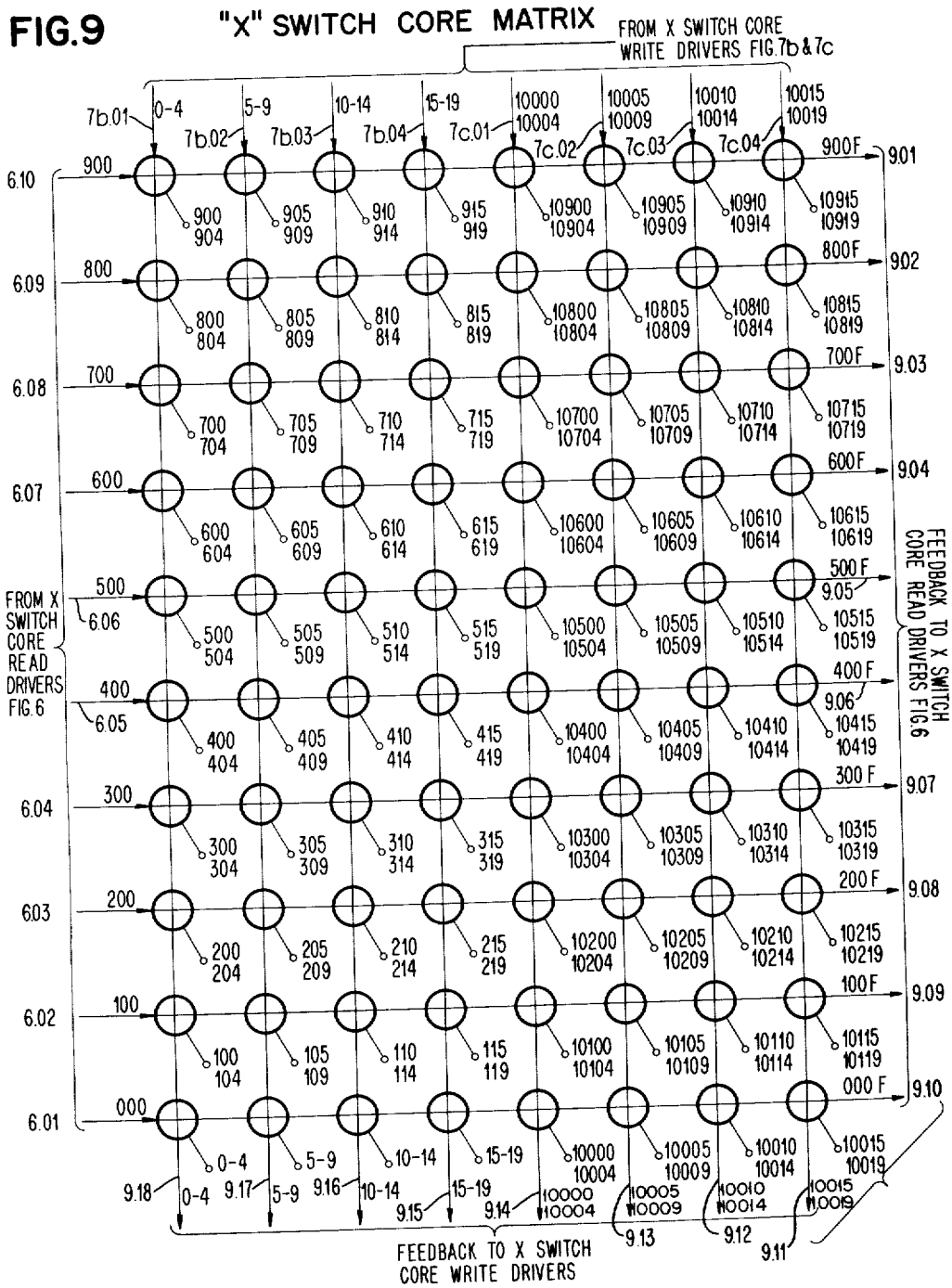
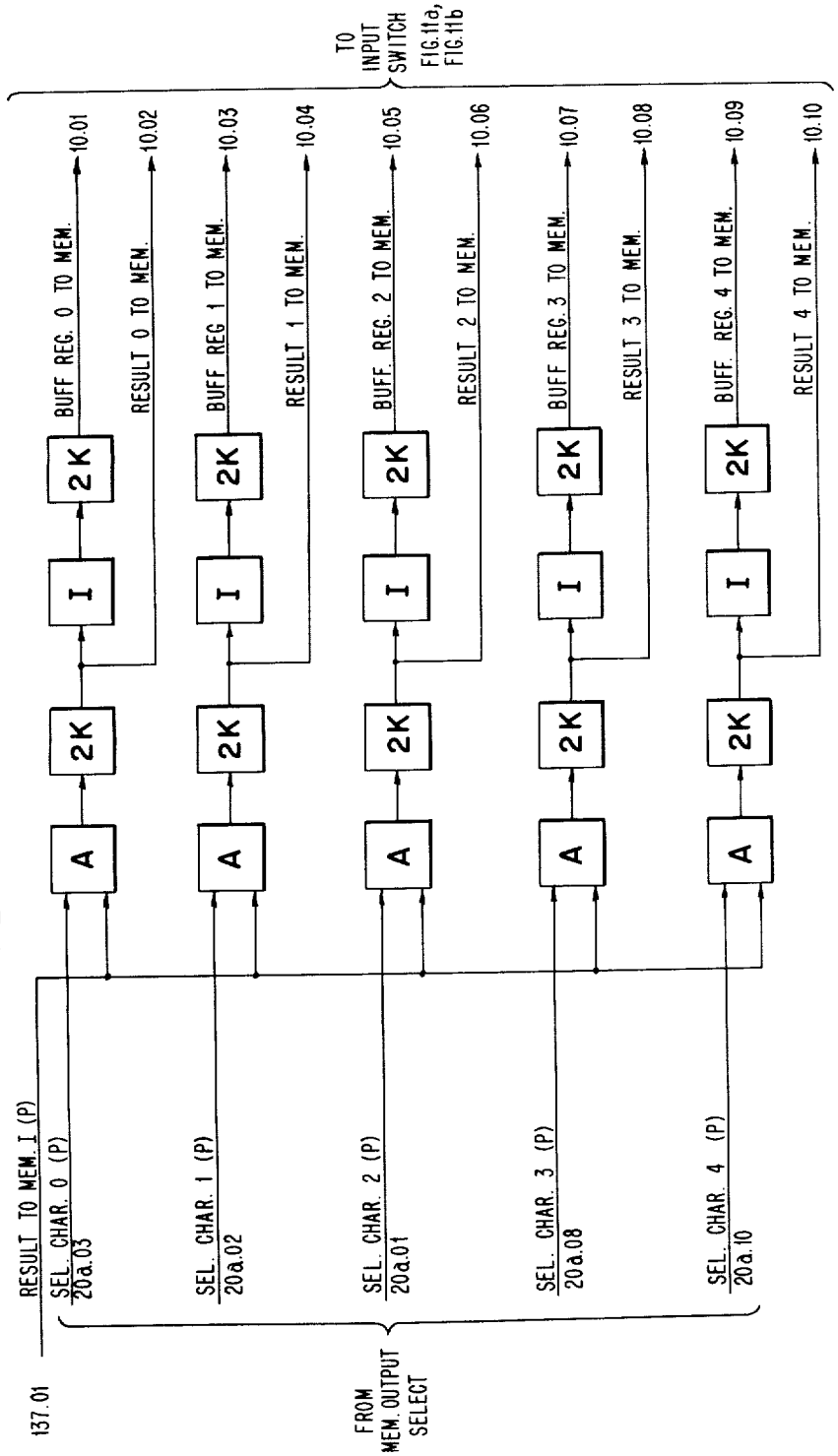

"X" SWITCH CORE MATRIX
FROM X SWITCH CORE WRITE DRIVERS FIG.7b&7c
7b.01
0-4
7b.02
5-9
7b.03
10-14
7b.04
15-19
7c.01
10000 10004
7c.02
10005 10009
7c.03
10010 10014
7c.04
10015 10019
900
900F
9.01
6.10
900 904
905 909
910 914
915 919
10900 10904
10905 10909
10910 10914
10915 10919
800
800F
9.02
6.09
800 804
805 809
810 814
815 819
10800 10804
10805 10809
10810 10814
10815 10819
700
700F
9.03
6.08
700 704
705 709
710 714
715 719
10700 10704
10705 10709
10710 10714
10715 10719
600
600F
9.04
6.07
600 604
605 609
610 614
615 619
10600 10604
10605 10609
10610 10614
10615 10619
500
500 F
9.05
FROM X SWITCH CORE READ DRIVERS FIG.6
6.06
500 504
505 509
510 514
515 519
10500 10504
10505 10509
10510 10514
10515 10519
400
400 F
9.06
6.05
400 404
405 409
410 414
415 419
10400 10404
10405 10409
10410 10414
10415 10419
300
300 F
9.07
6.04
300 304
305 309
310 314
315 319
10300 10304
10305 10309
10310 10314
10315 10319
200
200 F
9.08
6.03
200 204
205 209
210 214
215 219
10200 10204
10205 10209
10210 10214
10215 10219
100
100F
9.09
6.02
100 104
105 109
110 114
115 119
10100 10104
10105 10109
10110 10114
10115 10119
000
000 F
9.10
6.01
0-4
5-9
10-14
15-19
10000 10004
10005 10009
10010 10014
10015 10019
9.18
0-4
9.17
5-9
9.16
10-14
9.15
15-19
9.14
10000 10004
9.13
10005 10009
9.12
10010 10014
9.11
10015 10019
FEEDBACK TO X SWITCH CORE WRITE DRIVERS
FEEDBACK TO X SWITCH CORE READ DRIVERS FIG.6

FIG. 10
MEM INPUT SELECT



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FIG. 11a MEM. INPUT SWITCH CHAR. 4,3,2

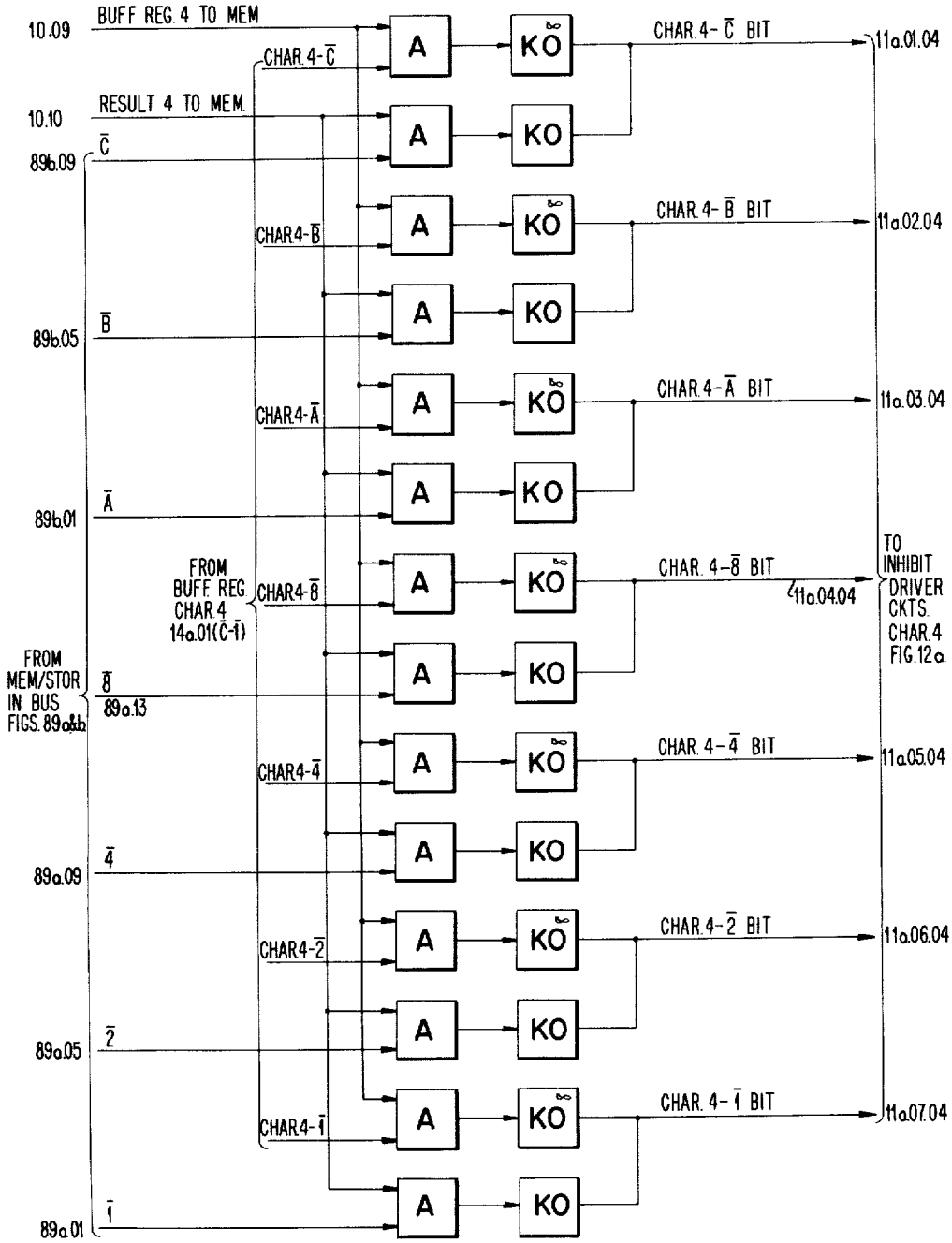


FIG.11b MEM. INPUT SWITCH CHAR. 0 & 1

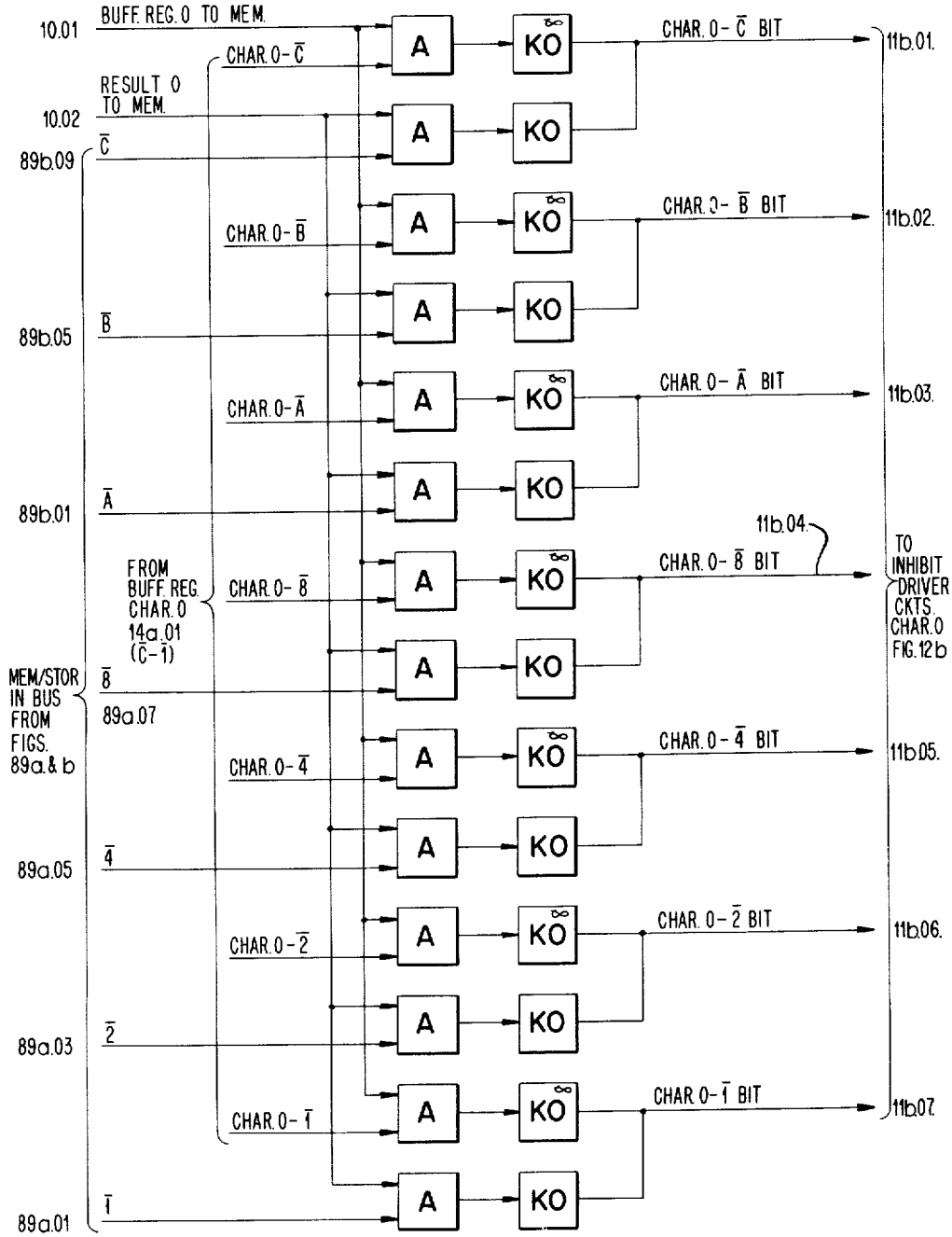


FIG.12a MEM. INHIBIT DRIVER CIRCUITS CHAR. 4,3 & 2

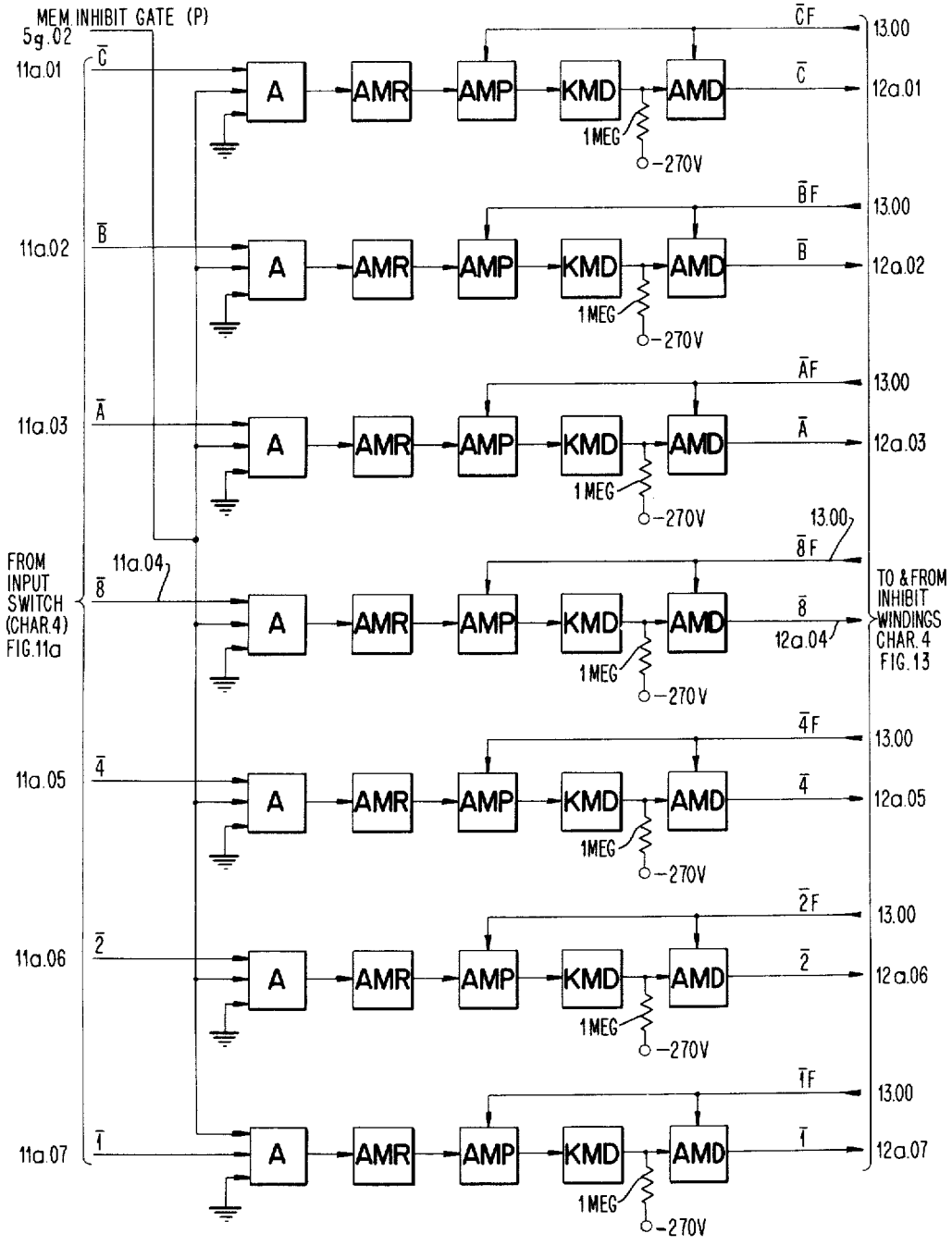


FIG.12b

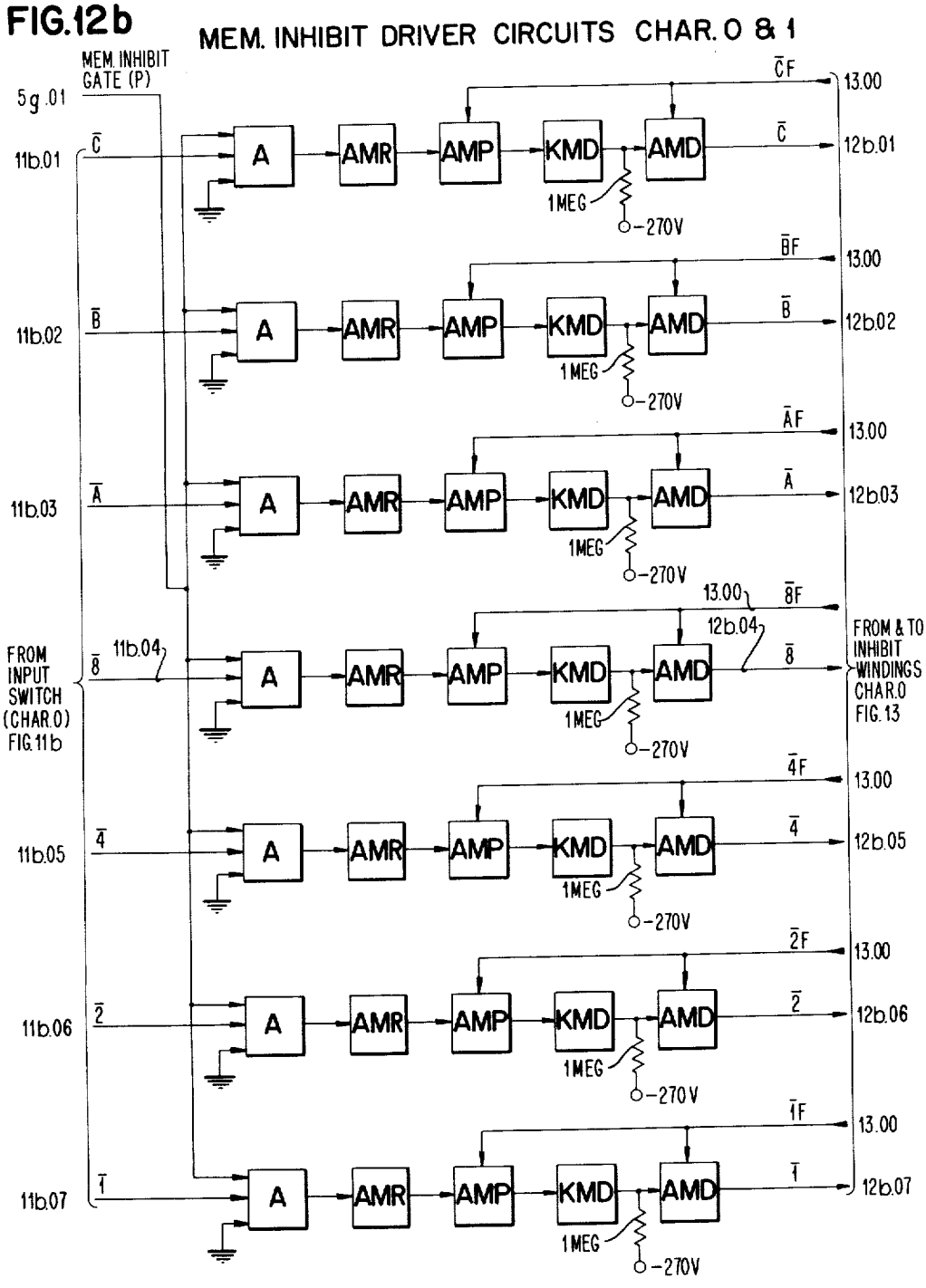
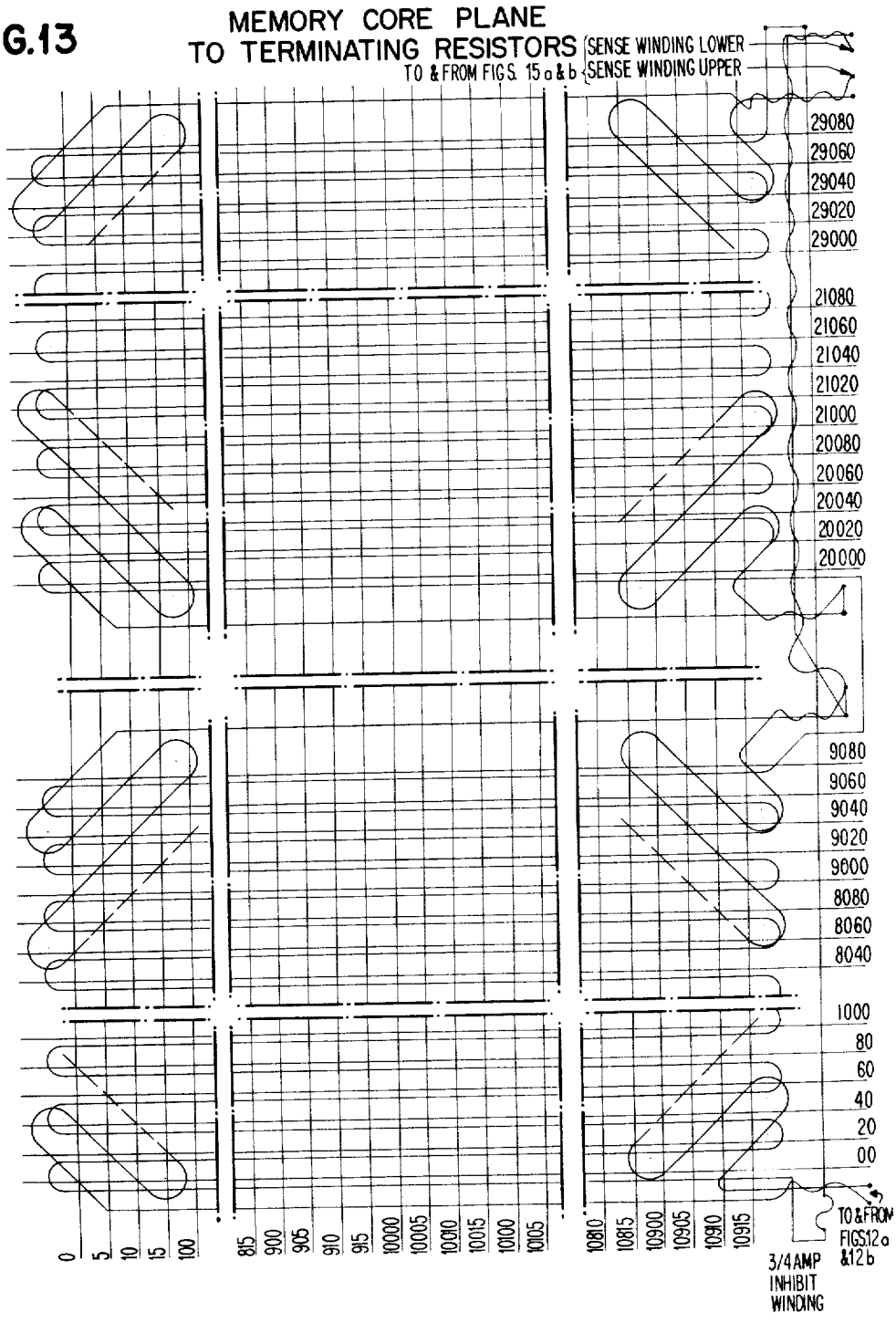

MEM. INHIBIT DRIVER CIRCUITS CHAR. 0 & 1
MEM. INHIBIT GATE (P)
5g.01
11b.01
11b.02
11b.03
11b.04
11b.05
11b.06
11b.07
FROM INPUT SWITCH (CHAR.0) FIG.11b
A
AMR
AMP
KMD
AMD
1MEG
-270V
13.00
12b.01
12b.02
12b.03
12b.04
12b.05
12b.06
12b.07
FROM & TO INHIBIT WINDINGS CHAR.0 FIG.13

FIG.13


MEMORY CORE PLANE
TO TERMINATING RESISTORS
TO & FROM FIGS. 15a & b
SENSE WINDING LOWER
SENSE WINDING UPPER
29080
29060
29040
29020
29000
21080
21060
21040
21020
21000
20080
20060
20040
20020
20000
9080
9060
9040
9020
9000
8080
8060
8040
1000
80
60
40
20
00
0
5
10
15
100
815
900
905
910
915
10000
10005
10010
10015
10100
10105
10810
10815
10900
10905
10910
10915
TO & FROM FIGS 12a & 12b
3/4 AMP INHIBIT WINDING

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FIG. 14a

MEMORY BUFFER REGISTER CHAR. 4,3 & 2

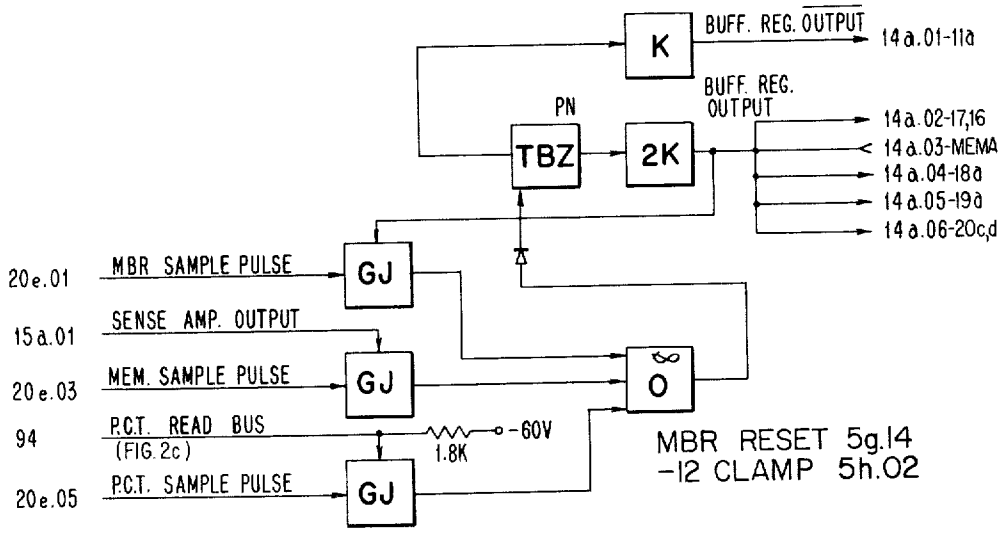


FIG. 14b

MEMORY BUFFER REGISTER CHAR. 0 & 1

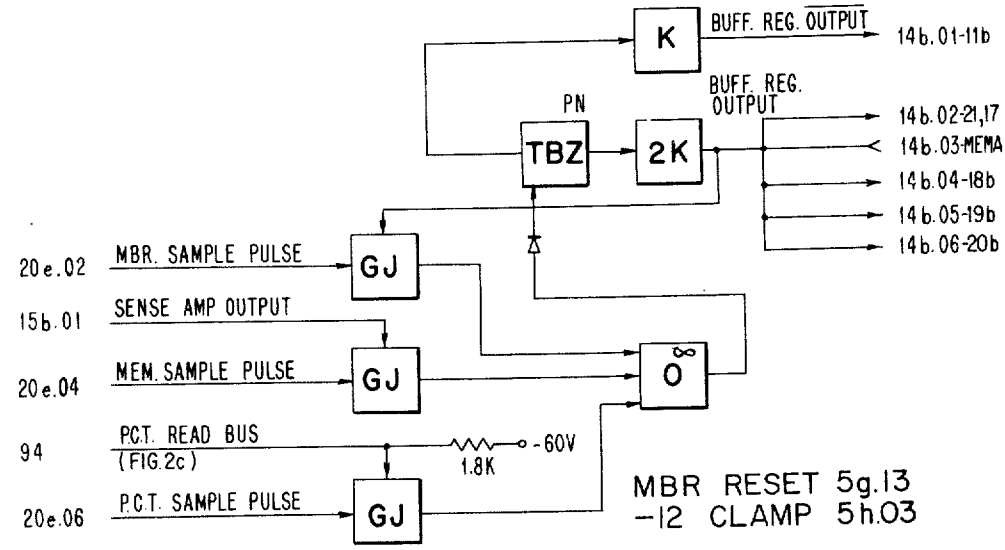


FIG. 15a
UPPER SENSE AMPLIFIER CIRCUITS
(TYPICAL OF ALL CHAR. 4,3&2 SENSE AMP.)

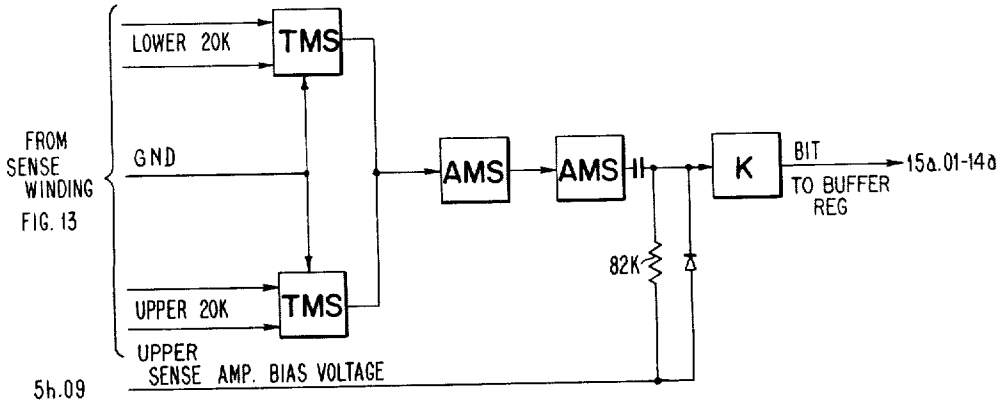


FIG. 15b
LOWER SENSE AMPLIFIER CIRCUITS
(TYPICAL OF ALL CHAR. 0 & 1 SENSE AMP.)

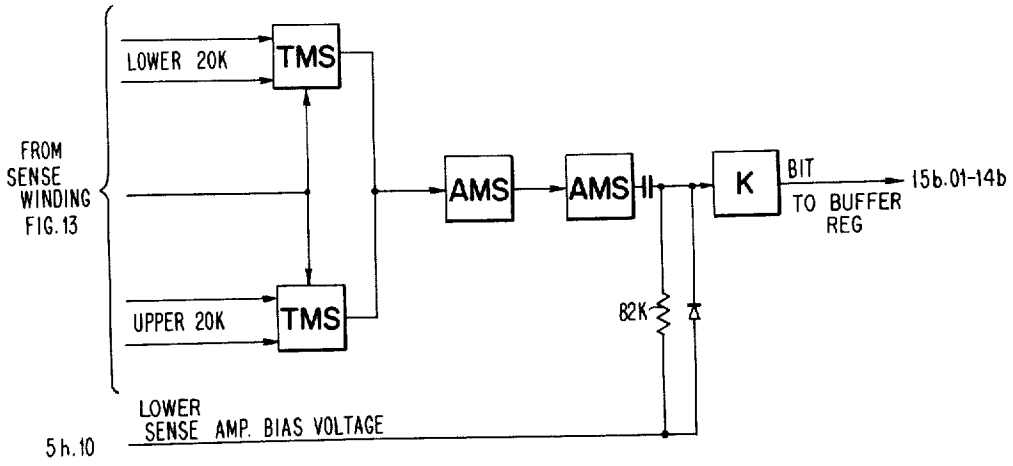


FIG. 16a

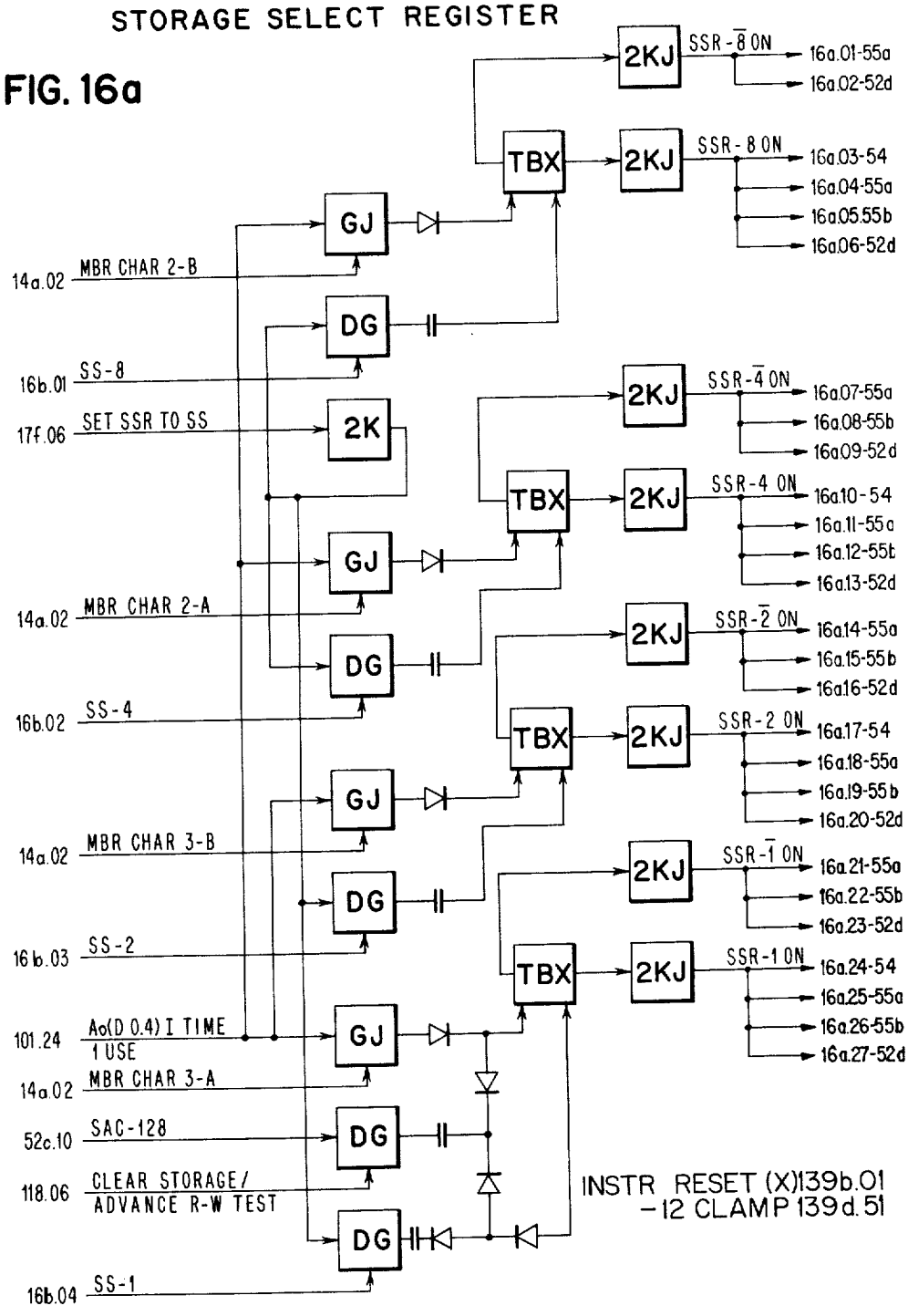
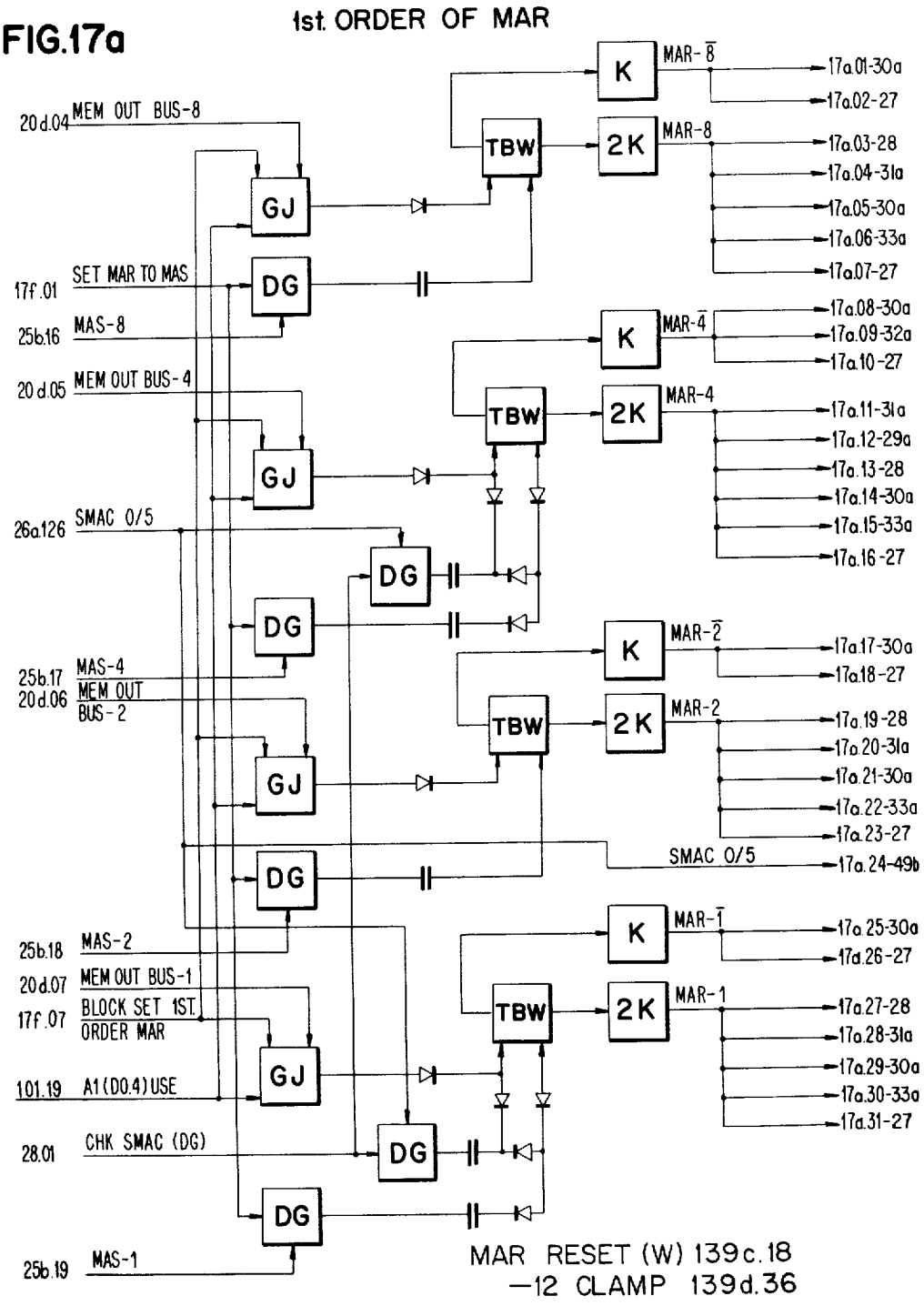

STORAGE SELECT REGISTER
2KJ
SSR-$\bar{8}$ ON
16a.01-55a
16a.02-52d
TBX
2KJ
SSR-8 ON
16a.03-54
16a.04-55a
16a.05-55b
16a.06-52d
GJ
14a.02 MBR CHAR 2-B
DG
16b.01 SS-8
17f.06 SET SSR TO SS
2K
2KJ
SSR-$\bar{4}$ ON
16a.07-55a
16a.08-55b
16a.09-52d
TBX
2KJ
SSR-4 ON
16a.10-54
16a.11-55a
16a.12-55b
16a.13-52d
GJ
14a.02 MBR CHAR 2-A
DG
2KJ
SSR-$\bar{2}$ ON
16a.14-55a
16a.15-55b
16a.16-52d
16b.02 SS-4
TBX
2KJ
SSR-2 ON
16a.17-54
16a.18-55a
16a.19-55b
16a.20-52d
GJ
14a.02 MBR CHAR 3-B
DG
2KJ
SSR-$\bar{1}$ ON
16a.21-55a
16a.22-55b
16a.23-52d
16b.03 SS-2
TBX
2KJ
SSR-1 ON
16a.24-54
16a.25-55a
16a.26-55b
16a.27-52d
101.24 Ao(D 0.4) I TIME 1 USE
GJ
14a.02 MBR CHAR 3-A
52c.10 SAC-128
DG
118.06 CLEAR STORAGE/ ADVANCE R-W TEST
DG
16b.04 SS-1
INSTR RESET (X)139b.01
-12 CLAMP 139d.51

FIG.17a


1st ORDER OF MAR
20d.04 MEM OUT BUS-8
17f.01 SET MAR TO MAS
25b.16 MAS-8
20d.05 MEM OUT BUS-4
26a.126 SMAC 0/5
25b.17 MAS-4
20d.06 MEM OUT BUS-2
25b.18 MAS-2
20d.07 MEM OUT BUS-1
17f.07 BLOCK SET 1ST ORDER MAR
101.19 A1(D0.4) USE
28.01 CHK SMAC (DG)
25b.19 MAS-1
GJ
DG
TBW
K
2K
MAR-8
MAR-4
MAR-2
MAR-1
17a.01-30a
17a.02-27
17a.03-28
17a.04-31a
17a.05-30a
17a.06-33a
17a.07-27
17a.08-30a
17a.09-32a
17a.10-27
17a.11-31a
17a.12-29a
17a.13-28
17a.14-30a
17a.15-33a
17a.16-27
17a.17-30a
17a.18-27
17a.19-28
17a.20-31a
17a.21-30a
17a.22-33a
17a.23-27
SMAC 0/5
17a.24-49b
17a.25-30a
17a.26-27
17a.27-28
17a.28-31a
17a.29-30a
17a.30-33a
17a.31-27
MAR RESET (W) 139c.18
—12 CLAMP 139d.36

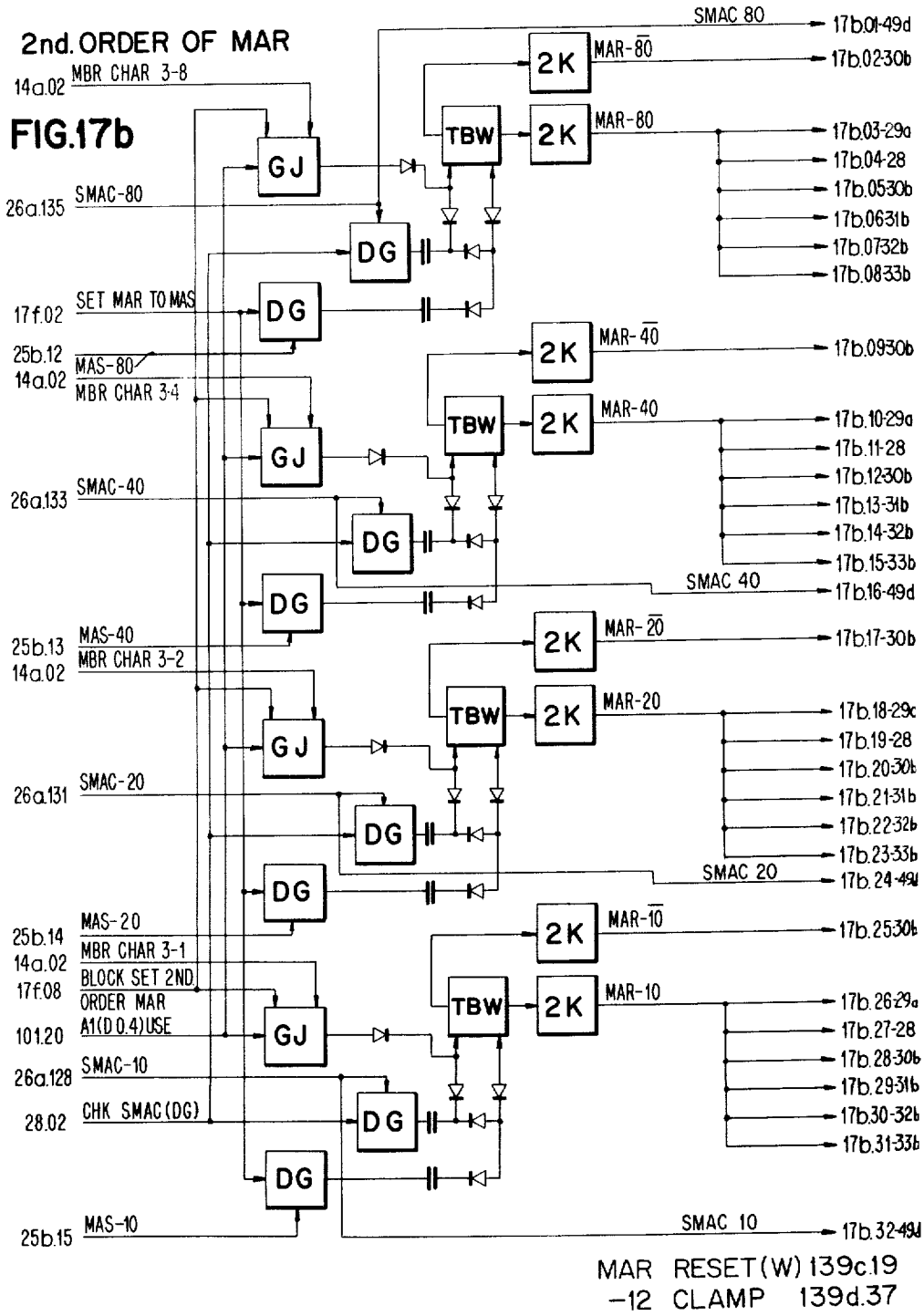

2nd. ORDER OF MAR
FIG.17b
14a.02 MBR CHAR 3-8
26a.135 SMAC-80
17f.02 SET MAR TO MAS
25b.12 MAS-80
14a.02 MBR CHAR 3-4
26a.133 SMAC-40
25b.13 MAS-40
14a.02 MBR CHAR 3-2
26a.131 SMAC-20
25b.14 MAS-20
14a.02 MBR CHAR 3-1
17f.08 BLOCK SET 2ND ORDER MAR
101.20 A1(D 0.4) USE
26a.128 SMAC-10
28.02 CHK SMAC(DG)
25b.15 MAS-10
GJ
DG
TBW
2K
SMAC 80
MAR-80
MAR-40
SMAC 40
MAR-20
SMAC 20
MAR-10
SMAC 10
17b.01-49d
17b.02-30b
17b.03-29a
17b.04-28
17b.05-30b
17b.06-31b
17b.07-32b
17b.08-33b
17b.09-30b
17b.10-29a
17b.11-28
17b.12-30b
17b.13-31b
17b.14-32b
17b.15-33b
17b.16-49d
17b.17-30b
17b.18-29c
17b.19-28
17b.20-30b
17b.21-31b
17b.22-32b
17b.23-33b
17b.24-49d
17b.25-30b
17b.26-29a
17b.27-28
17b.28-30b
17b.29-31b
17b.30-32b
17b.31-33b
17b.32-49d
MAR RESET(W) 139c.19
-12 CLAMP 139d.37

FIG.17c

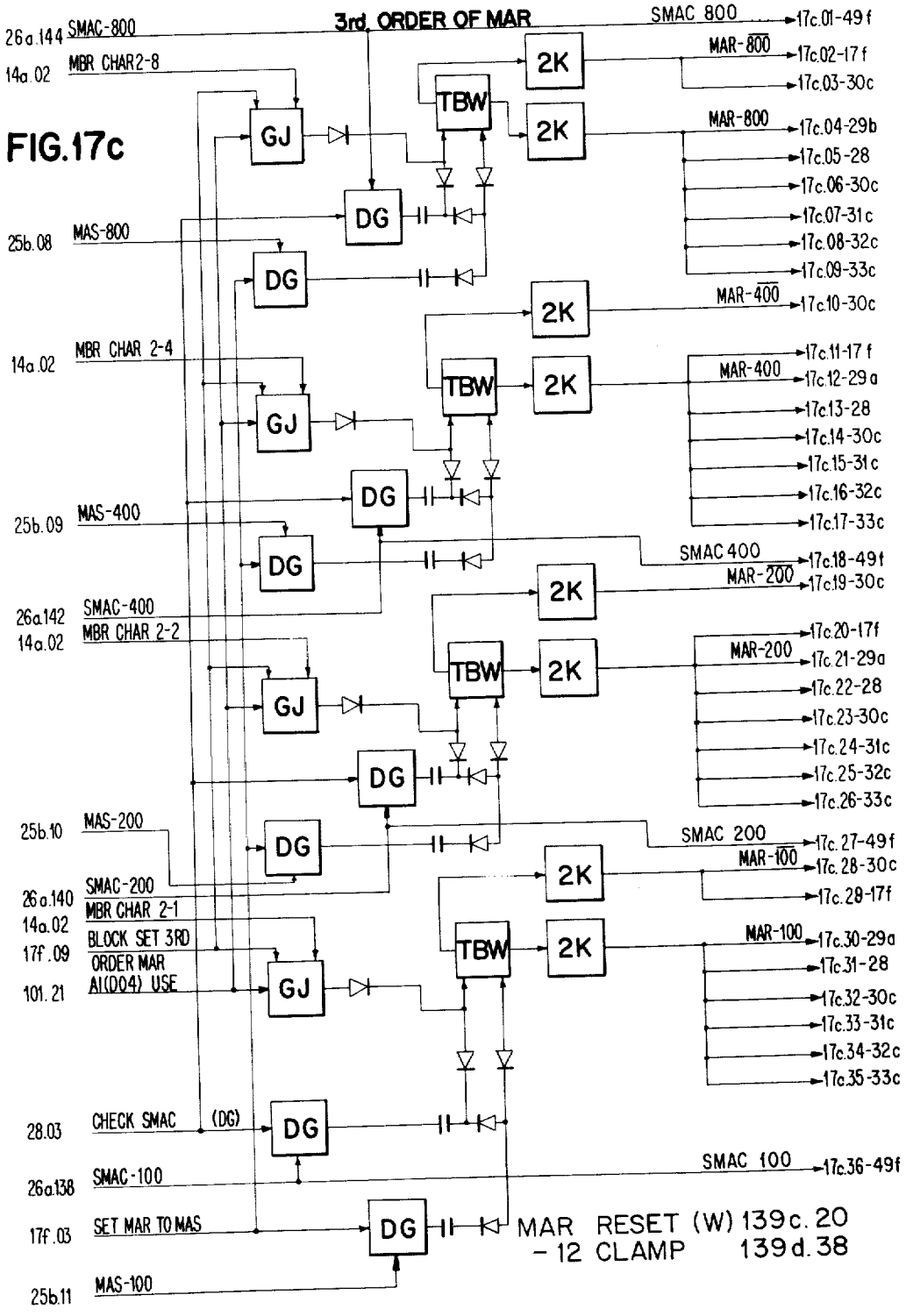

3rd ORDER OF MAR
26a.144 SMAC-800
14a.02 MBR CHAR2-8
25b.08 MAS-800
14a.02 MBR CHAR 2-4
25b.09 MAS-400
26a.142 SMAC-400
14a.02 MBR CHAR 2-2
25b.10 MAS-200
26a.140 SMAC-200
14a.02 MBR CHAR 2-1
17f.09 BLOCK SET 3RD ORDER MAR
101.21 AI(D04) USE
28.03 CHECK SMAC (DG)
26a.138 SMAC-100
17f.03 SET MAR TO MAS
25b.11 MAS-100
GJ
DG
TBW
2K
SMAC 800
MAR-800
MAR-800
MAR-400
MAR-400
SMAC 400
MAR-200
MAR-200
SMAC 200
MAR-100
MAR-100
SMAC 100
17c.01-49f
17c.02-17f
17c.03-30c
17c.04-29b
17c.05-28
17c.06-30c
17c.07-31c
17c.08-32c
17c.09-33c
17c.10-30c
17c.11-17f
17c.12-29a
17c.13-28
17c.14-30c
17c.15-31c
17c.16-32c
17c.17-33c
17c.18-49f
17c.19-30c
17c.20-17f
17c.21-29a
17c.22-28
17c.23-30c
17c.24-31c
17c.25-32c
17c.26-33c
17c.27-49f
17c.28-30c
17c.28-17f
17c.30-29a
17c.31-28
17c.32-30c
17c.33-31c
17c.34-32c
17c.35-33c
17c.36-49f
MAR RESET (W) 139c.20
-12 CLAMP 139d.38

FIG.17d

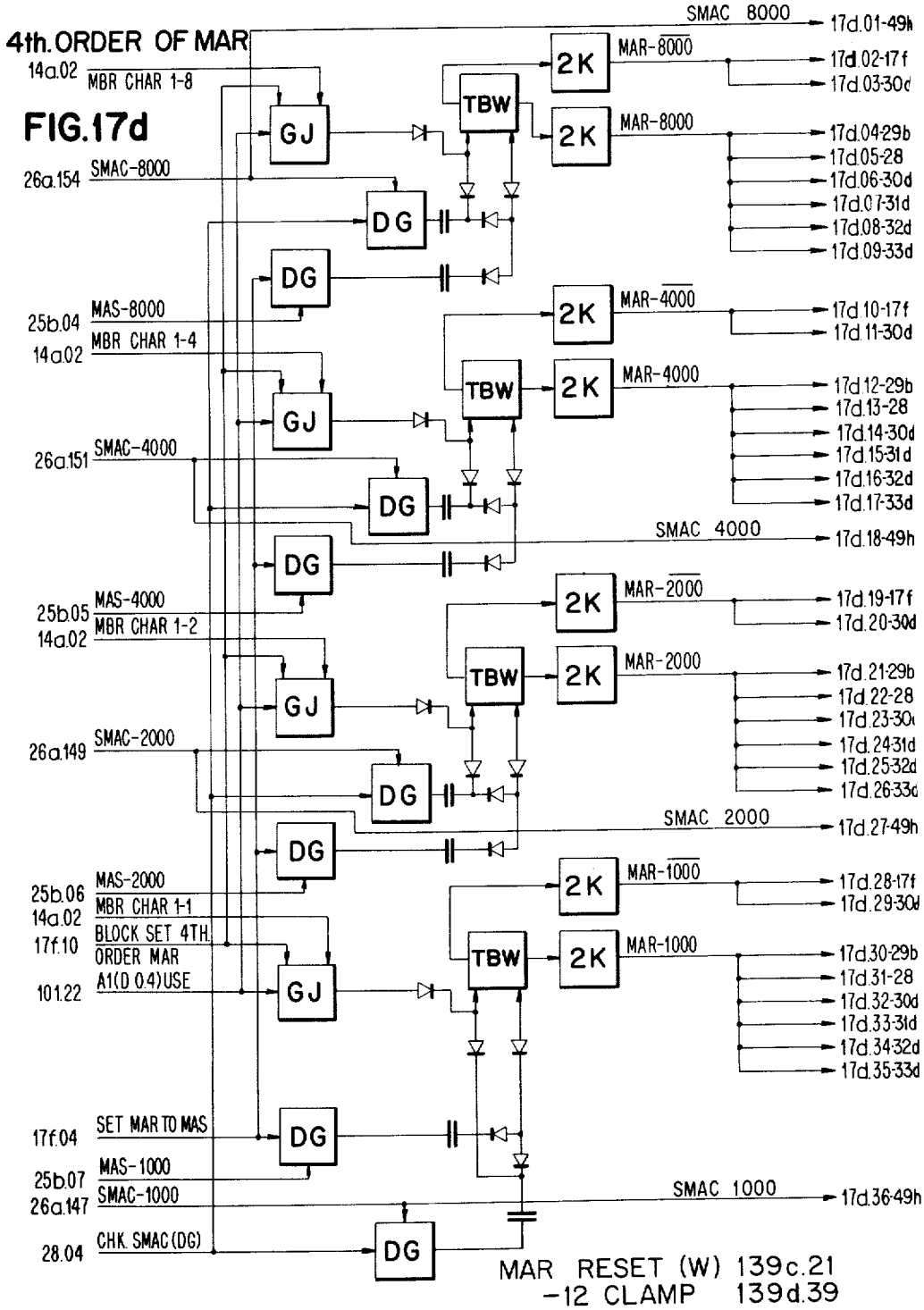

4th. ORDER OF MAR
14a.02 MBR CHAR 1-8
26a.154 SMAC-8000
25b.04 MAS-8000
14a.02 MBR CHAR 1-4
26a.151 SMAC-4000
25b.05 MAS-4000
14a.02 MBR CHAR 1-2
26a.149 SMAC-2000
25b.06 MAS-2000
14a.02 MBR CHAR 1-1
17f.10 BLOCK SET 4TH ORDER MAR
101.22 A1(D 0-4) USE
17f.04 SET MAR TO MAS
25b.07 MAS-1000
26a.147 SMAC-1000
28.04 CHK. SMAC (DG)
GJ
DG
TBW
2K
SMAC 8000
SMAC 4000
SMAC 2000
SMAC 1000
MAR-8000
MAR-4000
MAR-2000
MAR-1000
17d.01-49h
17d.02-17f
17d.03-30d
17d.04-29b
17d.05-28
17d.06-30d
17d.07-31d
17d.08-32d
17d.09-33d
17d.10-17f
17d.11-30d
17d.12-29b
17d.13-28
17d.14-30d
17d.15-31d
17d.16-32d
17d.17-33d
17d.18-49h
17d.19-17f
17d.20-30d
17d.21-29b
17d.22-28
17d.23-30d
17d.24-31d
17d.25-32d
17d.26-33d
17d.27-49h
17d.28-17f
17d.29-30d
17d.30-29b
17d.31-28
17d.32-30d
17d.33-31d
17d.34-32d
17d.35-33d
17d.36-49h
MAR RESET (W) 139c.21
-12 CLAMP 139d.39

FIG.17e

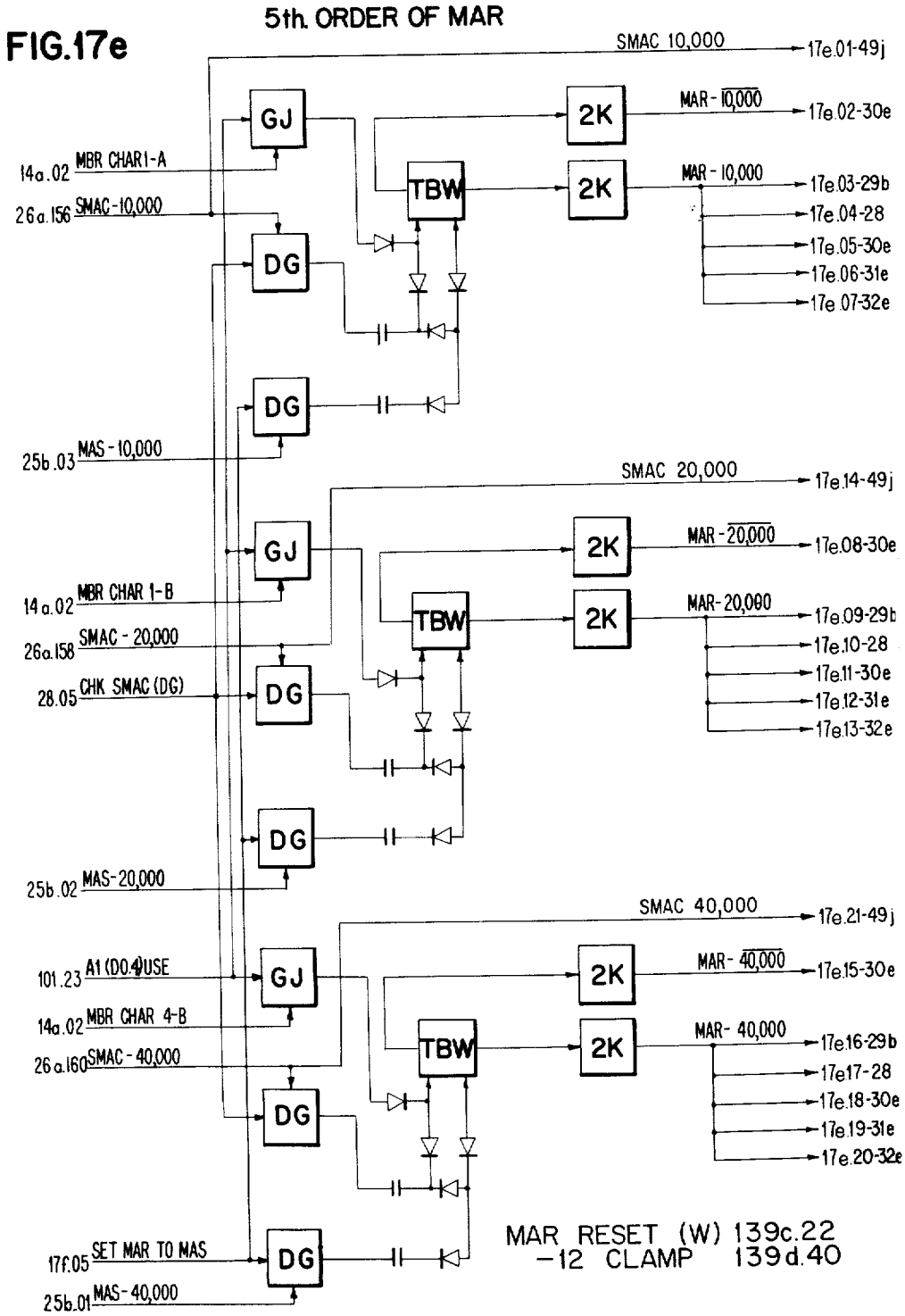

5th. ORDER OF MAR
SMAC 10,000
17e.01-49j
GJ
2K
MAR - 10,000
17e.02-30e
14a.02 MBR CHAR1-A
TBW
2K
MAR - 10,000
17e.03-29b
26a.156 SMAC-10,000
17e.04-28
17e.05-30e
17e.06-31e
17e.07-32e
DG
DG
25b.03 MAS - 10,000
SMAC 20,000
17e.14-49j
GJ
2K
MAR - 20,000
17e.08-30e
14a.02 MBR CHAR 1-B
TBW
2K
MAR-20,000
17e.09-29b
26a.158 SMAC - 20,000
17e.10-28
28.05 CHK SMAC (DG)
17e.11-30e
17e.12-31e
17e.13-32e
DG
DG
25b.02 MAS-20,000
SMAC 40,000
17e.21-49j
101.23 A1 (D0.4) USE
GJ
2K
MAR - 40,000
17e.15-30e
14a.02 MBR CHAR 4-B
TBW
2K
MAR- 40,000
17e.16-29b
26a.160 SMAC - 40,000
17e17-28
17e.18-30e
17e.19-31e
17e.20-32e
DG
17f.05 SET MAR TO MAS
DG
25b.01 MAS - 40,000
MAR RESET (W) 139c.22
-12 CLAMP 139d.40

FIG.17f

MEMORY ADDRESS REGISTER CONTROLS

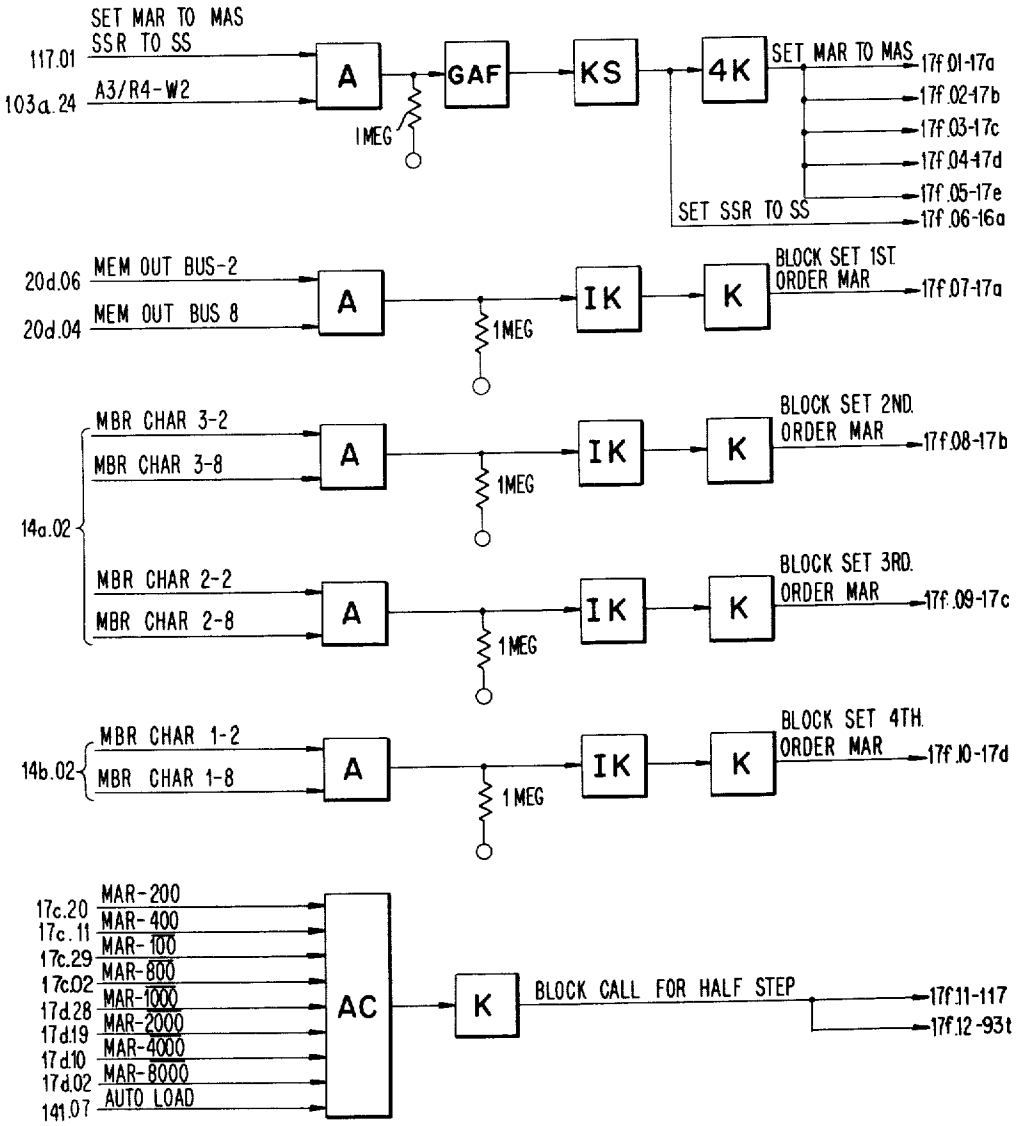


FIG. 18a

P.C.T. WRITE BUSSES CHAR. 4,3 & 2

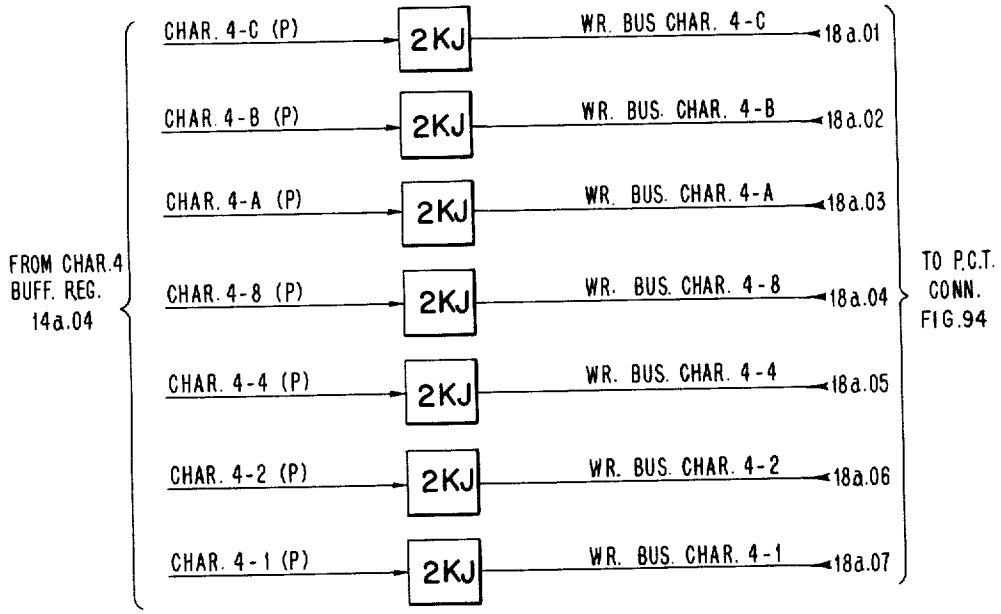
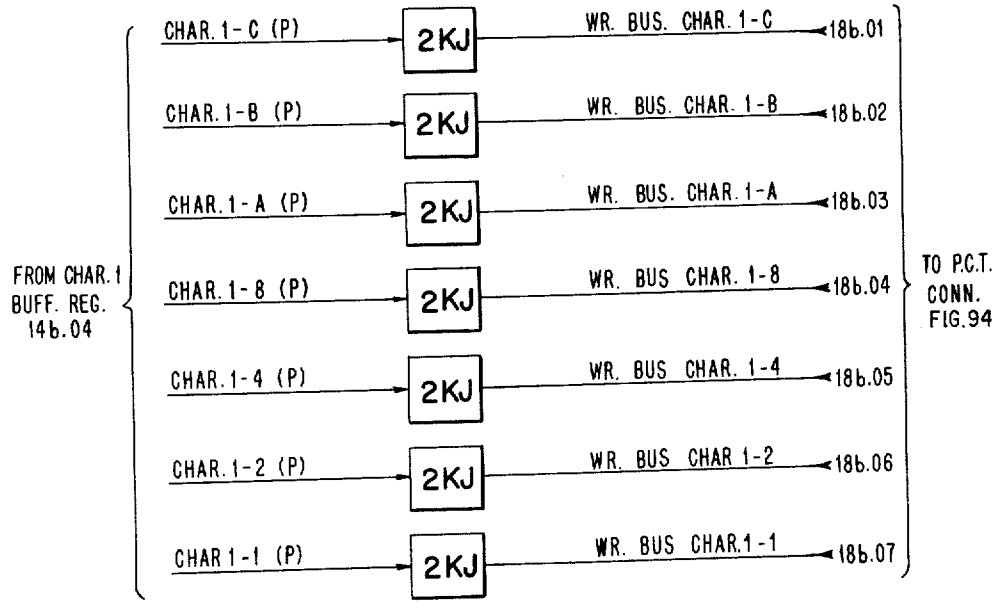


FIG. 18b

P.C.T. WRITE BUSSES CHAR. 1 & 0



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FIG.19a

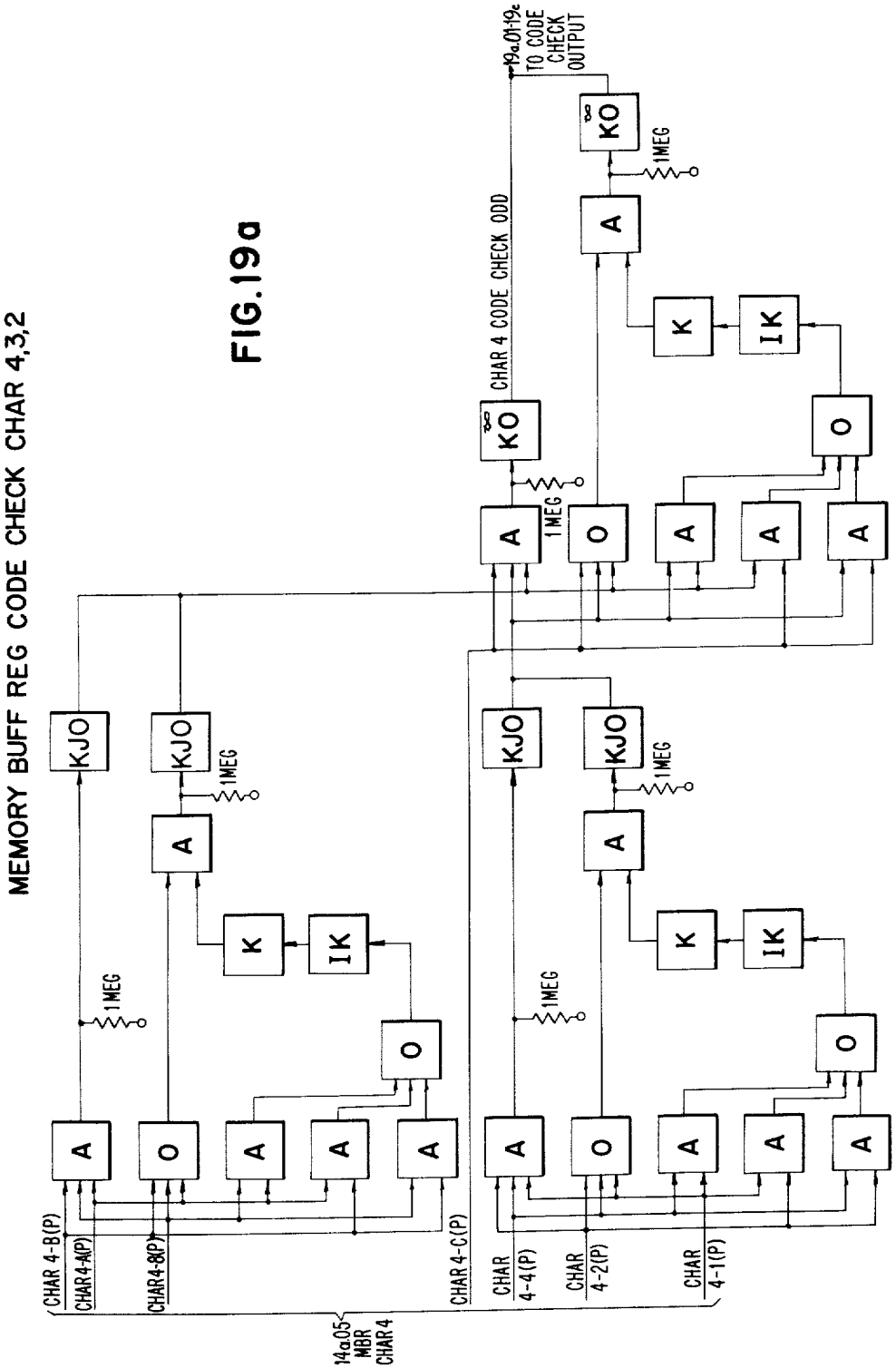


FIG.19b

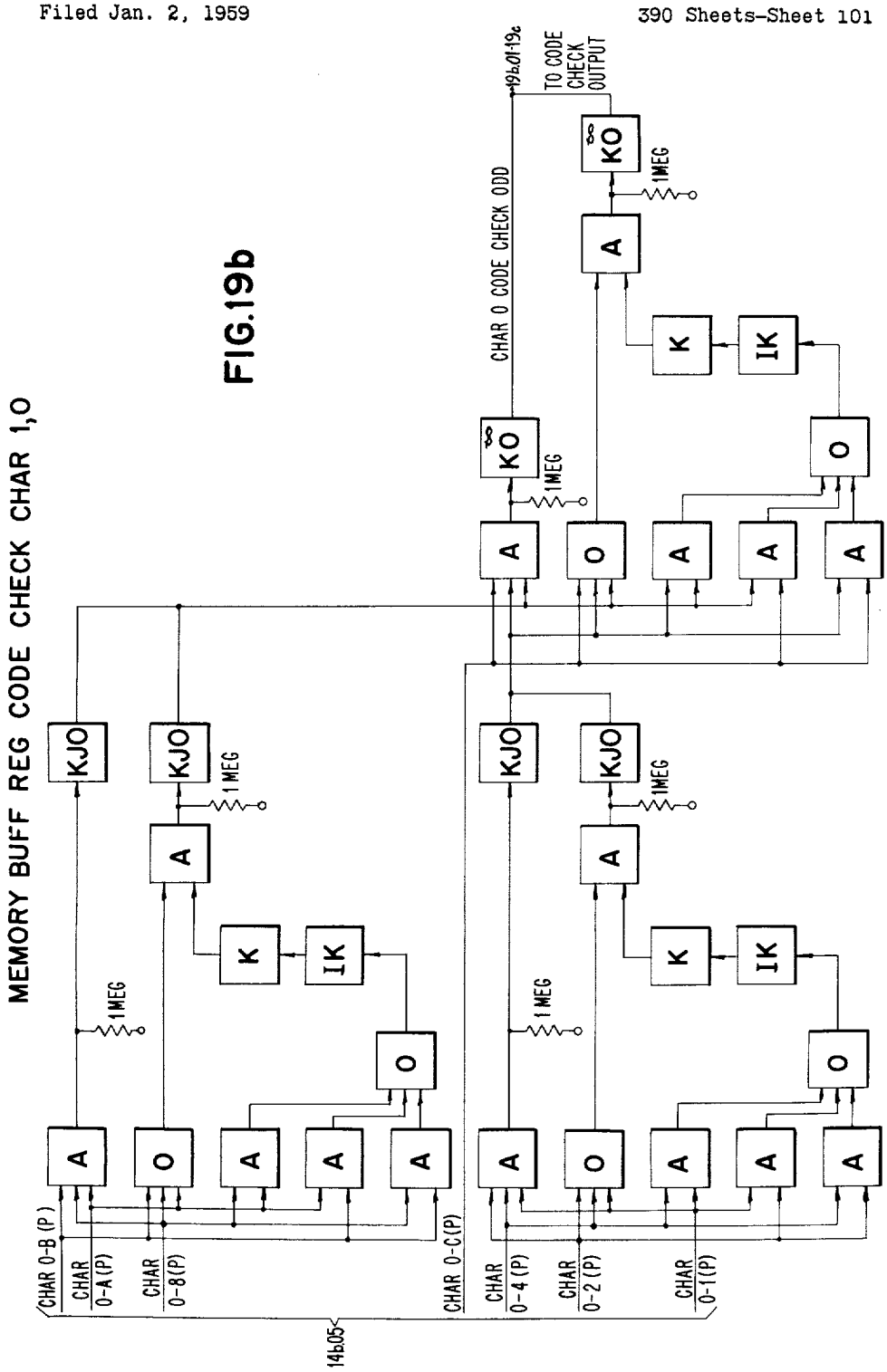

MEMORY BUFF REG CODE CHECK CHAR 1,0
CHAR 0 CODE CHECK ODD
TO CODE CHECK OUTPUT
19b01-19c
KO
KJO
K
IK
A
O
1MEG
CHAR 0-B (P)
CHAR 0-A (P)
CHAR 0-8 (P)
CHAR 0-C (P)
CHAR 0-4 (P)
CHAR 0-2 (P)
CHAR 0-1 (P)
14b05

FIG. 19c

MEMORY BUFF. REG. CODE CHECK OUTPUT

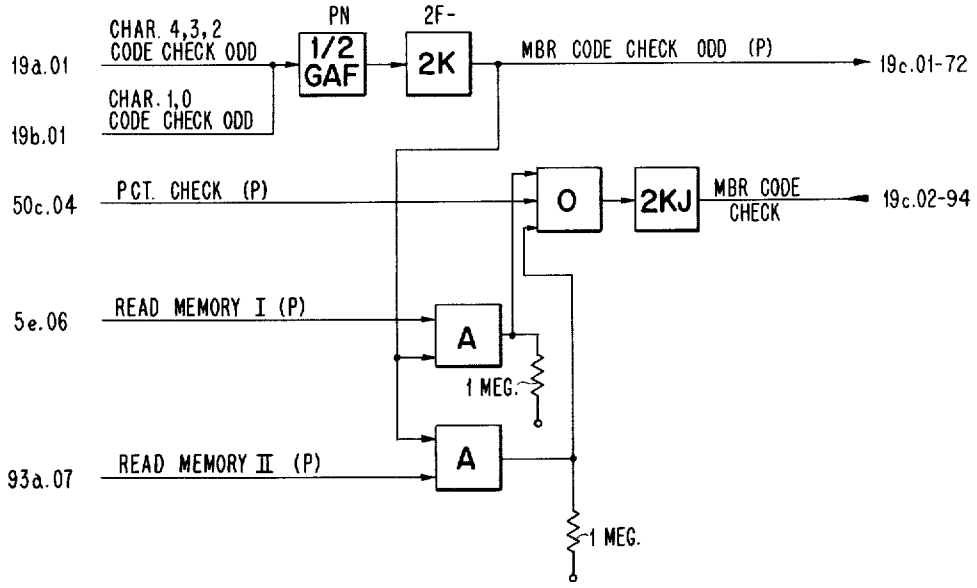


FIG. 142b DRIVER BIAS VOLTAGE REGULATOR

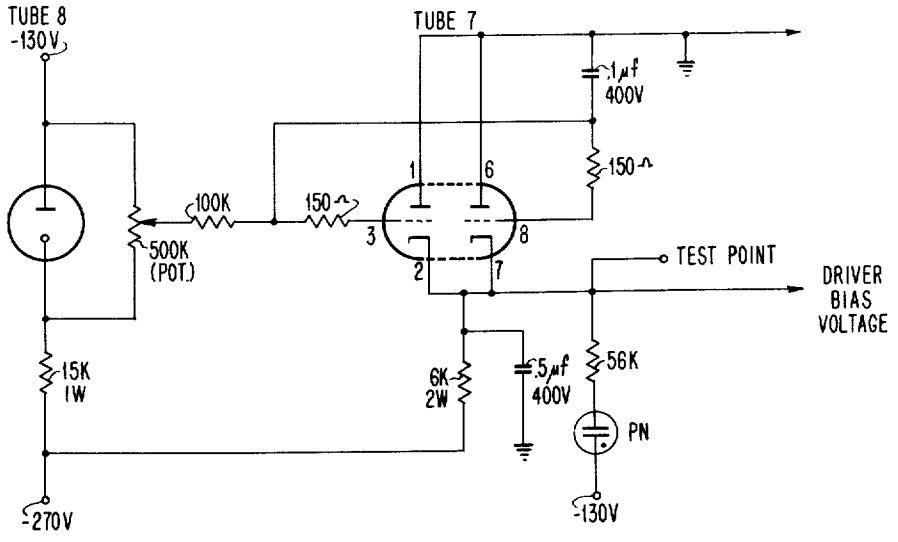
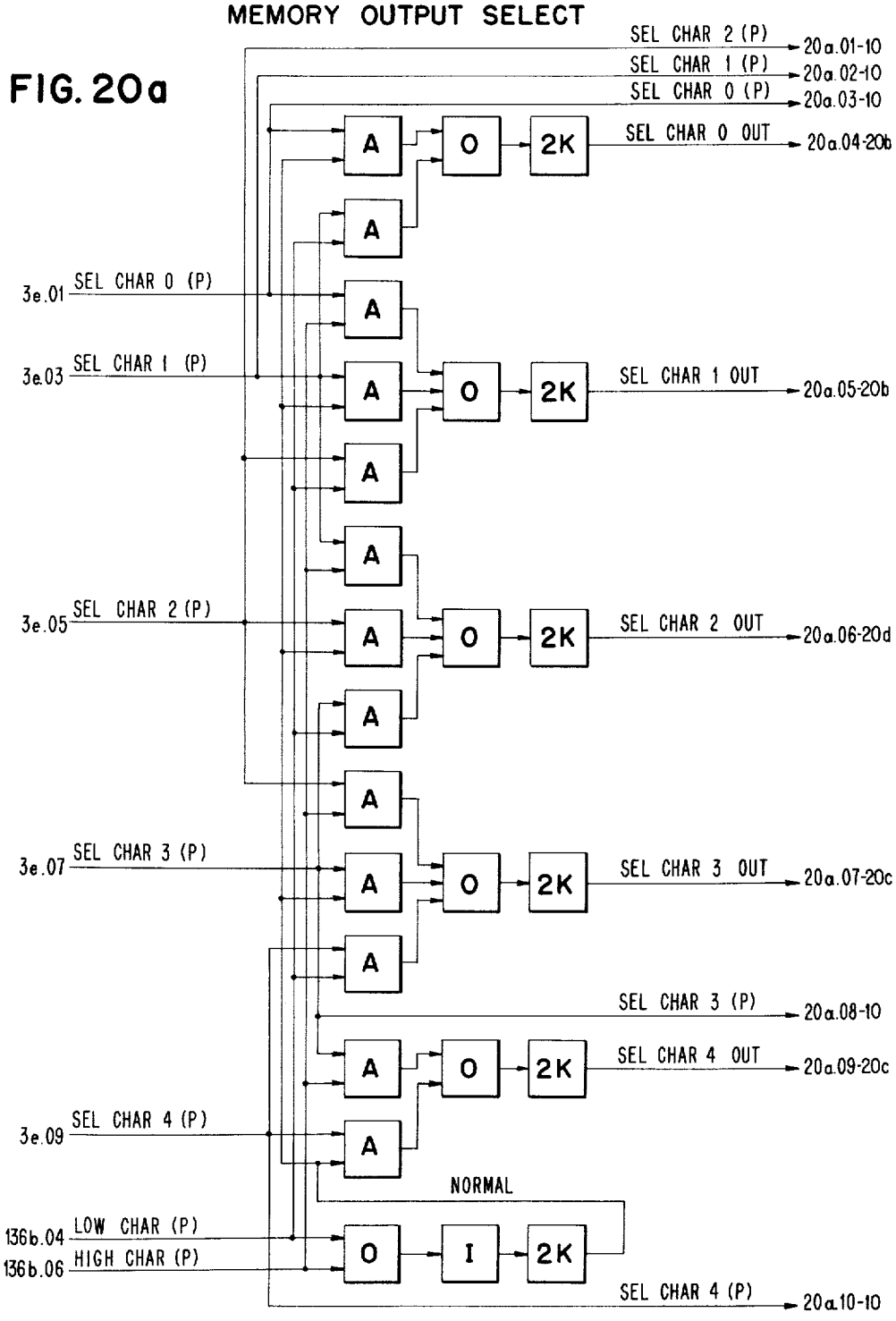


FIG. 20a


MEMORY OUTPUT SELECT
SEL CHAR 2 (P)
20a.01-10
SEL CHAR 1 (P)
20a.02-10
SEL CHAR 0 (P)
20a.03-10
A
O
2K
SEL CHAR 0 OUT
20a.04-20b
3e.01 SEL CHAR 0 (P)
3e.03 SEL CHAR 1 (P)
SEL CHAR 1 OUT
20a.05-20b
3e.05 SEL CHAR 2 (P)
SEL CHAR 2 OUT
20a.06-20d
3e.07 SEL CHAR 3 (P)
SEL CHAR 3 OUT
20a.07-20c
SEL CHAR 3 (P)
20a.08-10
SEL CHAR 4 OUT
20a.09-20c
3e.09 SEL CHAR 4 (P)
NORMAL
136b.04 LOW CHAR (P)
136b.06 HIGH CHAR (P)
I
SEL CHAR 4 (P)
20a.10-10

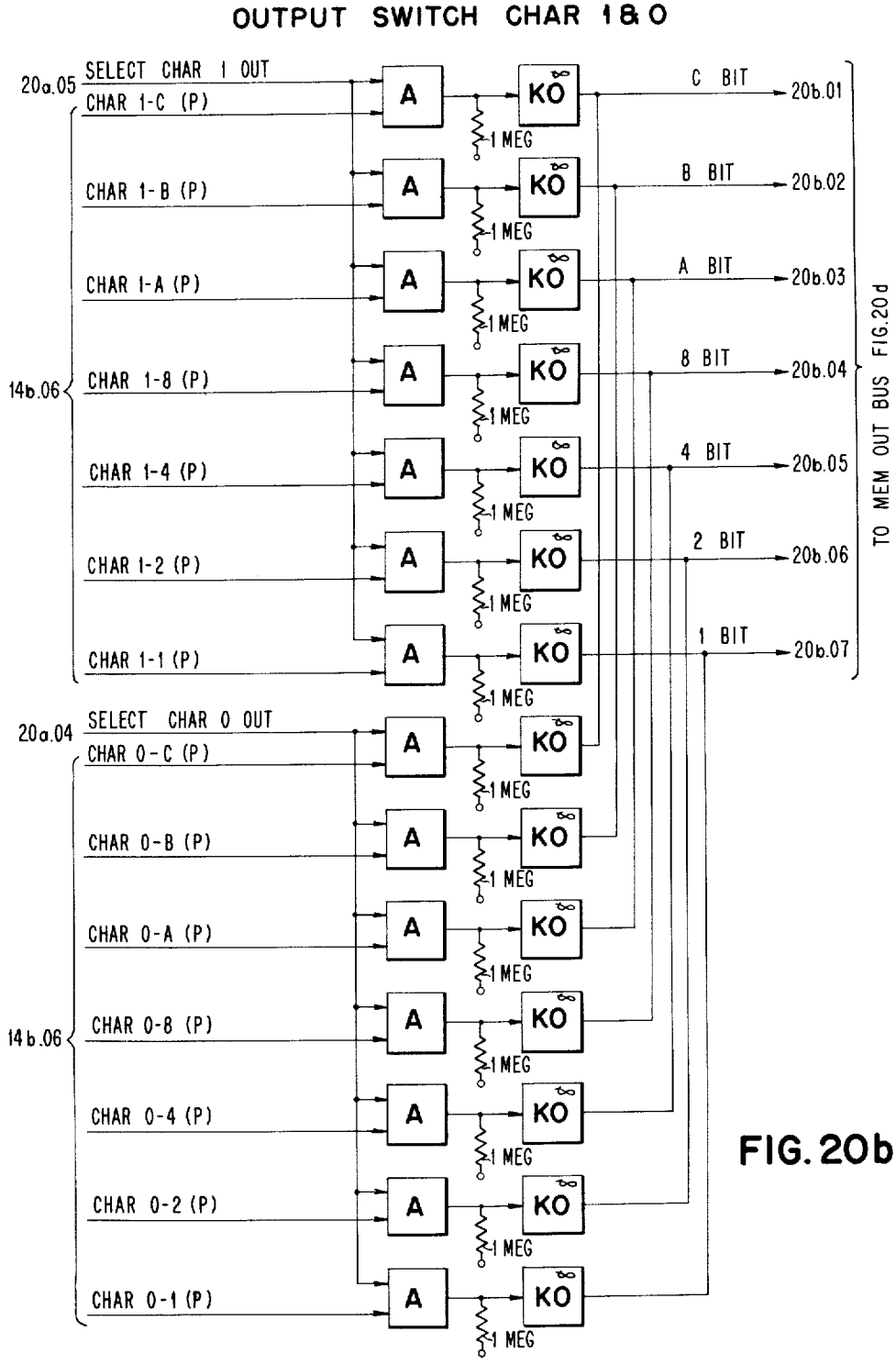

OUTPUT SWITCH CHAR 1 & 0
20a.05
SELECT CHAR 1 OUT
CHAR 1-C (P)
CHAR 1-B (P)
CHAR 1-A (P)
14b.06
CHAR 1-8 (P)
CHAR 1-4 (P)
CHAR 1-2 (P)
CHAR 1-1 (P)
20a.04
SELECT CHAR 0 OUT
CHAR 0-C (P)
CHAR 0-B (P)
CHAR 0-A (P)
14b.06
CHAR 0-8 (P)
CHAR 0-4 (P)
CHAR 0-2 (P)
CHAR 0-1 (P)
A
KO
1 MEG
C BIT
B BIT
A BIT
8 BIT
4 BIT
2 BIT
1 BIT
20b.01
20b.02
20b.03
20b.04
20b.05
20b.06
20b.07
TO MEM OUT BUS FIG.20d

FIG. 20b

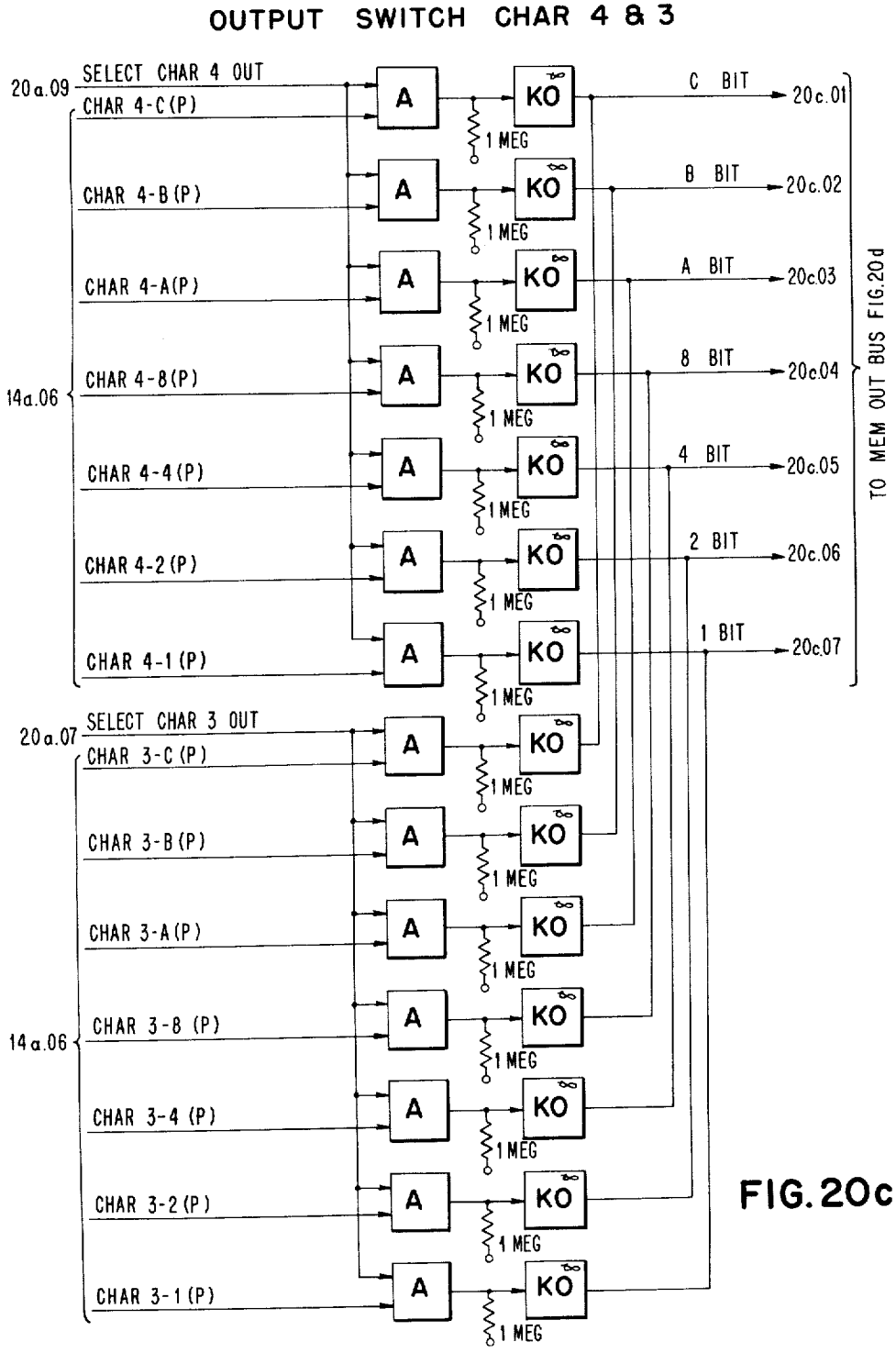

OUTPUT SWITCH CHAR 4 & 3
20a.09
SELECT CHAR 4 OUT
CHAR 4-C (P)
CHAR 4-B (P)
CHAR 4-A (P)
CHAR 4-8 (P)
CHAR 4-4 (P)
CHAR 4-2 (P)
CHAR 4-1 (P)
14a.06
20a.07
SELECT CHAR 3 OUT
CHAR 3-C (P)
CHAR 3-B (P)
CHAR 3-A (P)
CHAR 3-8 (P)
CHAR 3-4 (P)
CHAR 3-2 (P)
CHAR 3-1 (P)
14a.06
A
KO
1 MEG
C BIT
B BIT
A BIT
8 BIT
4 BIT
2 BIT
1 BIT
20c.01
20c.02
20c.03
20c.04
20c.05
20c.06
20c.07
TO MEM OUT BUS FIG.20d

FIG. 20c

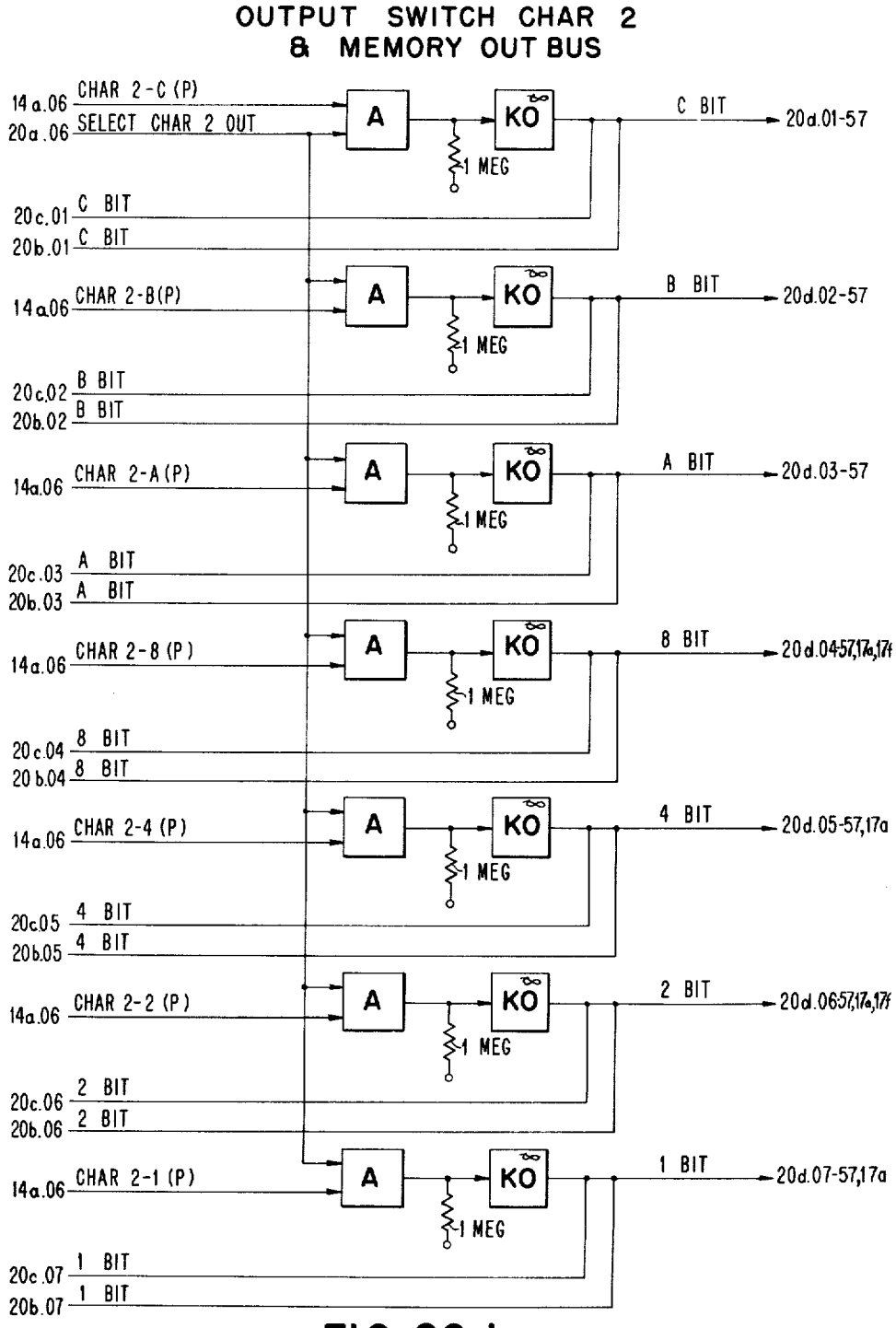

OUTPUT SWITCH CHAR 2
& MEMORY OUT BUS
14a.06 CHAR 2-C (P)
20a.06 SELECT CHAR 2 OUT
A
KO
1 MEG
C BIT
20d.01-57
20c.01 C BIT
20b.01 C BIT
14a.06 CHAR 2-B(P)
B BIT
20d.02-57
20c.02 B BIT
20b.02 B BIT
14a.06 CHAR 2-A(P)
A BIT
20d.03-57
20c.03 A BIT
20b.03 A BIT
14a.06 CHAR 2-8 (P)
8 BIT
20d.04-57,17a,17f
20c.04 8 BIT
20b.04 8 BIT
14a.06 CHAR 2-4 (P)
4 BIT
20d.05-57,17a
20c.05 4 BIT
20b.05 4 BIT
14a.06 CHAR 2-2 (P)
2 BIT
20d.06-57,17a,17f
20c.06 2 BIT
20b.06 2 BIT
14a.06 CHAR 2-1 (P)
1 BIT
20d.07-57,17a
20c.07 1 BIT
20b.07 1 BIT

FIG. 20d

FIG. 20e

MEMORY SAMPLE PULSE GENERATOR & P.C.T. SAMPLE PULSE GEN. &
M.B.R SAMPLE PULSE GENERATOR

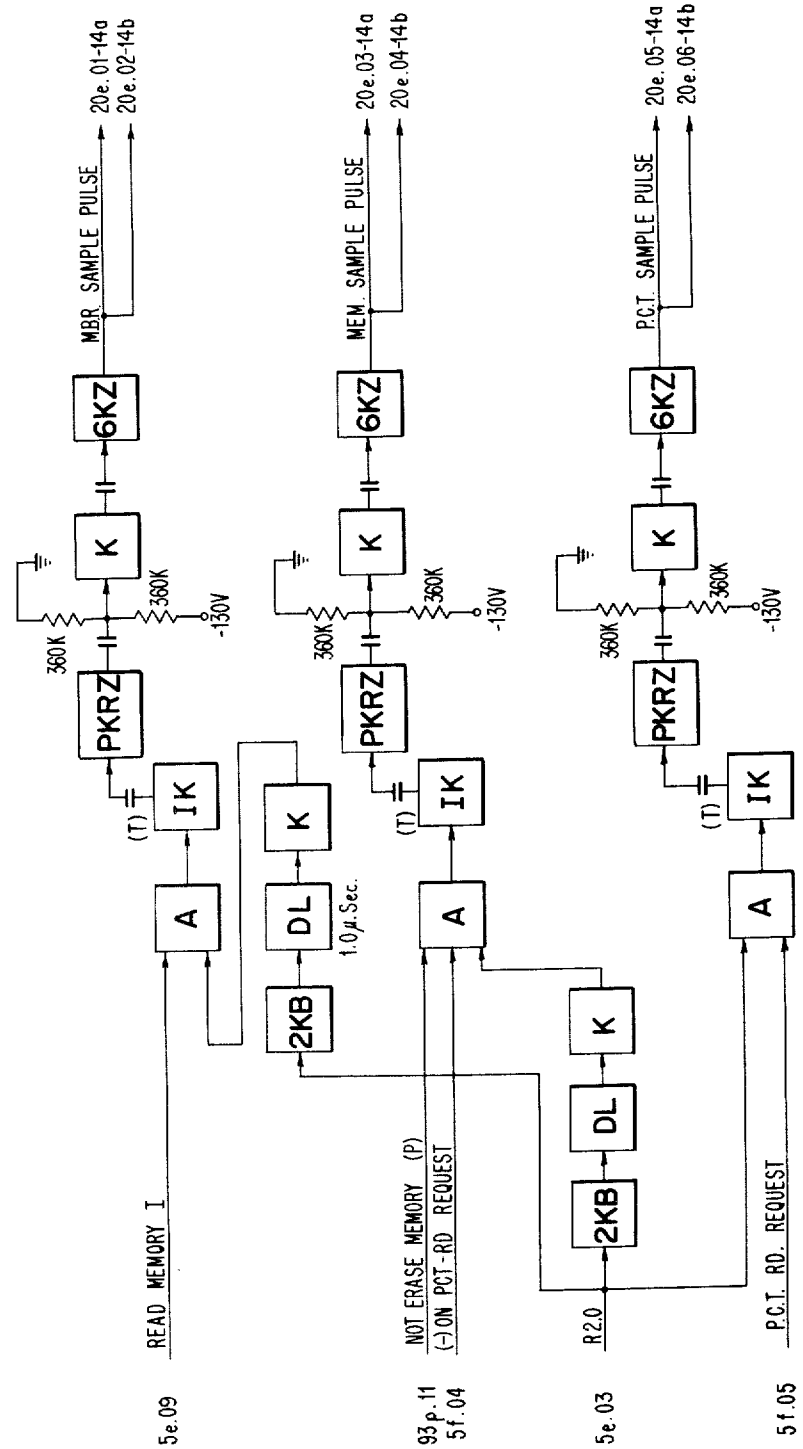


FIG. 21a

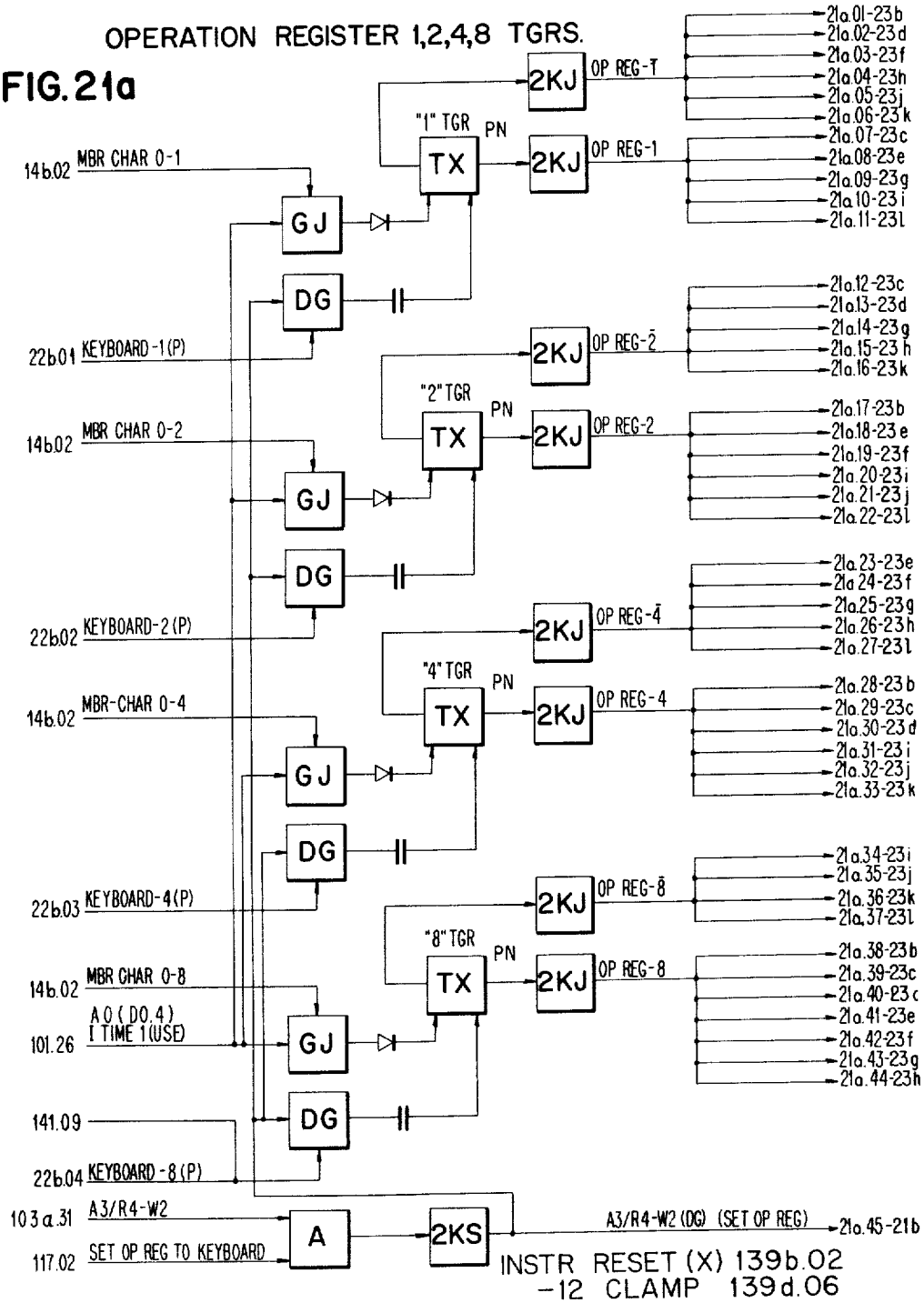
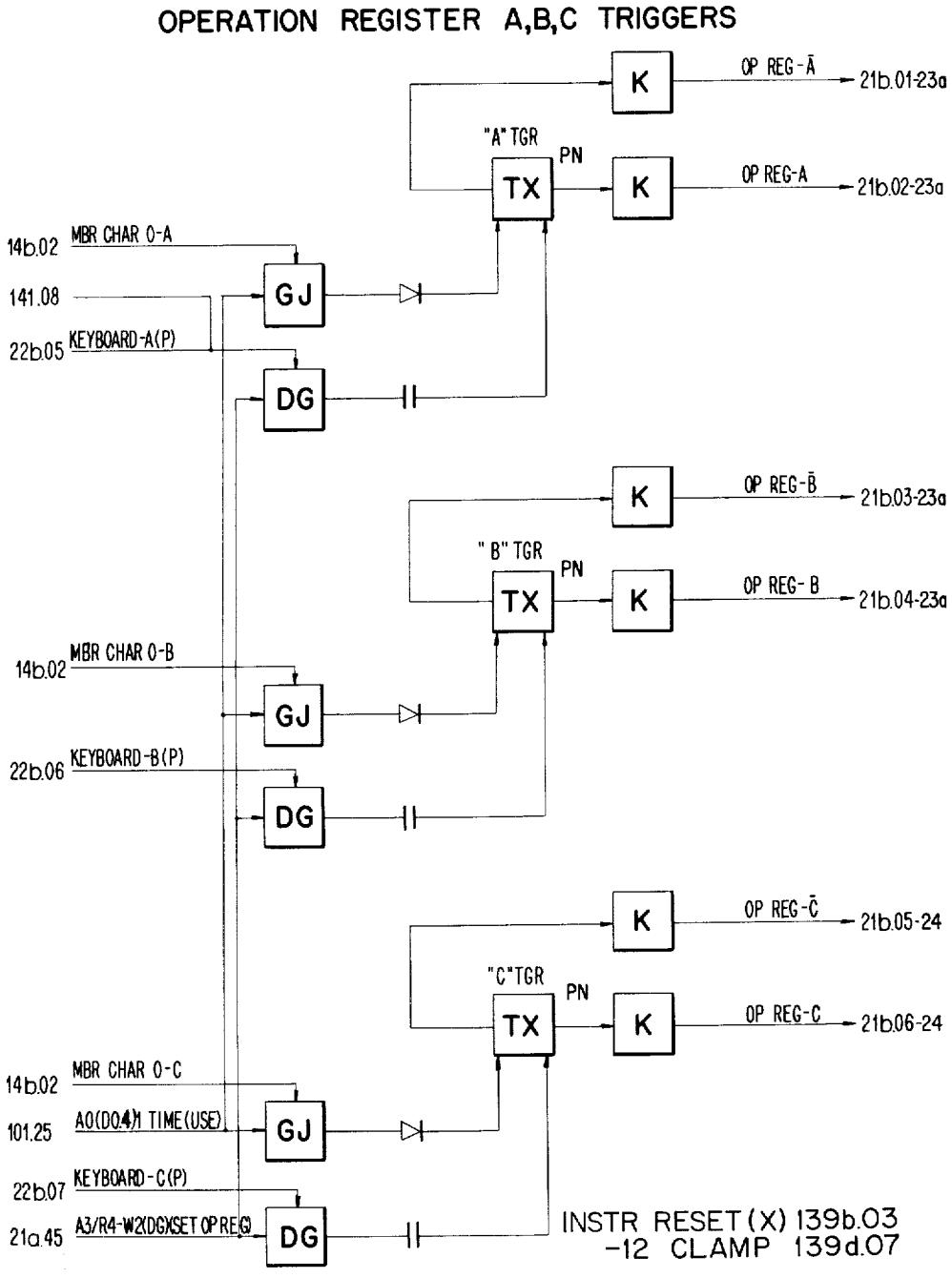

OPERATION REGISTER 1,2,4,8 TGRS.
14b.02 MBR CHAR 0-1
22b.01 KEYBOARD-1(P)
14b.02 MBR CHAR 0-2
22b.02 KEYBOARD-2(P)
14b.02 MBR-CHAR 0-4
22b.03 KEYBOARD-4(P)
14b.02 MBR CHAR 0-8
101.26 A 0 (D0.4) I TIME 1(USE)
141.09
22b.04 KEYBOARD-8(P)
103a.31 A3/R4-W2
117.02 SET OP REG TO KEYBOARD
"1" TGR
"2" TGR
"4" TGR
"8" TGR
PN
TX
GJ
DG
A
2KJ
2KS
OP REG-1
OP REG-2
OP REG-4
OP REG-8
A3/R4-W2 (DG) (SET OP REG)
INSTR RESET (X) 139b.02
-12 CLAMP 139d.06

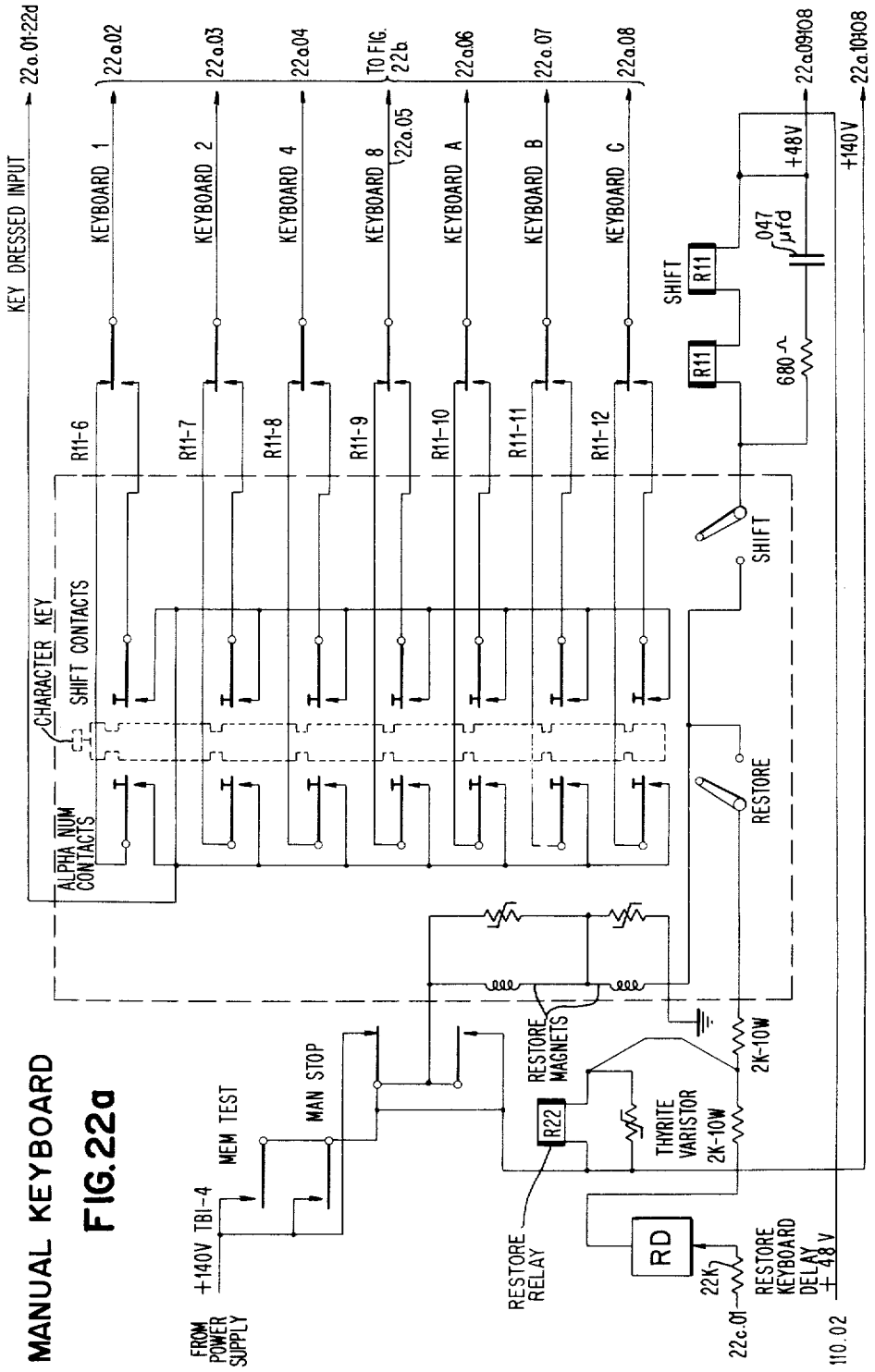
FIG.21b


OPERATION REGISTER A,B,C TRIGGERS
K
OP REG-Ā
21b.01-23a
"A" TGR
PN
TX
K
OP REG-A
21b.02-23a
14b.02 MBR CHAR 0-A
141.08
GJ
22b.05 KEYBOARD-A(P)
DG
K
OP REG-B̄
21b.03-23a
" B" TGR
PN
TX
K
OP REG-B
21b.04-23a
14b.02 MBR CHAR 0-B
GJ
22b.06 KEYBOARD-B(P)
DG
K
OP REG-C̄
21b.05-24
"C"TGR
PN
TX
K
OP REG-C
21b.06-24
14b.02 MBR CHAR 0-C
101.25 A0(D04)M TIME(USE)
GJ
22b.07 KEYBOARD-C(P)
21a.45 A3/R4-W2(DGXSET OP REG)
DG
INSTR RESET(X) 139b.03
-12 CLAMP 139d.07

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OVERLAP MODE CONTROL

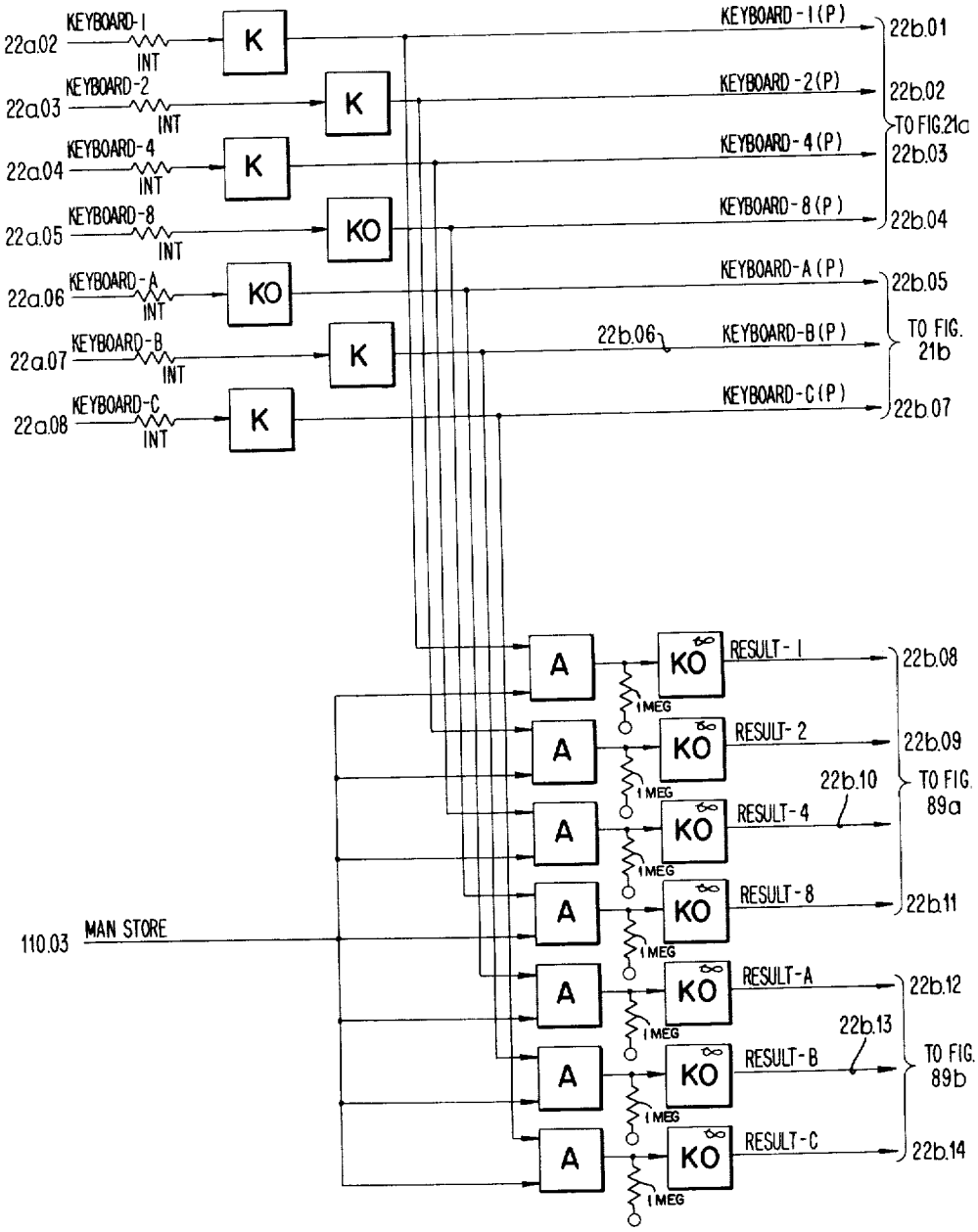
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MANUAL KEYBOARD

FIG. 22a

FIG.22b KEYBOARD OUTPUTS



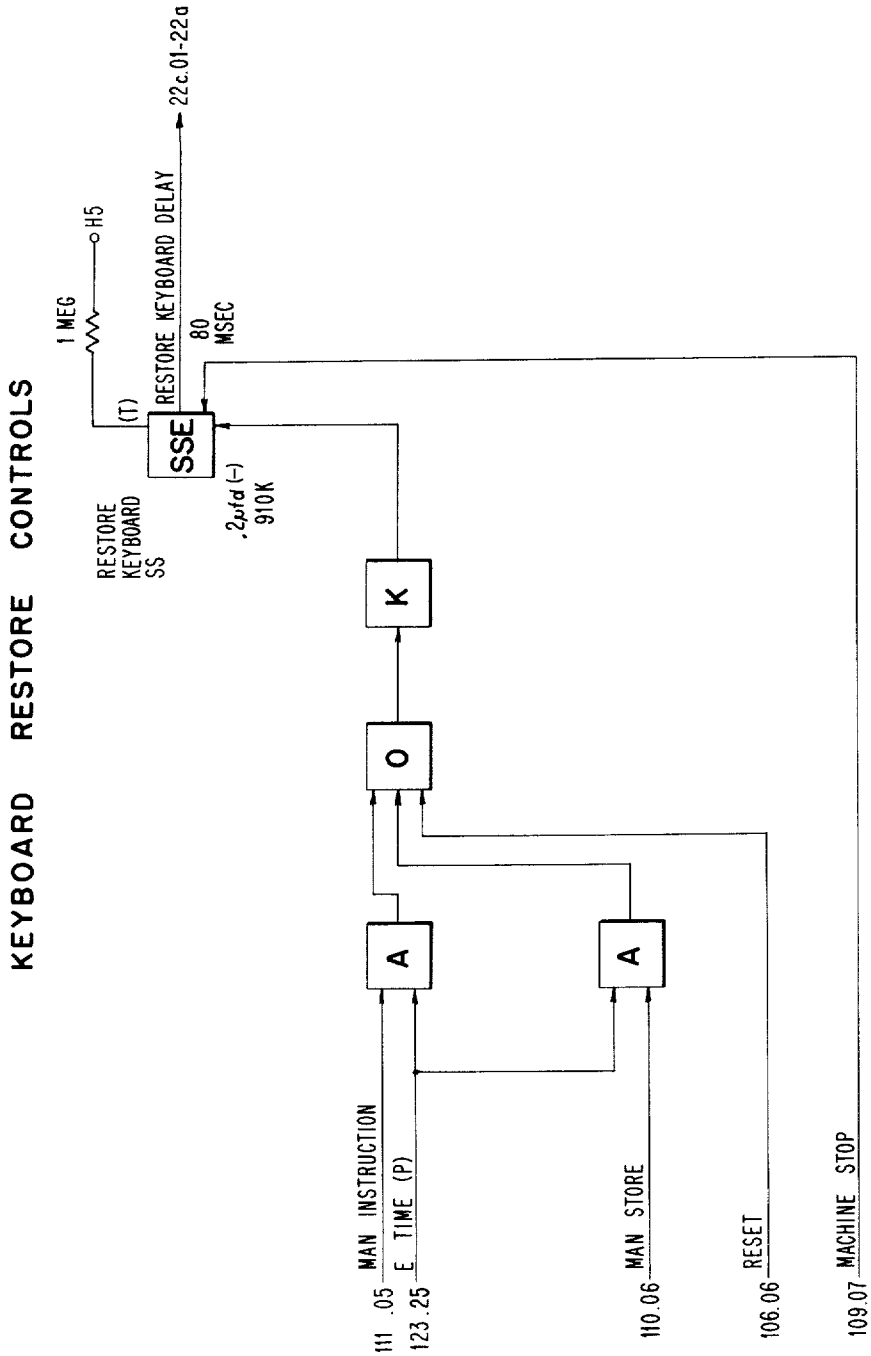

KEYBOARD RESTORE CONTROLS
RESTORE KEYBOARD SS
1 MEG
H5
(T)
SSE
.2μfd (-)
910K
RESTORE KEYBOARD DELAY
80 MSEC
22c.01-22a
K
O
A
A
MAN INSTRUCTION
E TIME (P)
MAN STORE
RESET
MACHINE STOP
111 .05
123.25
110.06
106.06
109.07
-12 CLAMP 139e.08

FIG. 22c

FIG. 22d

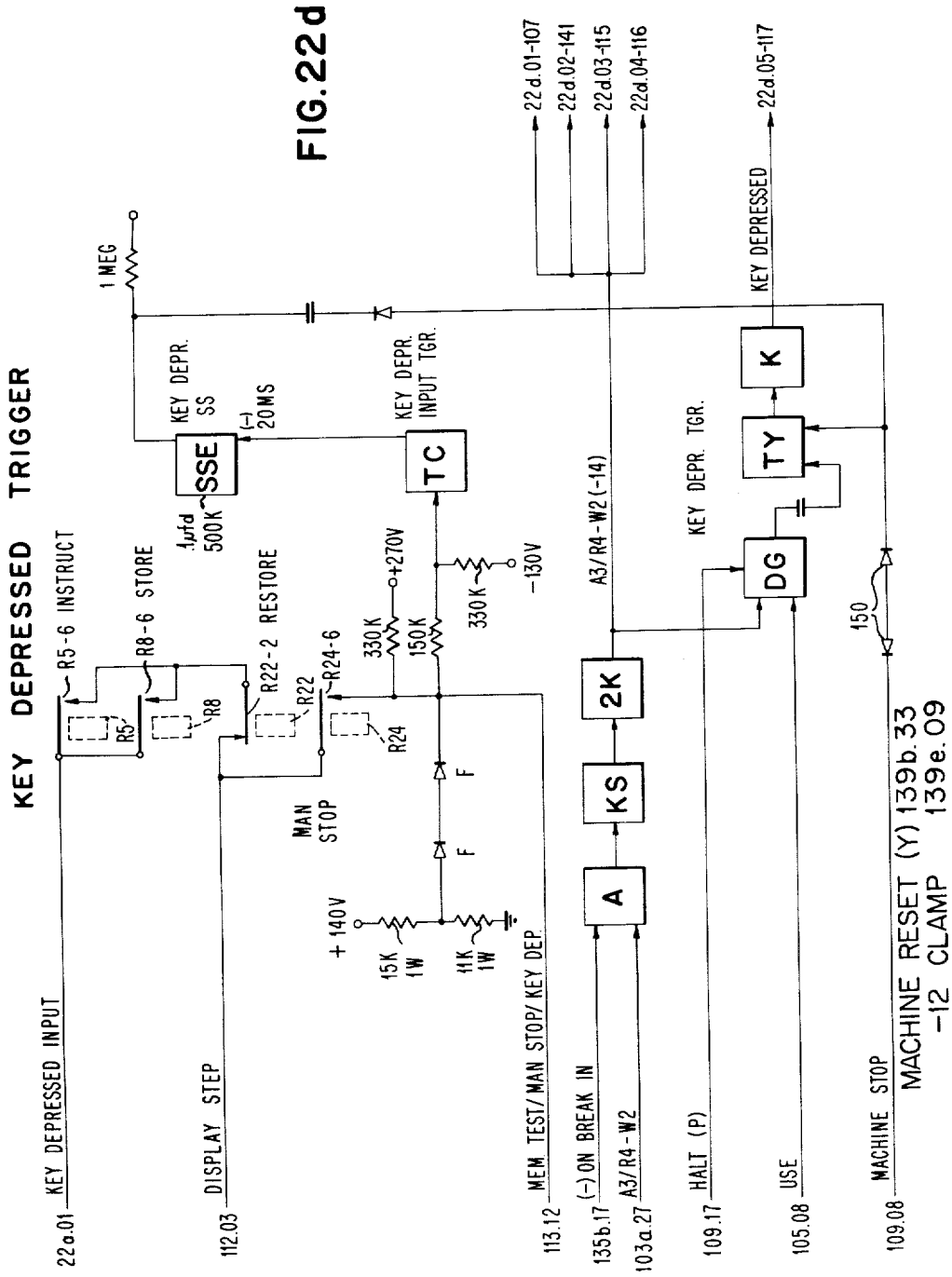

KEY DEPRESSED TRIGGER
22a.01 KEY DEPRESSED INPUT
R5-6 INSTRUCT
R8-6 STORE
R22-2 RESTORE
R5
R8
R22
R24-6
R24
112.03 DISPLAY STEP
MAN STOP
+140V
15K 1W
11K 1W
F
F
330K
150K
+270V
330K
-130V
1MEG
.1μfd 500K
KEY DEPR. SS
(-) 20MS
SSE
KEY DEPR. INPUT TGR.
TC
113.12 MEM TEST/MAN STOP/KEY DEP
135b.17 (-) ON BREAK IN
103a.27 A3/R4-W2
A
KS
2K
A3/R4-W2(-14)
22d.01-107
22d.02-141
22d.03-115
22d.04-116
KEY DEPR. TGR.
DG
TY
K
KEY DEPRESSED
22d.05-117
150
109.17 HALT (P)
105.08 USE
109.08 MACHINE STOP
MACHINE RESET (Y) 139b.33
-12 CLAMP 139e.09

FIG.23a

OPERATION ZONE DECODER

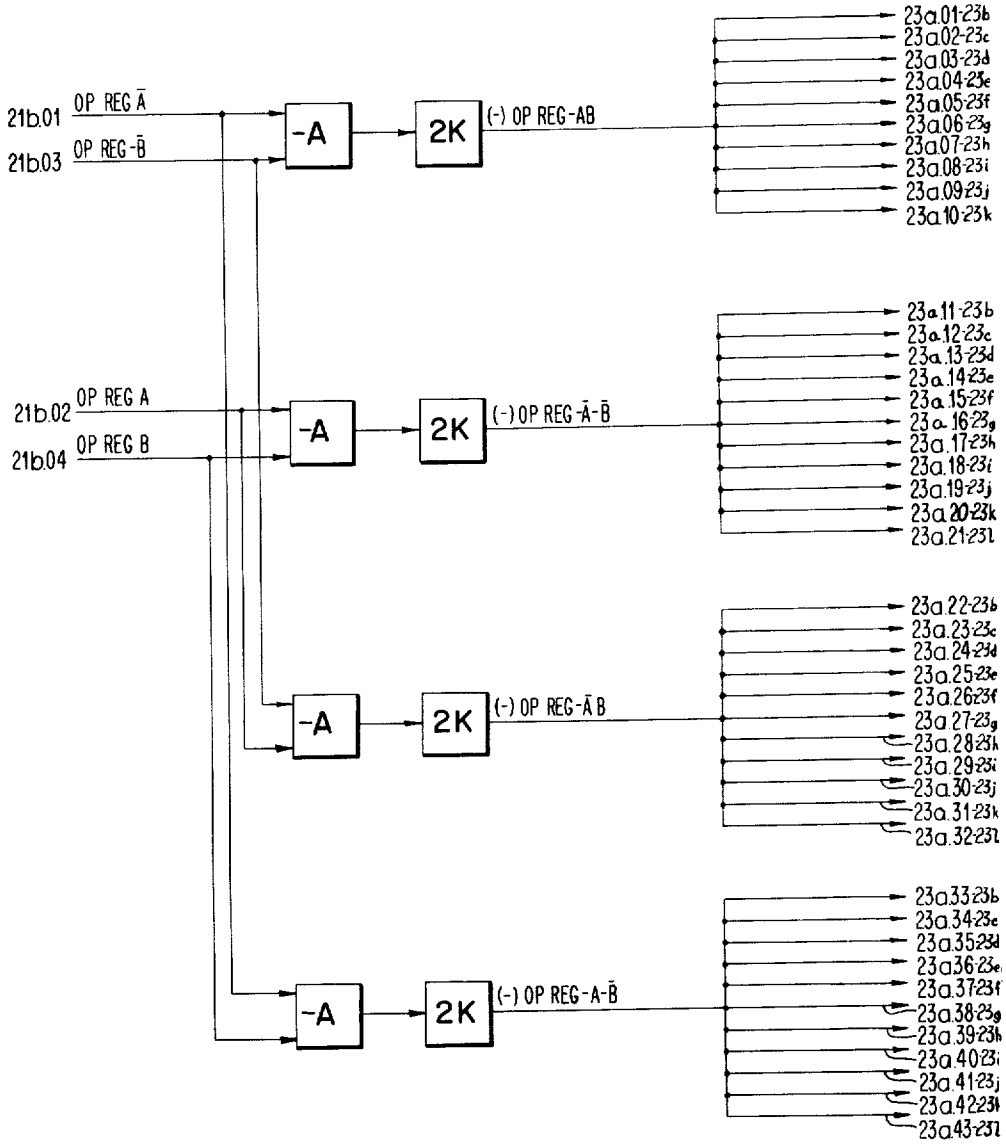


FIG.23b

OPERATION DECODER NO OP, STOP, TR, SEND

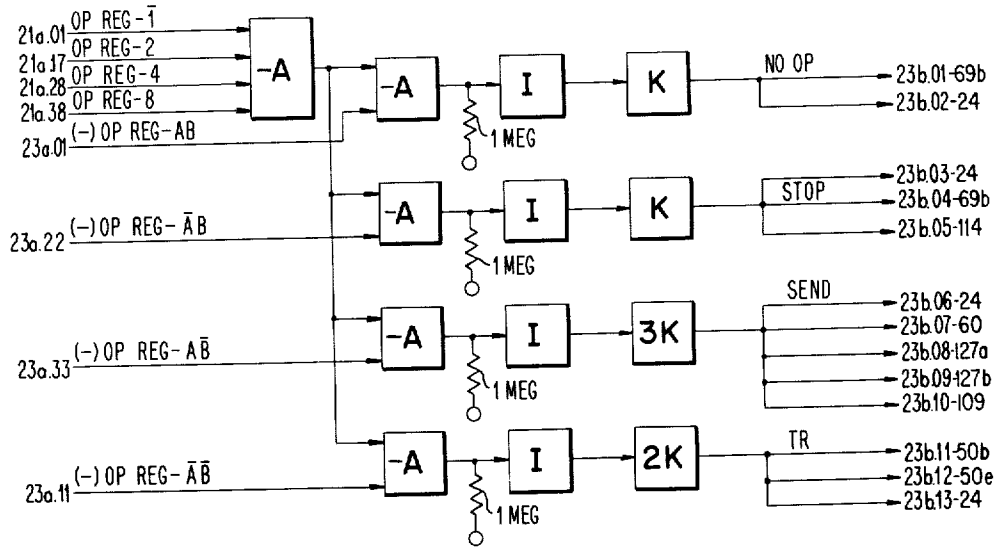


FIG.23c

OPERATION DECODER SET L, TR HI, RWW SEL

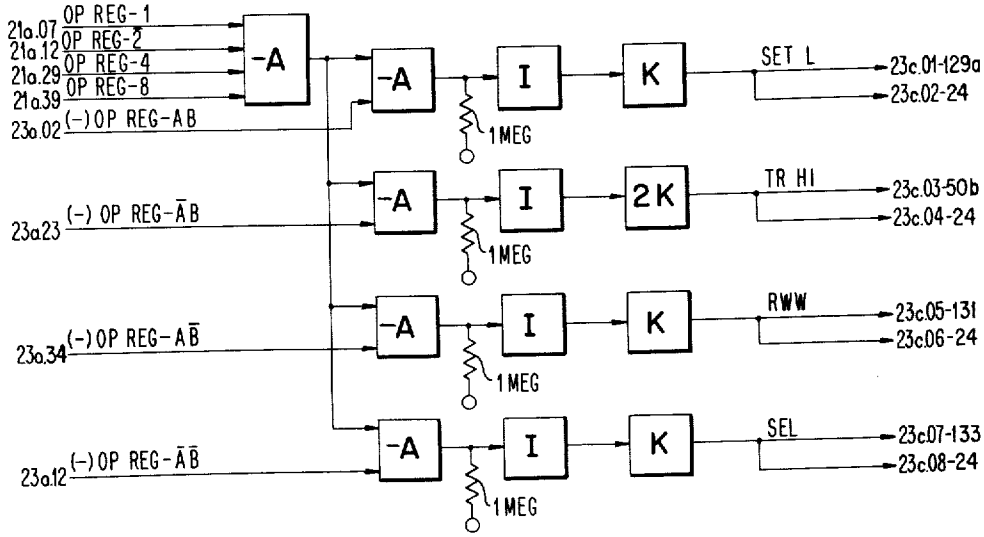


FIG.23d

OPERATION DECODER SHOR, TR EQ, SIGN CTRL.

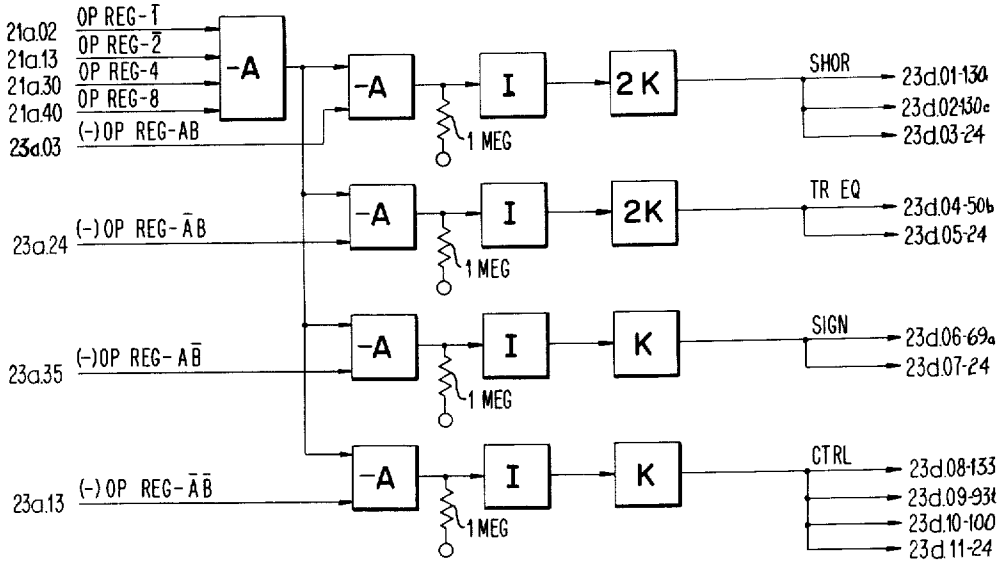


FIG.23l

OPERATION DECODER ULA, AAM, SB

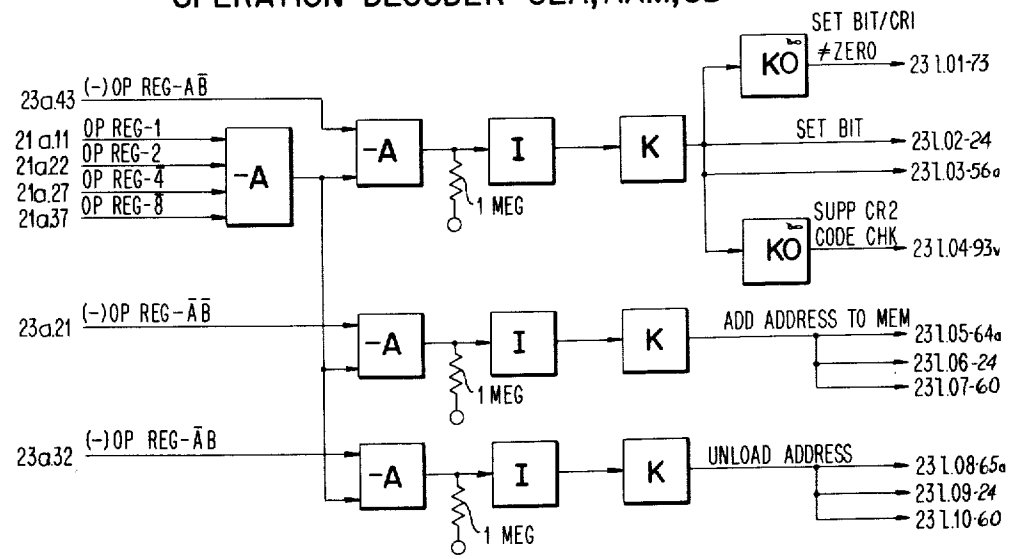


FIG.23e OPERATION DECODER LENG, TR PLS, RCV, COMP

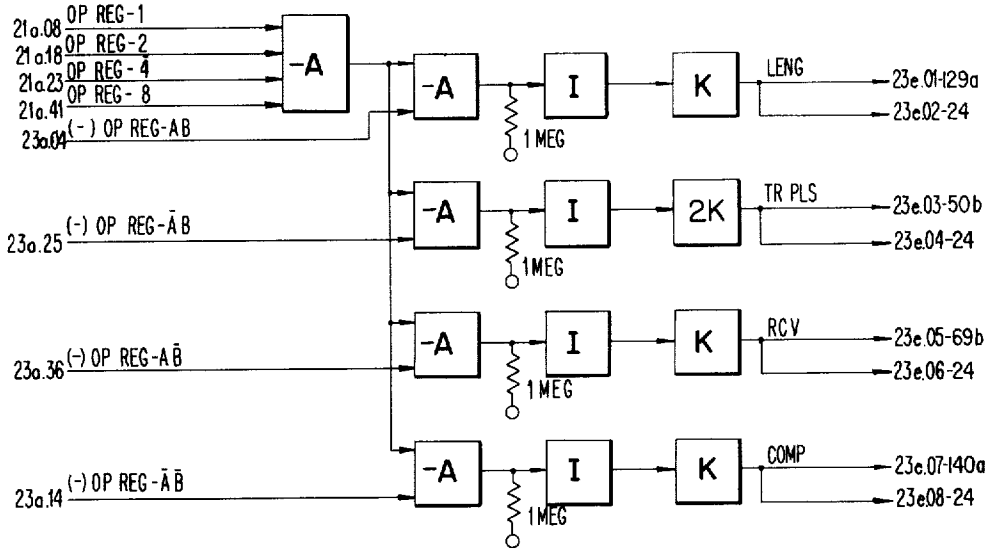
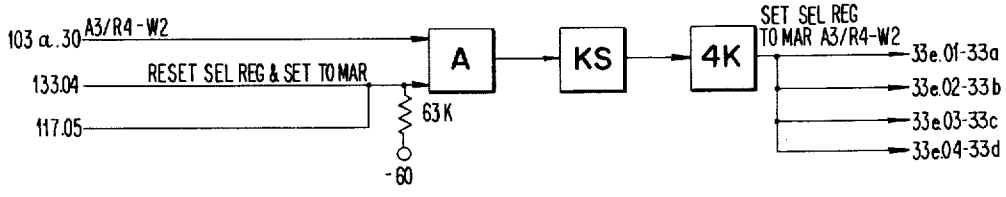


FIG.33e SELECT REGISTER CONTROLS



OPERATION DECODER-ROUND, TR ZRO, MPY, ST PR

FIG. 23f

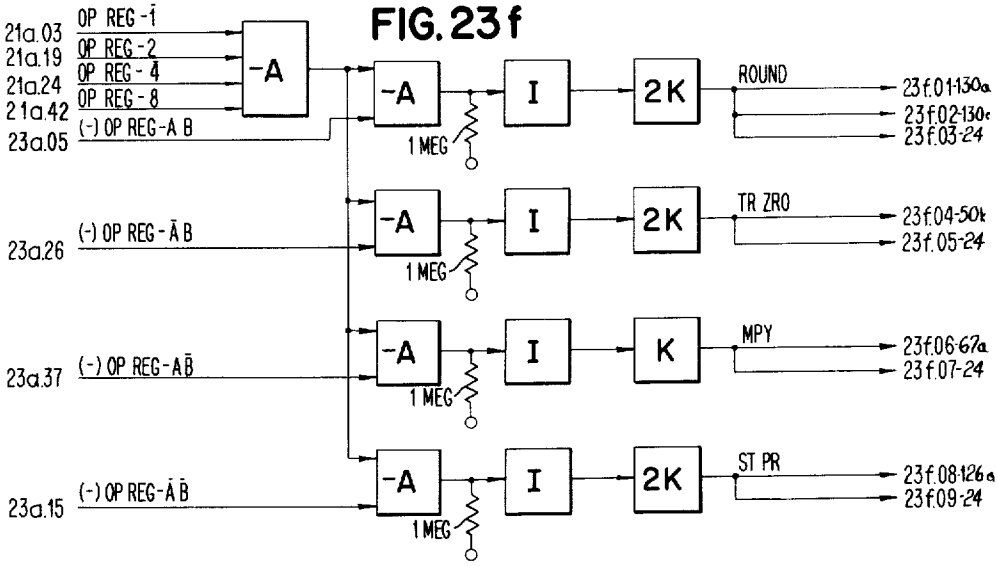


FIG. 23g

OPERATION DECODER STORE, TR SIG, DIV, ADD MEM

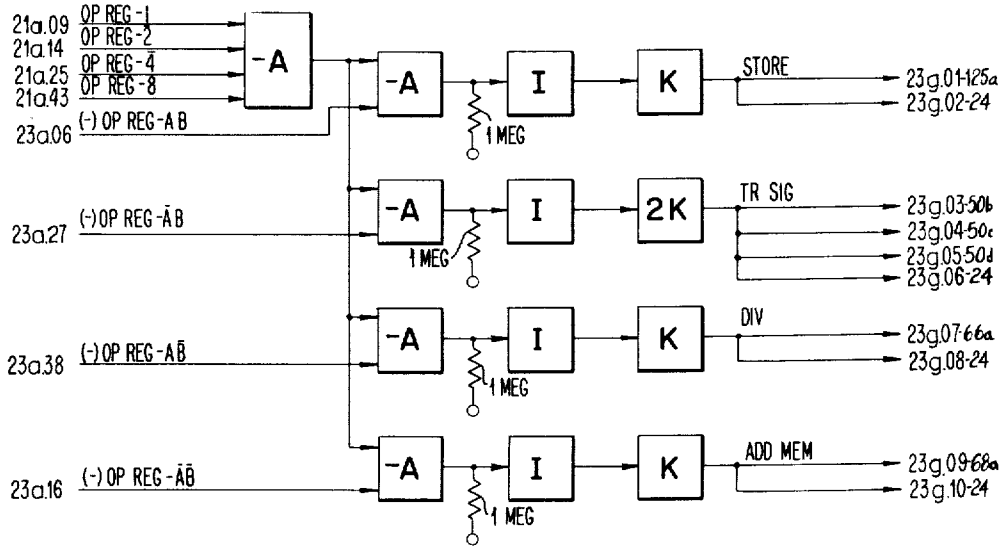


FIG.23h

OPERATION DECODER ADD, SUB, NORM TR, LOAD

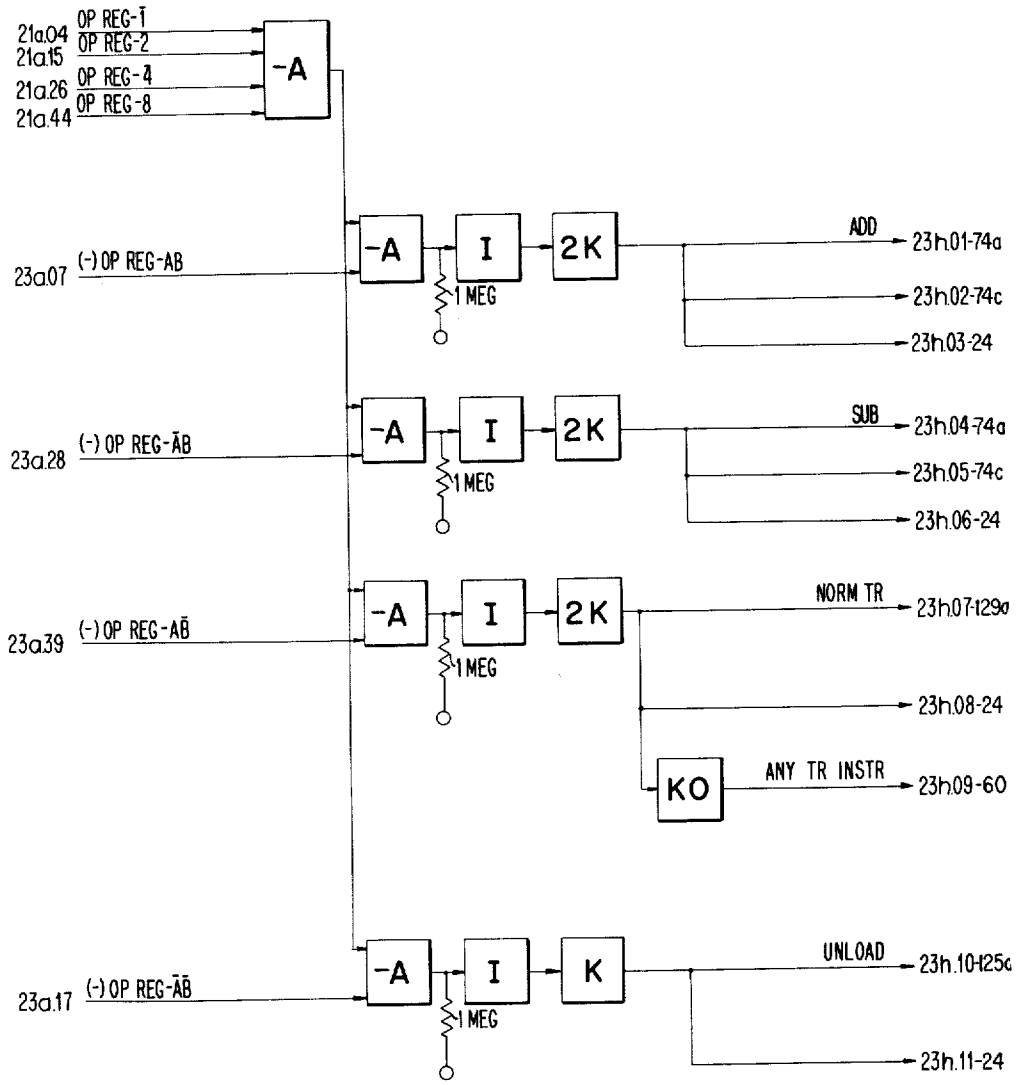


FIG.23i

OPERATION DECODER-R ADD, R SUB, READ, LOAD

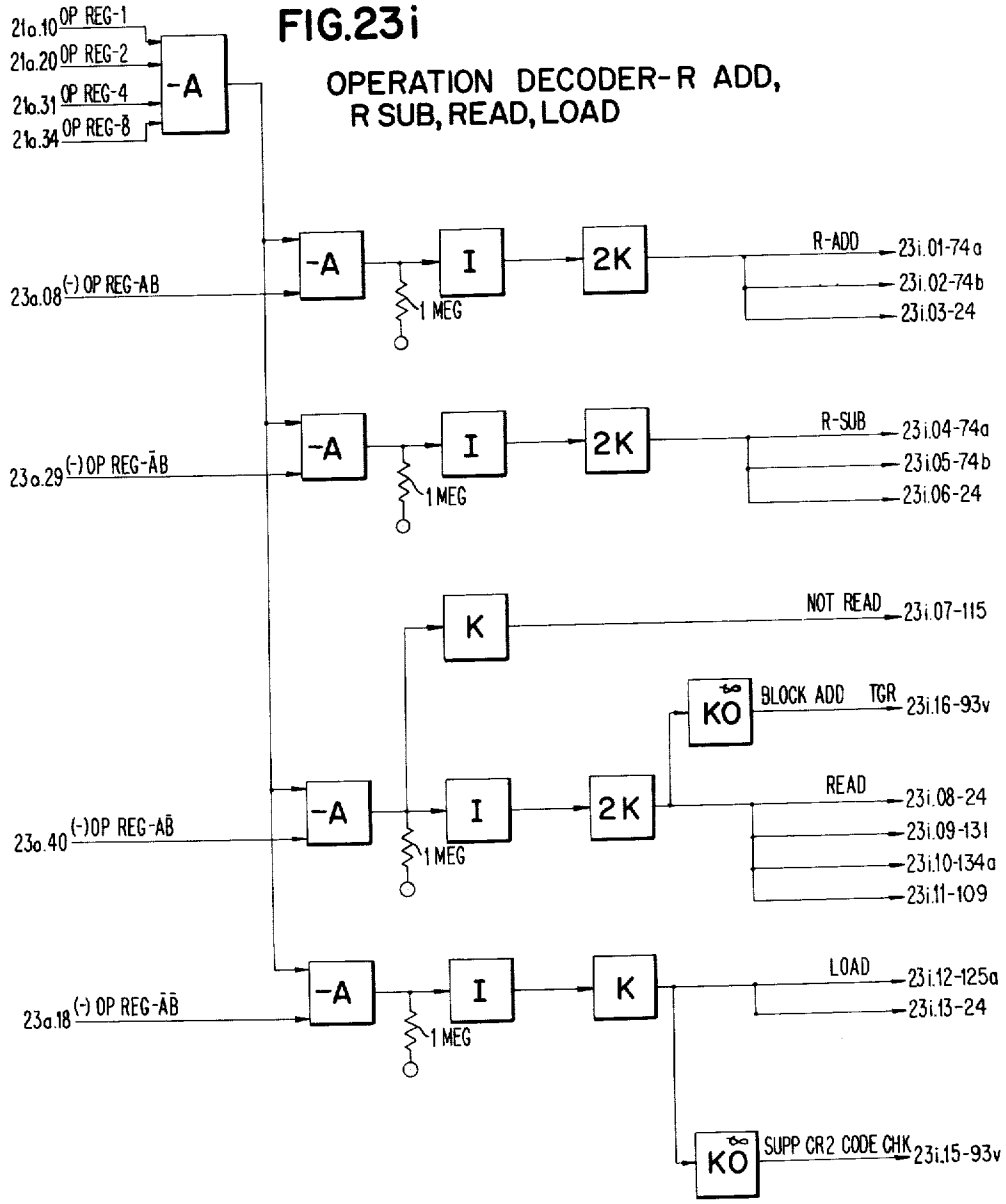
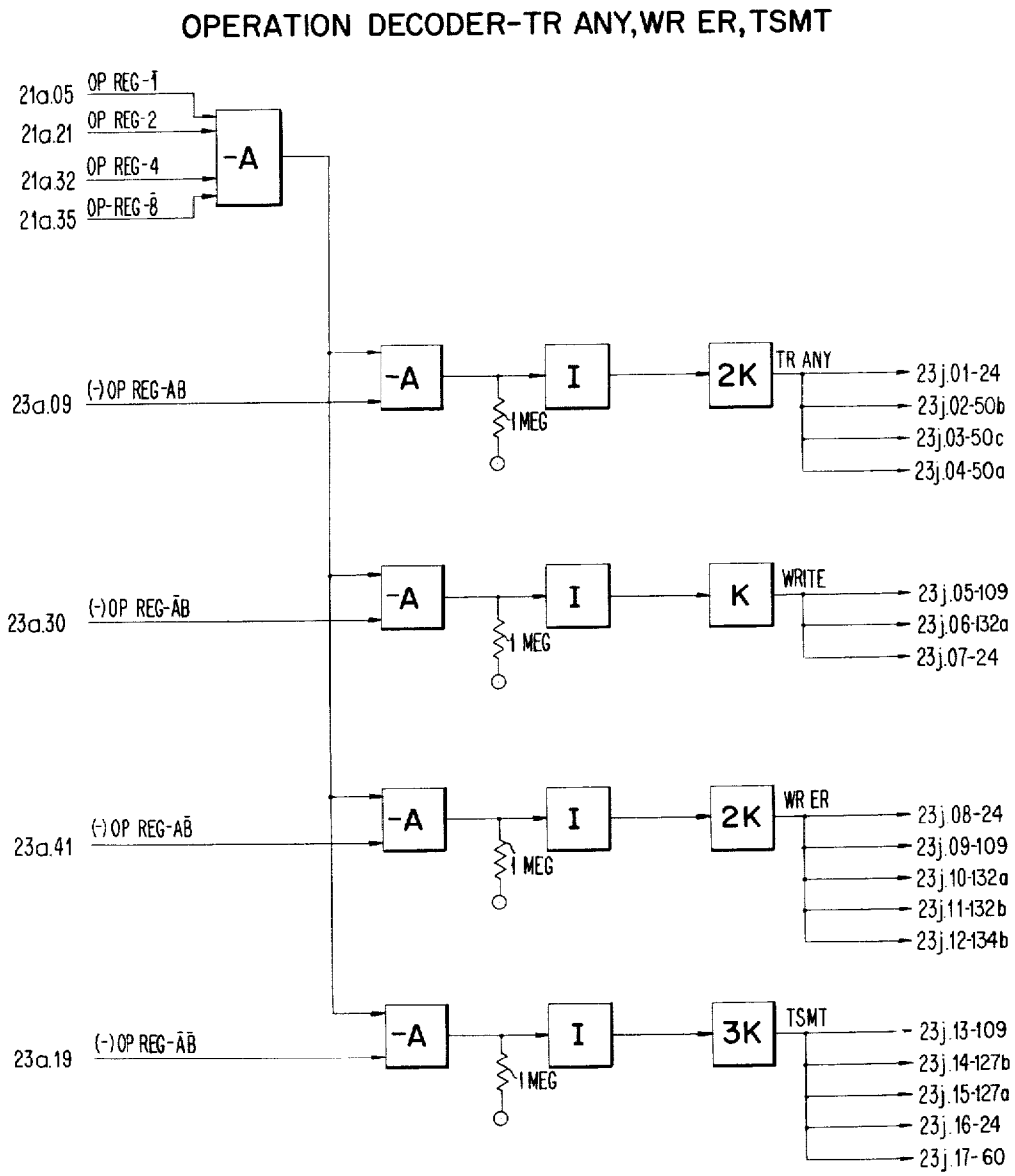


FIG. 23 j


OPERATION DECODER-TR ANY,WR ER,TSMT
21a.05
OP REG-1
21a.21
OP REG-2
21a.32
OP REG-4
21a.35
OP-REG-8
-A
23a.09
(-)OP REG-AB
-A
I
1 MEG
2K
TR ANY
23j.01-24
23j.02-50b
23j.03-50c
23j.04-50a
23a.30
(-)OP REG-ĀB
-A
I
1 MEG
K
WRITE
23j.05-109
23j.06-132a
23j.07-24
23a.41
(-)OP REG-AB̄
-A
I
1 MEG
2K
WR ER
23j.08-24
23j.09-109
23j.10-132a
23j.11-132b
23j.12-134b
23a.19
(-)OP REG-ĀB̄
-A
I
1 MEG
3K
TSMT
23j.13-109
23j.14-127b
23j.15-127a
23j.16-24
23j.17-60

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FIG.23k OPERATION DECODER LDA, BLM, TZB

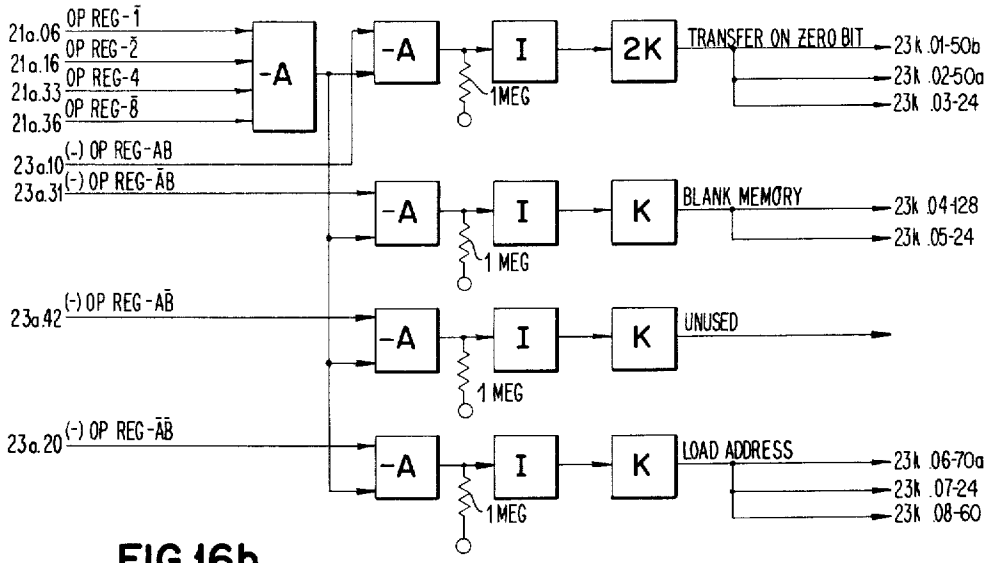


FIG.16b

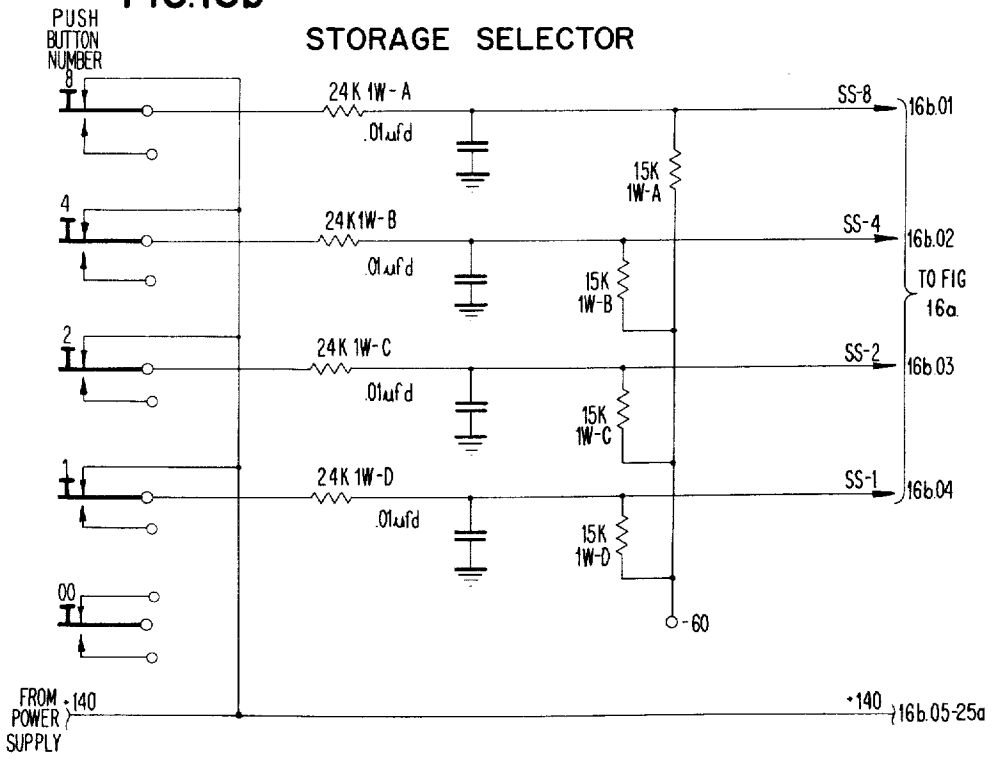


FIG. 24 OPERATION CHECK CIRCUITS

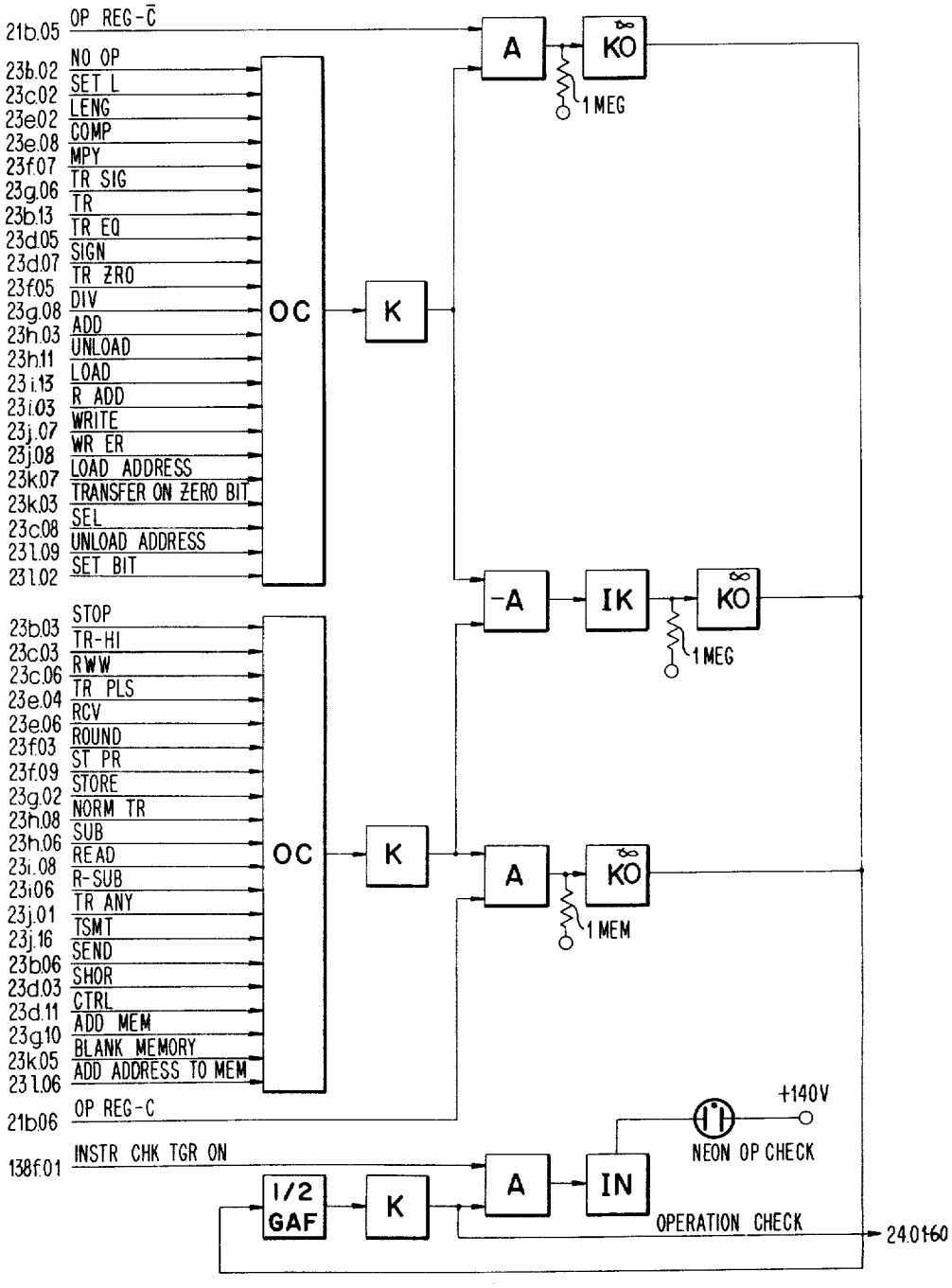


FIG.25a MEMORY ADDRESS SELECTOR KEYS

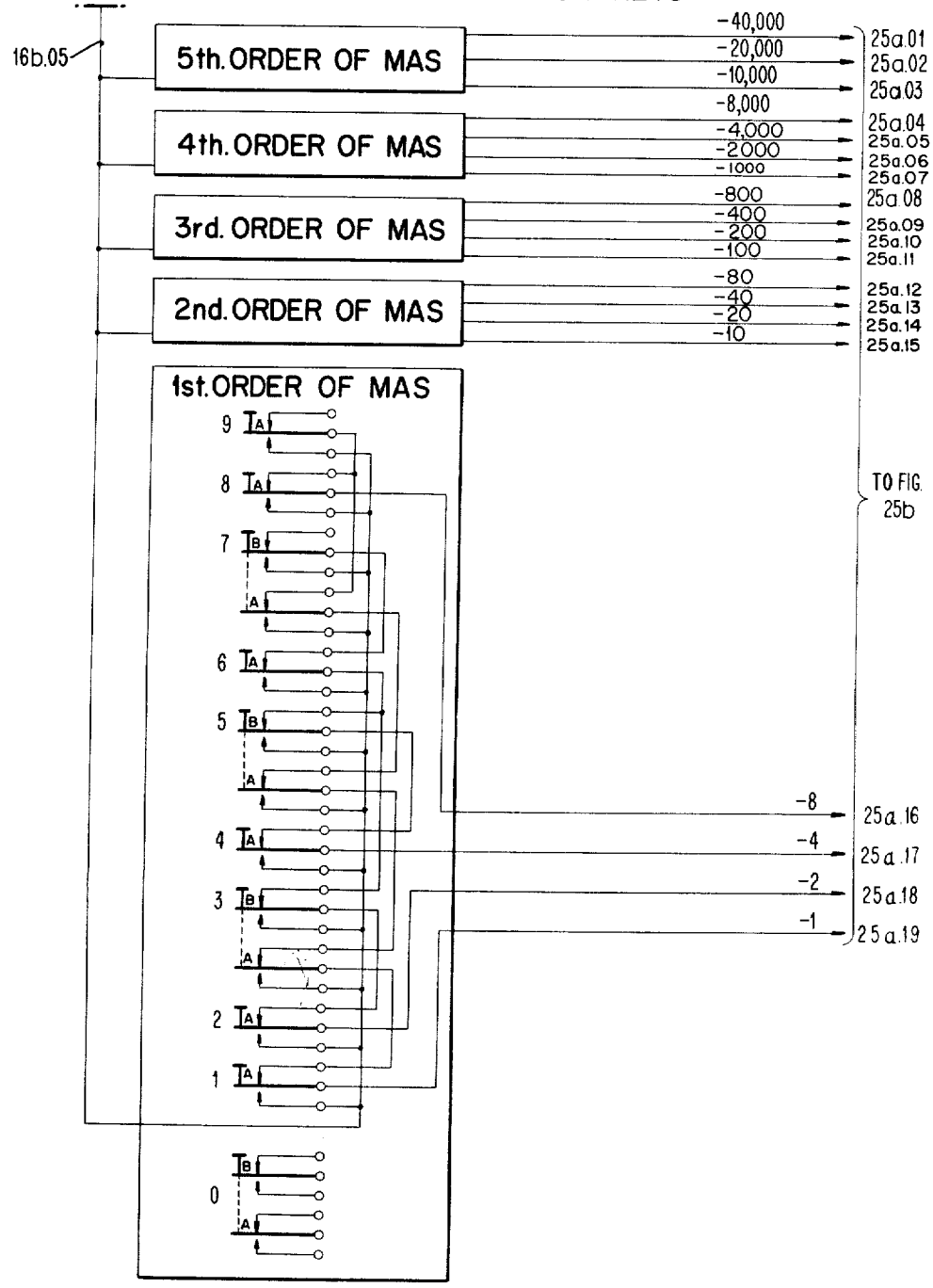


FIG.25b MEMORY ADDRESS SELECTOR KEY OUTPUTS

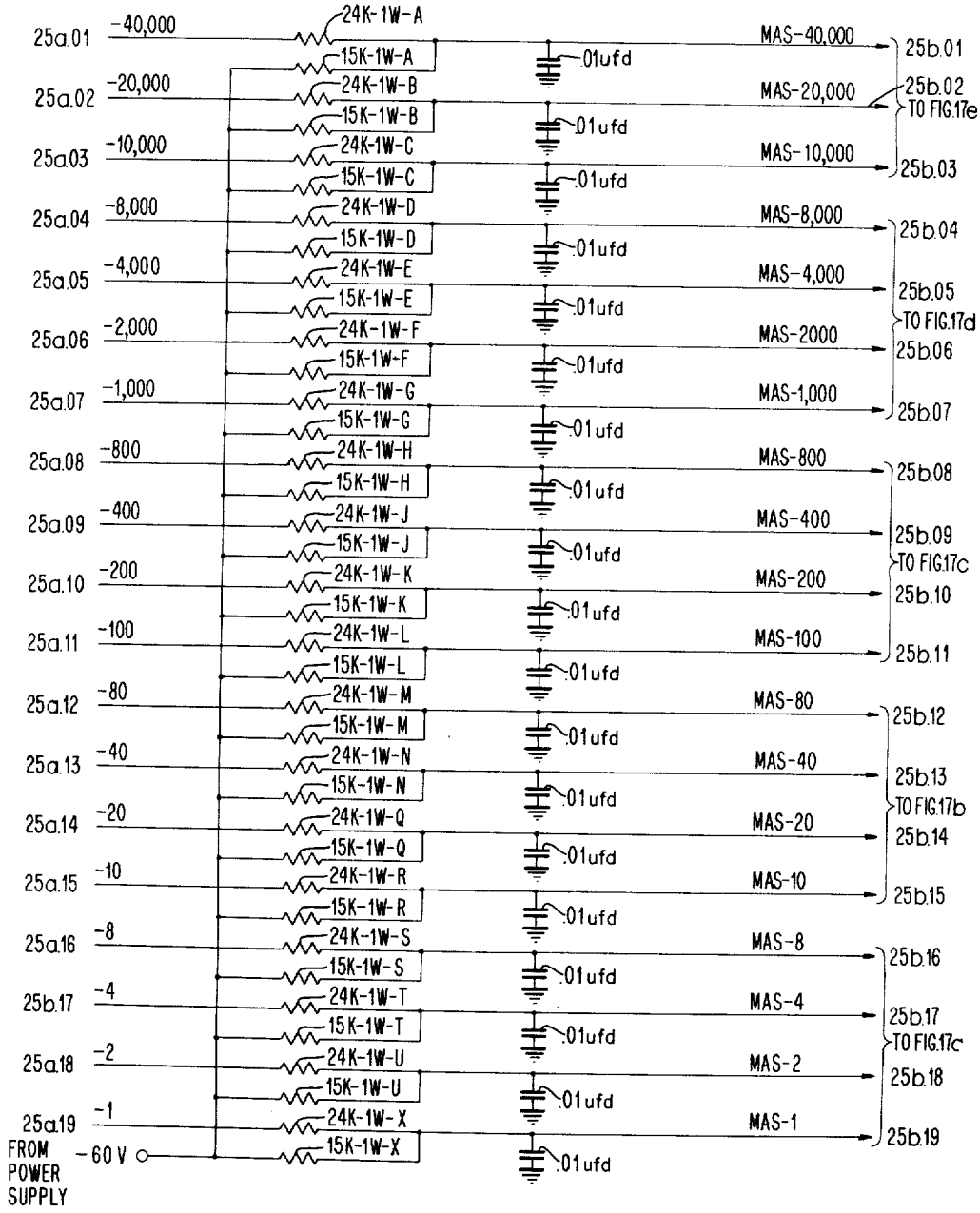


FIG. 26a PARALLEL CHARACTER TRANSMISSION CABLE A CONNECTOR LAYOUT

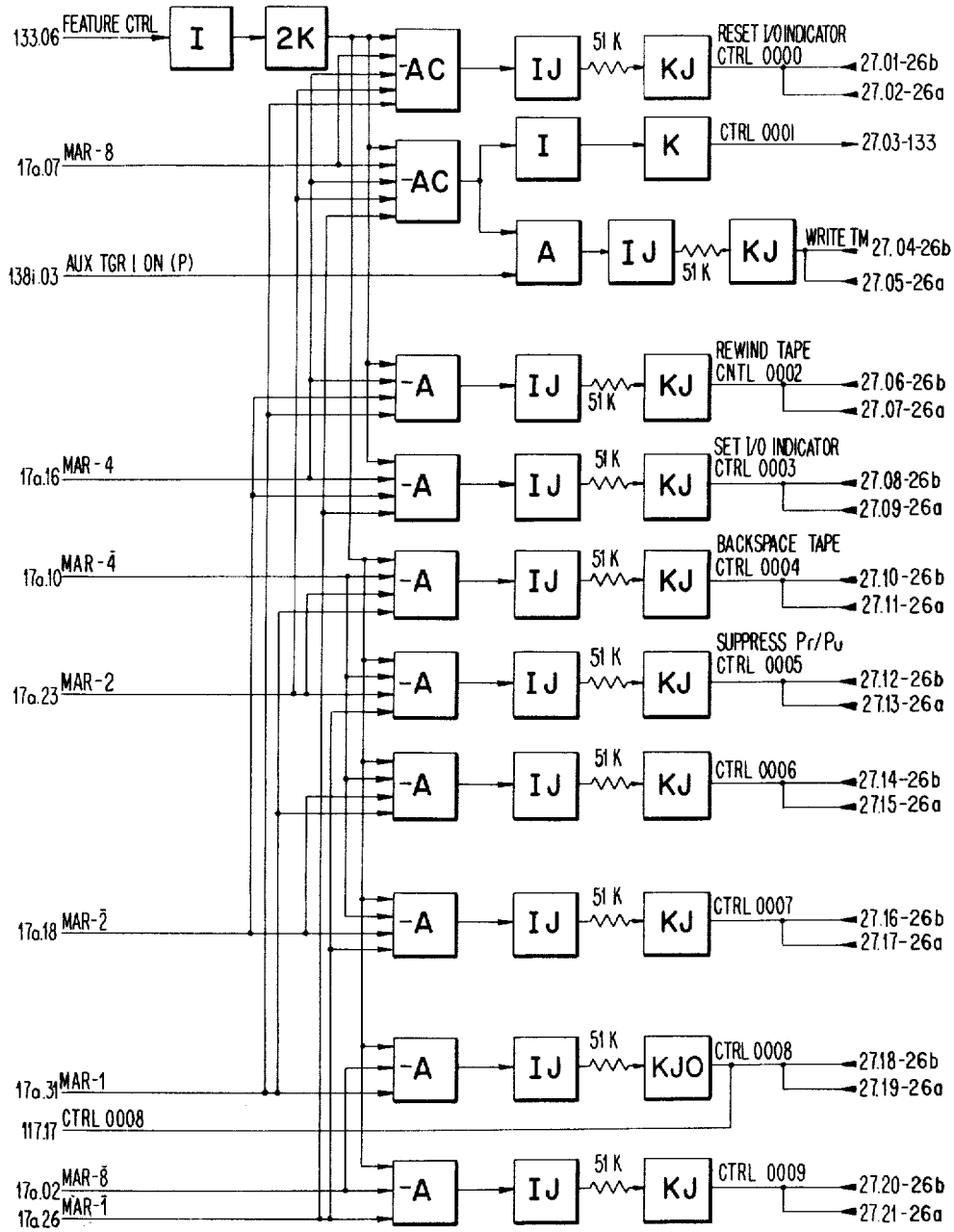
8 PCT ADDR CHECK 109	7 SMAC-MAR CHECK 28.06	6 SPARE	5 PCT CHECK 50c	4 PCT IND ON 134 c	3 SR = 02XX 33f.14	2 SPARE	1 NEON PCT OPEN FIL
16 PCT REQUEST(P) 135 b.21	15 PCT READ 135b	14 PCT READY 50c	13 GND	12 MACH STOP 109.03	11 GND	10 READ CALL (P) 138 b.10	9 GND
24 GND	23 A1/R2-W1 (P) 104.06	22 GND	21 PCT DISC 134 f	20 GND	19 PCT SVC CALL 135a	18 GND	17 SPARE
32 W3-R2 (P) 104.05	31 GND	30 W1-R0 (P) 104.01	29 GND	28 PCT ADDR CHK RESET 109.01	27 GND	26 WRITE CALL (P) 138e.06	25 GND
40 GND	39 WRITE TM 27.05	38 GND	37 CTRL 0000 27.02	36 GND	35 W0-W3 (P) 104.04	34 GND	33 SPARE
48 CTRL 0005 27.13	47 GND	46 CTRL 0004 27.11	45 GND	44 CTRL 0003 27.09	43 GND	42 CTRL 0002 27.07	41 GND
56 GND	55 CTRL 0008 27.19	54 GND	53 CTRL 0007 27.17	52 GND	51 CTRL 0006 27.15	50 GND	49 PCT CHK SMAC 135 a
64 SEL REG 2 33a.08	63 GND	62 SEL REG 1 33a.04	61 GND	60 SEL REG 1000's ORD=0 33f.12	59 GND	58 CTRL 0009 27.21	57 GND
72 GND	71 SEL REG 10 33b.04	70 GND	69 SEL REG 8 33a.15	68 GND	67 SEL REG 4 33a.12	66 GND	65 SPARE
80 SEL REG 100 33c.05	79 GND	78 SEL REG 80 33b.13	77 GND	76 SEL REG 40 33b.10	75 GND	74 SEL REG 20 33b.07	73 GND
88 GND	87 SEL REG 800 33c.15	86 GND	85 SEL REG 400 33c.12	84 GND	83 SEL REG 200 33c.08	82 GND	81 SSR-1(P) 55a.01
96 MAR/MASR 40(P) 29a.04	95 GND	94 MAR/MASR 20(P) 29a.03	93 GND	92 MAR/MASR 10 (P) 29a.02	91 GND	90 MAR/MASR 0/5 29a.01	89 GND
104 GND	103 MAR/MASR 200 (P) 29a.07	102 GND	101 MAR/MASR 100 (P) 29a.06	100 GND	99 MAR/MASR 80 (P) 29a.05	98 GND	97 SSR-2(P) 55a.07
112 MAR/MASR 2000 (P) 29b.03	111 GND	110 MAR/MASR 1,000 (P) 29b.02	109 GND	108 MAR/MASR 800 (P) 29b.01	107 GND	106 MAR/MASR 400 (P) 29a.08	105 GND
120 GND	119 MAR/MASR 10,000 (P) 29b.06	118 GND	117 MAR/MASR 8,000 (P) 29b.05	116 GND	115 MAR/MASR 4,000 (P) 29b.04	114 GND	113 SPARE
128 SMAC 10 17b	127 GND	126 SMAC 0/5 17a	125 GND	124 MAR/MASR 40,000 (P) 29b.08	123 GND	122 MAR/MASR 20,000 (P) 29b.07	121 GND
136 GND	135 SMAC 80 17b	134	133 SMAC 40 17b	132	131 SMAC 20 17b	130	129 DSU SELECTED 132b
144 SMAC 800 17c	143 GND	142 SMAC 400 17c	141 GND	140 SMAC 200 17c	139 GND	138 SMAC 100 17c	137 GND
152 GND	151 SMAC 4000 17d	150 GND	149 SMAC 2000 17d	148 GND	147 SMAC 1000 17d	146 GND	145 SPARE
160 SMAC 40,000 17e	159 GND	158 SMAC 20,000 17e	157 GND	156 SMAC 10,000 17e	155 GND	154 SMAC 8,000 17d	153 GND

FIG. 26b I/O SIGNAL CABLE CONNECTOR LAYOUT SP CONNECTOR RECEPTACLE - WIRING SIDE

8 GND	7 READY 50c	6 GND	5 I/O SYNC PULSE 134f.01	4 GND	3 SPARE	2 GND	1 SPARE
16 READ BUS 8 48	15 GND	14 READ BUS 4 48	13 GND	12 READ BUS 2 48	11 GND	10 READ BUS 1 48	9 GND
24 GND	23 END R/W(P) 93t.01	22 GND	21 READ BUS C 48	20 GND	19 READ BUS B 48	18 GND	17 READ BUS A 48
32 WR BUS 8 58.41	31 GND	30 WR BUS 4 58.46	29 GND	28 WR BUS 2 58.51	27 GND	26 WR BUS 1 58.56	25 GND
40 GND	39 PREPARE TO READ (P) 93t.10	38 GND	37 WR BUS C 58.04	36 GND	35 WR BUS B 58.21	34 GND	33 WR BUS A 58.36
48 WR TM 27.04	47 GND	46 CTRL 0000 27.01	45 GND	44 WR CALL (P) 138e.05	43 GND	42 RD CALL (P) 138b.07	41 GND
56 GND	55 CTRL 0005 27.12	54 GND	53 CTRL 0004 27.10	52 GND	51 CTRL 0003 27.08	50 GND	49 CTRL 0002 27.06
64 CTRL 0009 27.20	63 GND	62 CTRL 0008 27.18	61 GND	60 CTRL 0007 27.16	59 GND	58 CTRL 0006 27.14	57 GND
72 GND	71 I/O OPEN FIL	70 GND	69 I/O IND ON 134c	68 GND	67 R/W ERROR 134c	66 GND	65 RECORD ERROR 134c
80 READ DISC 93t	79 GND	78 READ RESPONSE 93t	77 GND	76 WRITE DISC 93t	75 GND	74 WRITE RESPONSE 93t	73 GND
88 DC RETURN	87 GND	86 GND	85 GND	84 GND	83 GND	82 GND	81 DC RETURN
96 SEL REG 80 33b.12	95 SEL REG 40 33b.09	94 SEL REG 20 33b.06	93 SEL REG 10 33b.03	92 SEL REG 8 33a.14	91 SEL REG 4 33a.11	90 SEL REG 2 33a.07	89 SEL REG 1 33a.03
104 SEL REG 8000 33d.08	103 SEL REG 4000 33d.06	102 SEL REG 2000 33d.04	101 SEL REG 1000 33d.02	100 SEL REG 800 33c.14	99 SEL REG 400 33c.11	98 SEL REG 200 33c.07	97 SEL REG 100 33c.04
112 SPARE	111 SPARE	110 SPARE	109 SPARE	108 SPARE	107 SPARE	106 SPARE	105 SR 1000 ORDER = 0 33f.11
120 SPARE	119 SPARE	118 SPARE	117 SPARE	116 SPARE	115 SPARE	114 SPARE	113 SPARE
128 SPARE	127 SPARE	126 SPARE	125 SPARE	124 SPARE	123 SPARE	122 SPARE	121 SPARE
136 SPARE	135 SPARE	134 SPARE	133 SPARE	132 SPARE	131 SPARE	130 SPARE	129 SPARE
144	143	142	141 SPARE	140 SPARE	139	138	137
152	151	150	149	148	147	146	145
160	159	158	157	156	155	154	153

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FIG. 27 CONTROL ADDRESS DECODER



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FIG.28

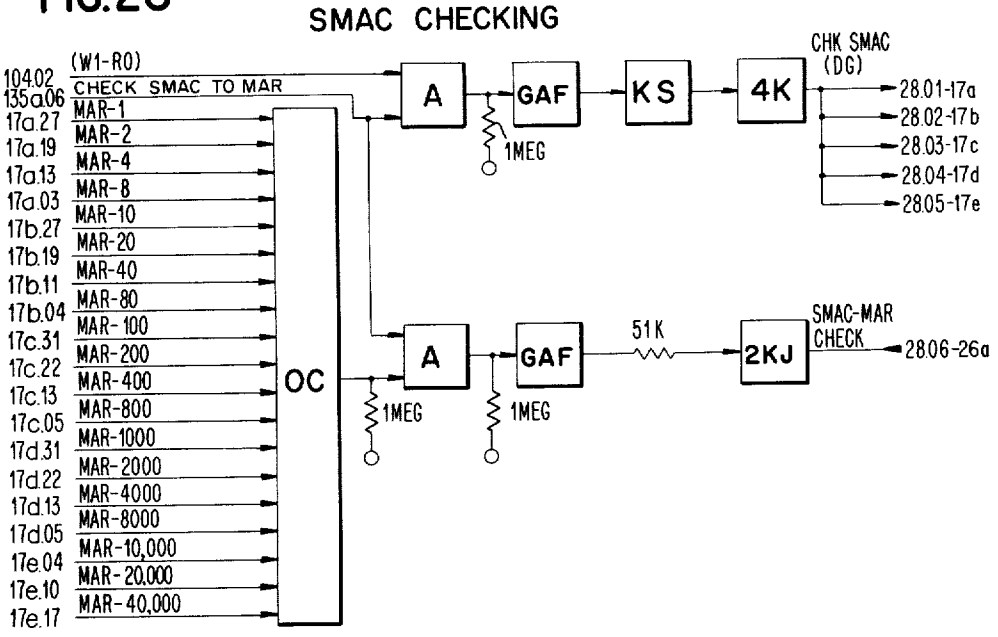


FIG.31e

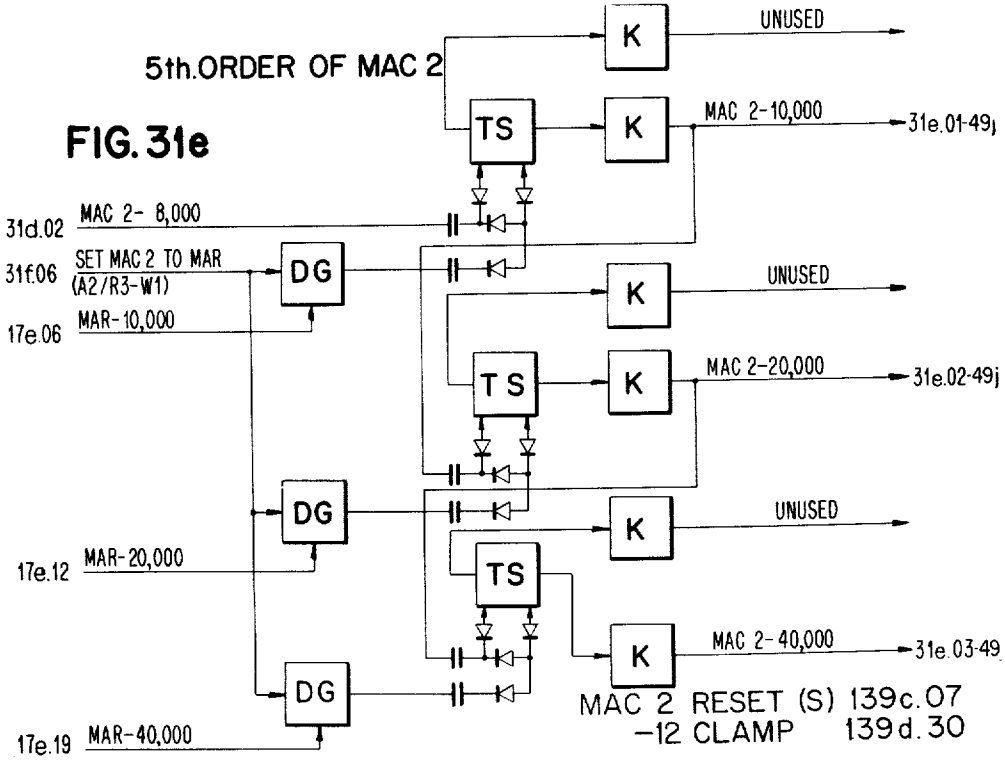
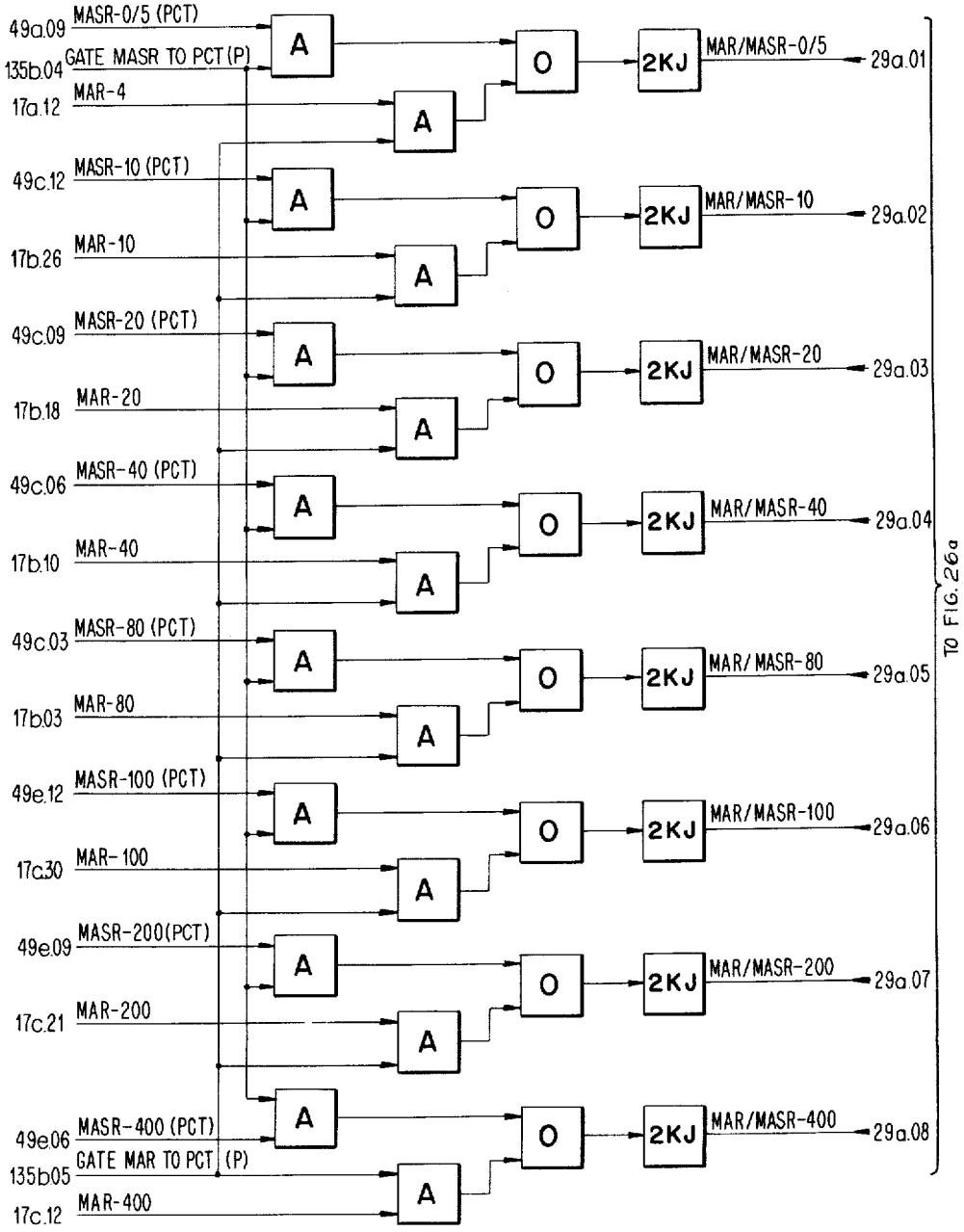


FIG.29a MASR/MAR TO DSU POWERING



MASR/MAR TO DSU POWERING

FIG. 29b

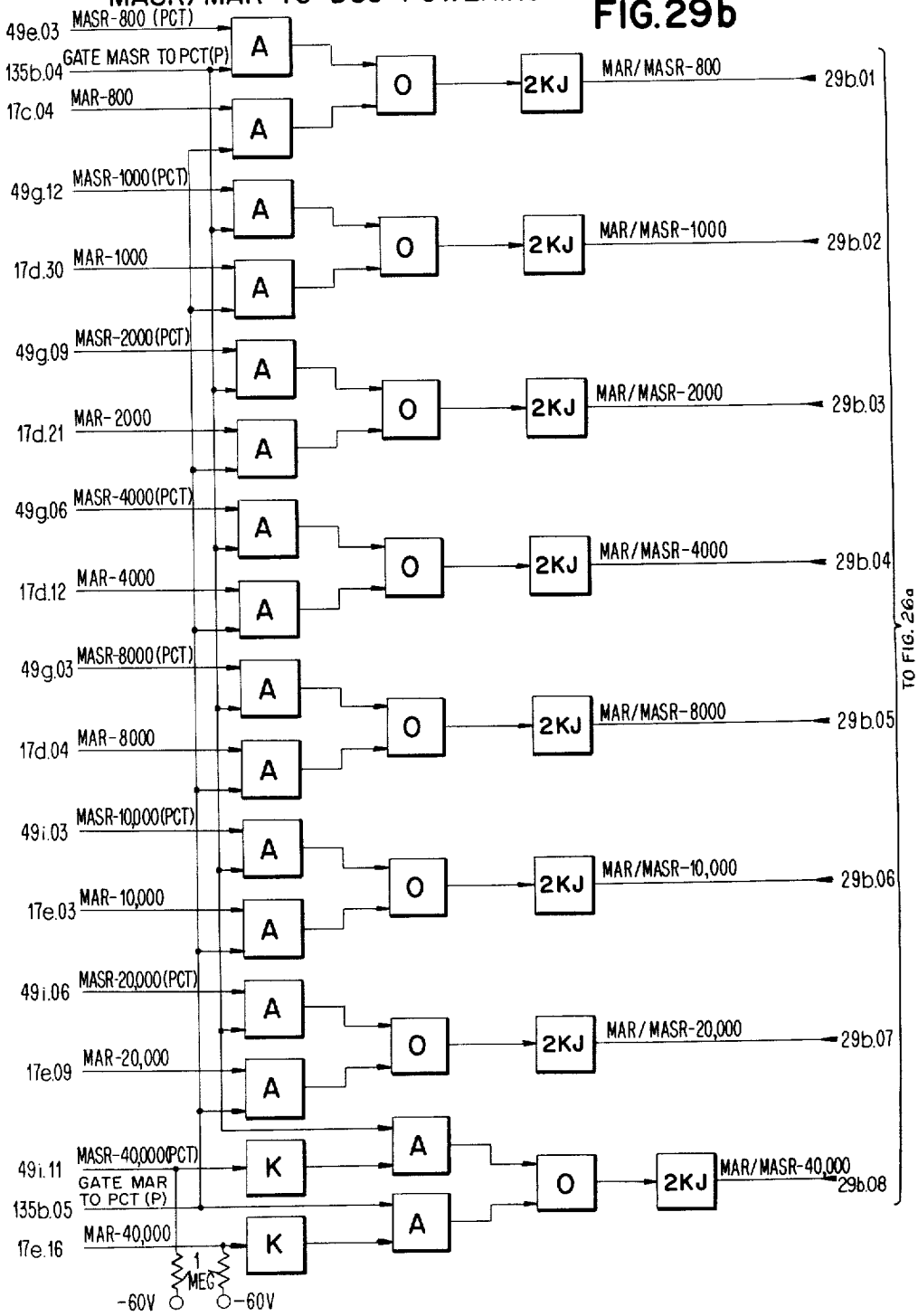
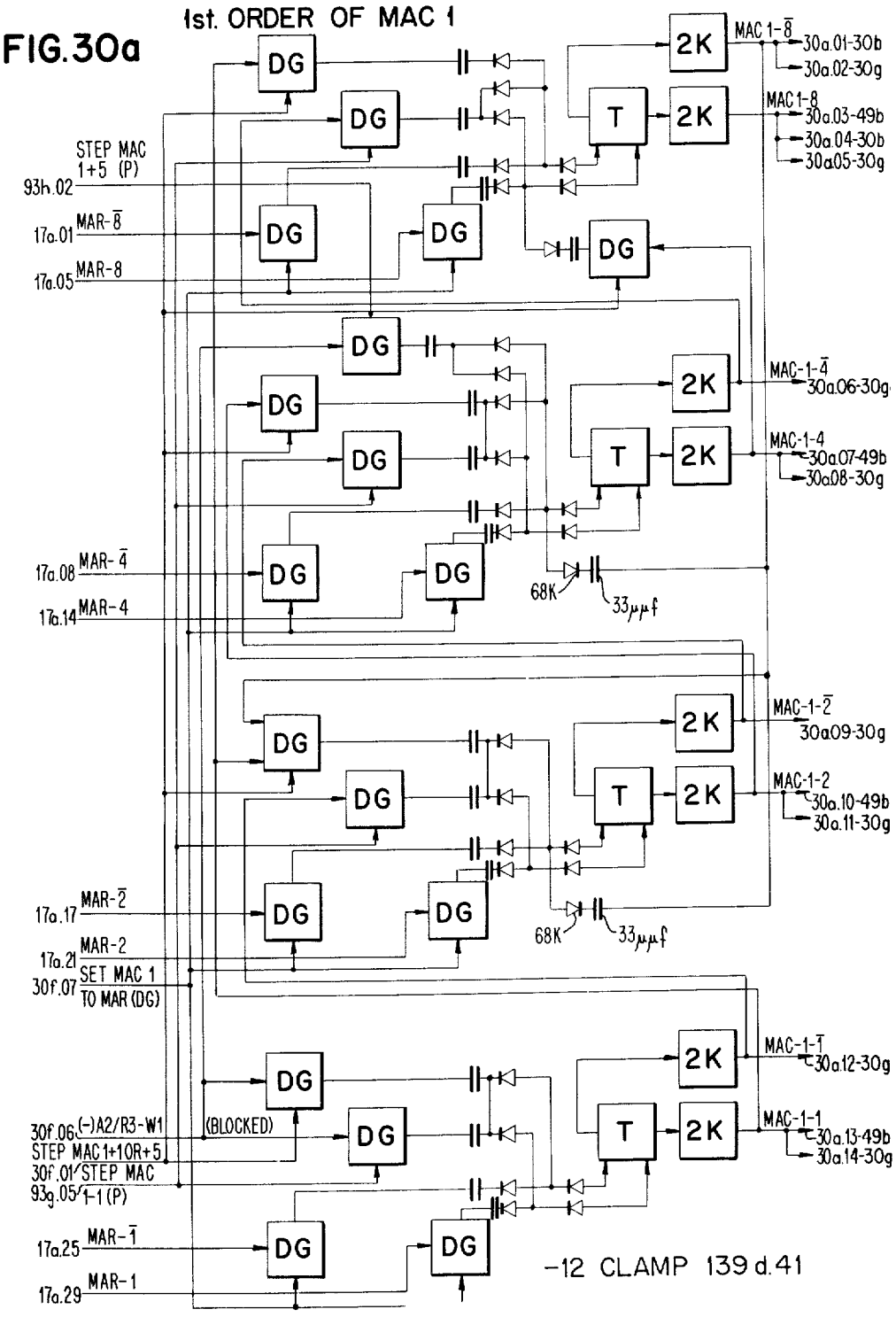


FIG.30a

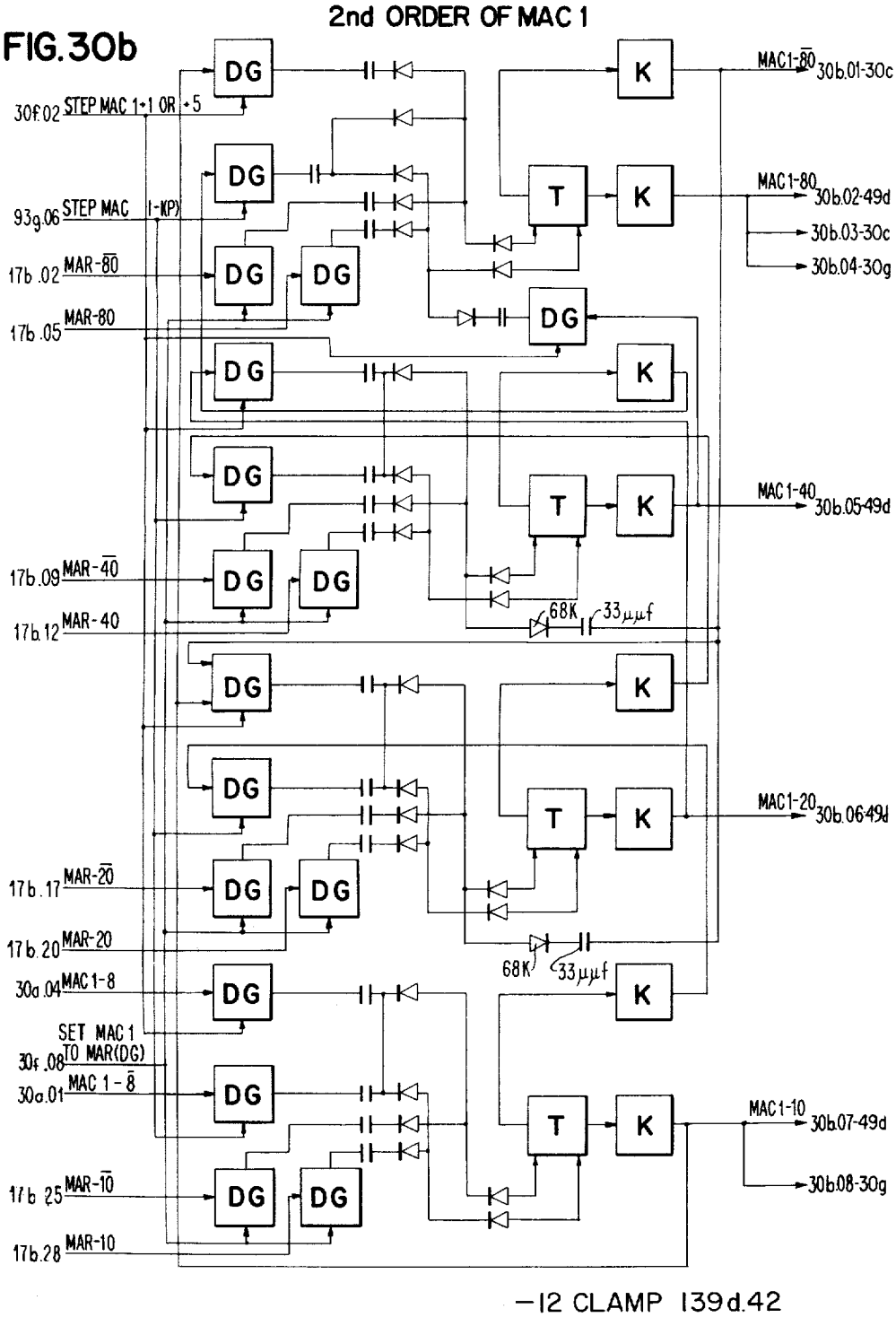

1st. ORDER OF MAC 1
DG
2K
T
MAC 1-8
30a.01-30b
30a.02-30g
MAC 1-8
30a.03-49b
30a.04-30b
30a.05-30g
STEP MAC 1+5 (P)
93h.02
17a.01 MAR-8
17a.05 MAR-8
MAC-1-4
30a.06-30g
MAC-1-4
30a.07-49b
30a.08-30g
17a.08 MAR-4
17a.14 MAR-4
68K
33μμf
MAC-1-2
30a.09-30g
MAC-1-2
30a.10-49b
30a.11-30g
17a.17 MAR-2
17a.21 MAR-2
30f.07 SET MAC 1 TO MAR (DG)
MAC-1-1
30a.12-30g
MAC-1-1
30a.13-49b
30a.14-30g
30f.06 (-)A2/R3-W1
(BLOCKED)
STEP MAC 1+10R+5
30f.01 STEP MAC 93g.05 1-1 (P)
17a.25 MAR-1
17a.29 MAR-1
-12 CLAMP 139 d.41

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FIG.30b



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FIG. 30c

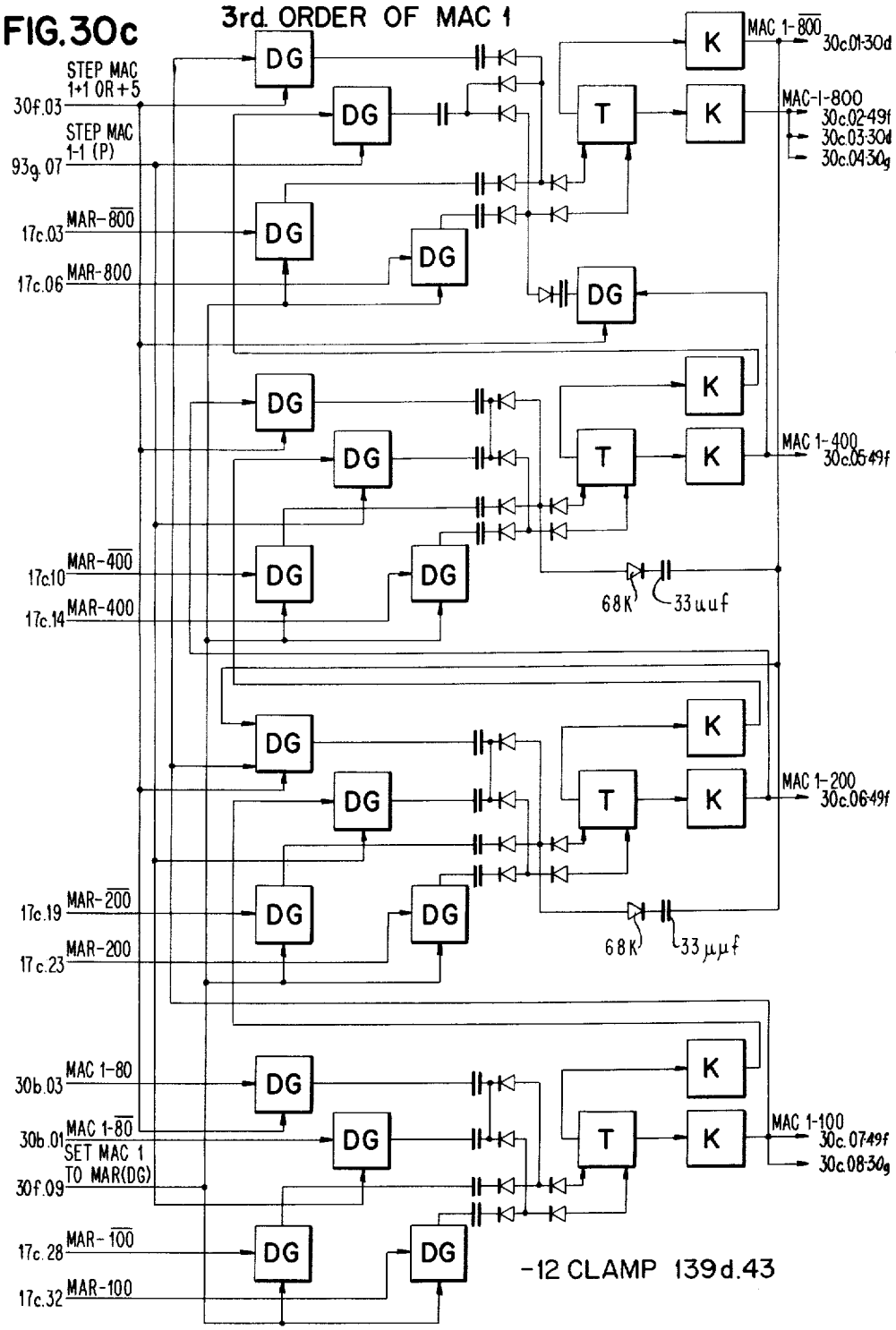


FIG. 30d

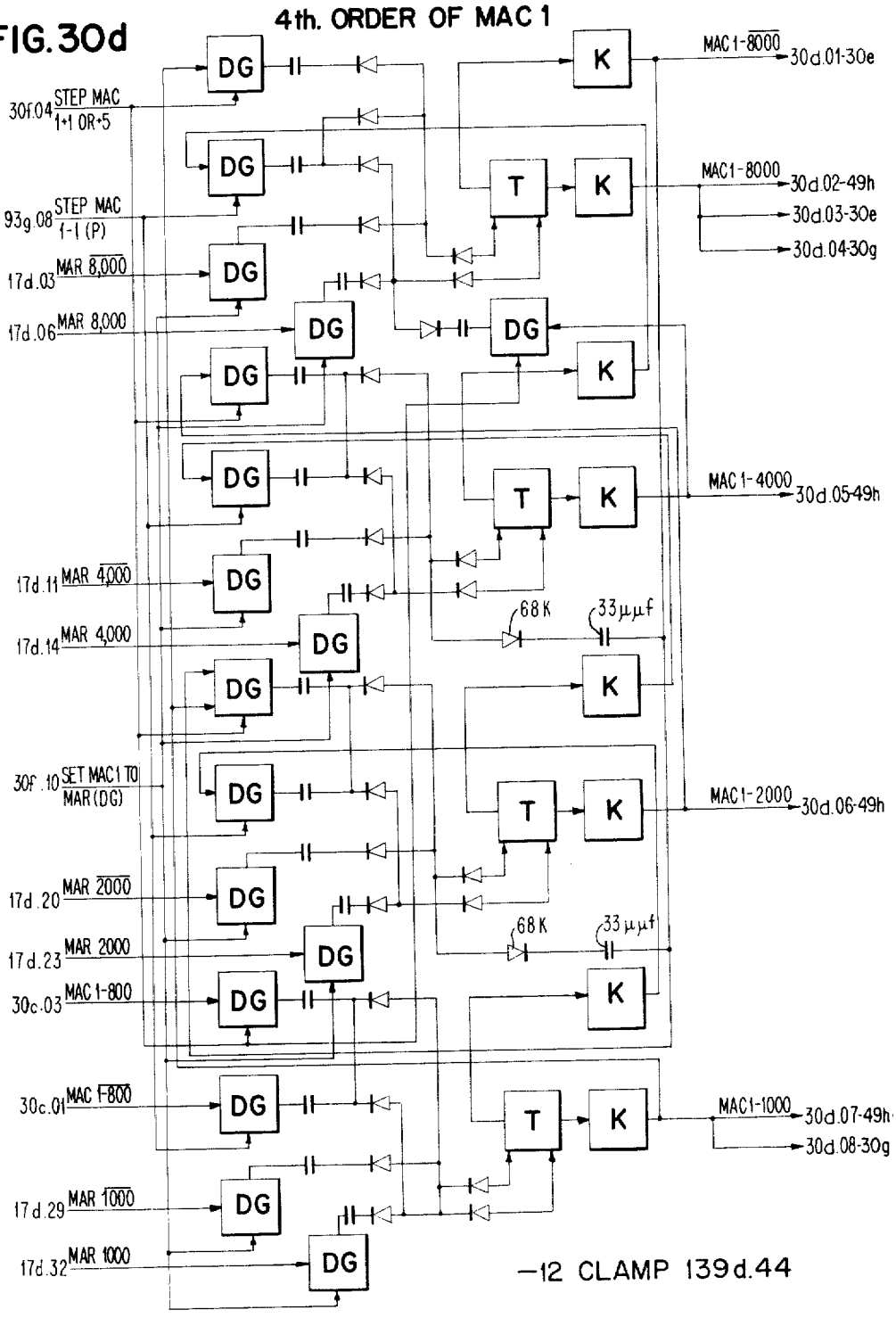

4th. ORDER OF MAC 1
DG
K
T
MAC 1-8000
30d.01-30e
30f.04 STEP MAC 1+1 OR+5
93g.08 STEP MAC 1-1 (P)
MAC 1-8000
30d.02-49h
30d.03-30e
30d.04-30g
17d.03 MAR 8,000
17d.06 MAR 8,000
MAC 1-4000
30d.05-49h
17d.11 MAR 4,000
17d.14 MAR 4,000
68K
33μμf
30f.10 SET MAC 1 TO MAR (DG)
MAC 1-2000
30d.06-49h
17d.20 MAR 2000
17d.23 MAR 2000
30c.03 MAC 1-800
30c.01 MAC 1-800
MAC 1-1000
30d.07-49h
30d.08-30g
17d.29 MAR 1000
17d.32 MAR 1000
-12 CLAMP 139d.44

FIG.30e

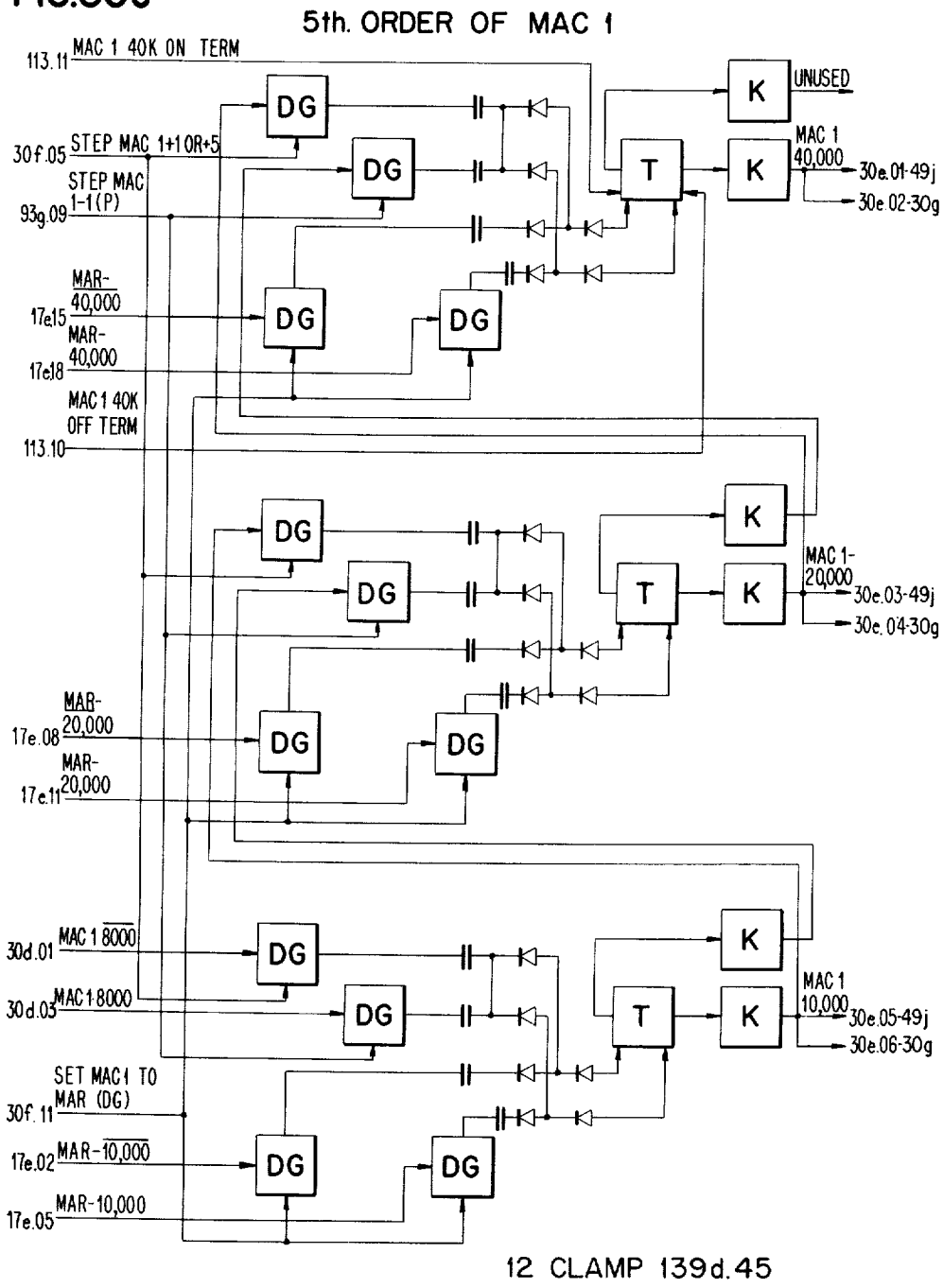

5th. ORDER OF MAC 1
113.11 MAC 1 40K ON TERM
30f.05 STEP MAC 1+1 OR+5
93g.09 STEP MAC 1-1(P)
17e.15 MAR-40,000
17e.18 MAR-40,000
113.10 MAC 1 40K OFF TERM
17e.08 MAR-20,000
17e.11 MAR-20,000
30d.01 MAC 1 8000
30d.03 MAC 1 8000
30f.11 SET MAC 1 TO MAR (DG)
17e.02 MAR-10,000
17e.05 MAR-10,000
DG
T
K
UNUSED
MAC 1 40,000
30e.01-49j
30e.02-30g
MAC 1-20,000
30e.03-49j
30e.04-30g
MAC 1 10,000
30e.05-49j
30e.06-30g
12 CLAMP 139d.45

FIG.30f

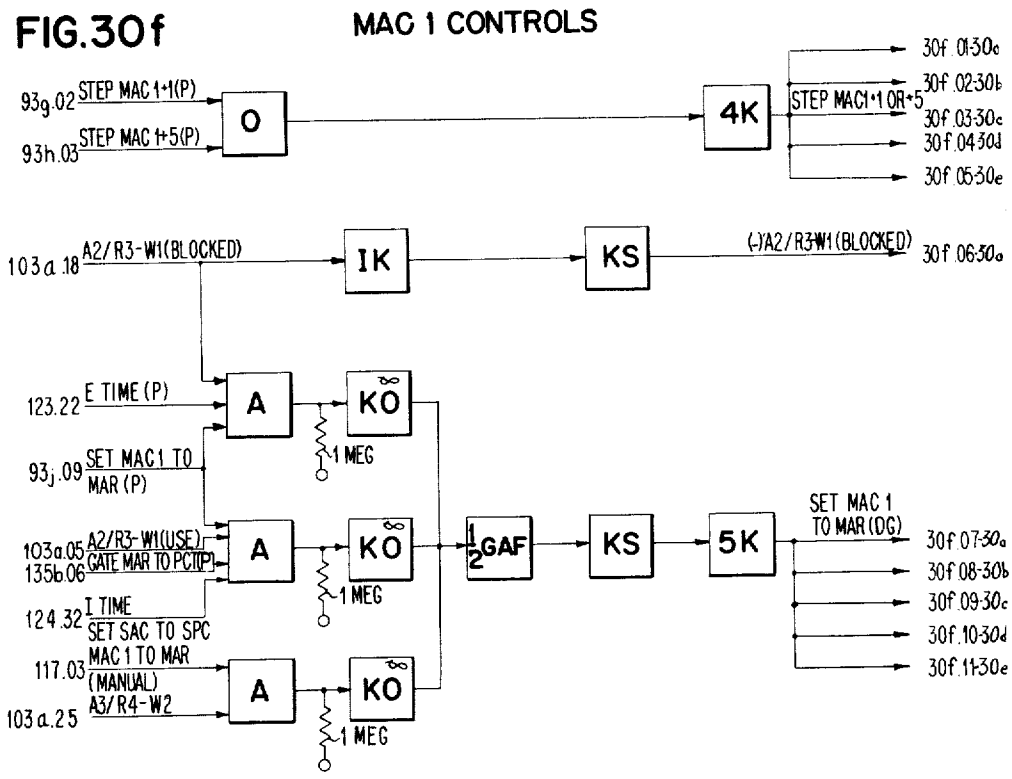


FIG.31f

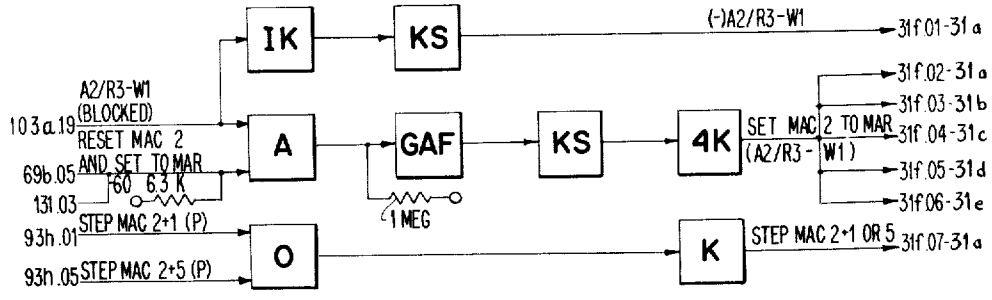


FIG.30g

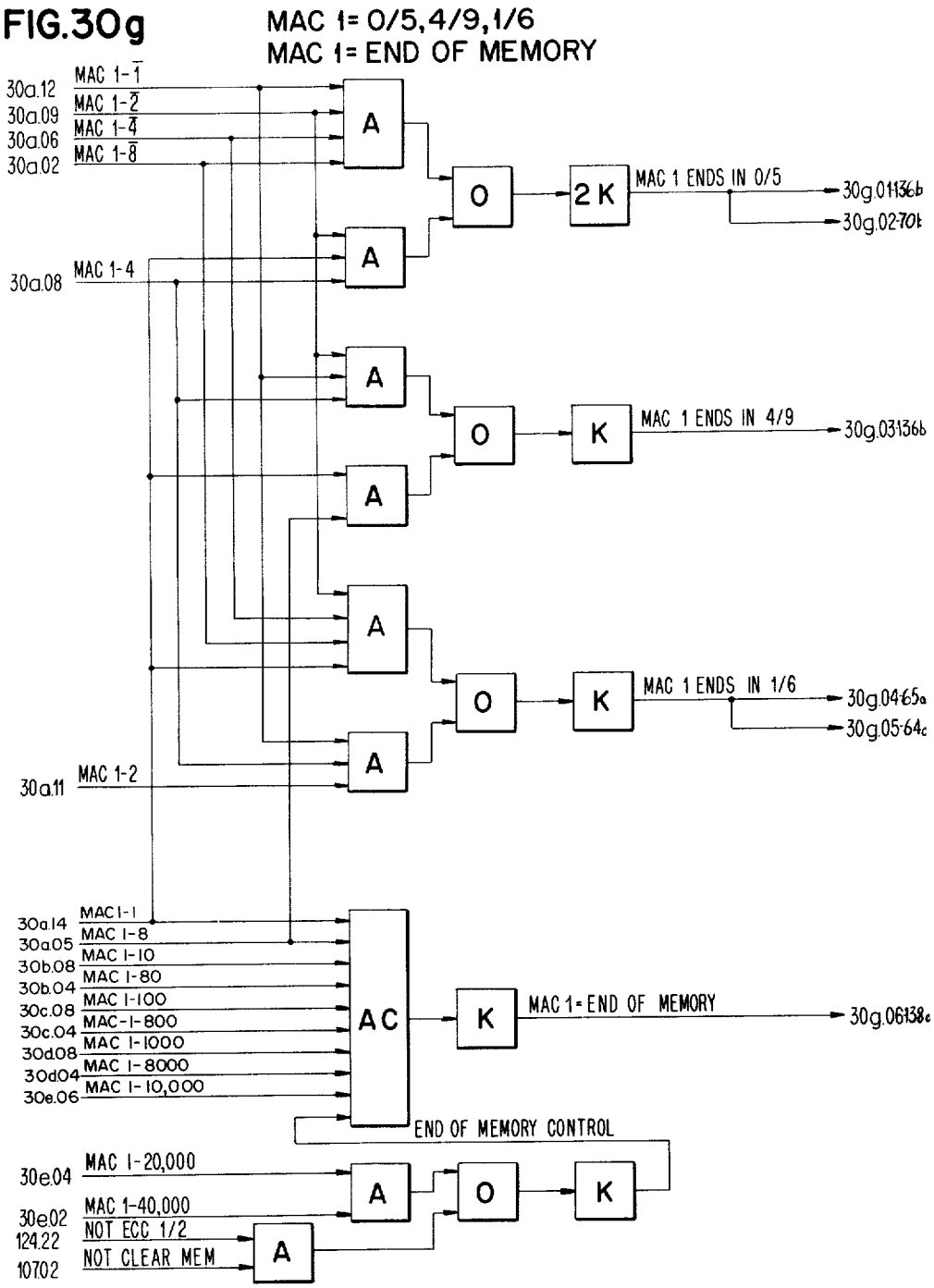

MAC 1= 0/5,4/9,1/6
MAC 1= END OF MEMORY
30a.12
30a.09
30a.06
30a.02
MAC 1-1
MAC 1-2
MAC 1-4
MAC 1-8
A
O
2 K
MAC 1 ENDS IN 0/5
30g.01136b
30g.02-70b
30a.08
MAC 1-4
K
MAC 1 ENDS IN 4/9
30g.03136b
MAC 1 ENDS IN 1/6
30g.04-65a
30g.05-64c
30a.11
MAC 1-2
30a.14
30a.05
30b.08
30b.04
30c.08
30c.04
30d.08
30d.04
30e.06
MAC 1-1
MAC 1-8
MAC 1-10
MAC 1-80
MAC 1-100
MAC-1-800
MAC 1-1000
MAC 1-8000
MAC 1-10,000
AC
MAC 1= END OF MEMORY
30g.06138c
END OF MEMORY CONTROL
30e.04
30e.02
124.22
107.02
MAC 1-20,000
MAC 1-40,000
NOT ECC 1/2
NOT CLEAR MEM

FIG. 31a

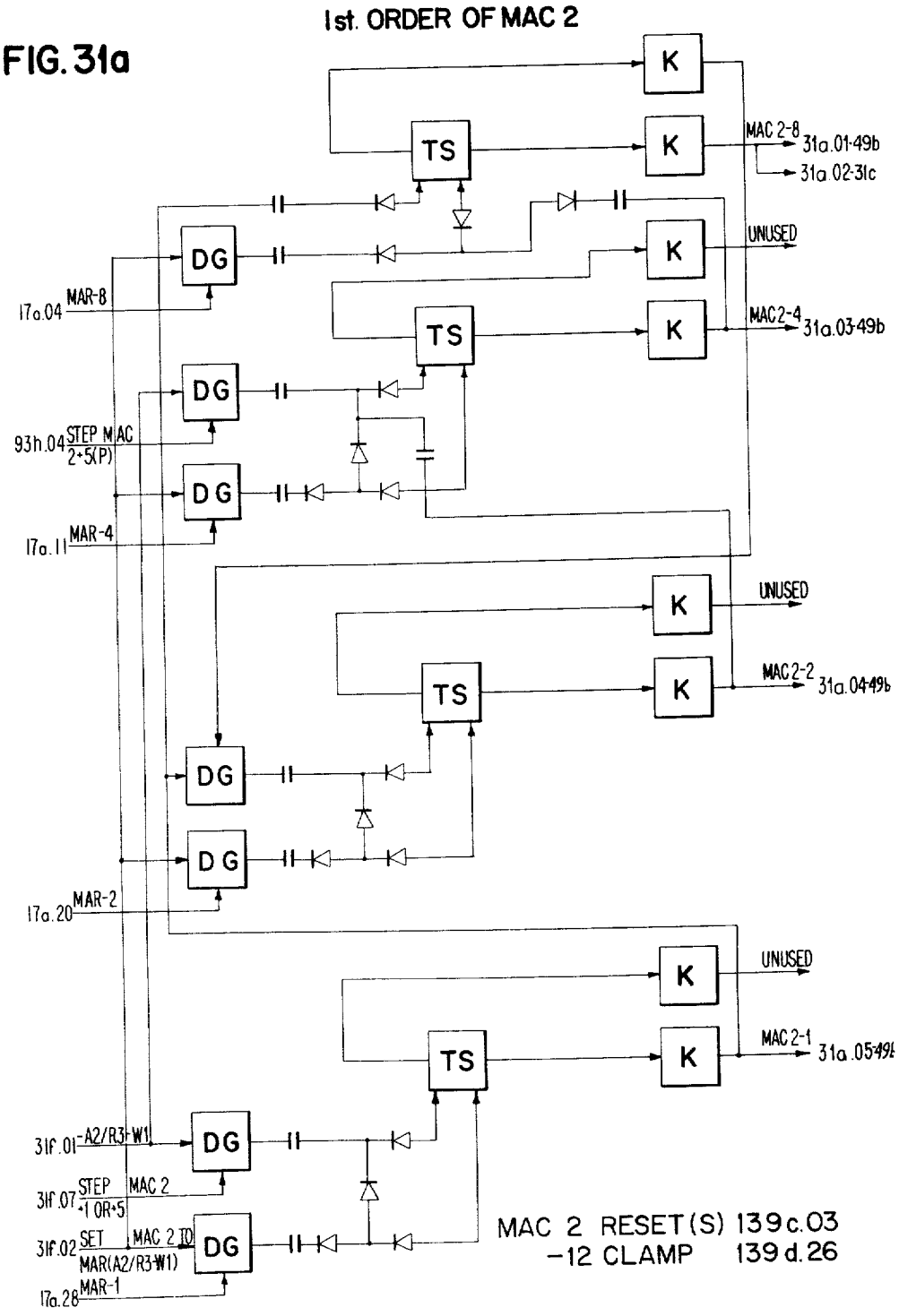

1st. ORDER OF MAC 2
K
TS
DG
MAC 2-8
31a.01-49b
31a.02-31c
UNUSED
MAC 2-4
31a.03-49b
MAC 2-2
31a.04-49b
MAC 2-1
31a.05-49b
17a.04 MAR-8
93h.04 STEP MAC 2+5(P)
17a.11 MAR-4
17a.20 MAR-2
31f.01 -A2/R3+W1
31f.07 STEP +1 OR+5 MAC 2
31f.02 SET MAR(A2/R3+W1) MAC 2 ID
17a.28 MAR-1
MAC 2 RESET(S) 139c.03
-12 CLAMP 139d.26

FIG. 31b

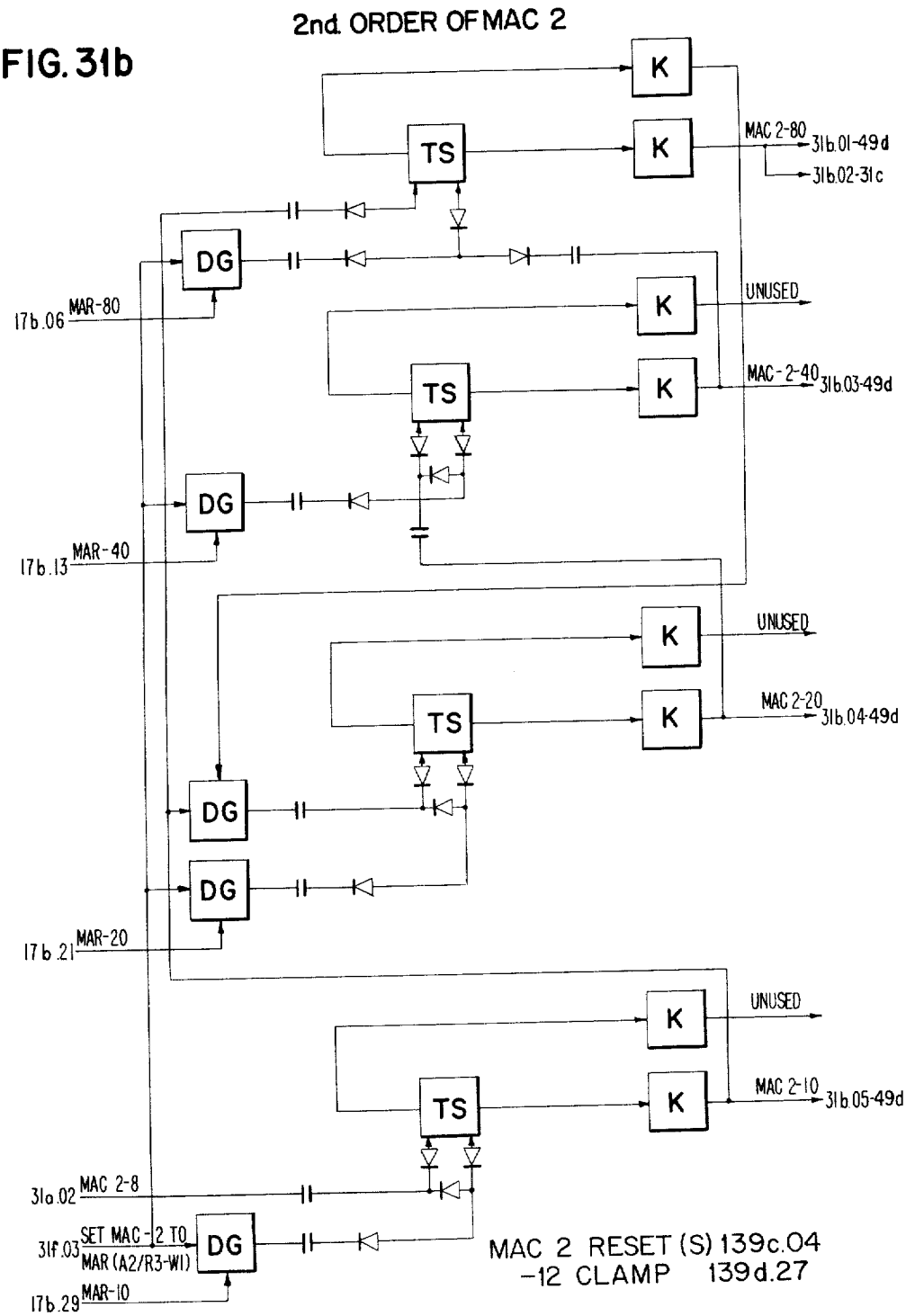
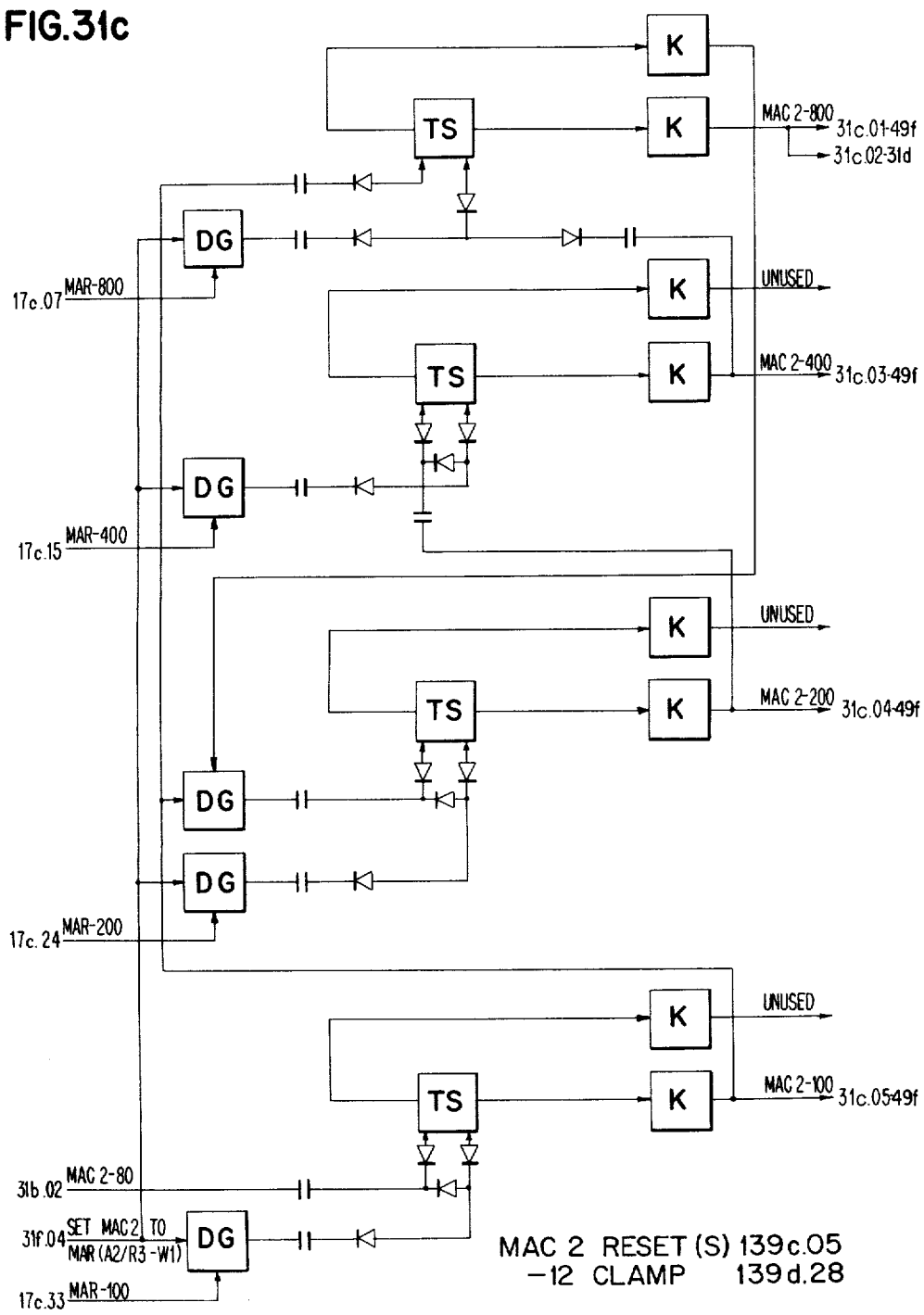

2nd ORDER OF MAC 2
K
TS
DG
MAC 2-80
31b.01-49d
31b.02-31c
UNUSED
MAC-2-40
31b.03-49d
MAC 2-20
31b.04-49d
MAC 2-10
31b.05-49d
17b.06 MAR-80
17b.13 MAR-40
17b.21 MAR-20
17b.29 MAR-10
31a.02 MAC 2-8
31f.03 SET MAC-2 TO MAR (A2/R3-W1)
MAC 2 RESET (S) 139c.04
-12 CLAMP 139d.27

FIG.31c

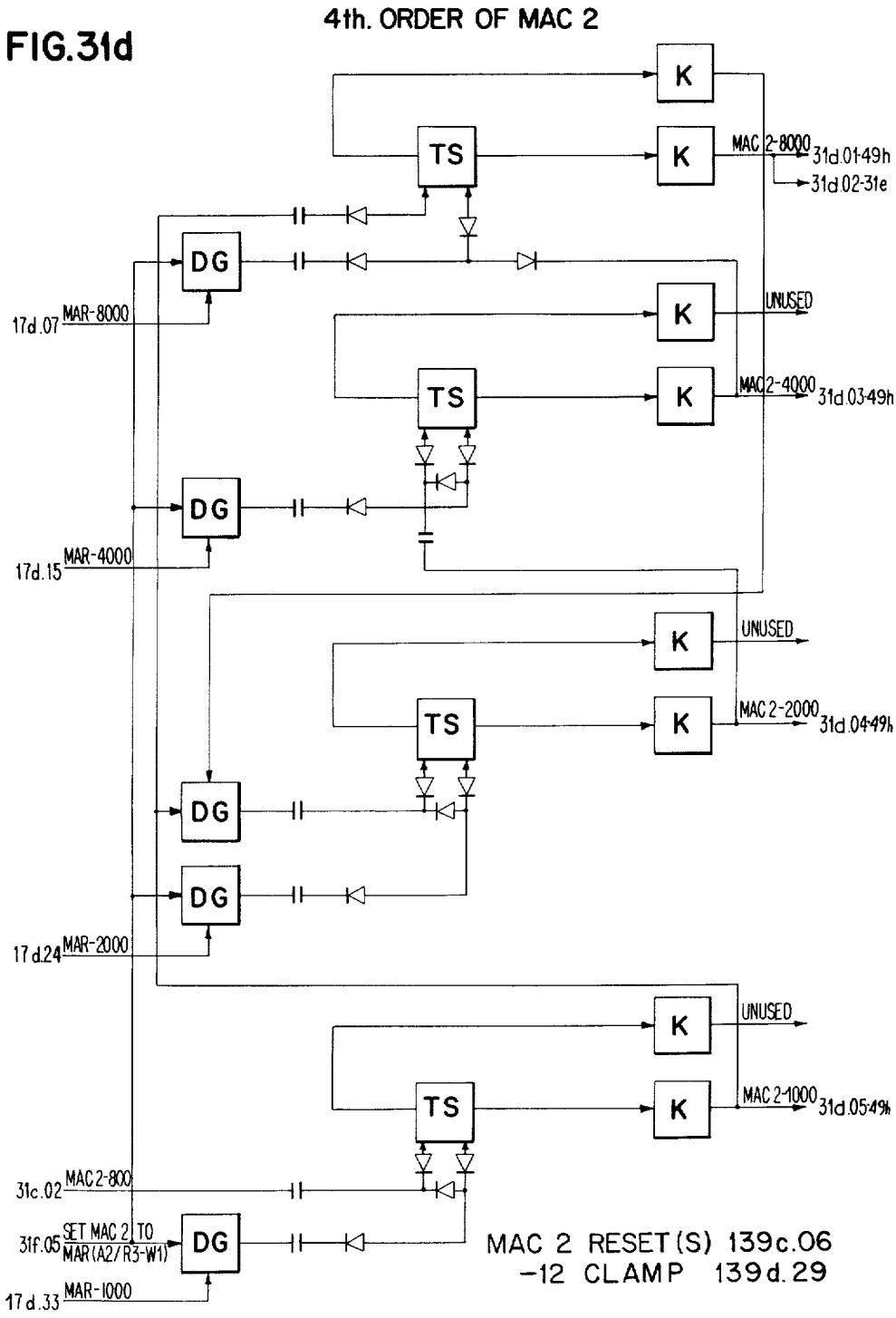

3rd. ORDER OF MAC 2
K
TS
K
MAC 2-800
31c.01-49f
31c.02-31d
DG
17c.07 MAR-800
K
UNUSED
TS
K
MAC 2-400
31c.03-49f
DG
17c.15 MAR-400
K
UNUSED
TS
K
MAC 2-200
31c.04-49f
DG
DG
17c.24 MAR-200
K
UNUSED
TS
K
MAC 2-100
31c.05-49f
31b.02 MAC 2-80
31f.04 SET MAC 2 TO MAR (A2/R3-W1)
DG
17c.33 MAR-100
MAC 2 RESET (S) 139c.05
-12 CLAMP 139d.28

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OVERLAP MODE CONTROL

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FIG.31d



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OVERLAP MODE CONTROL
Filed Jan. 2, 1959 390 Sheets-Sheet 143

FIG. 32a INSTRUCTION COUNTER CONTROLS & 4,9, OF IC

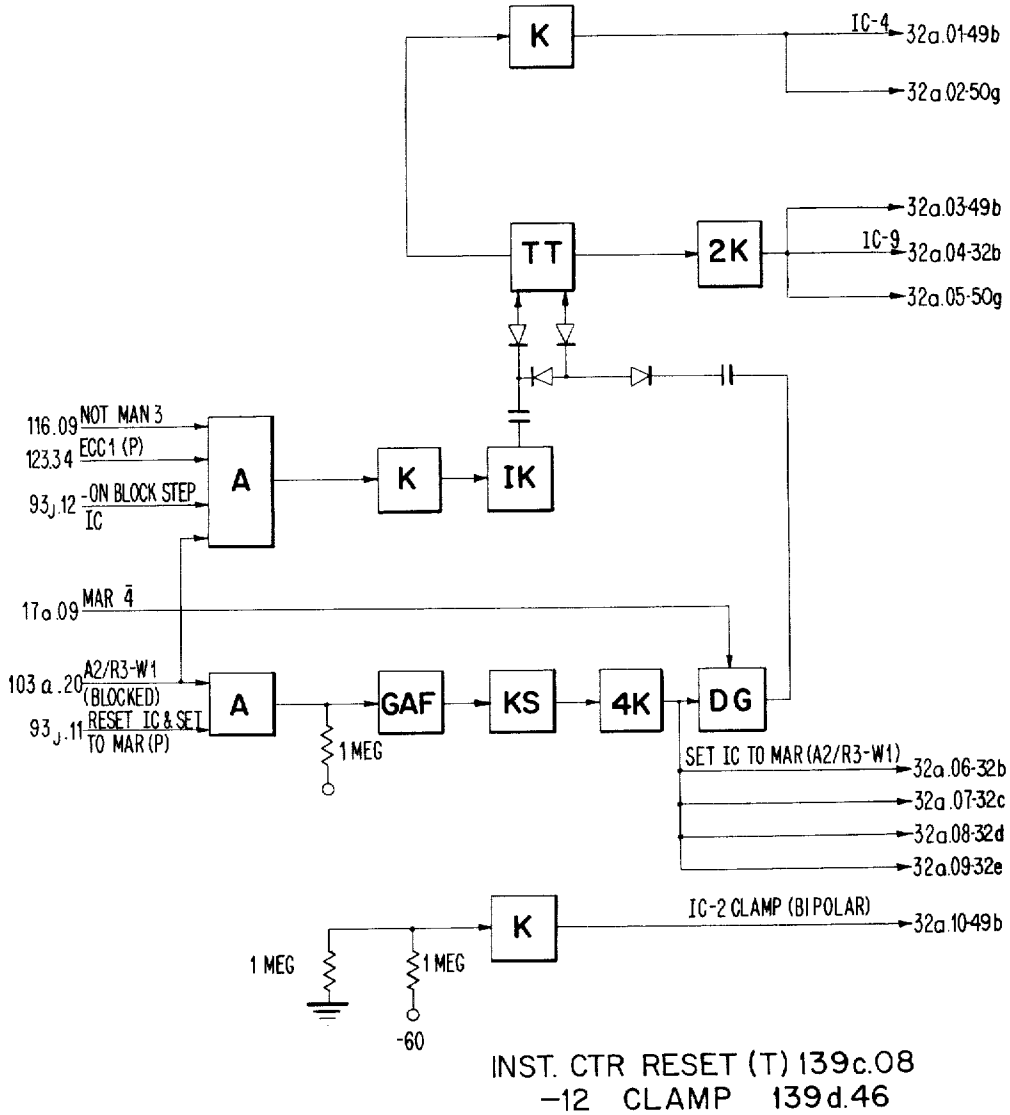


FIG. 32b

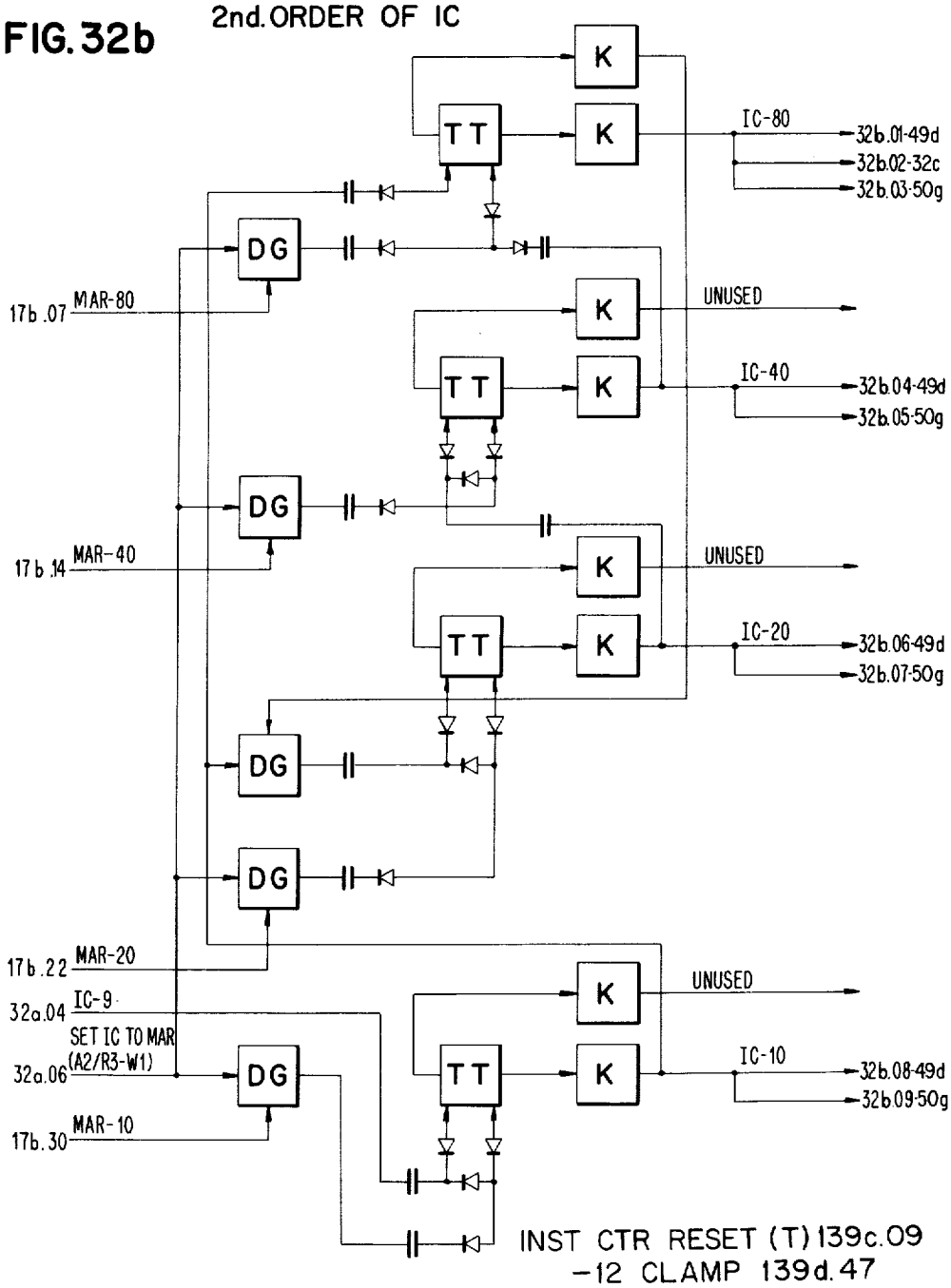
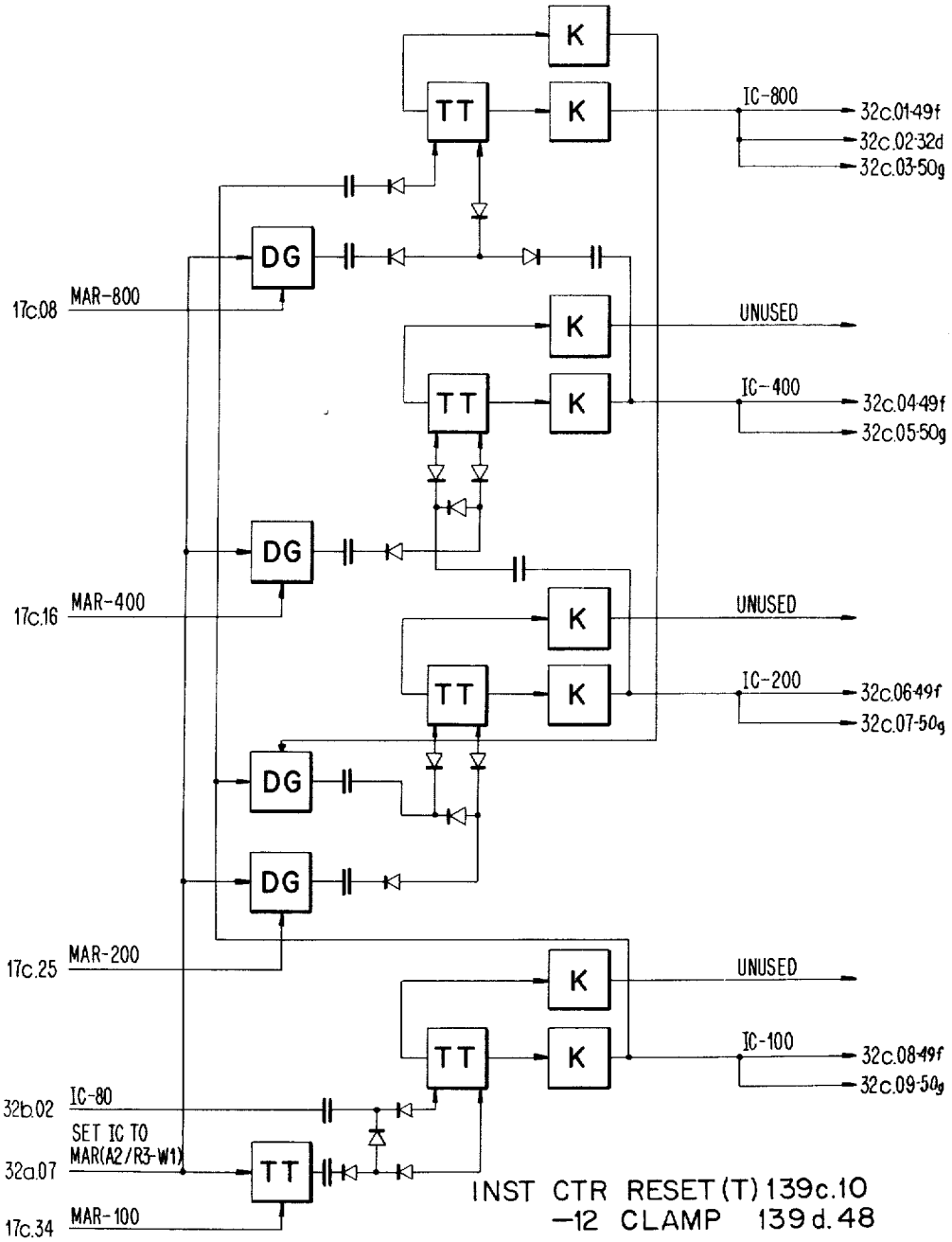

2nd. ORDER OF IC
K
TT
K
IC-80
32b.01-49d
32b.02-32c
32b.03-50g
DG
17b.07 MAR-80
K
UNUSED
TT
K
IC-40
32b.04-49d
32b.05-50g
DG
17b.14 MAR-40
K
UNUSED
TT
K
IC-20
32b.06-49d
32b.07-50g
DG
DG
17b.22 MAR-20
32a.04 IC-9
SET IC TO MAR (A2/R3-W1)
32a.06
K
UNUSED
TT
K
IC-10
32b.08-49d
32b.09-50g
DG
17b.30 MAR-10
INST CTR RESET (T) 139c.09
-12 CLAMP 139d.47

FIG.32c 3rd. ORDER OF IC



4th. ORDER OF IC

FIG. 32d

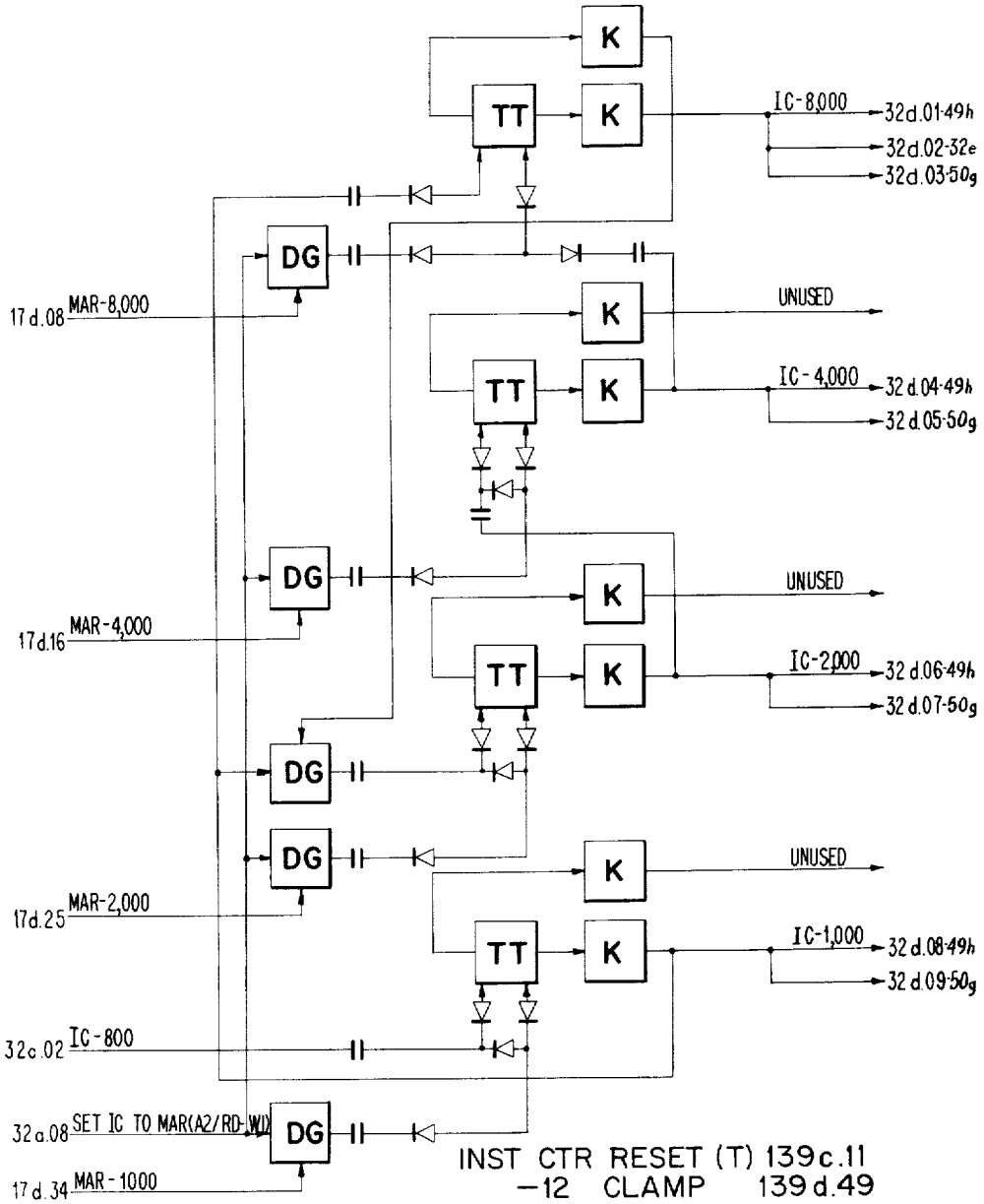


FIG. 32e

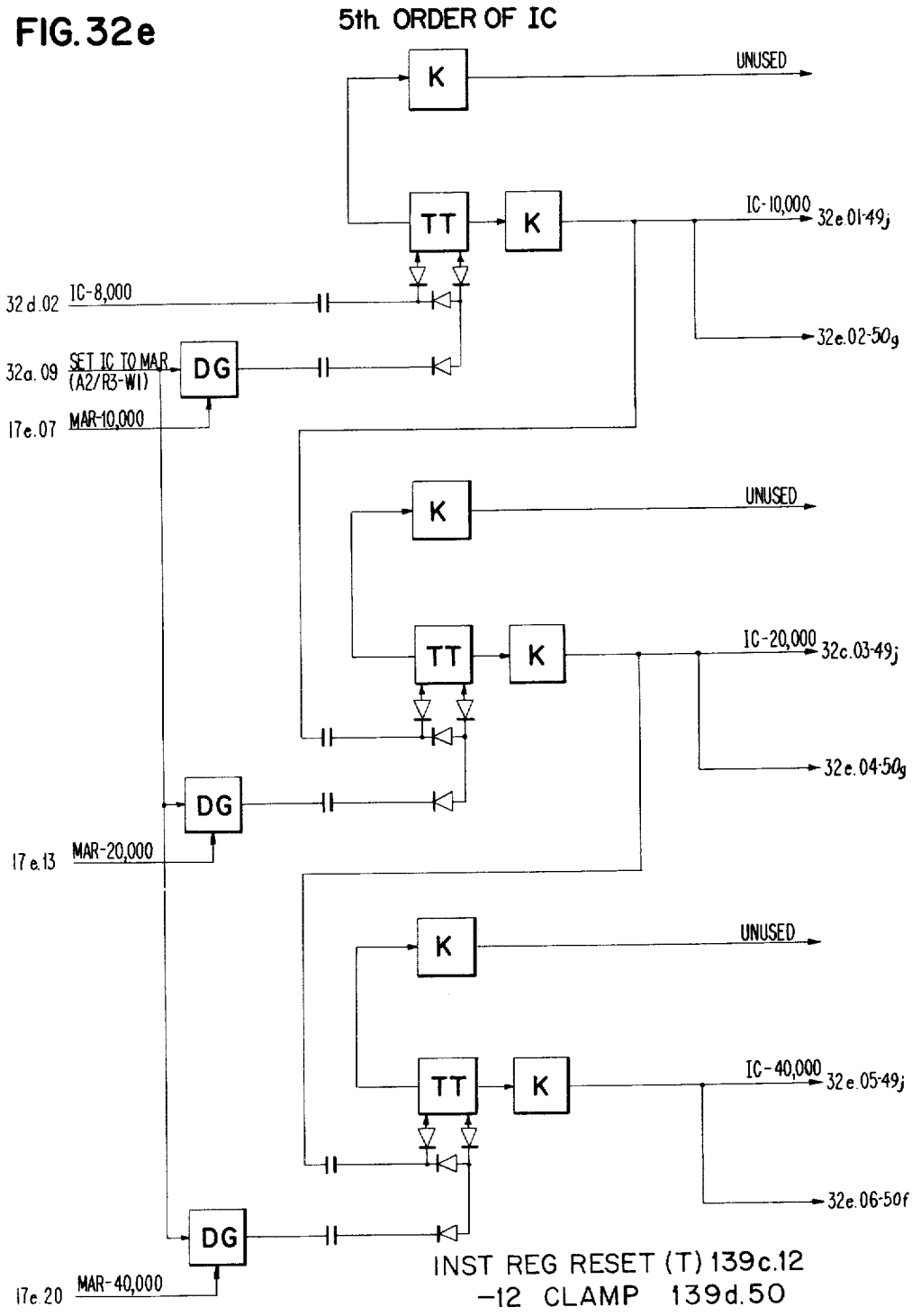

5th ORDER OF IC
K
UNUSED
TT
K
IC-10,000
32e.01-49j
32e.02-50g
32d.02 IC-8,000
32a.09 SET IC TO MAR (A2/R3-W1)
DG
17e.07 MAR-10,000
K
UNUSED
TT
K
IC-20,000
32c.03-49j
32e.04-50g
DG
17e.13 MAR-20,000
K
UNUSED
TT
K
IC-40,000
32e.05-49j
32e.06-50f
DG
17e.20 MAR-40,000
INST REG RESET (T) 139c.12
-12 CLAMP 139d.50

FIG.33a

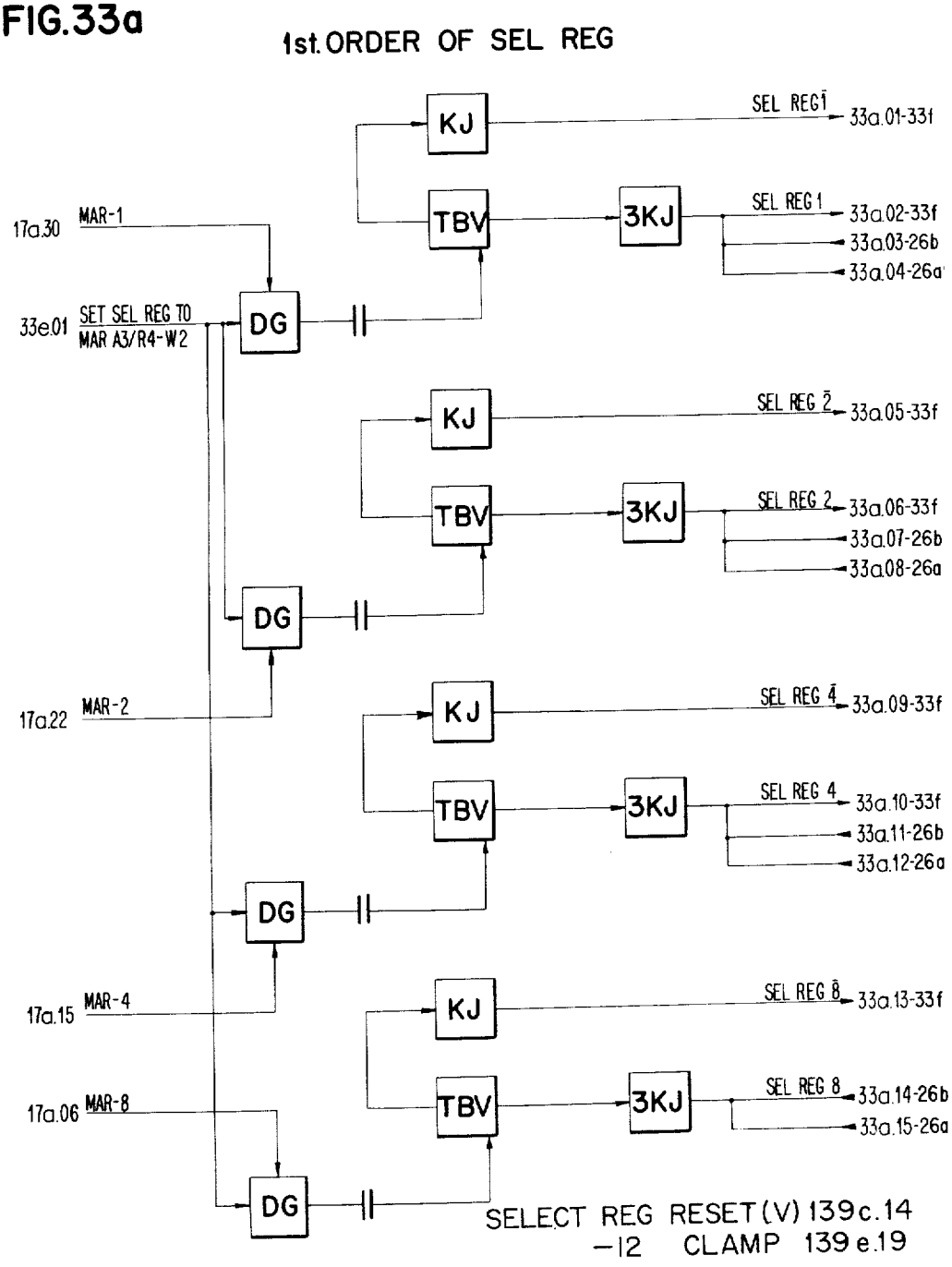

1st. ORDER OF SEL REG
KJ
TBV
3KJ
DG
SEL REG 1
SEL REG 2
SEL REG 4
SEL REG 8
33a.01-33f
33a.02-33f
33a.03-26b
33a.04-26a
33a.05-33f
33a.06-33f
33a.07-26b
33a.08-26a
33a.09-33f
33a.10-33f
33a.11-26b
33a.12-26a
33a.13-33f
33a.14-26b
33a.15-26a
17a.30 MAR-1
33e.01 SET SEL REG TO MAR A3/R4-W2
17a.22 MAR-2
17a.15 MAR-4
17a.06 MAR-8
SELECT REG RESET (V) 139c.14
-12 CLAMP 139e.19

FIG. 33b

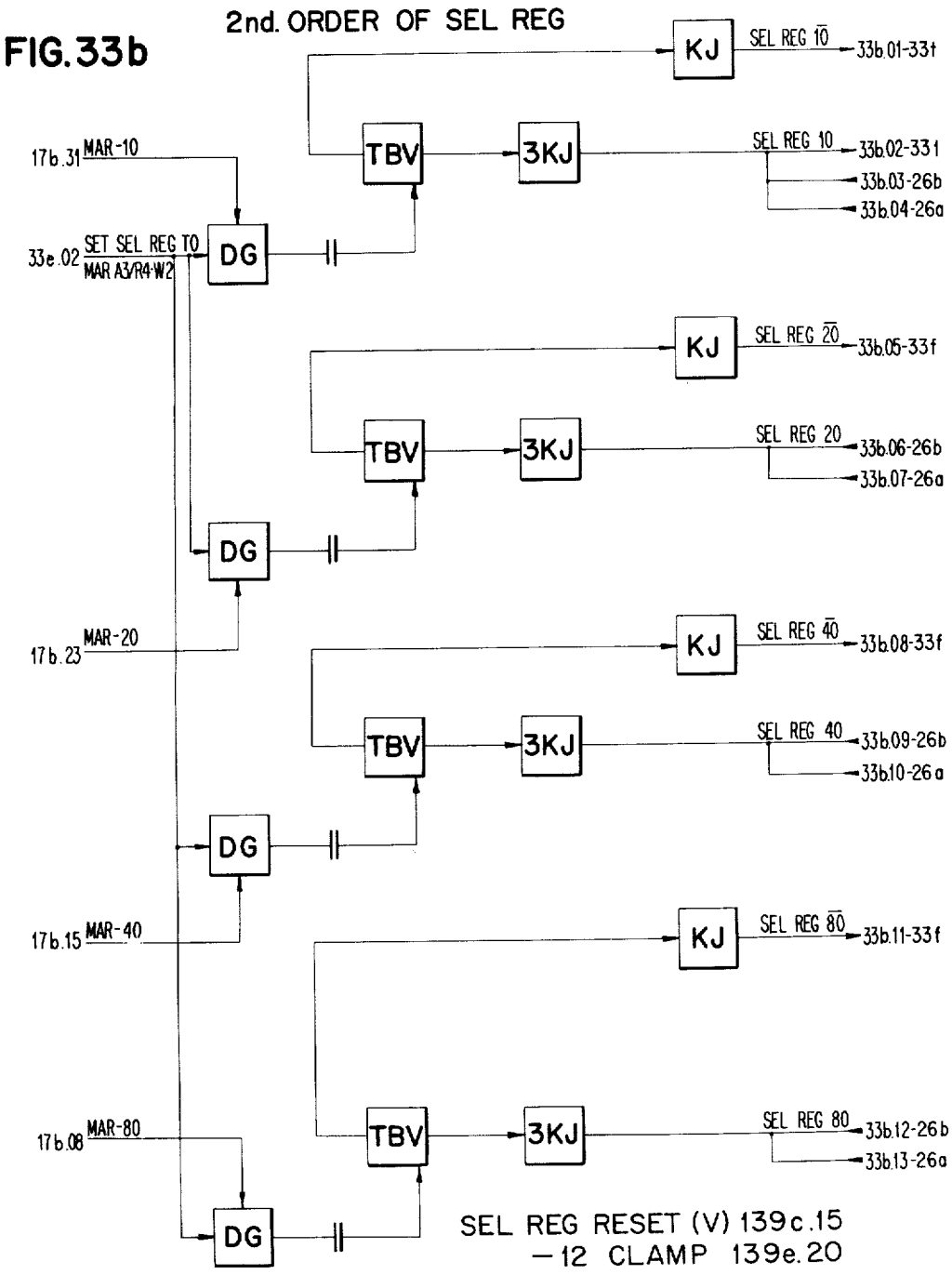
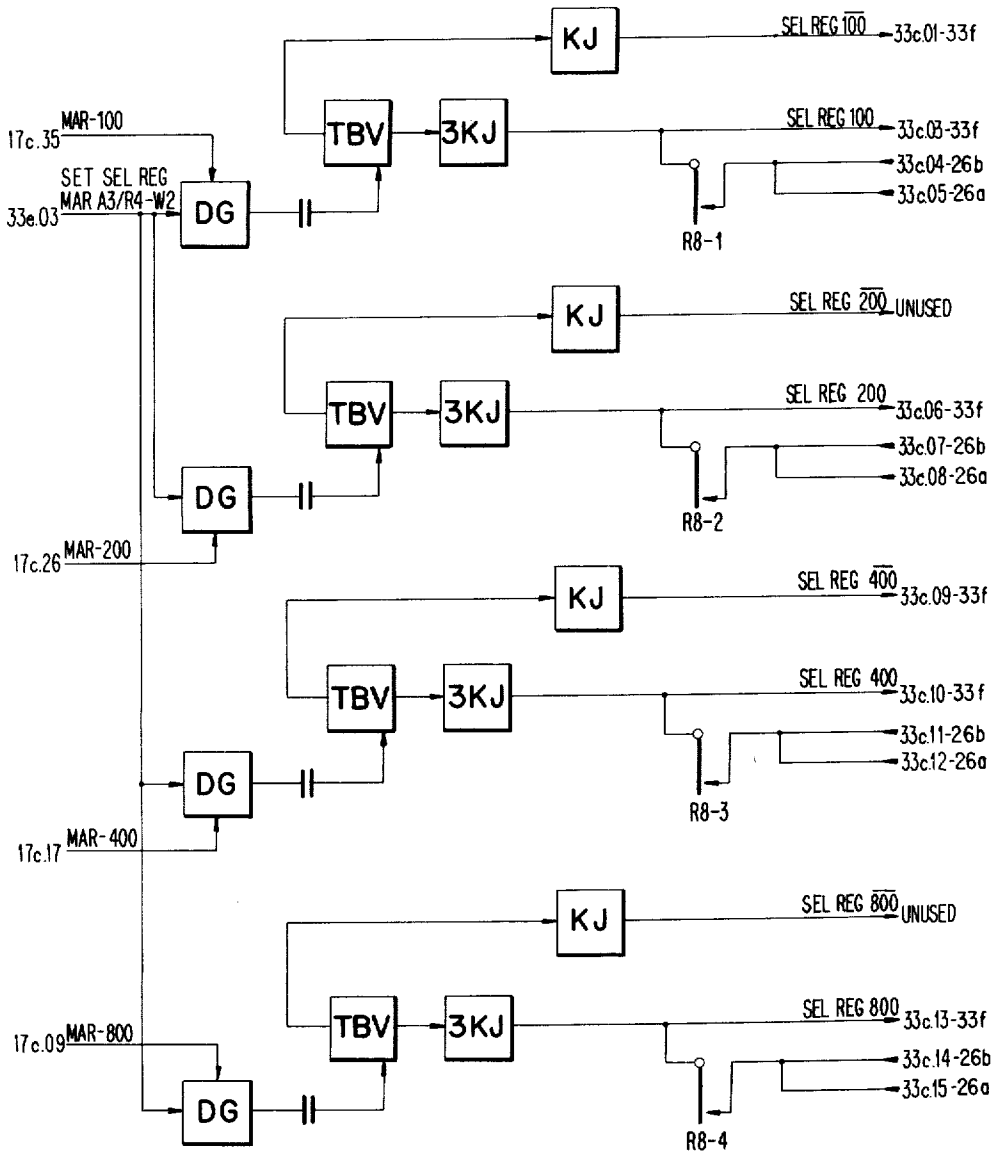

2nd. ORDER OF SEL REG
KJ
SEL REG 10
33b.01-33t
17b.31 MAR-10
TBV
3KJ
SEL REG 10
33b.02-33t
33b.03-26b
33b.04-26a
33e.02 SET SEL REG TO MAR A3/R4-W2
DG
KJ
SEL REG 20
33b.05-33f
TBV
3KJ
SEL REG 20
33b.06-26b
33b.07-26a
DG
17b.23 MAR-20
KJ
SEL REG 40
33b.08-33f
TBV
3KJ
SEL REG 40
33b.09-26b
33b.10-26a
DG
17b.15 MAR-40
KJ
SEL REG 80
33b.11-33f
17b.08 MAR-80
TBV
3KJ
SEL REG 80
33b.12-26b
33b.13-26a
DG
SEL REG RESET (V) 139c.15
-12 CLAMP 139e.20

FIG. 33c 3rd. ORDER OF SEL. REG.



SEL REG RESET (V) 139c.16
-12 CLAMP 139e.21

FIG. 33d 4th. ORDER OF SEL REG

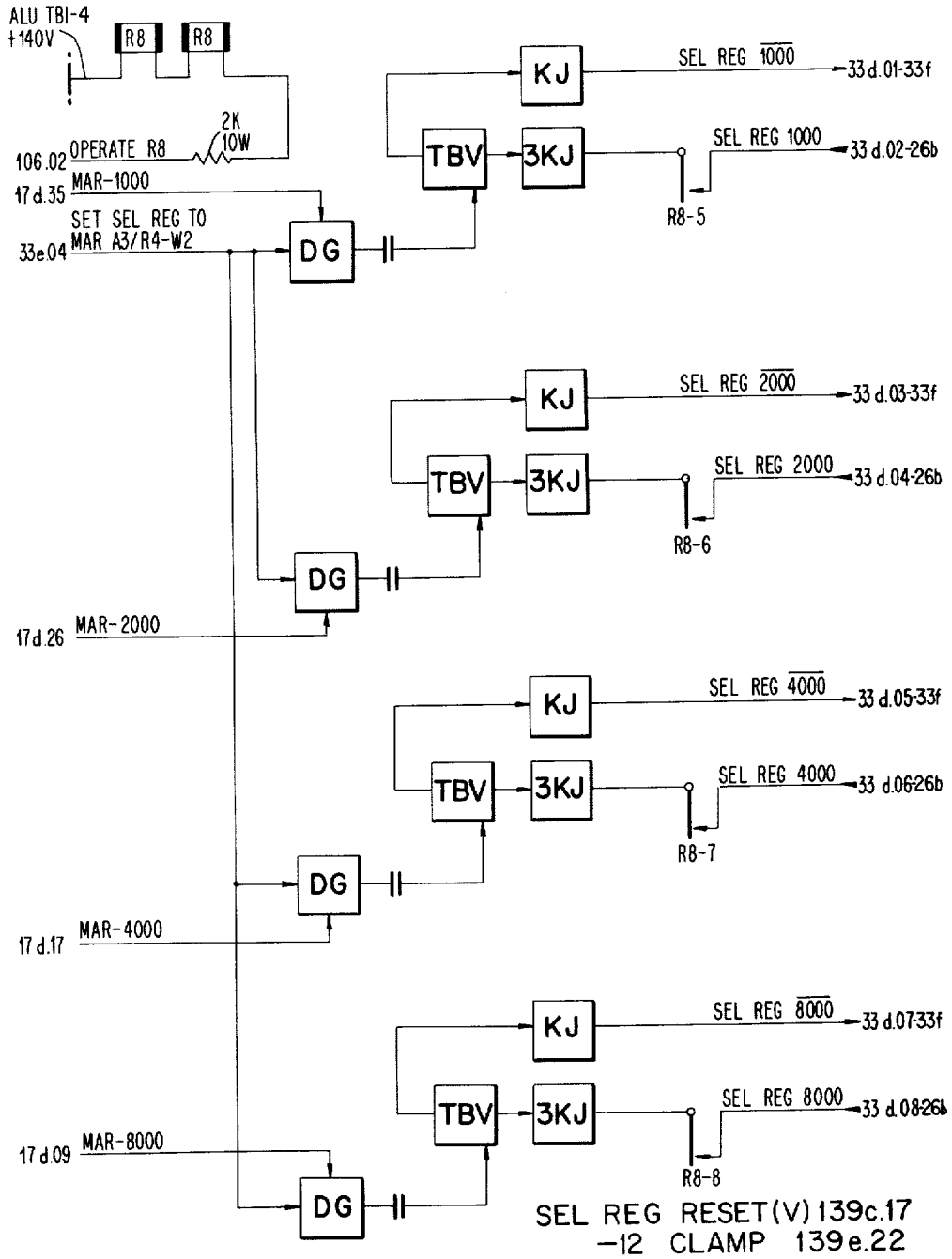


FIG. 33f

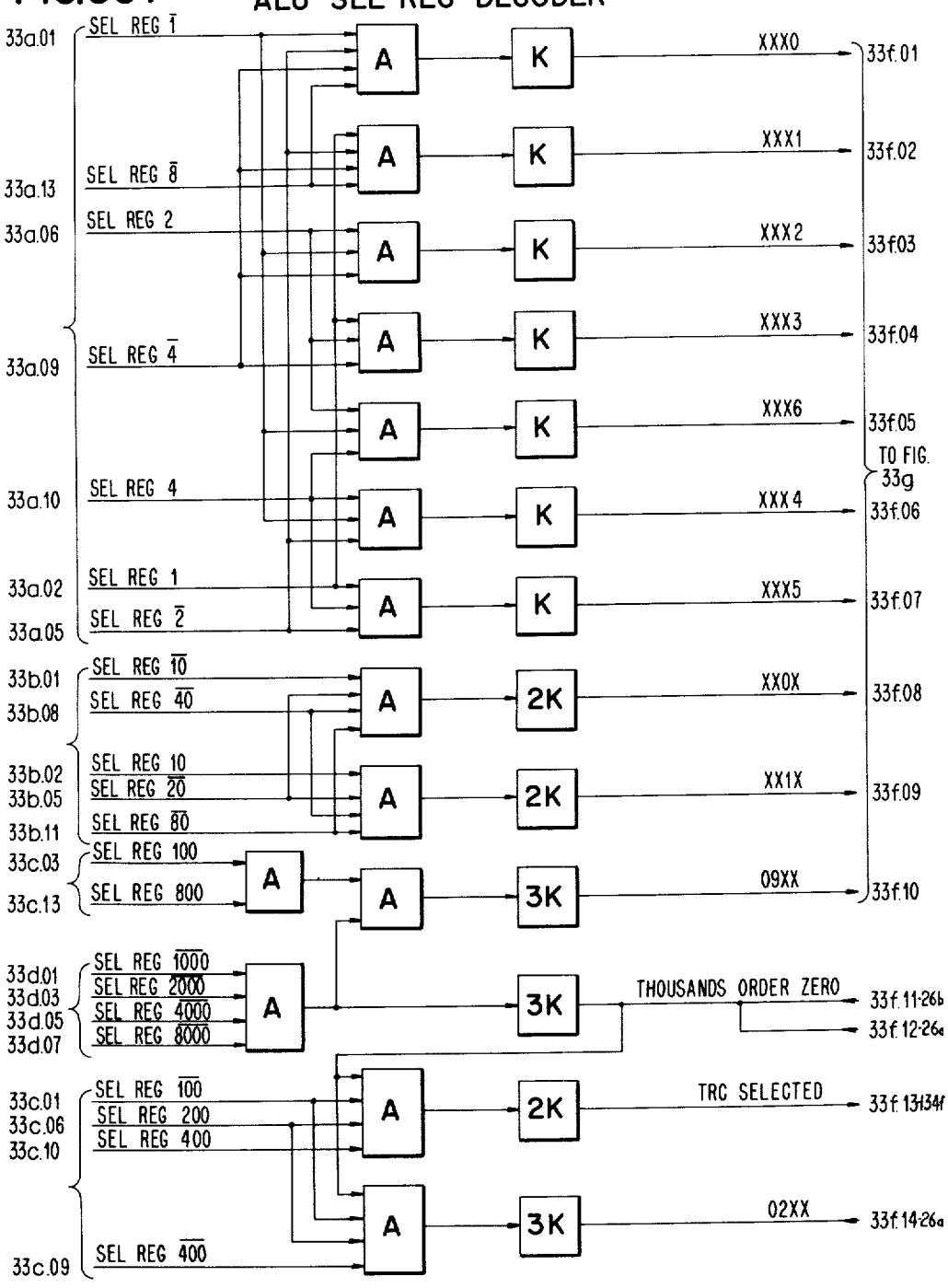

ALU SEL REG DECODER
33a.01
SEL REG 1
33a.13
SEL REG 8
33a.06
SEL REG 2
33a.09
SEL REG 4
33a.10
SEL REG 4
33a.02
SEL REG 1
33a.05
SEL REG 2
33b.01
SEL REG 10
33b.08
SEL REG 40
33b.02
SEL REG 10
33b.05
SEL REG 20
33b.11
SEL REG 80
33c.03
SEL REG 100
33c.13
SEL REG 800
33d.01
SEL REG 1000
33d.03
SEL REG 2000
33d.05
SEL REG 4000
33d.07
SEL REG 8000
33c.01
SEL REG 100
33c.06
SEL REG 200
33c.10
SEL REG 400
33c.09
SEL REG 400
A
K
2K
3K
XXX0
XXX1
XXX2
XXX3
XXX6
XXX4
XXX5
XXOX
XX1X
09XX
THOUSANDS ORDER ZERO
TRC SELECTED
02XX
33f.01
33f.02
33f.03
33f.04
33f.05
TO FIG. 33g
33f.06
33f.07
33f.08
33f.09
33f.10
33f.11-26b
33f.12-26a
33f.13-13f
33f.14-26a

FIG. 33g

ALU SEL. REG. DECODER

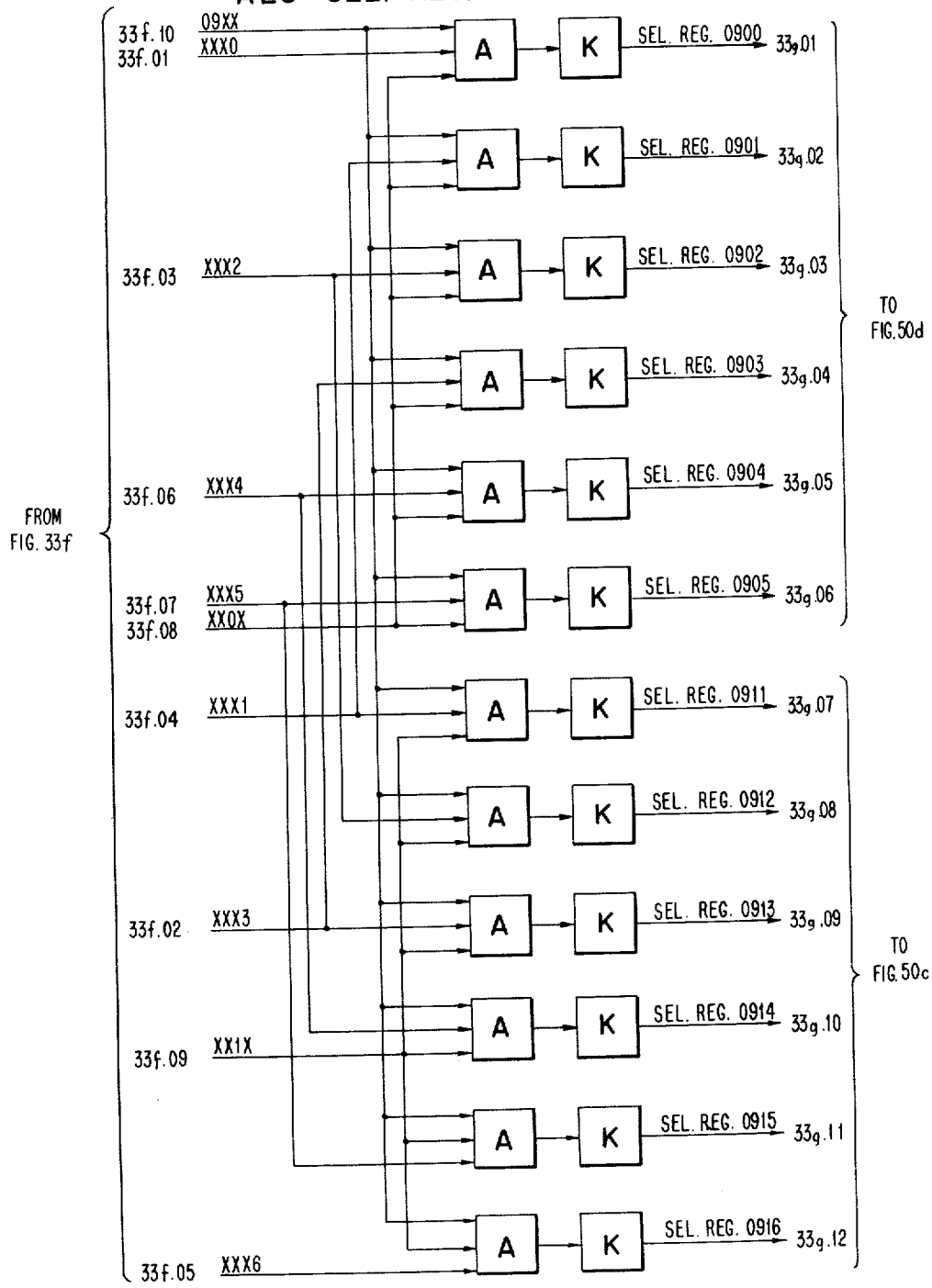


FIG.34a STORAGE 2X4 DECODER 128,256

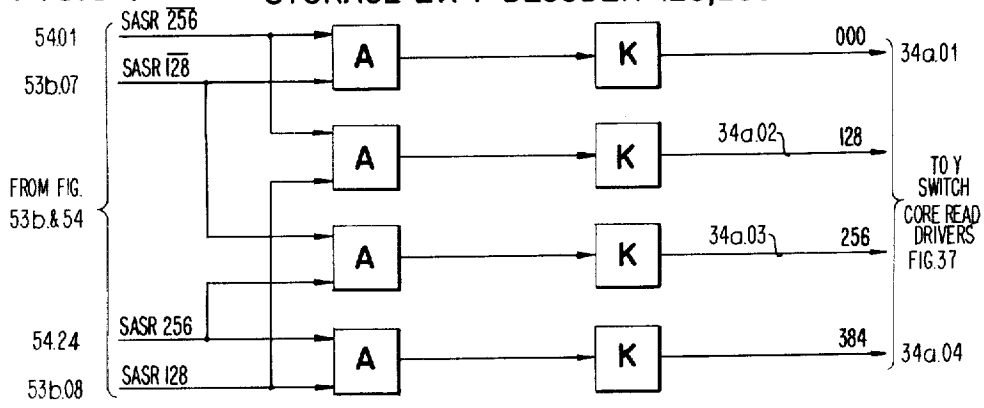


FIG. 34b STORAGE 2X4 DECODER 32,64

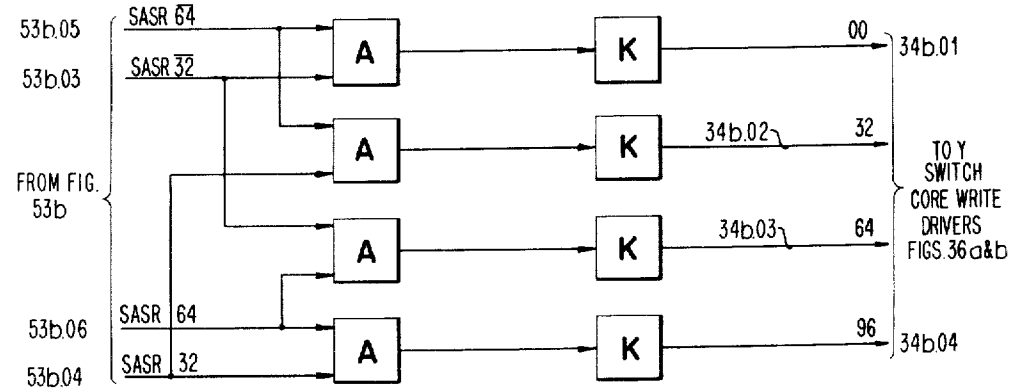


FIG. 34c STORAGE 2X4 DECODER 8,16

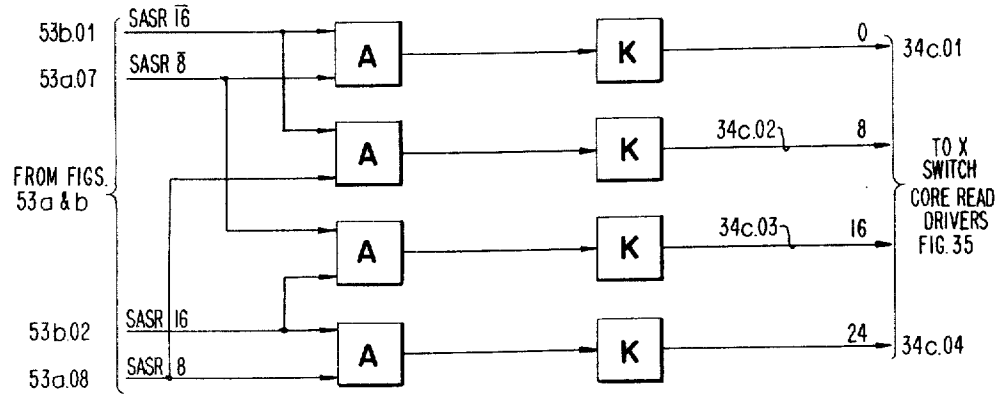


FIG. 34d

STORAGE 3X8 DECODER

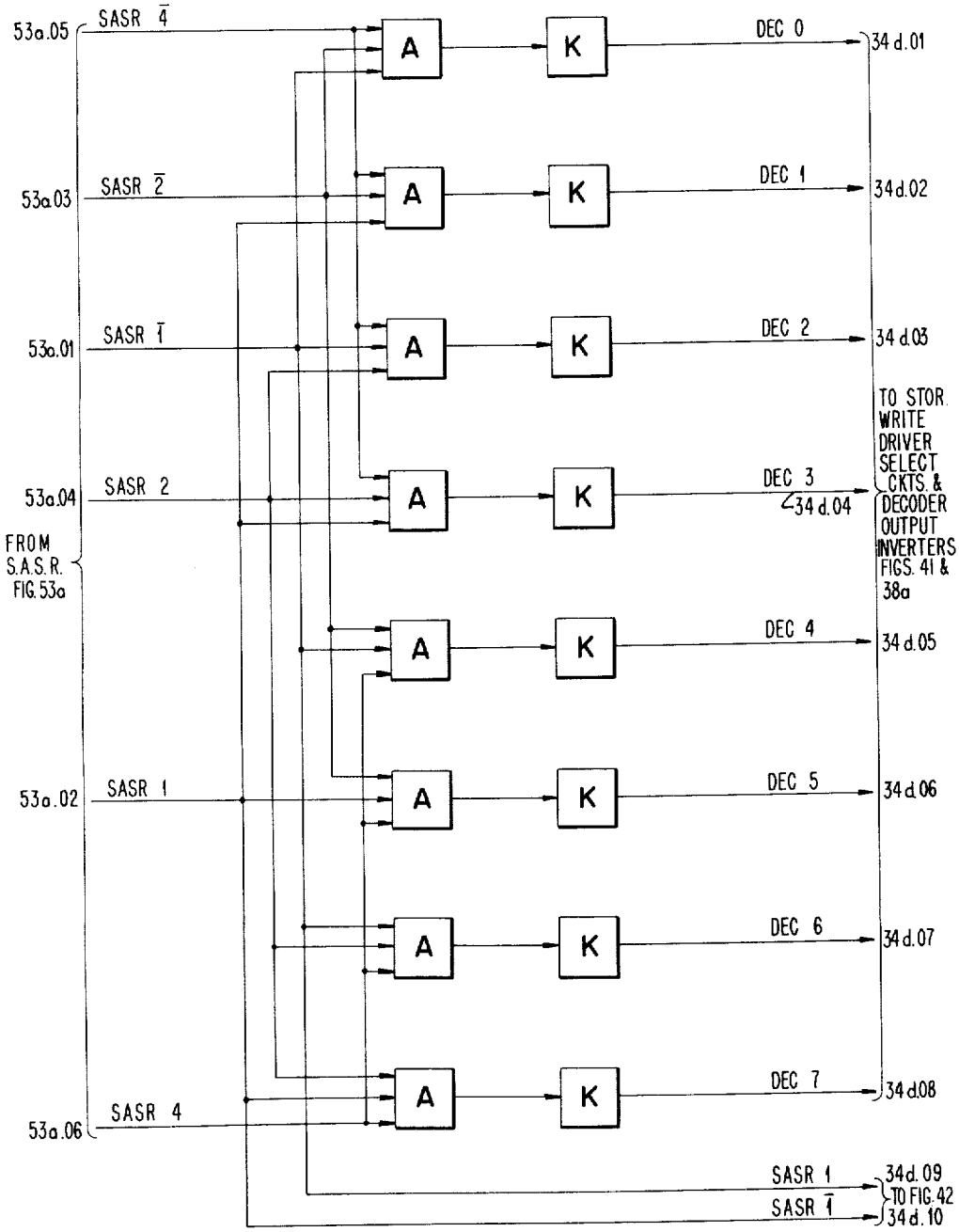


FIG.35

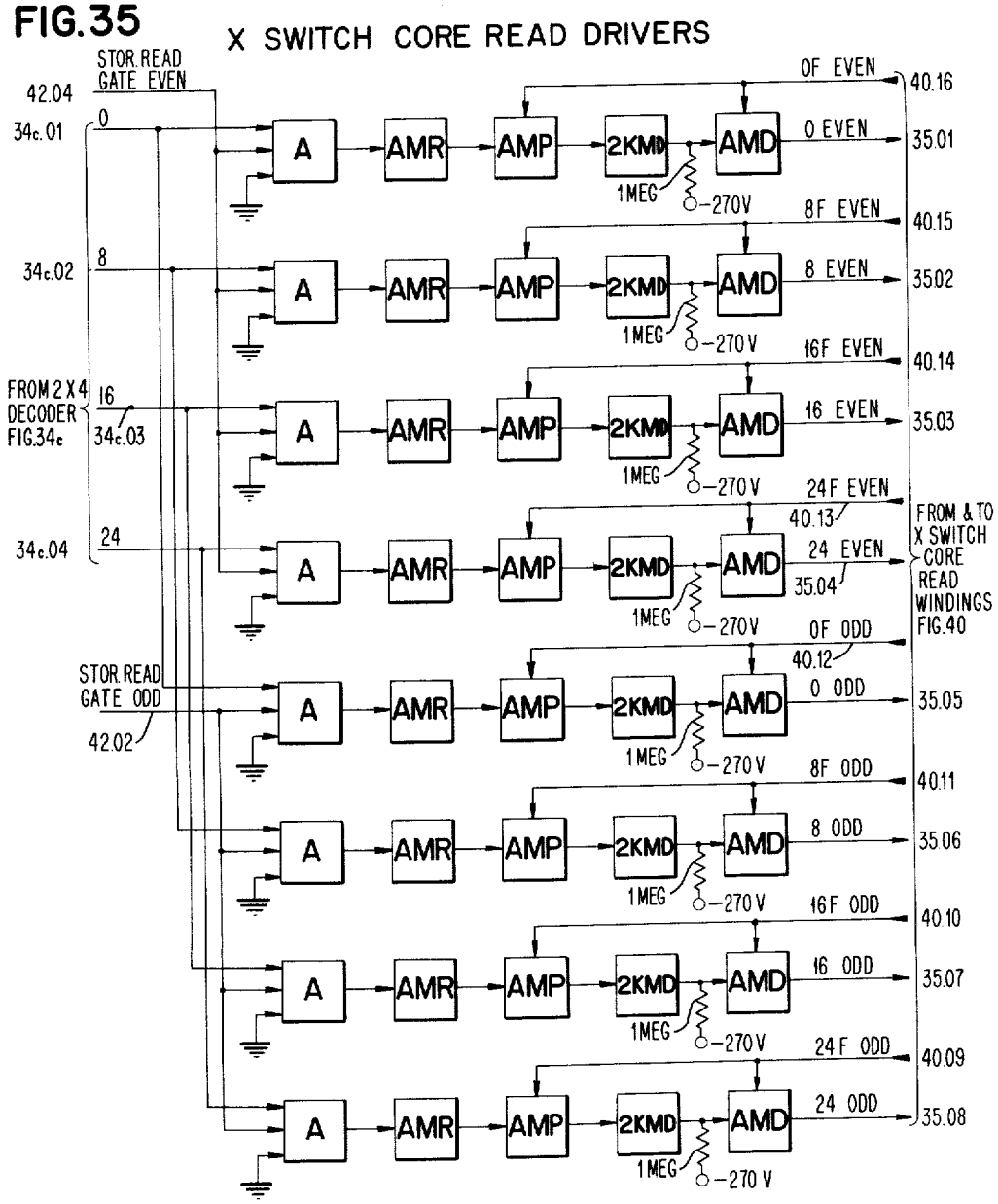
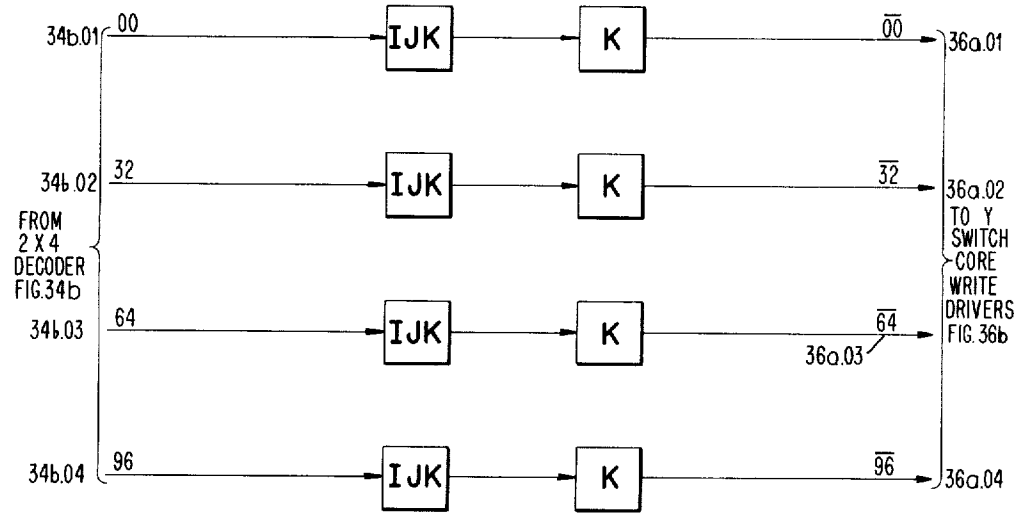

X SWITCH CORE READ DRIVERS
STOR. READ GATE EVEN
42.04
34c.01
0
34c.02
8
FROM 2 X 4 DECODER FIG.34c
16
34c.03
34c.04
24
STOR. READ GATE ODD
42.02
A
AMR
AMP
2KMD
AMD
1MEG
-270V
0F EVEN
40.16
0 EVEN
35.01
8F EVEN
40.15
8 EVEN
35.02
16F EVEN
40.14
16 EVEN
35.03
24F EVEN
40.13
24 EVEN
35.04
FROM & TO X SWITCH CORE READ WINDINGS FIG.40
0F ODD
40.12
0 ODD
35.05
8F ODD
40.11
8 ODD
35.06
16F ODD
40.10
16 ODD
35.07
24F ODD
40.09
24 ODD
35.08

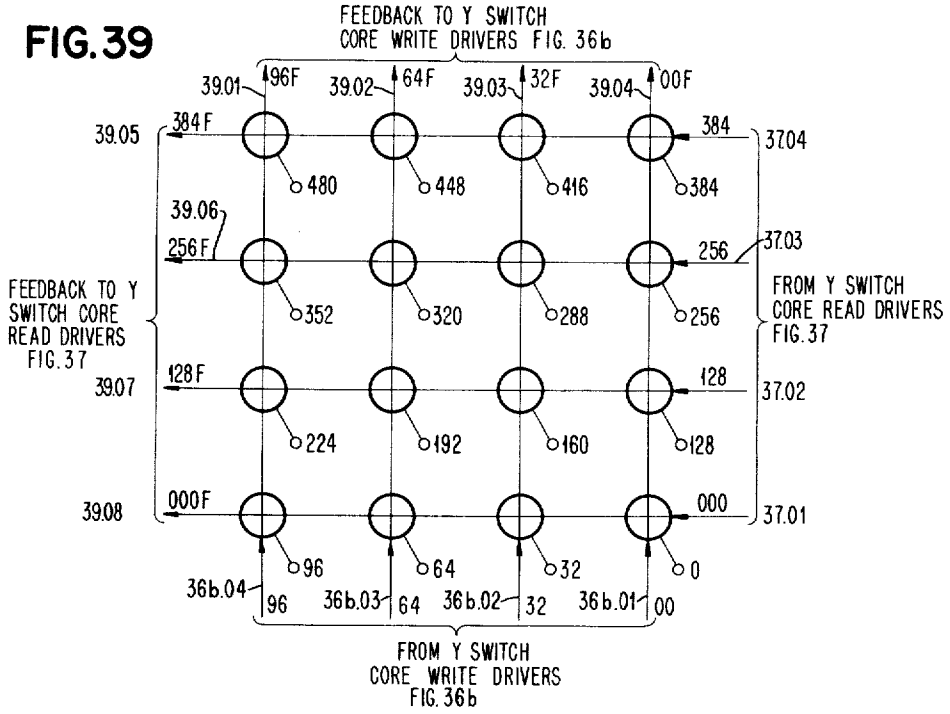
FIG. 36a

2 X 4 DECODER OUTPUT INVERTERS



"Y" SWITCH CORE MATRIX

FIG. 39



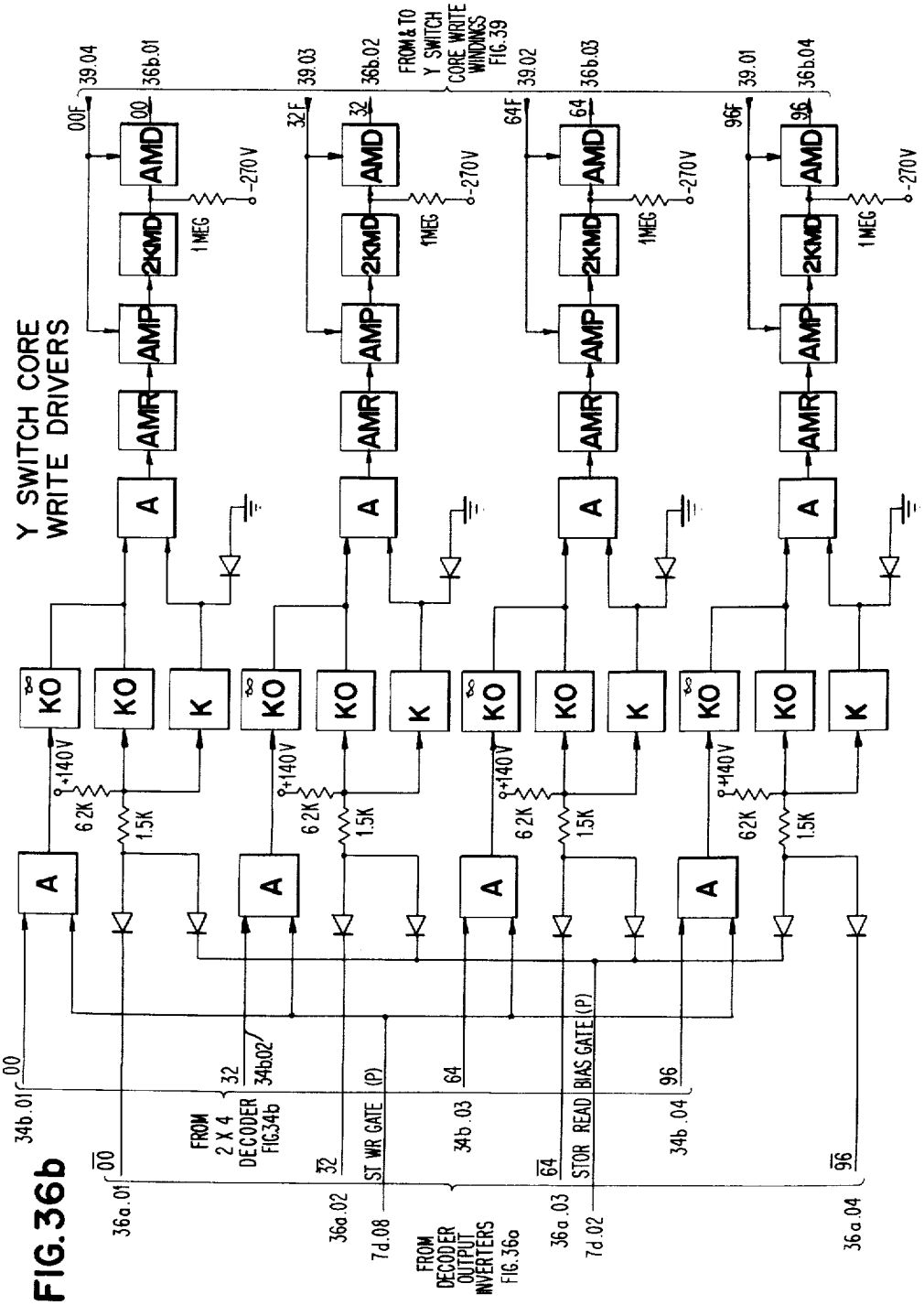

Y SWITCH CORE WRITE DRIVERS
FROM & TO Y SWITCH CORE WRITE WINDINGS FIG. 39
39.04
39.03
39.02
39.01
36b.01
36b.02
36b.03
36b.04
00F
32F
64F
96F
AMD
2KMD
AMP
AMR
A
KO
K
-270 V
1 MEG
+140 V
6.2K
1.5K
34b.01
34b.02
34b.03
34b.04
FROM 2 X 4 DECODER FIG. 34b
ST WR GATE (P)
STOR READ BIAS GATE (P)
36a.01
36a.02
36a.03
36a.04
7d.08
7d.02
FROM DECODER OUTPUT INVERTERS FIG. 36a

FIG. 36b

FIG. 37

Y SWITCH CORE READ DRIVERS

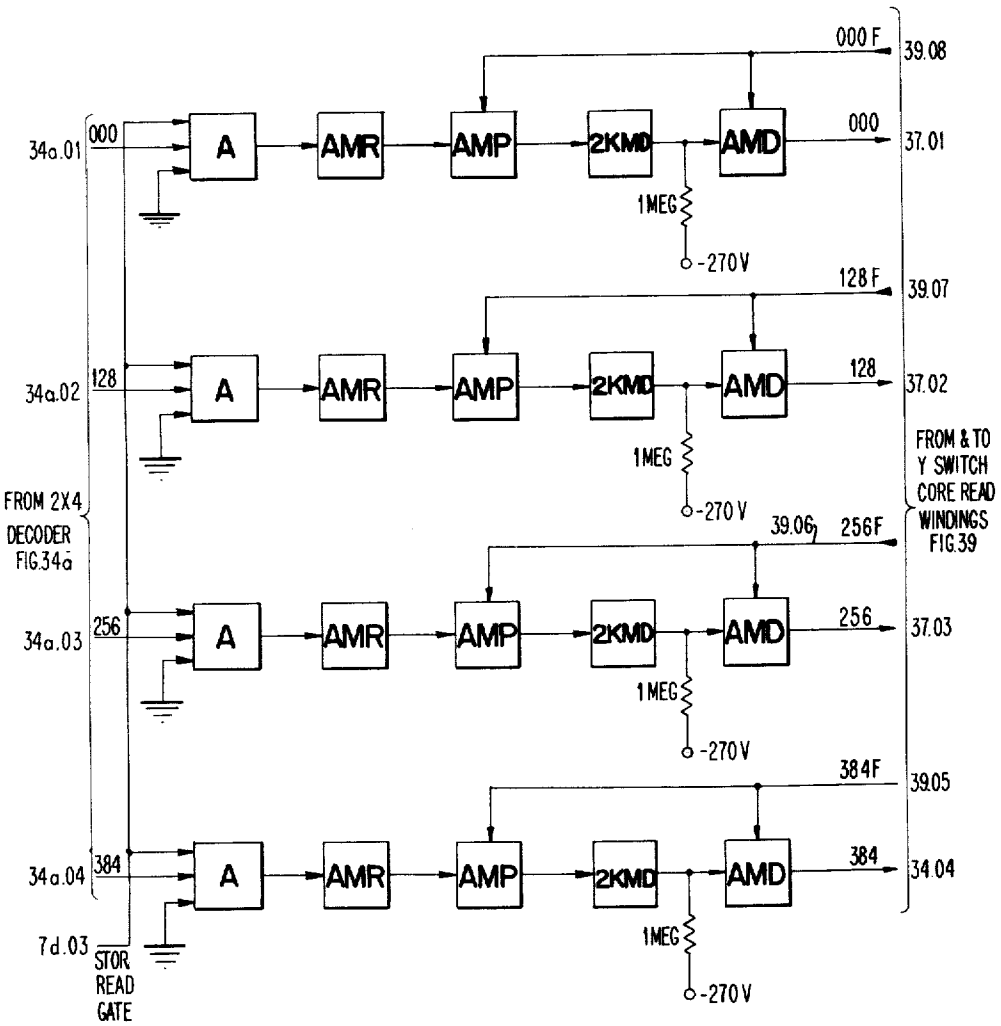
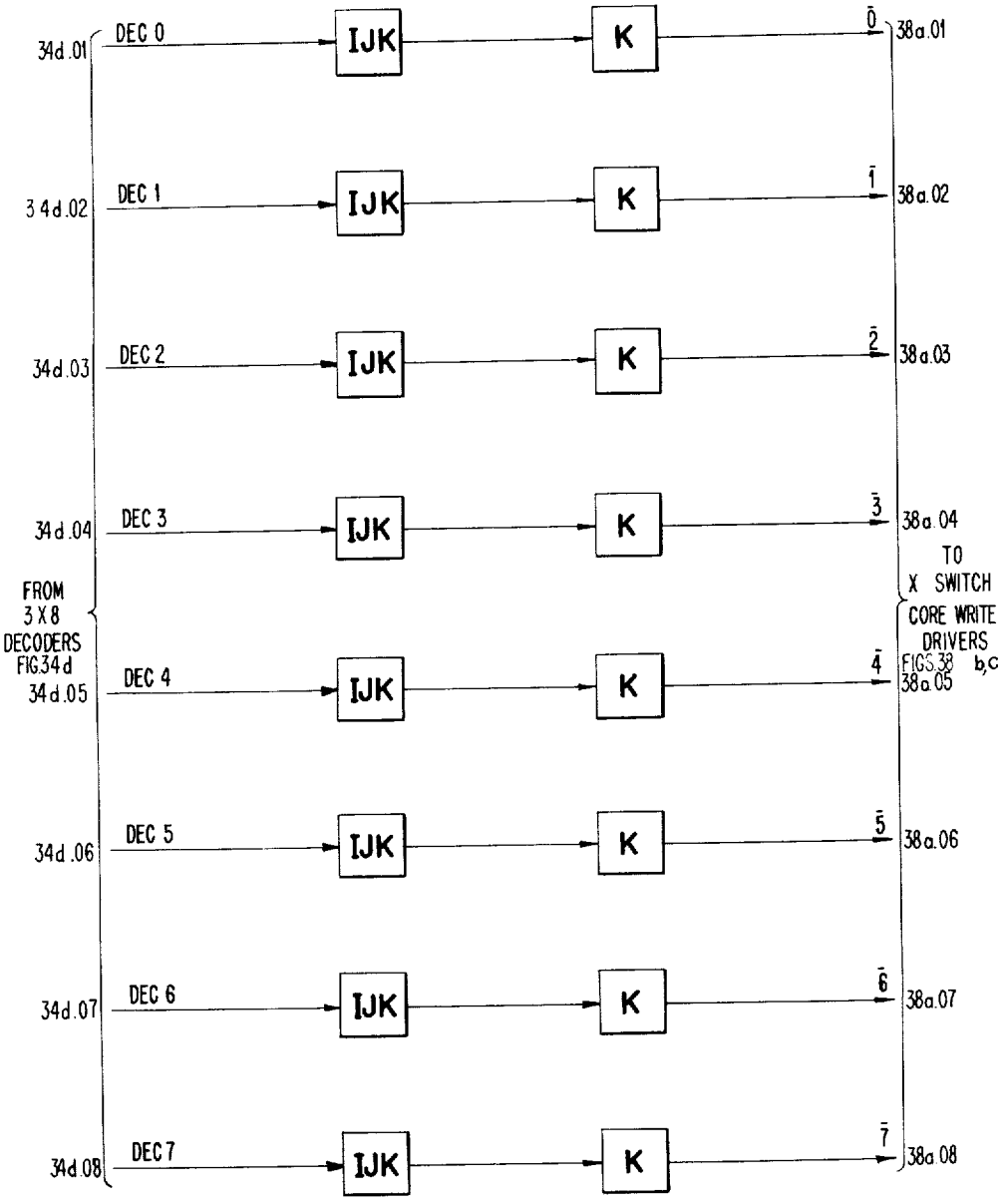
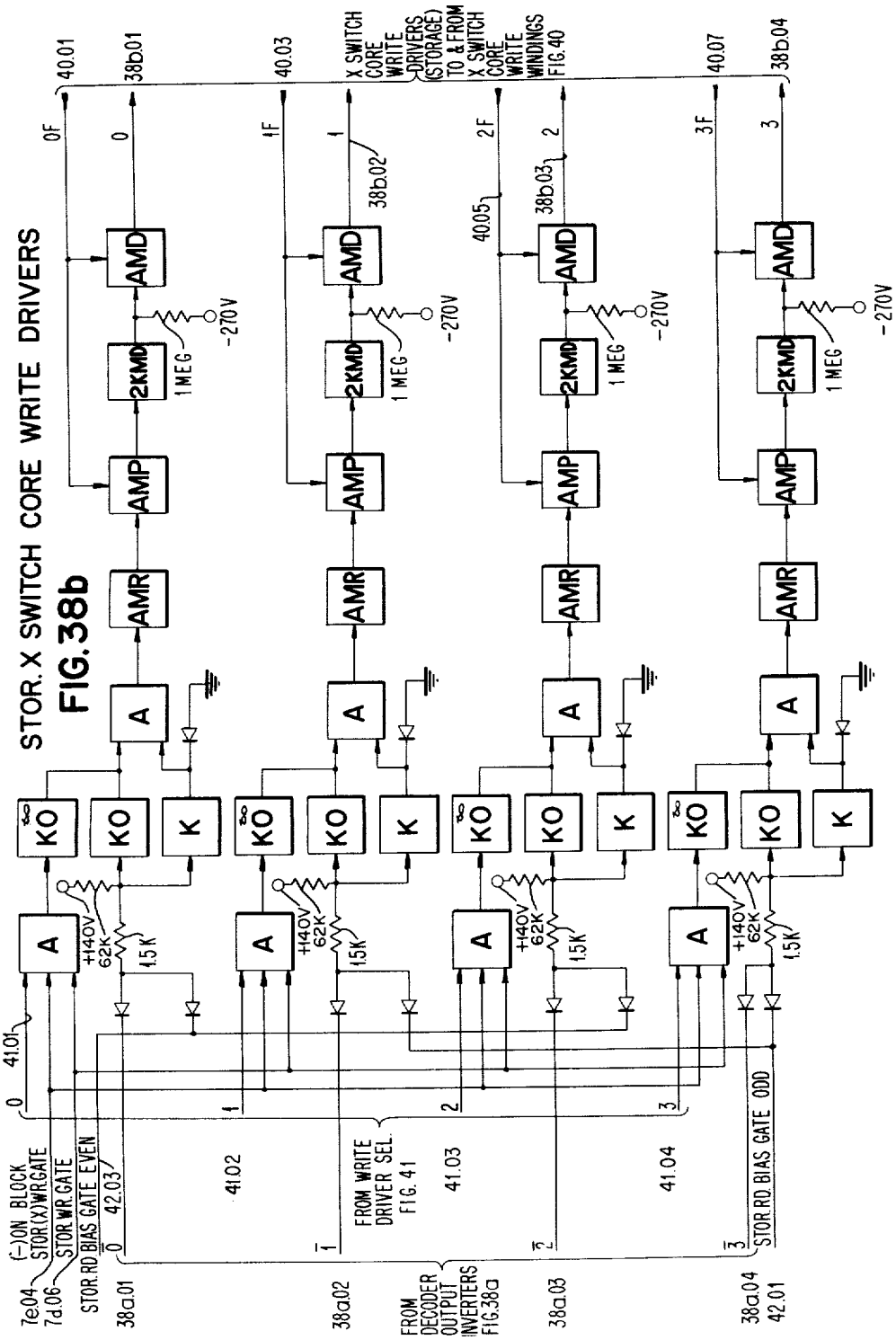


FIG. 38a

3 X 8 DECODER OUTPUT INVERTERS




STOR. X SWITCH CORE WRITE DRIVERS
FIG. 38b
40.01
38b.01
40.03
38b.02
40.05
38b.03
40.07
38b.04
X SWITCH CORE WRITE DRIVERS (STORAGE) TO & FROM X SWITCH CORE WRITE WINDINGS FIG. 40
0F
1F
2F
3F
AMD
2KMD
AMP
AMR
A
KO
K
1 MEG
-270V
+140V
62K
1.5K
41.01
41.02
41.03
41.04
FROM WRITE DRIVER SEL. FIG. 41
(-)ON BLOCK STOR(X)WR.GATE
STOR.WR.GATE
STOR.RD BIAS GATE EVEN
STOR.RD BIAS GATE ODD
42.03
7e.04
7d.06
38a.01
38a.02
38a.03
38a.04
42.01
FROM DECODER OUTPUT INVERTERS FIG. 38a

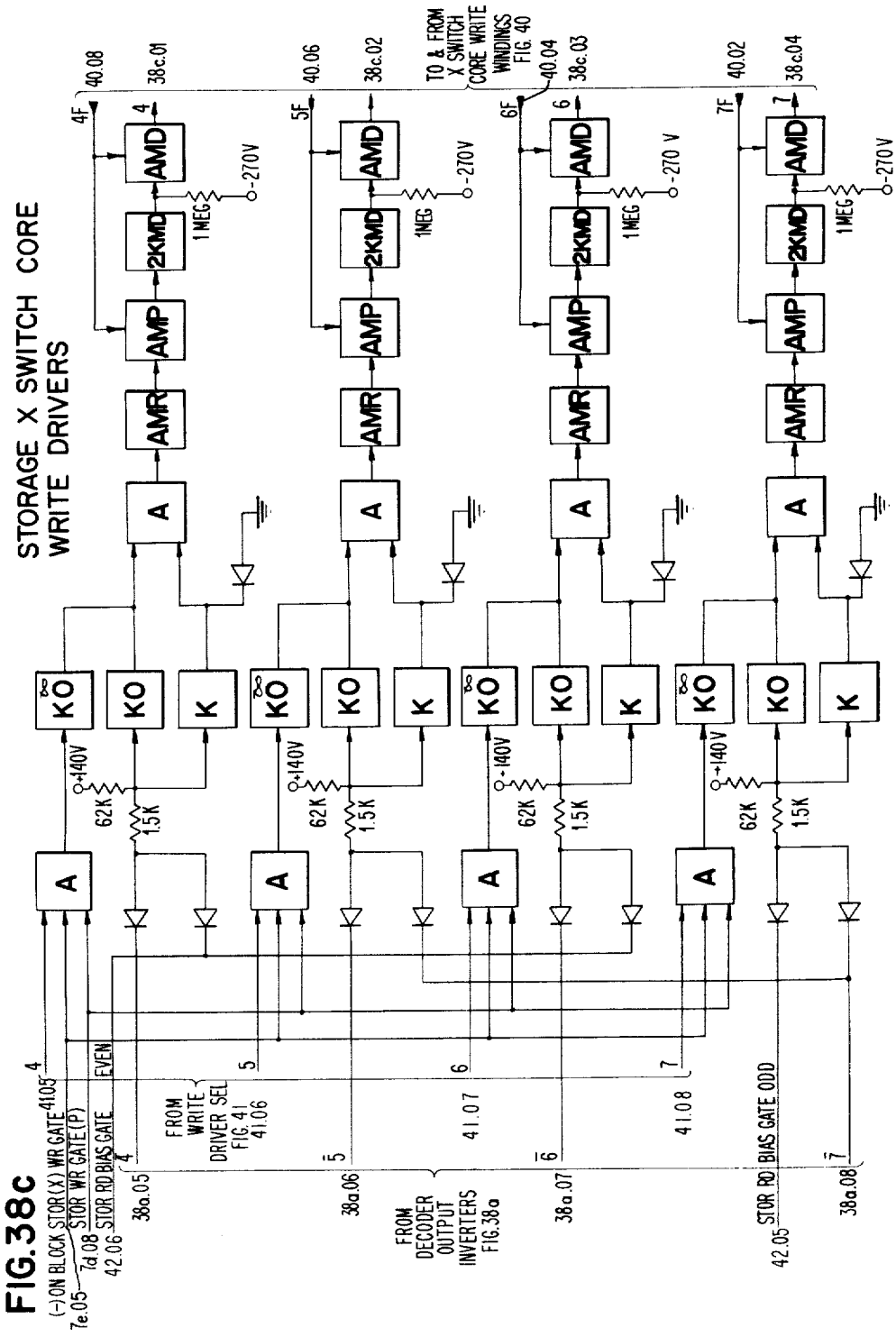

STORAGE X SWITCH CORE WRITE DRIVERS
TO & FROM X SWITCH CORE WRITE WINDINGS FIG. 40
AMD
2KMD
AMP
AMR
A
KO
K
+140V
62K
1.5K
1MEG
-270V
FROM WRITE DRIVER SEL FIG. 41
FROM DECODER OUTPUT INVERTERS FIG. 38a
(-) ON BLOCK STOR (X) WR GATE
STOR WR GATE (P)
STOR RD BIAS GATE
EVEN
ODD

FIG. 38c

FIG.40 "X" SWITCH CORE MATRIX 4 X 8 DIAGRAM

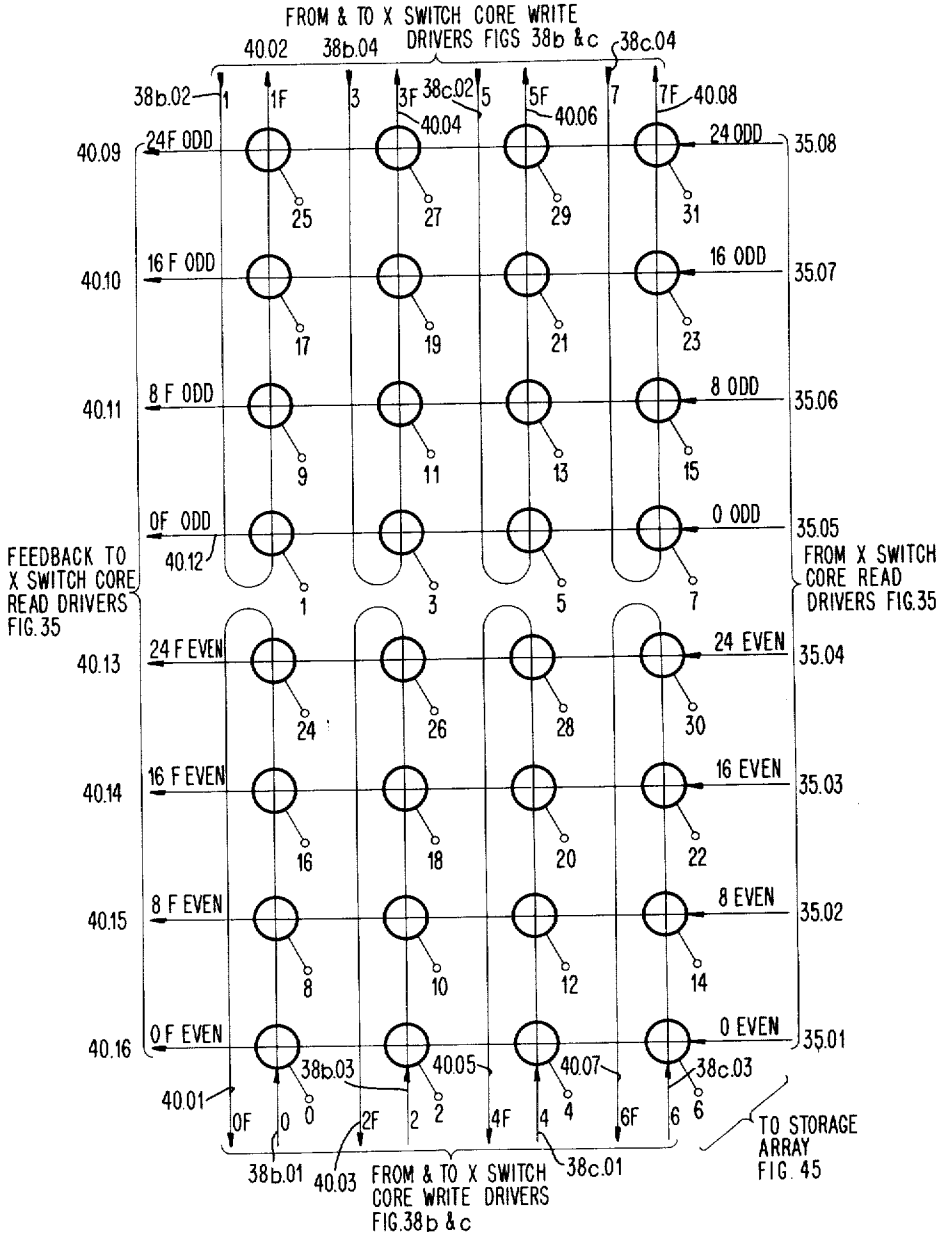


FIG. 41 STORAGE WRITE DRIVER SELECT CIRCUIT

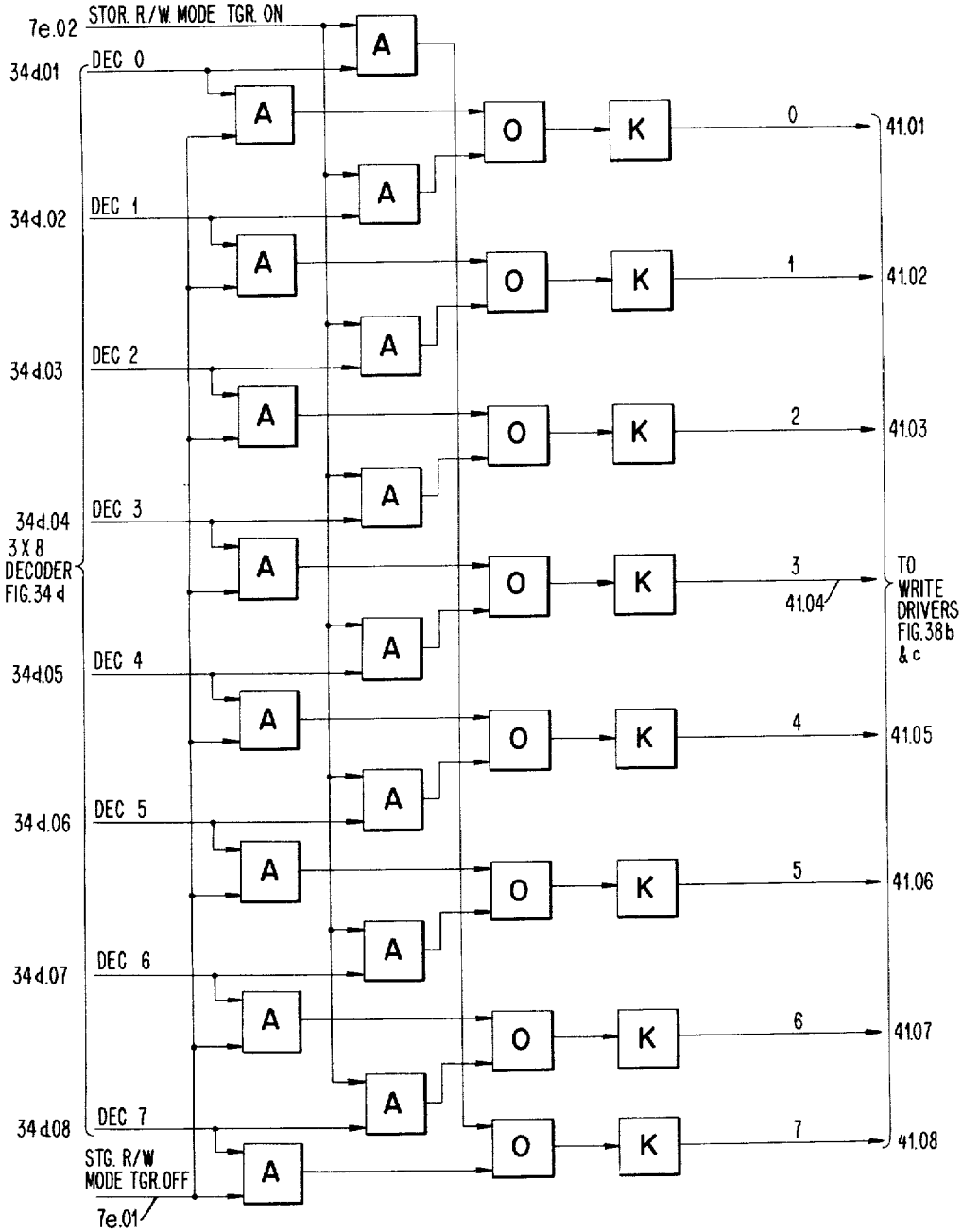


FIG. 42
ODD-EVEN GATING CIRCUIT

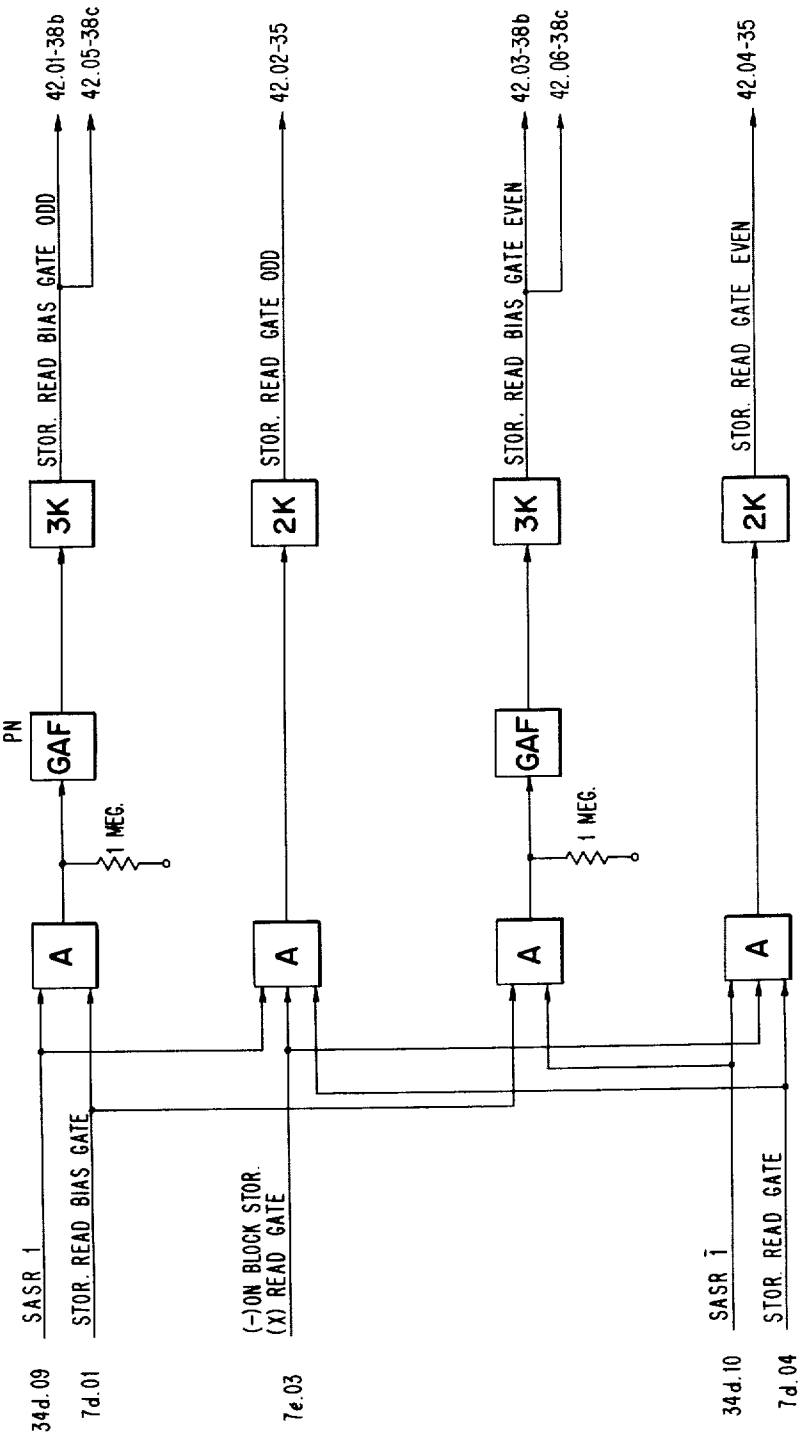


FIG.43 STORAGE INPUT SELECT & SWITCH CKTS.

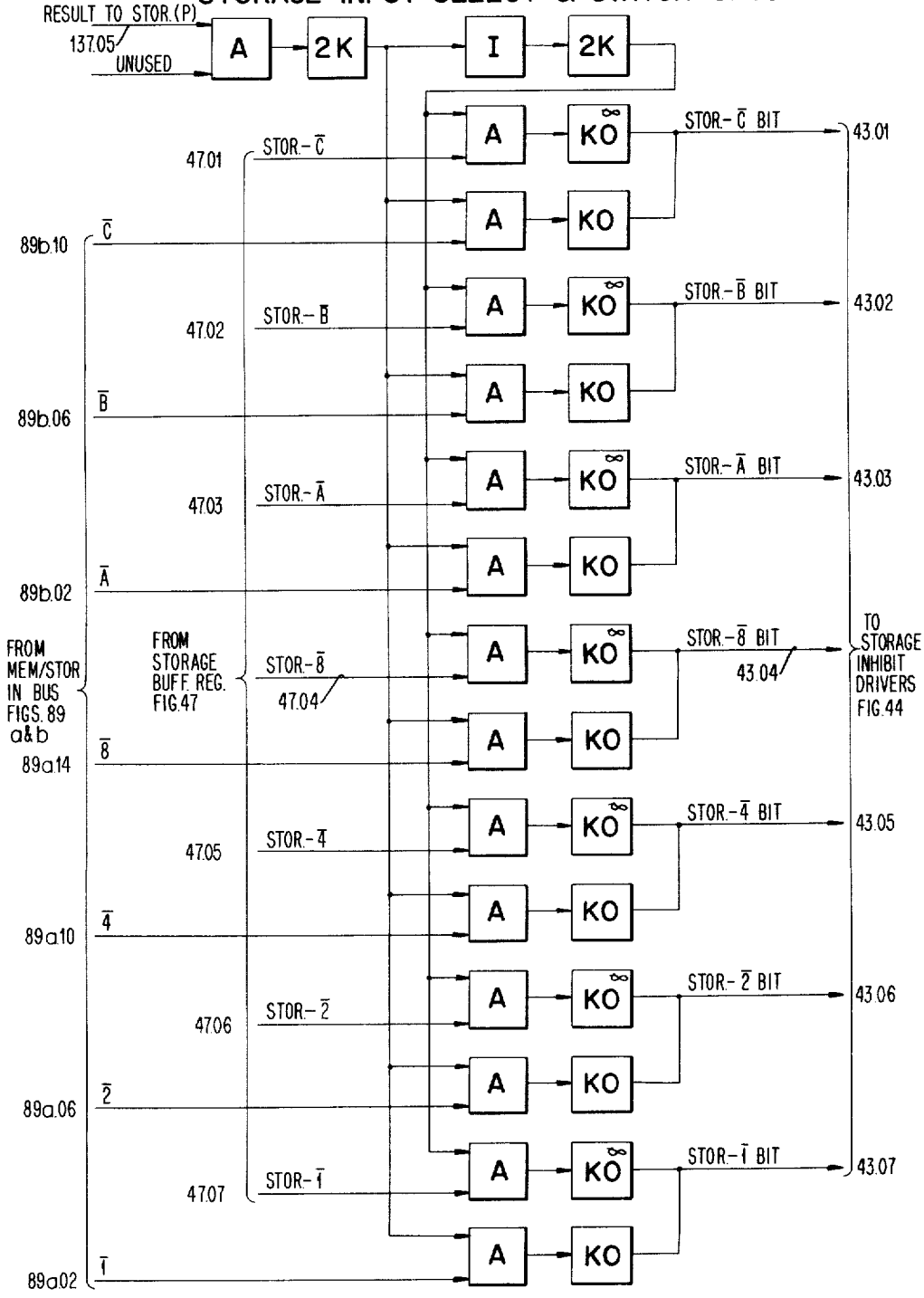


FIG. 44 STORAGE INHIBIT DRIVERS

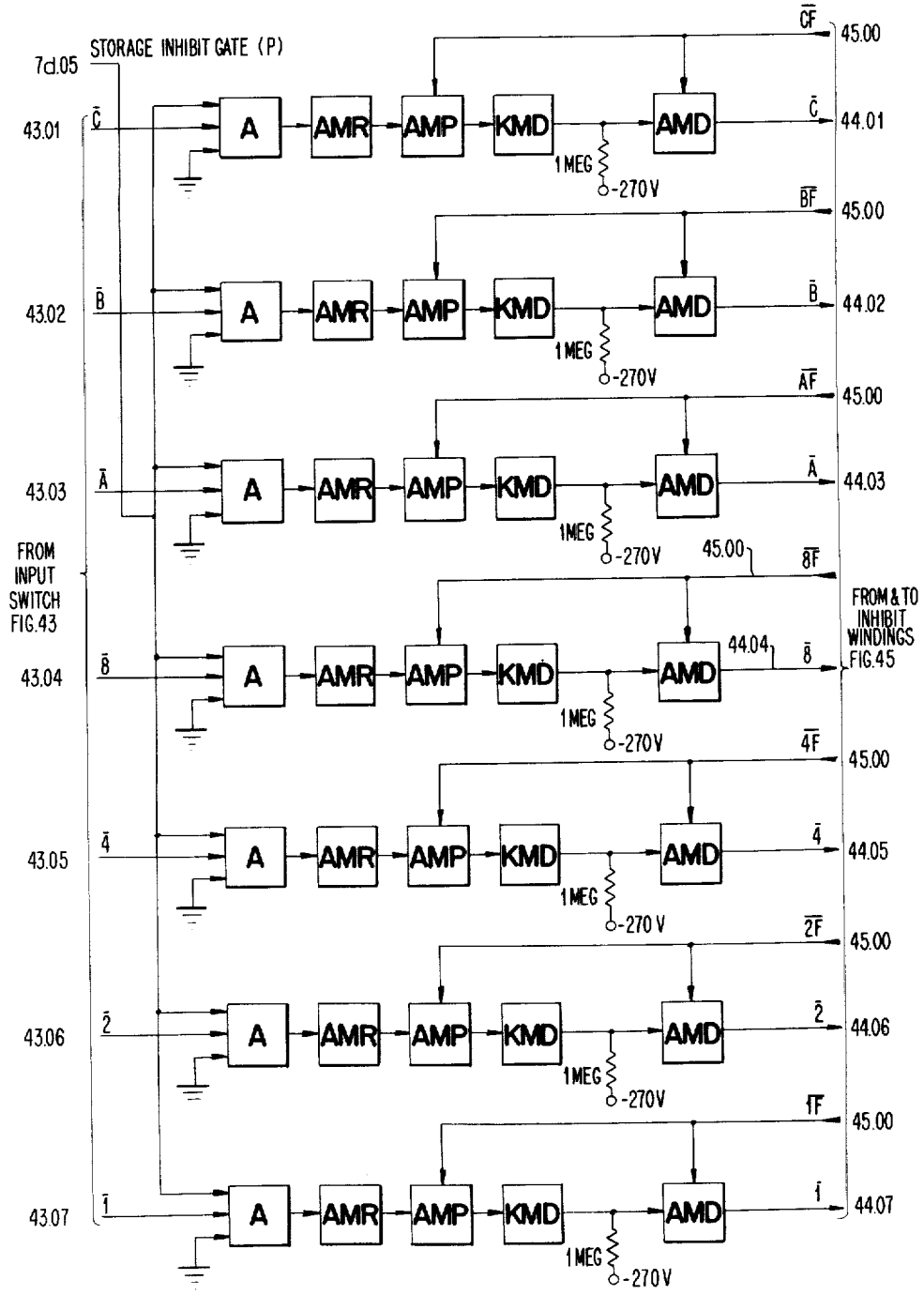


FIG.45

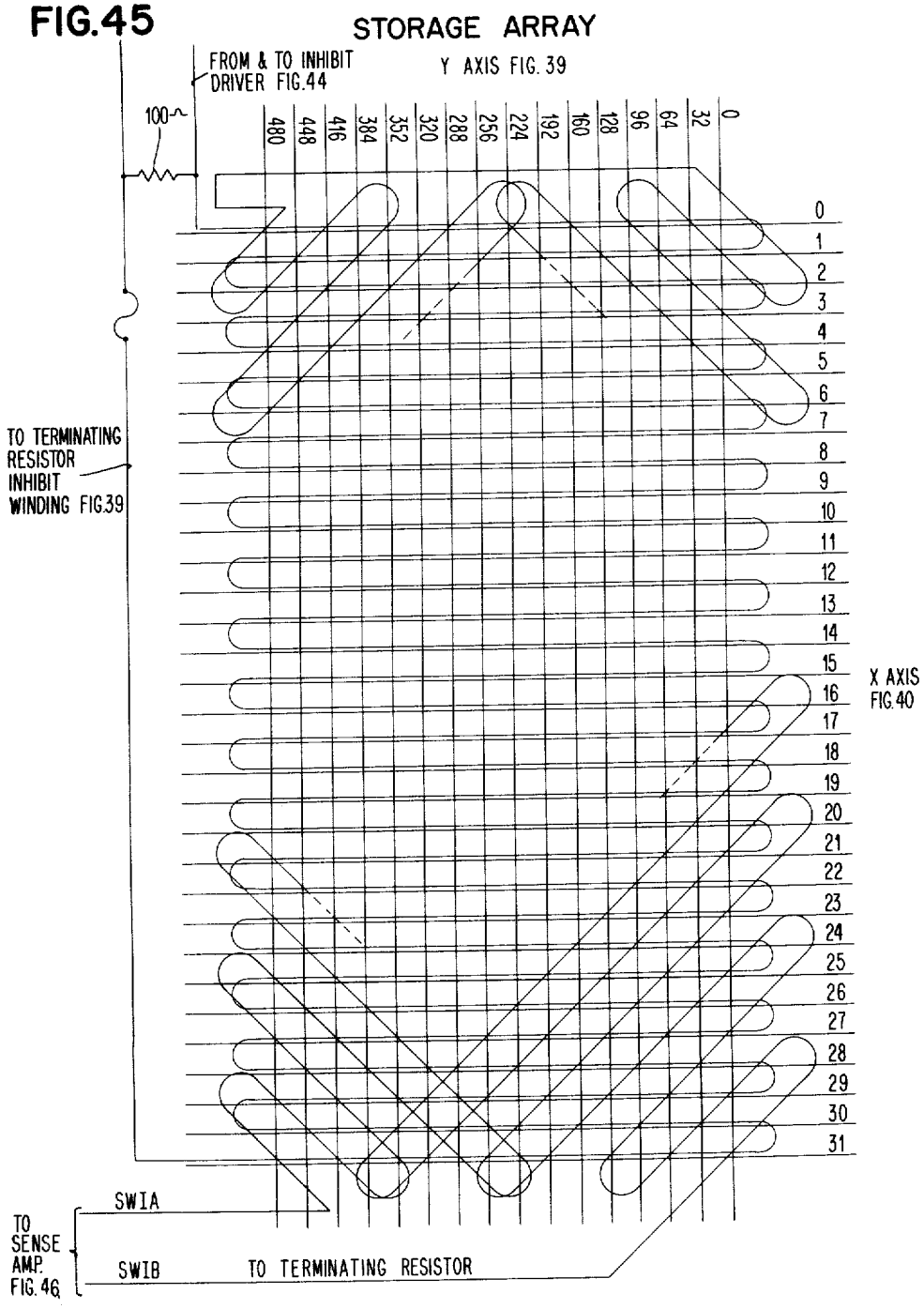

STORAGE ARRAY
FROM & TO INHIBIT DRIVER FIG.44
Y AXIS FIG. 39
100
480
448
416
384
352
320
288
256
224
192
160
128
96
64
32
0
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
X AXIS FIG.40
TO TERMINATING RESISTOR INHIBIT WINDING FIG.39
SWIA
SWIB
TO TERMINATING RESISTOR
TO SENSE AMP. FIG. 46

FIG. 46
SENSE AMPLIFIER (STORAGE)

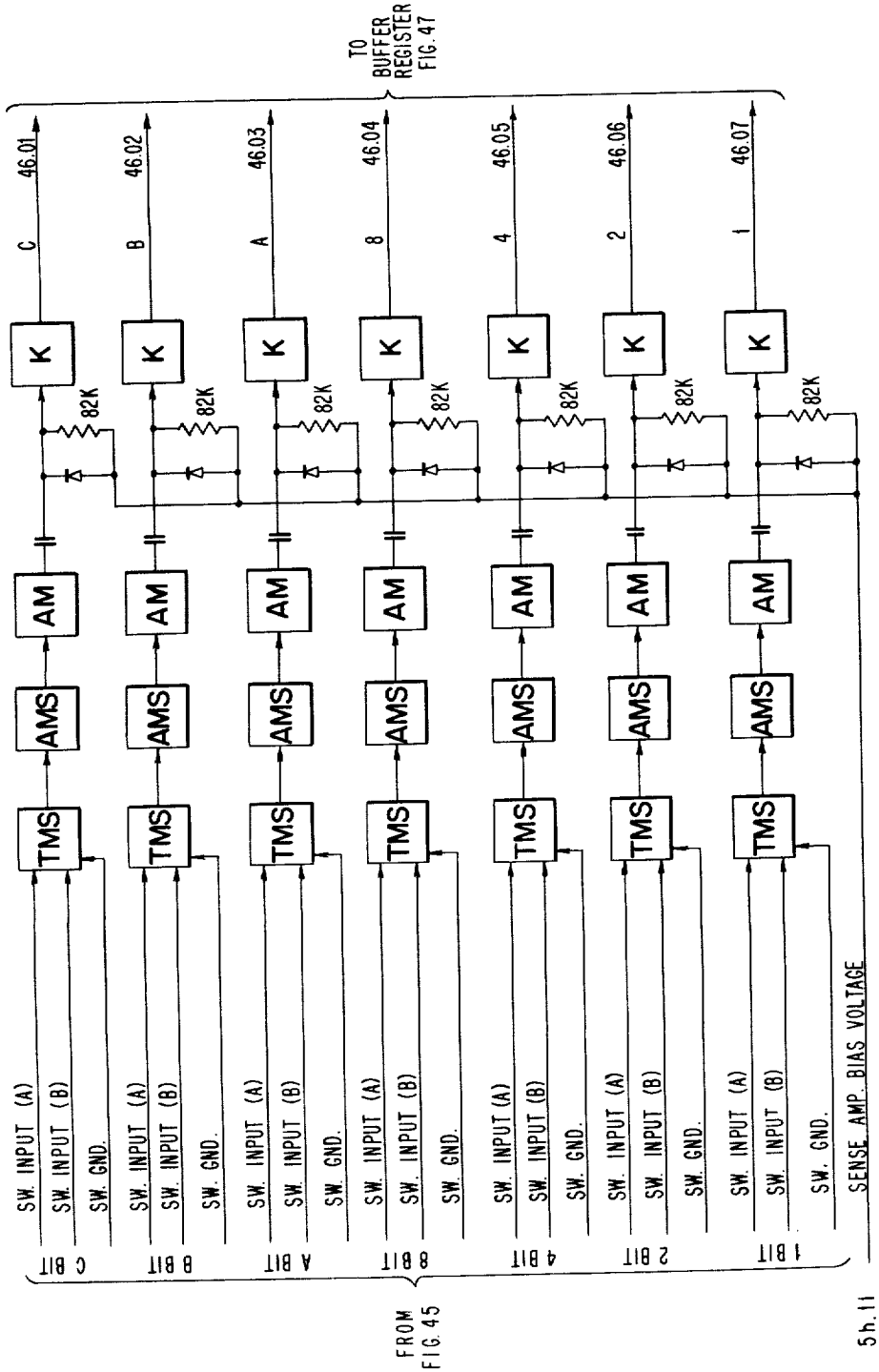
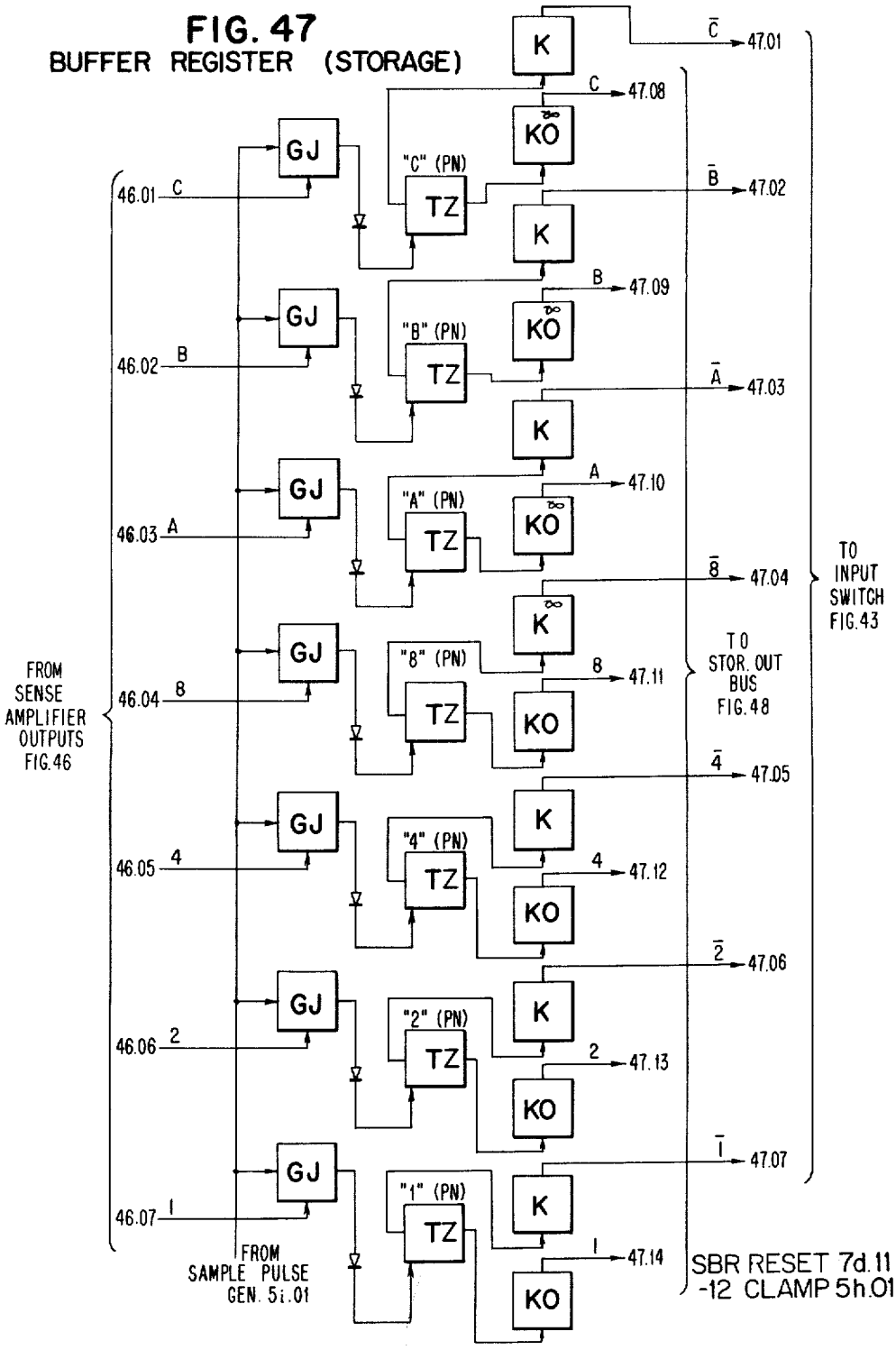


FIG. 47
BUFFER REGISTER (STORAGE)



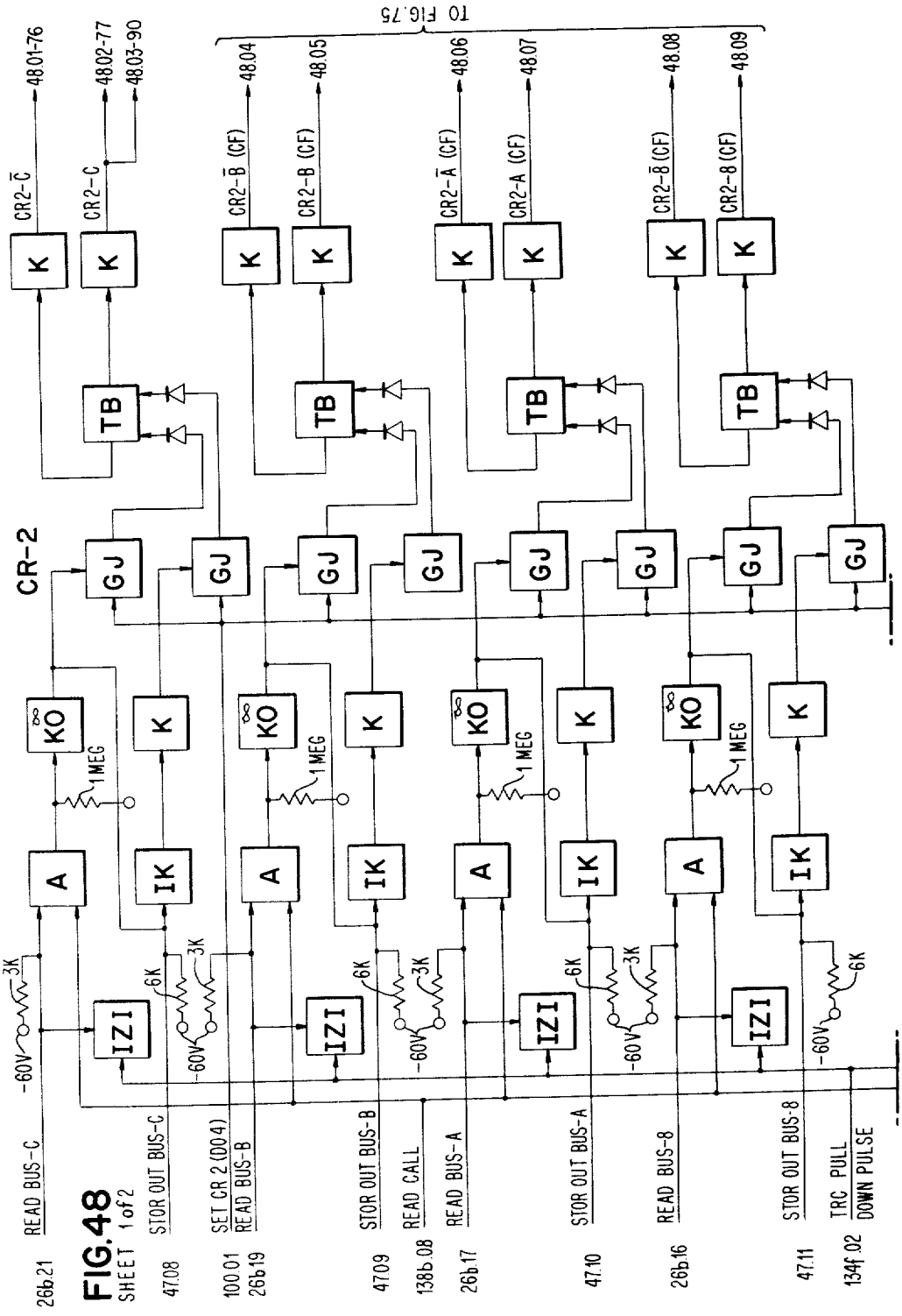


FIG. 48
SHEET 1 of 2

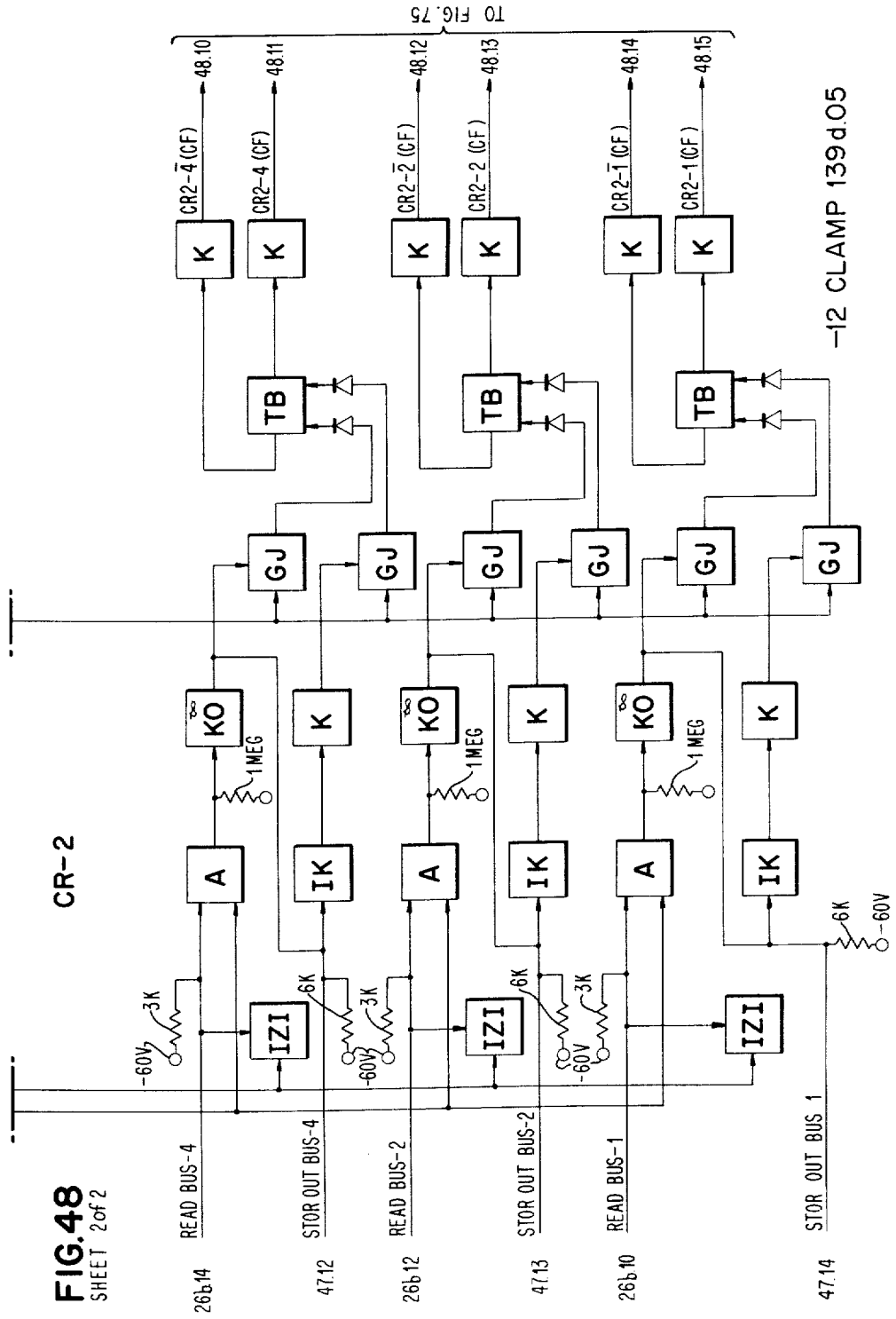
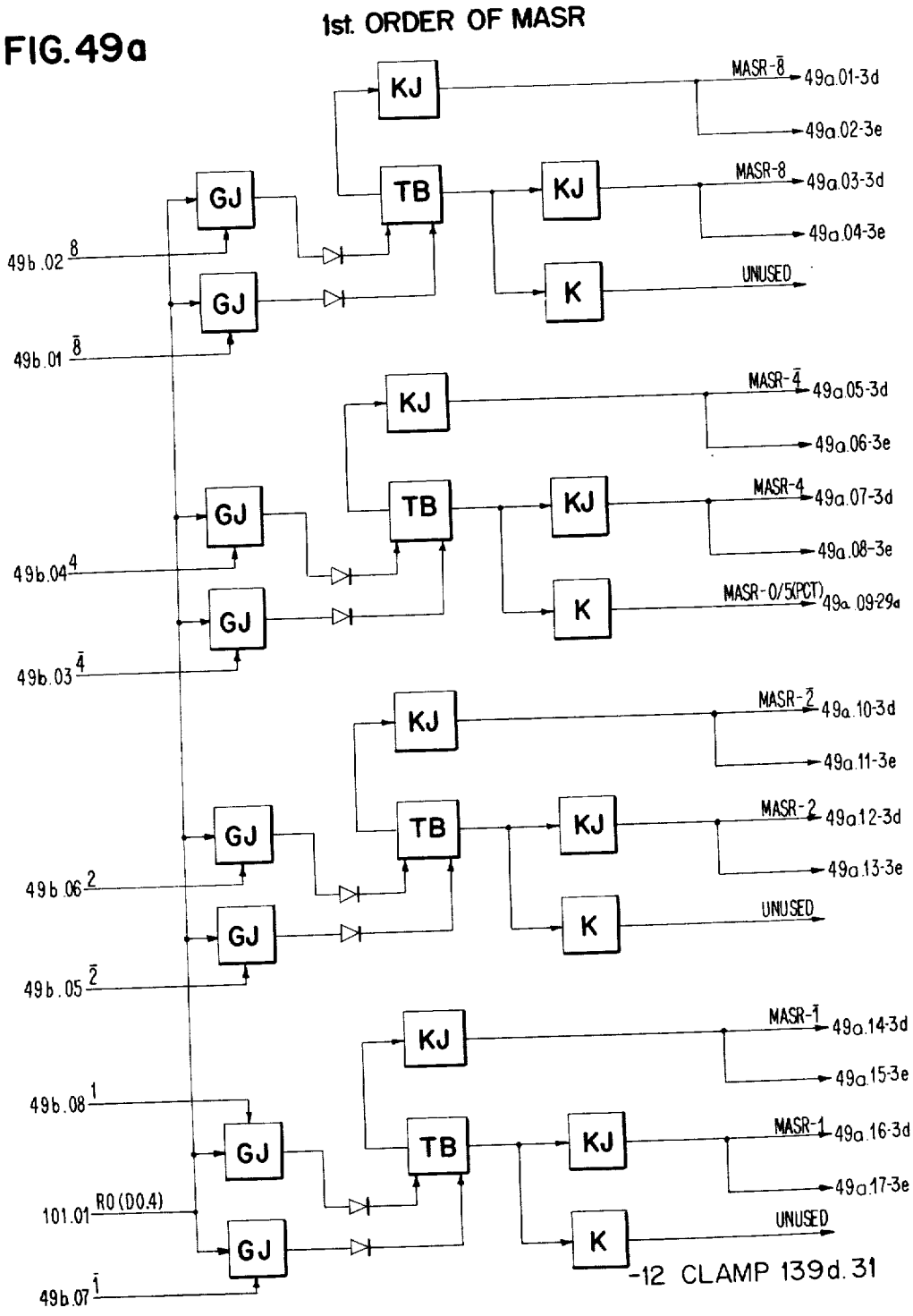


FIG.48
SHEET 2 of 2

FIG. 49a


1st. ORDER OF MASR
KJ
TB
GJ
K
MASR-8̄
49a.01-3d
49a.02-3e
MASR-8
49a.03-3d
49a.04-3e
UNUSED
49b.02 8
49b.01 8̄
MASR-4̄
49a.05-3d
49a.06-3e
MASR-4
49a.07-3d
49a.08-3e
MASR-0/5(PCT)
49a.09-29a
49b.04 4
49b.03 4̄
MASR-2̄
49a.10-3d
49a.11-3e
MASR-2
49a.12-3d
49a.13-3e
UNUSED
49b.06 2
49b.05 2̄
MASR-1̄
49a.14-3d
49a.15-3e
MASR-1
49a.16-3d
49a.17-3e
UNUSED
49b.08 1
101.01 RO (DO.4)
49b.07 1̄
-12 CLAMP 139d.31

1st. ORDER MASR SET CIRCUITS FIG. 49b

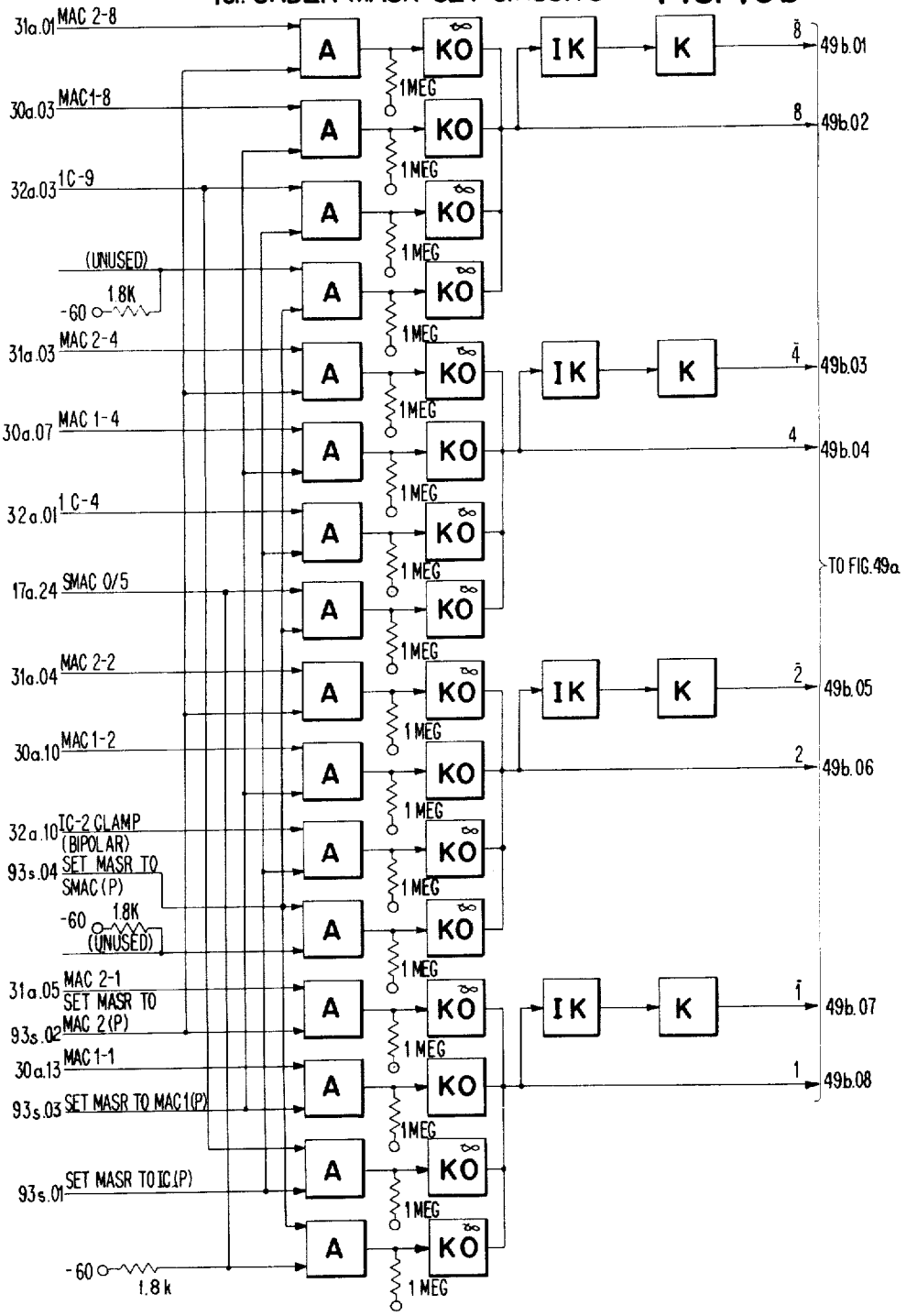


FIG. 49c

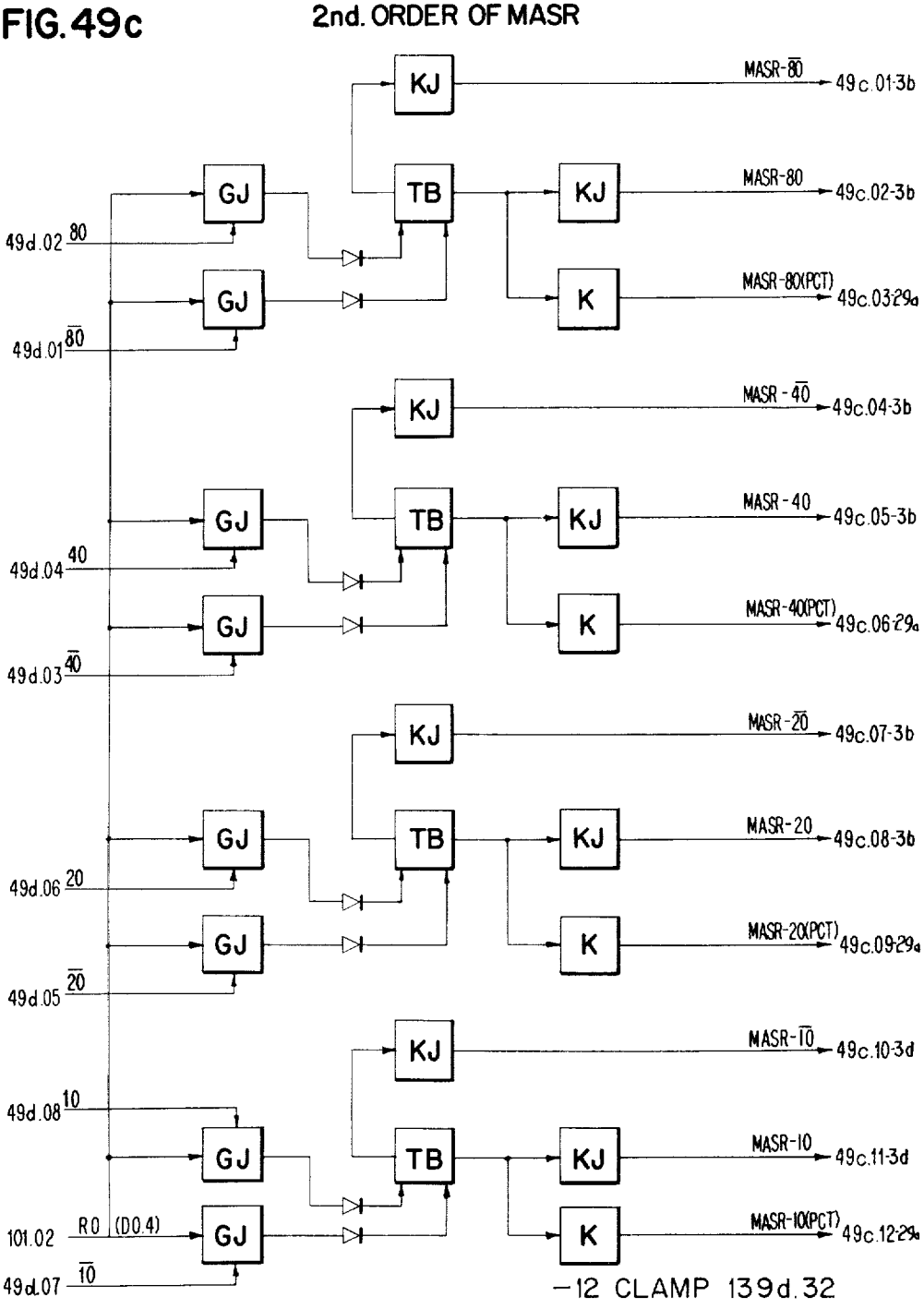
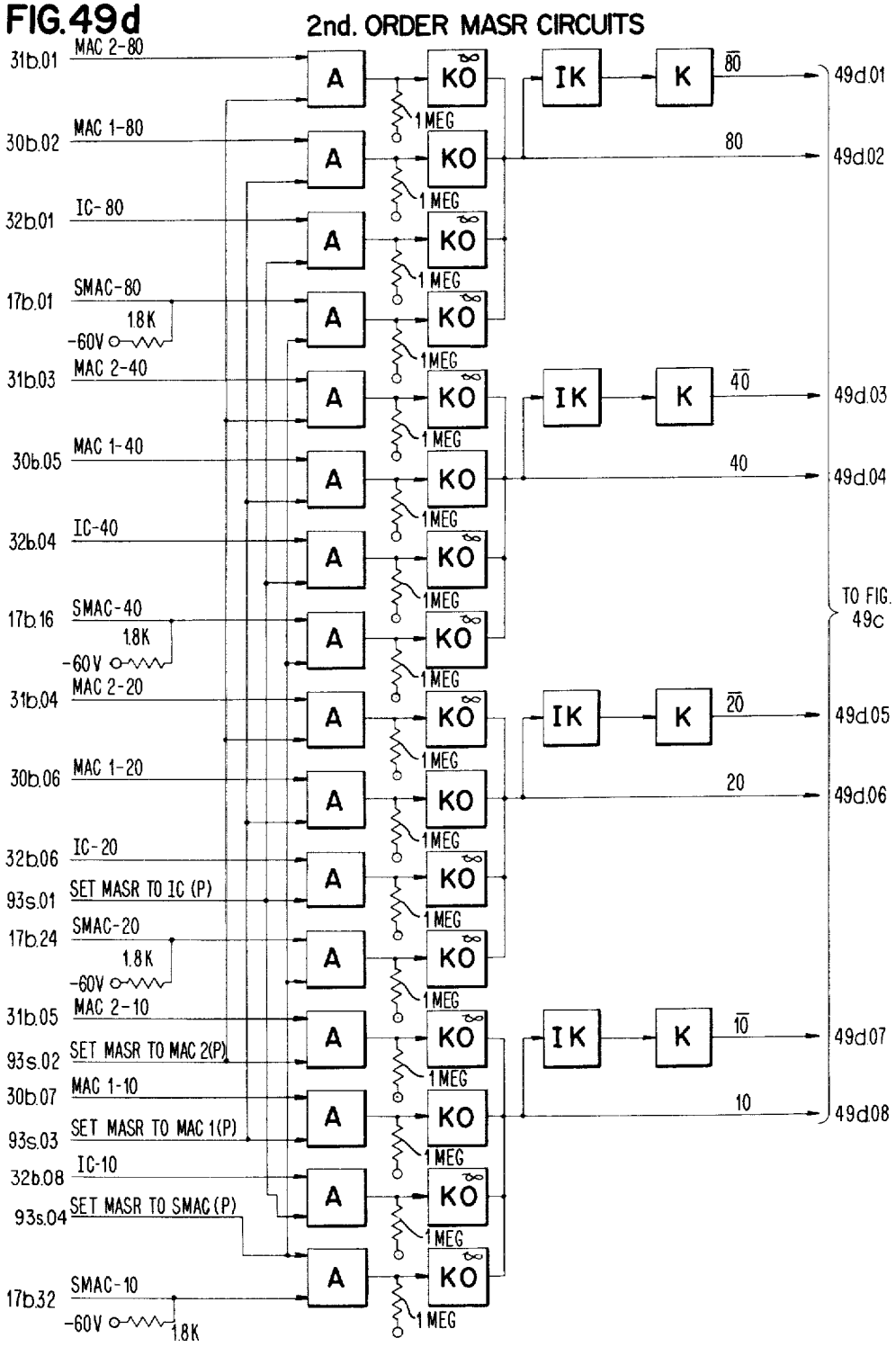

2nd. ORDER OF MASR
KJ
TB
GJ
K
MASR-$\overline{80}$
49c.01-3b
MASR-80
49c.02-3b
MASR-80(PCT)
49c.03-29a
MASR-$\overline{40}$
49c.04-3b
MASR-40
49c.05-3b
MASR-40(PCT)
49c.06-29a
MASR-$\overline{20}$
49c.07-3b
MASR-20
49c.08-3b
MASR-20(PCT)
49c.09-29a
MASR-$\overline{10}$
49c.10-3d
MASR-10
49c.11-3d
MASR-10(PCT)
49c.12-29a
49d.02 80
49d.01 $\overline{80}$
49d.04 40
49d.03 $\overline{40}$
49d.06 20
49d.05 $\overline{20}$
49d.08 10
49d.07 $\overline{10}$
101.02 R0 (D0.4)
-12 CLAMP 139d.32

FIG. 49d


2nd. ORDER MASR CIRCUITS
31b.01 MAC 2-80
30b.02 MAC 1-80
32b.01 IC-80
17b.01 SMAC-80
1.8K
-60V
31b.03 MAC 2-40
30b.05 MAC 1-40
32b.04 IC-40
17b.16 SMAC-40
1.8K
-60V
31b.04 MAC 2-20
30b.06 MAC 1-20
32b.06 IC-20
93s.01 SET MASR TO IC (P)
17b.24 SMAC-20
1.8K
-60V
31b.05 MAC 2-10
93s.02 SET MASR TO MAC 2(P)
30b.07 MAC 1-10
93s.03 SET MASR TO MAC 1(P)
32b.08 IC-10
93s.04 SET MASR TO SMAC (P)
17b.32 SMAC-10
-60V
1.8K
A
KO
1 MEG
IK
K
80
40
20
10
49d.01
49d.02
49d.03
49d.04
49d.05
49d.06
49d.07
49d.08
TO FIG. 49c

3rd. ORDER OF MASR

FIG.49e

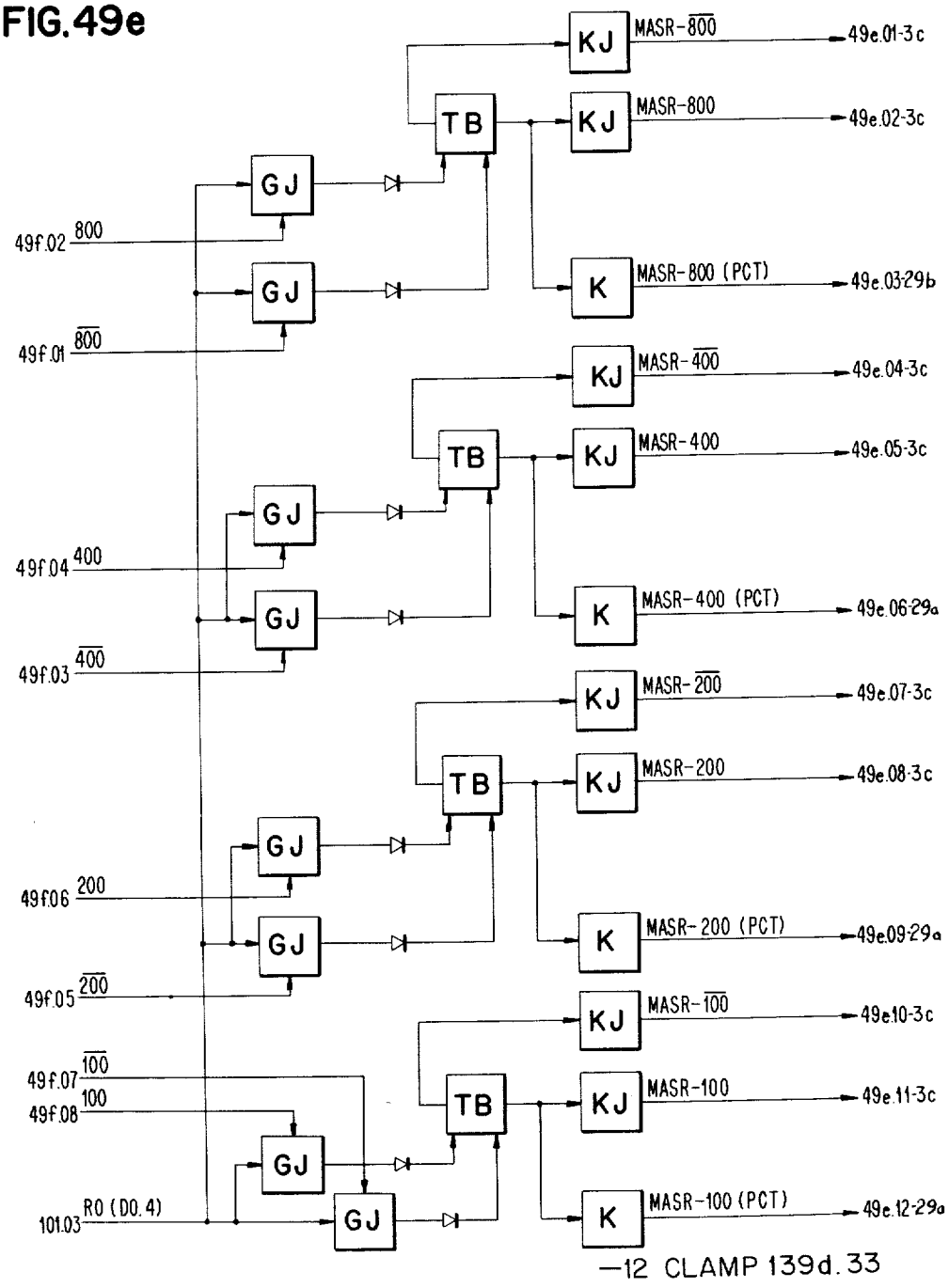


FIG. 49f

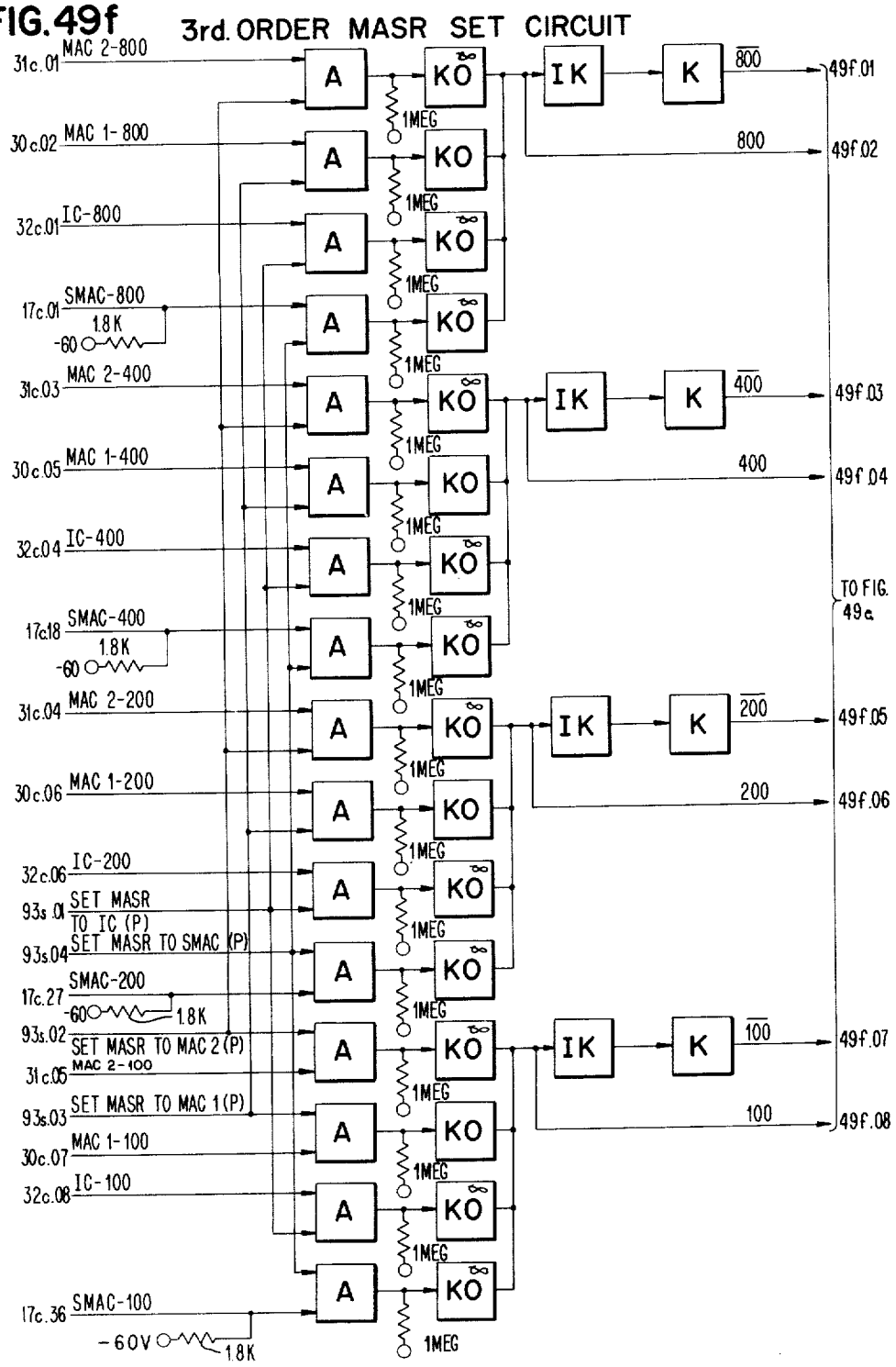

3rd. ORDER MASR SET CIRCUIT
31c.01 MAC 2-800
30c.02 MAC 1-800
32c.01 IC-800
17c.01 SMAC-800
1.8K
-60
31c.03 MAC 2-400
30c.05 MAC 1-400
32c.04 IC-400
17c.18 SMAC-400
1.8K
-60
31c.04 MAC 2-200
30c.06 MAC 1-200
32c.06 IC-200
93s.01 SET MASR TO IC (P)
93s.04 SET MASR TO SMAC (P)
17c.27 SMAC-200
-60
1.8K
93s.02 SET MASR TO MAC 2 (P)
31c.05 MAC 2-100
93s.03 SET MASR TO MAC 1 (P)
30c.07 MAC 1-100
32c.08 IC-100
17c.36 SMAC-100
-60V
1.8K
A
KO
1MEG
IK
K
800
800
49f.01
49f.02
400
400
49f.03
49f.04
200
200
49f.05
49f.06
100
100
49f.07
49f.08
TO FIG. 49a

FIG.49g

4th. ORDER OF MASR

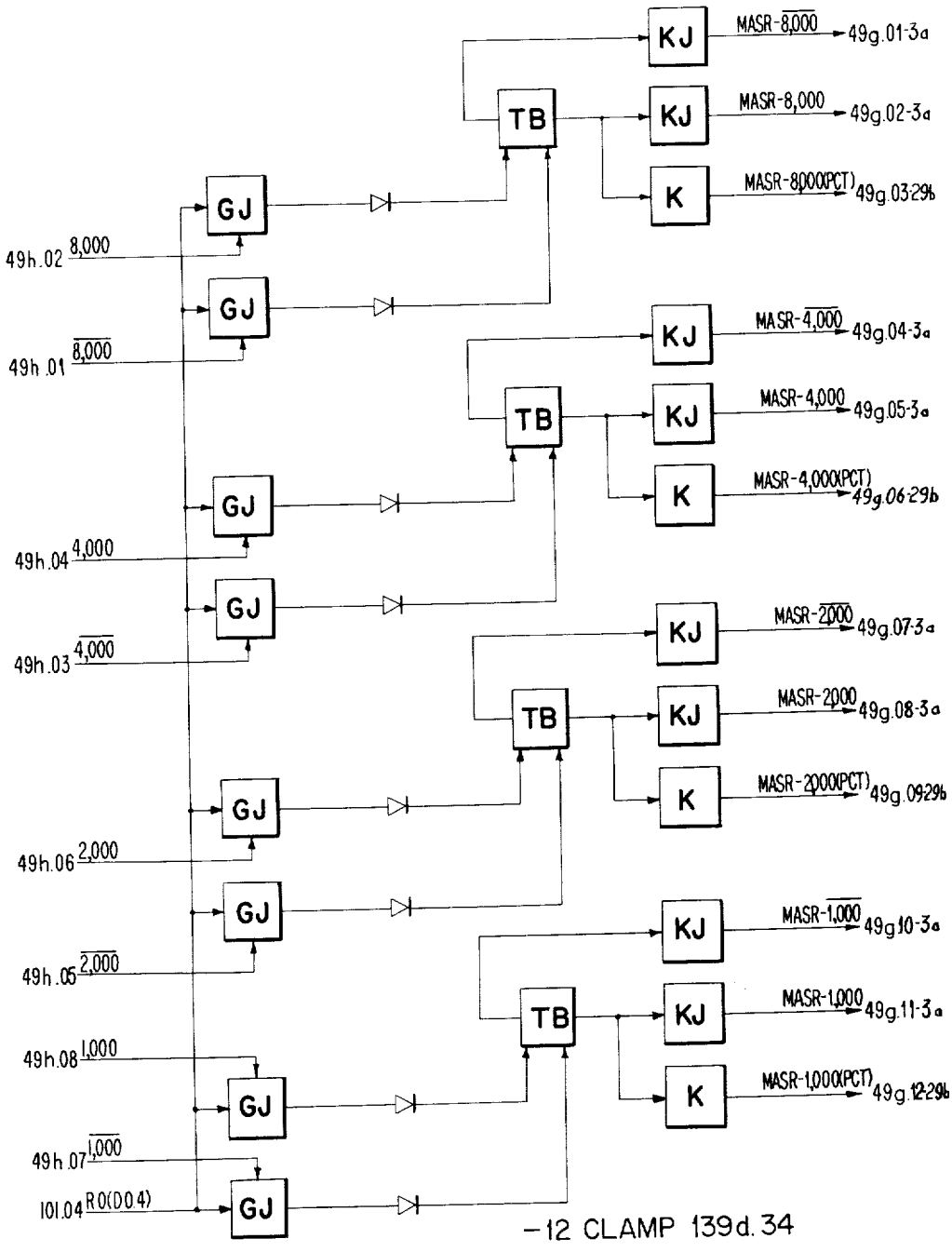


FIG. 49h 4th. ORDER MASR SET CIRCUITS

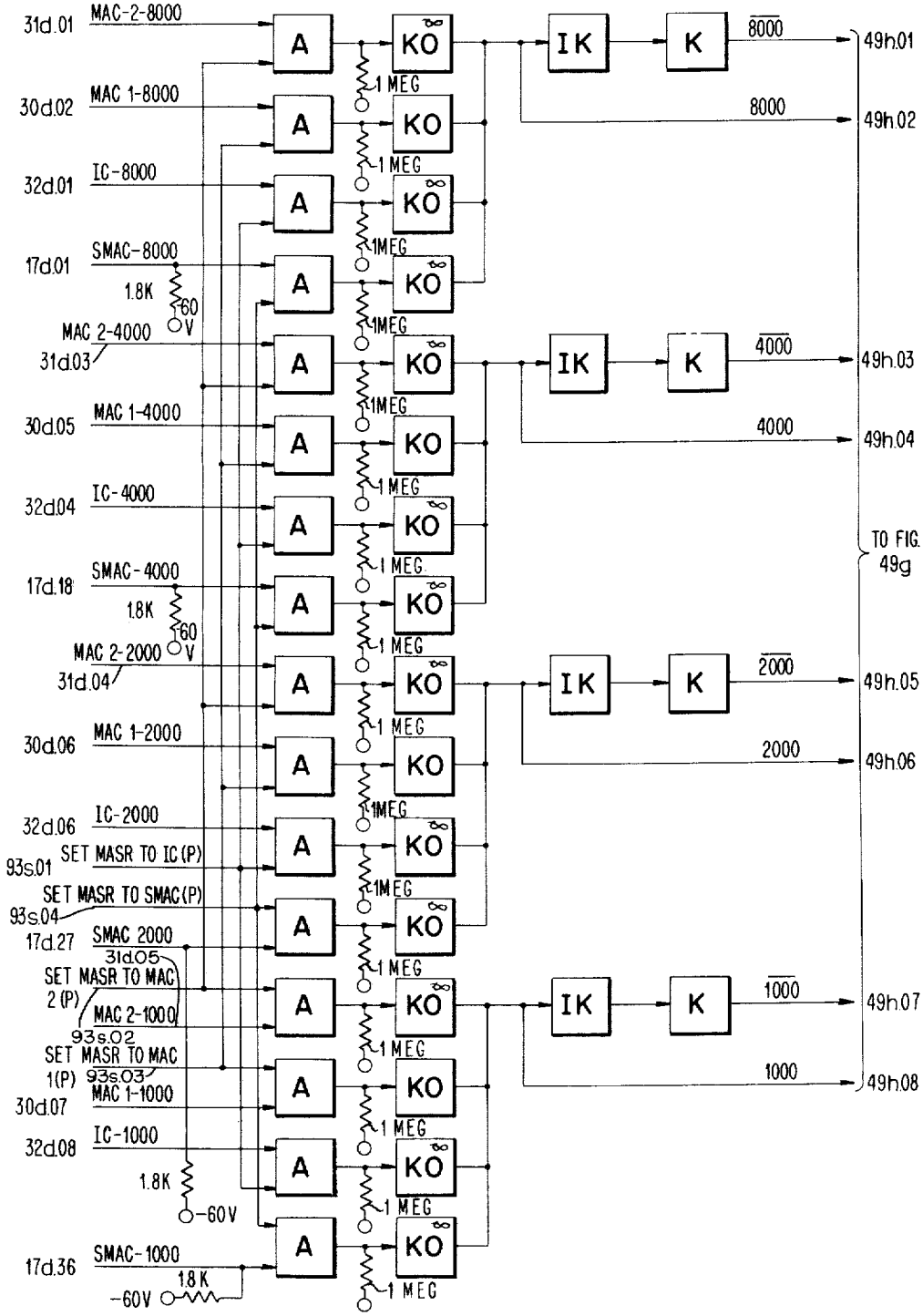


FIG.49i

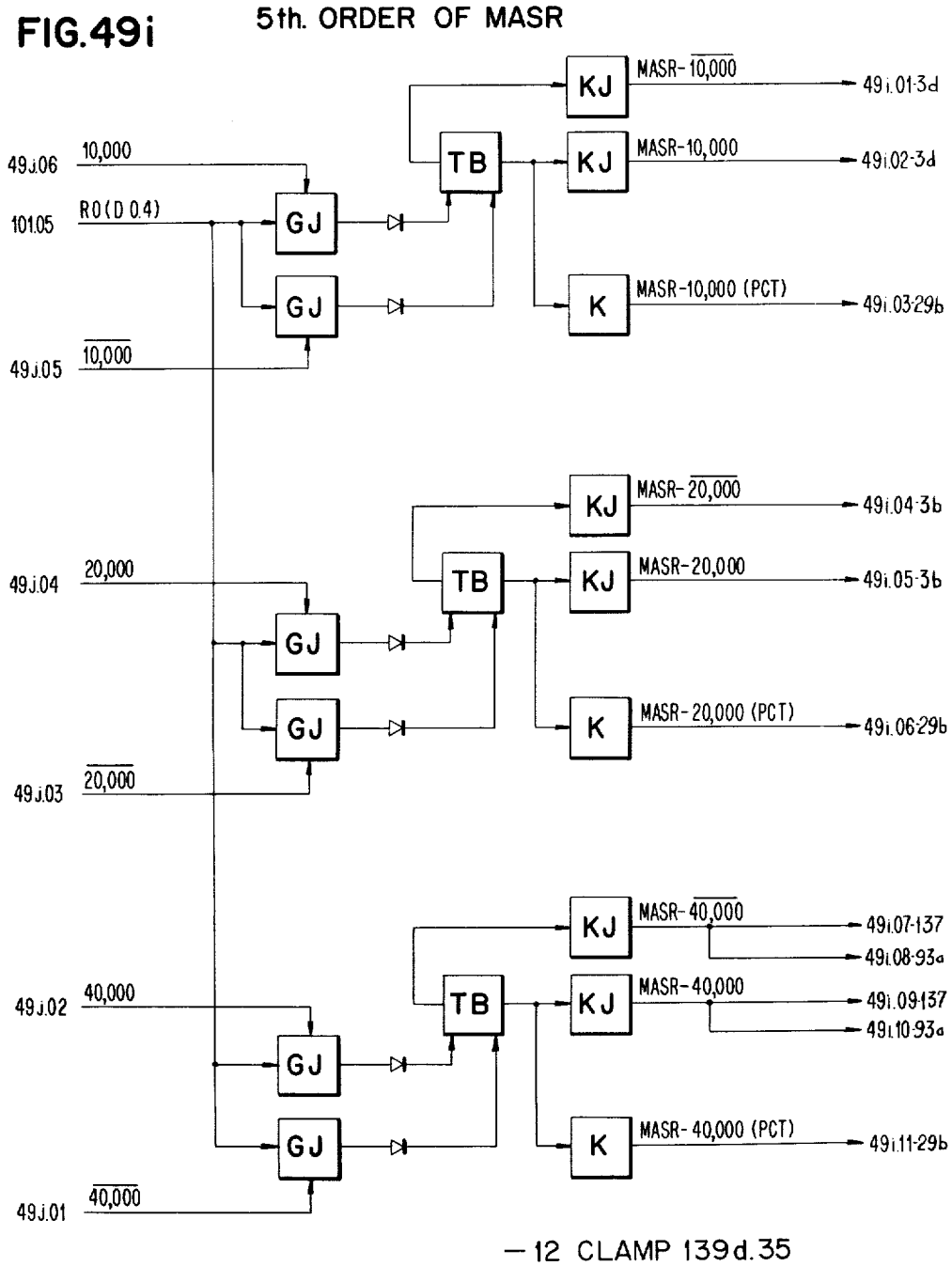
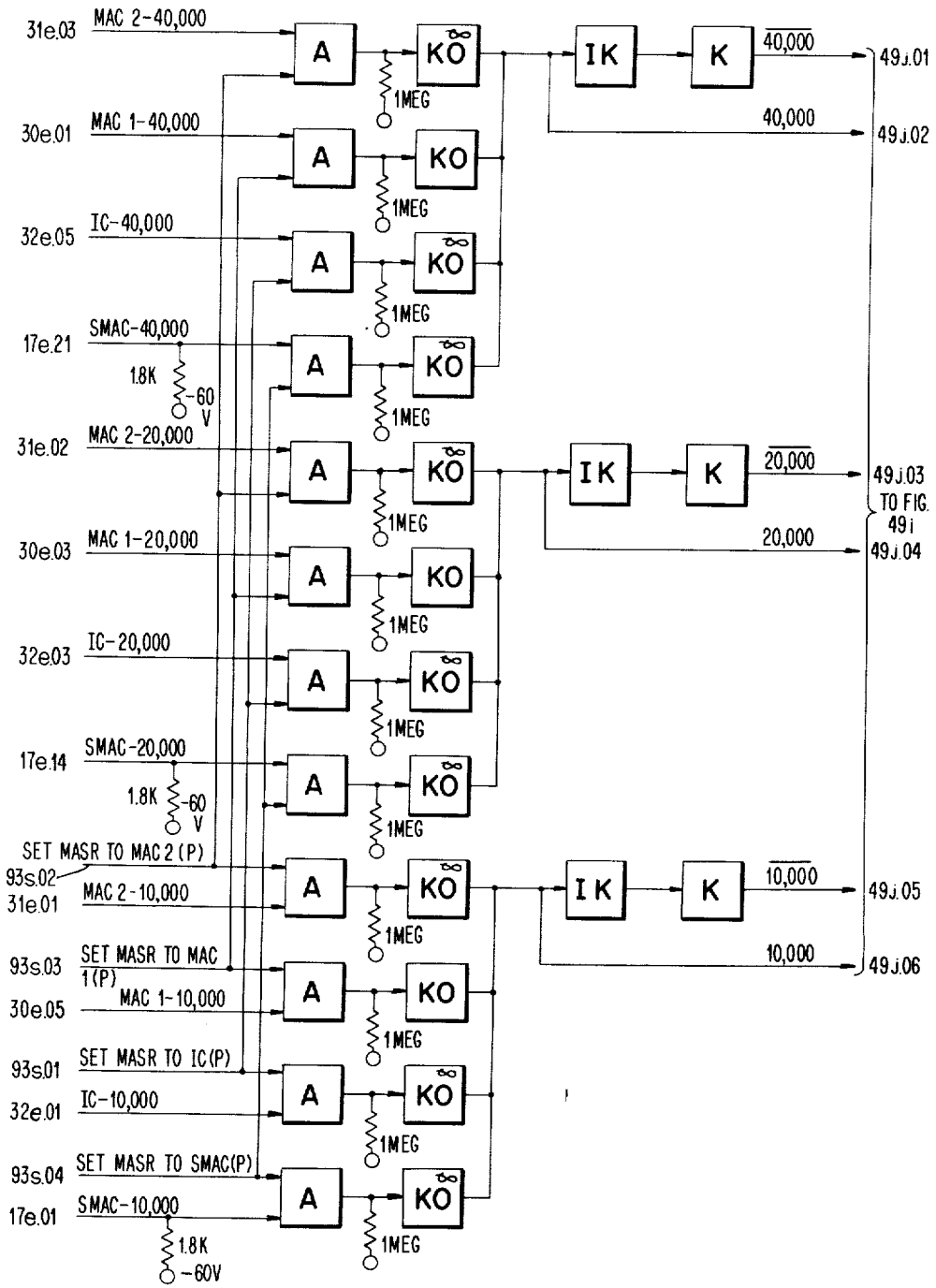

5th. ORDER OF MASR
KJ
MASR-10,000
49i.01-3d
TB
KJ
MASR-10,000
49i.02-3d
49j.06
10,000
101.05
R0(D 0.4)
GJ
GJ
K
MASR-10,000 (PCT)
49i.03-29b
49j.05
10,000
KJ
MASR-20,000
49i.04-3b
49j.04
20,000
TB
KJ
MASR-20,000
49i.05-3b
GJ
GJ
K
MASR-20,000 (PCT)
49i.06-29b
49j.03
20,000
KJ
MASR-40,000
49i.07-137
49i.08-93a
49j.02
40,000
TB
KJ
MASR-40,000
49i.09-137
49i.10-93a
GJ
GJ
K
MASR-40,000 (PCT)
49i.11-29b
49j.01
40,000
— 12 CLAMP 139d.35

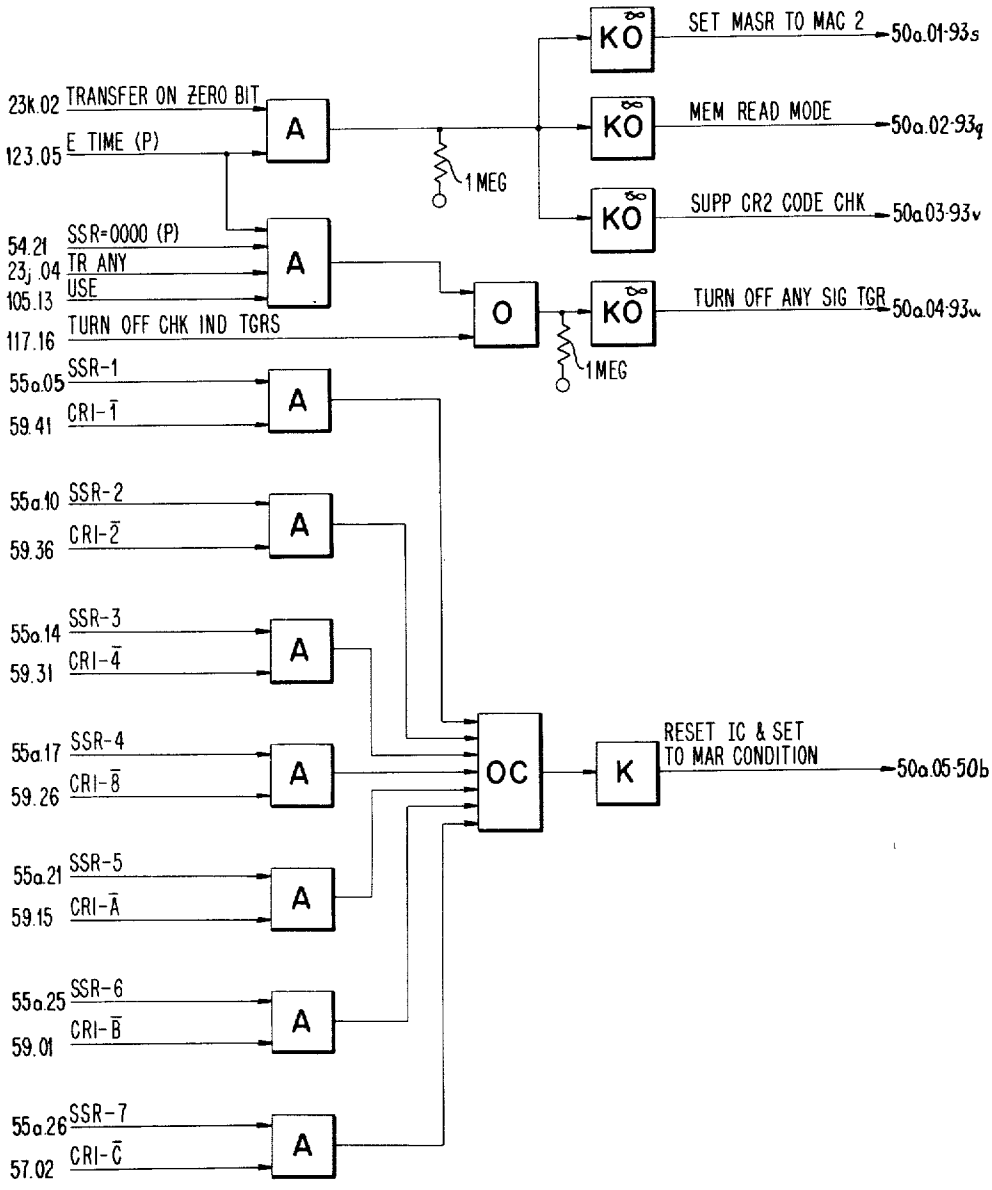
FIG. 49j

5th. ORDER MASR SET CIRCUITS



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FIG. 50a



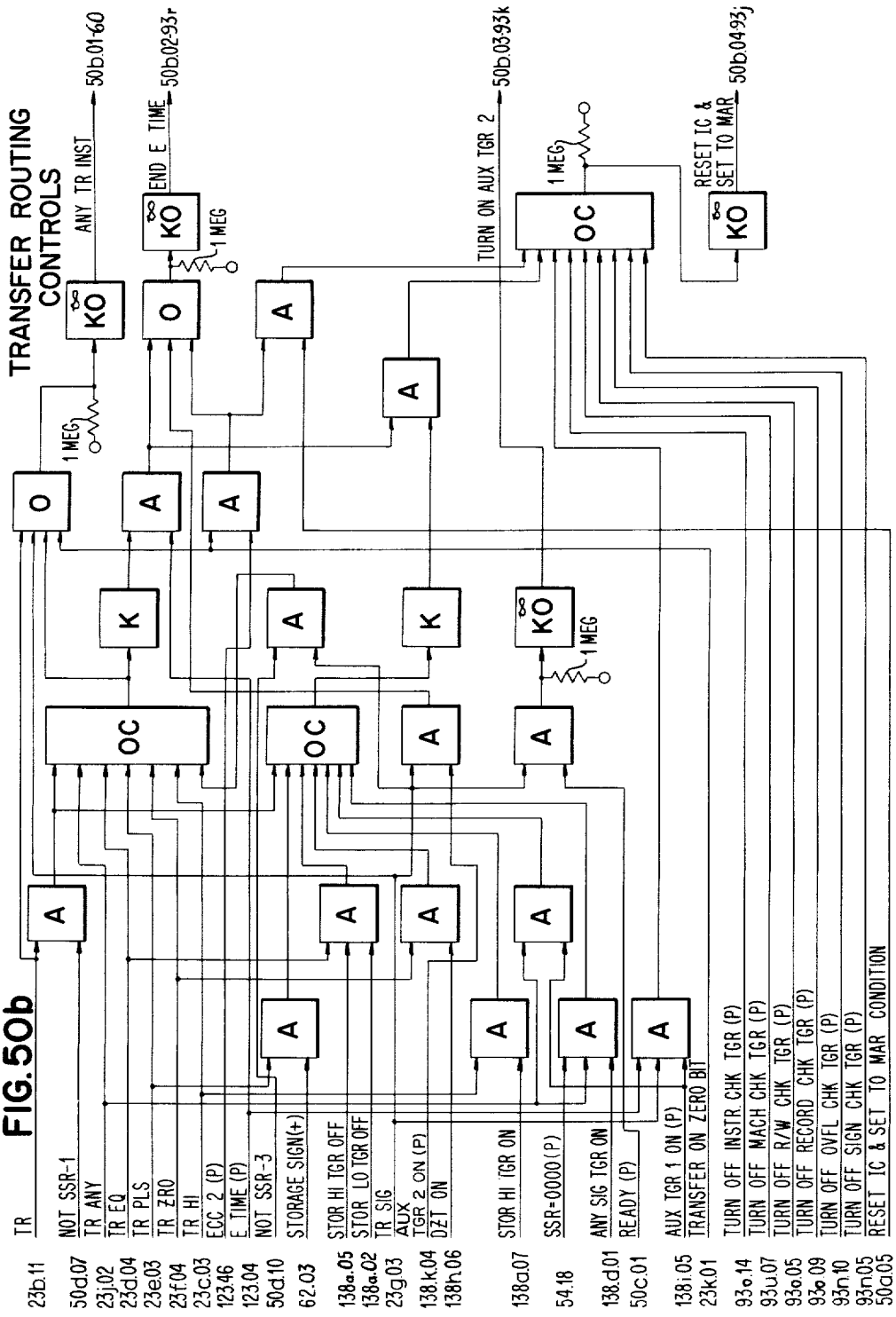
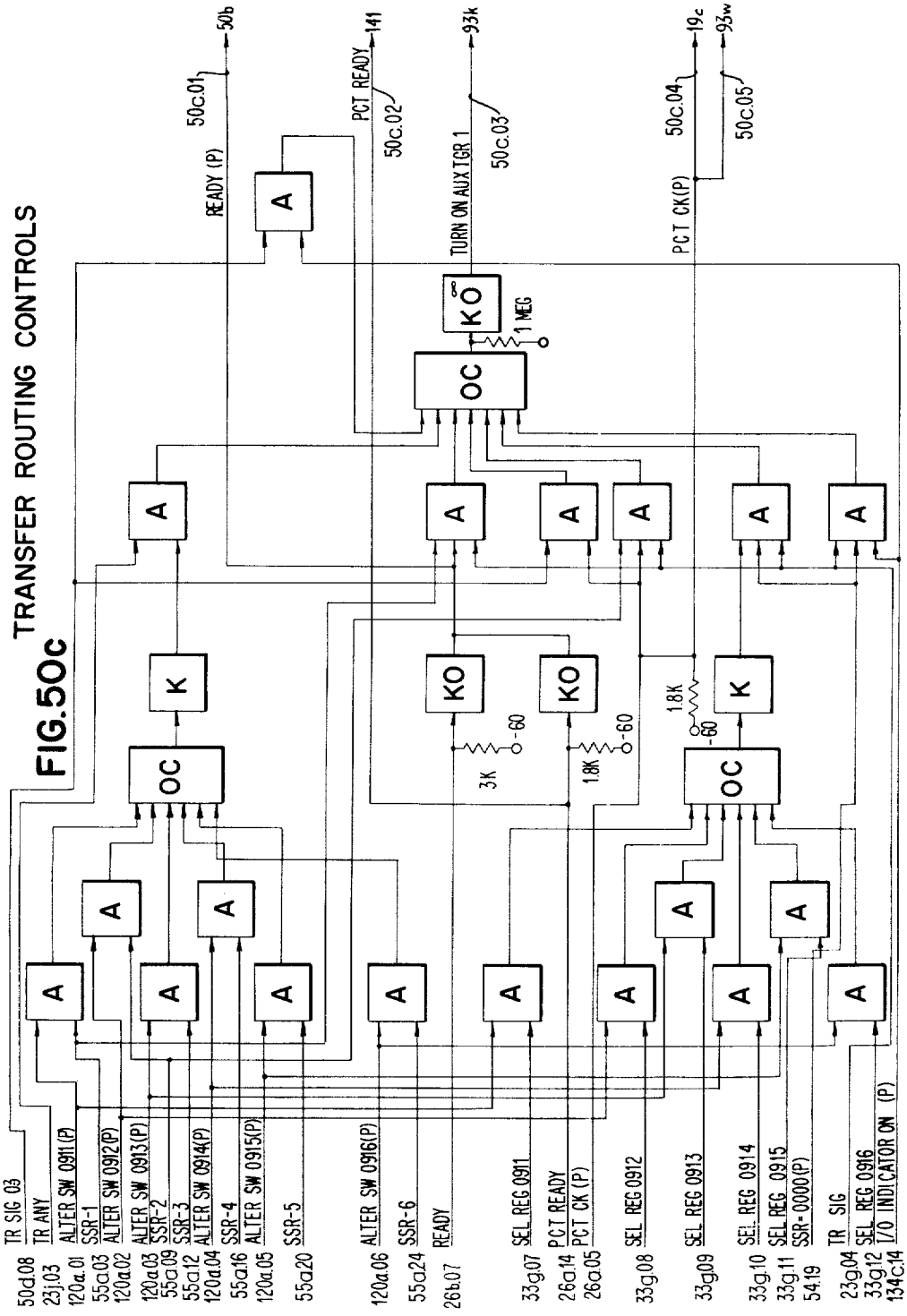

TRANSFER ROUTING CONTROLS
ANY TR INST
50b.01-60
END E TIME
50b.02-93r
TURN ON AUX TGR 2
50b.03-93k
RESET IC & SET TO MAR
50b.04-93j
1 MEG
O
A
K
KO
OC
TR
NOT SSR-1
TR ANY
TR EQ
TR PLS
TR ZRO
TR HI
ECC 2 (P)
E TIME (P)
NOT SSR-3
STORAGE SIGN(+)
STOR HI TGR OFF
STOR LO TGR OFF
TR SIG
AUX TGR 2 ON (P)
DZT ON
STOR HI TGR ON
SSR=0000 (P)
ANY SIG TGR ON
READY (P)
AUX TGR 1 ON (P)
TRANSFER ON ZERO BIT
TURN OFF INSTR CHK TGR (P)
TURN OFF MACH CHK TGR (P)
TURN OFF R/W CHK TGR (P)
TURN OFF RECORD CHK TGR (P)
TURN OFF OVFL CHK TGR (P)
TURN OFF SIGN CHK TGR (P)
RESET IC & SET TO MAR CONDITION
23b.11
50d.07
23j.02
23d.04
23e.03
23f.04
23c.03
123.46
123.04
50d.10
62.03
138a.05
138a.02
23g.03
138k.04
138h.06
138a.07
54.18
138.d.01
50c.01
138i.05
23k.01
93o.14
93u.07
93o.05
93o.09
93n.10
93n.05
50a.05

FIG.50b

FIG.50c TRANSFER ROUTING CONTROLS



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FIG.50d TRANSFER ROUTING CONTROLS

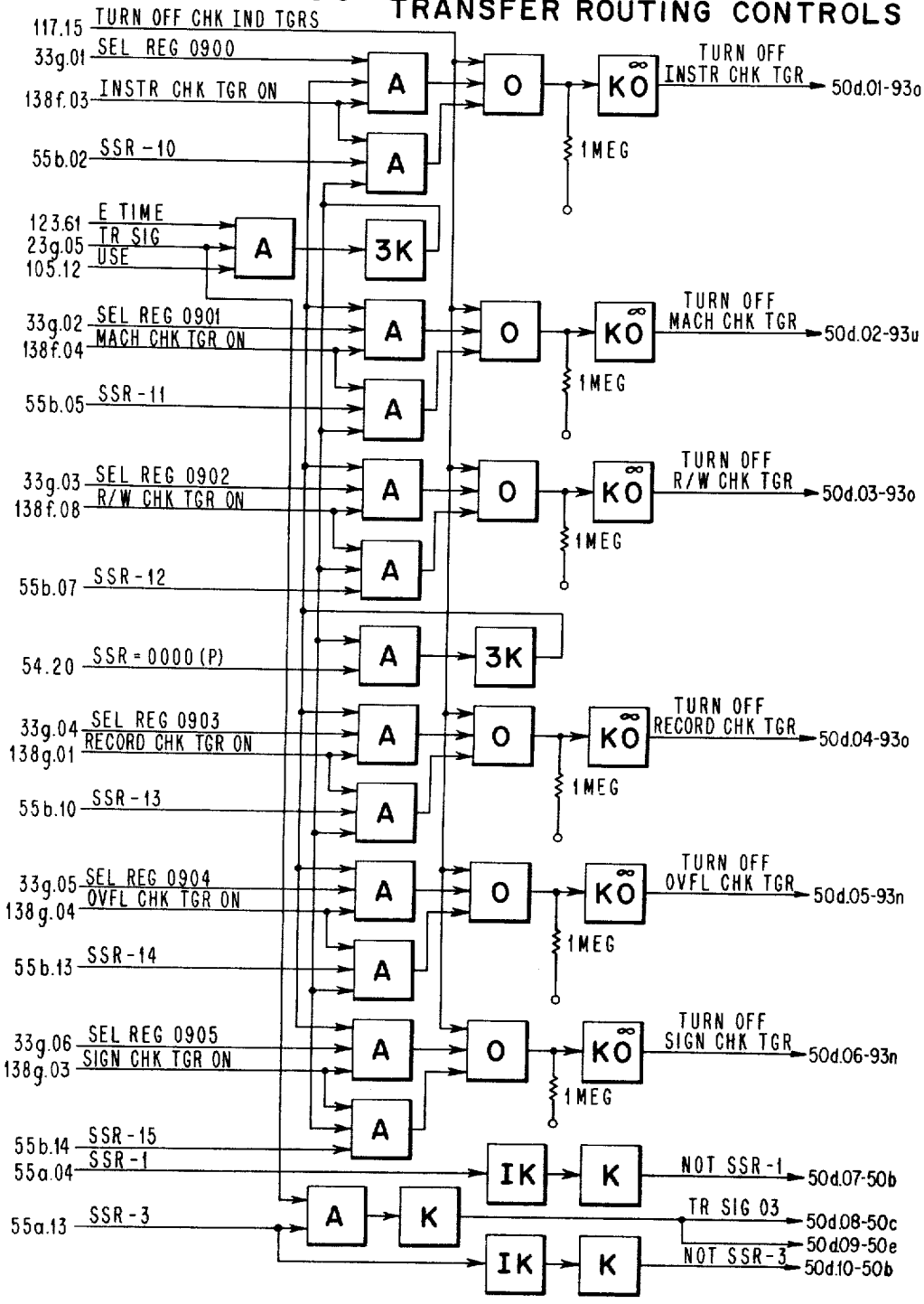


FIG. 50e

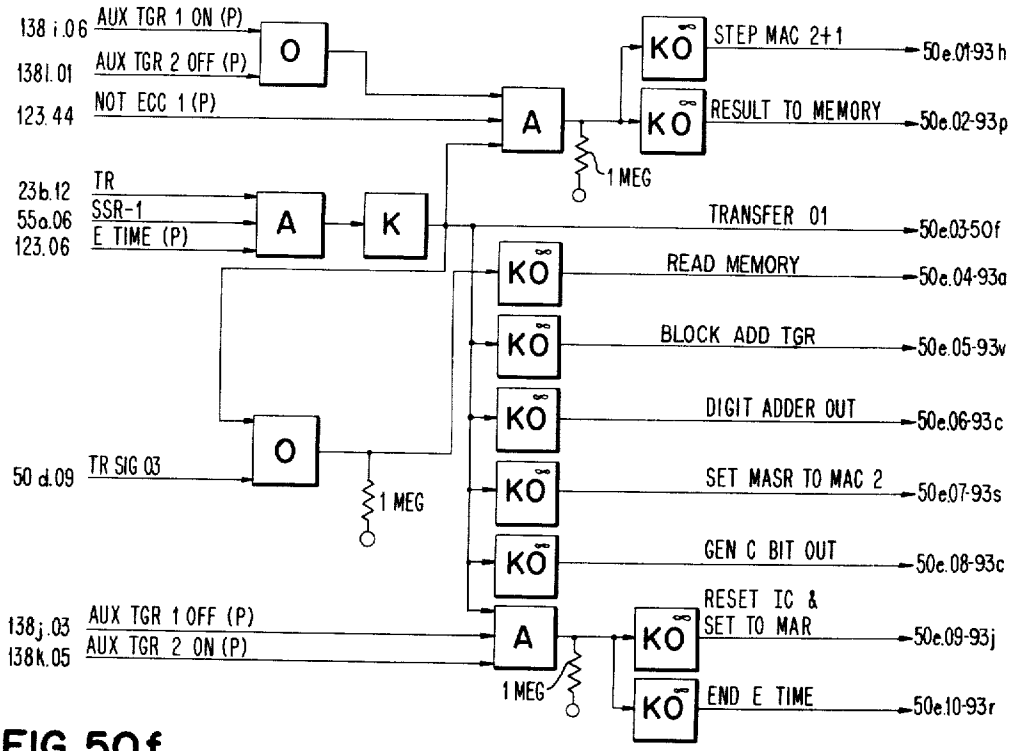
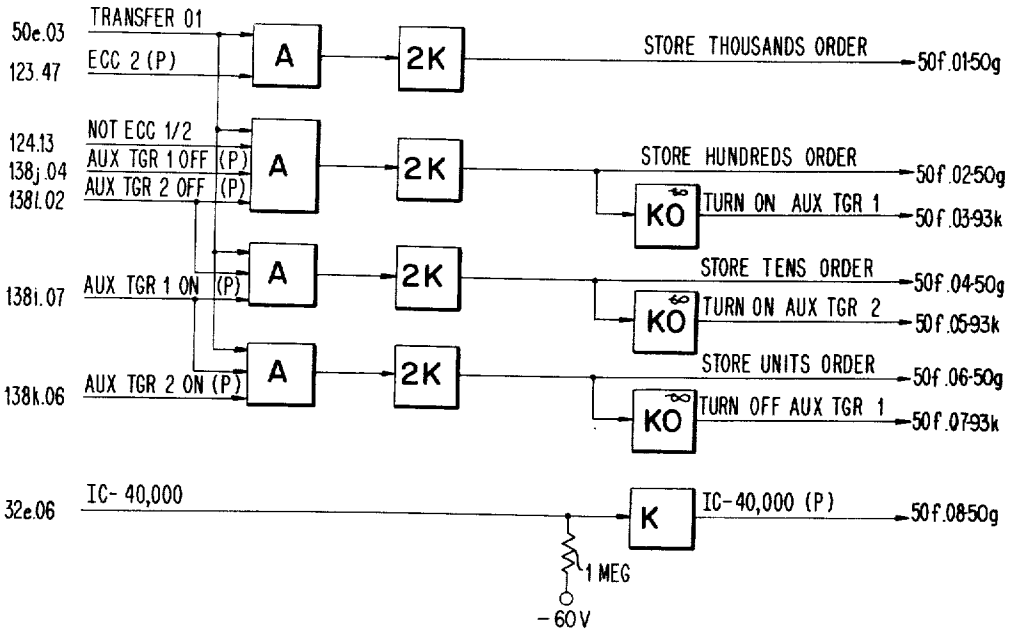
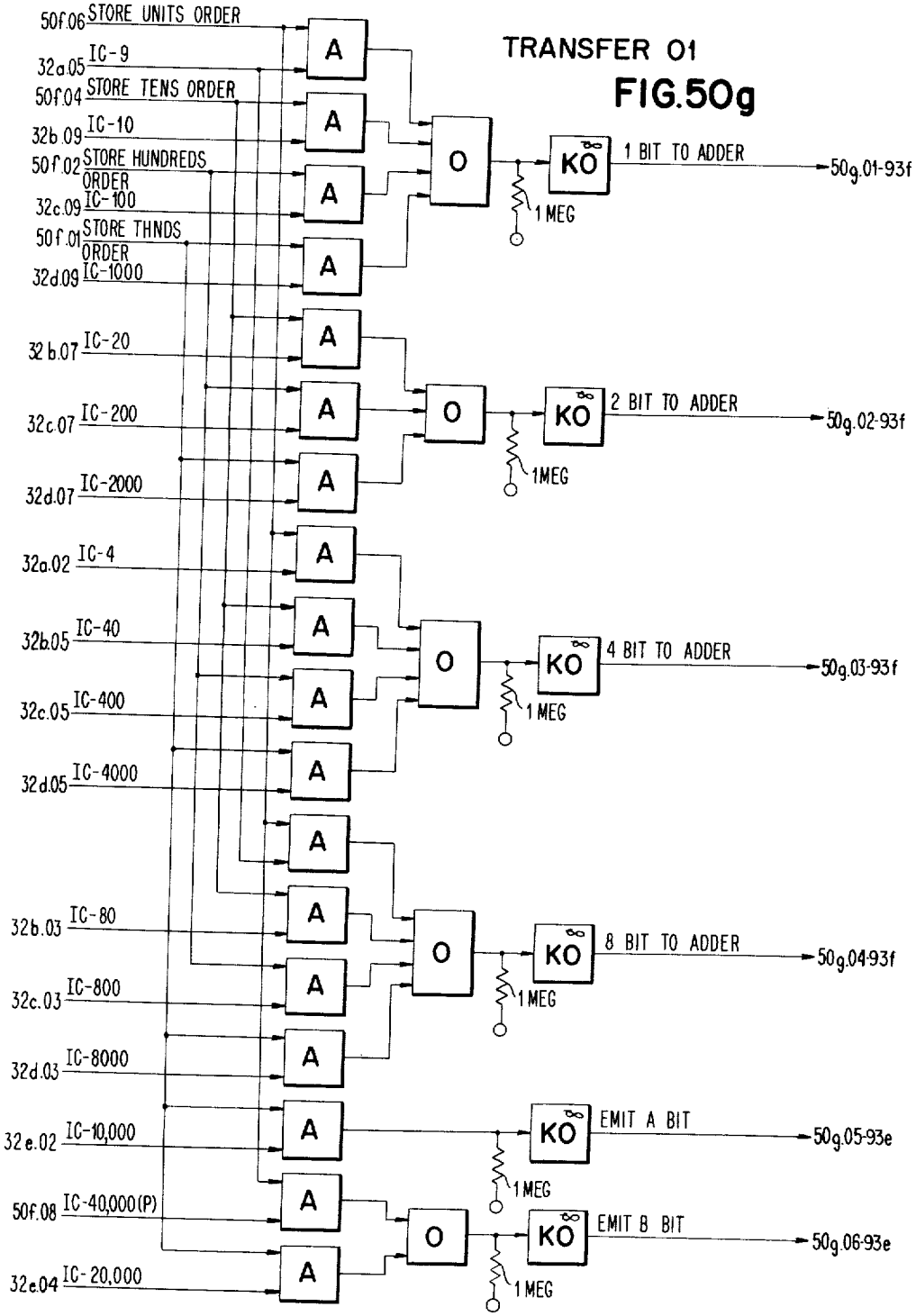


FIG. 50f



TRANSFER 01

FIG.50g



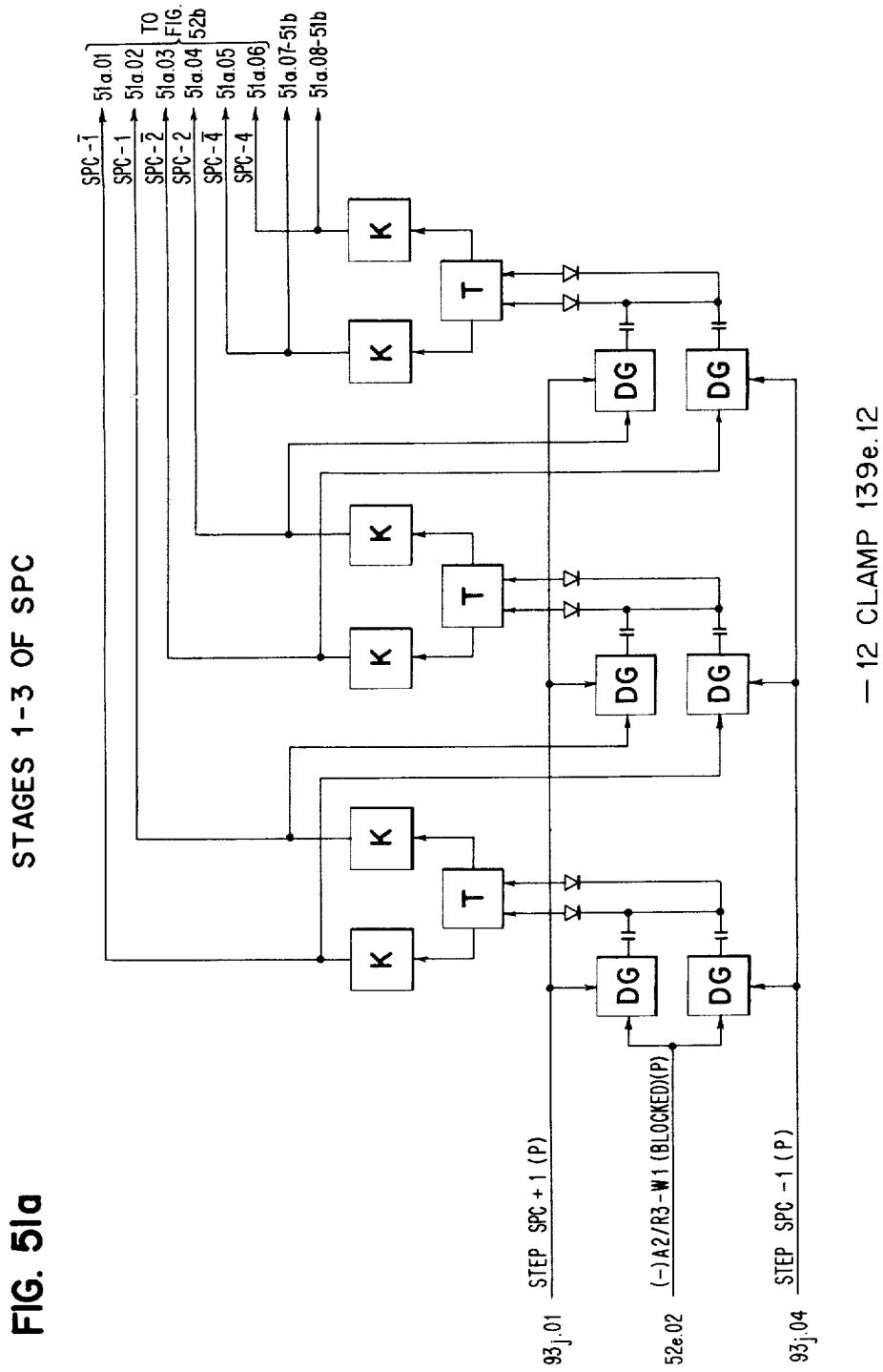

SPC-1̄
SPC-1
SPC-2̄
SPC-2
SPC-4̄
SPC-4
51a.01
51a.02
51a.03
51a.04
51a.05
51a.06
TO FIG. 52b
51a.07-51b
51a.08-51b
K
T
DG
STEP SPC + 1 (P)
93j.01
(-)A2/R3-W1 (BLOCKED)(P)
52e.02
STEP SPC -1 (P)
93j.04
STAGES 1-3 OF SPC
12 CLAMP 139e.12

FIG. 51a

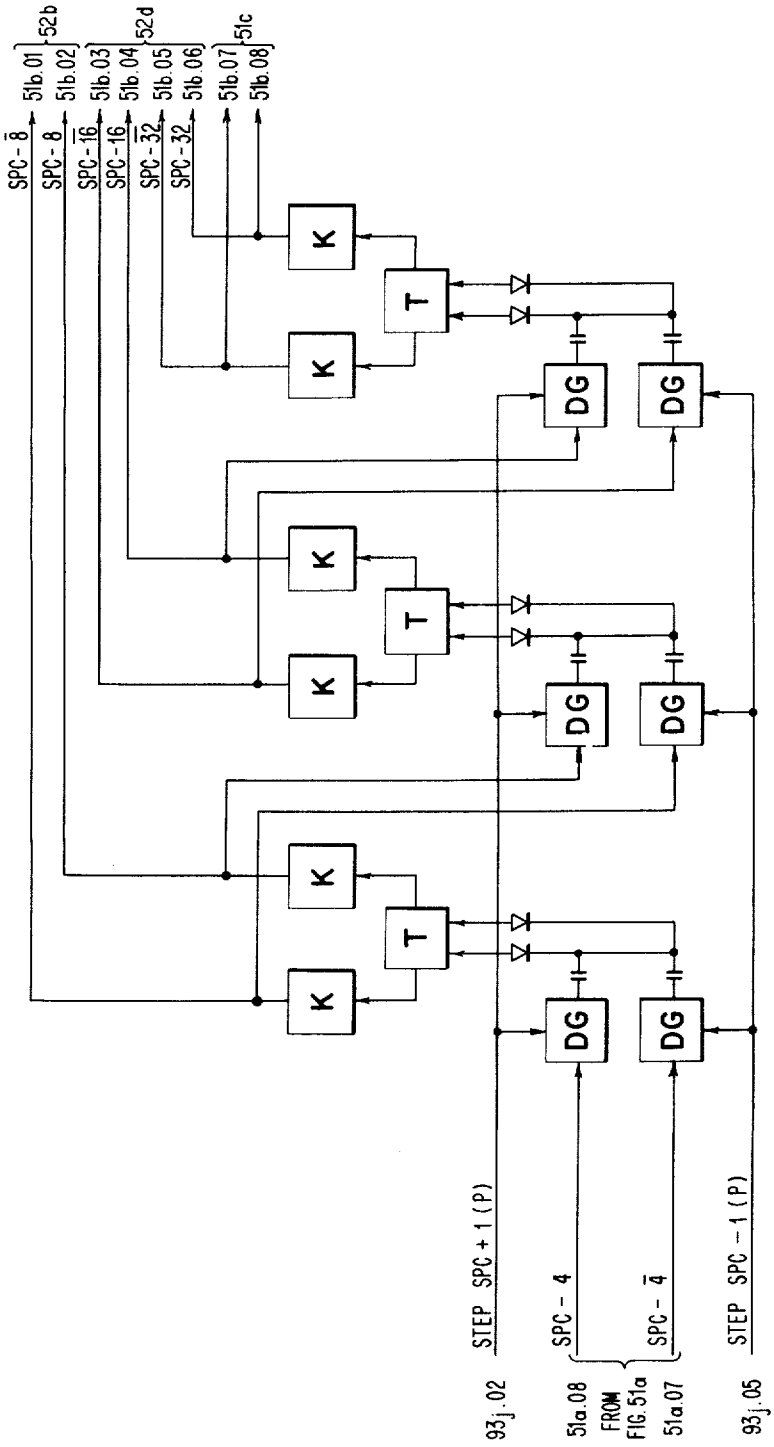


FIG. 51b

STAGES 4-6 OF SPC

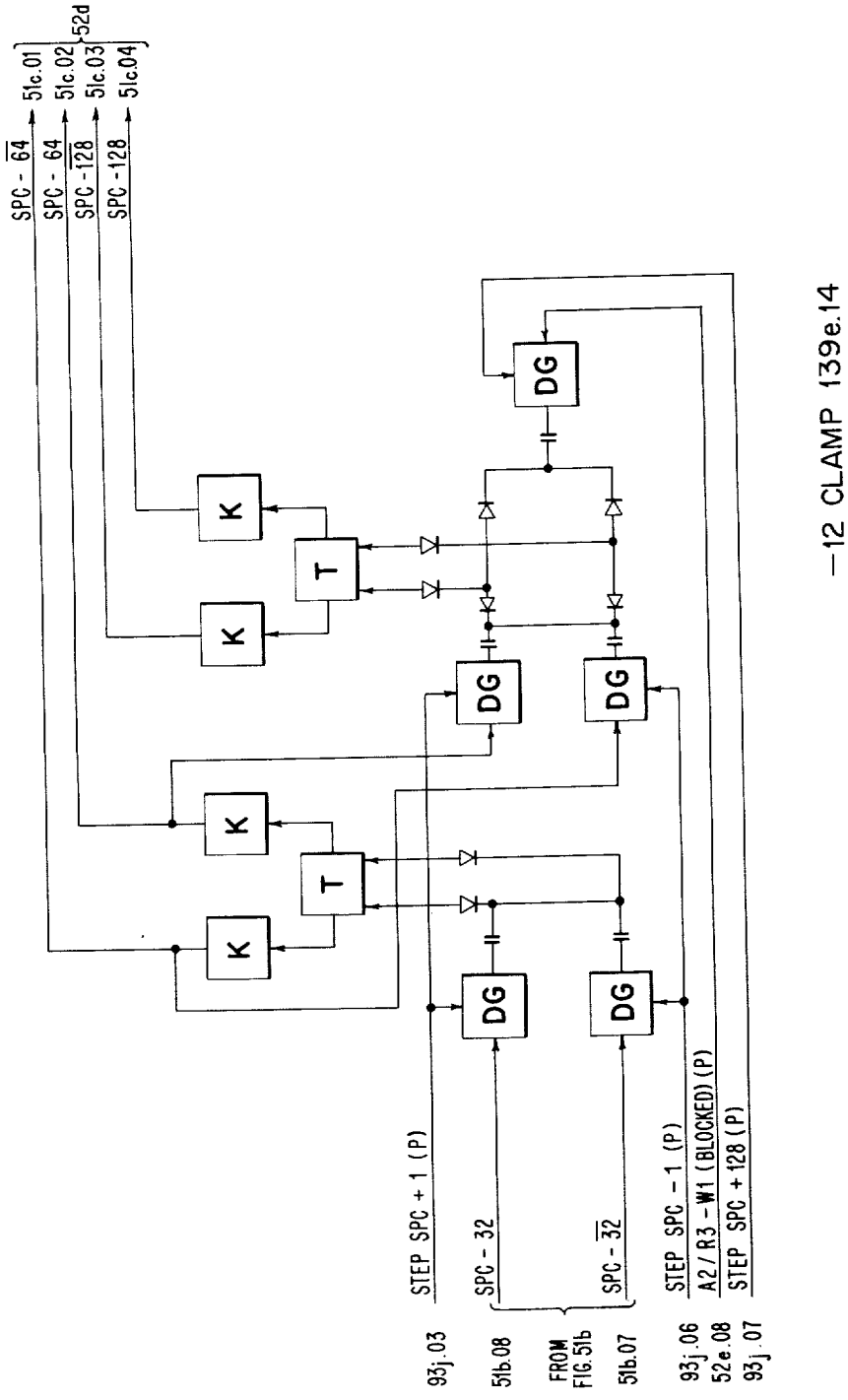
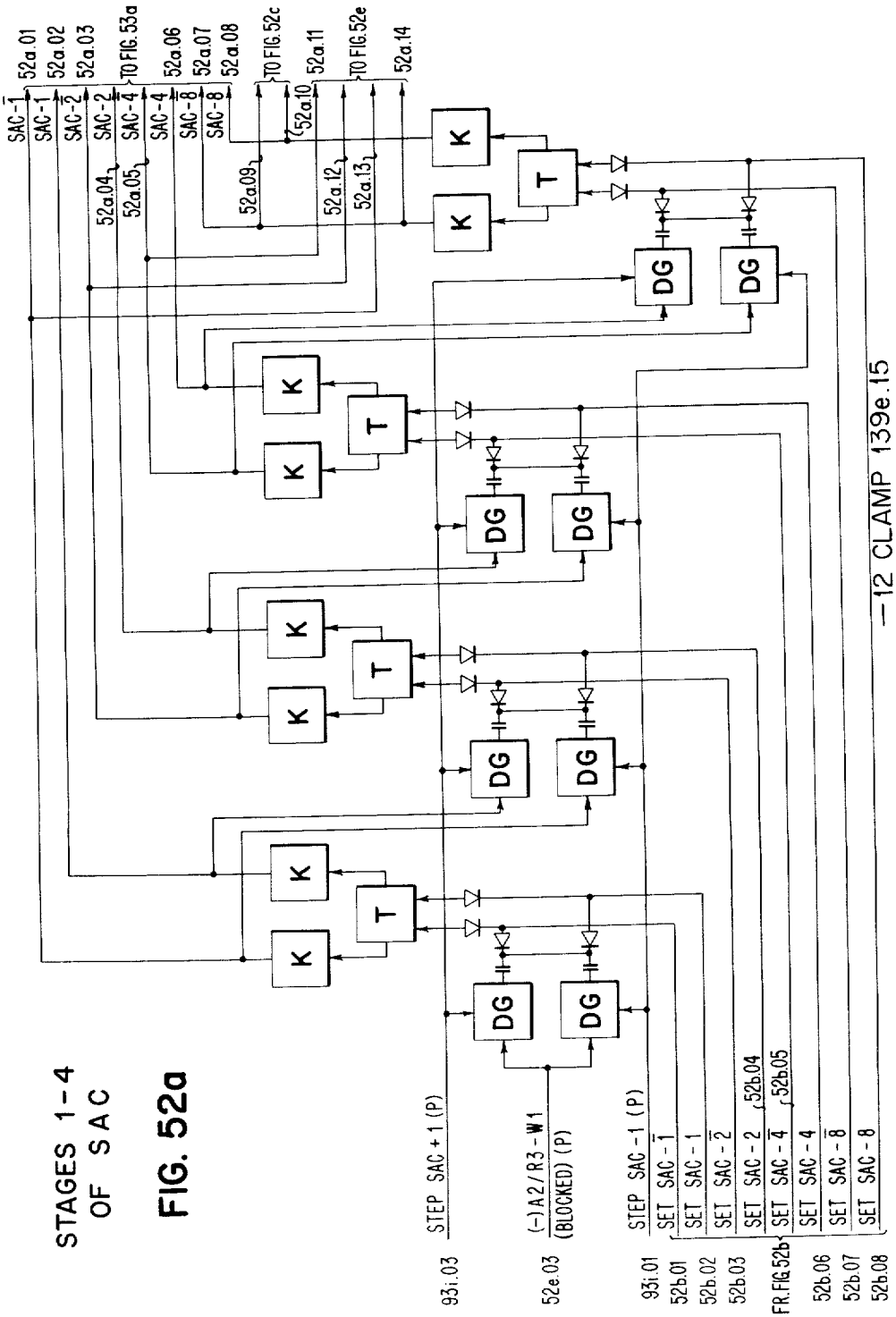

SPC - 64
SPC - 64
SPC -128
SPC -128
51c.01
51c.02
51c.03
51c.04
52d
K
T
DG
STEP SPC + 1 (P)
SPC - 32
SPC - 32
STEP SPC - 1 (P)
A2/R3 - W1 (BLOCKED) (P)
STEP SPC + 128 (P)
93j.03
51b.08
FROM FIG. 51b
51b.07
93j.06
52e.08
93j.07
STAGES 7-8 OF SPC
-12 CLAMP 139e.14

FIG. 51c

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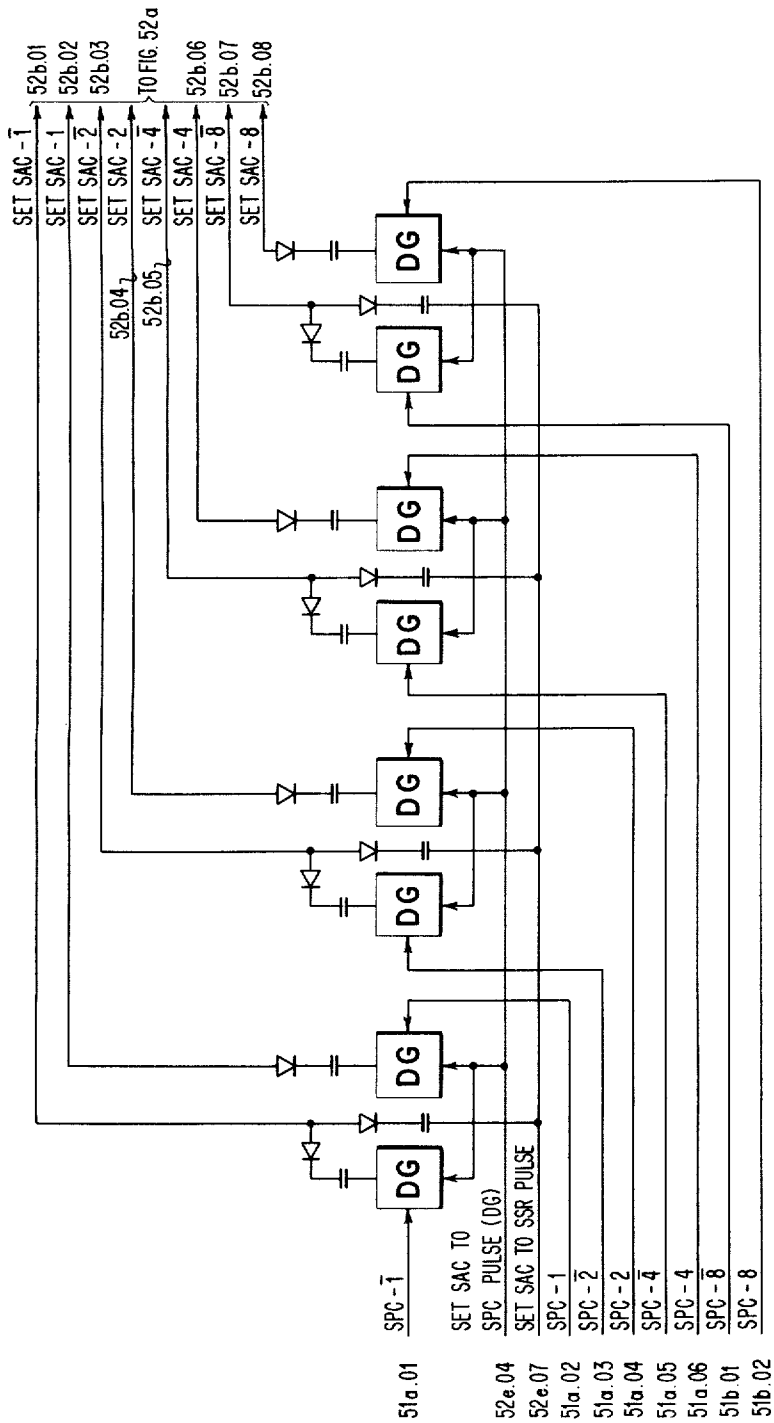


STAGES 1-4 OF SAC

FIG. 52a

FIG. 52b

STAGES 1-4 OF SAC



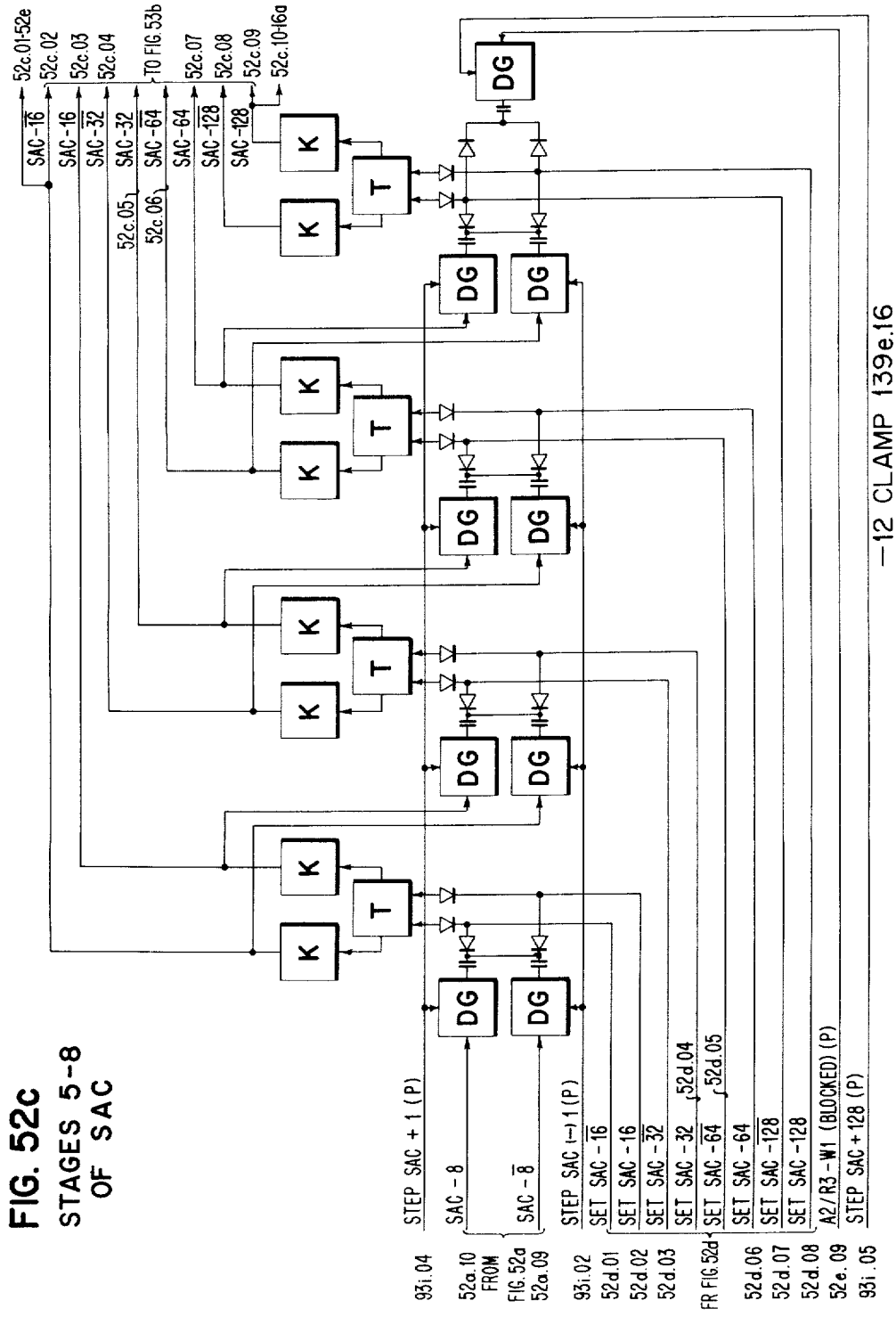
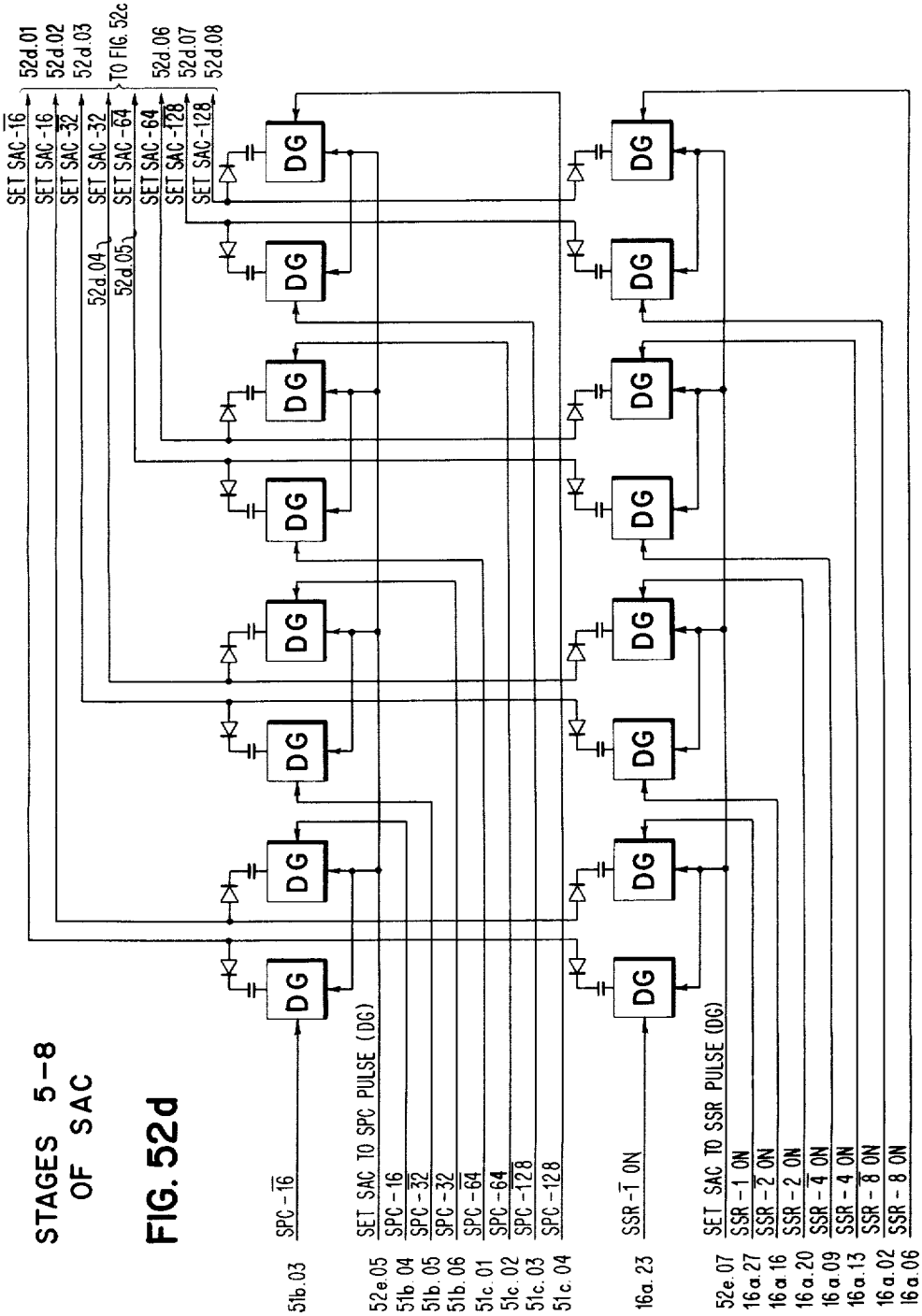


FIG. 52c
STAGES 5-8 OF SAC

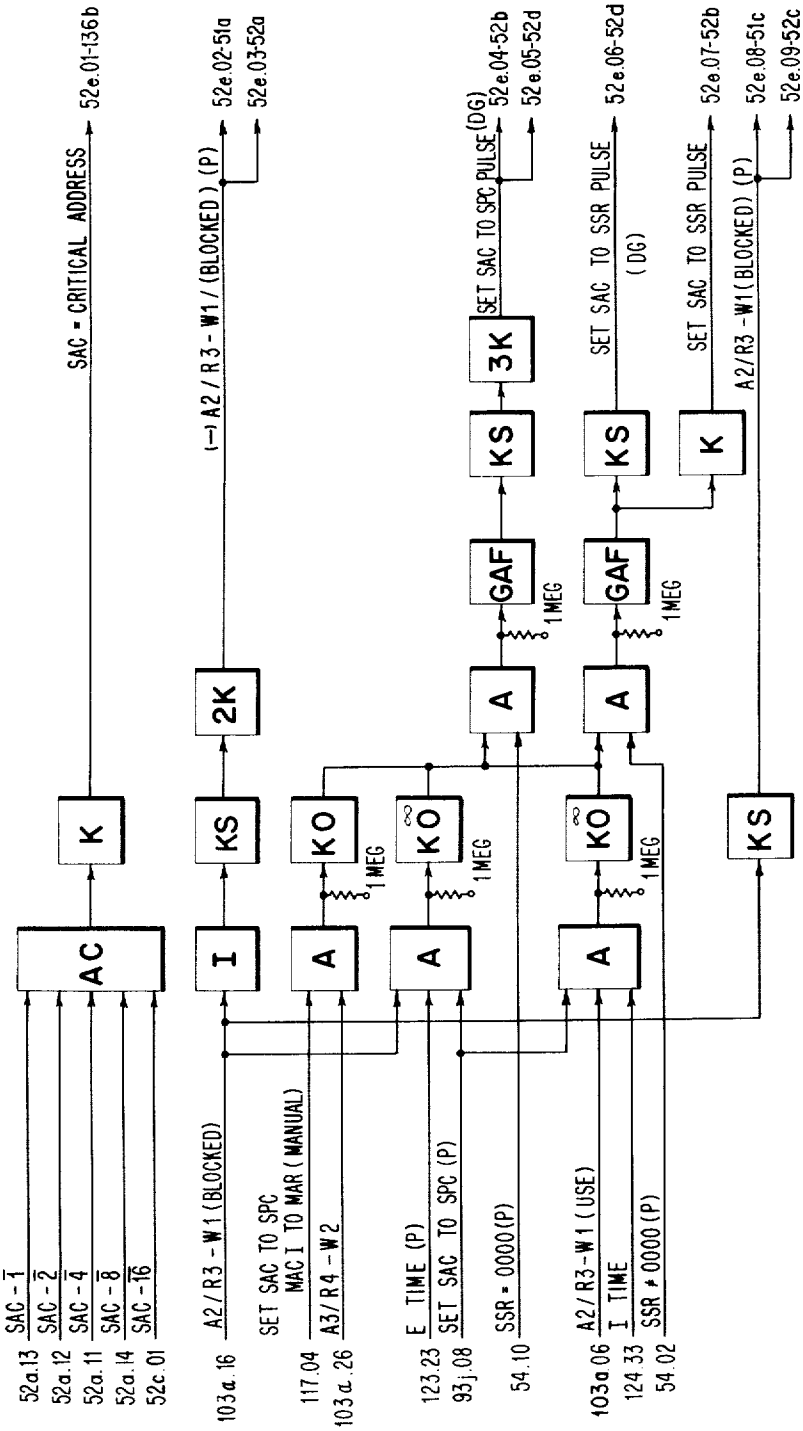


STAGES 5-8 OF SAC

FIG. 52d

FIG. 52e

SAC CONTROLS



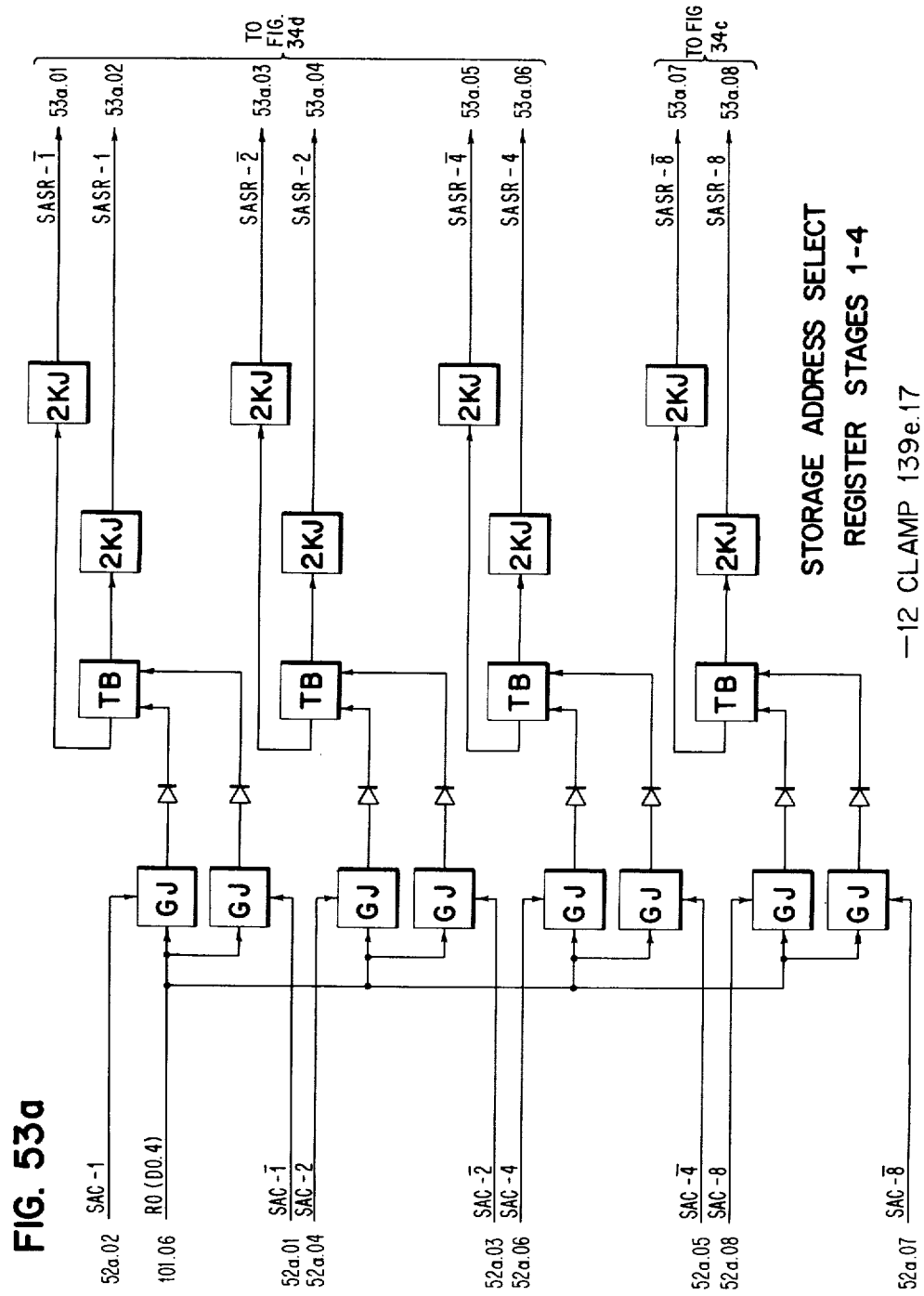

TO FIG. 34d
TO FIG 34c
SASR - $\overline{1}$
SASR - 1
SASR - $\overline{2}$
SASR - 2
SASR - $\overline{4}$
SASR - 4
SASR - $\overline{8}$
SASR - 8
53a.01
53a.02
53a.03
53a.04
53a.05
53a.06
53a.07
53a.08
2KJ
TB
GJ
STORAGE ADDRESS SELECT
REGISTER STAGES 1-4
—12 CLAMP 139e.17
SAC - 1
RO (DO.4)
SAC - $\overline{1}$
SAC - 2
SAC - $\overline{2}$
SAC - 4
SAC - $\overline{4}$
SAC - 8
SAC - $\overline{8}$
52a.02
101.06
52a.01
52a.04
52a.03
52a.06
52a.05
52a.08
52a.07

FIG. 53a

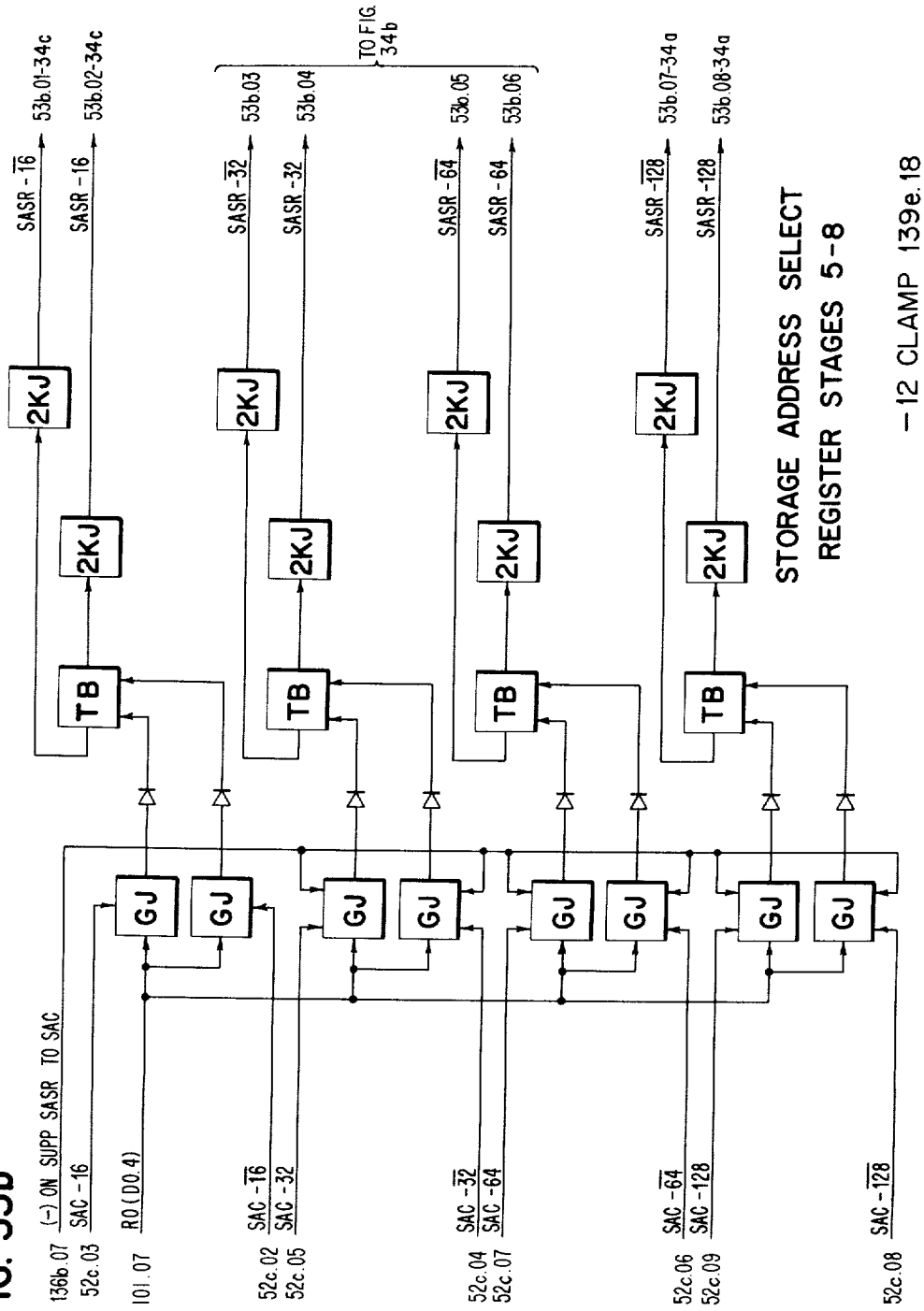
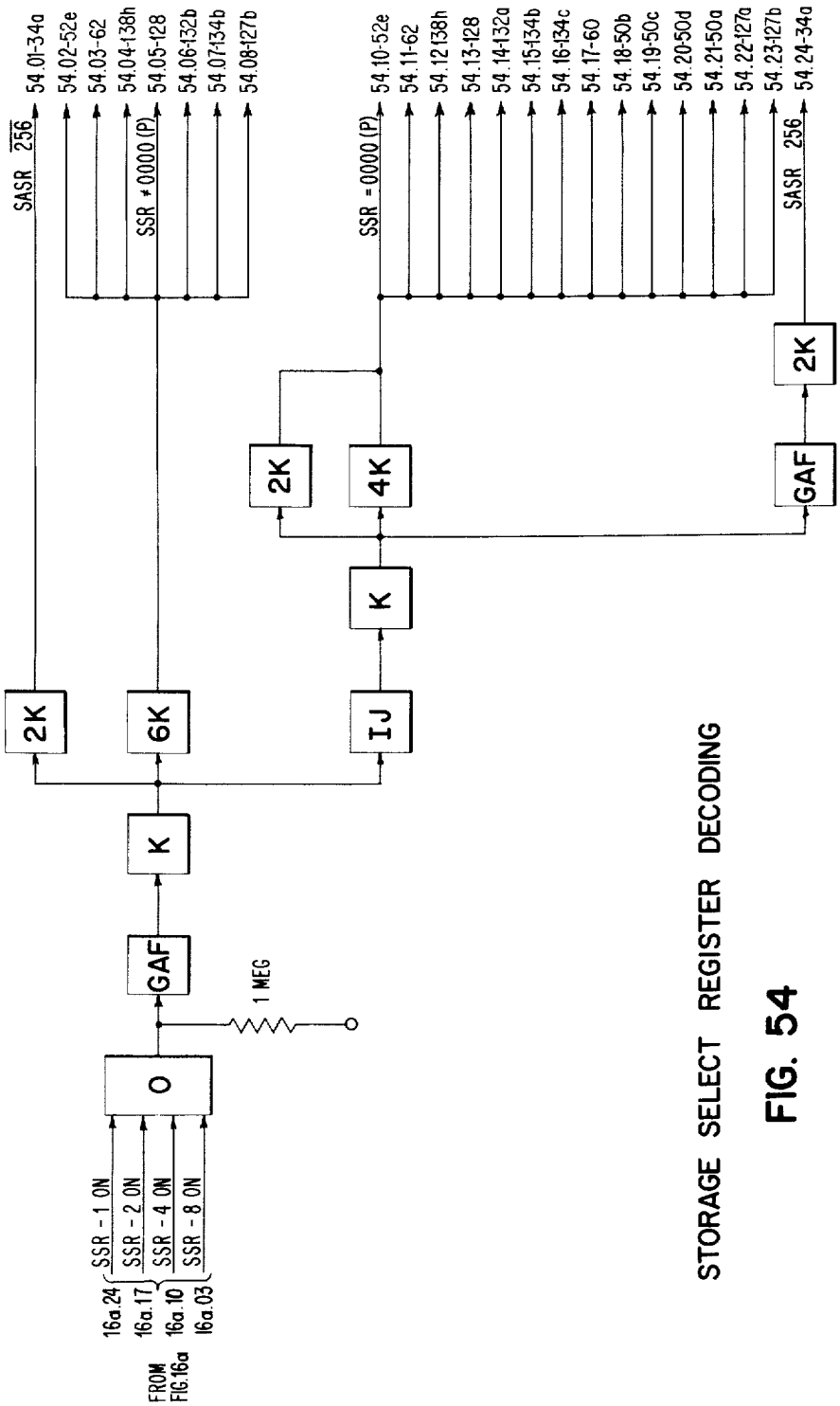

TO FIG. 34b
53b.01-34c
53b.02-34c
53b.03
53b.04
53b.05
53b.06
53b.07-34a
53b.08-34a
SASR - 16
SASR - 16
SASR - 32
SASR - 32
SASR - 64
SASR - 64
SASR - 128
SASR - 128
2KJ
TB
GJ
STORAGE ADDRESS SELECT
REGISTER STAGES 5-8
- 12 CLAMP 139e.18
136b.07 (-) ON SUPP SASR TO SAC
52c.03 SAC - 16
101.07 RO (D0.4)
52c.02 SAC - 16
52c.05 SAC - 32
52c.04 SAC - 32
52c.07 SAC - 64
52c.06 SAC - 64
52c.09 SAC - 128
52c.08 SAC - 128

FIG. 53b



STORAGE SELECT REGISTER DECODING

FIG. 54

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FIG. 55a SSR DECODER 1-8

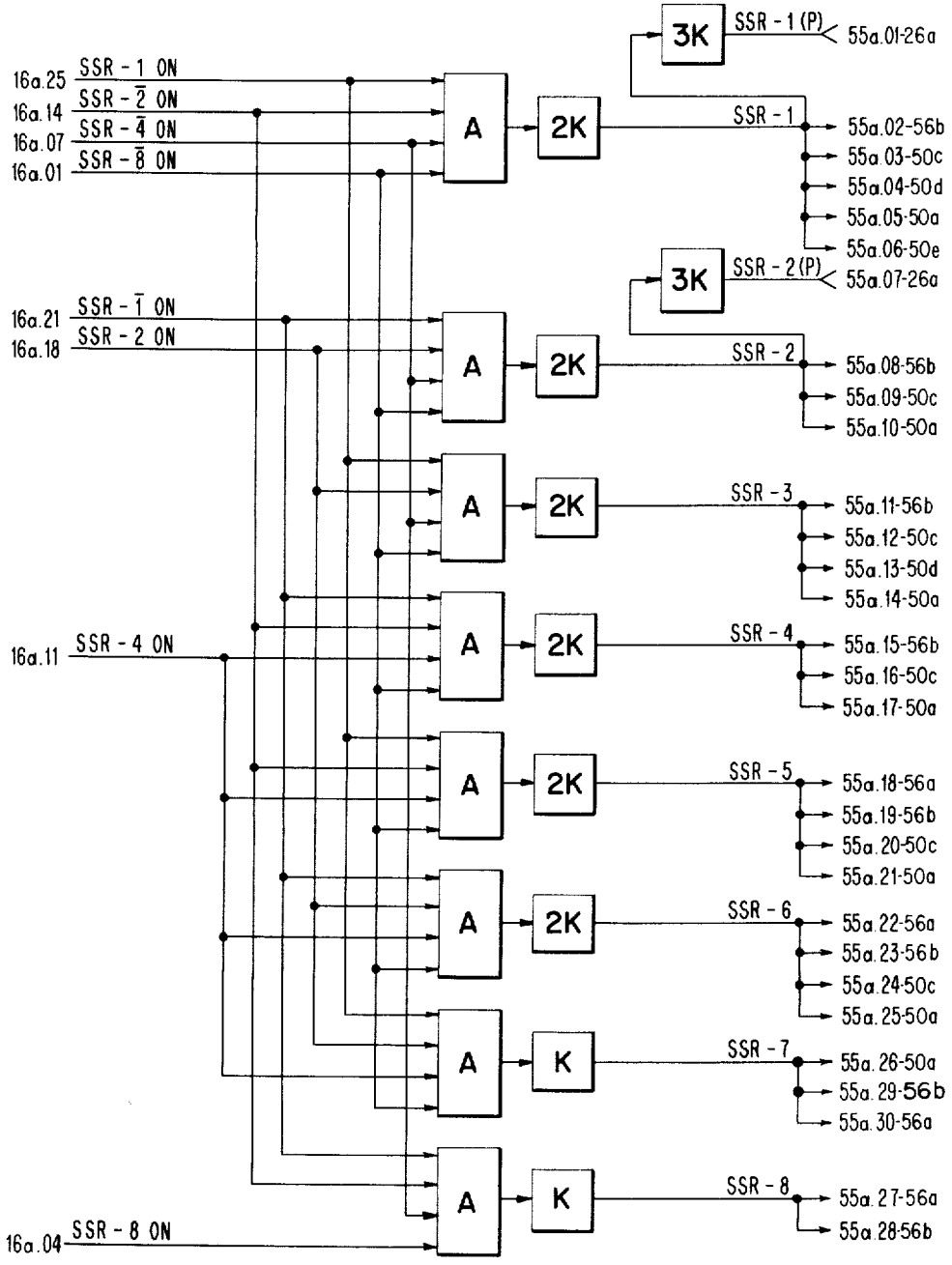
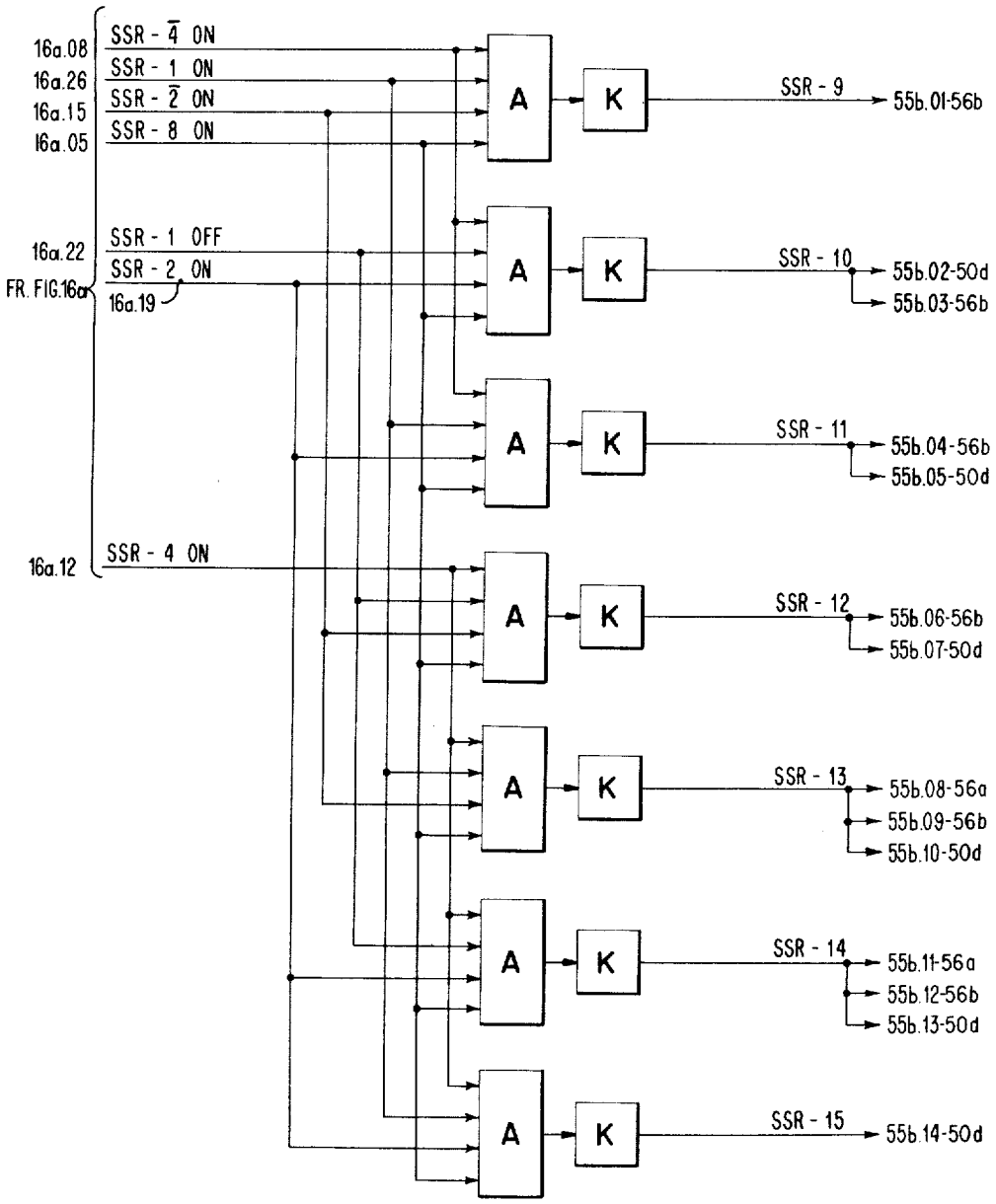


FIG. 55b SSR DECODER 9-15



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FIG.56a

SET BIT ROUTING CONTROLS

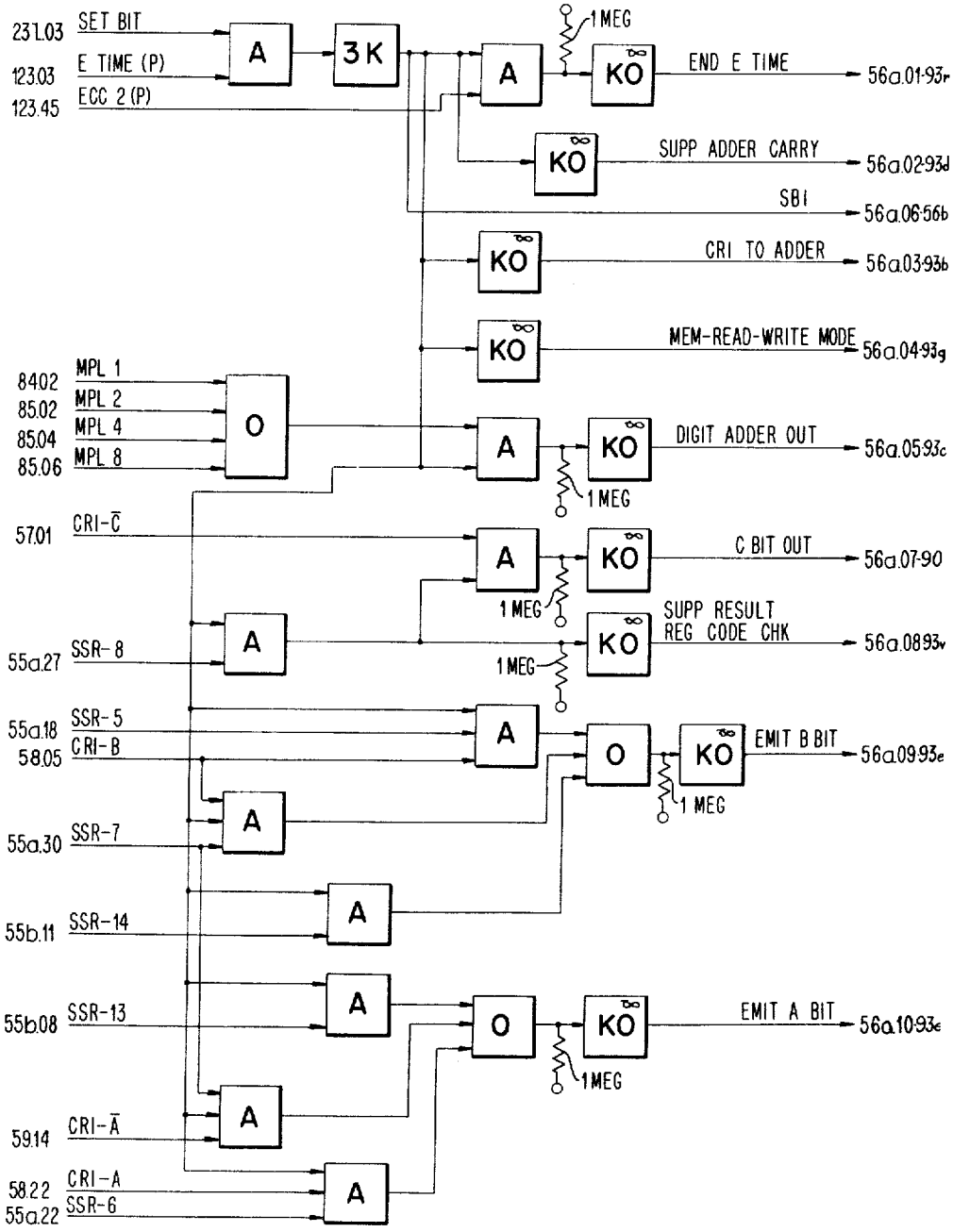


FIG. 56b

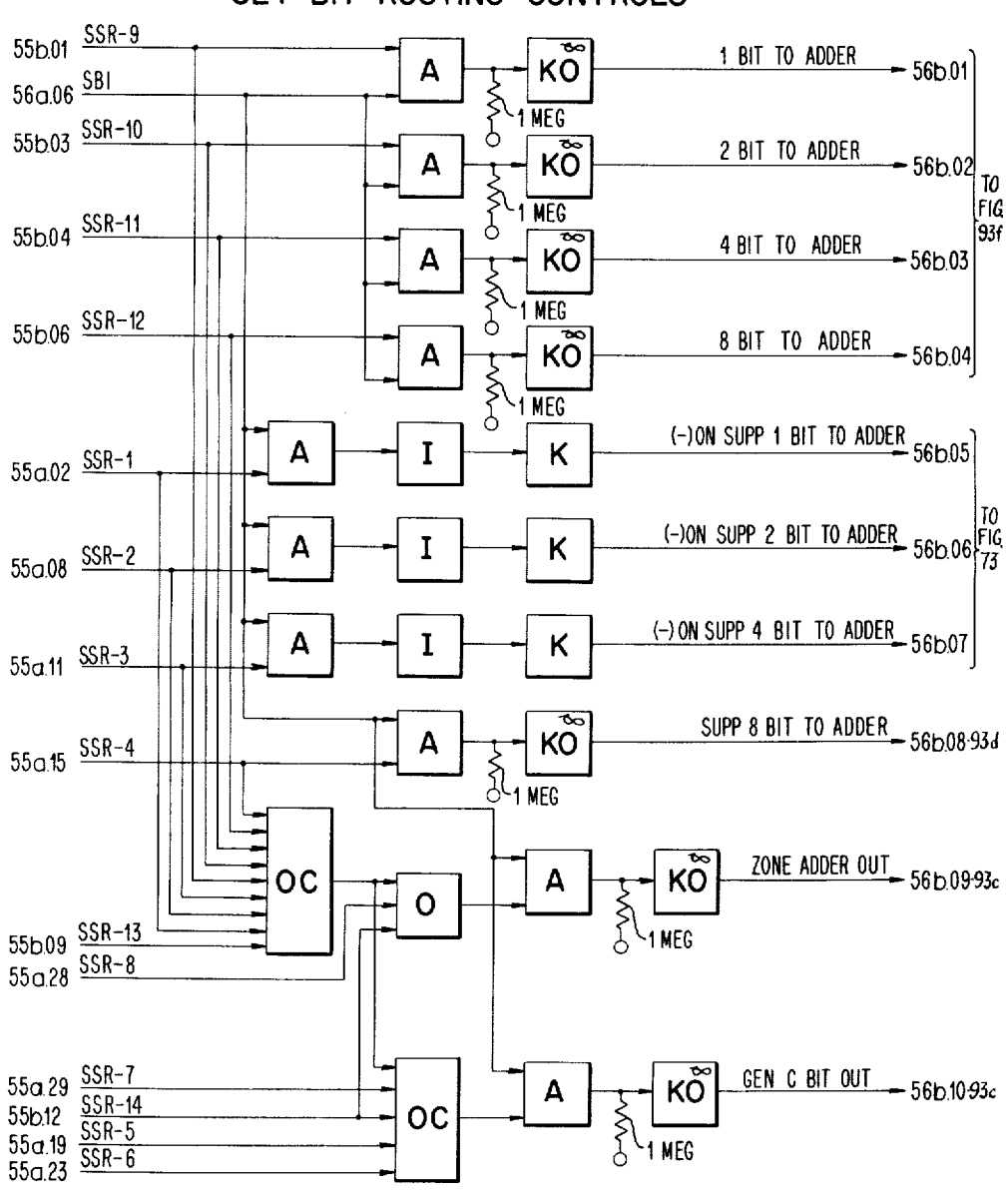

SET BIT ROUTING CONTROLS
55b.01 SSR-9
56a.06 SBI
55b.03 SSR-10
55b.04 SSR-11
55b.06 SSR-12
55a.02 SSR-1
55a.08 SSR-2
55a.11 SSR-3
55a.15 SSR-4
55b.09 SSR-13
55a.28 SSR-8
55a.29 SSR-7
55b.12 SSR-14
55a.19 SSR-5
55a.23 SSR-6
A
I
K
KO
OC
O
1 MEG
1 BIT TO ADDER
2 BIT TO ADDER
4 BIT TO ADDER
8 BIT TO ADDER
(-)ON SUPP 1 BIT TO ADDER
(-)ON SUPP 2 BIT TO ADDER
(-)ON SUPP 4 BIT TO ADDER
SUPP 8 BIT TO ADDER
ZONE ADDER OUT
GEN C BIT OUT
56b.01
56b.02
56b.03
56b.04
56b.05
56b.06
56b.07
56b.08-93d
56b.09-93c
56b.10-93c
TO FIG. 93f
TO FIG. 73

FIG.57

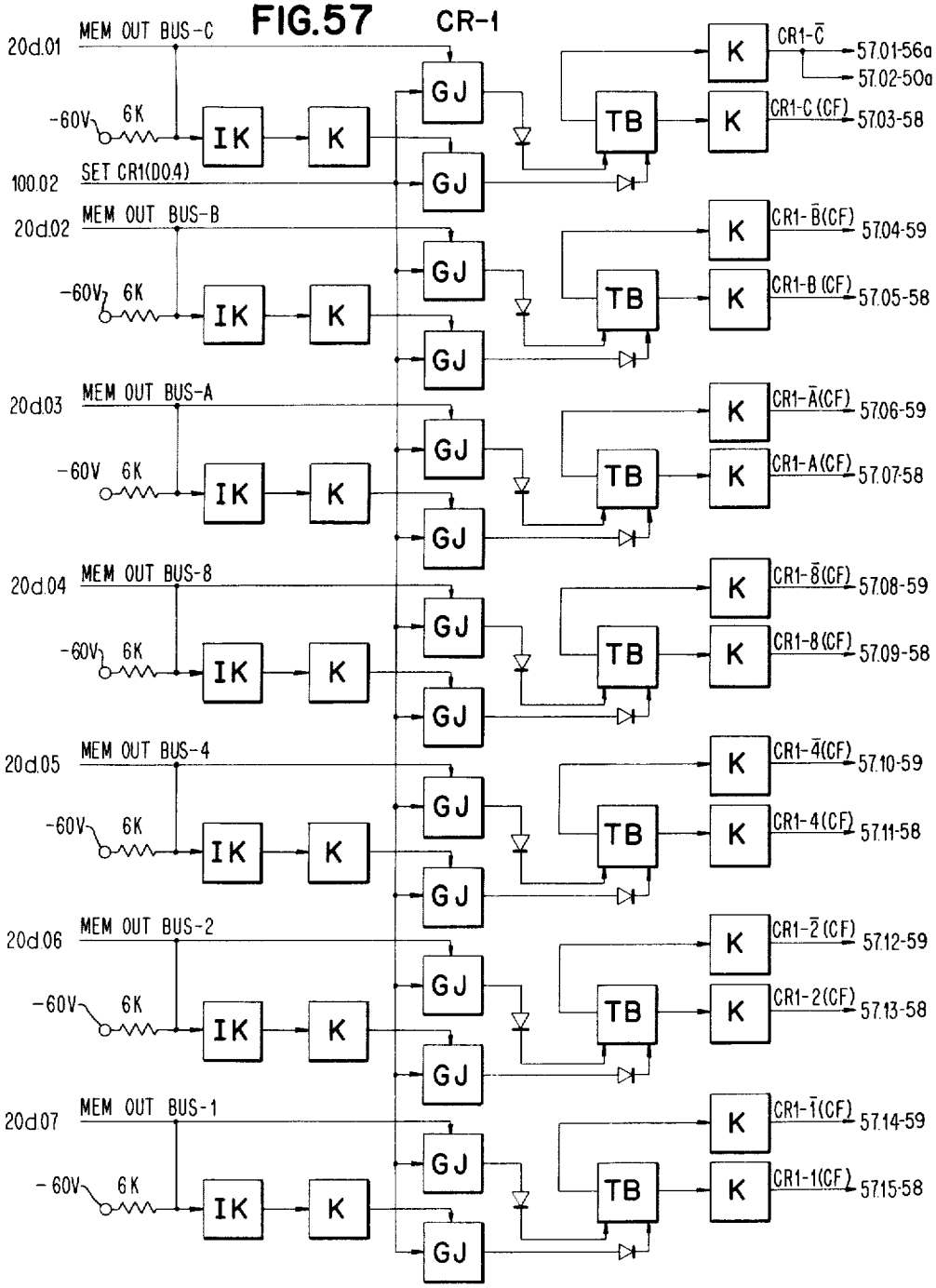

CR-1
20d.01
MEM OUT BUS-C
-60V
6K
IK
K
GJ
TB
CR1-C̄
57.01-56a
57.02-50a
CR1-C (CF)
57.03-58
100.02
SET CR1(D0.4)
20d.02
MEM OUT BUS-B
CR1-B̄(CF)
57.04-59
CR1-B (CF)
57.05-58
20d.03
MEM OUT BUS-A
CR1-Ā(CF)
57.06-59
CR1-A(CF)
57.07-58
20d.04
MEM OUT BUS-8
CR1-8̄(CF)
57.08-59
CR1-8(CF)
57.09-58
20d.05
MEM OUT BUS-4
CR1-4̄(CF)
57.10-59
CR1-4(CF)
57.11-58
20d.06
MEM OUT BUS-2
CR1-2̄(CF)
57.12-59
CR1-2(CF)
57.13-58
20d.07
MEM OUT BUS-1
CR1-1̄(CF)
57.14-59
CR1-1(CF)
57.15-58

FIG.58
SHEET 1 of 2

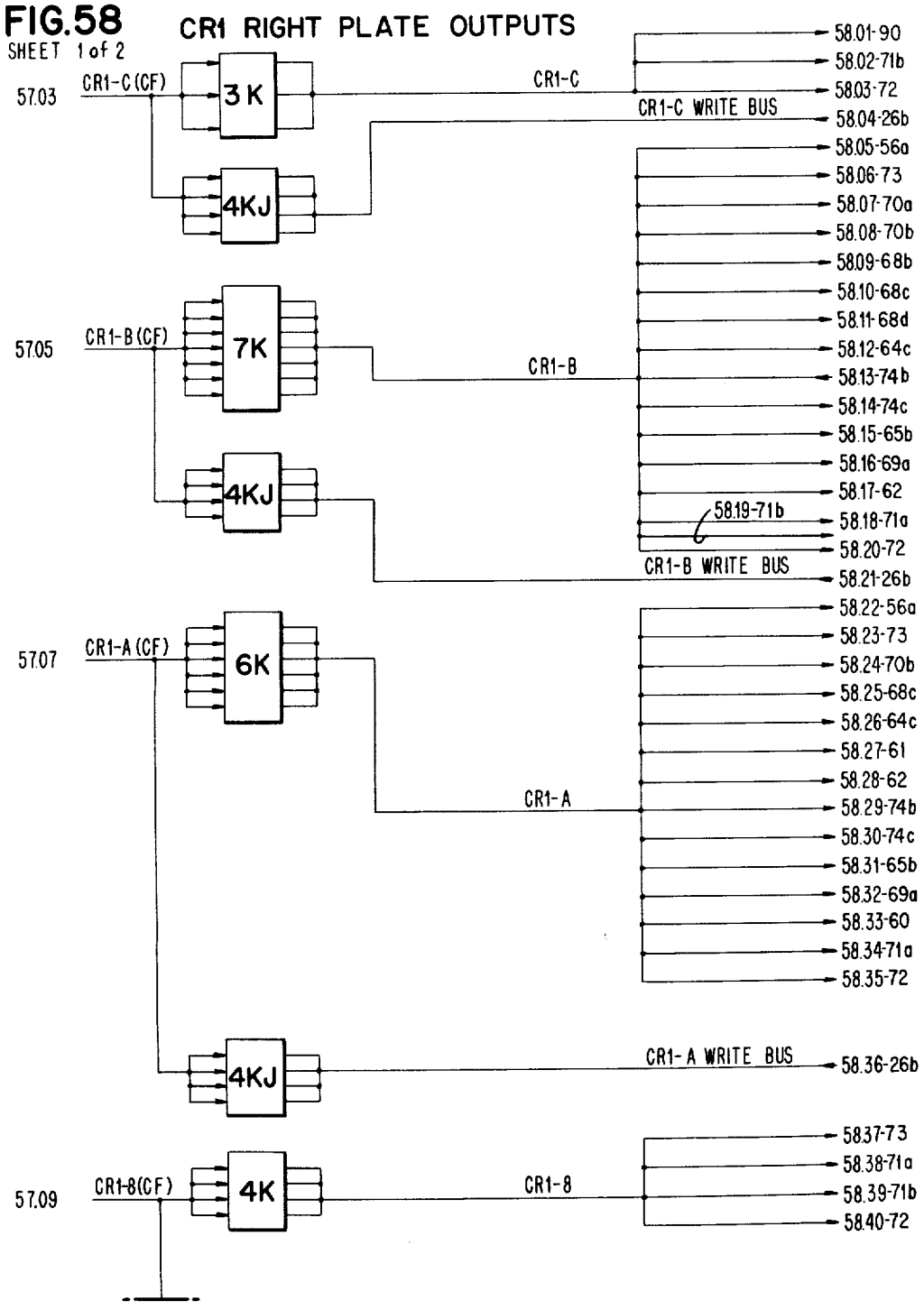


FIG.58
SHEET 2 of 2

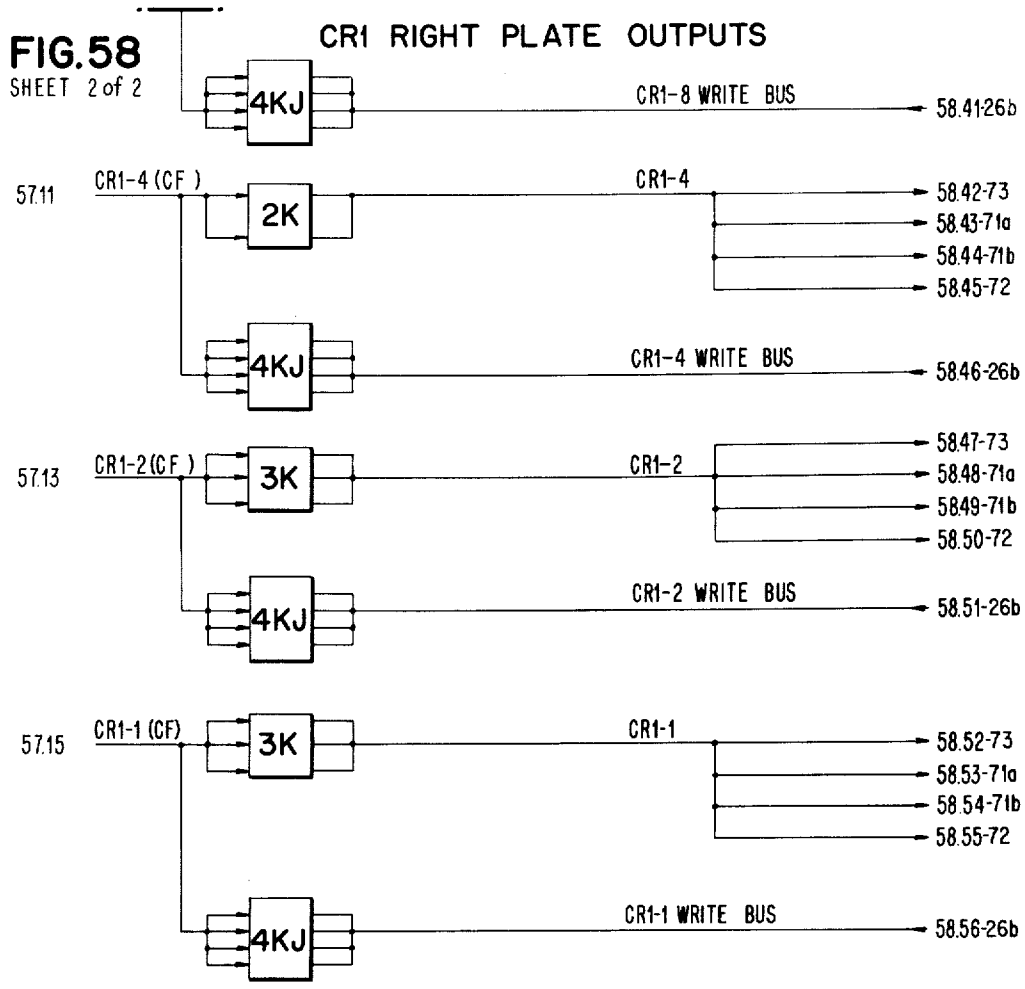


FIG. 59 CR1 LEFT PLATE OUTPUTS

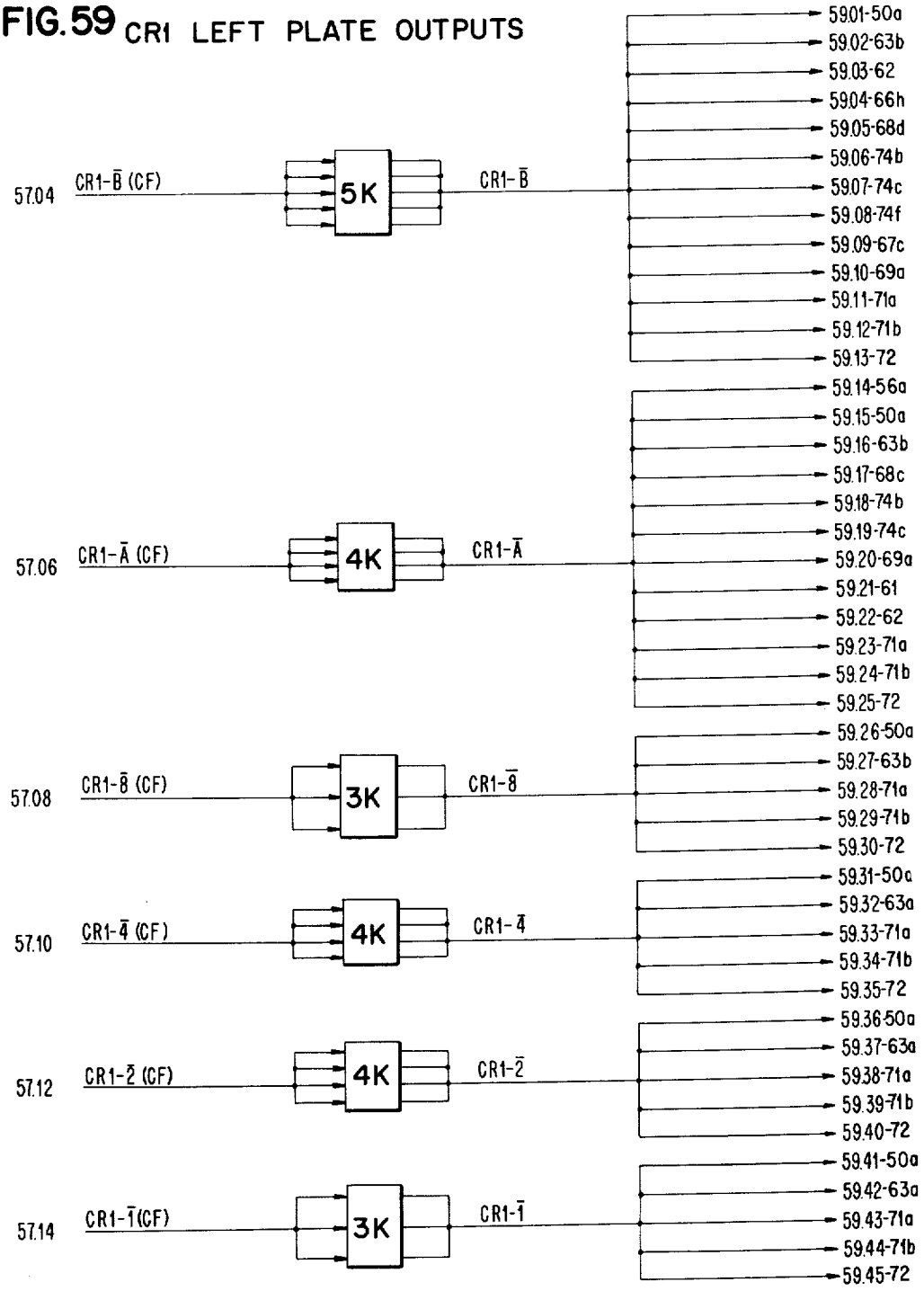
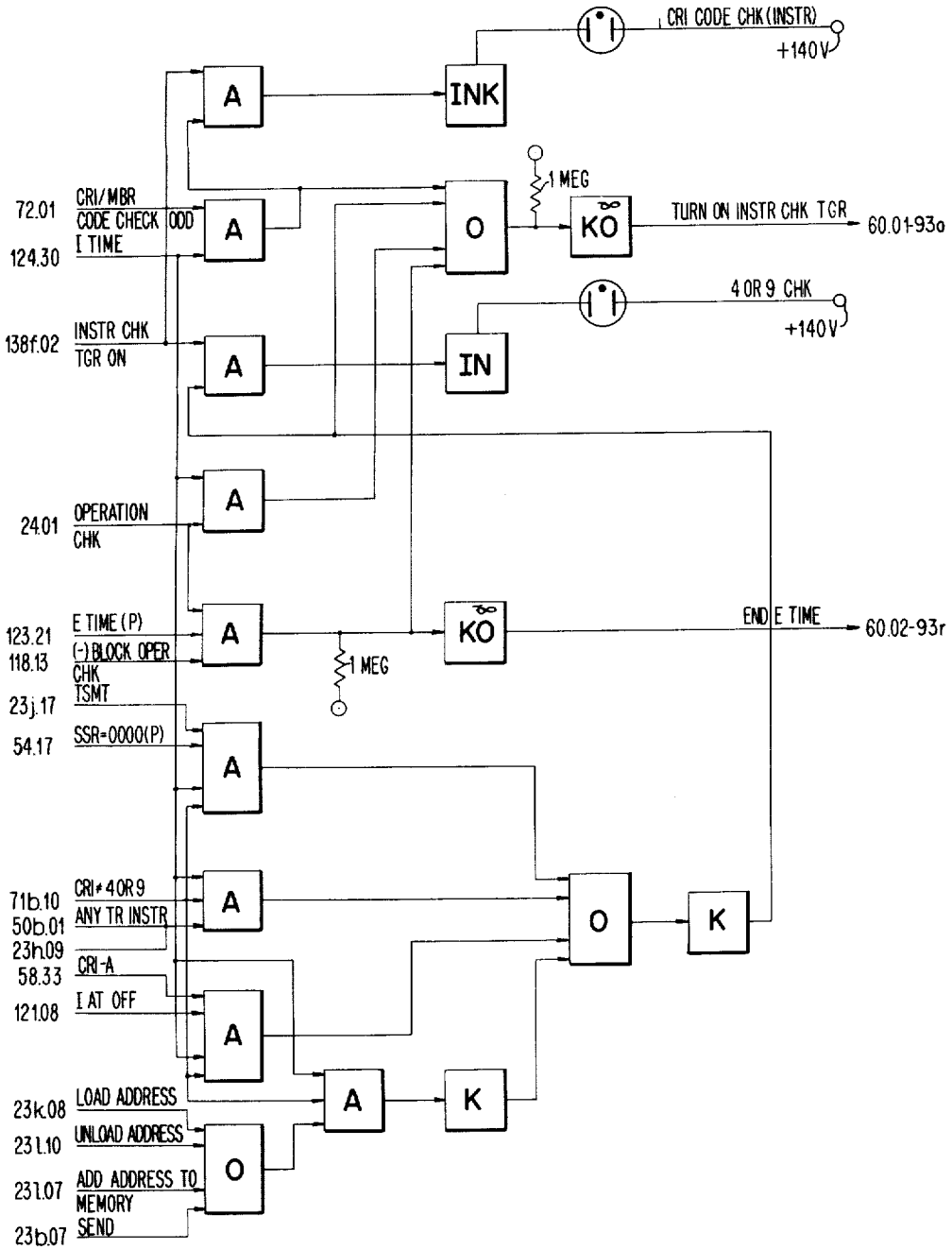


FIG. 60 INSTRUCTION CHECK CIRCUITS



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FIG. 61

I TIME ROUTING CONTROLS

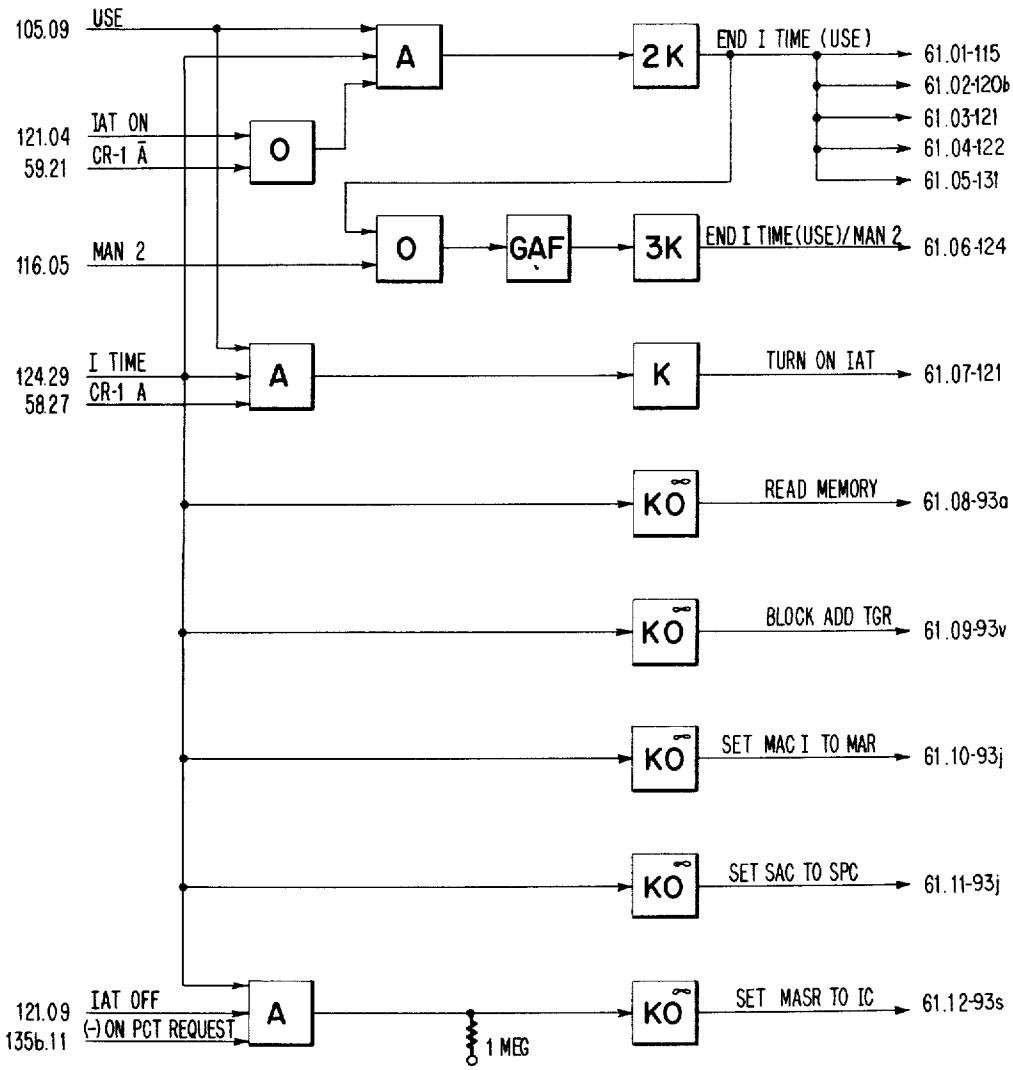
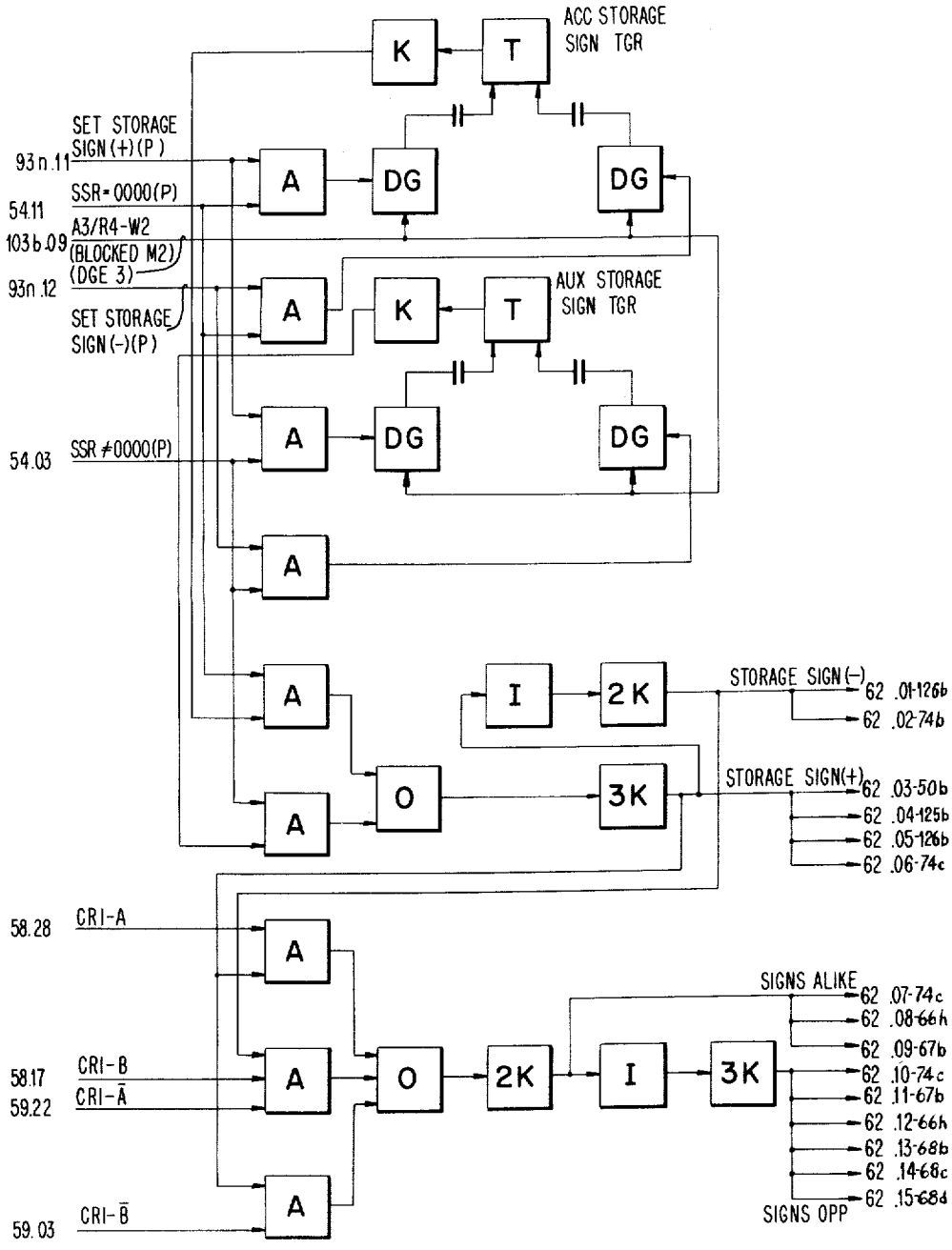


FIG. 62 STORAGE SIGN TGRS. & CONTROLS



—12 CLAMP 139e.23

FIG.63a

INTER REG CHECK ROUTING 1

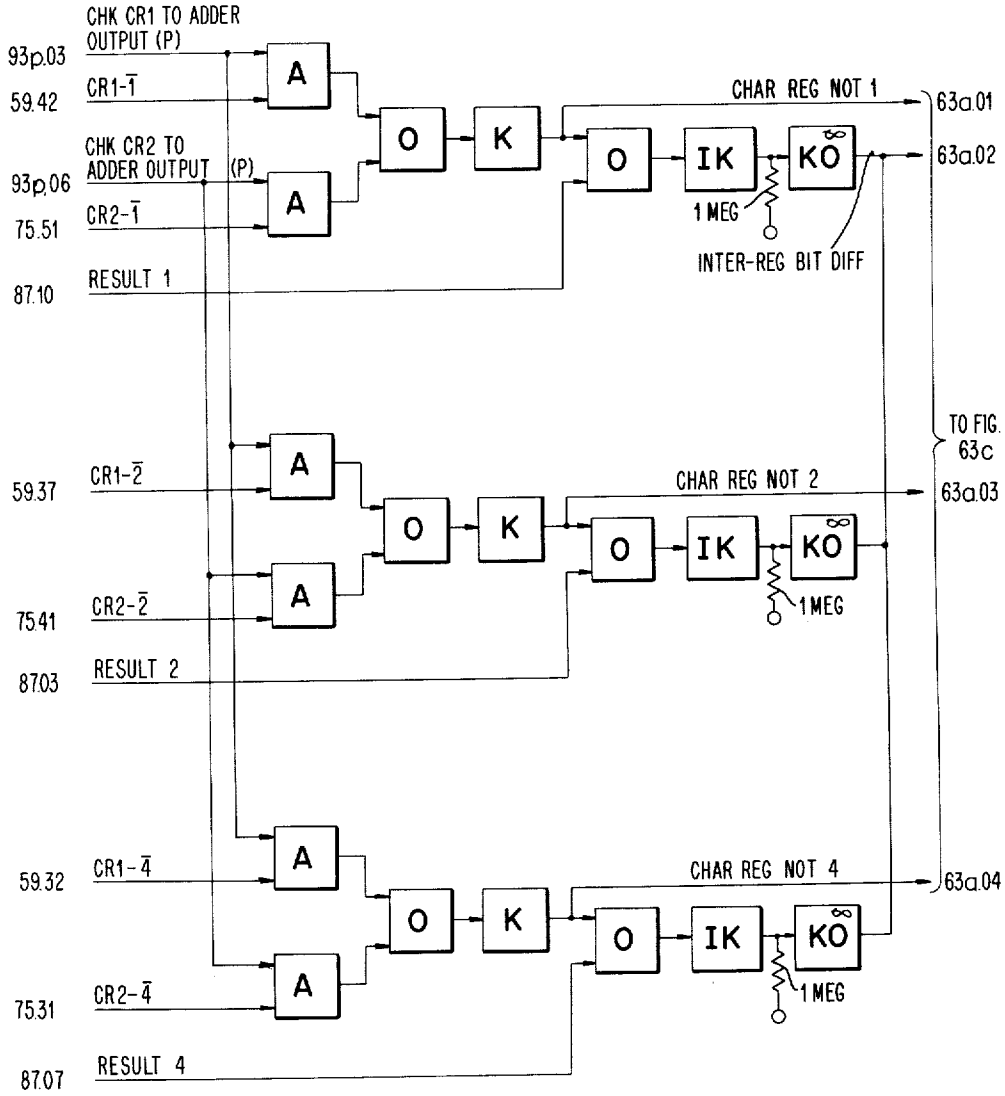
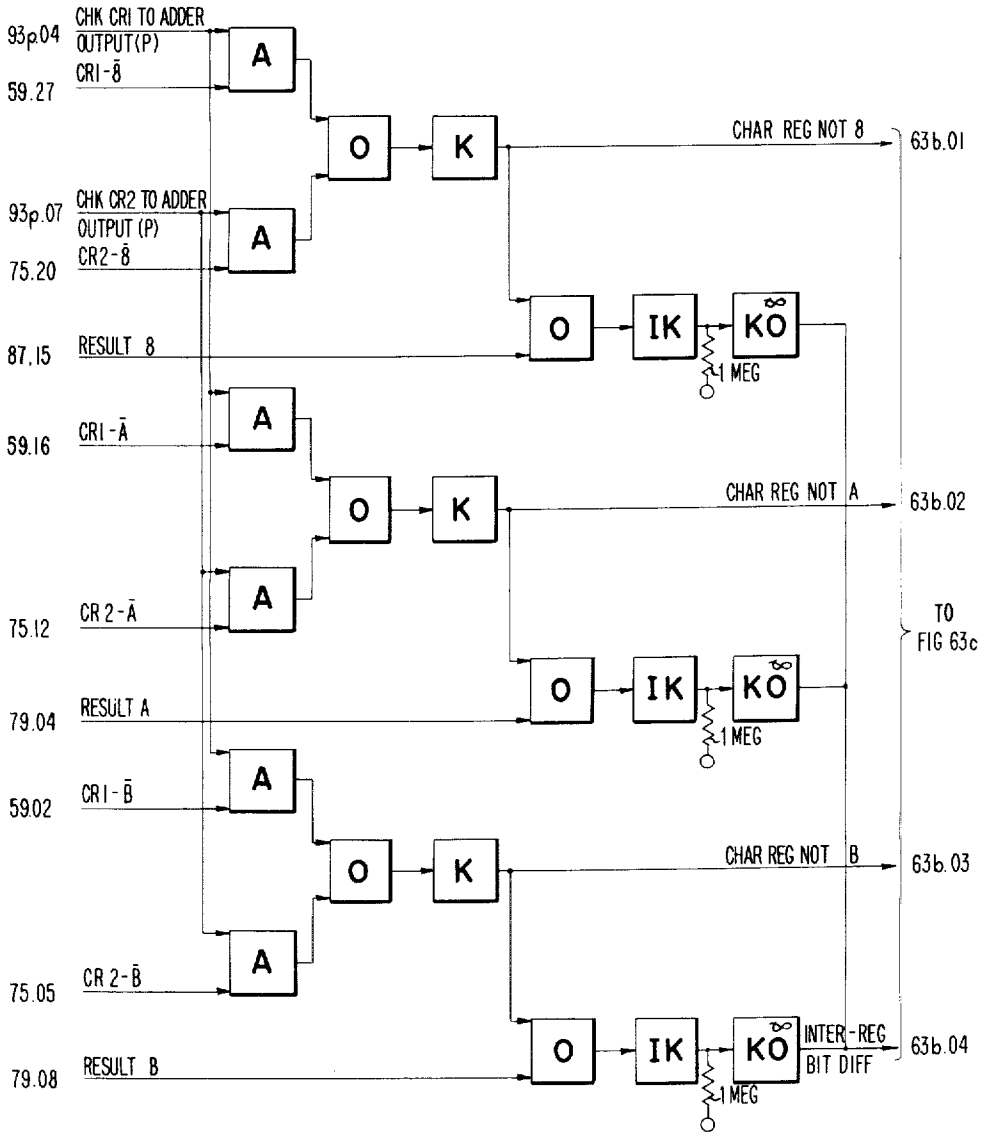


FIG. 63b

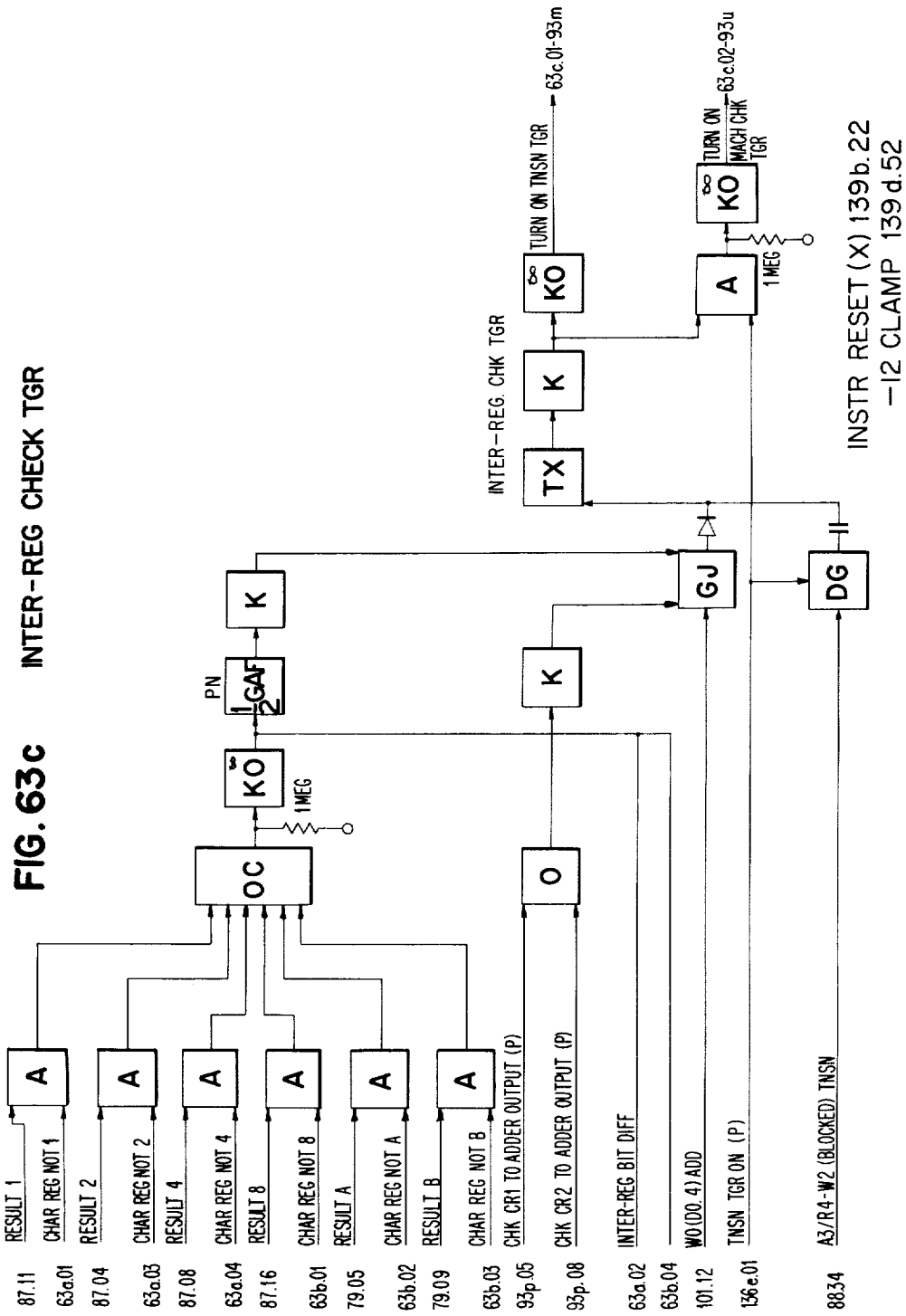
INTER-REG CHECK ROUTING 2



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FIG.64a

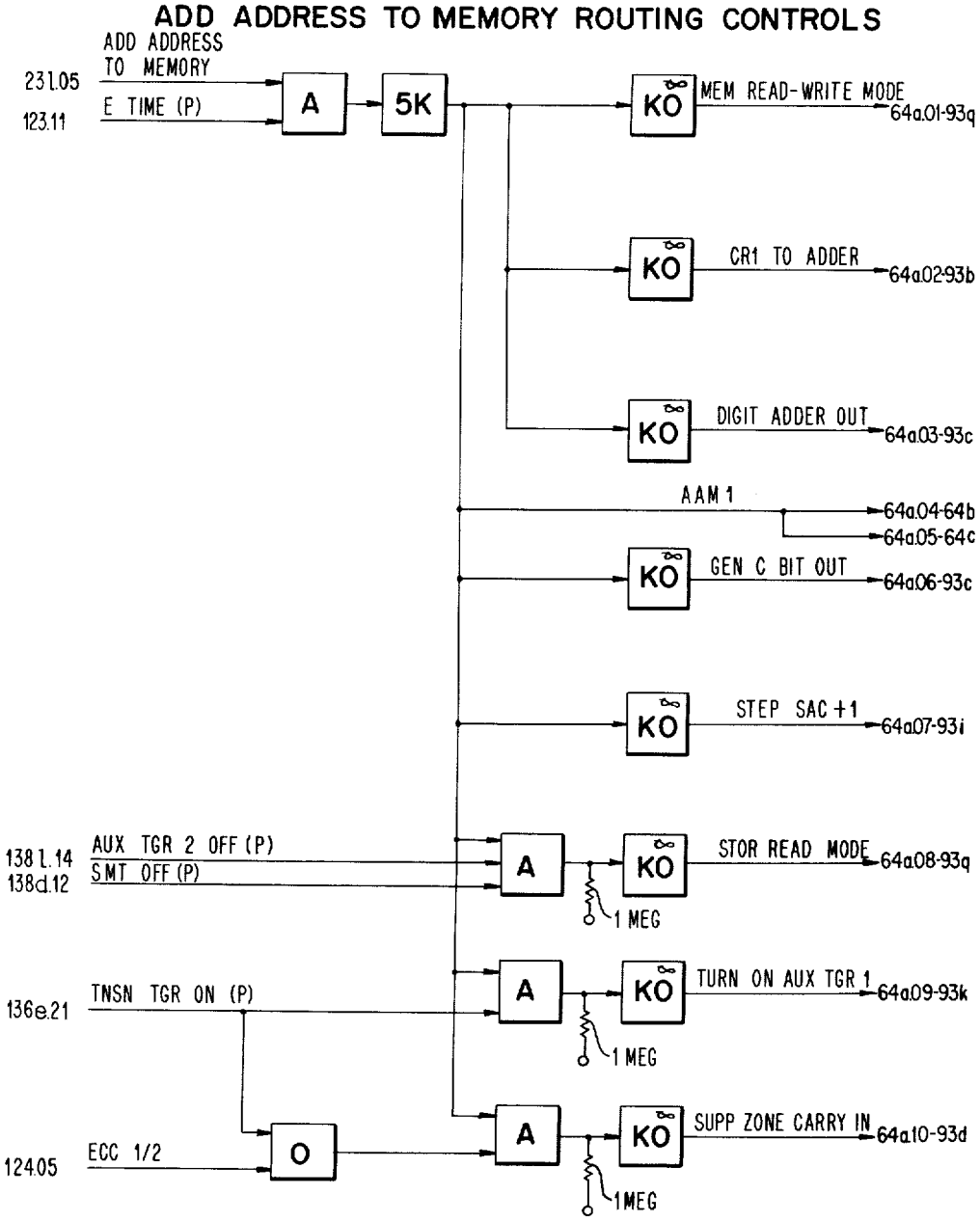
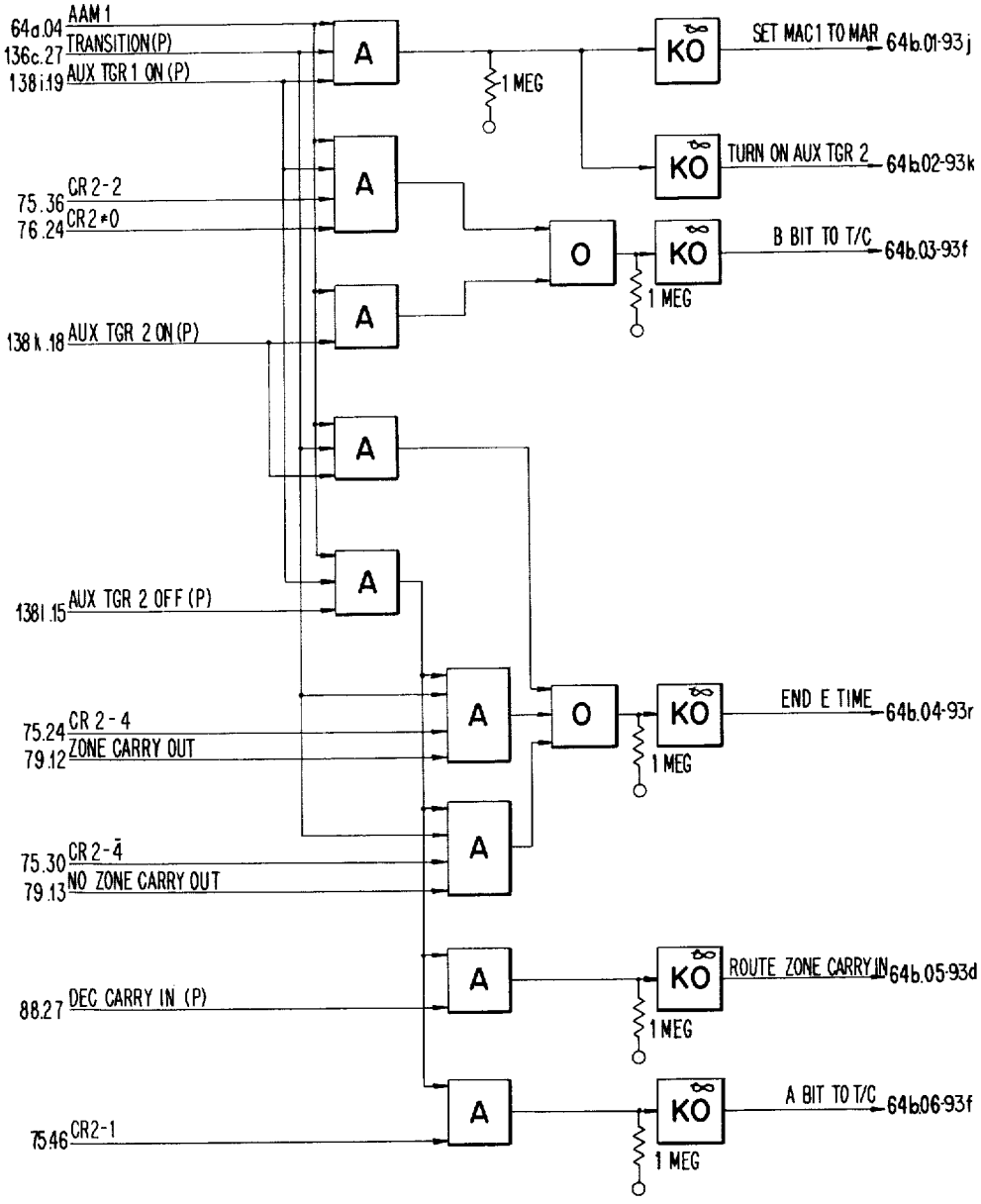


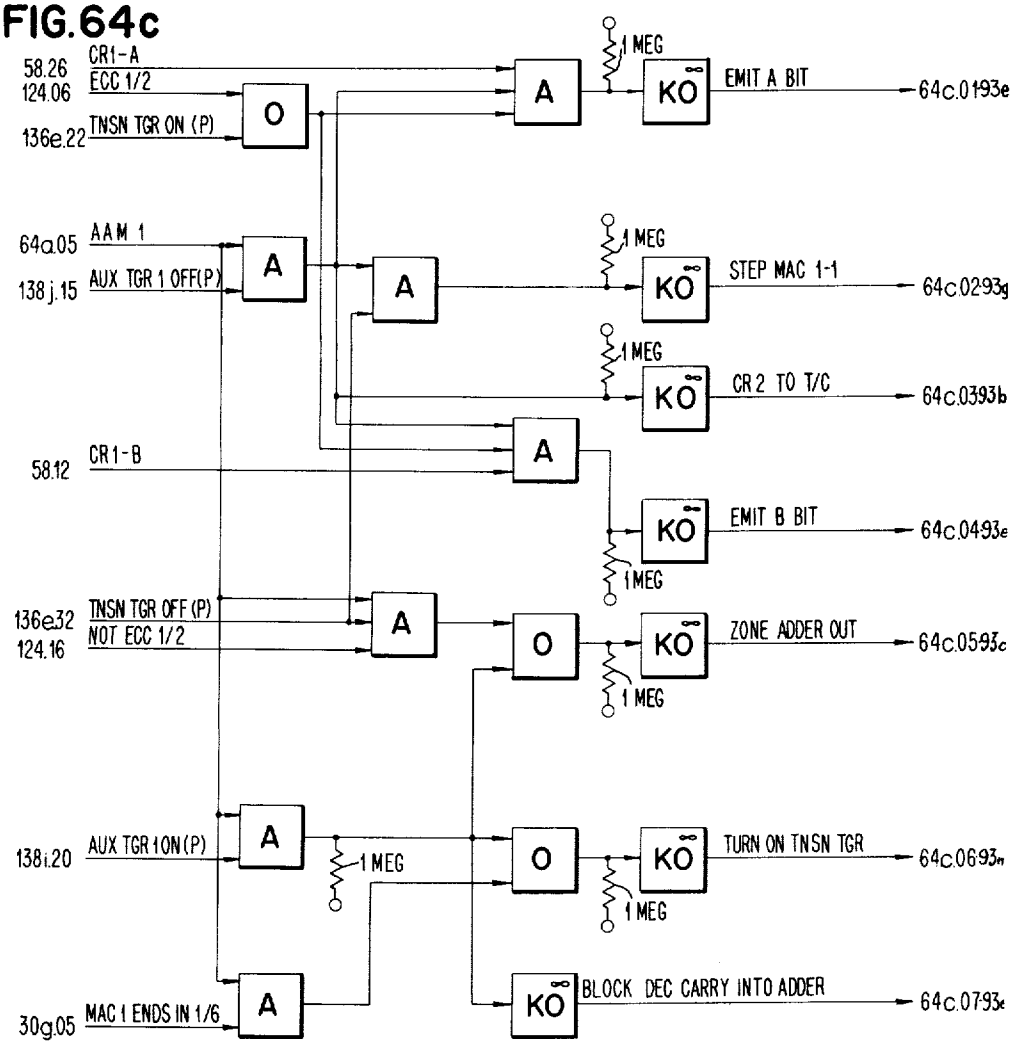
FIG.64b

ADD ADDRESS TO MEMORY ROUTING CONTROLS



ADD ADDRESS TO MEMORY ROUTING CONTROLS

FIG. 64c



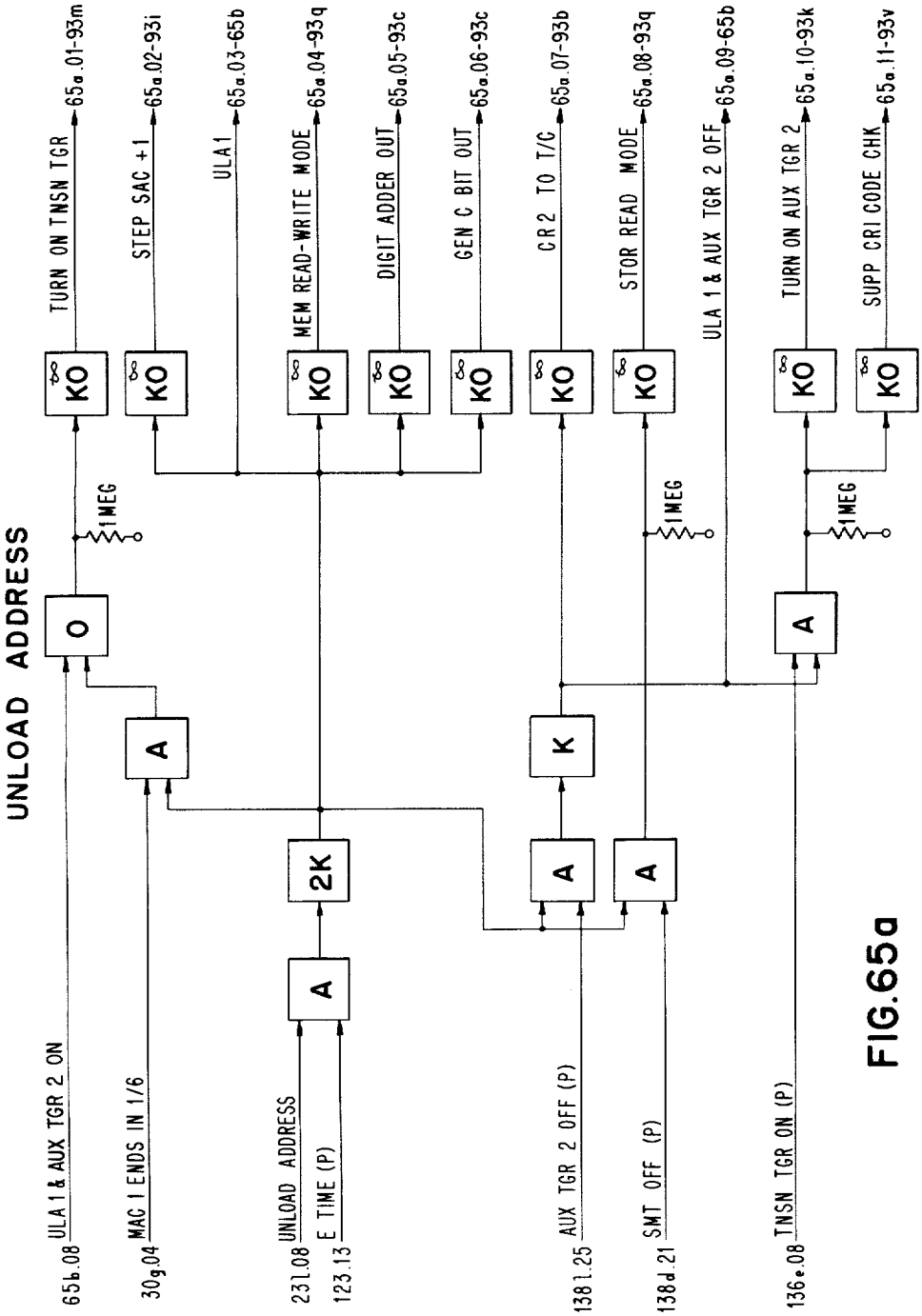
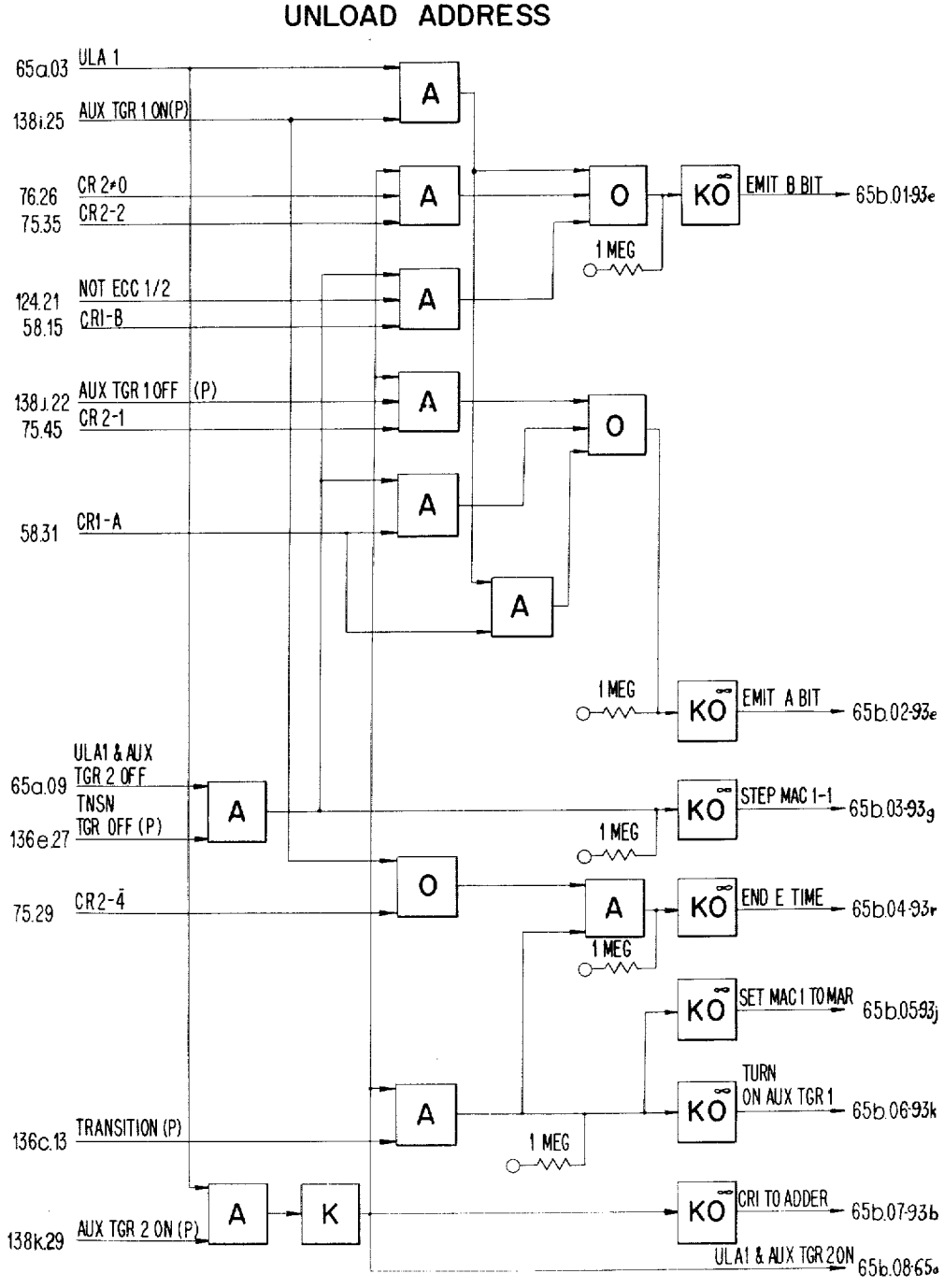

UNLOAD ADDRESS
TURN ON TNSN TGR 65a.01-93m
STEP SAC +1 65a.02-93i
ULA1 65a.03-65b
MEM READ-WRITE MODE 65a.04-93q
DIGIT ADDER OUT 65a.05-93c
GEN C BIT OUT 65a.06-93c
CR 2 TO T/C 65a.07-93b
STOR READ MODE 65a.08-93q
ULA 1 & AUX TGR 2 OFF 65a.09-65b
TURN ON AUX TGR 2 65a.10-93k
SUPP CRI CODE CHK 65a.11-93v
KO
1MEG
O
A
2K
K
65b.08 ULA 1 & AUX TGR 2 ON
30g.04 MAC 1 ENDS IN 1/6
231.08 UNLOAD ADDRESS
123.13 E TIME (P)
138 l.25 AUX TGR 2 OFF (P)
138d.21 SMT OFF (P)
136e.08 TNSN TGR ON (P)

FIG.65a

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FIG.65b



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OVERLAP MODE CONTROL

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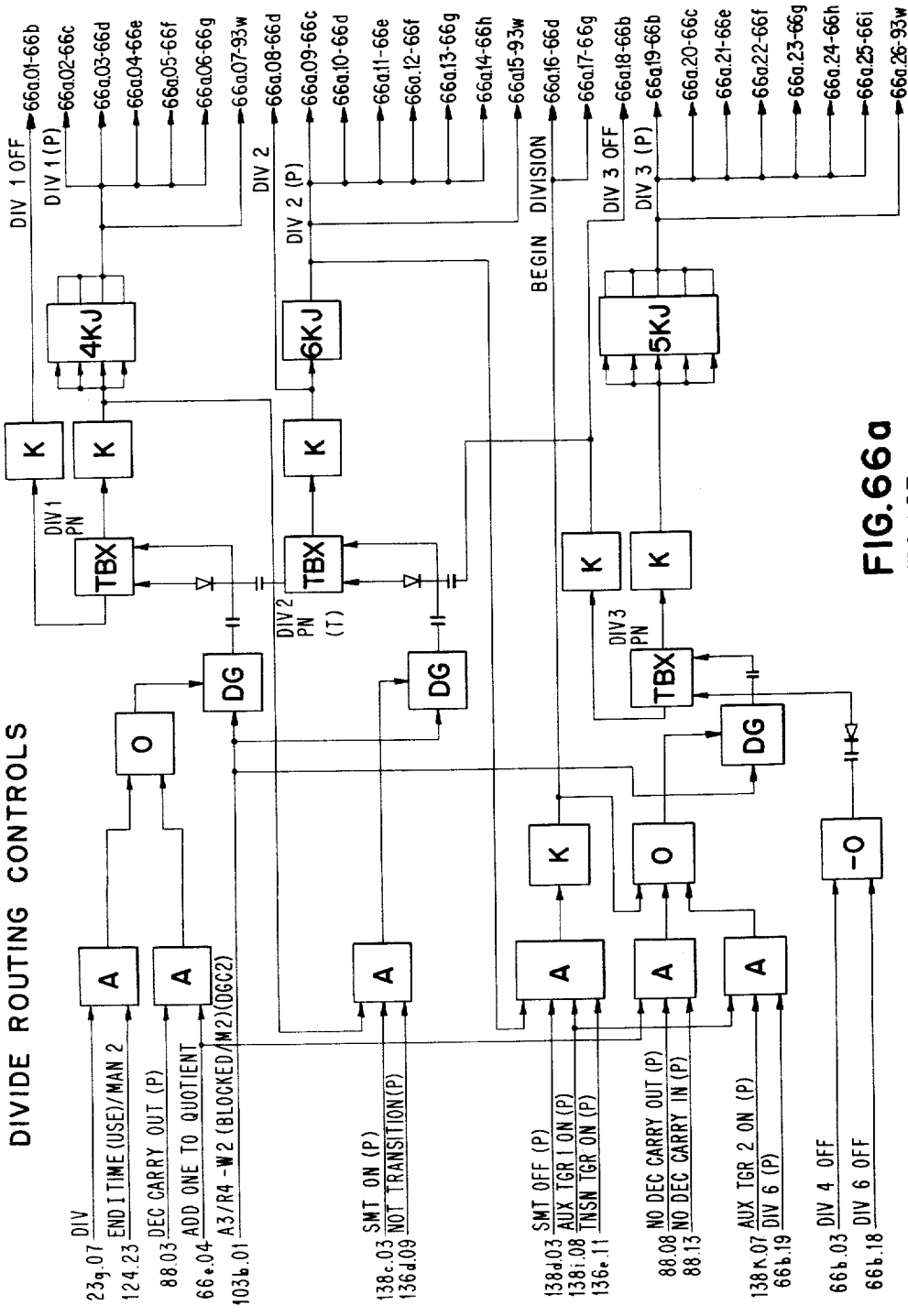


FIG.66a

March 27, 1962 O. D. EVANS ETAL 3,027,081

OVERLAP MODE CONTROL

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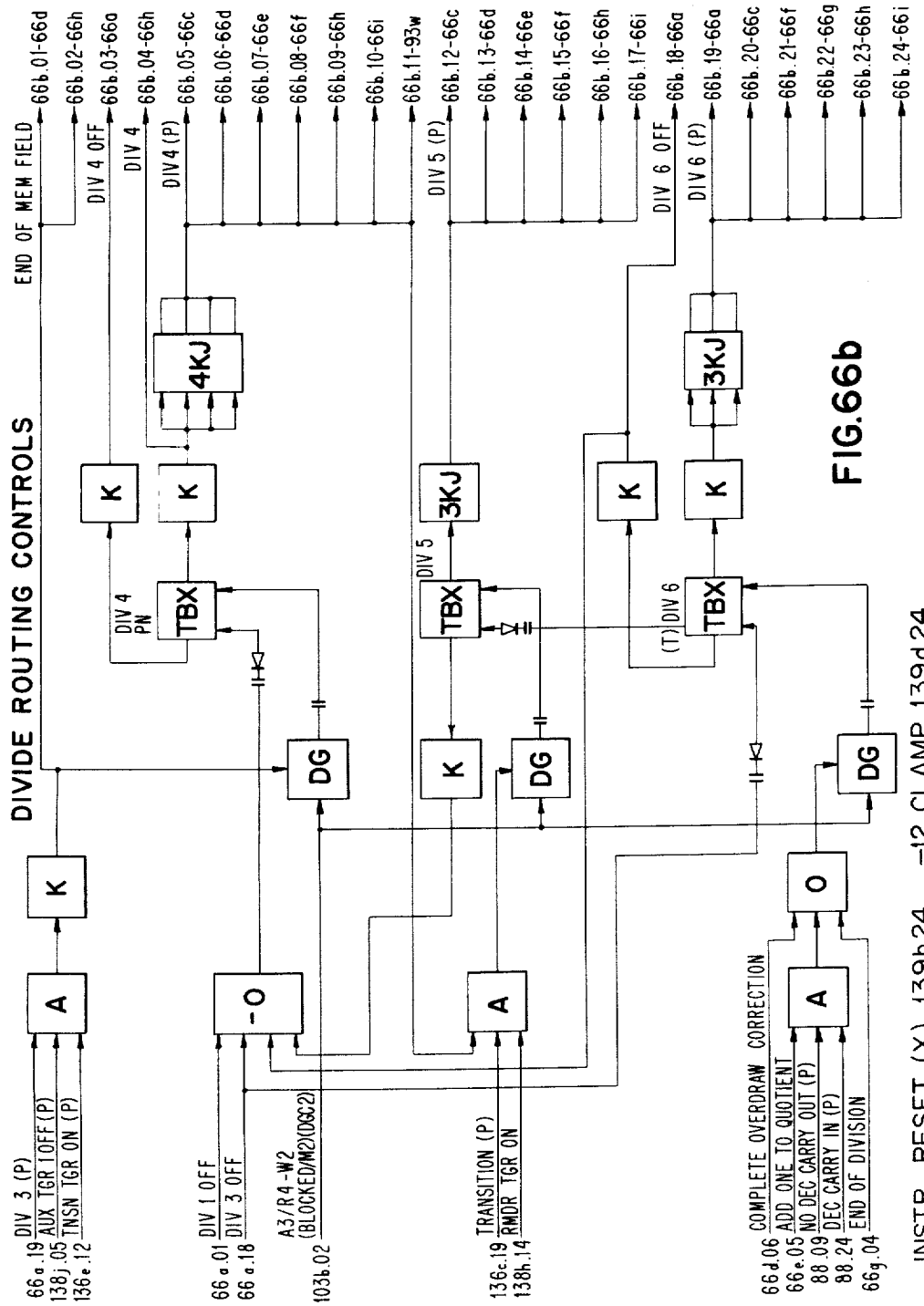


FIG.66b

March 27, 1962 O. D. EVANS ETAL 3,027,081

OVERLAP MODE CONTROL

Filed Jan. 2, 1959 390 Sheets-Sheet 221

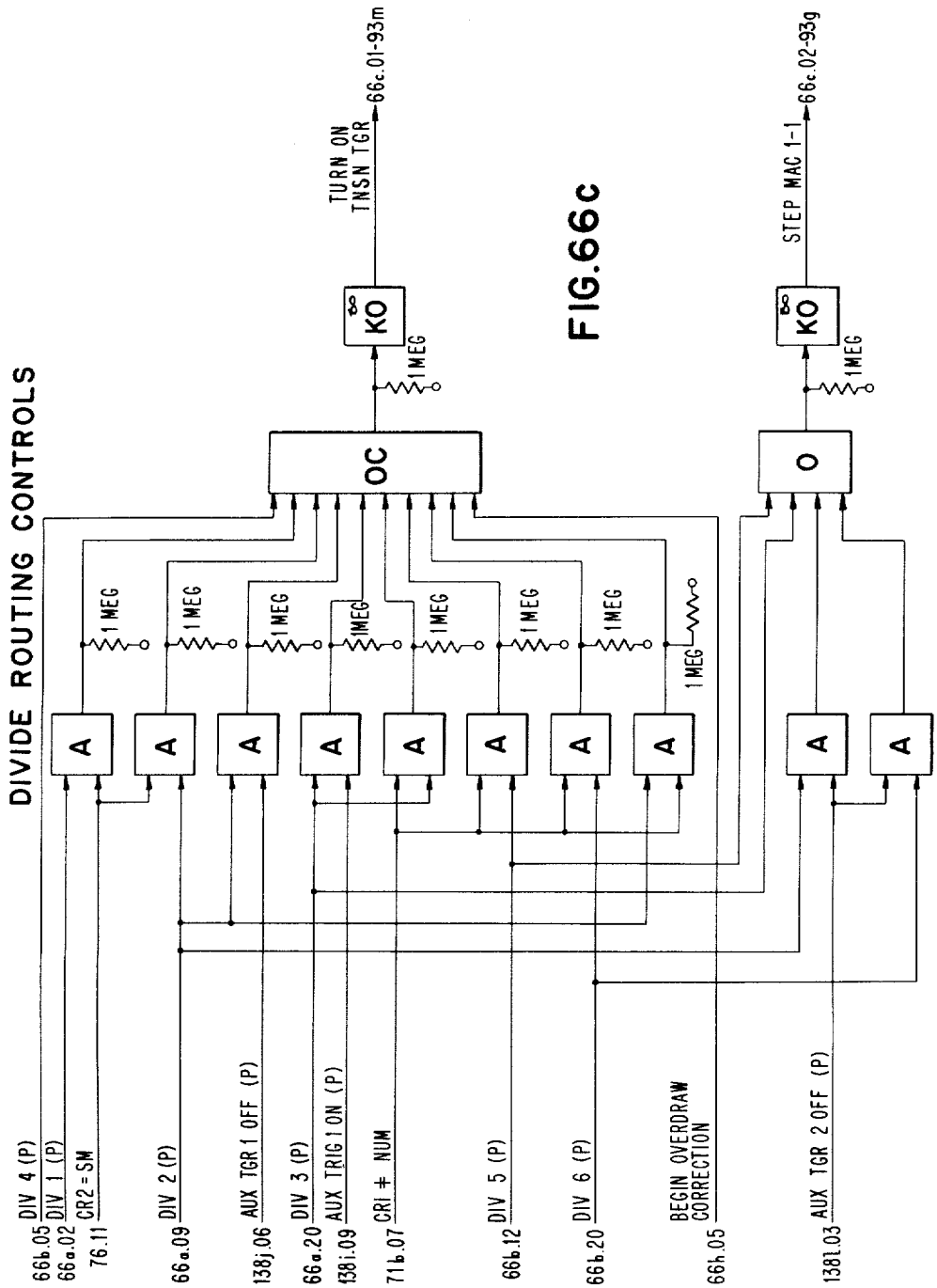


FIG.66c

FIG.66d

DIVIDE ROUTING CONTROLS

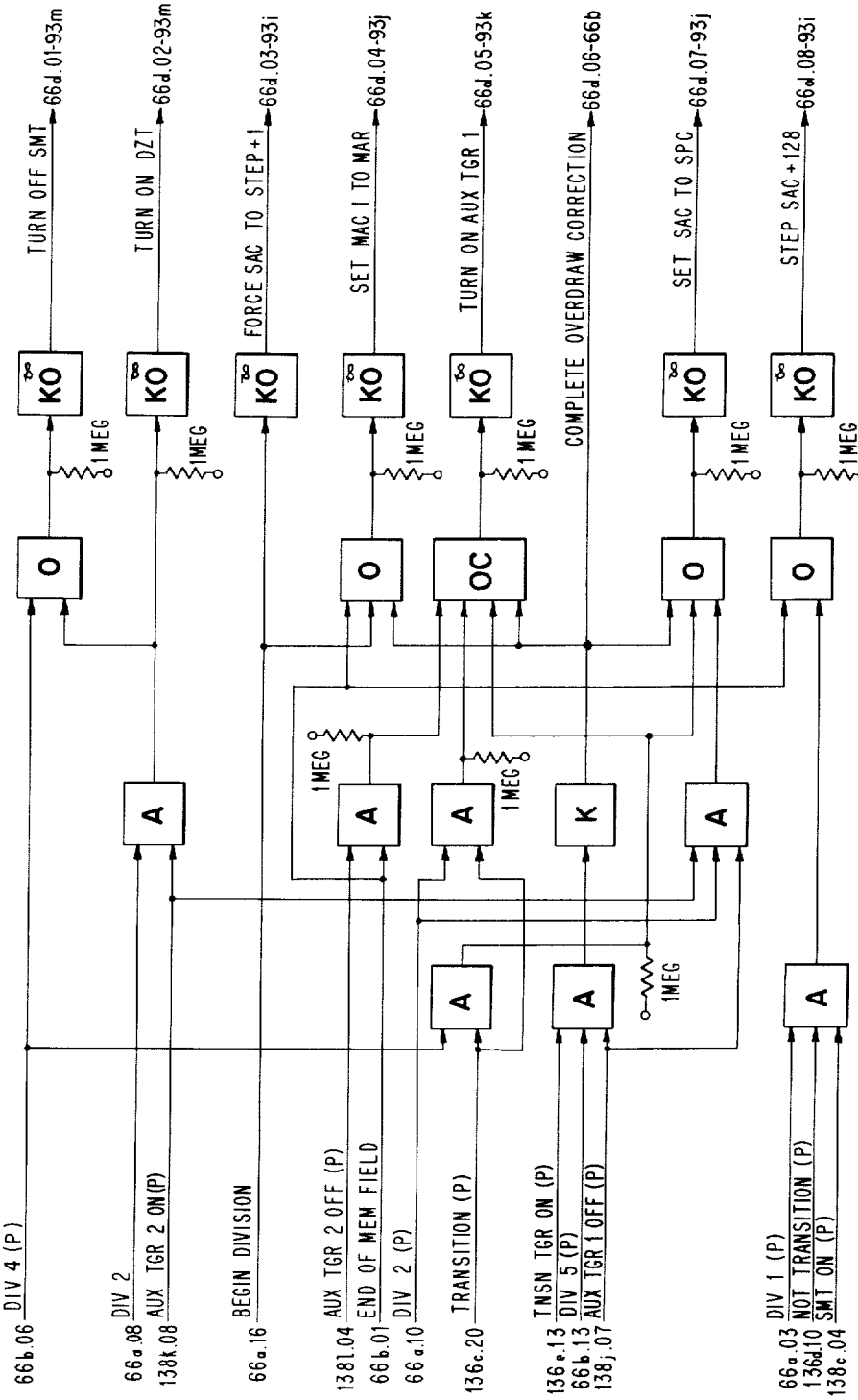


FIG. 66e

DIVIDE ROUTING CONTROLS

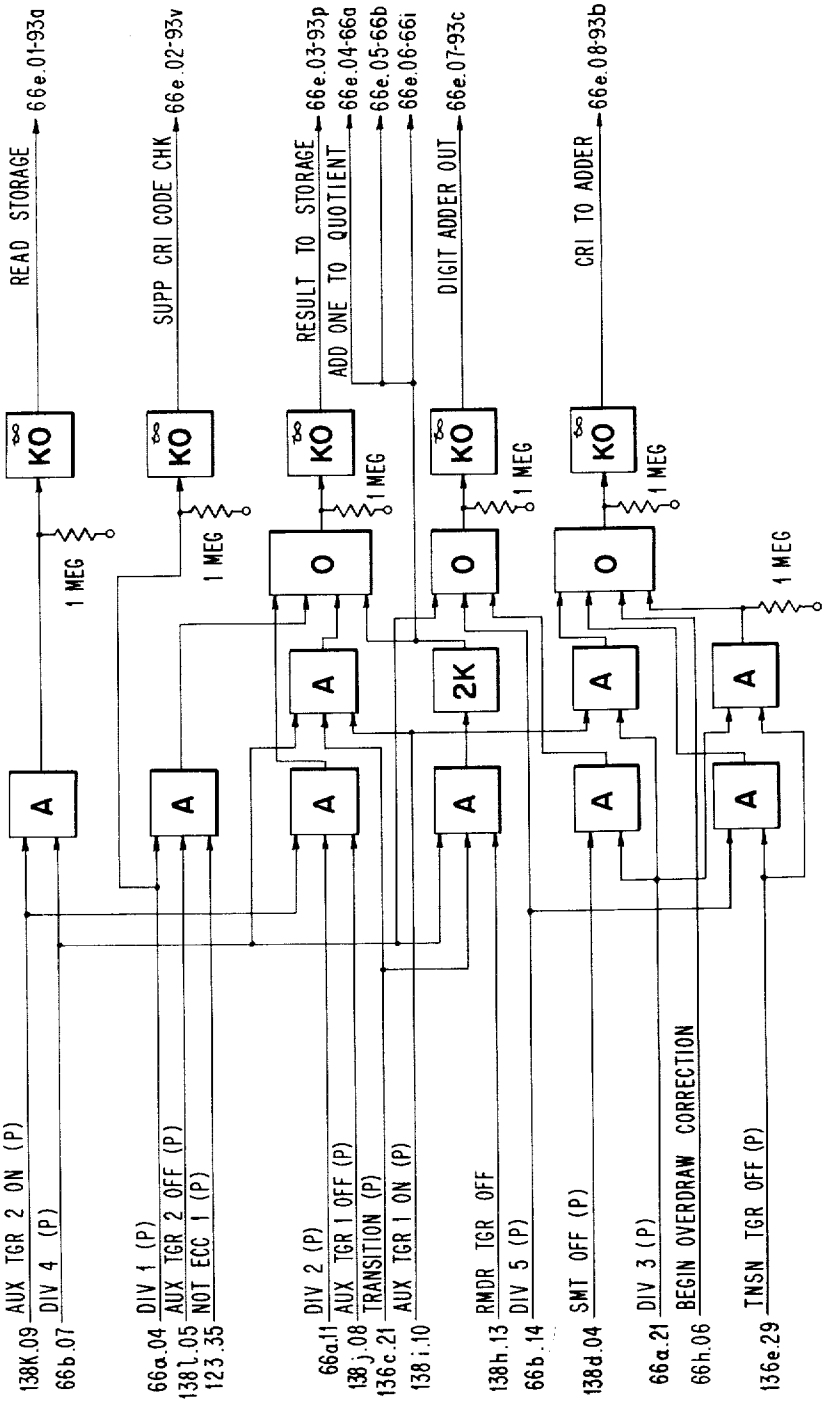
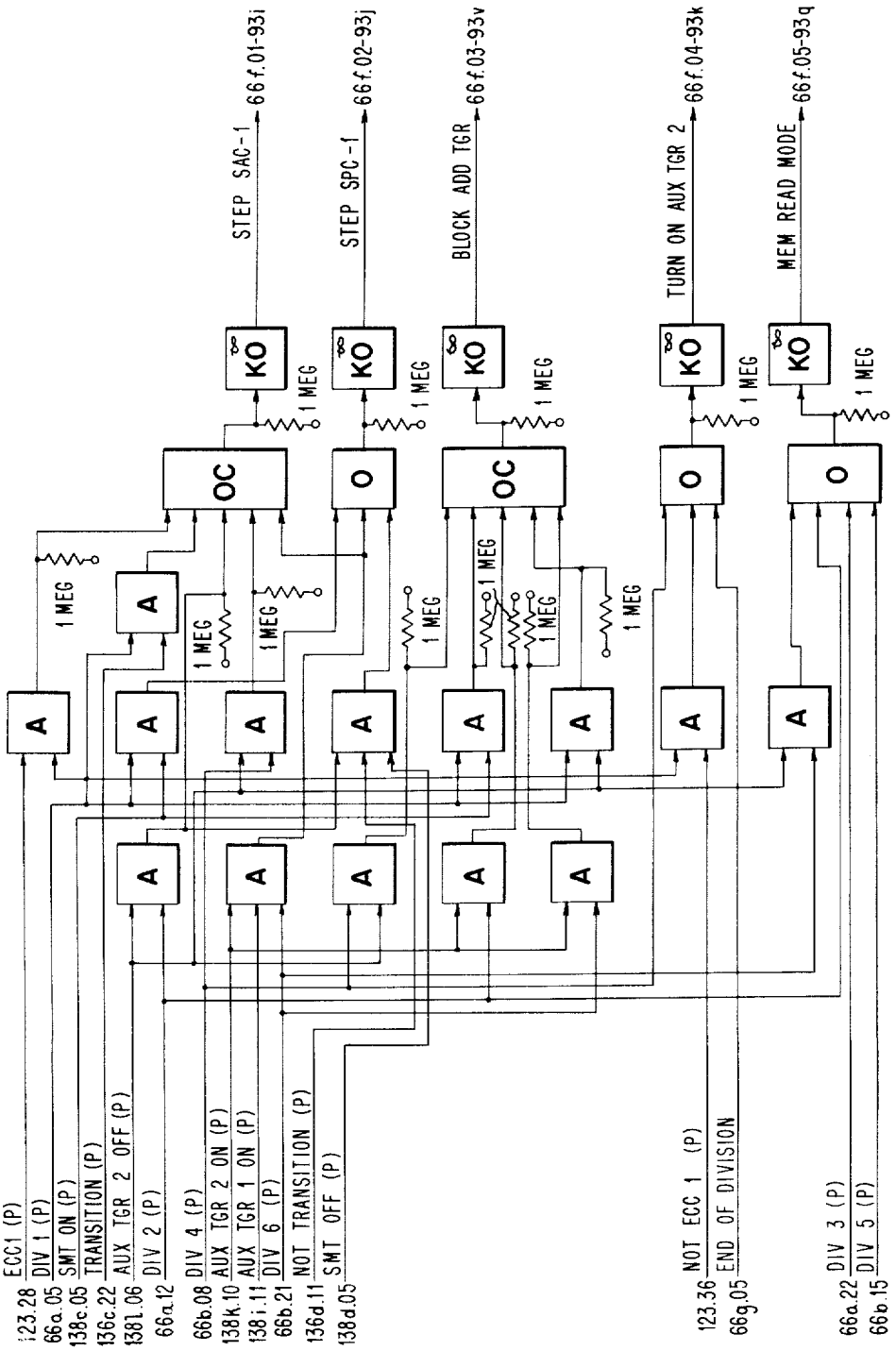


FIG. 66f

DIVIDE ROUTING CONTROLS



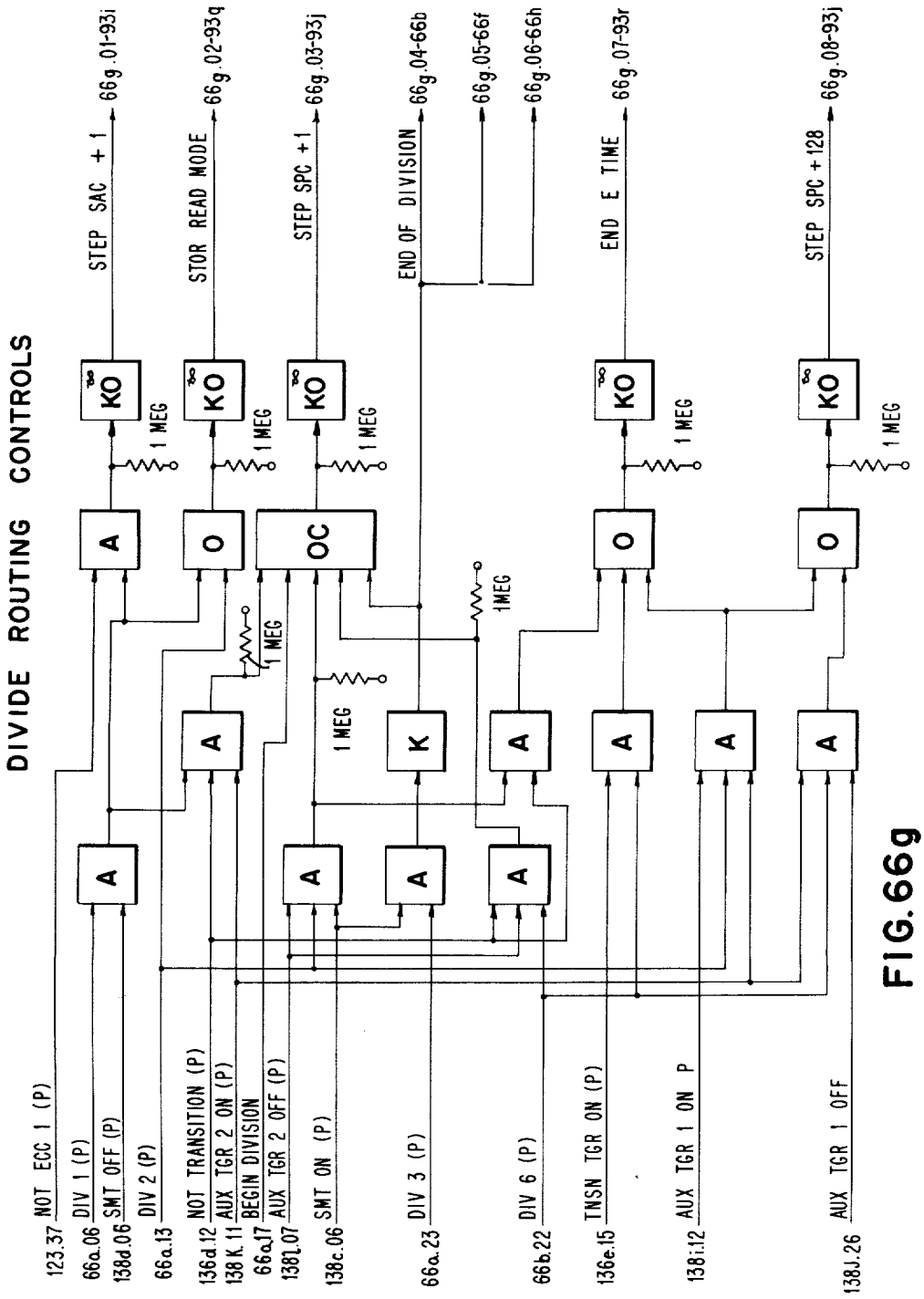

DIVIDE ROUTING CONTROLS
STEP SAC + 1
66g.01-93i
STOR READ MODE
66g.02-93q
STEP SPC +1
66g.03-93j
END OF DIVISION
66g.04-66b
66g.05-66f
66g.06-66h
END E TIME
66g.07-93r
STEP SPC +128
66g.08-93j
KO
A
O
OC
K
1 MEG
123.37 NOT ECC 1 (P)
66a.06 DIV 1 (P)
138d.06 SMT OFF (P)
66a.13 DIV 2 (P)
136a.12 NOT TRANSITION (P)
138K.11 AUX TGR 2 ON (P)
66a.17 BEGIN DIVISION
138L.07 AUX TGR 2 OFF (P)
138c.06 SMT ON (P)
66a.23 DIV 3 (P)
66b.22 DIV 6 (P)
136e.15 TNSN TGR ON (P)
138i.12 AUX TGR 1 ON P
138J.26 AUX TGR 1 OFF

FIG.66g

FIG. 66h DIVIDE ROUTING CONTROLS

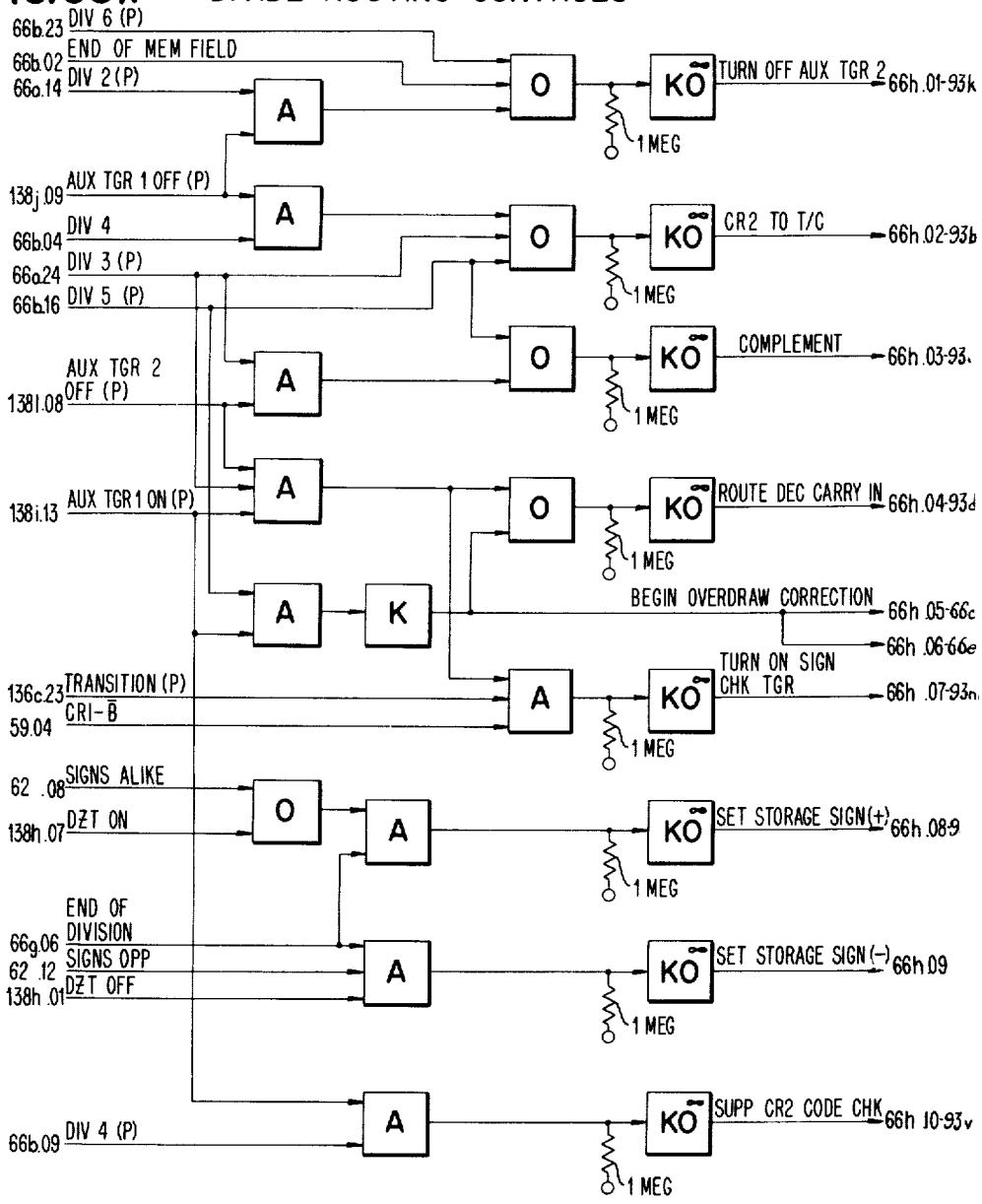


FIG. 66i

DIVIDE ROUTING CONTROLS

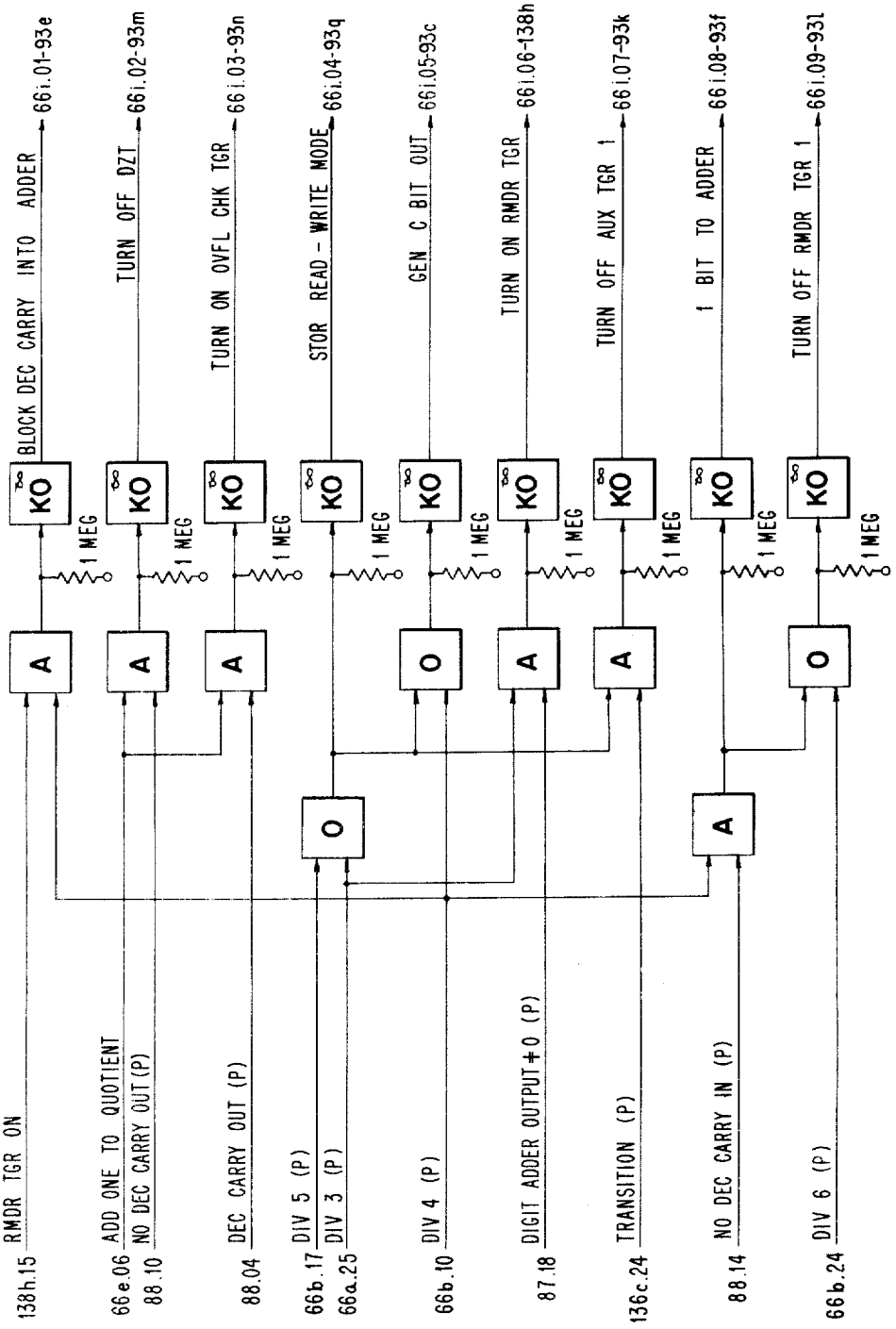


FIG. 67a

MULTIPLY ROUTING CONTROLS

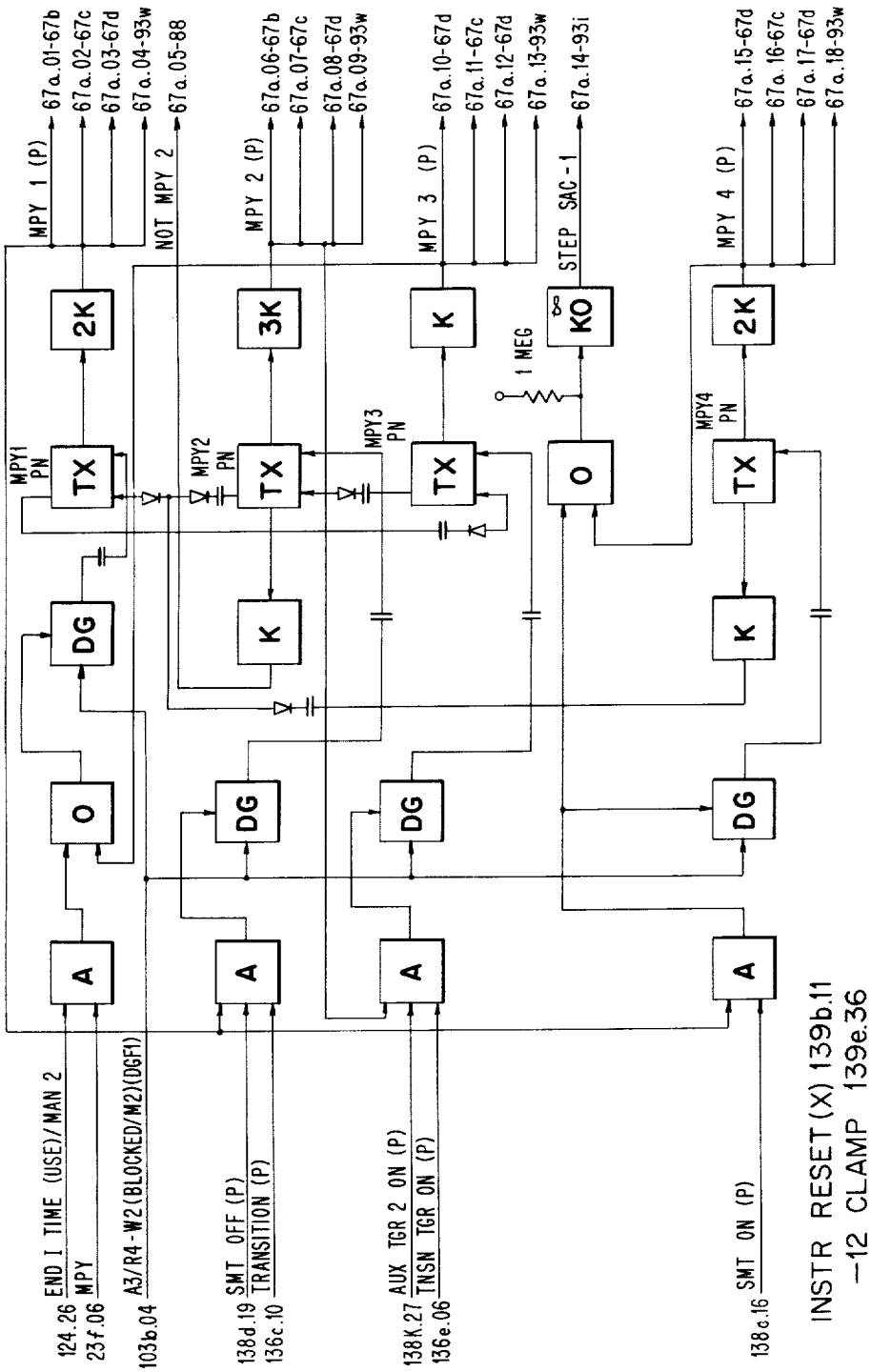


FIG. 67b
MULTIPLY ROUTING CONTROL

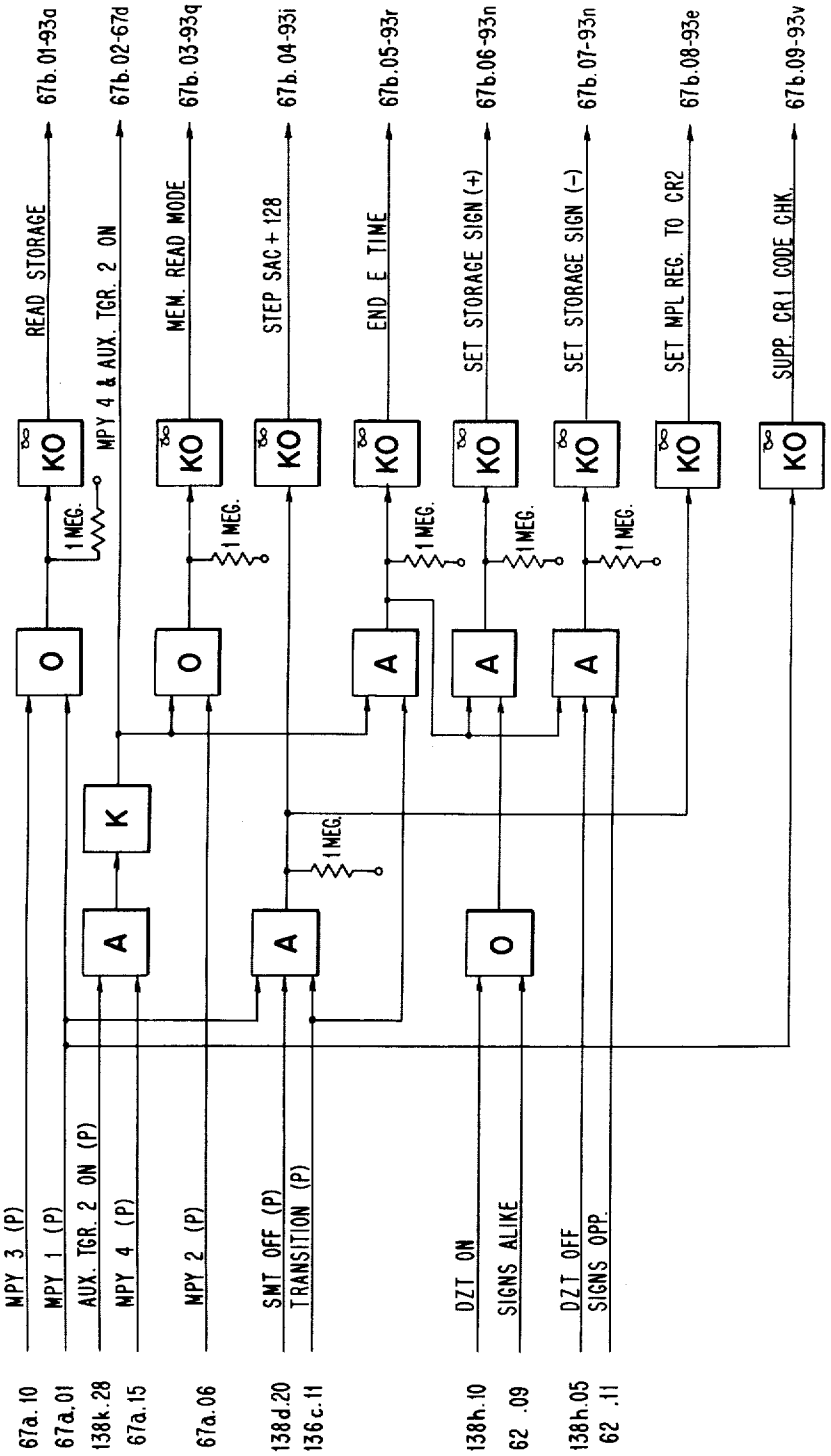
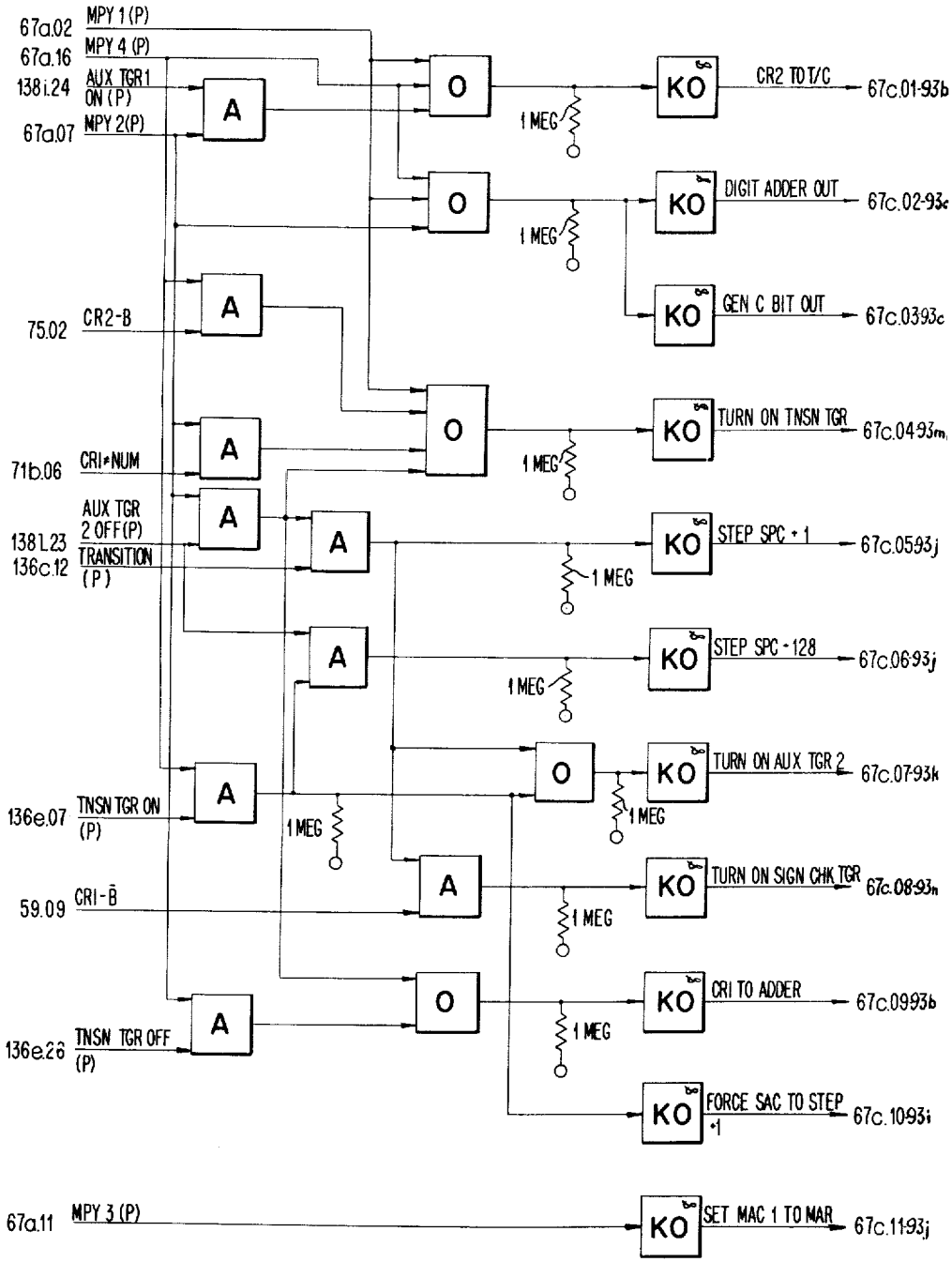


FIG.67c

MULTIPLY ROUTING CONTROLS



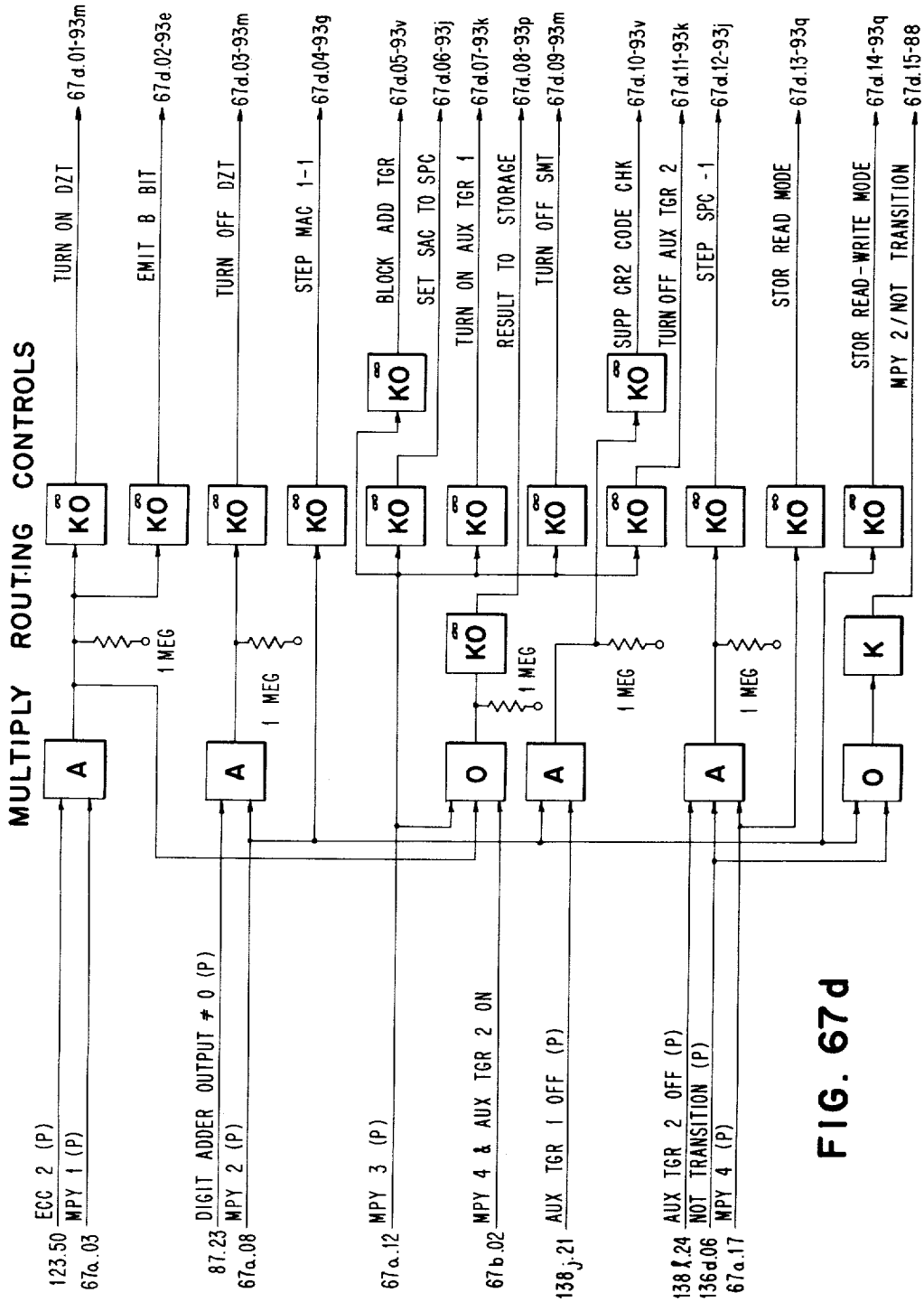

MULTIPLY ROUTING CONTROLS
TURN ON DZT
67d.01-93m
EMIT B BIT
67d.02-93e
TURN OFF DZT
67d.03-93m
STEP MAC 1-1
67d.04-93g
BLOCK ADD TGR
67d.05-93v
SET SAC TO SPC
67d.06-93j
TURN ON AUX TGR 1
67d.07-93k
RESULT TO STORAGE
67d.08-93p
TURN OFF SMT
67d.09-93m
SUPP CR2 CODE CHK
67d.10-93v
TURN OFF AUX TGR 2
67d.11-93k
STEP SPC -1
67d.12-93j
STOR READ MODE
67d.13-93q
STOR READ-WRITE MODE
67d.14-93q
MPY 2 / NOT TRANSITION
67d.15-88
KO
A
O
K
1 MEG
123.50 ECC 2 (P)
67a.03 MPY 1 (P)
87.23 DIGIT ADDER OUTPUT ≠ 0 (P)
67a.08 MPY 2 (P)
67a.12 MPY 3 (P)
67b.02 MPY 4 & AUX TGR 2 ON
138j.21 AUX TGR 1 OFF (P)
138f.24 AUX TGR 2 OFF (P)
136d.06 NOT TRANSITION (P)
67a.17 MPY 4 (P)

FIG. 67d

FIG. 68a

ADD TO MEMORY ROUTING CONTROLS

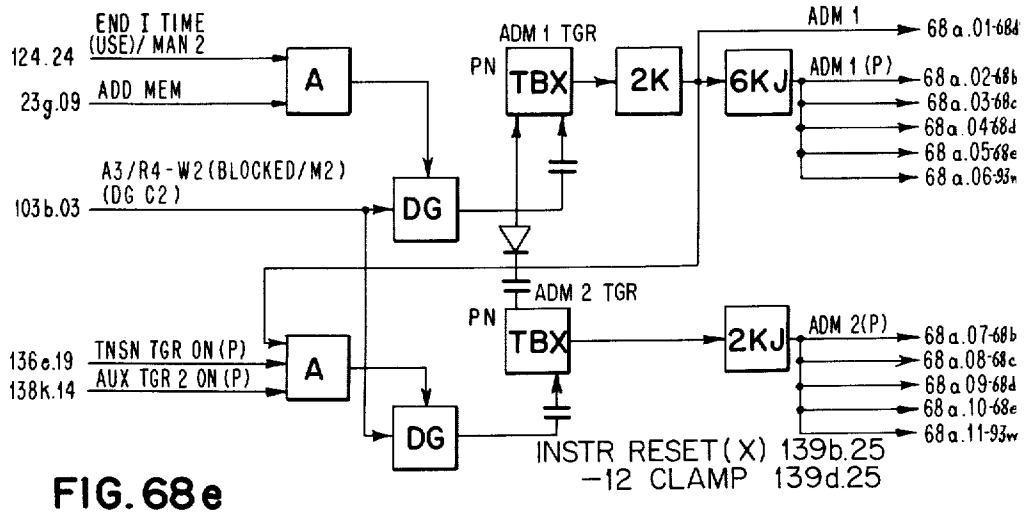
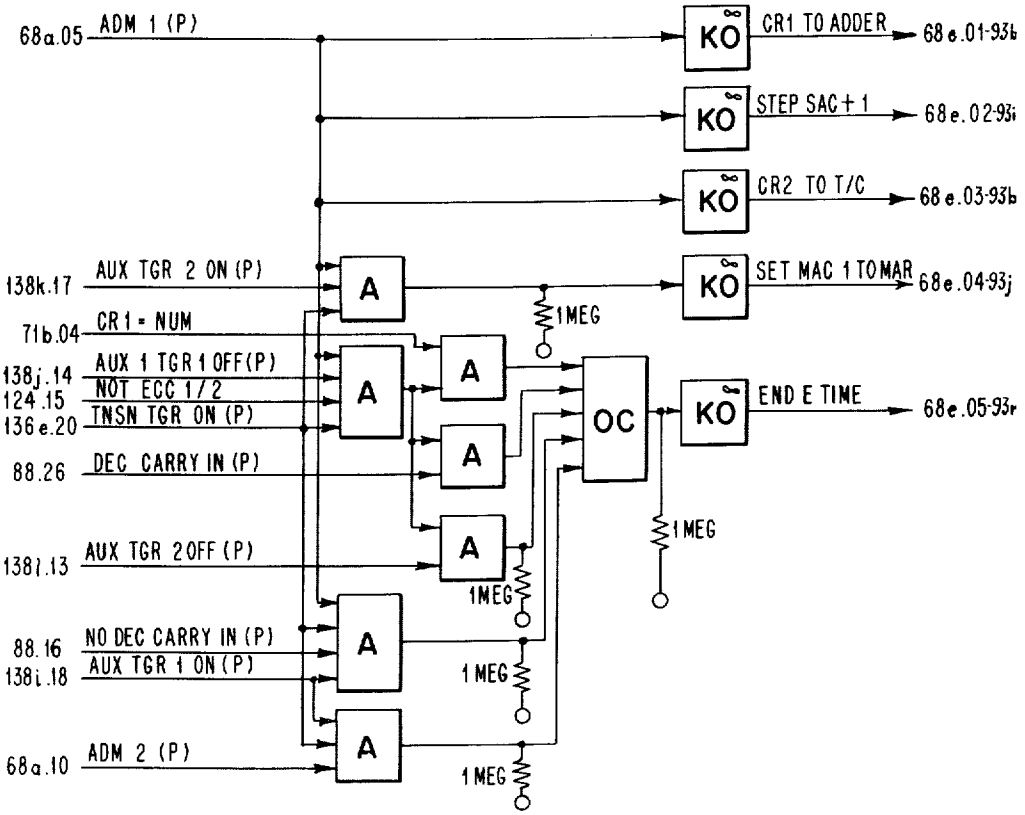


FIG. 68e

ADD TO MEMORY ROUTING CONTROLS



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FIG.68b ADD TO MEMORY ROUTING CONTROLS

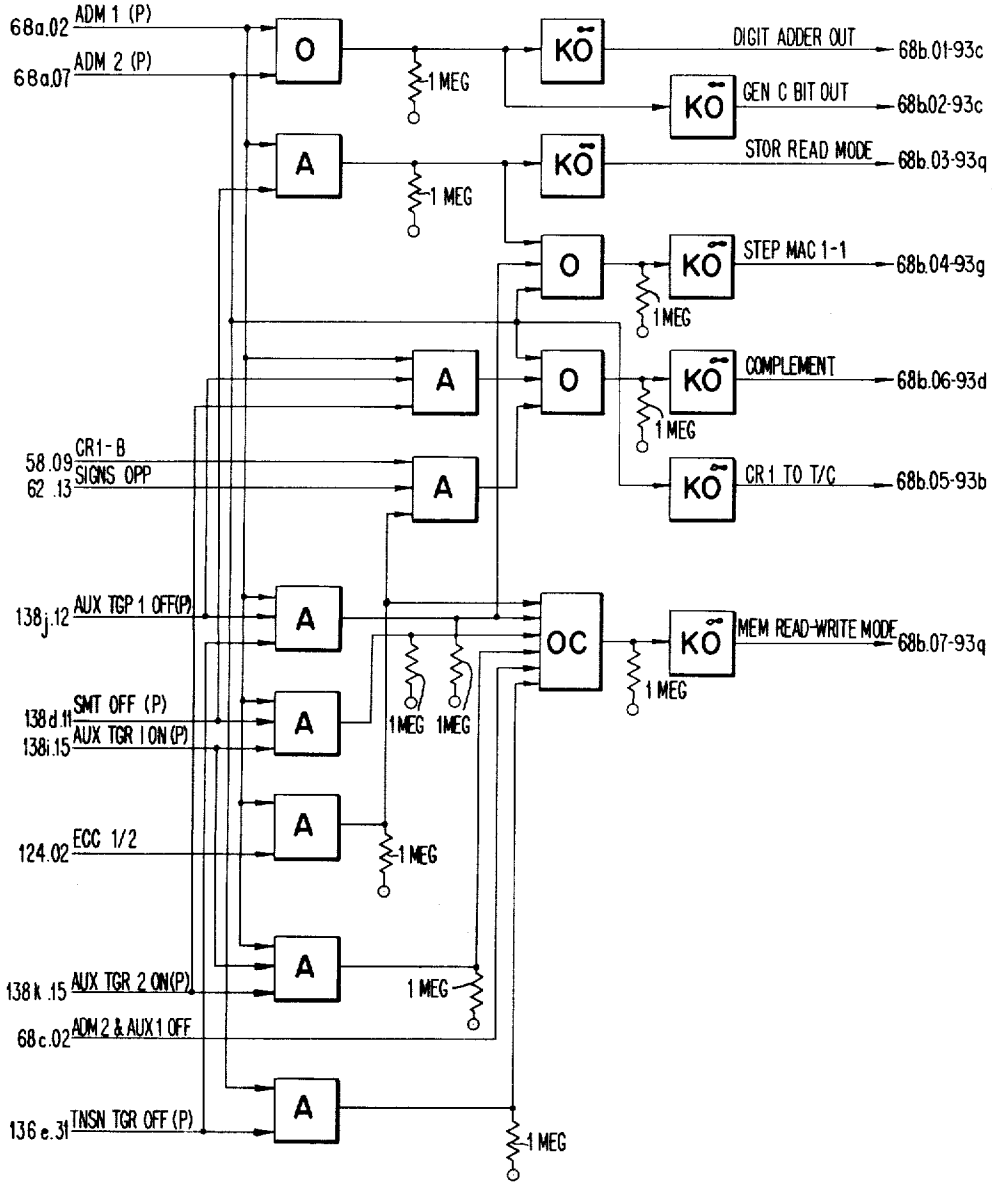


FIG.68c ADD TO MEMORY ROUTING CONTROLS

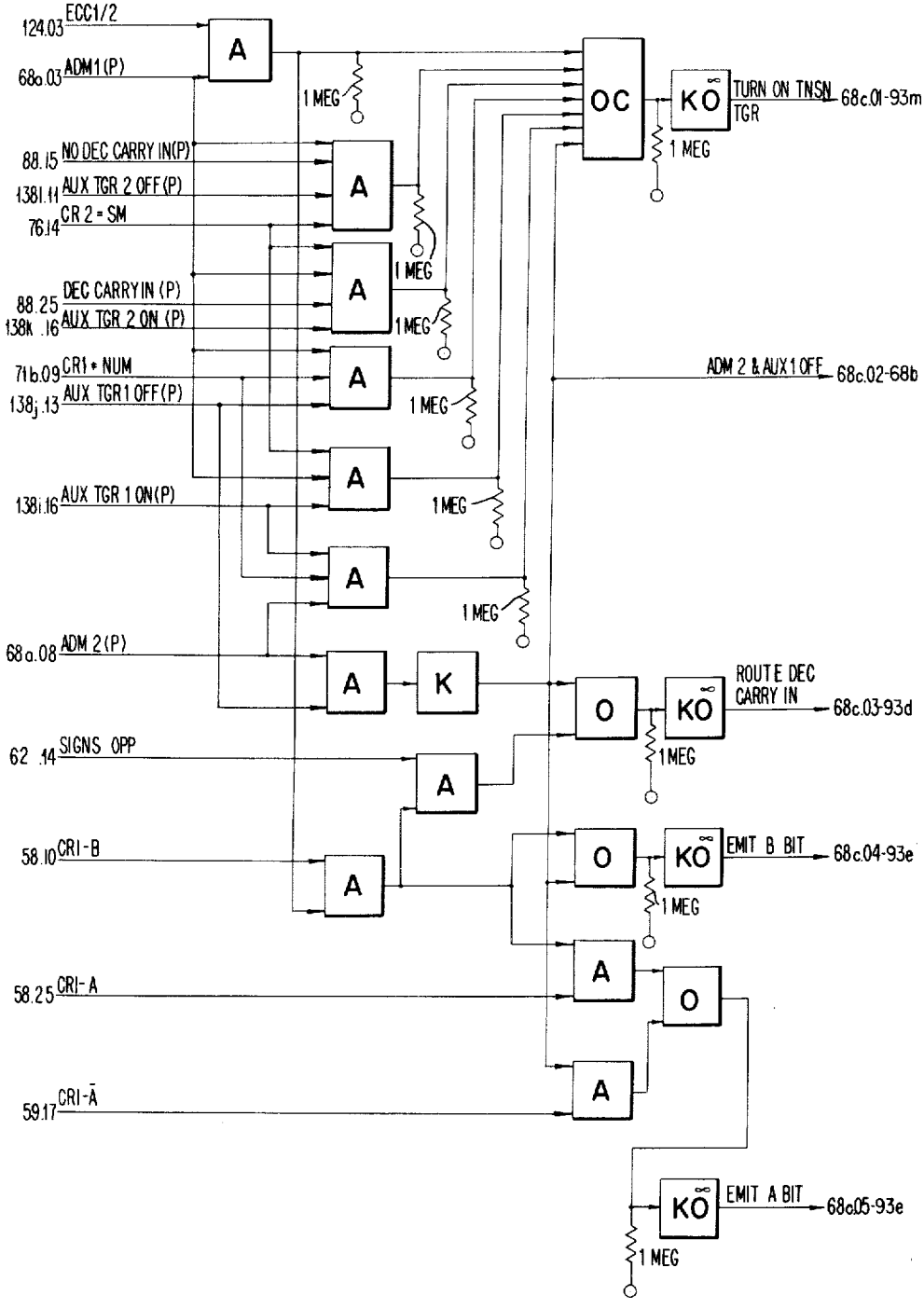


FIG. 68d ADD TO MEMORY ROUTING CONTROLS

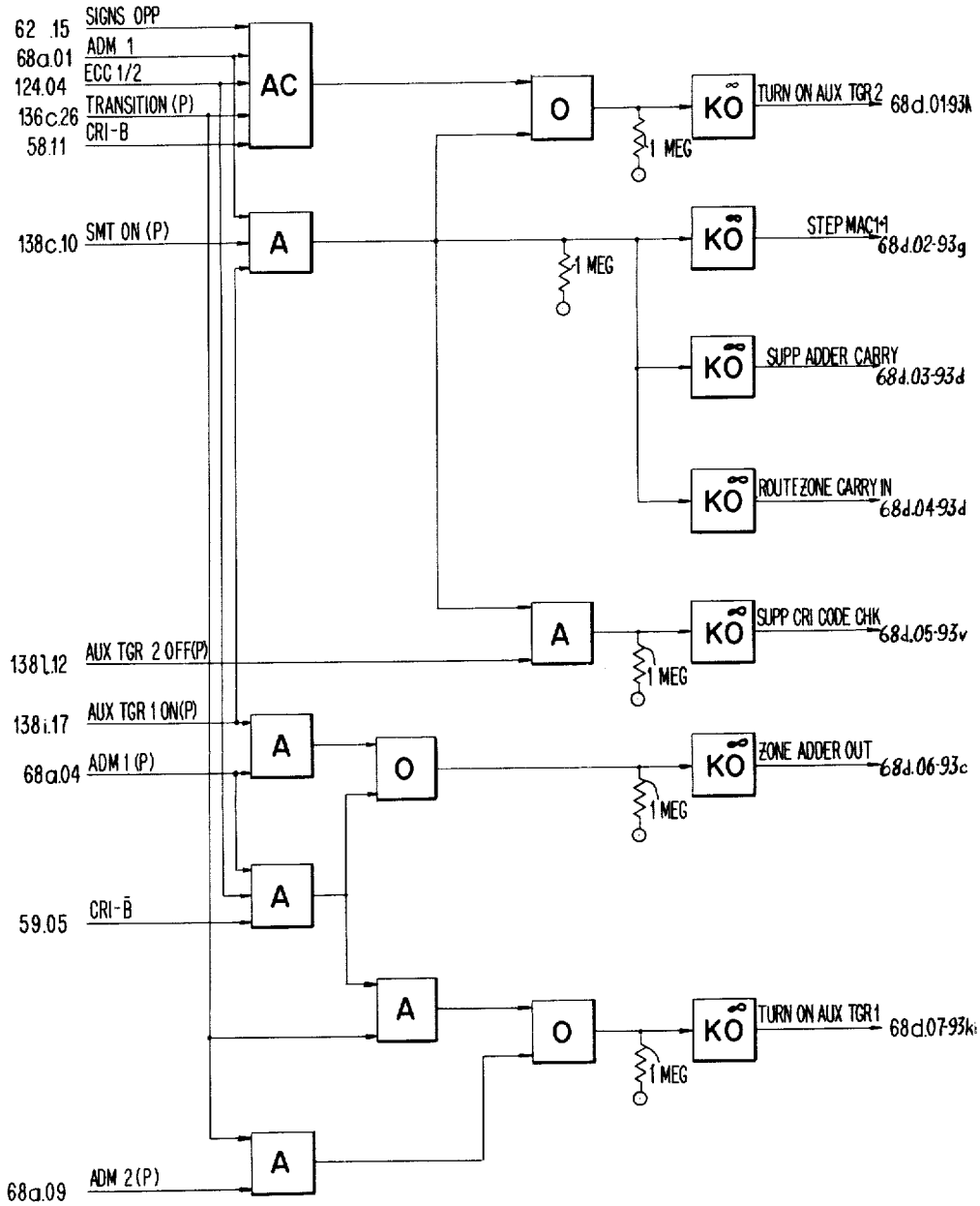


FIG.69a

SIGN, NO OP, RECEIVE & STOP ROUTING CONTROLS

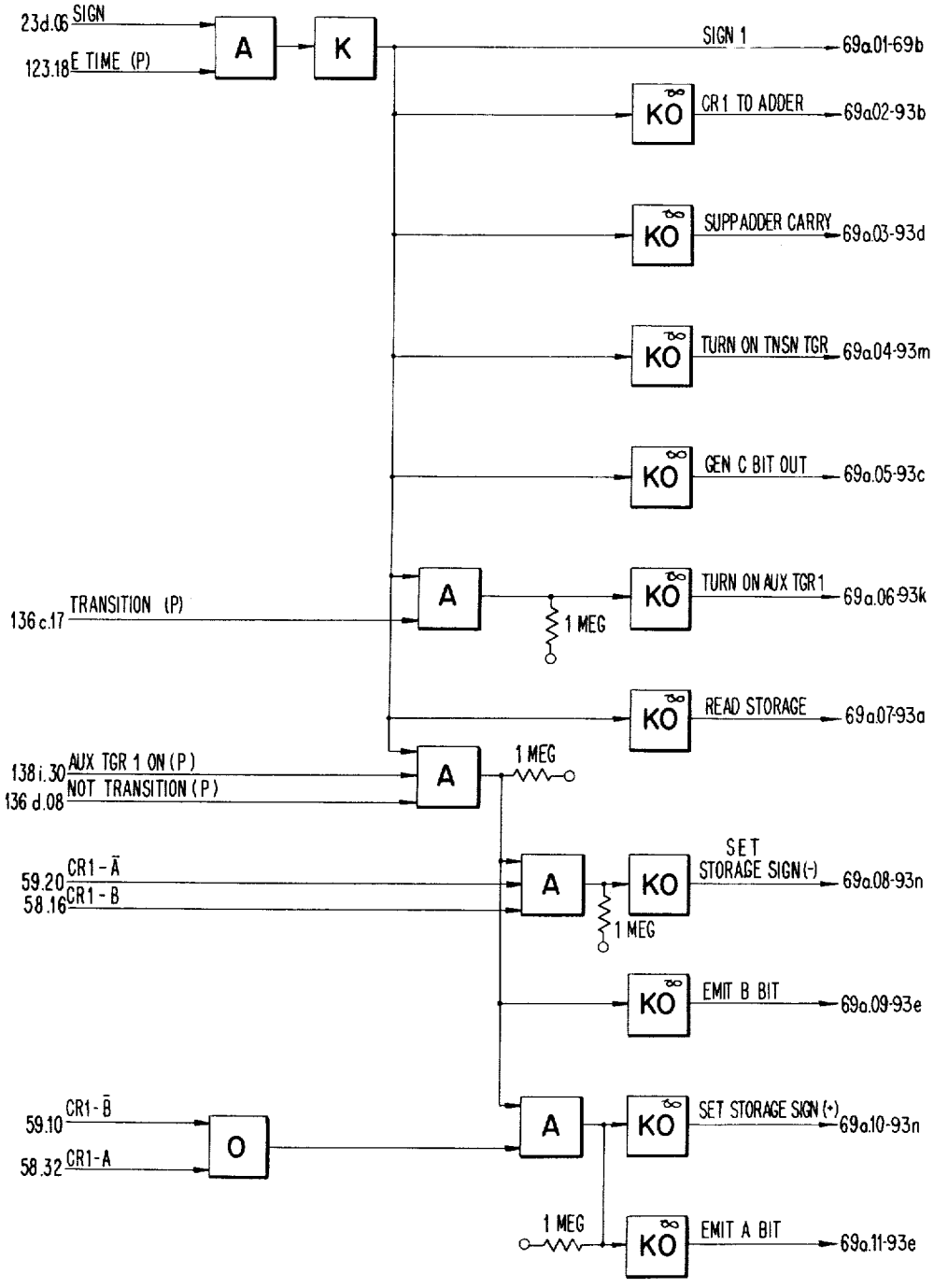


FIG. 69b

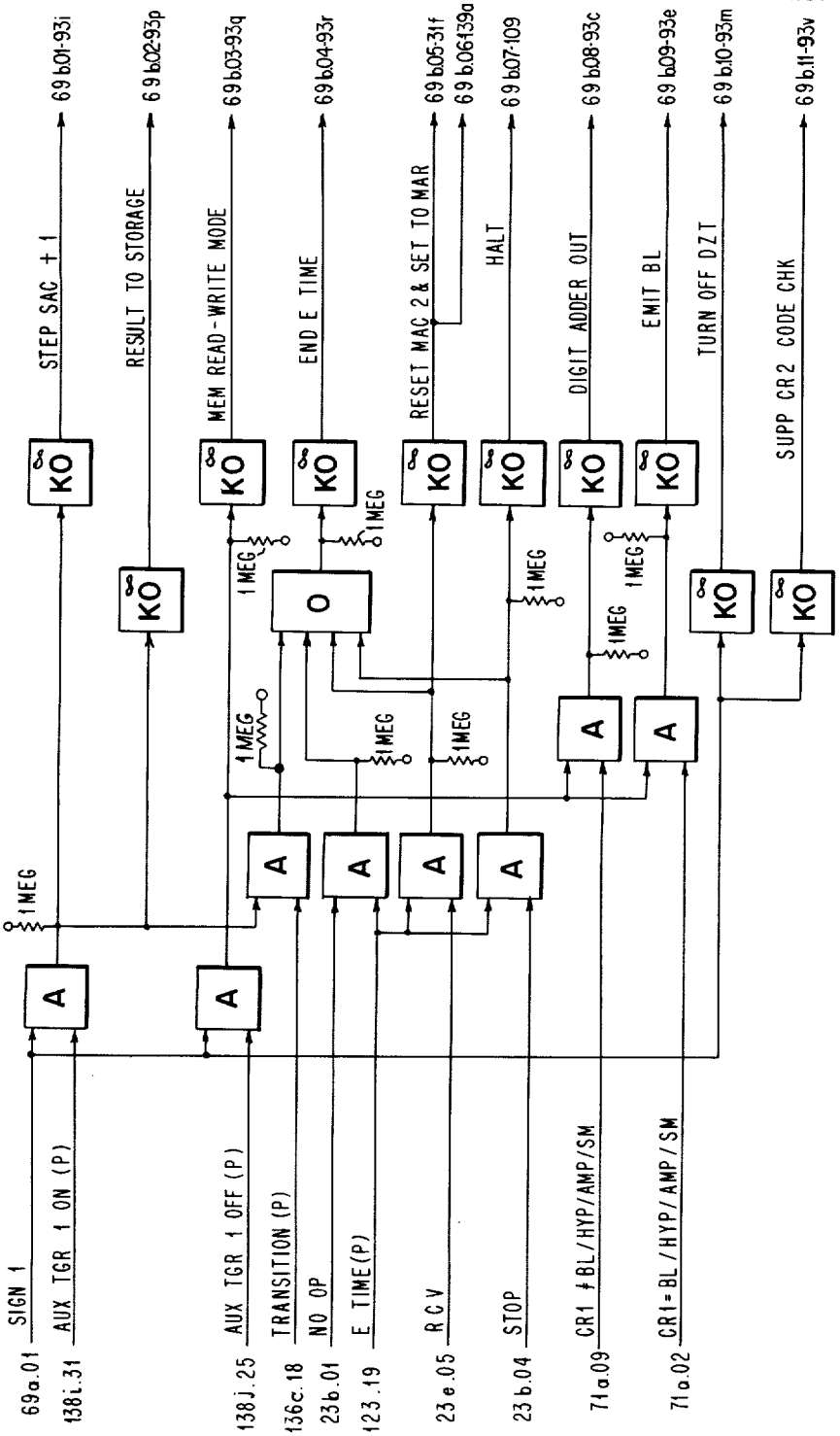
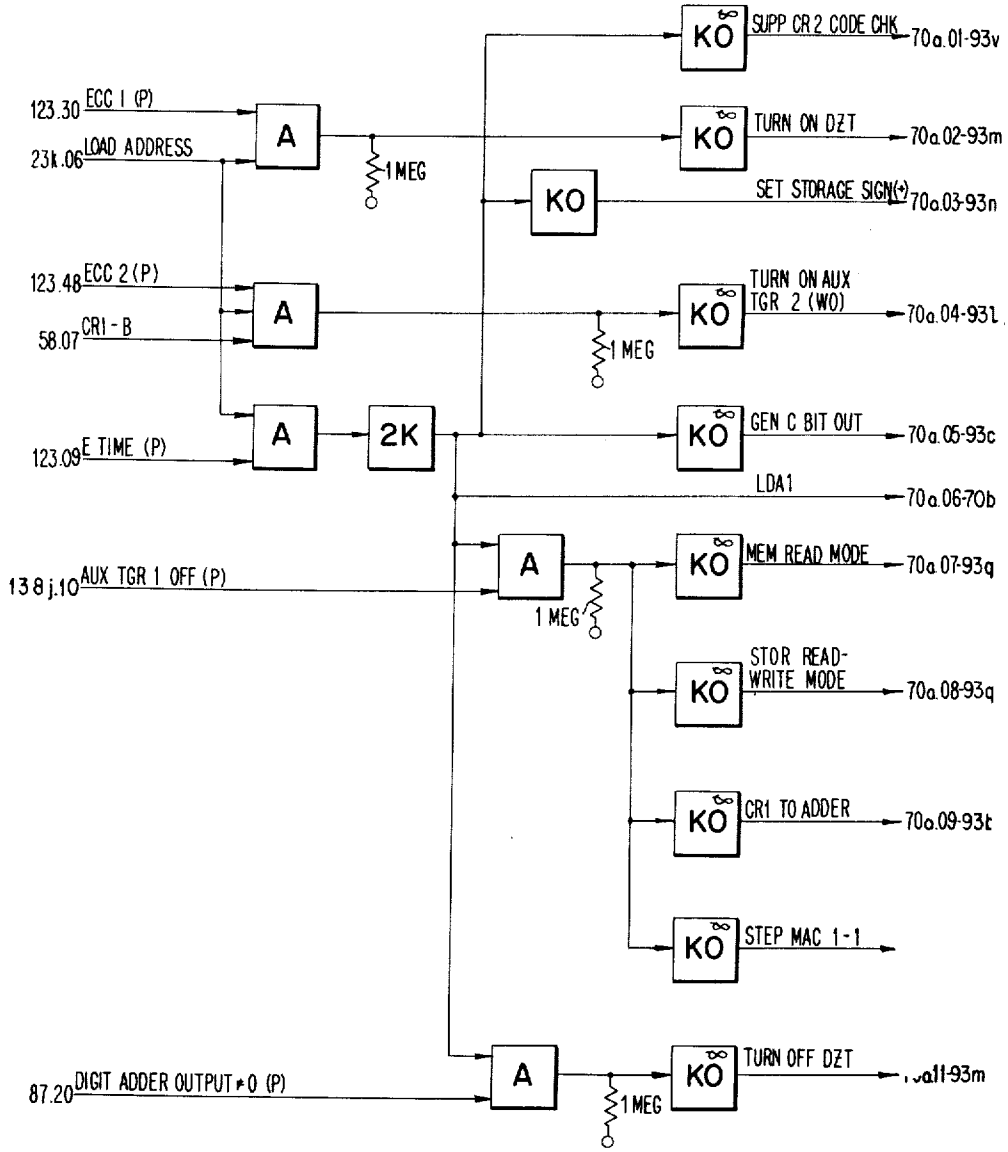

SIGN, NO OP, RECEIVE & STOP ROUTING CONTROLS
69a.01 SIGN 1
138i.31 AUX TGR 1 ON (P)
138j.25 AUX TGR 1 OFF (P)
136c.18 TRANSITION (P)
23b.01 NO OP
123.19 E TIME (P)
23e.05 R C V
23b.04 STOP
71a.09 CR1 ≠ BL/HYP/AMP/SM
71a.02 CR1 = BL/HYP/AMP/SM
STEP SAC + 1
RESULT TO STORAGE
MEM READ-WRITE MODE
END E TIME
RESET MAC 2 & SET TO MAR
HALT
DIGIT ADDER OUT
EMIT BL
TURN OFF DZT
SUPP CR2 CODE CHK
69b01-93i
69b02-93p
69b03-93q
69b04-93r
69b05-31f
69b06139a
69b07-109
69b08-93c
69b09-93e
69b10-93m
69b11-93w
KO
A
O
1MEG

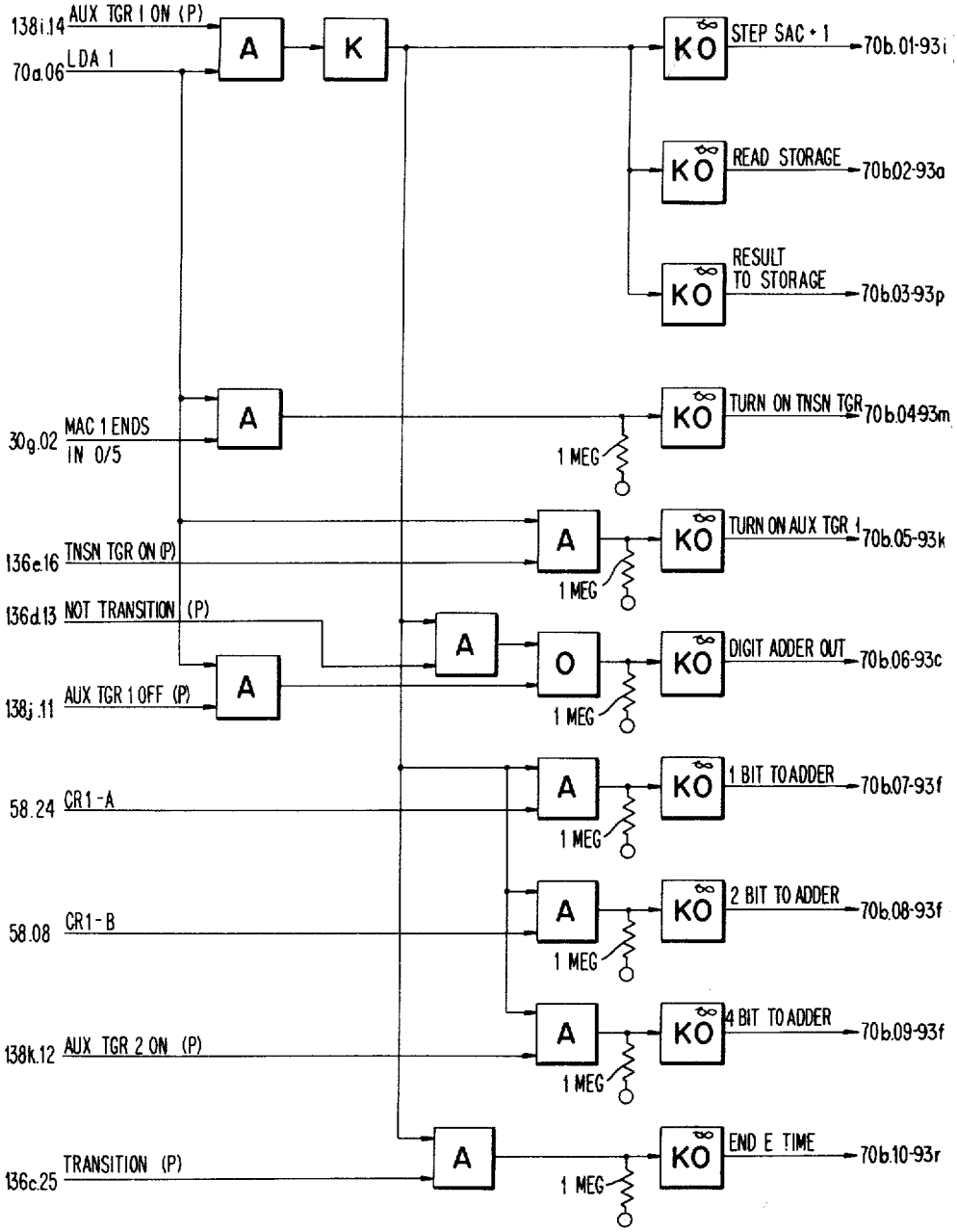
FIG. 70a

LOAD ADDRESS ROUTING CONTROLS



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FIG. 70b LOAD ADDRESS ROUTING CONTROLS



OVERLAP MODE CONTROL

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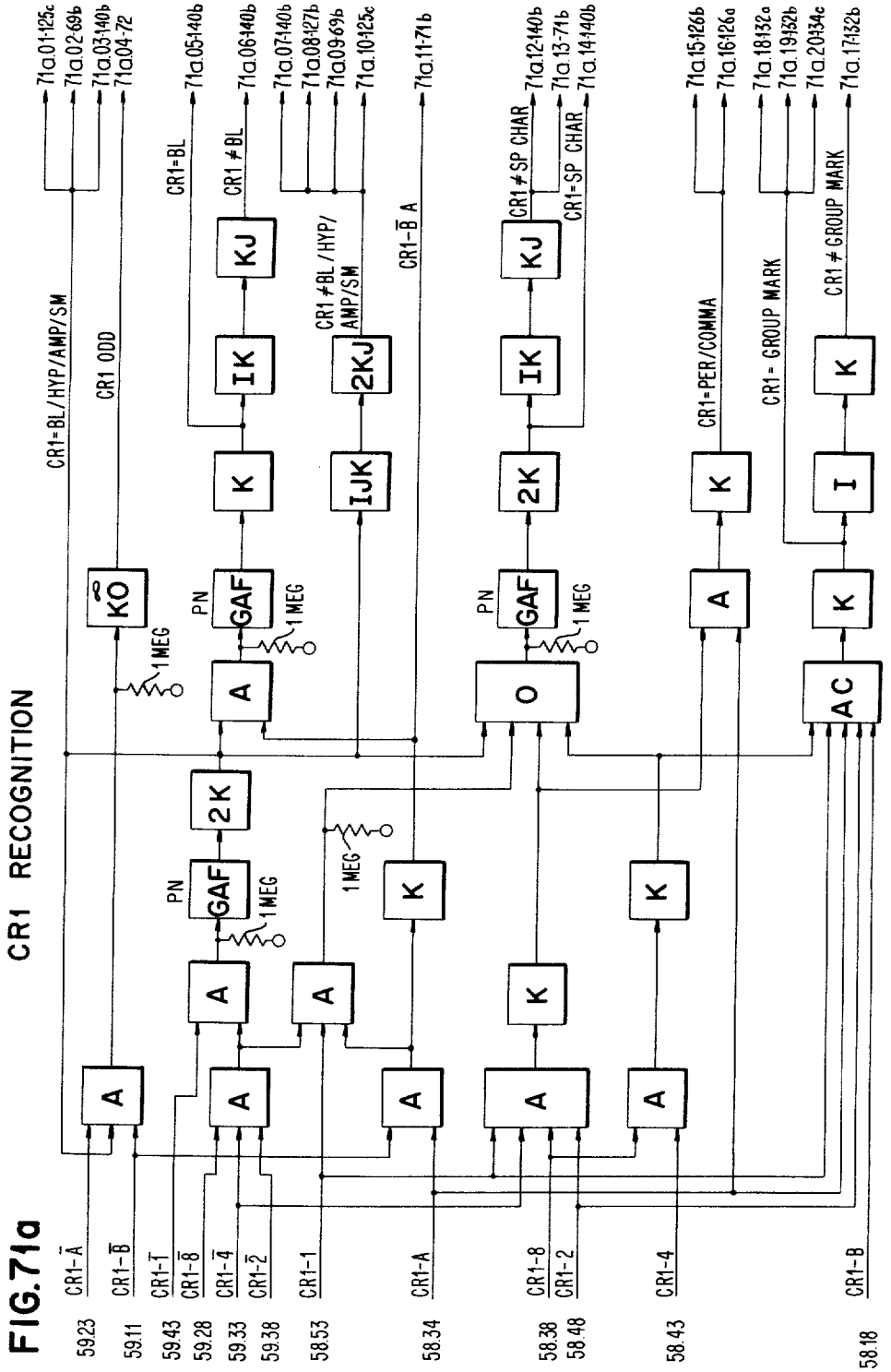


FIG.71a

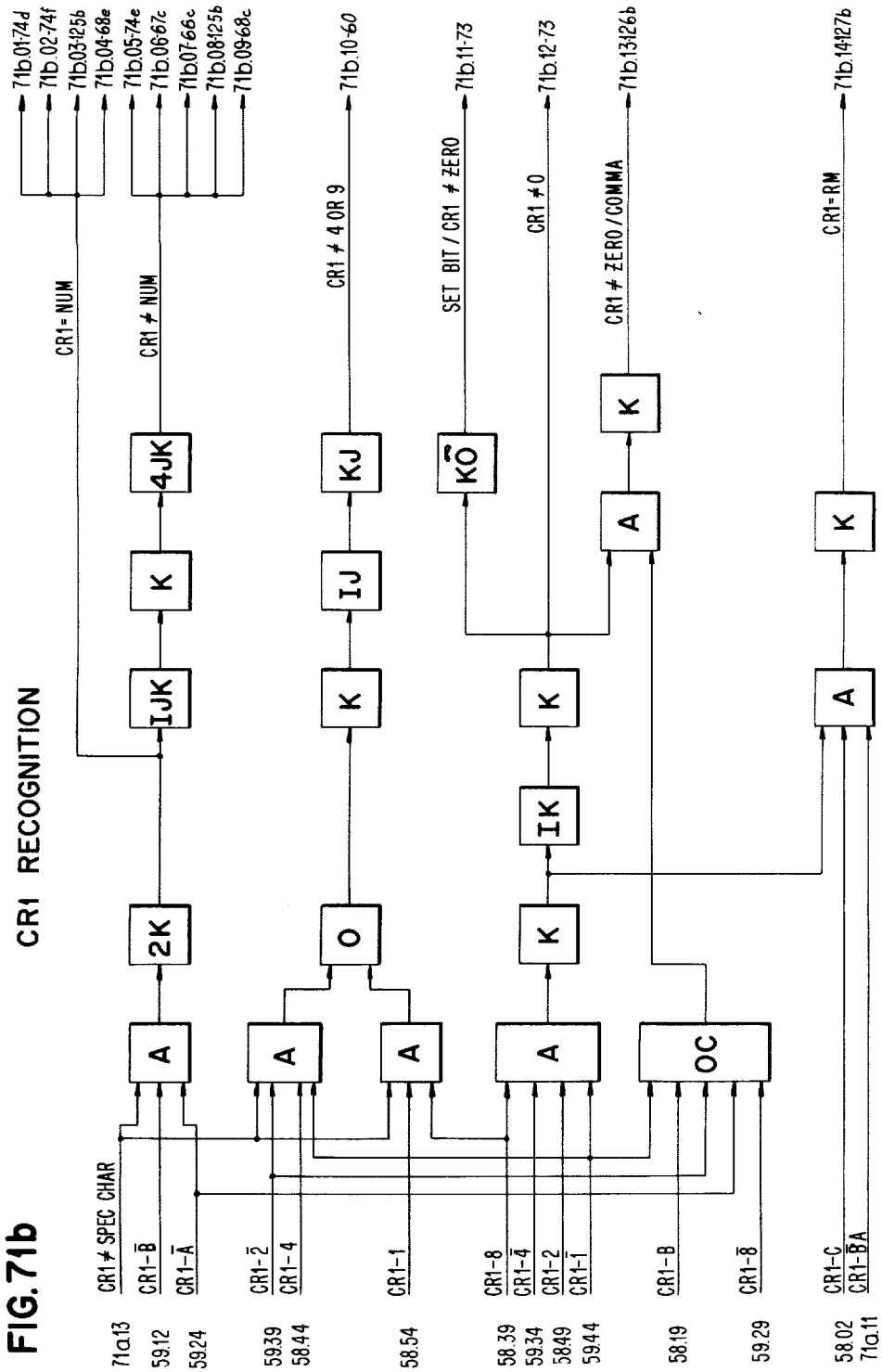

CR1 RECOGNITION
71b.01-74d
71b.02-74f
71b.03-125b
71b.04-68e
71b.05-74e
71b.06-67c
71b.07-66c
71b.08-125b
71b.09-68c
71b.10-60
71b.11-73
71b.12-73
71b.13-126b
71b.14-127b
CR1 = NUM
CR1 ≠ NUM
CR1 ≠ 4 OR 9
SET BIT / CR1 ≠ ZERO
CR1 ≠ 0
CR1 ≠ ZERO / COMMA
CR1 = RM
4JK
K
IJK
2K
KJ
IJ
K
O
KŌ
K
IK
K
K
A
K
A
A
A
A
OC
A
CR1 ≠ SPEC CHAR
CR1-B̄
CR1-Ā
CR1-2̄
CR1-4
CR1-1
CR1-8
CR1-4̄
CR1-2
CR1-1̄
CR1-B
CR1-8̄
CR1-C
CR1-B̄A
71a.13
59.12
59.24
59.39
58.44
58.54
58.39
59.34
58.49
59.44
58.19
59.29
58.02
71a.11

FIG. 71b

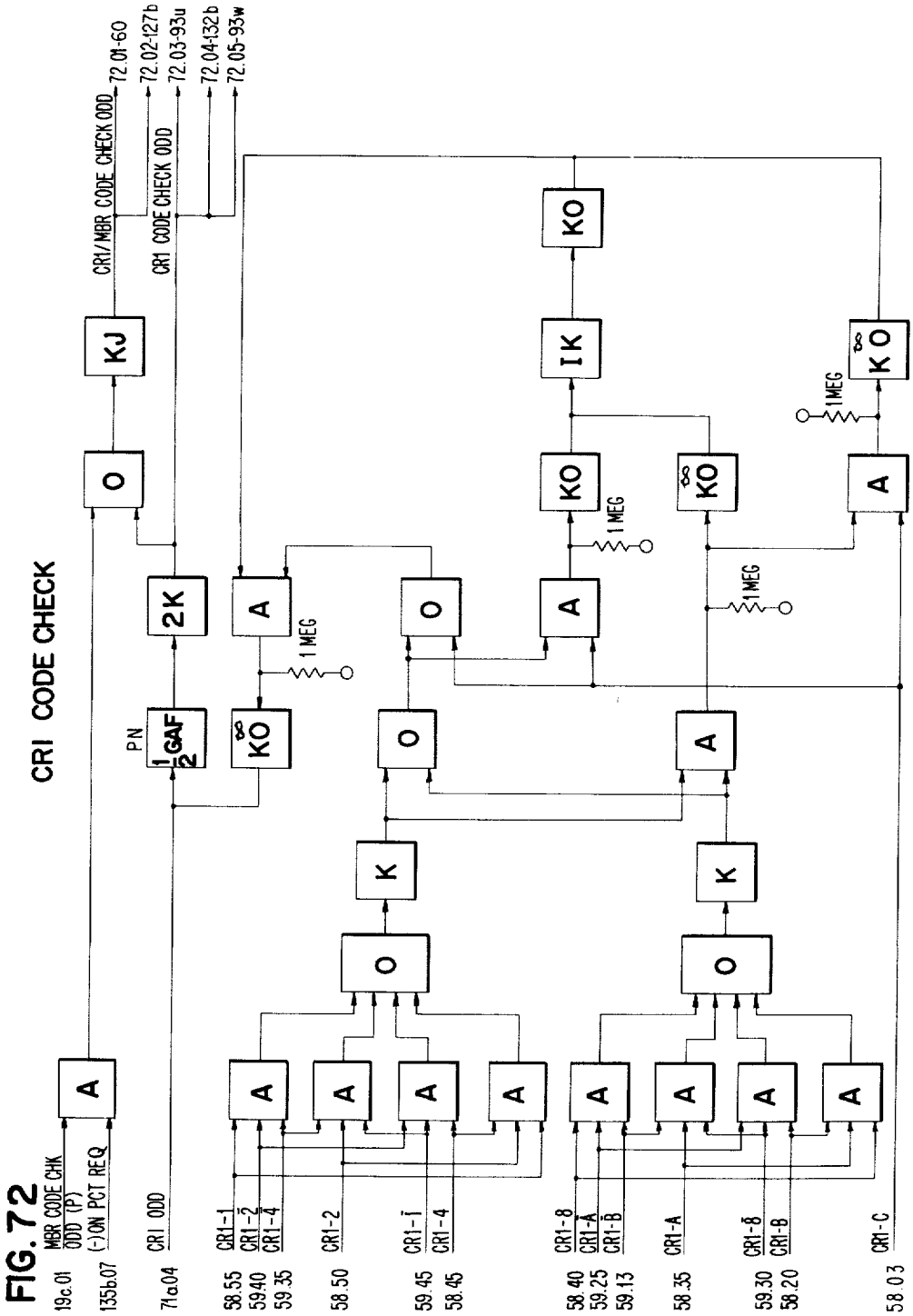

CRI CODE CHECK
CR1/MBR CODE CHECK ODD
CR1 CODE CHECK ODD
72.01-60
72.02-127b
72.03-93u
72.04-132b
72.05-93w
KJ
O
2K
1 GAF
P/N
A
KO
1 MEG
IK
K
MBR CODE CHK ODD (P)
(-)ON PCT REQ
CRI ODD
19c.01
135b.07
71a.04
CR1-1
CR1-2
CR1-4
CR1-i
CR1-8
CR1-A
CR1-B
CR1-C
58.55
59.40
59.35
58.50
59.45
58.45
58.40
59.25
59.13
58.35
59.30
58.20
58.03

FIG. 72

FIG. 73 ADDER INPUT SWITCHING

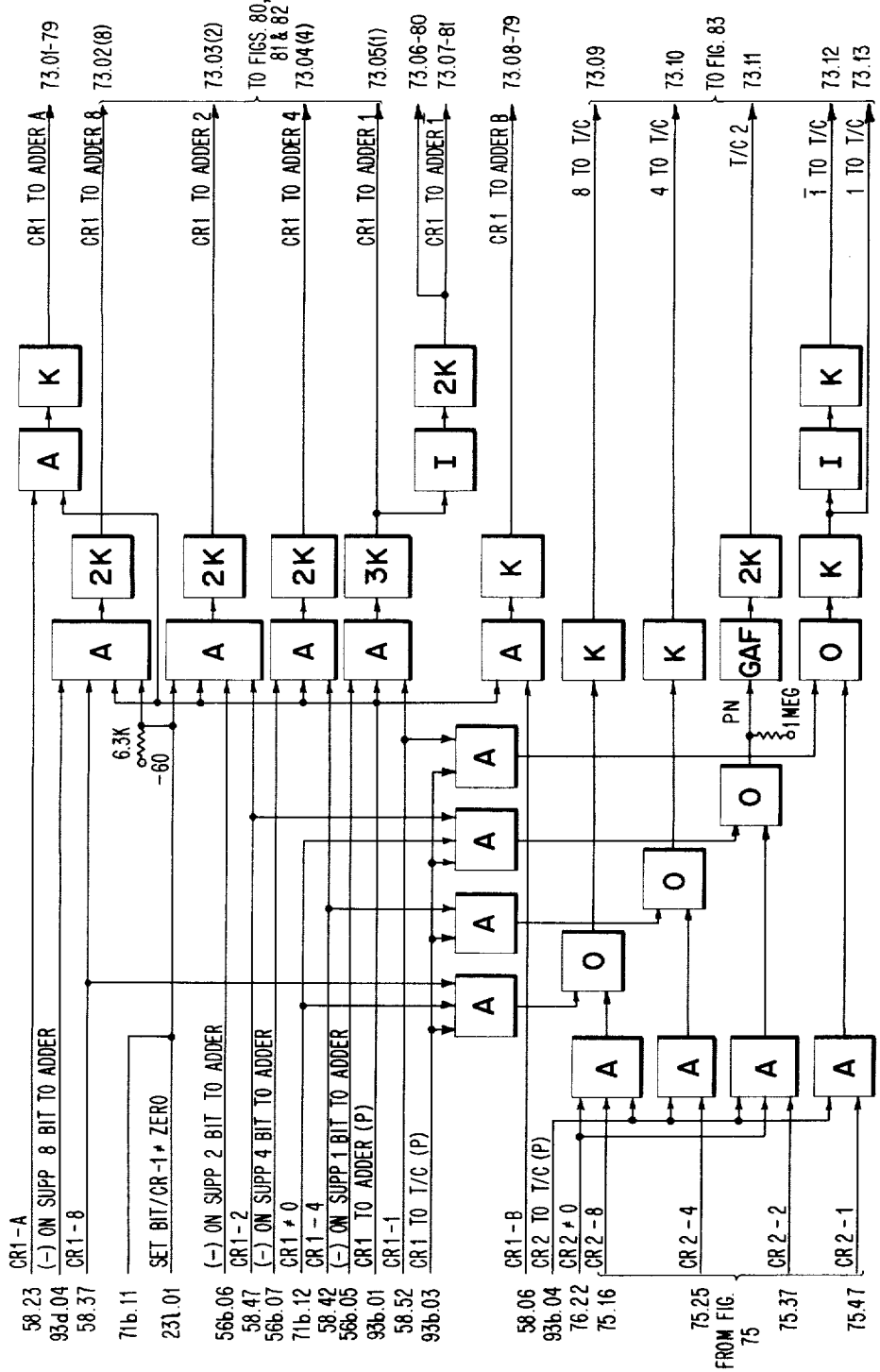
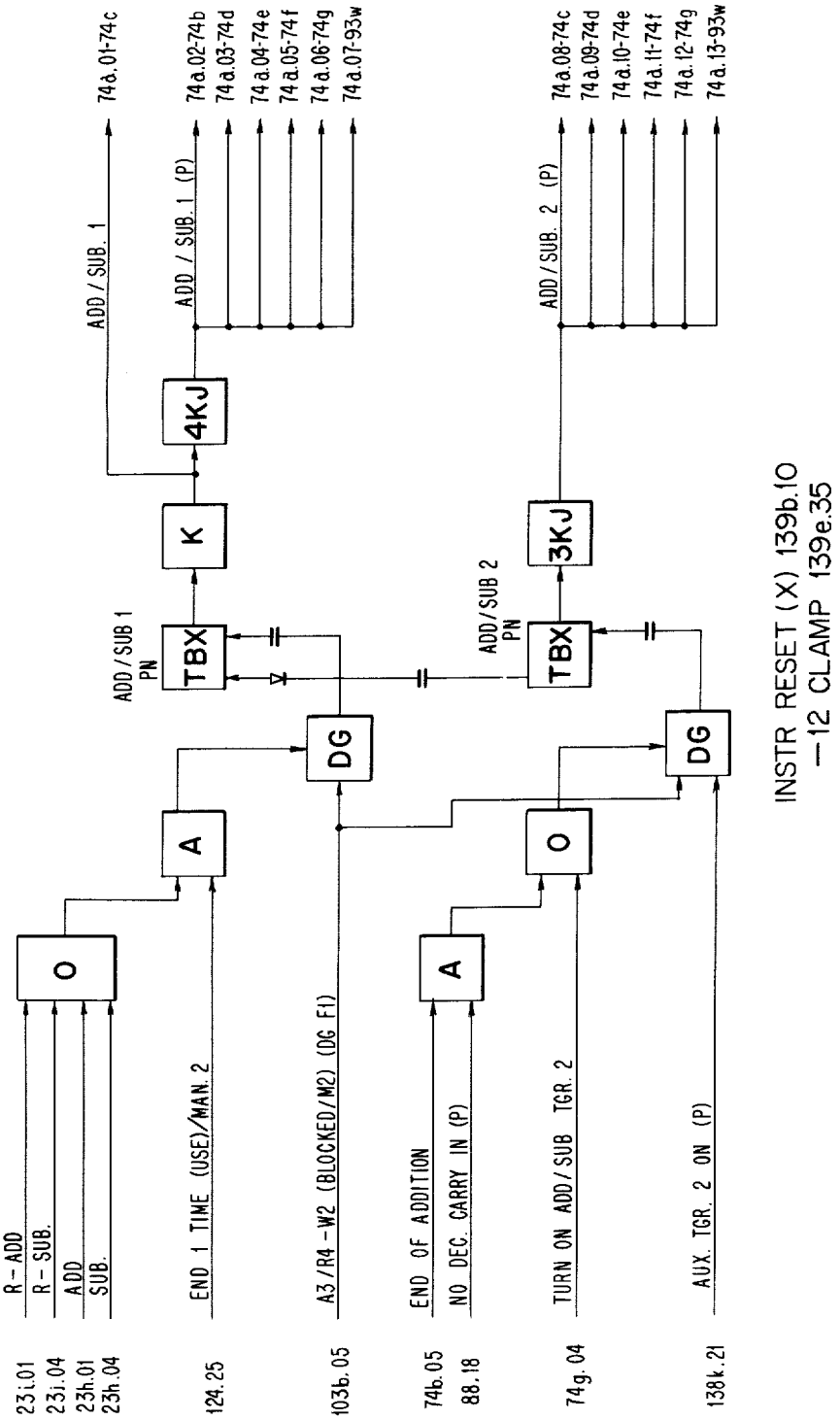


FIG. 74a

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS



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FIG. 74b

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS

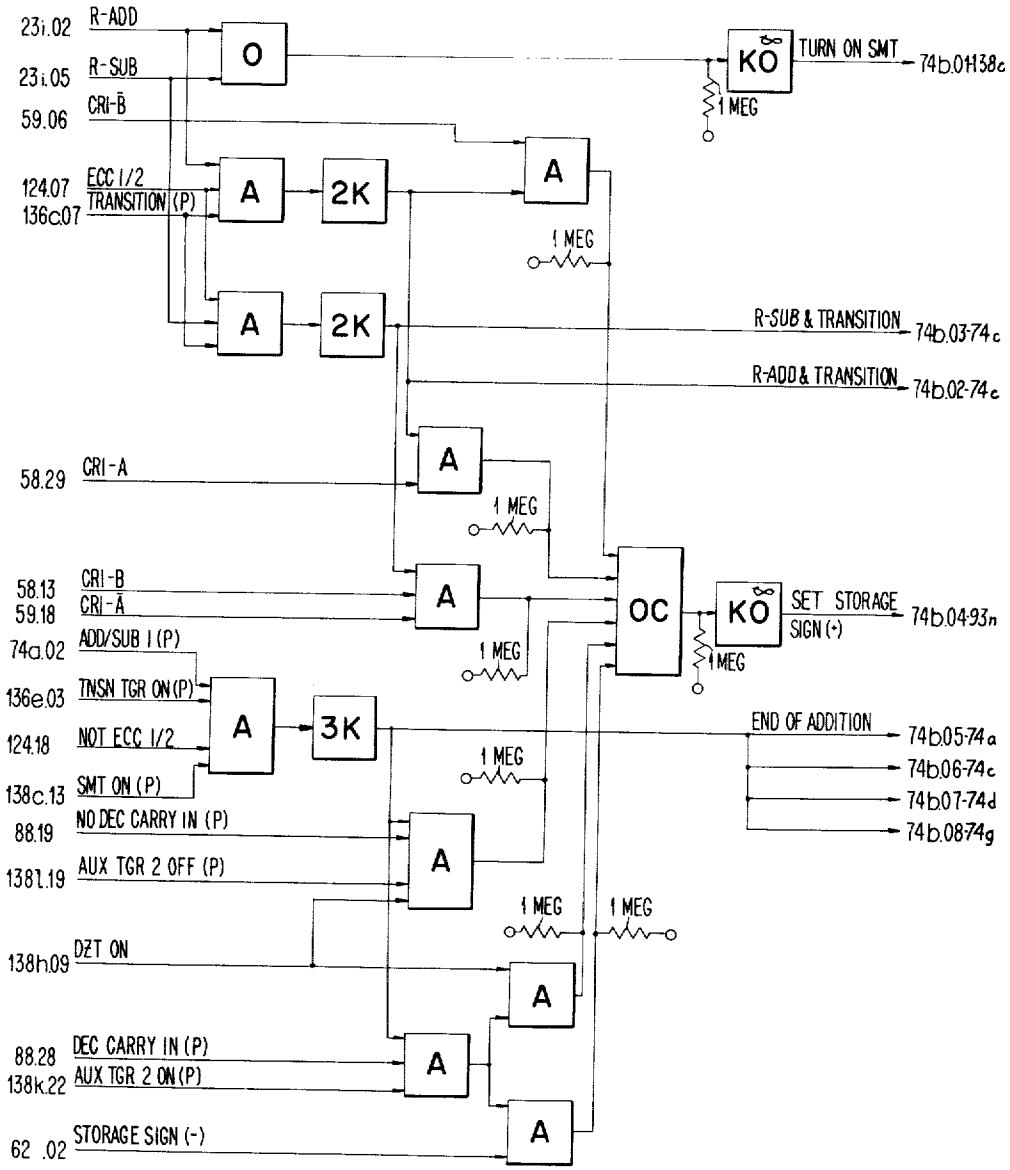
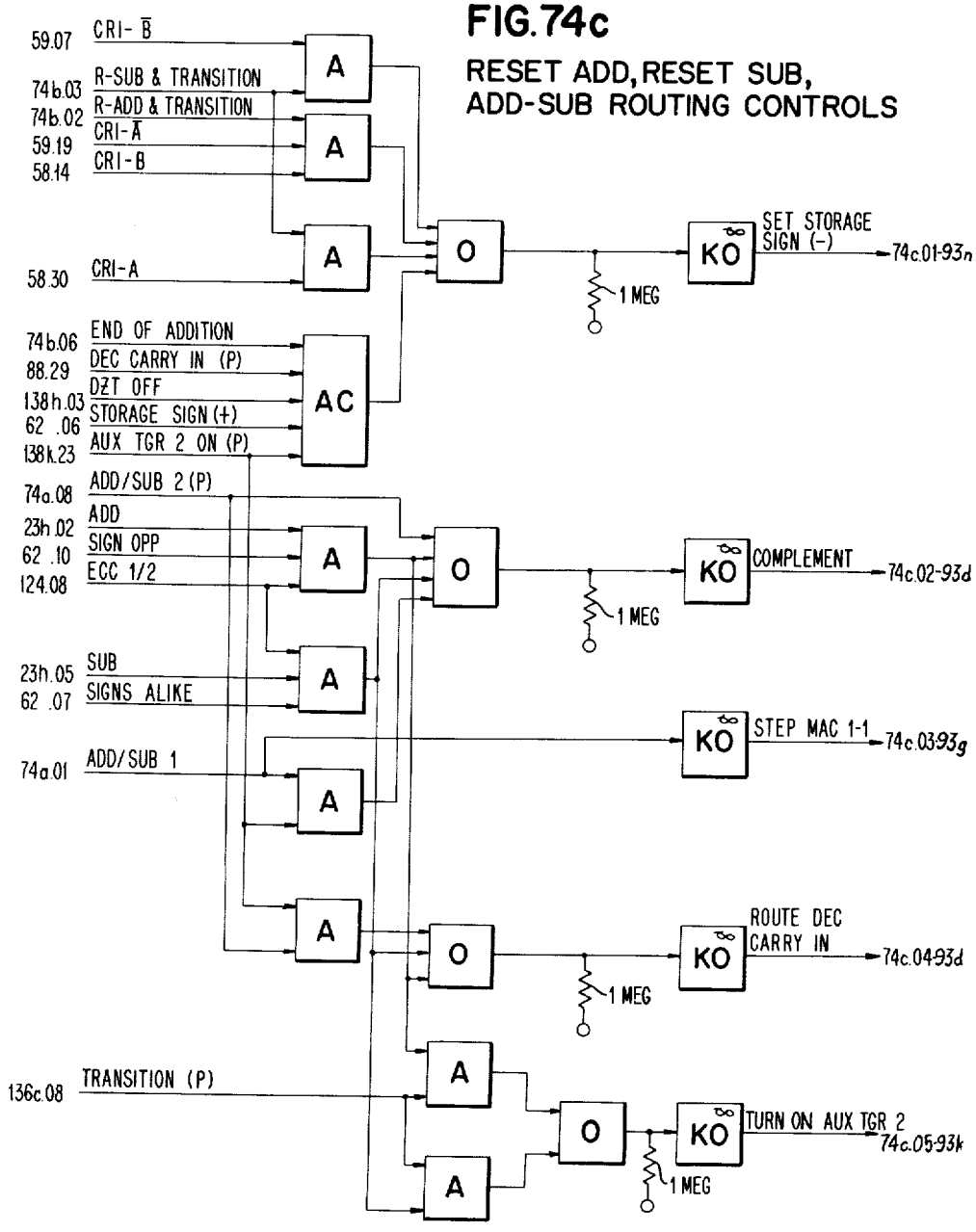


FIG. 74c

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS



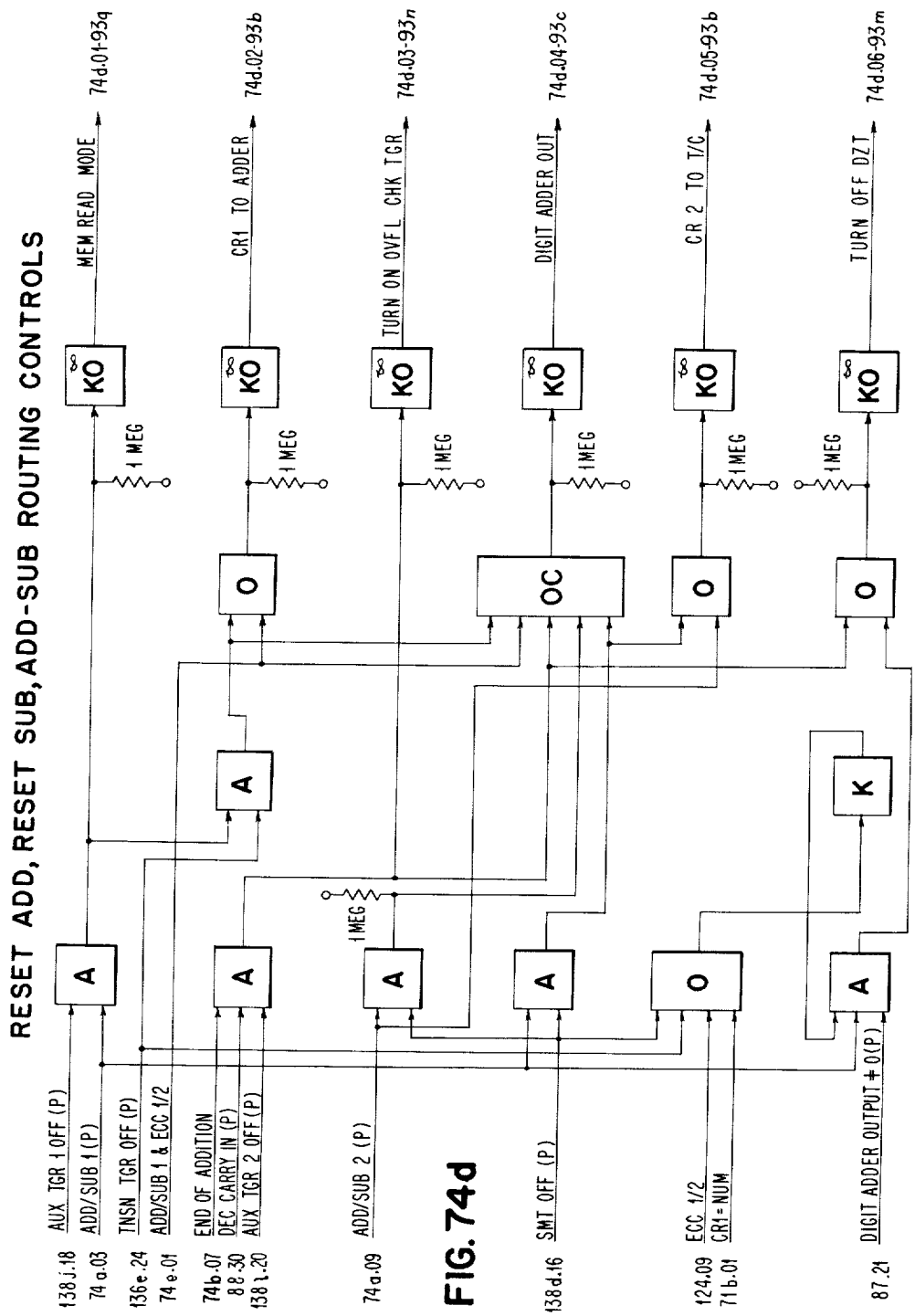

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS
MEM READ MODE
74d.01-93q
CR1 TO ADDER
74d.02-93b
TURN ON OVFL CHK TGR
74d.03-93n
DIGIT ADDER OUT
74d.04-93c
CR 2 TO T/C
74d.05-93b
TURN OFF DZT
74d.06-93m
KO
1 MEG
O
OC
A
K
AUX TGR 1 OFF (P)
138 i.18
ADD/SUB 1 (P)
74 a.03
TNSN TGR OFF (P)
136 e.24
ADD/SUB 1 & ECC 1/2
74 e.01
END OF ADDITION
74b.07
DEC CARRY IN (P)
8 8.30
AUX TGR 2 OFF (P)
138 i.20
ADD/SUB 2 (P)
74 a.09
SMT OFF (P)
138 d.16
ECC 1/2
124.09
CR1=NUM
71 b.01
DIGIT ADDER OUTPUT + 0(P)
87.21

FIG. 74d

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FIG. 74e

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS

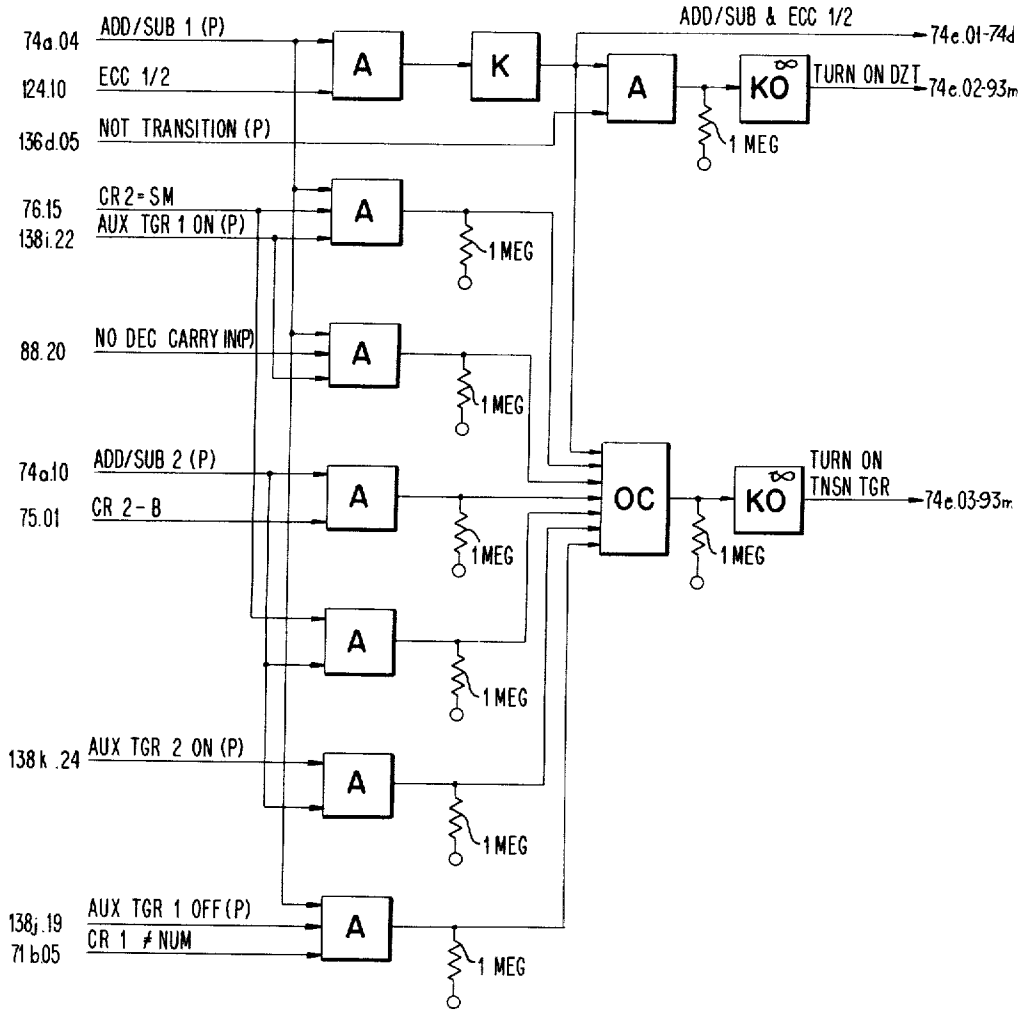
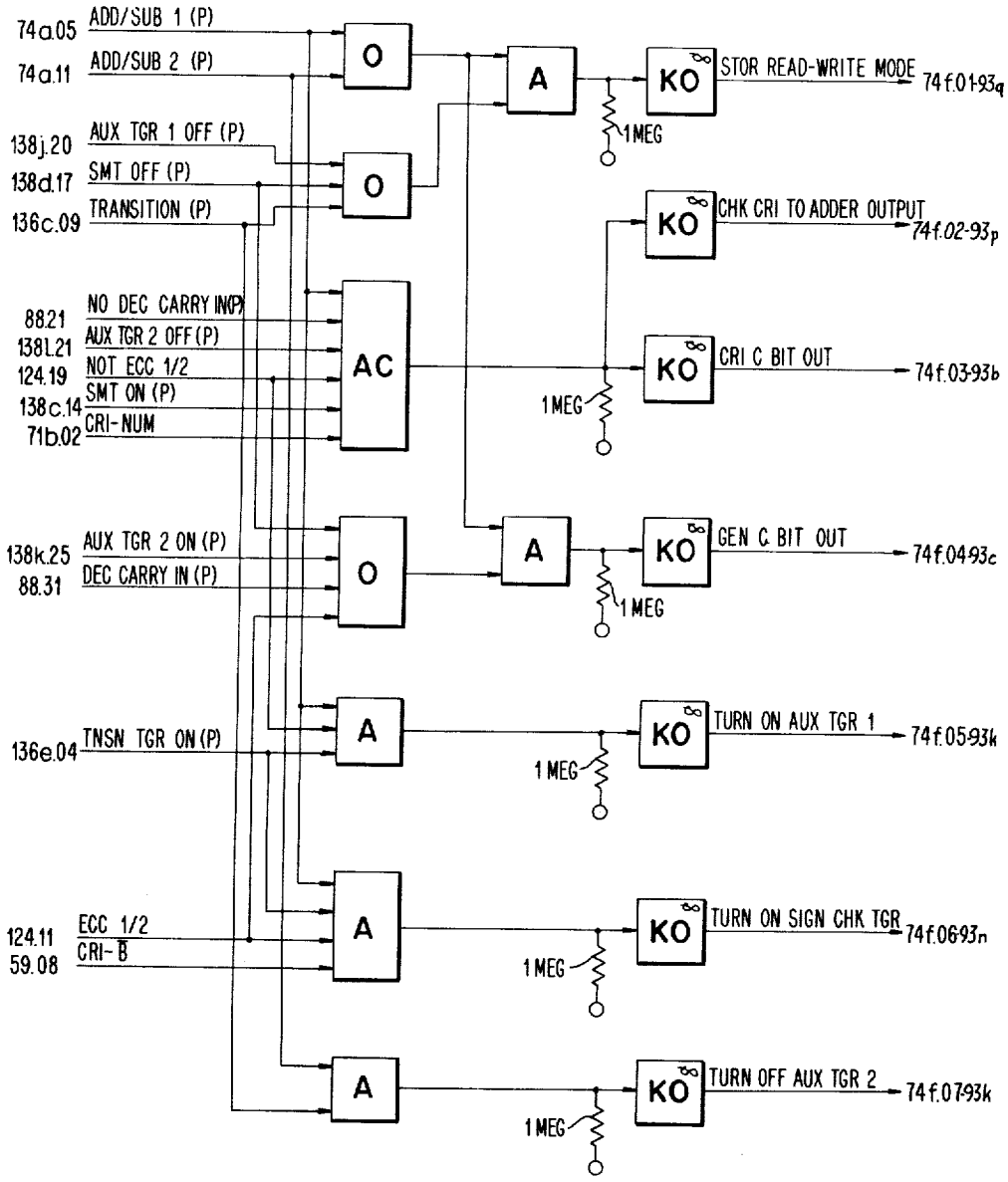


FIG. 74f

RESET ADD, RESET SUB, ADD-SUB ROUTING CONTROLS



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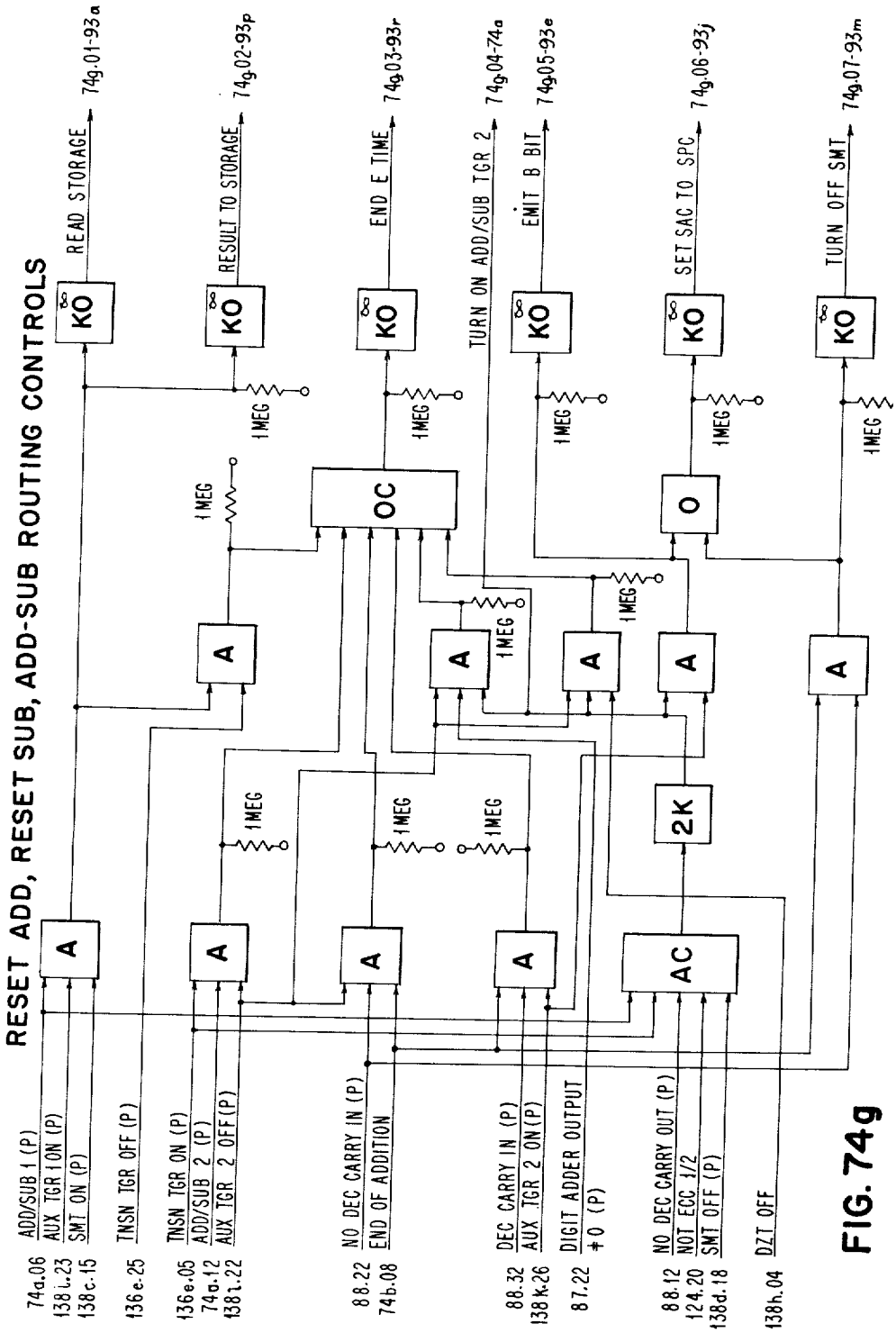
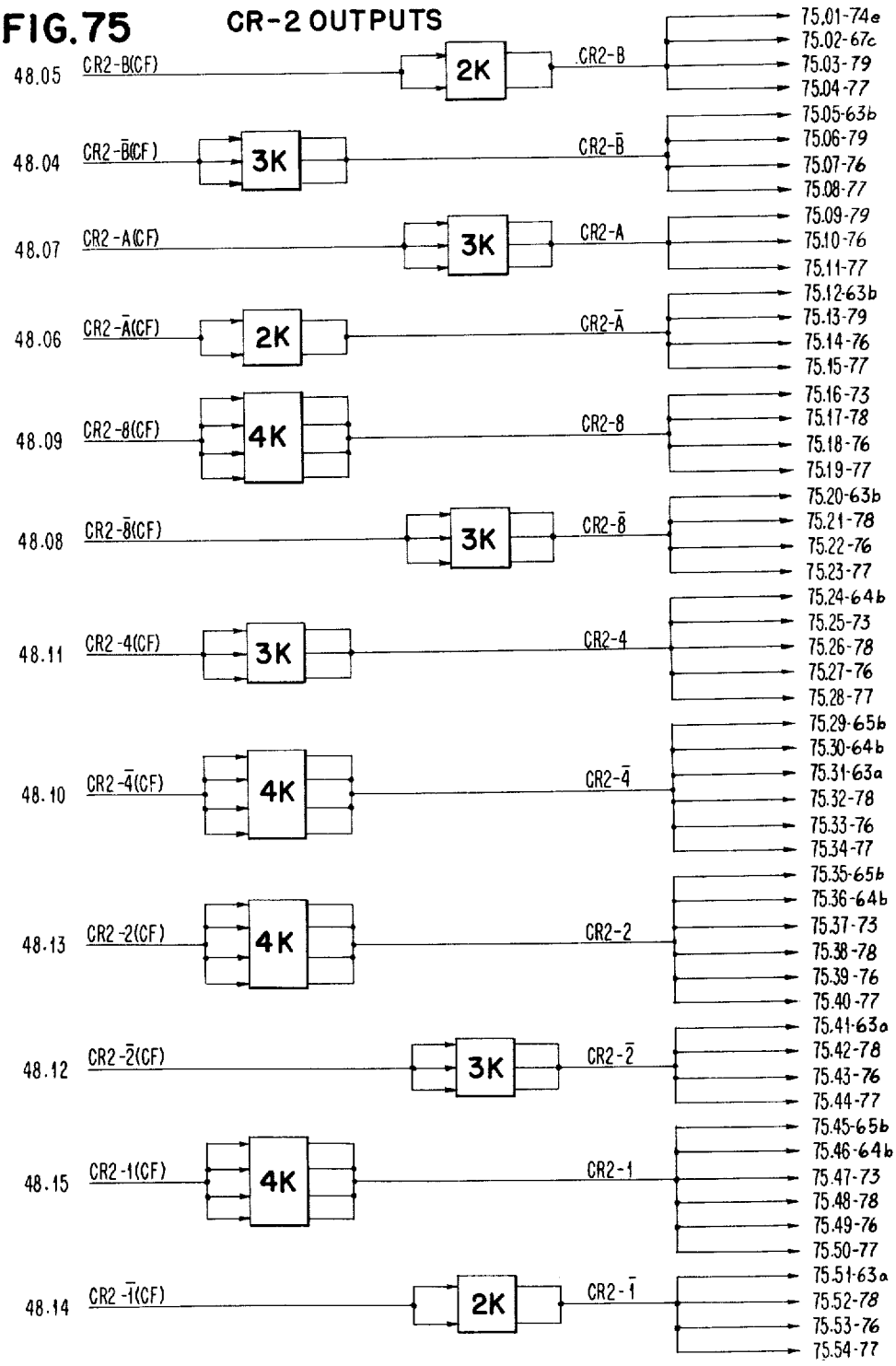


FIG. 74g

FIG. 75


CR-2 OUTPUTS
48.05
CR2-B(CF)
2K
CR2-B
75.01-74e
75.02-67c
75.03-79
75.04-77
48.04
CR2-B̄(CF)
3K
CR2-B̄
75.05-63b
75.06-79
75.07-76
75.08-77
48.07
CR2-A(CF)
3K
CR2-A
75.09-79
75.10-76
75.11-77
48.06
CR2-Ā(CF)
2K
CR2-Ā
75.12-63b
75.13-79
75.14-76
75.15-77
48.09
CR2-8(CF)
4K
CR2-8
75.16-73
75.17-78
75.18-76
75.19-77
48.08
CR2-8̄(CF)
3K
CR2-8̄
75.20-63b
75.21-78
75.22-76
75.23-77
48.11
CR2-4(CF)
3K
CR2-4
75.24-64b
75.25-73
75.26-78
75.27-76
75.28-77
48.10
CR2-4̄(CF)
4K
CR2-4̄
75.29-65b
75.30-64b
75.31-63a
75.32-78
75.33-76
75.34-77
48.13
CR2-2(CF)
4K
CR2-2
75.35-65b
75.36-64b
75.37-73
75.38-78
75.39-76
75.40-77
48.12
CR2-2̄(CF)
3K
CR2-2̄
75.41-63a
75.42-78
75.43-76
75.44-77
48.15
CR2-1(CF)
4K
CR2-1
75.45-65b
75.46-64b
75.47-73
75.48-78
75.49-76
75.50-77
48.14
CR2-1̄(CF)
2K
CR2-1̄
75.51-63a
75.52-78
75.53-76
75.54-77

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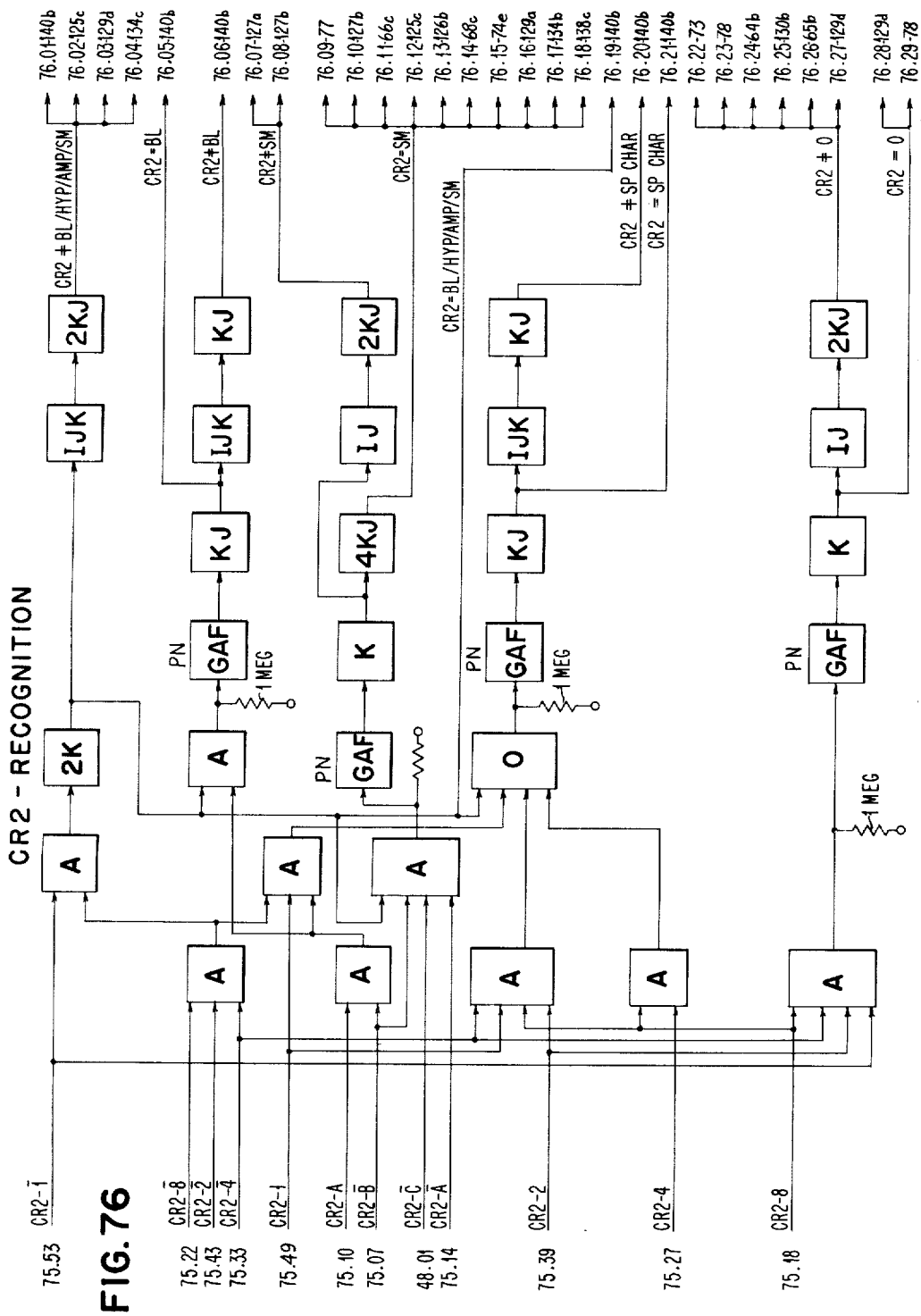
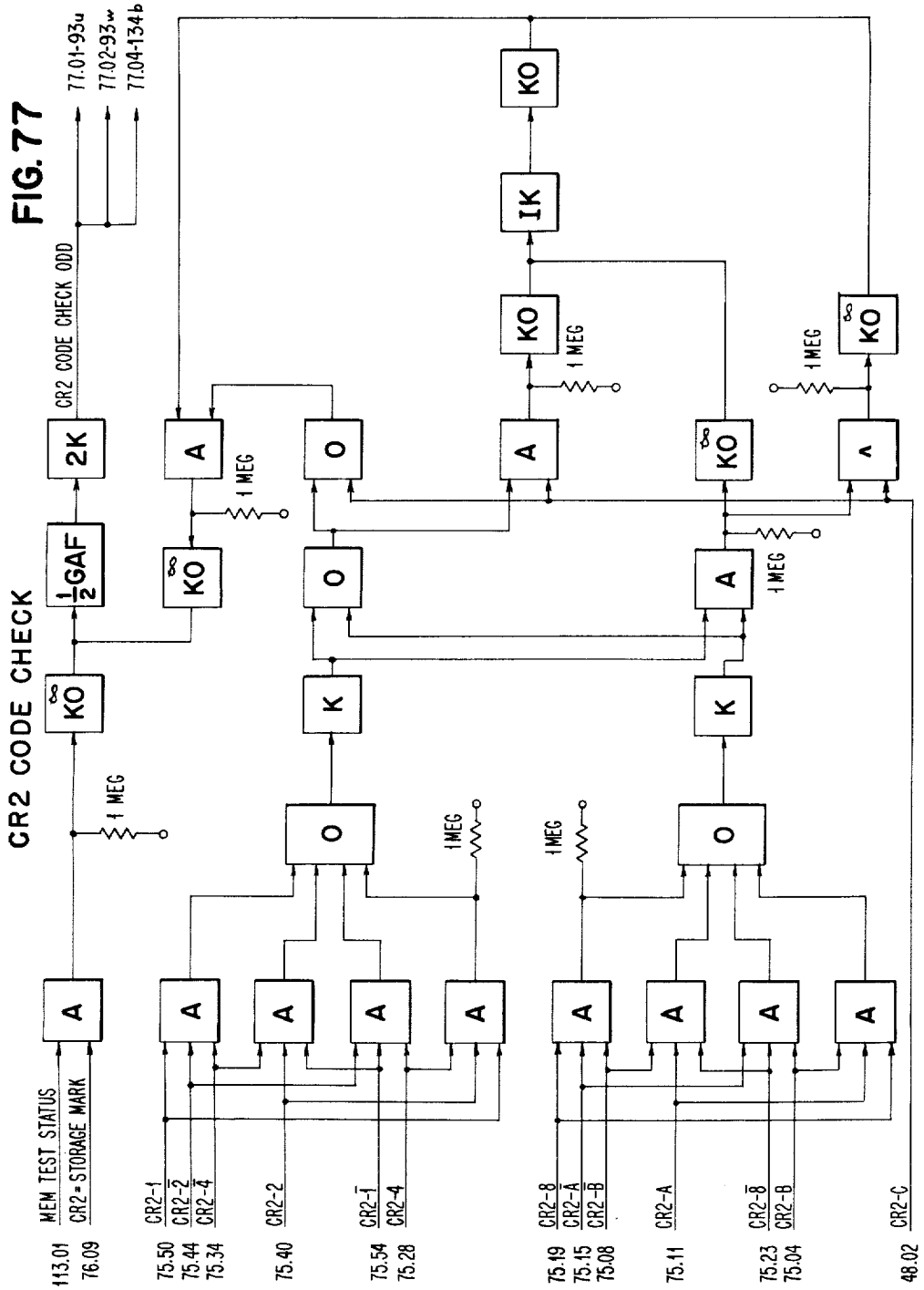


FIG. 76

FIG. 77


CR2 CODE CHECK
CR2 CODE CHECK ODD
77.01-93u
77.02-93w
77.04-134b
2K
½GAF
KO
A
O
K
IK
1 MEG
MEM TEST STATUS
CR2 • STORAGE MARK
113.01
76.09
CR2-1
CR2-2̄
CR2-4̄
CR2-2
CR2-1̄
CR2-4
CR2-8
CR2-Ā
CR2-B̄
CR2-A
CR2-8̄
CR2-B
CR2-C
75.50
75.44
75.34
75.40
75.54
75.28
75.19
75.15
75.08
75.11
75.23
75.04
48.02

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FIG. 78

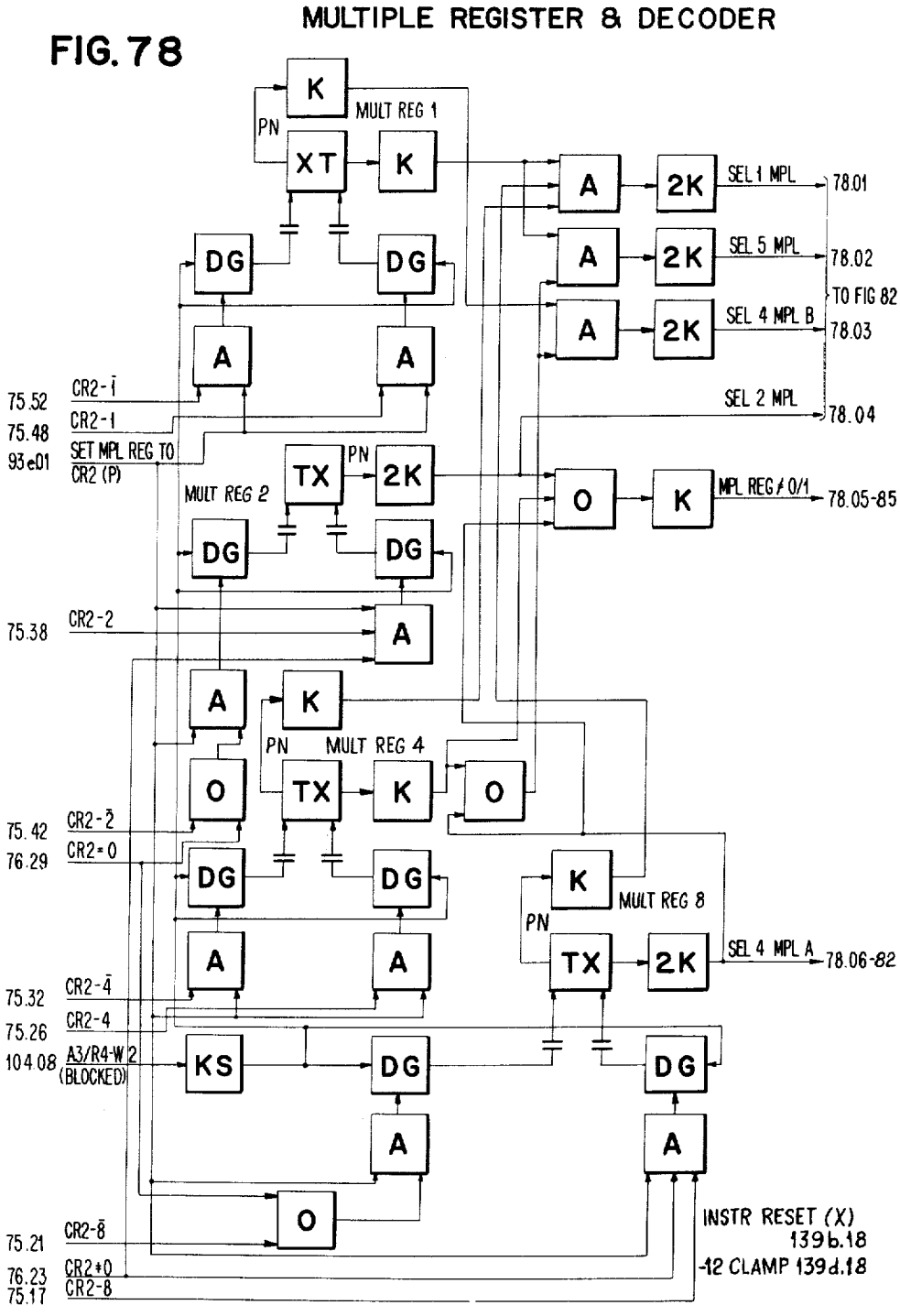
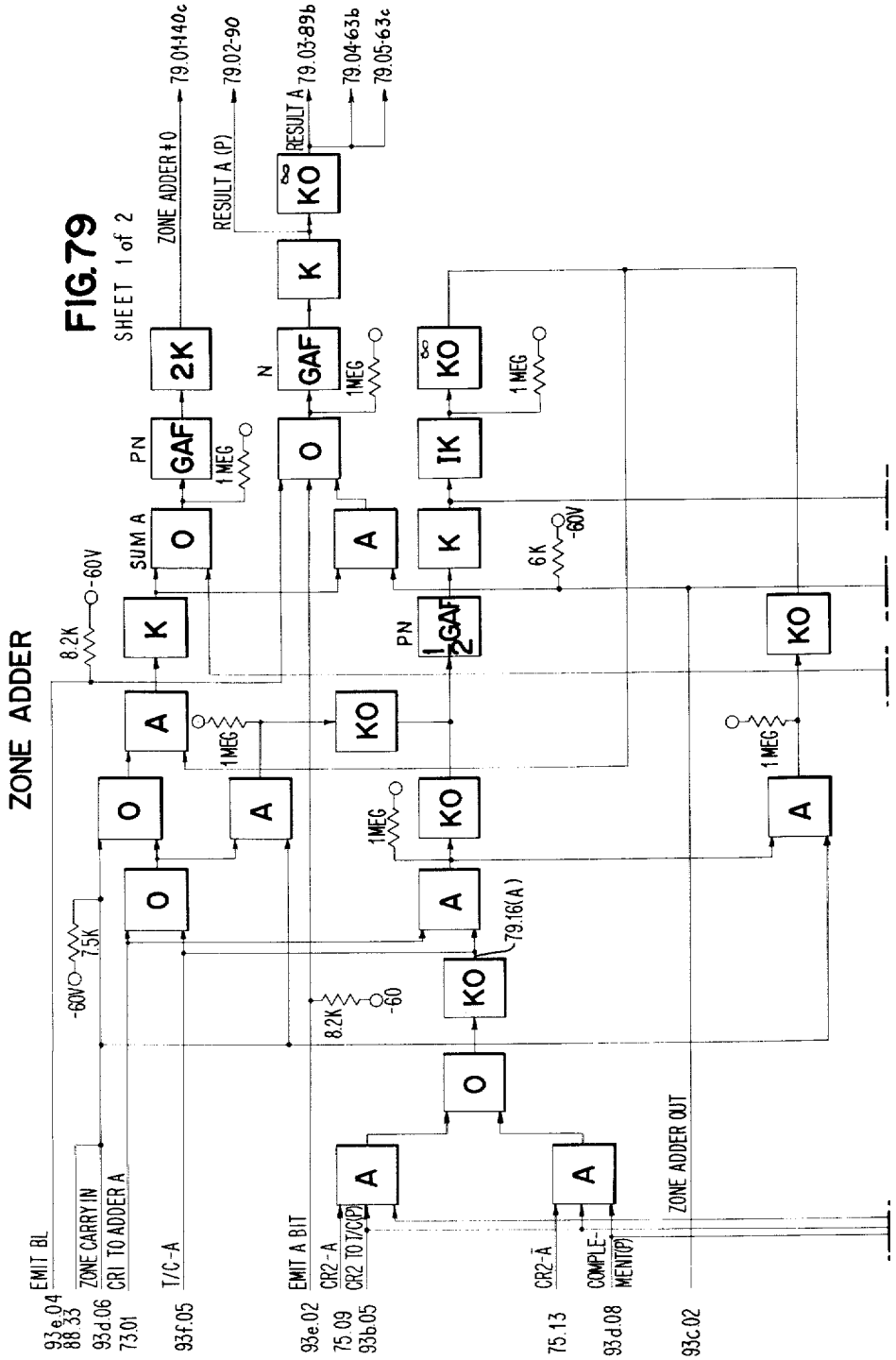


FIG. 79
SHEET 1 of 2



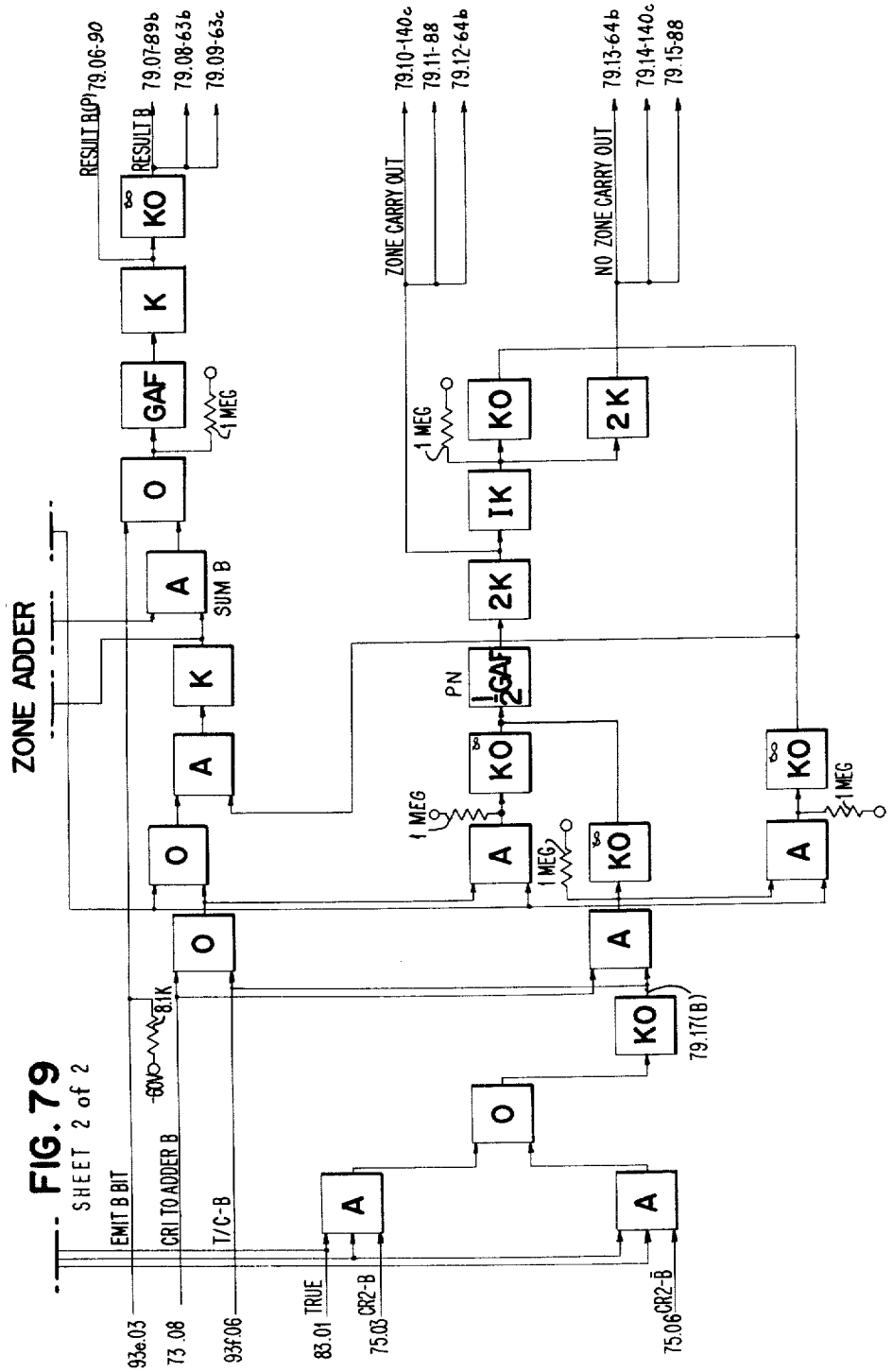


FIG. 79
SHEET 2 of 2

FIG.80 MULTIPLICAND DOUBLER & QUADRUPLER
SHEET 1 of 2

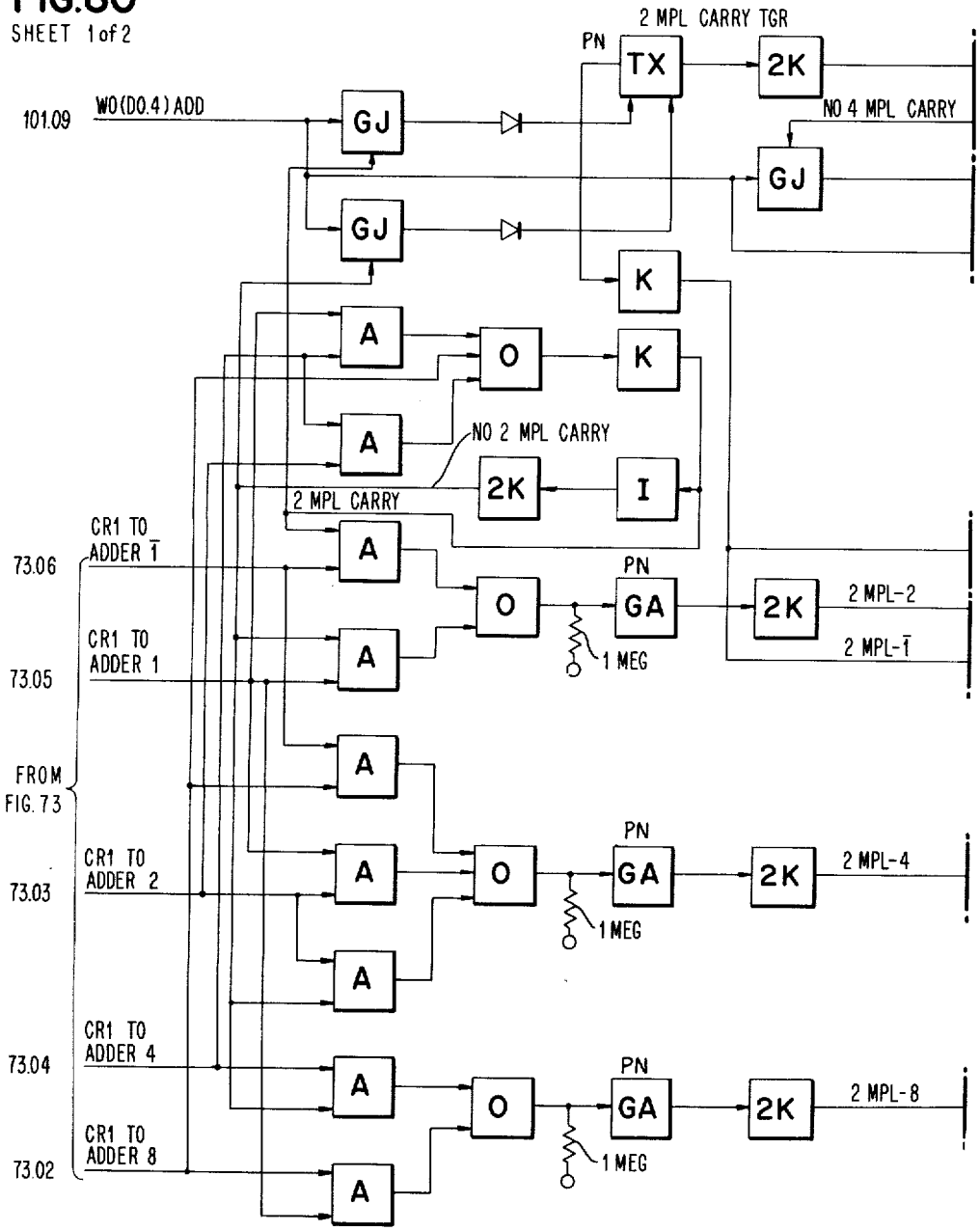
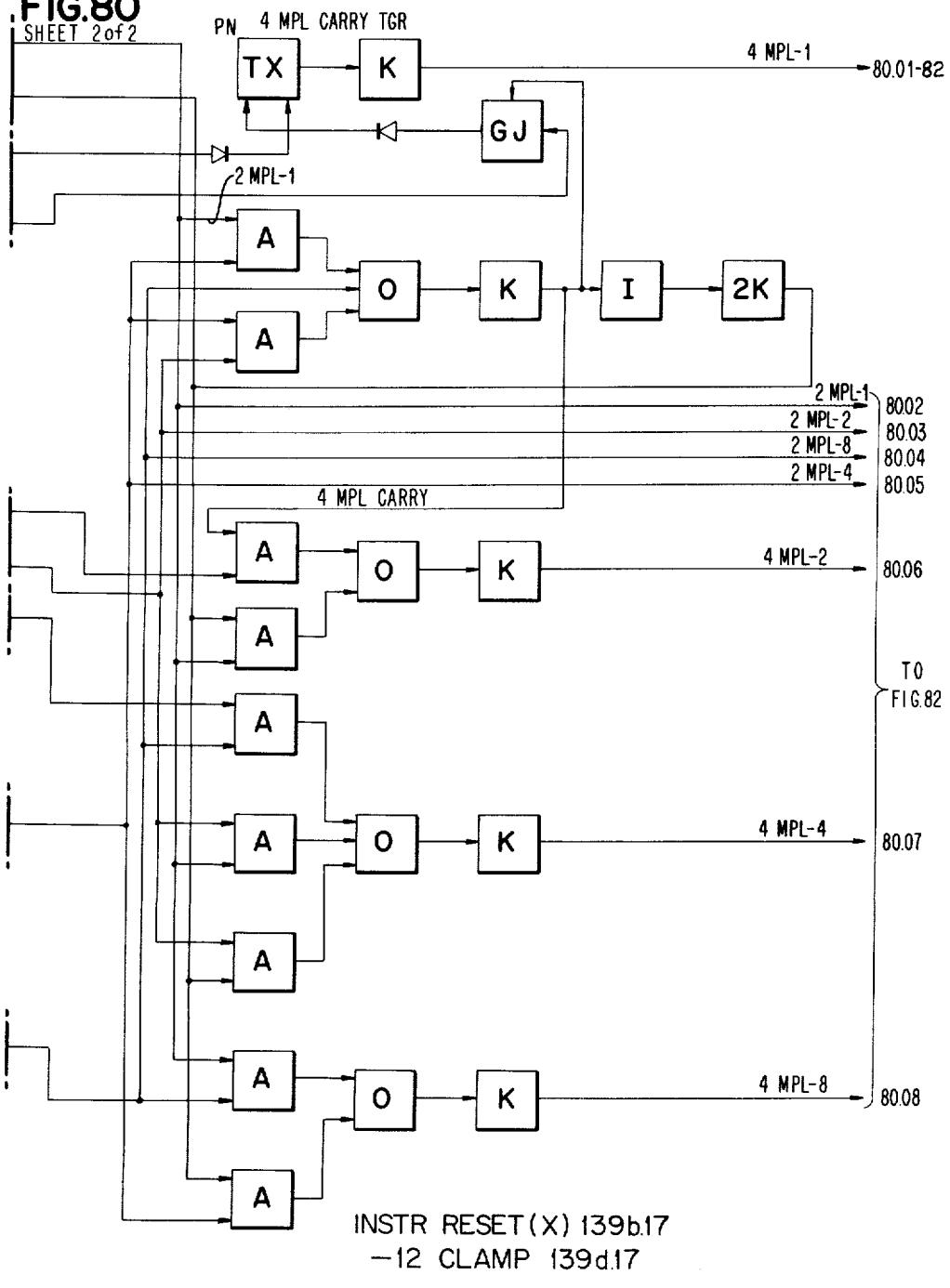


FIG.80
SHEET 2of2

MULTIPLICAND DOUBLER & QUADRUPLER



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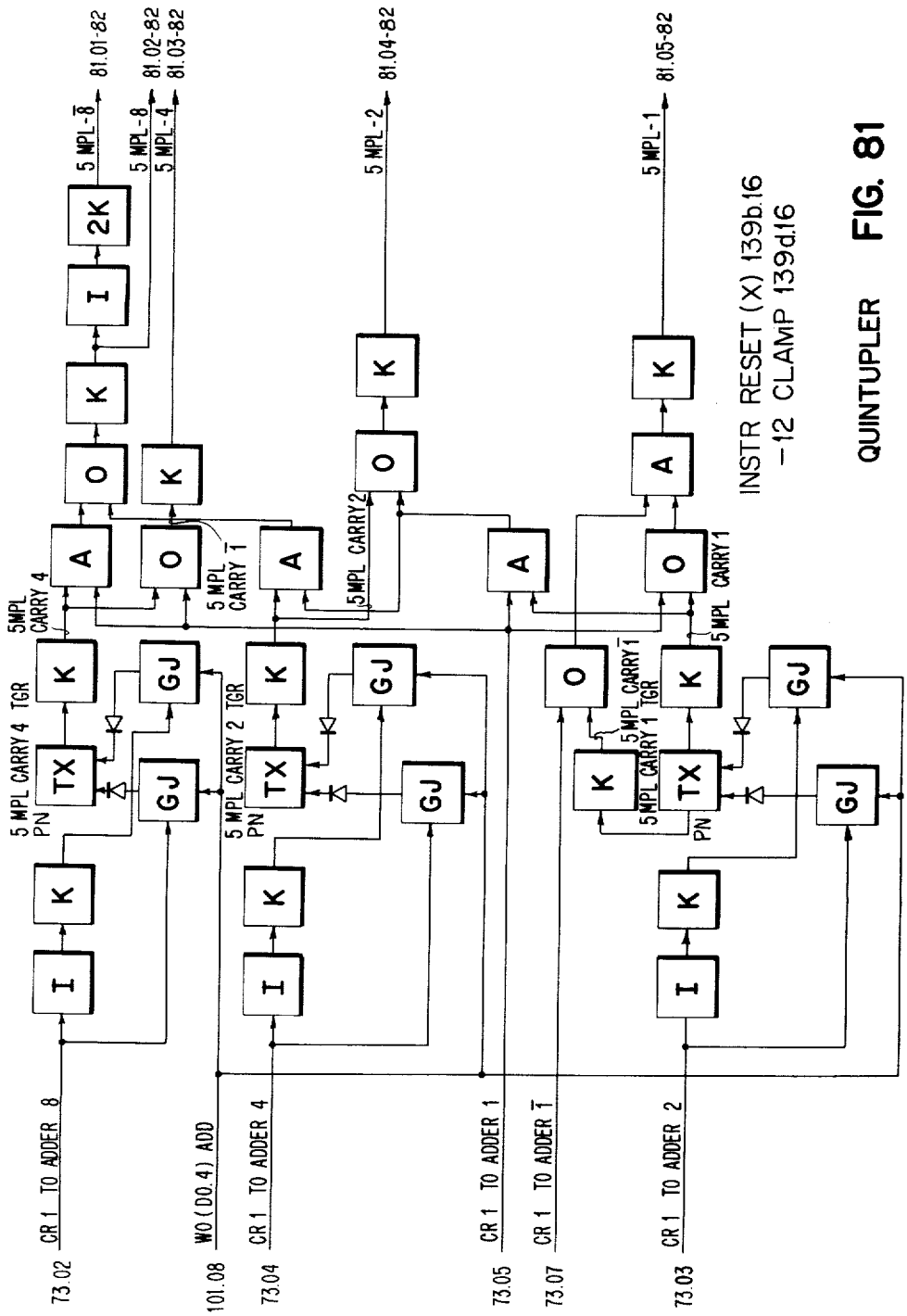
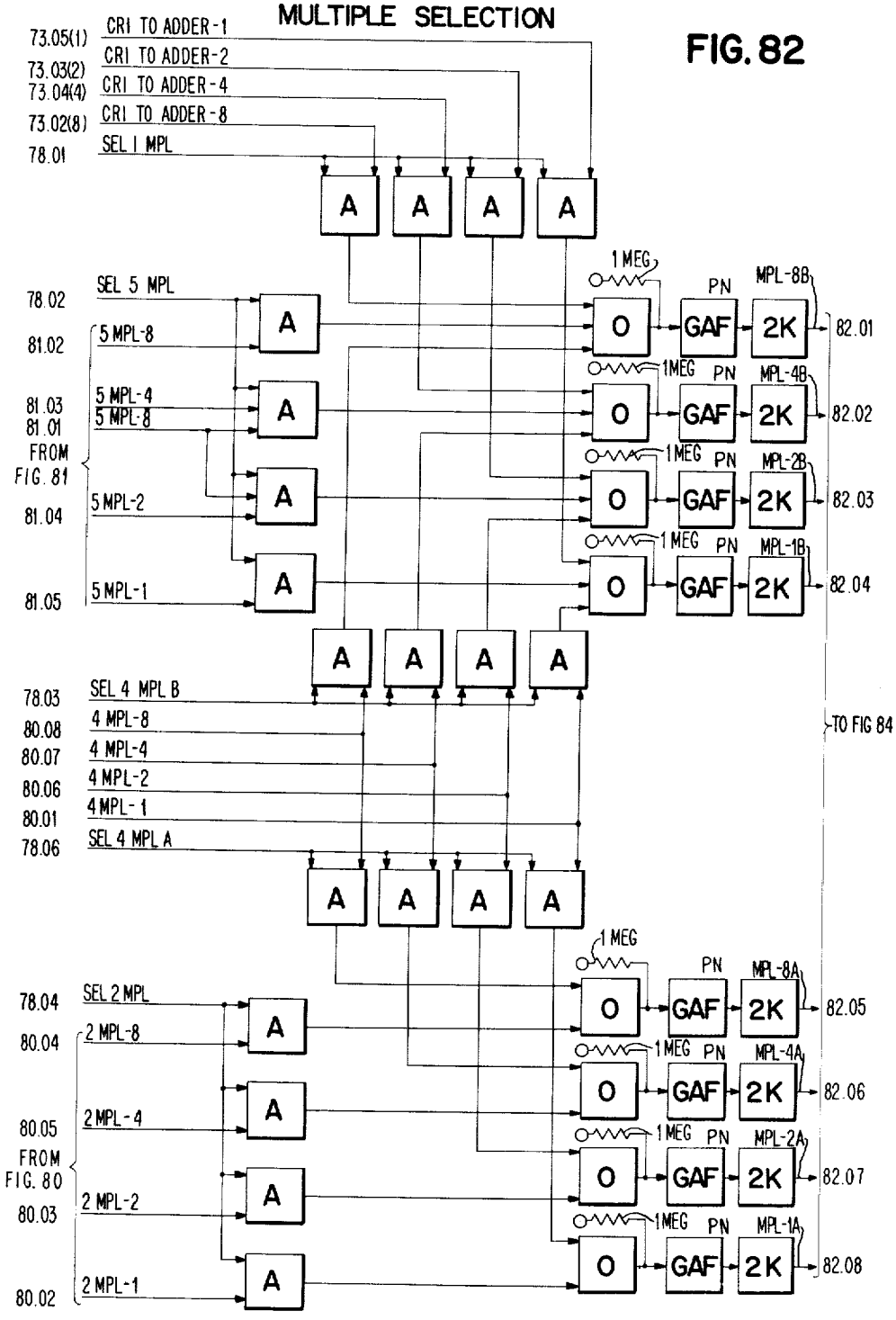


FIG. 81

MULTIPLE SELECTION

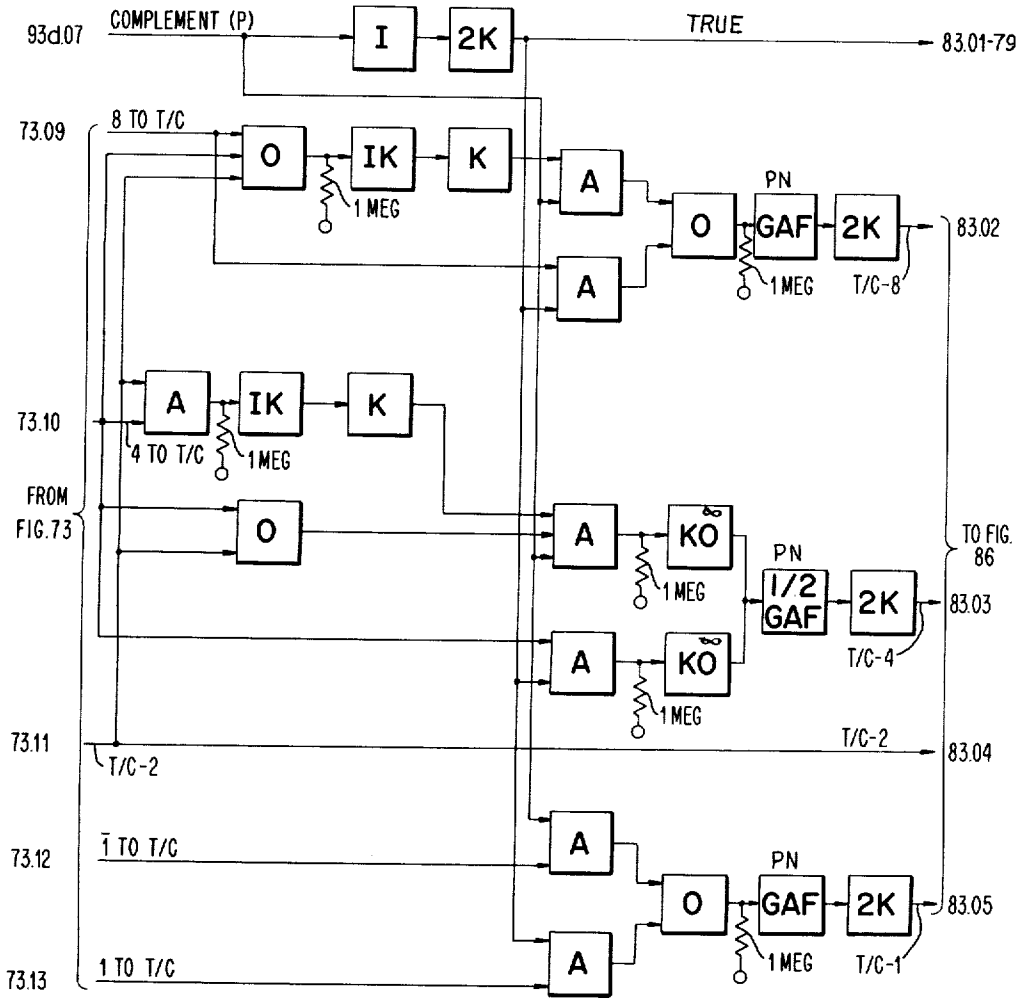
FIG. 82



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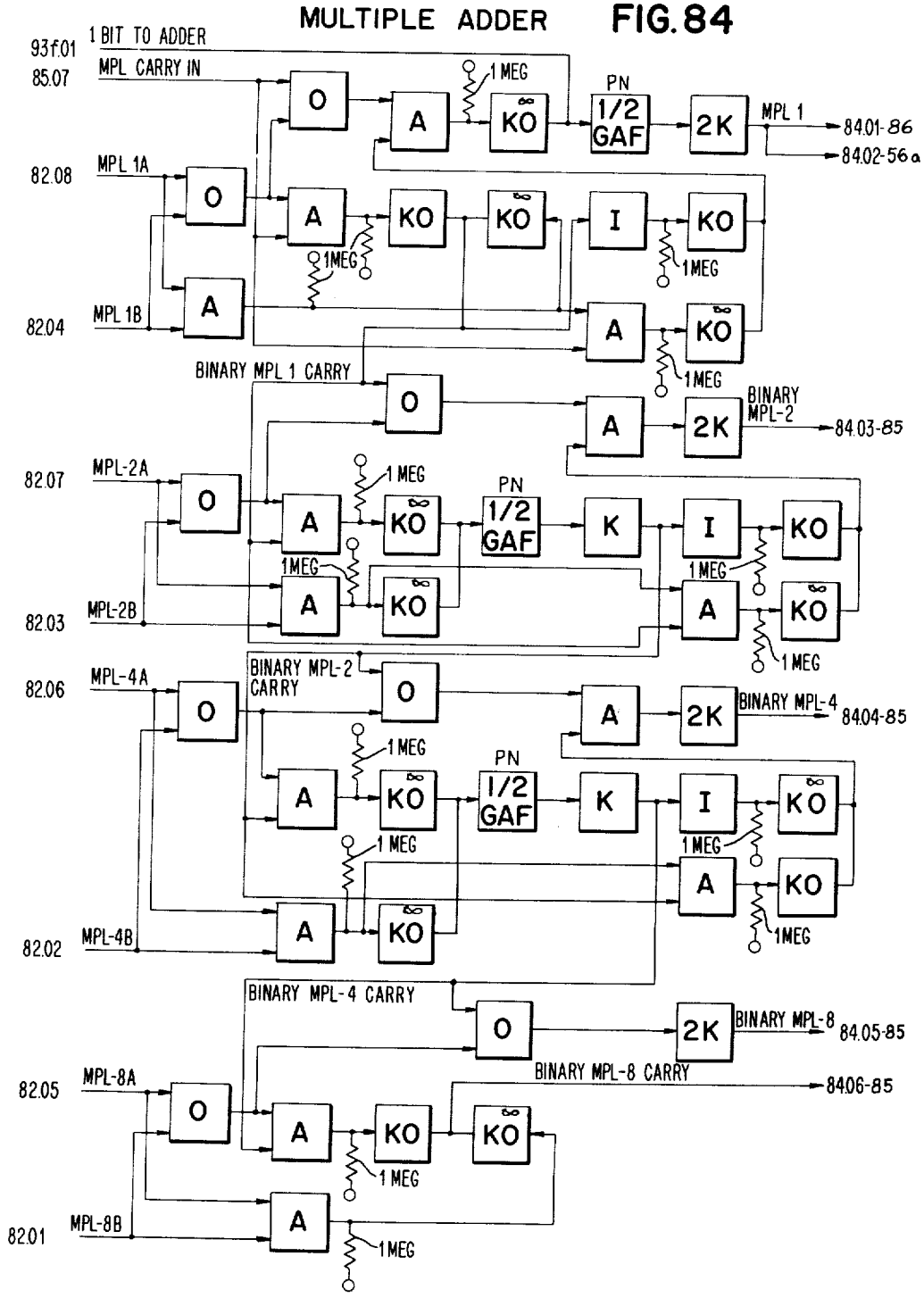
FIG.83

TRUE/COMP CONTROL



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MULTIPLE ADDER FIG. 84



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FIG. 85 DECIMAL CORRECTION CKTS

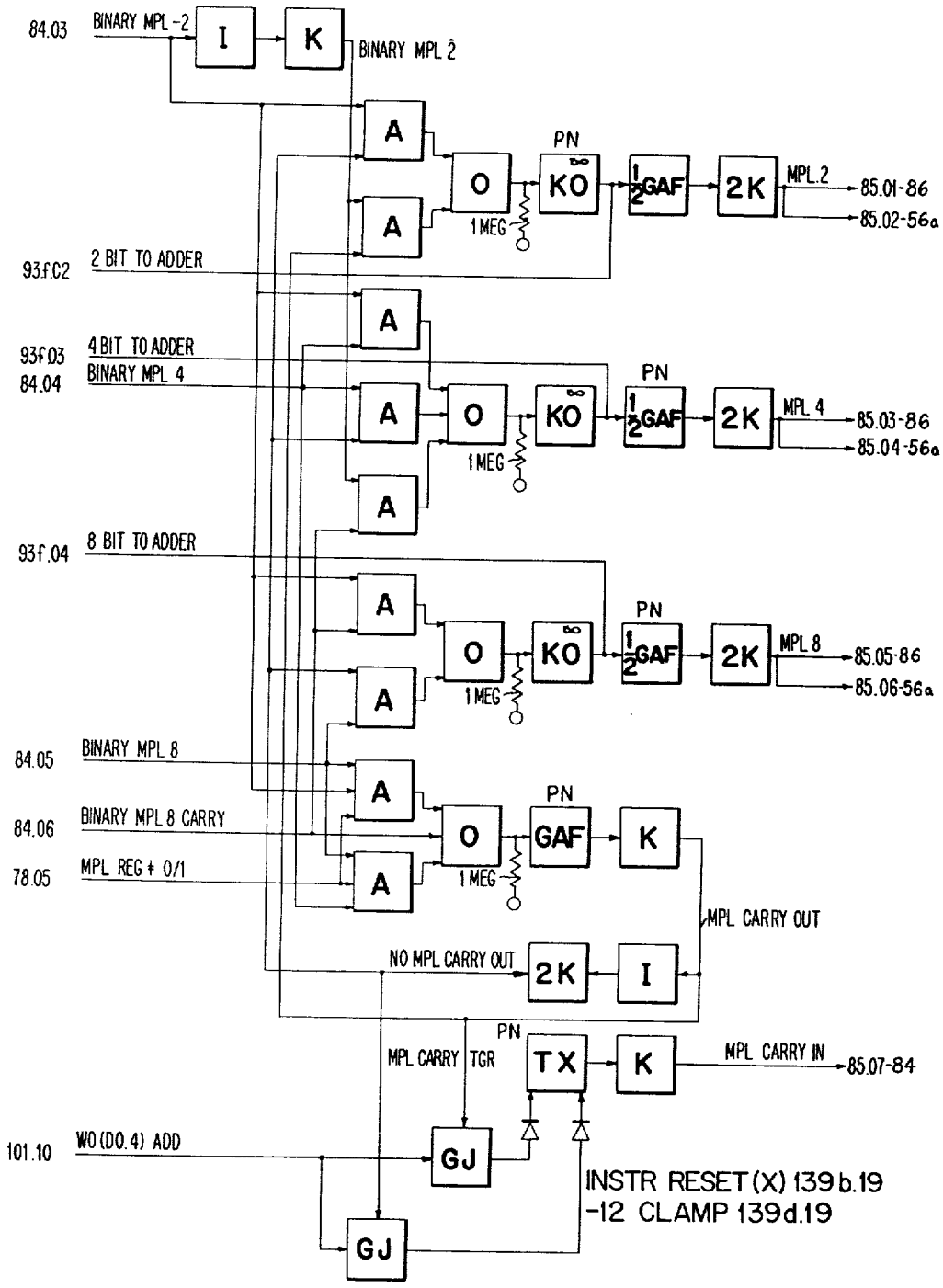
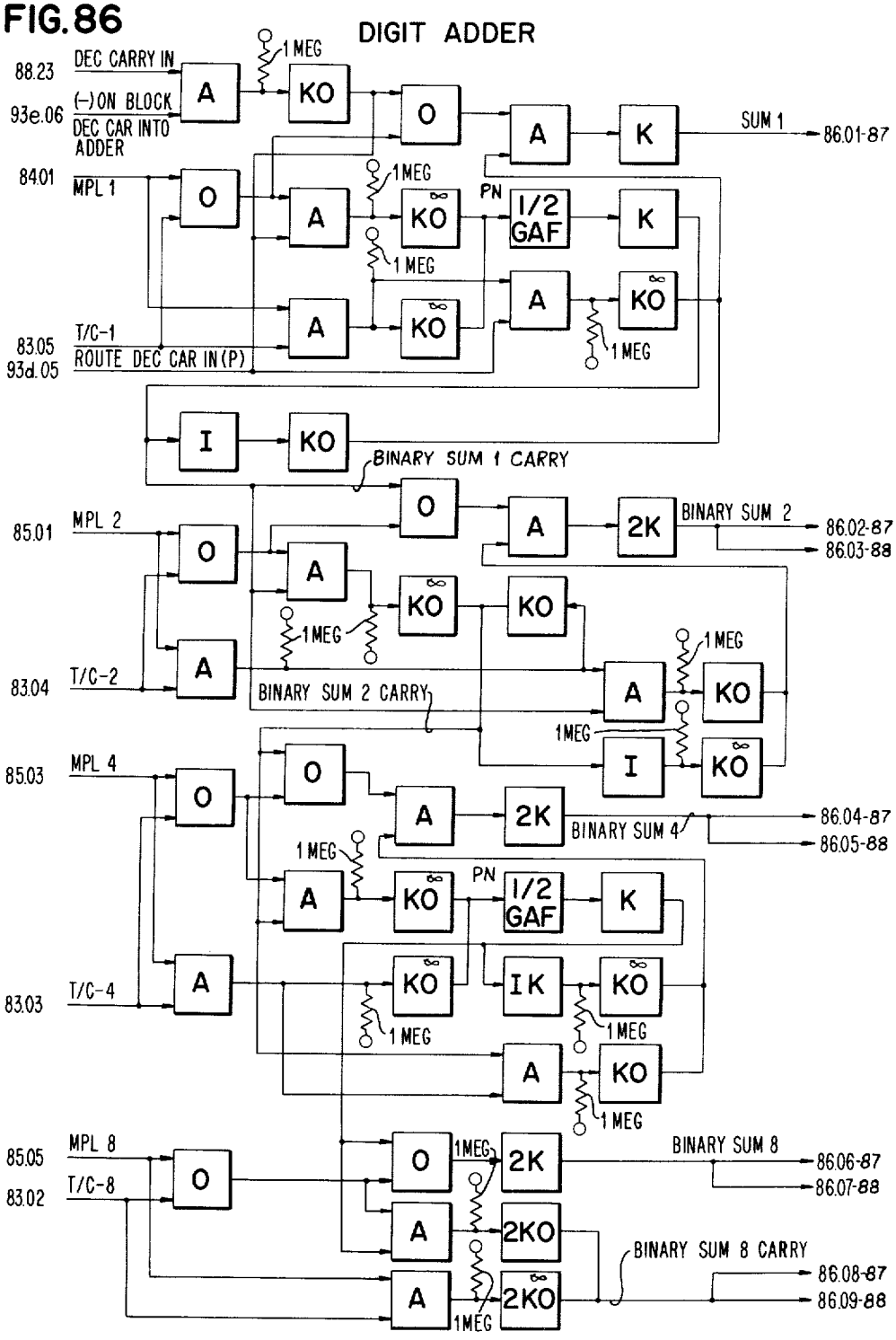


FIG. 86


DIGIT ADDER
88.23
DEC CARRY IN
93e.06
(-) ON BLOCK DEC CAR INTO ADDER
84.01
MPL 1
83.05
93d.05
T/C-1
ROUTE DEC CAR IN (P)
85.01
MPL 2
83.04
T/C-2
85.03
MPL 4
83.03
T/C-4
85.05
MPL 8
83.02
T/C-8
1 MEG
A
KO
O
K
SUM 1
86.01-87
PN
1/2 GAF
I
BINARY SUM 1 CARRY
2K
BINARY SUM 2
86.02-87
86.03-88
BINARY SUM 2 CARRY
BINARY SUM 4
86.04-87
86.05-88
IK
2KO
BINARY SUM 8
86.06-87
86.07-88
BINARY SUM 8 CARRY
86.08-87
86.09-88

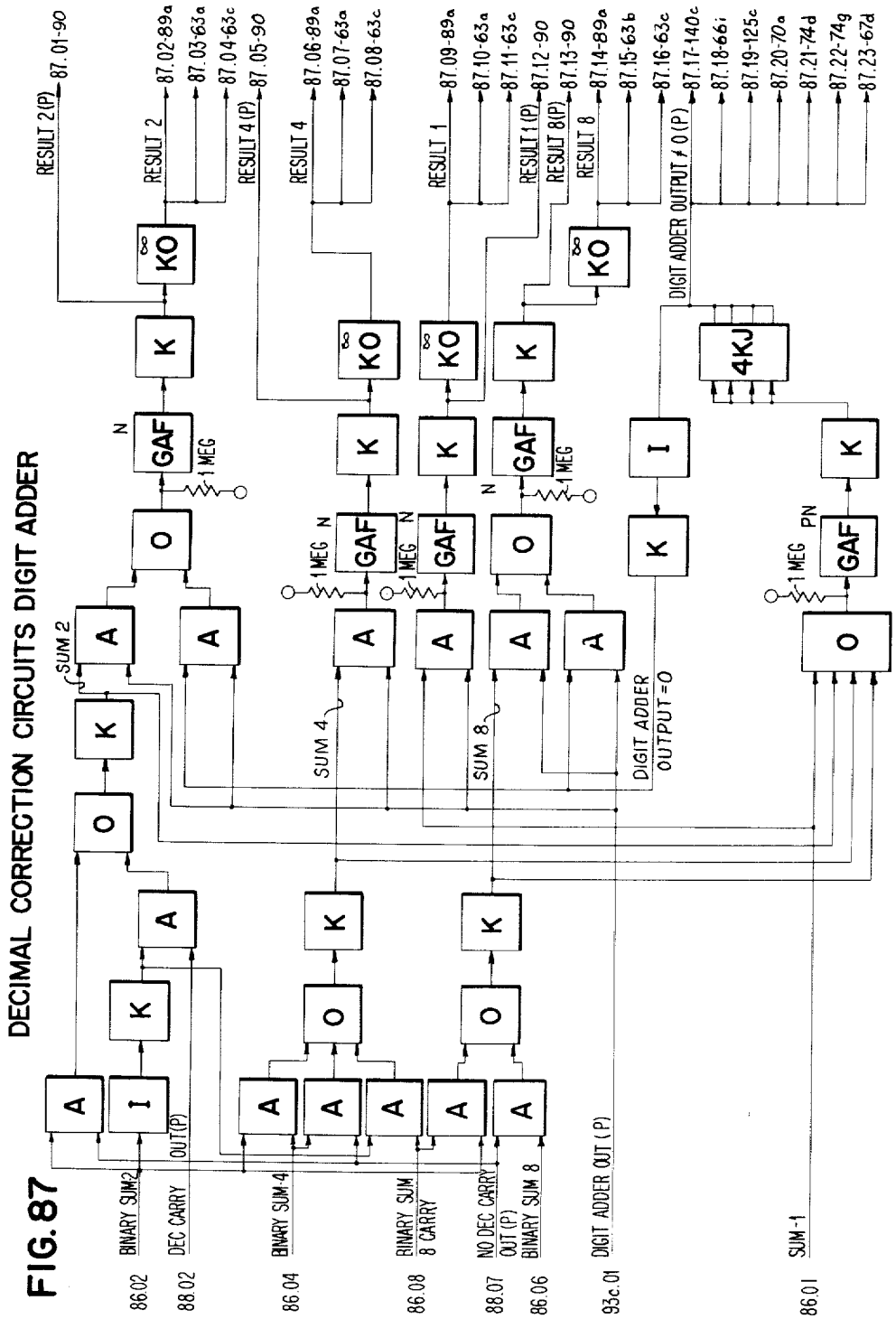
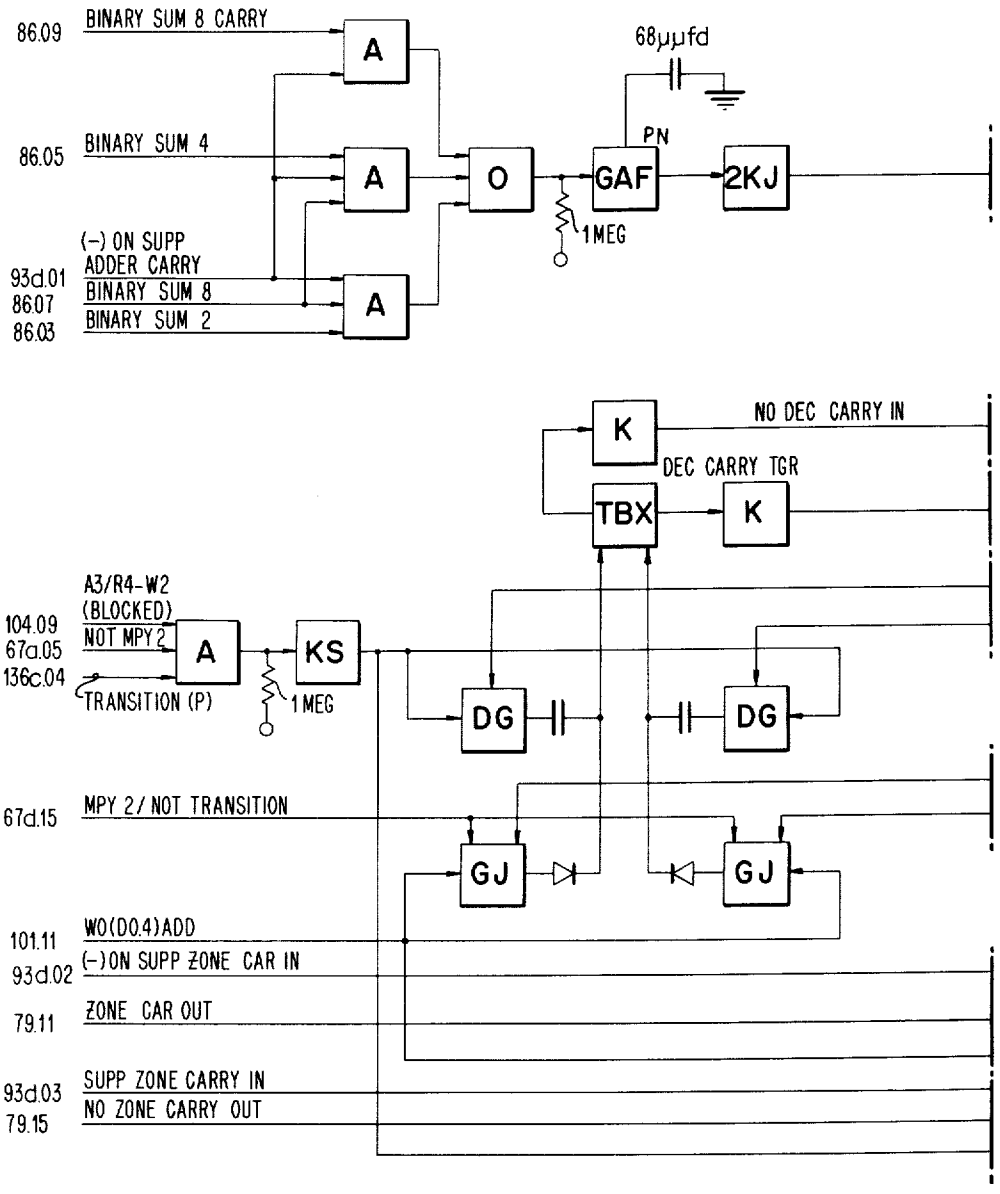

DECIMAL CORRECTION CIRCUITS DIGIT ADDER
RESULT 2(P)
87.01-90
RESULT 2
87.02-89a
87.03-63a
87.04-63c
RESULT 4(P)
87.05-90
RESULT 4
87.06-89a
87.07-63a
87.08-63c
RESULT 1
87.09-89a
87.10-63a
87.11-63c
RESULT 1(P)
87.12-90
RESULT 8(P)
87.13-90
RESULT 8
87.14-89a
87.15-63b
87.16-63c
DIGIT ADDER OUTPUT ≠ 0 (P)
87.17-140c
87.18-66i
87.19-125c
87.20-70a
87.21-74d
87.22-74g
87.23-67d
KO
K
GAF
1 MEG
N
O
A
I
4KJ
PN
SUM 2
SUM 4
SUM 8
DIGIT ADDER OUTPUT=0
BINARY SUM2
DEC CARRY OUT(P)
BINARY SUM 4
BINARY SUM 8 CARRY
NO DEC CARRY OUT (P)
BINARY SUM 8
DIGIT ADDER OUT (P)
SUM -1
86.02
88.02
86.04
86.08
88.07
86.06
93c.01
86.01

FIG. 87

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FIG. 88
SHEET 1 of 2

DEC CARRY CIRCUITS & ZONE CARRY TGR



INSTR RESET (X) 139b.21
-12 CLAMP 139d.20

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FIG. 88
SHEET 2 of 2

DEC CARRY CIRCUITS & ZONE CARRY TGR

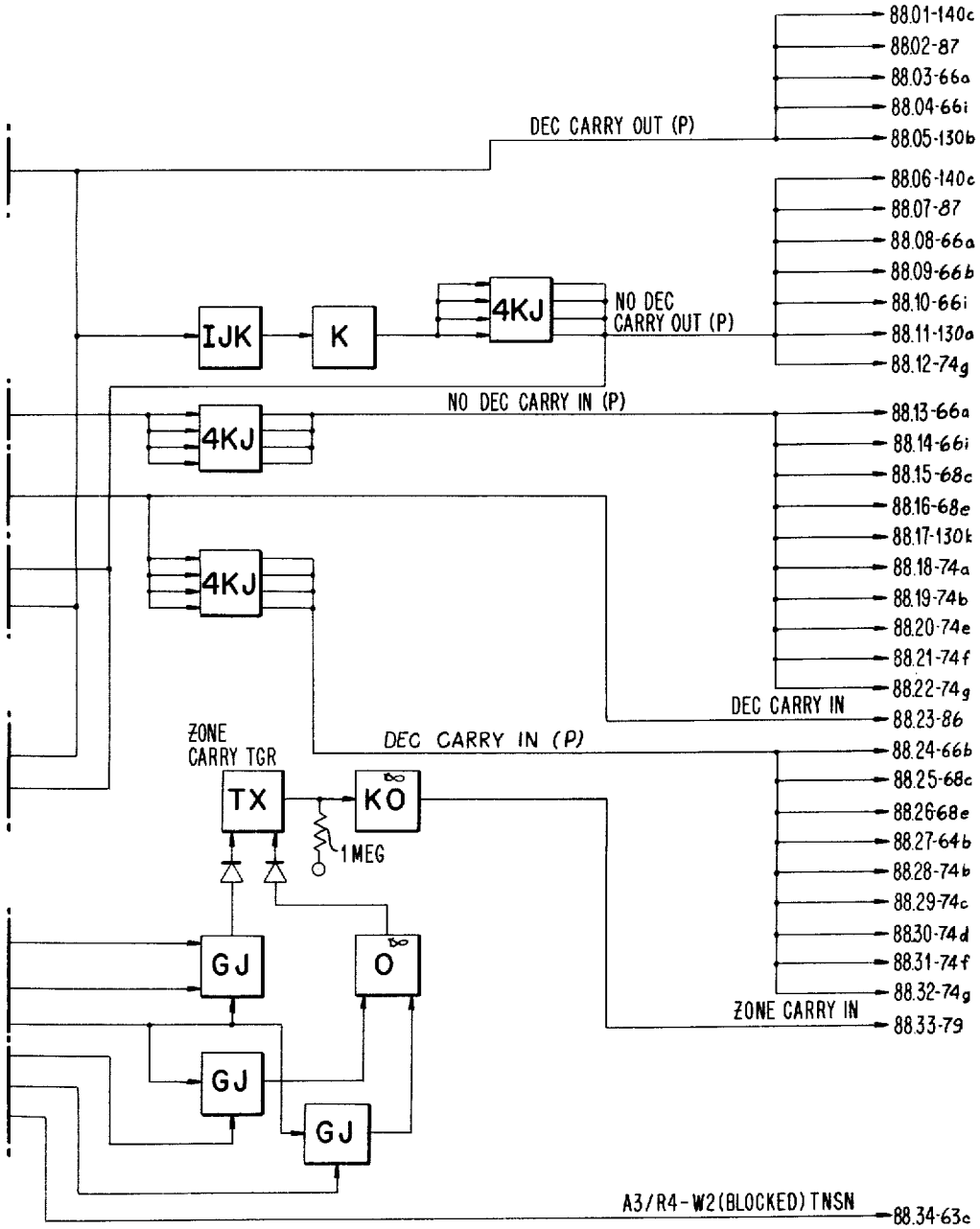


FIG. 89a

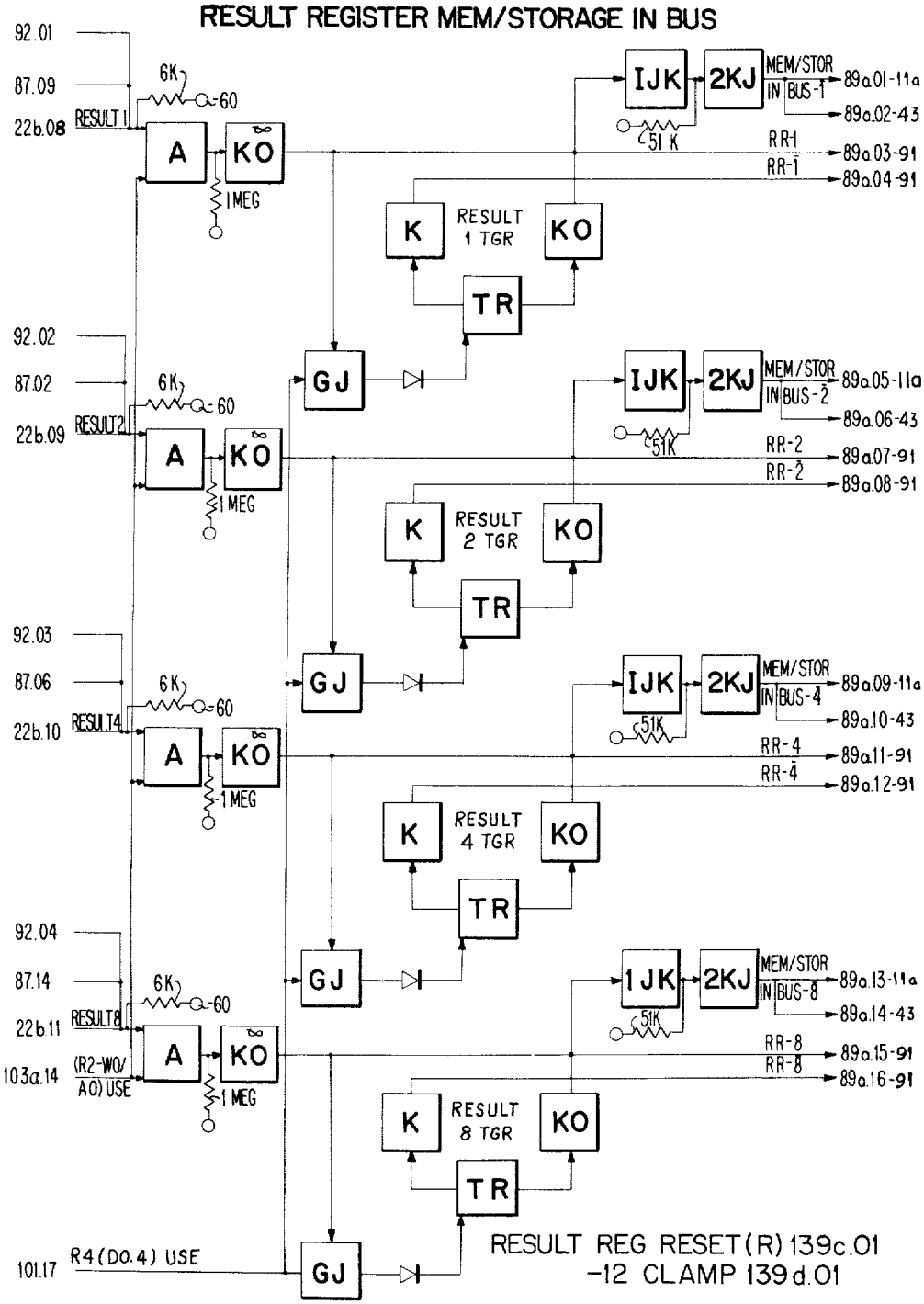
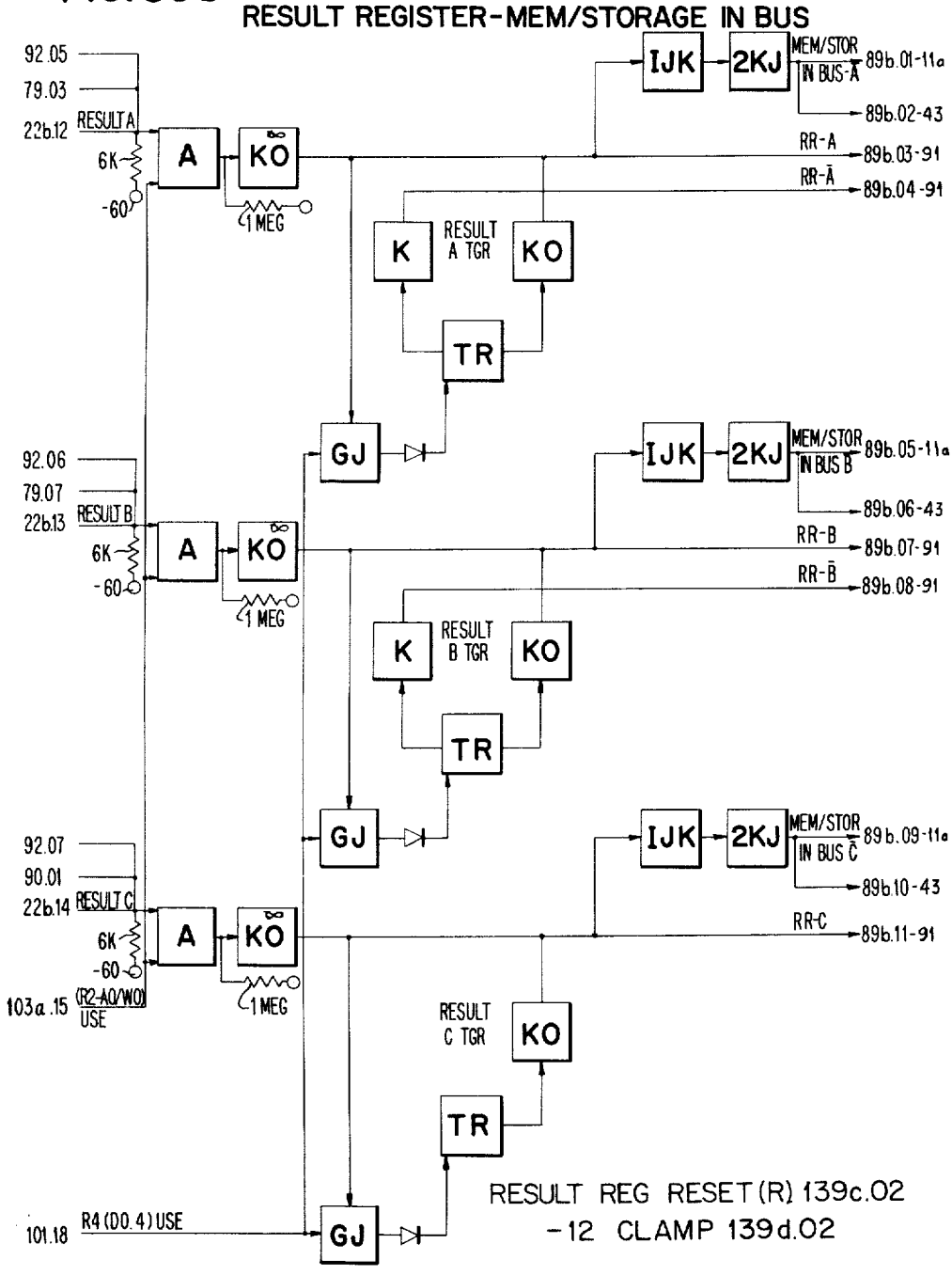

RESULT REGISTER MEM/STORAGE IN BUS
92.01
87.09
22b.08
RESULT 1
6K
60
A
KO
1 MEG
IJK
2KJ
51K
MEM/STOR IN BUS-1
89a.01-11a
89a.02-43
RR-1
RR-1
89a.03-91
89a.04-91
K
RESULT 1 TGR
KO
TR
92.02
87.02
22b.09
RESULT 2
GJ
MEM/STOR IN BUS-2
89a.05-11a
89a.06-43
RR-2
RR-2
89a.07-91
89a.08-91
RESULT 2 TGR
92.03
87.06
22b.10
RESULT 4
MEM/STOR IN BUS-4
89a.09-11a
89a.10-43
RR-4
RR-4
89a.11-91
89a.12-91
RESULT 4 TGR
92.04
87.14
22b.11
RESULT 8
1JK
MEM/STOR IN BUS-8
89a.13-11a
89a.14-43
RR-8
RR-8
89a.15-91
89a.16-91
RESULT 8 TGR
103a.14
(R2-WO/ AO) USE
101.17
R4 (D0.4) USE
RESULT REG RESET (R) 139c.01 -12 CLAMP 139d.01

FIG. 89b


RESULT REGISTER-MEM/STORAGE IN BUS
92.05
79.03
22b.12
RESULT A
6K
-60
A
KO
1 MEG
IJK
2KJ
MEM/STOR IN BUS Ā
89b.01-11a
89b.02-43
RR-A
89b.03-91
RR-Ā
89b.04-91
K
RESULT A TGR
KO
TR
GJ
92.06
79.07
22b.13
RESULT B
6K
-60
A
KO
1 MEG
IJK
2KJ
MEM/STOR IN BUS B
89b.05-11a
89b.06-43
RR-B
89b.07-91
RR-B̄
89b.08-91
K
RESULT B TGR
KO
TR
GJ
92.07
90.01
22b.14
RESULT C
6K
-60
103a.15
(R2-A0/W0) USE
A
KO
1 MEG
IJK
2KJ
MEM/STOR IN BUS C̄
89b.09-11a
89b.10-43
RR-C
89b.11-91
RESULT C TGR
KO
TR
GJ
101.18
R4 (D0.4) USE
RESULT REG RESET (R) 139c.02
-12 CLAMP 139d.02

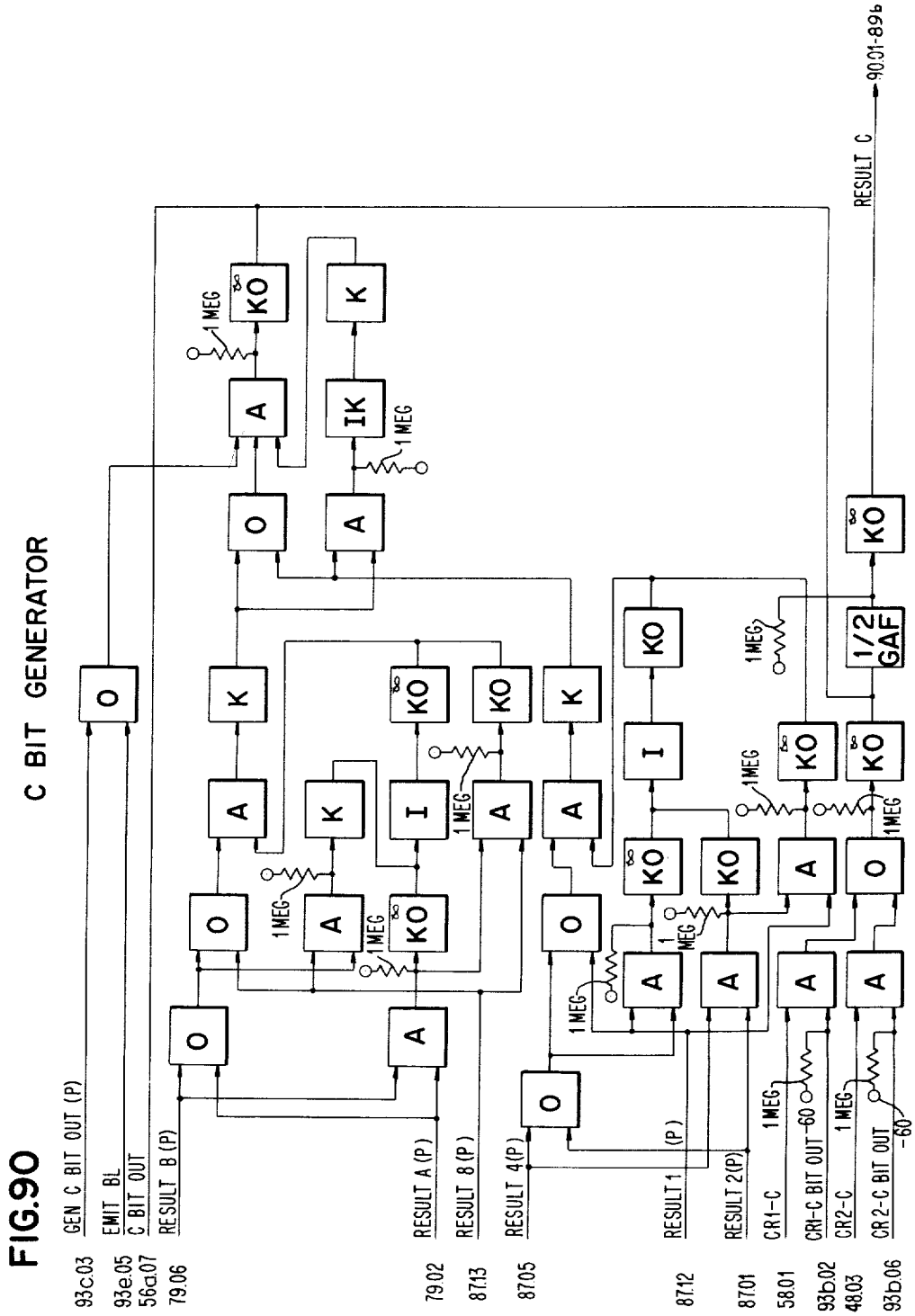
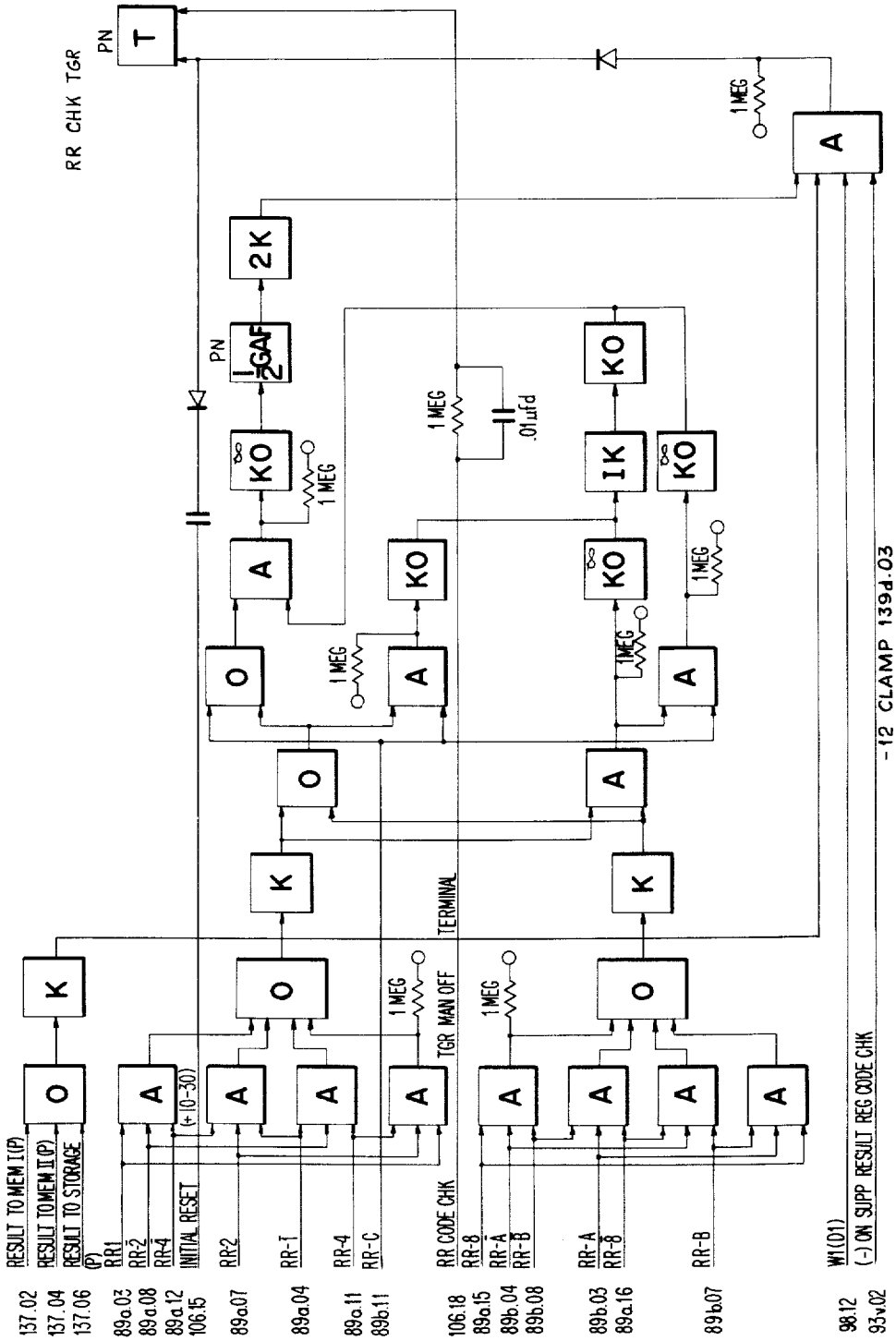

C BIT GENERATOR
GEN C BIT OUT (P)
EMIT BL
C BIT OUT
RESULT B (P)
RESULT A (P)
RESULT 8 (P)
RESULT 4(P)
RESULT 1 (P)
RESULT 2(P)
CR1-C
CR-C BIT OUT -60
CR2-C
CR 2-C BIT OUT -60
RESULT C
1 MEG
93c.03
93e.05
56a.07
79.06
79.02
87.13
87.05
87.12
87.01
58.01
93b.02
48.03
93b.06
90.01-89b

FIG.90

FIG. 91 RESULT REGISTER CODE CHECK - ERROR TRIGGER



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FIG.92

MEMORY TEST-CHARACTER SELECTOR

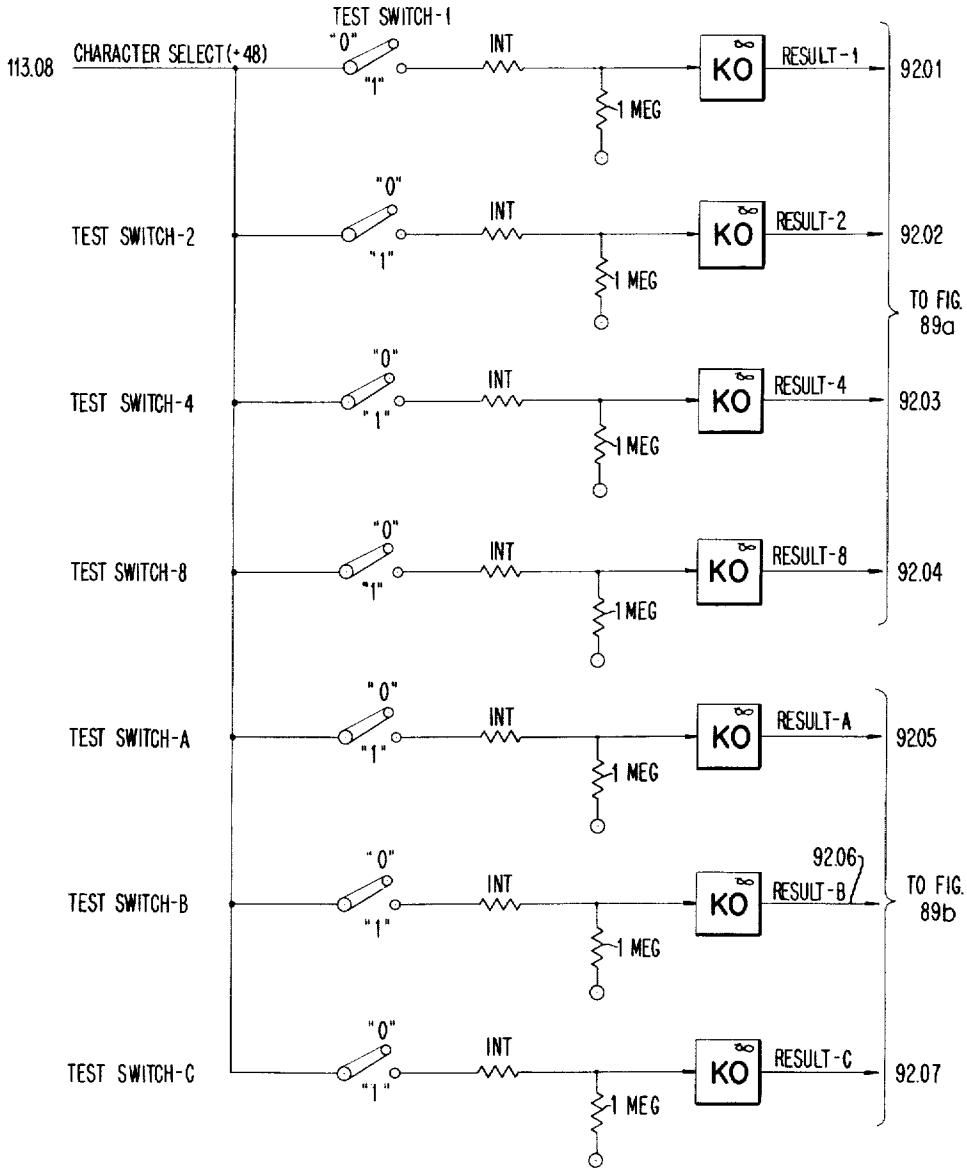


FIG.93a

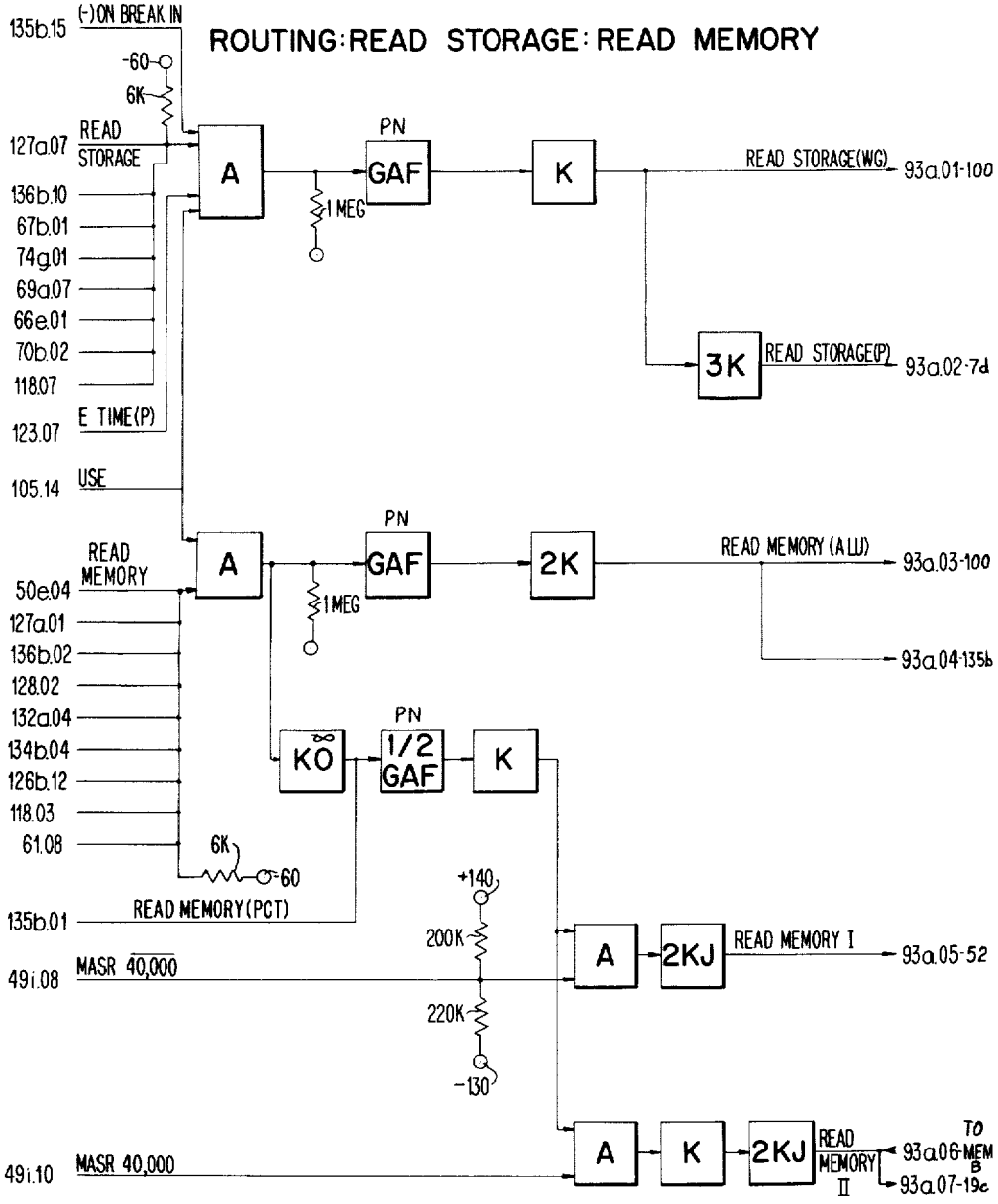

ROUTING:READ STORAGE:READ MEMORY
135b.15 (-)ON BREAK IN
-60
6K
127a.07 READ STORAGE
136b.10
67b.01
74g.01
69a.07
66e.01
70b.02
118.07
123.07 E TIME(P)
105.14 USE
50e.04 READ MEMORY
127a.01
136b.02
128.02
132a.04
134b.04
126b.12
118.03
61.08
135b.01 READ MEMORY(PCT)
49i.08 MASR 40,000
49i.10 MASR 40,000
A
PN
GAF
1 MEG
K
READ STORAGE(WG)
93a.01-100
3K
READ STORAGE(P)
93a.02-7d
2K
READ MEMORY (ALU)
93a.03-100
93a.04-135b
KO
1/2 GAF
+140
200K
220K
-130
2KJ
READ MEMORY I
93a.05-52
READ MEMORY II
TO MEM B
93a.06-19c
93a.07-19c

FIG. 93b

CHARACTER REGISTERS TO ADDER ROUTING

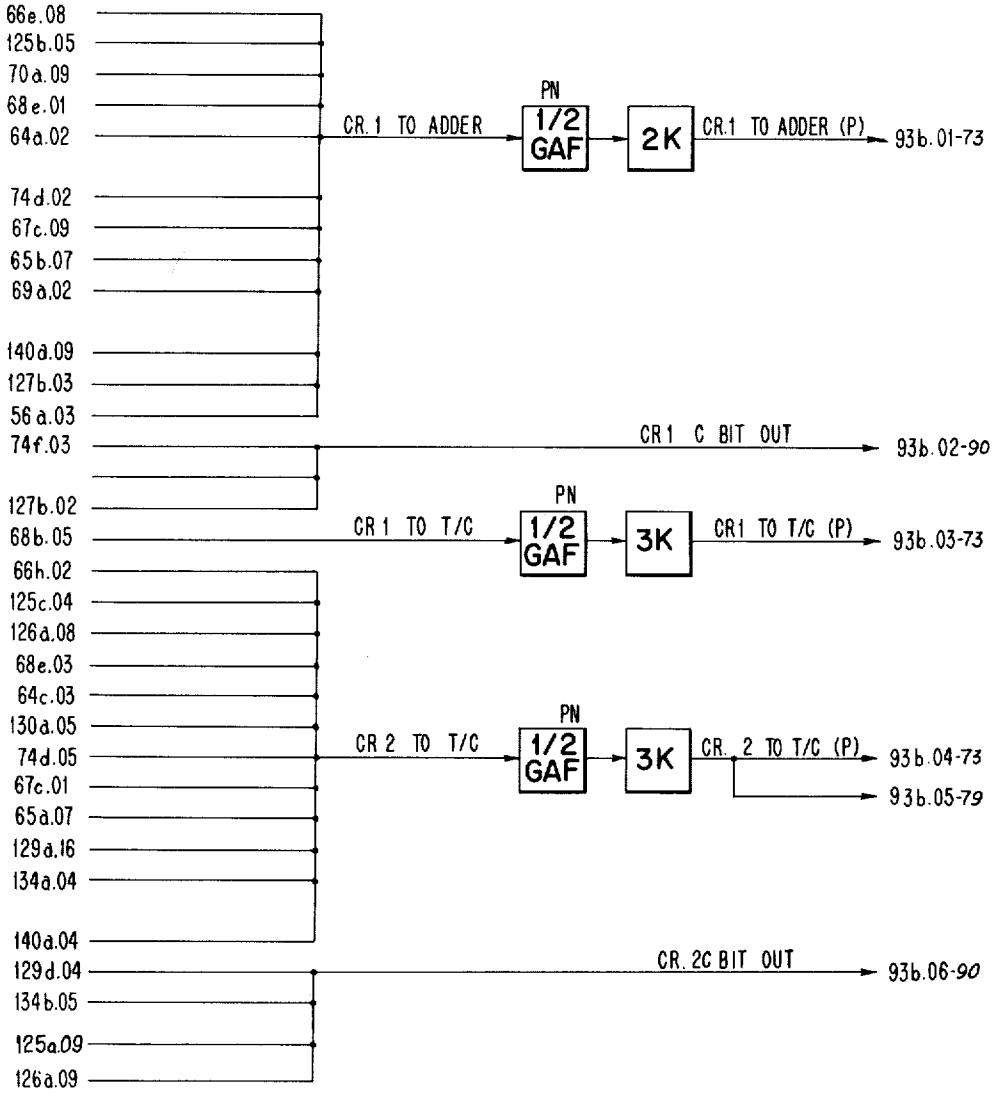


FIG. 93c
ADDER OUT ROUTING

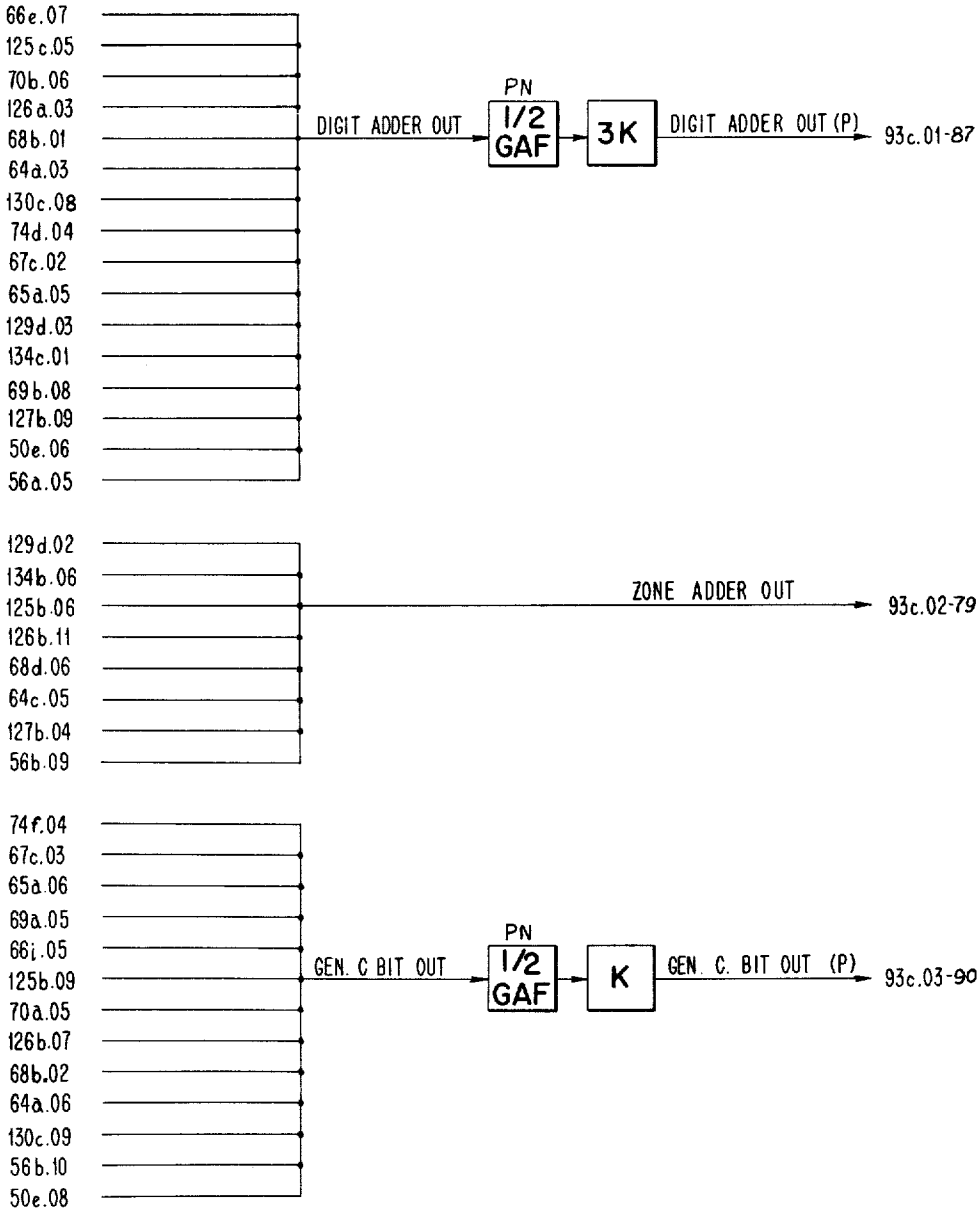


FIG. 93d
ADDER CARRY ROUTING

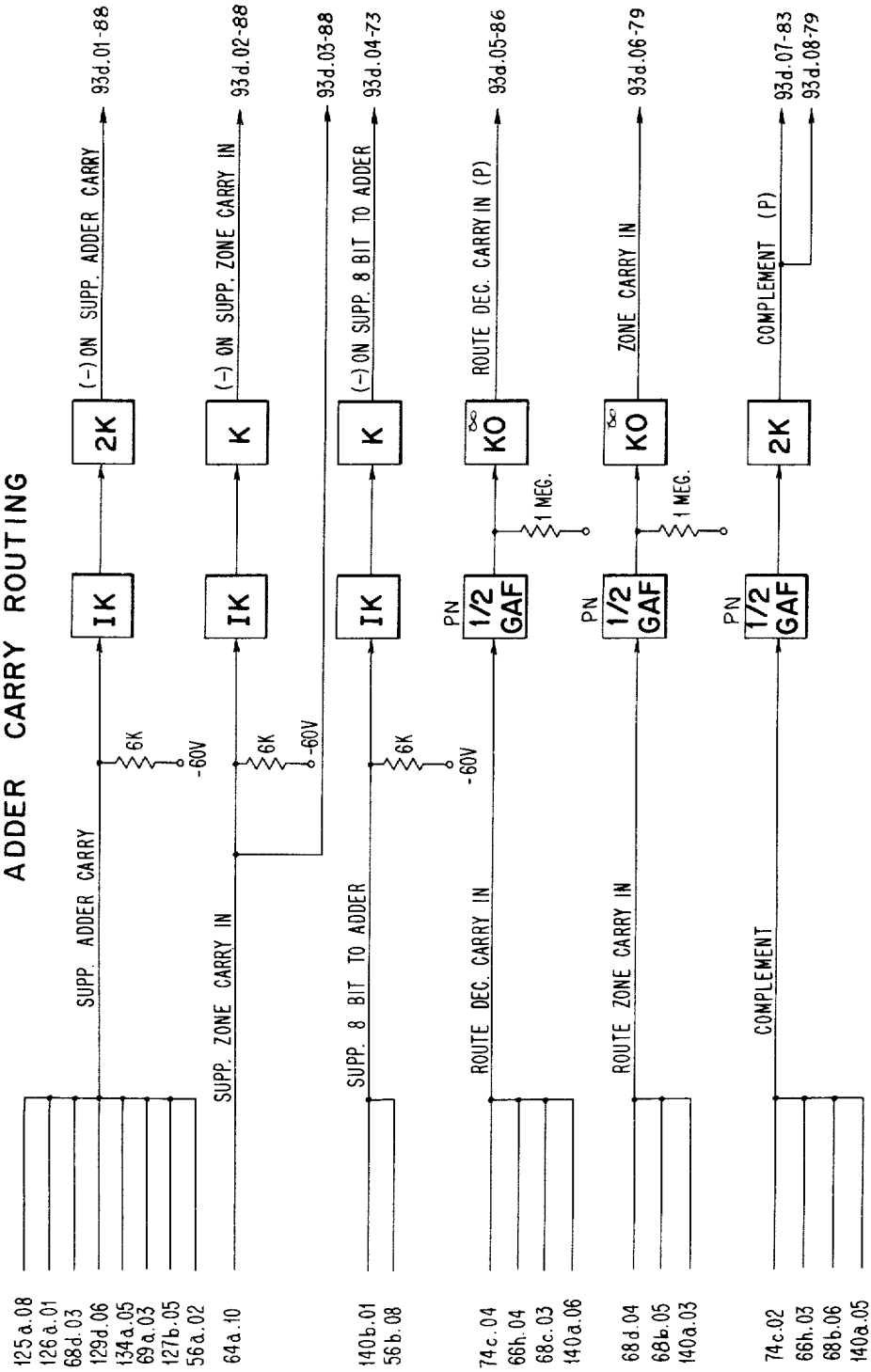


FIG. 93e
ADDER EMITTER AND MPL REG. ROUTING

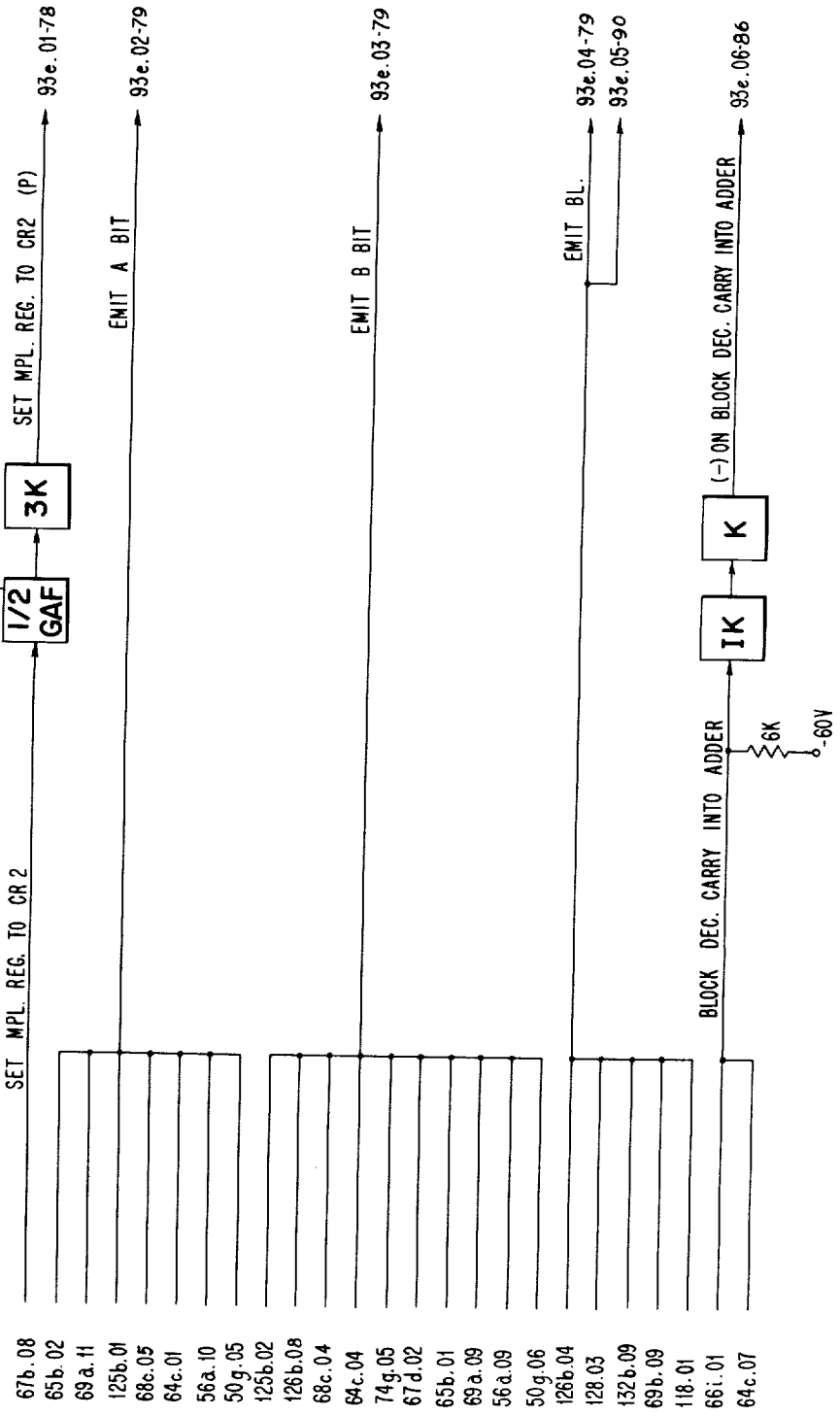


FIG. 93f

BIT TO ADDER ROUTING

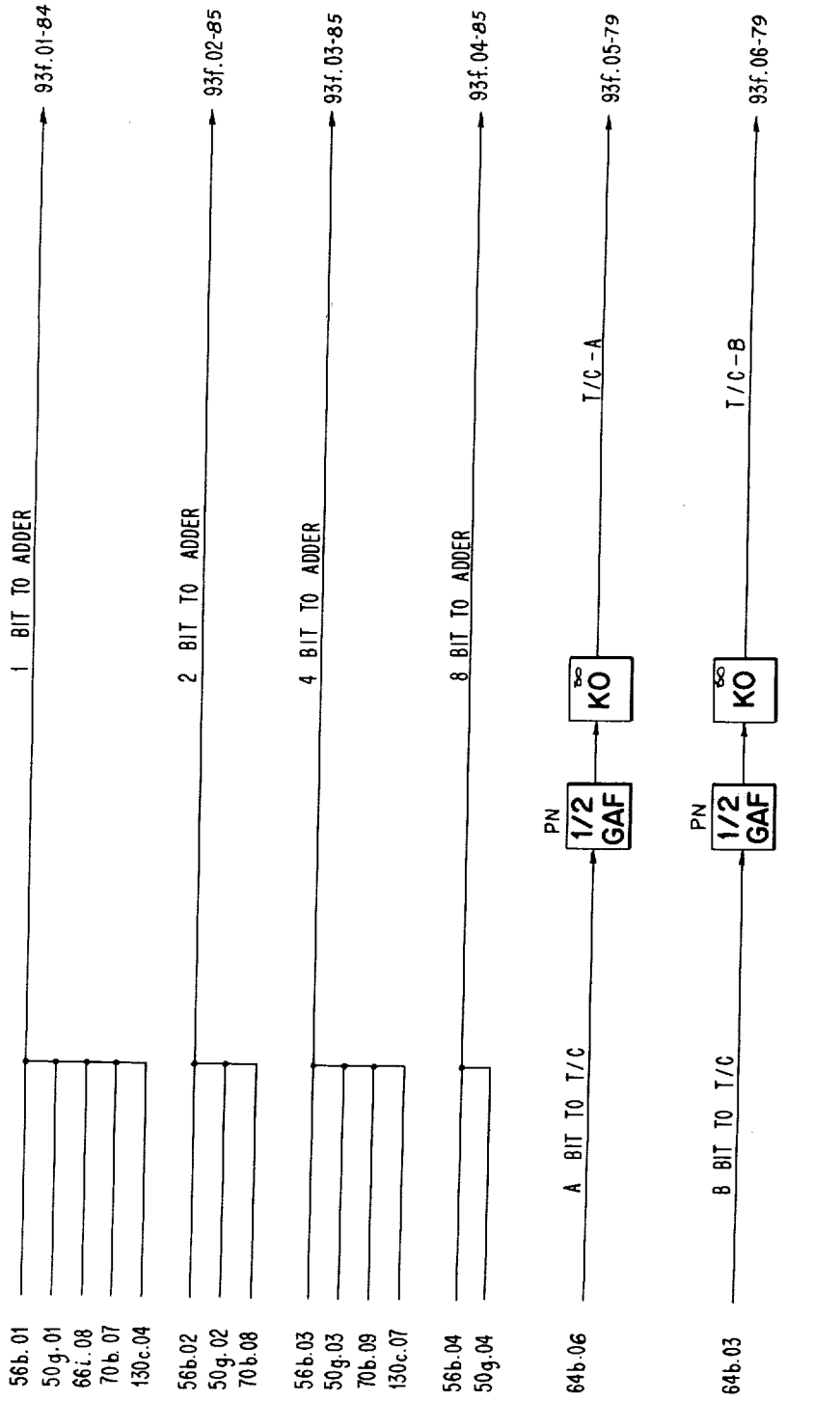


FIG. 93g

STEP MAC. 1 ± 1 ROUTING

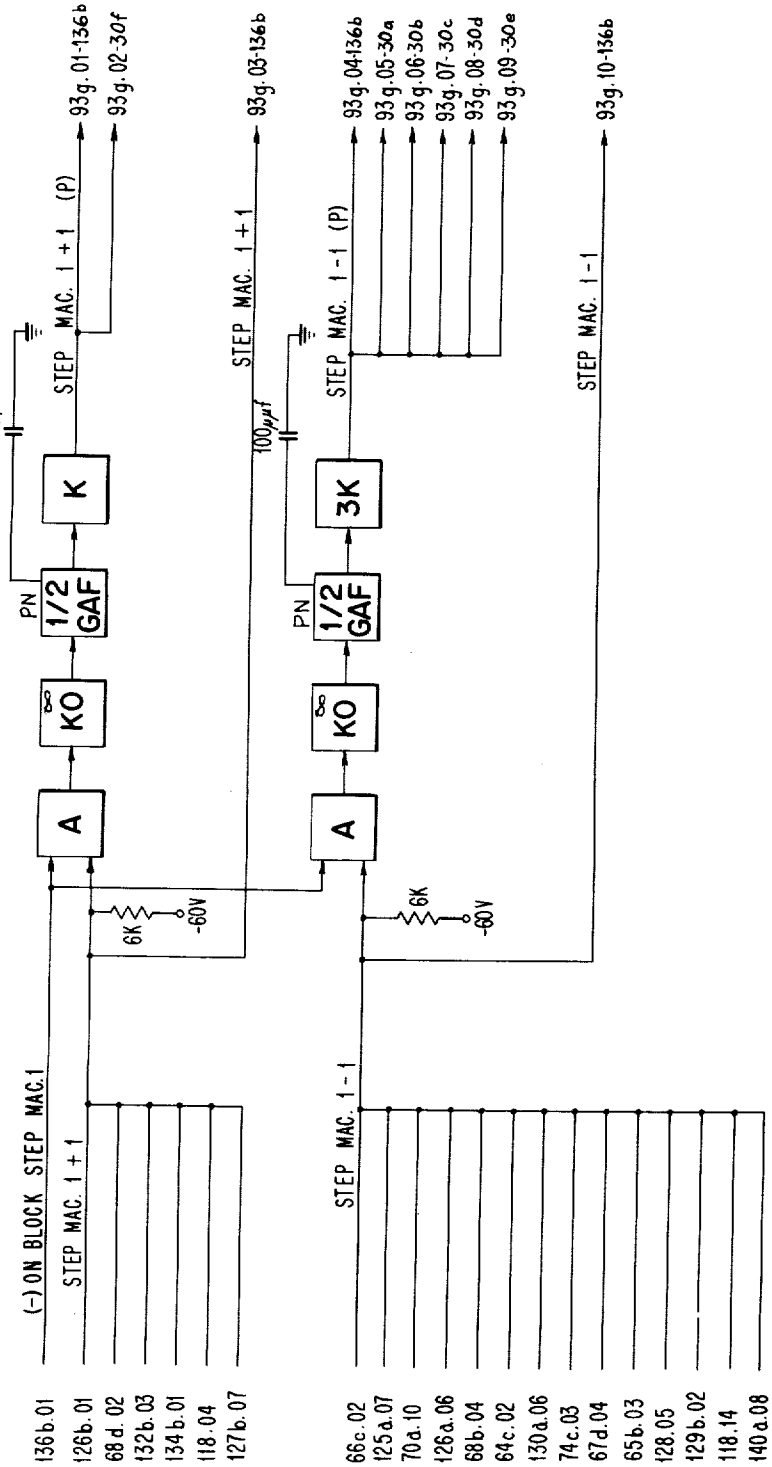


FIG. 93h

STEP MAC. 2+1, STEP MAC. 1+5, STEP MAC. 2+5

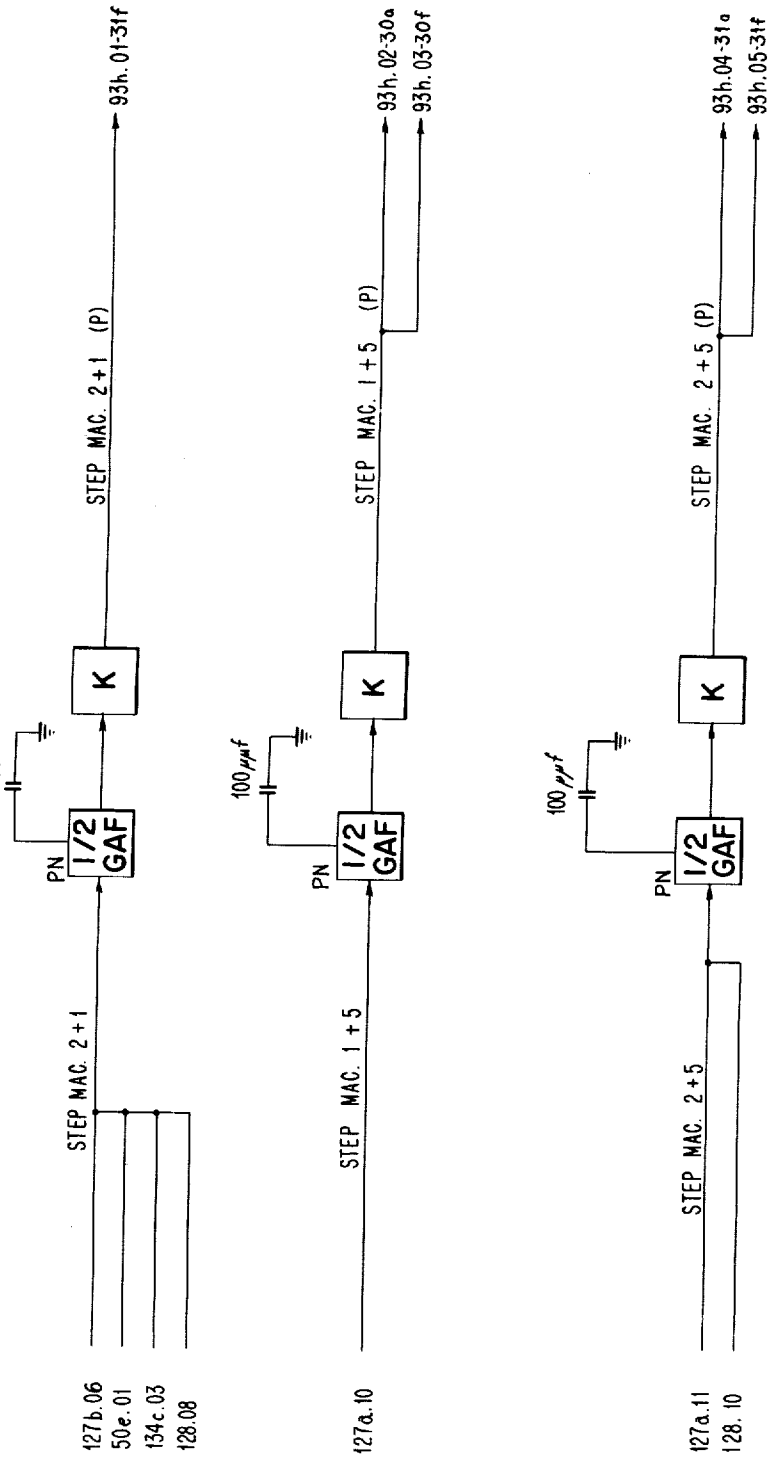


FIG. 93i
STEP SAC ROUTING

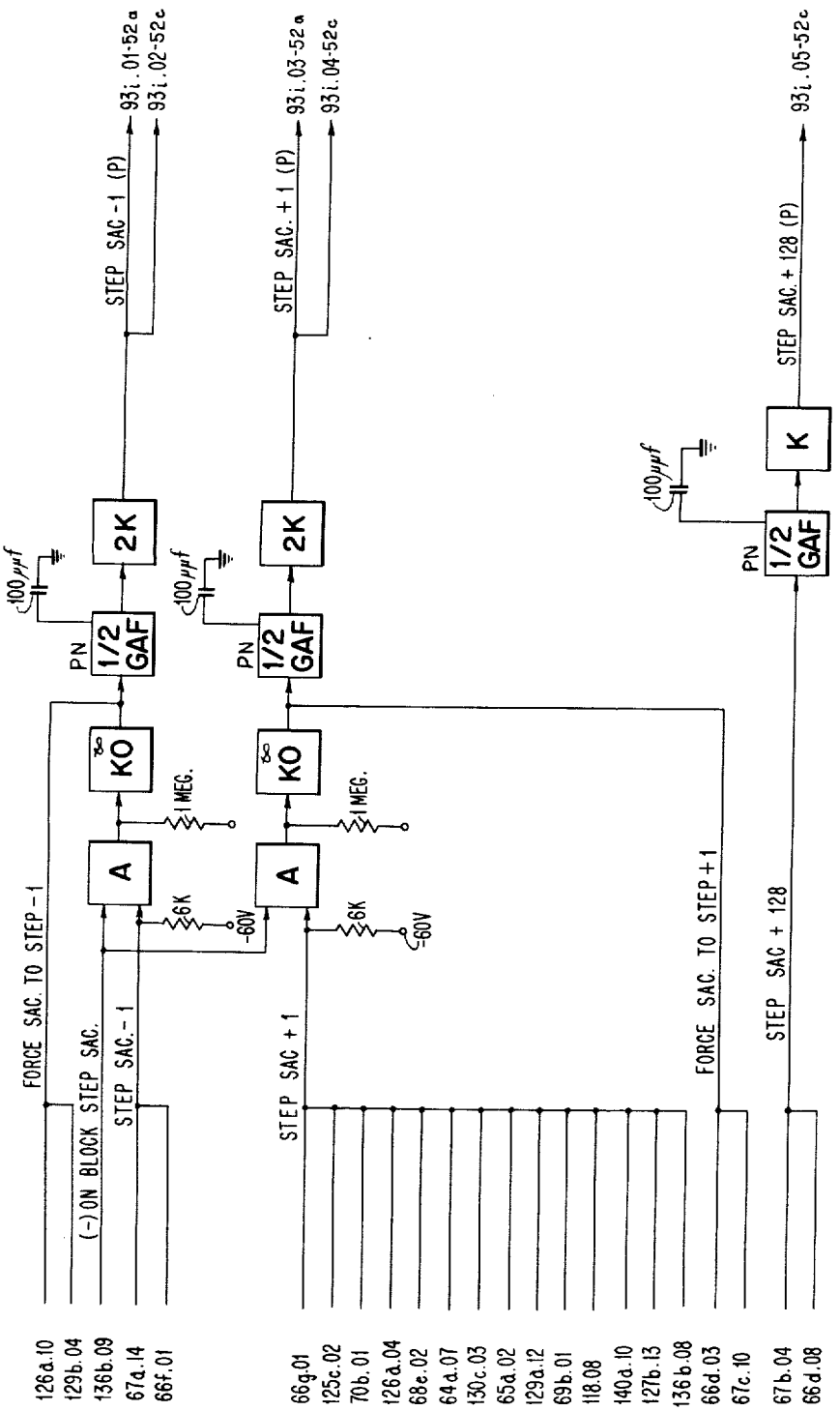


FIG. 93j
STORAGE, MEMORY AND INSTRUCTION COUNTER ROUTING

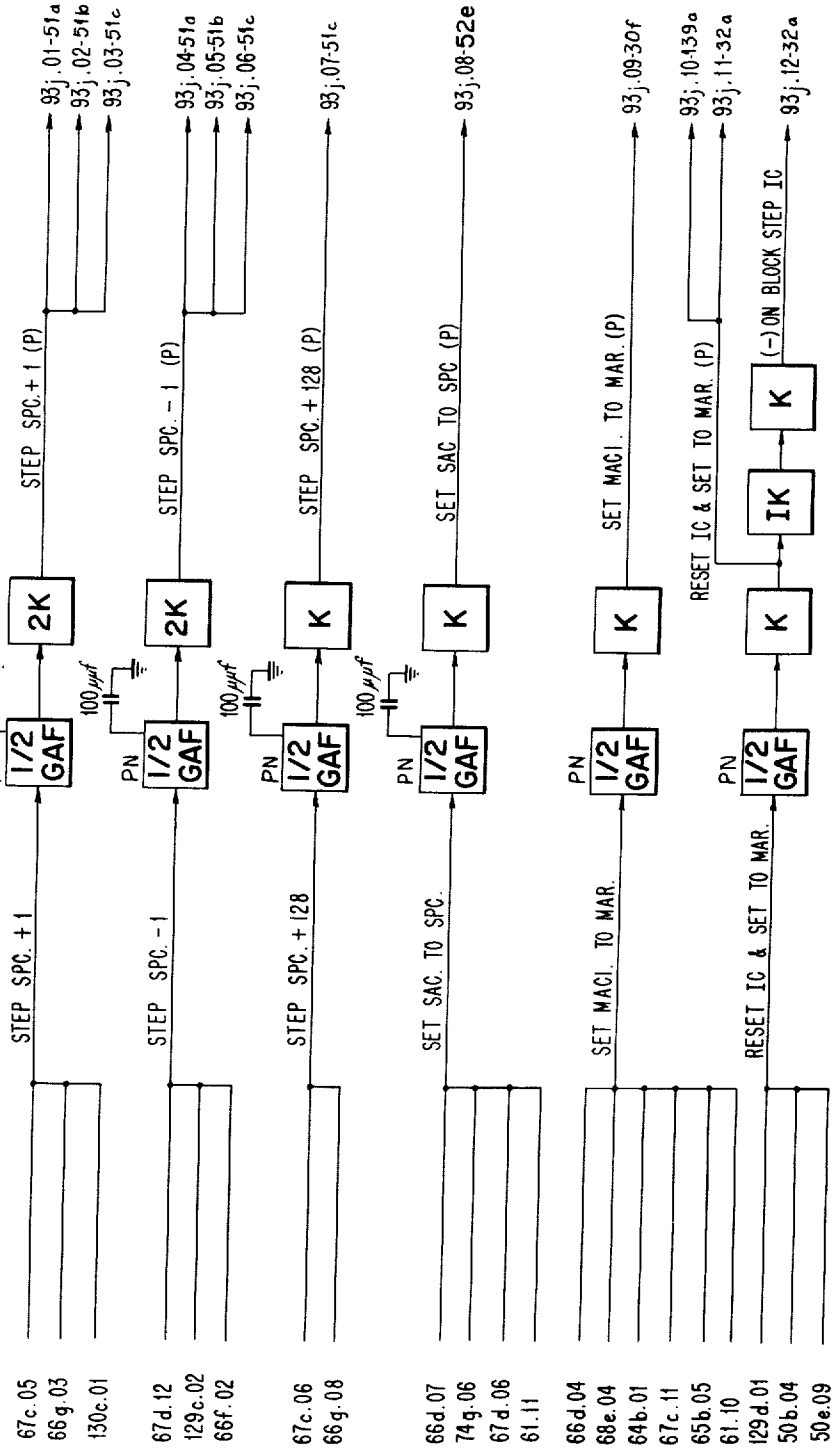


FIG. 93k

AUXILIARY TRIG.'S ROUTING

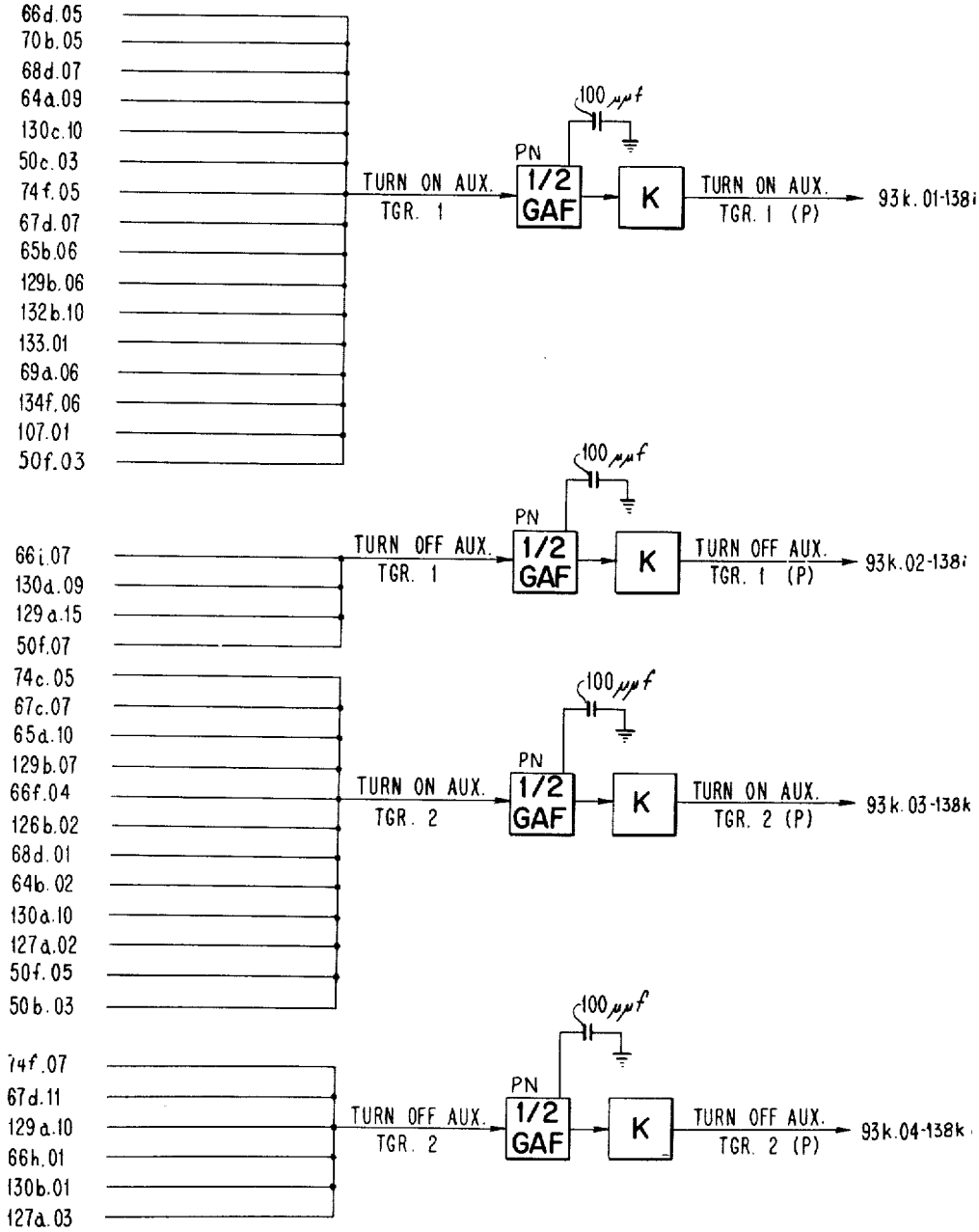


FIG. 931

AUX. TRIG. STOR. HI. TRIG., AND RMDR. TRIG. ROUTING

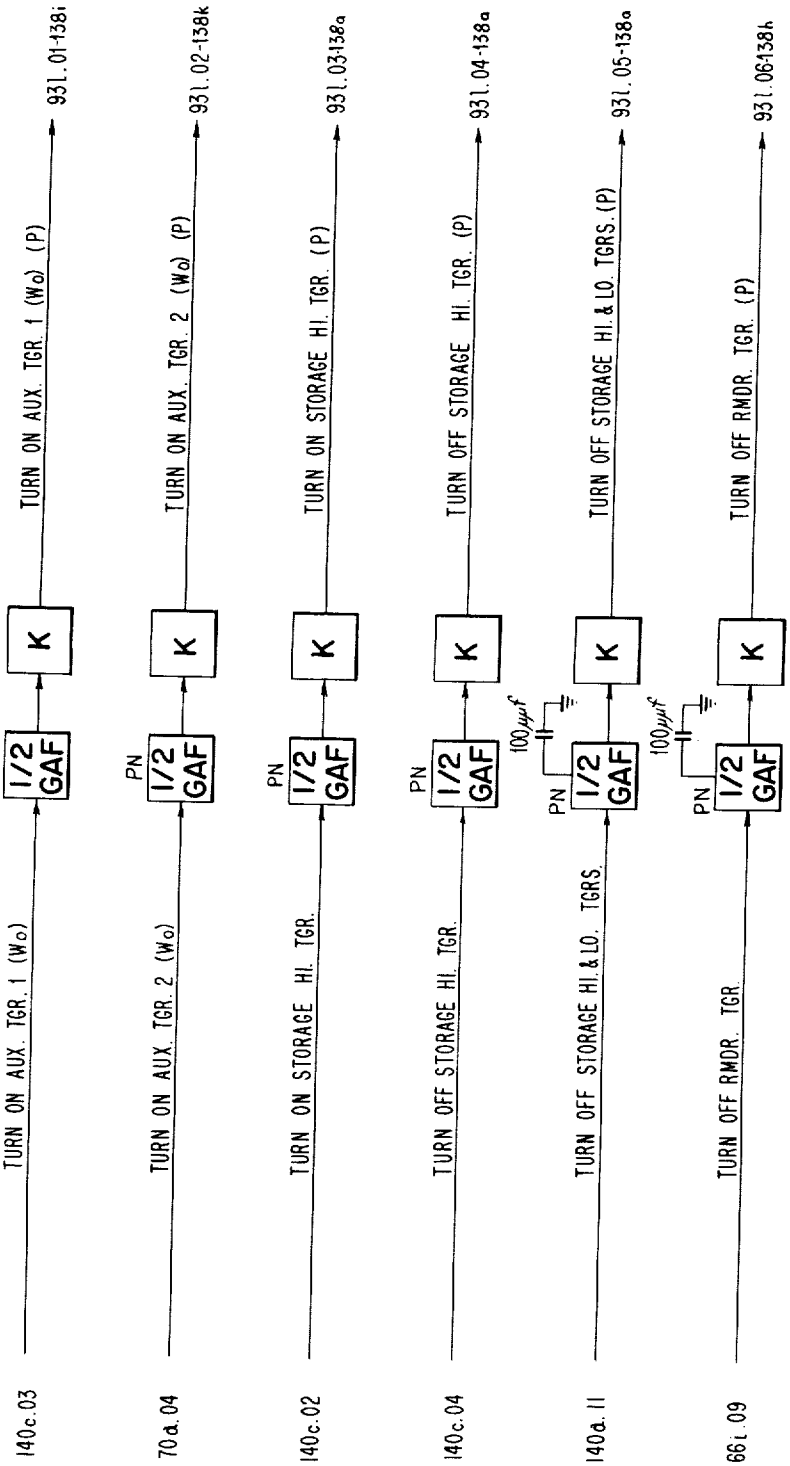
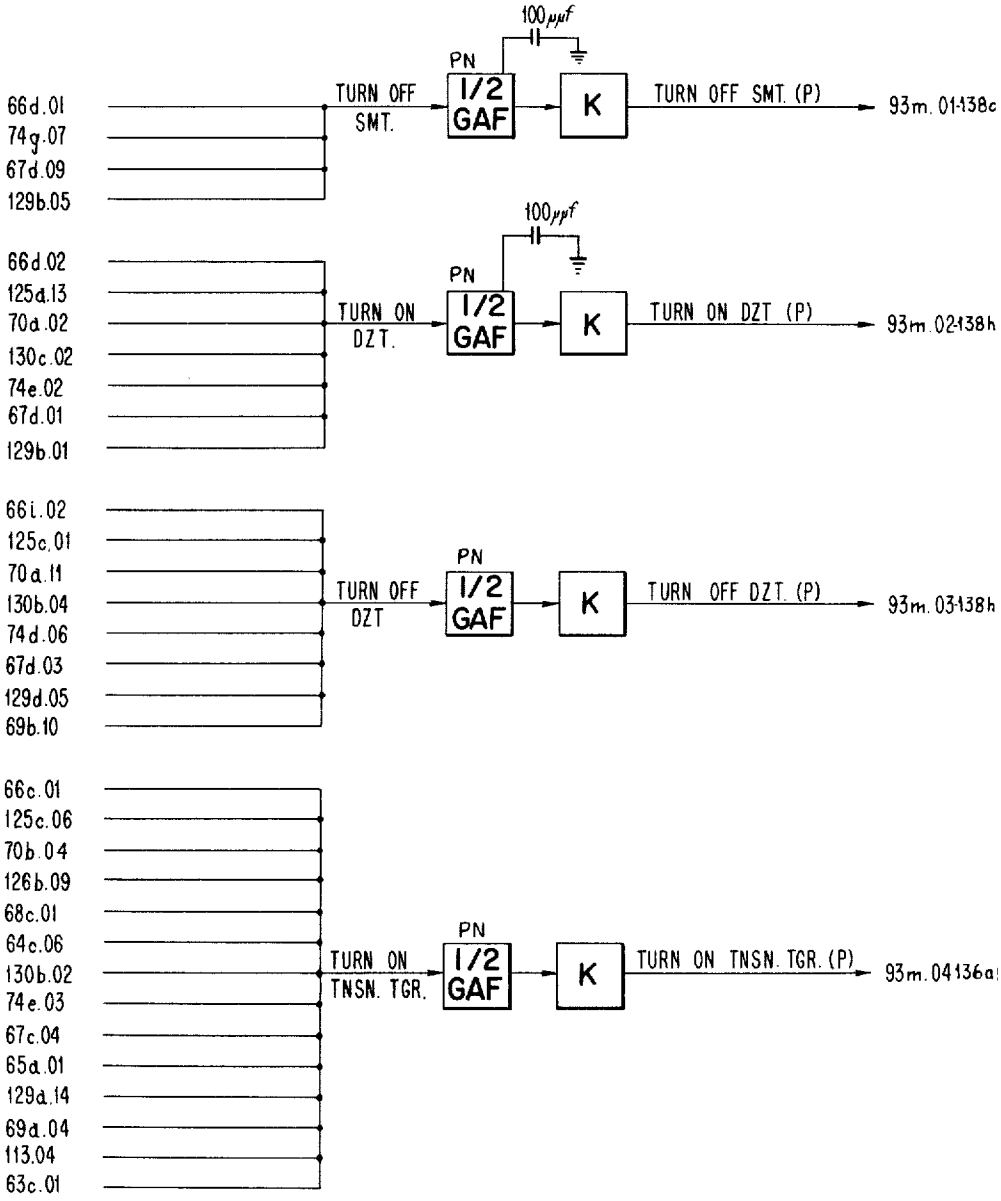


FIG. 93m

SMT. DZT. AND TNSN TRIG. ROUTING



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FIG.93n SIGN CHK TGR OVFL CHK TRIG AND STOR SIGN TRIG ROUTING

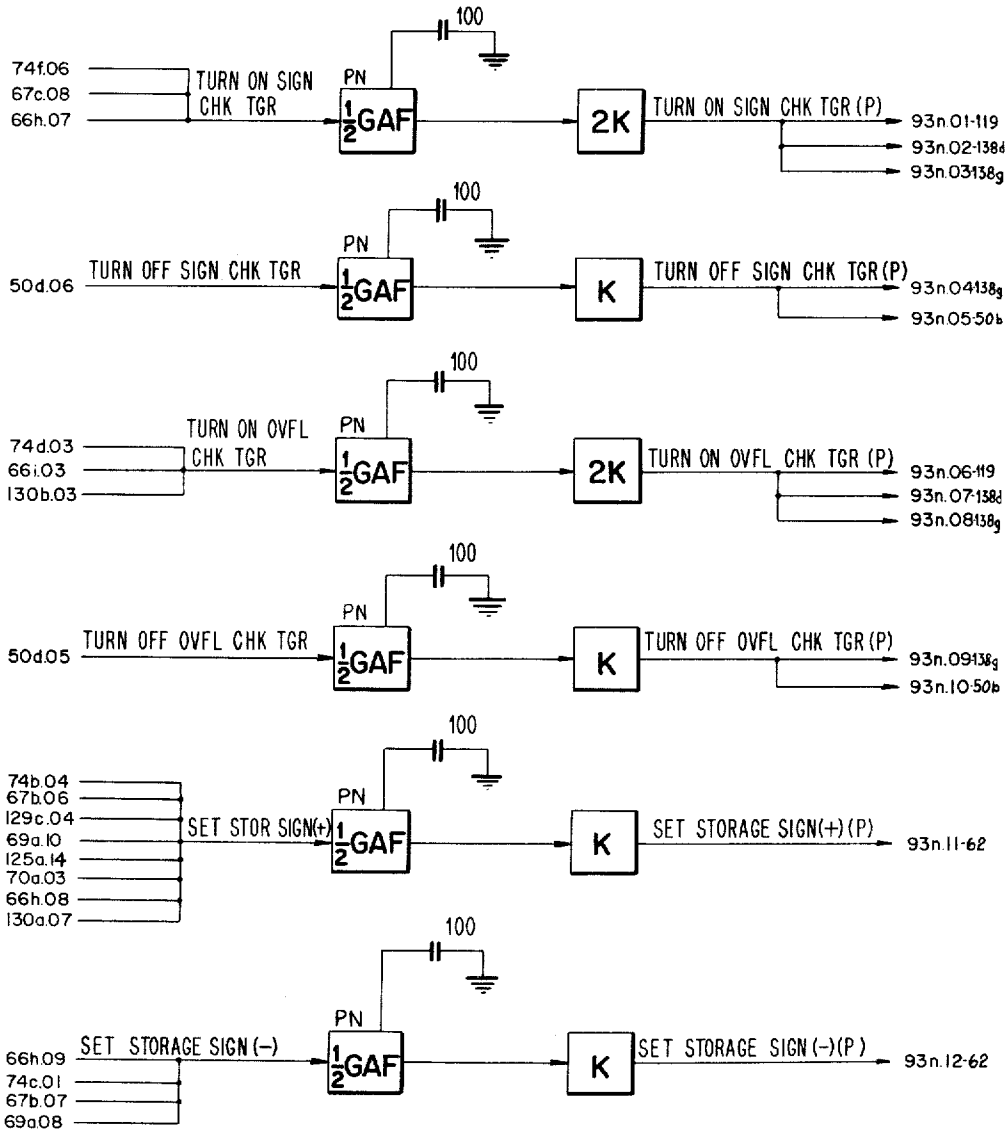


FIG.93o

R/W CHK TGR, RECORD CHK TGR AND INSTR CHK TGR ROUTING

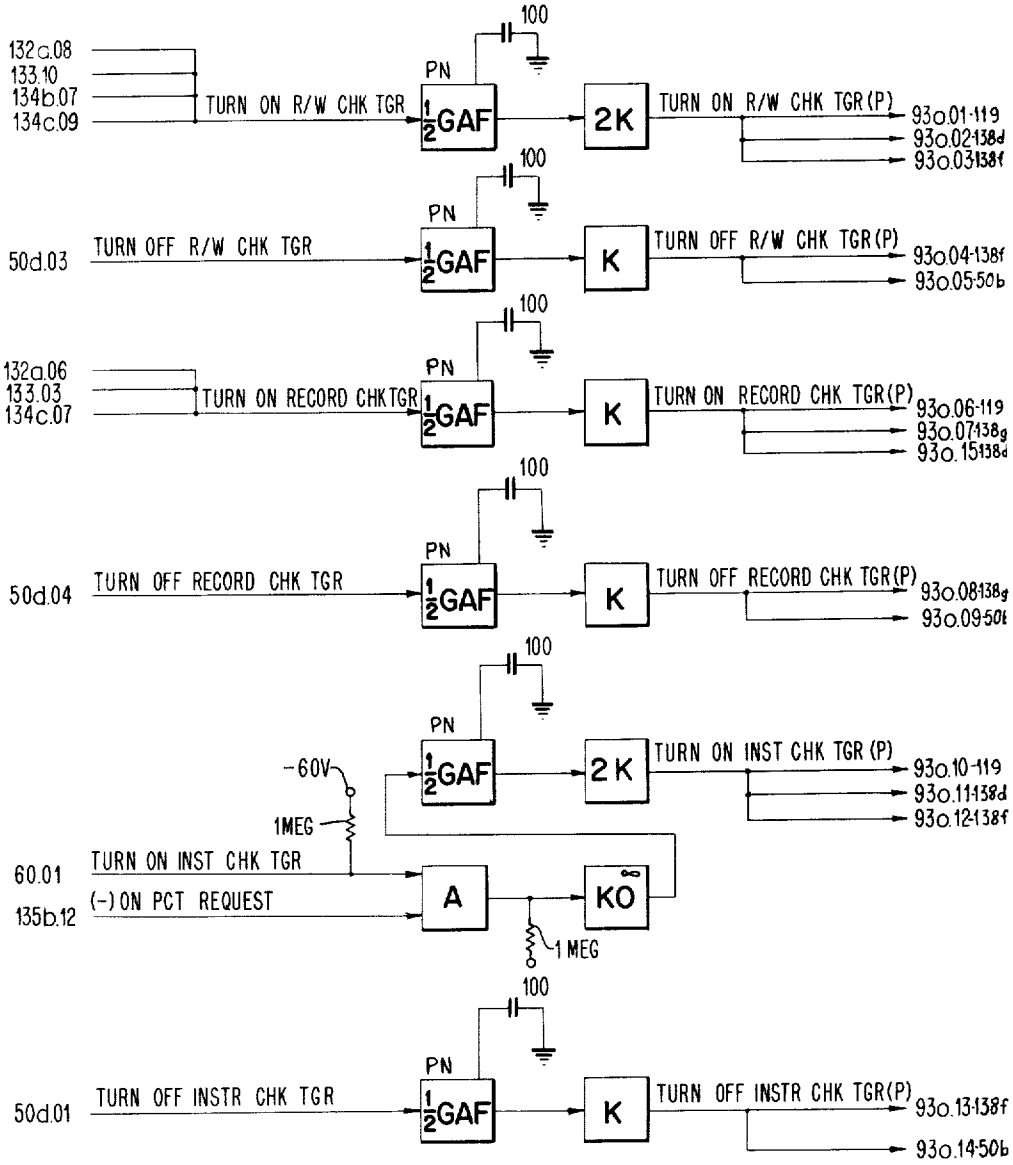


FIG.93p

MEMORY CONTROL ROUTING

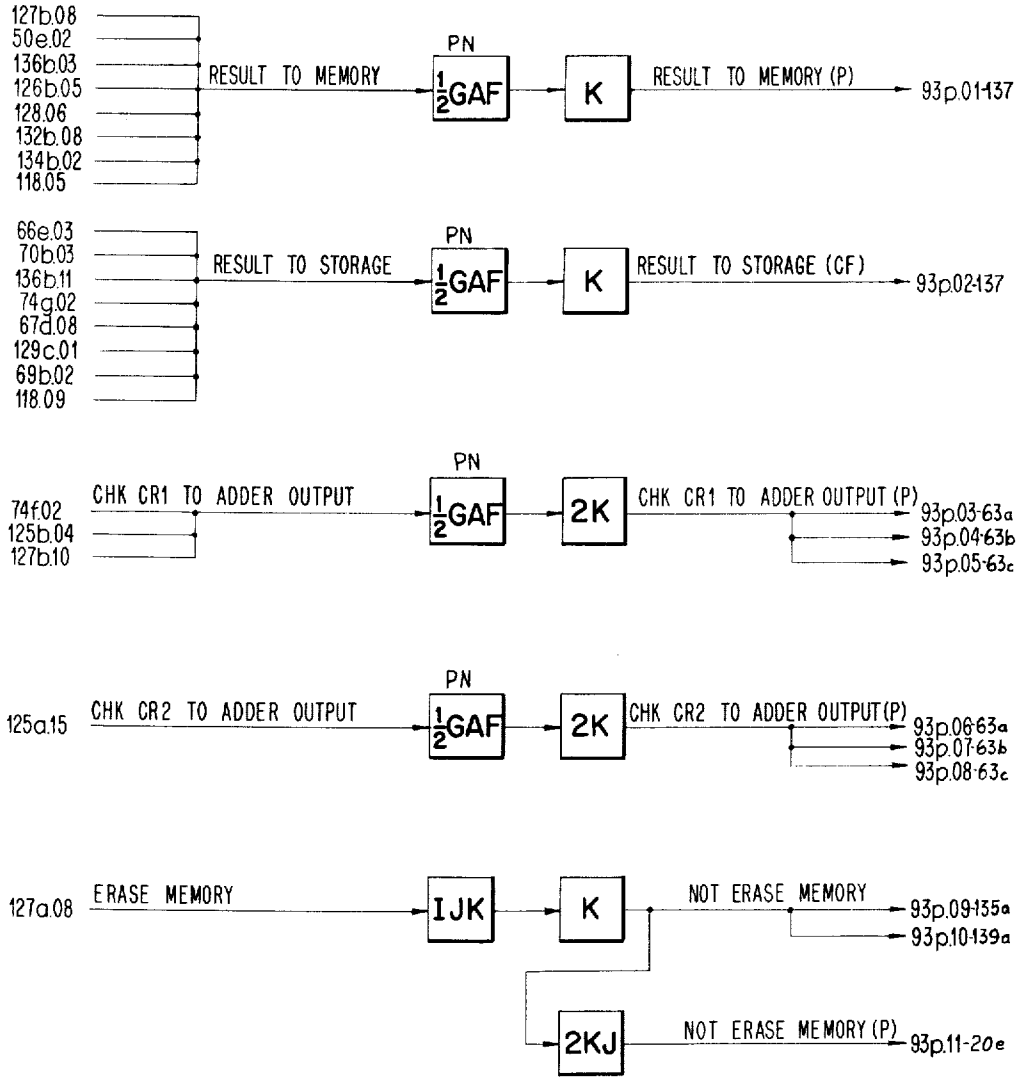


FIG.93q

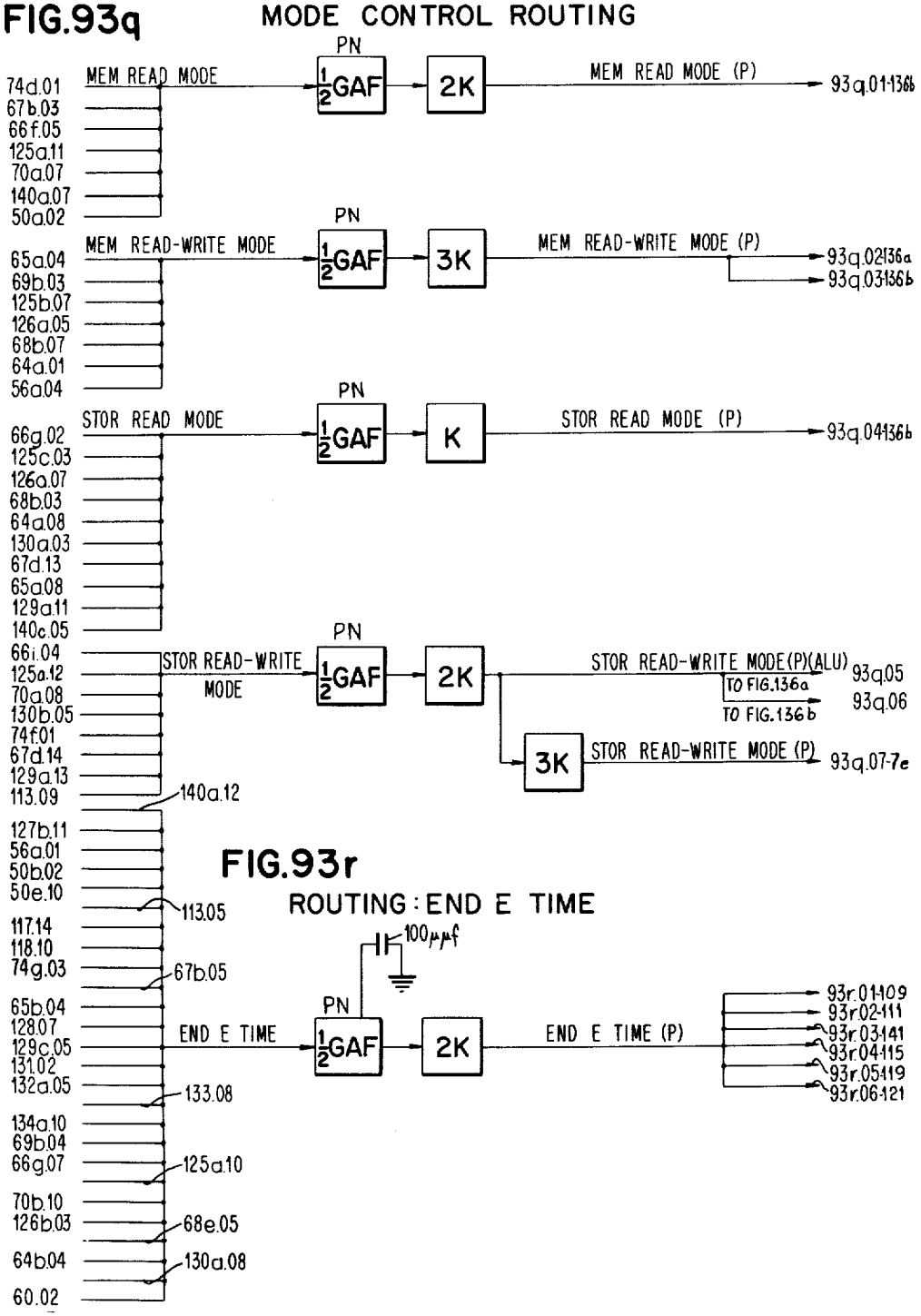


FIG.93r

FIG. 93s

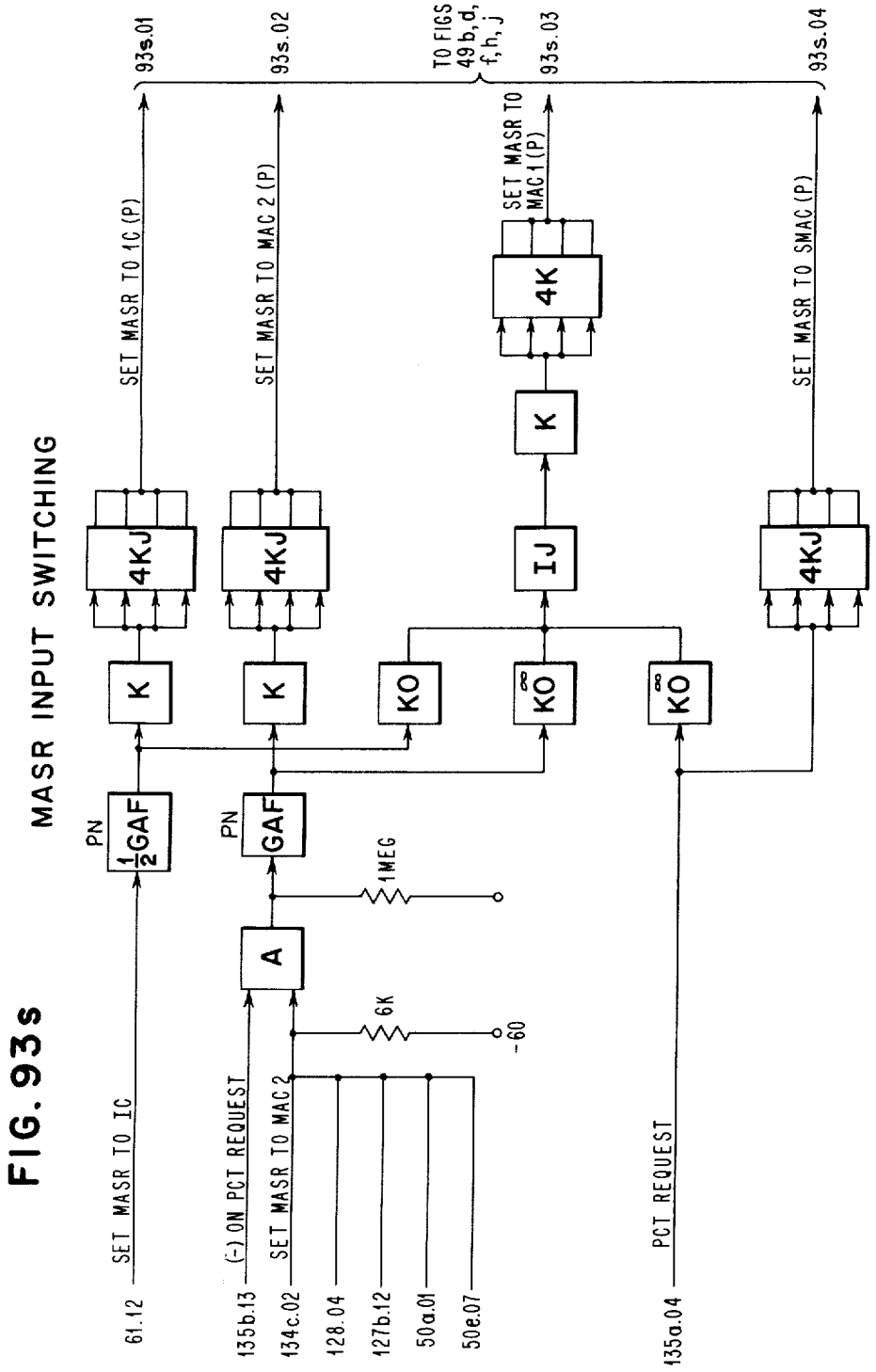

MASR INPUT SWITCHING
93s.01
93s.02
TO FIGS 49b,d, f,h,j
93s.03
93s.04
SET MASR TO 1C (P)
SET MASR TO MAC 2 (P)
SET MASR TO MAC 1 (P)
SET MASR TO SMAC (P)
4KJ
4KJ
4K
K
IJ
4KJ
K
K
KO
KO
KO
PN ½GAF
PN GAF
1MEG
A
6K
-60
SET MASR TO IC
(-) ON PCT REQUEST
SET MASR TO MAC 2
PCT REQUEST
61.12
135b.13
134c.02
128.04
127b.12
50a.01
50e.07
135a.04

FIG. 93t

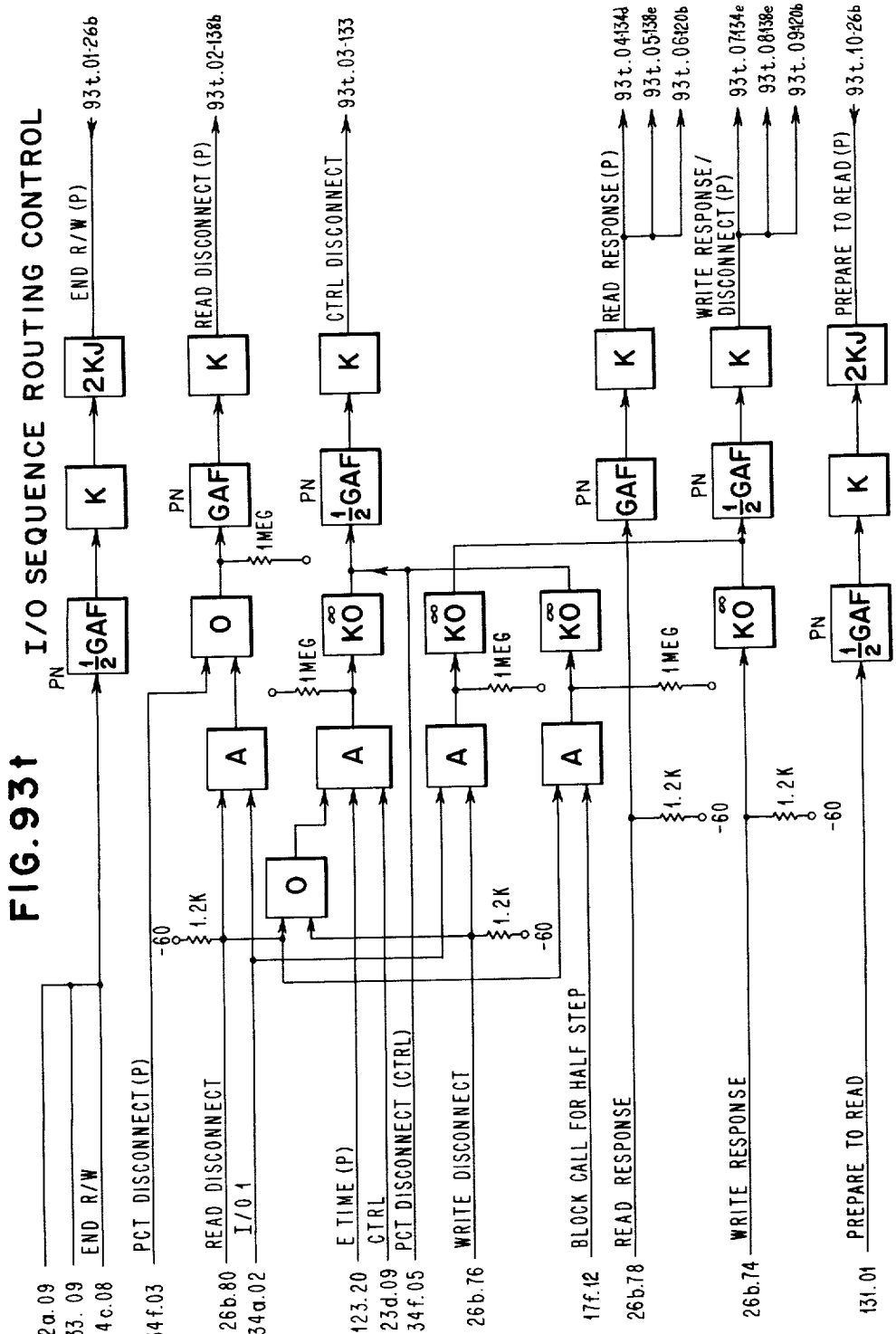

I/O SEQUENCE ROUTING CONTROL
132a.09
133.09
134c.08
134f.03
26b.80
134a.02
123.20
23d.09
134f.05
26b.76
17f.12
26b.78
26b.74
131.01
END R/W
PCT DISCONNECT(P)
READ DISCONNECT
I/O 1
E TIME (P)
CTRL
PCT DISCONNECT (CTRL)
WRITE DISCONNECT
BLOCK CALL FOR HALF STEP
READ RESPONSE
WRITE RESPONSE
PREPARE TO READ
PN
½GAF
K
2KJ
93t.01-26b
END R/W (P)
O
A
1MEG
1.2K
-60
GAF
READ DISCONNECT (P)
93t.02-138b
KO
CTRL DISCONNECT
93t.03-133
READ RESPONSE (P)
93t.04134d
93t.05138e
93t.06120b
WRITE RESPONSE / DISCONNECT (P)
93t.07134e
93t.08138e
93t.09120b
PREPARE TO READ (P)
93t.10-26b

FIG. 93u

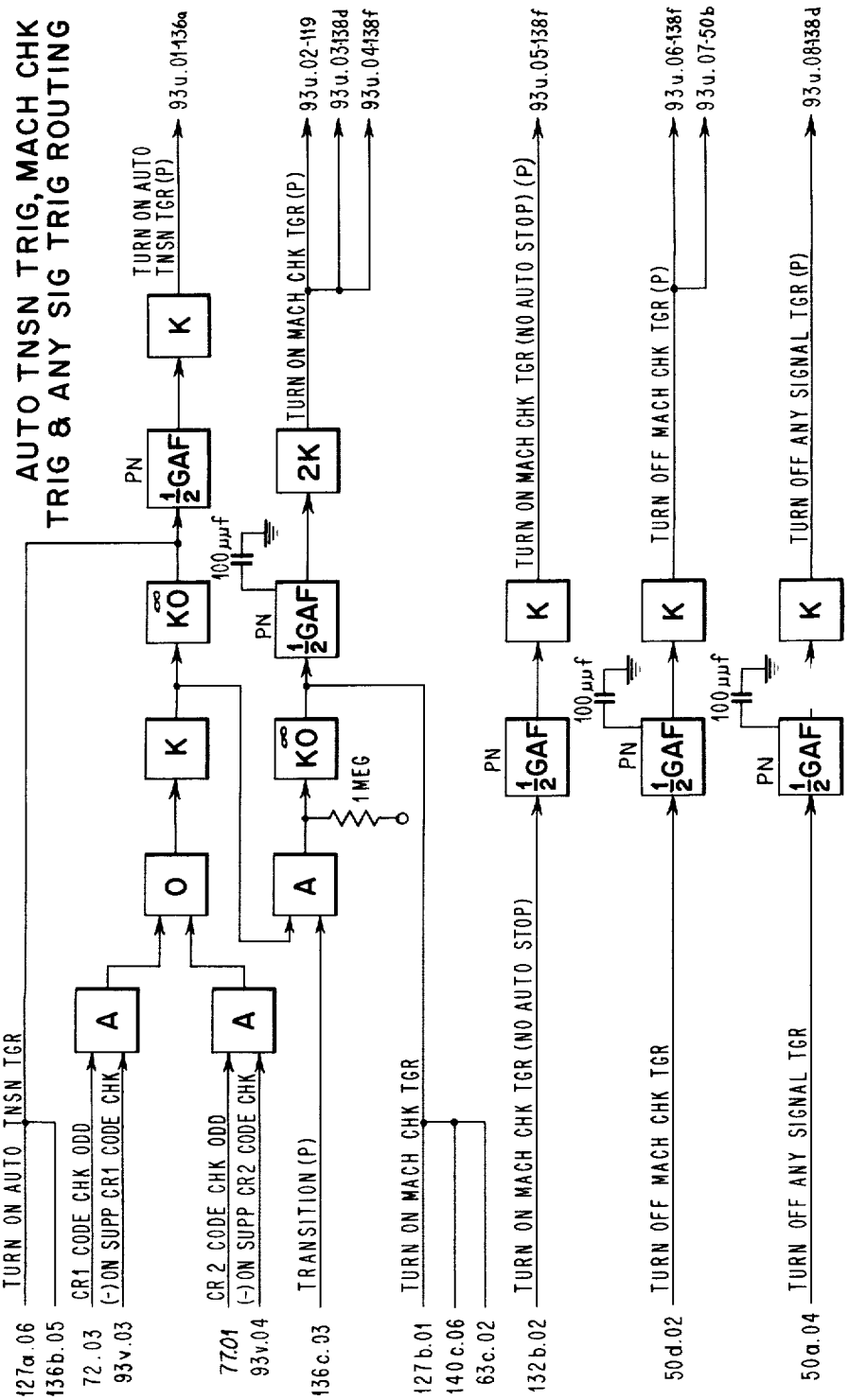

AUTO TNSN TRIG, MACH CHK TRIG & ANY SIG TRIG ROUTING
TURN ON AUTO TNSN TGR
CR1 CODE CHK ODD
(-) ON SUPP CR1 CODE CHK
CR 2 CODE CHK ODD
(-) ON SUPP CR2 CODE CHK
TRANSITION (P)
TURN ON MACH CHK TGR
TURN ON MACH CHK TGR (NO AUTO STOP)
TURN OFF MACH CHK TGR
TURN OFF ANY SIGNAL TGR
TURN ON AUTO TNSN TGR (P)
TURN ON MACH CHK TGR (P)
TURN ON MACH CHK TGR (NO AUTO STOP) (P)
TURN OFF MACH CHK TGR (P)
TURN OFF ANY SIGNAL TGR (P)
A
O
K
KO
2K
PN
1/2GAF
100 µµf
1 MEG
93u.01-136a
93u.02-119
93u.03-138d
93u.04-138f
93u.05-138f
93u.06-138f
93u.07-50b
93u.08-138d
127a.06
136b.05
72.03
93v.03
77.01
93v.04
136c.03
127b.01
140c.06
63c.02
132b.02
50d.02
50a.04

FIG. 93v

BLOCK ADD TGR, SUPP CODE CHECKING

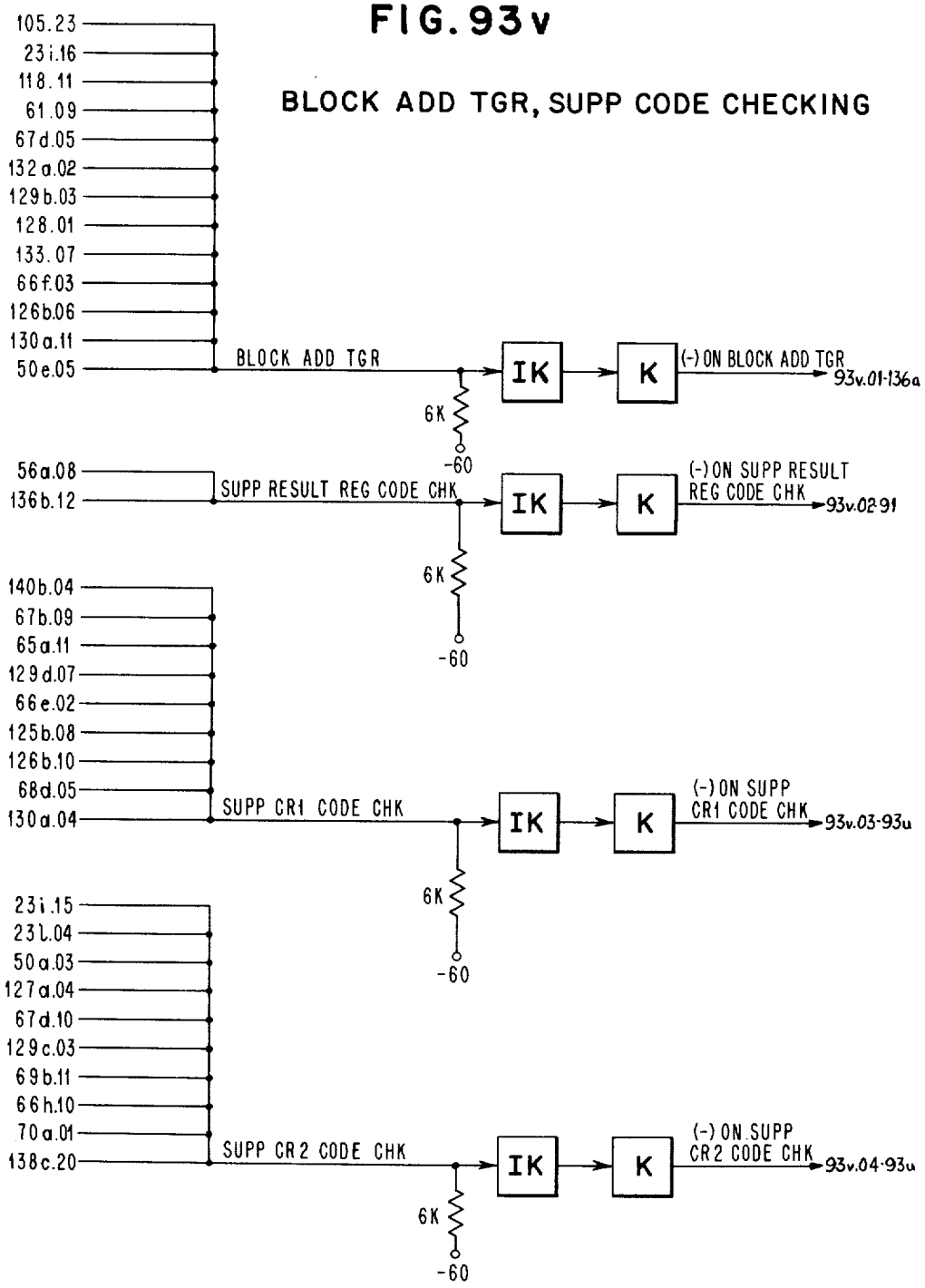


FIG.93w TYPE CYCLE NEONS, PAR I/O CHK NEON, CODE CHK NEONS

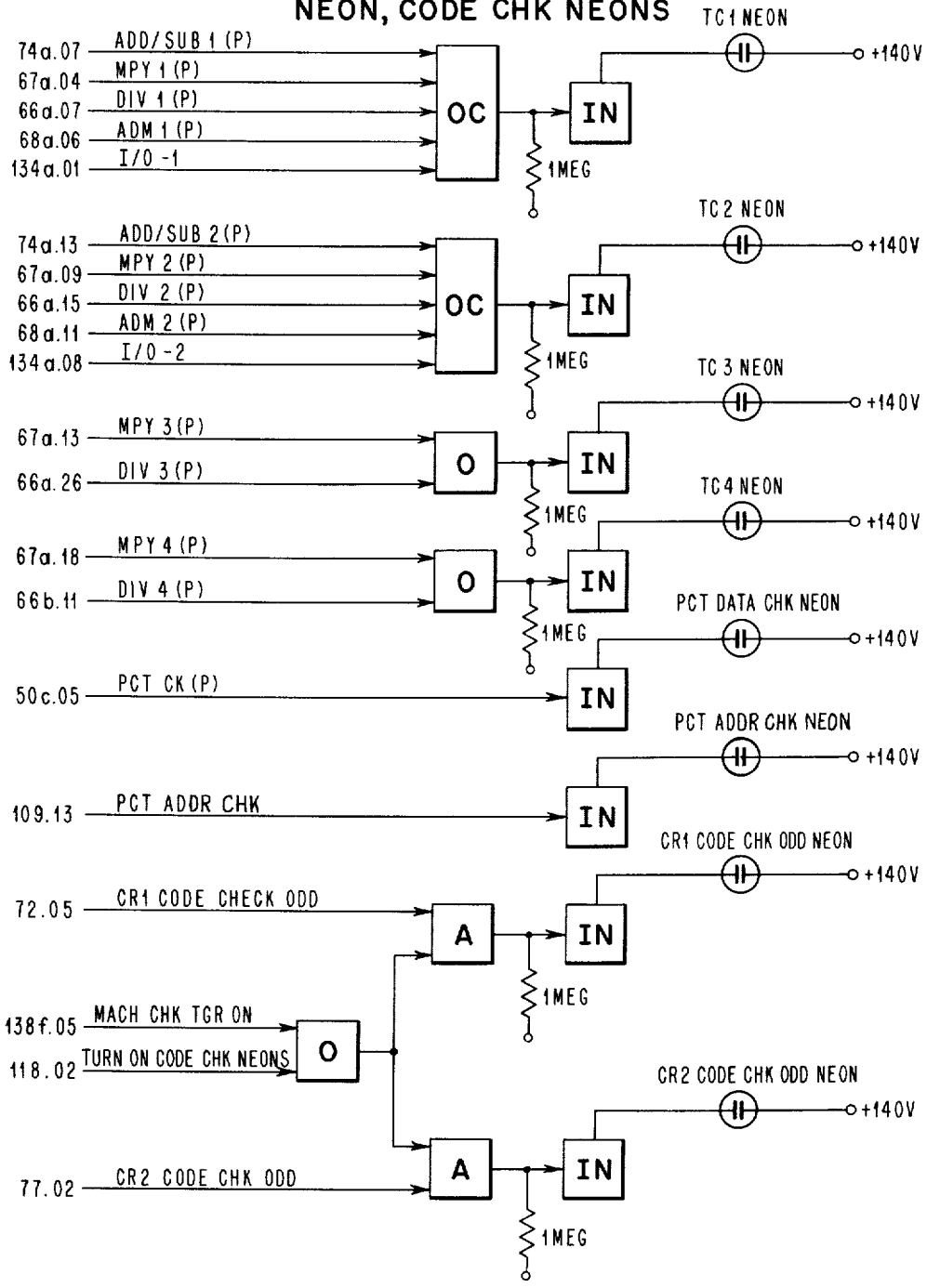


FIG. 94 P.C.T. CABLE B- CONNECTOR RECEPTACLE SHOWN FROM WIRING SIDE

8 RD BUS CHAR 0-1 14b	7 NOT DEMAND 7	6 NOT DEMAND 6	5 NOT DEMAND 5	4 NOT DEMAND 4	3 NOT DEMAND 3	2 NOT DEMAND 2	1 NOT DEMAND 1
16 RD BUS CHAR 0-B 14b	15 RD BUS CHAR 0-A 14b	14 RD BUS CHAR 0-8 14b	13 GND	12 RD BUS CHAR 0-4 14b	11 GND	10 RD BUS CHAR 0-2 14b	9 GND
24 GND	23 RD BUS CHAR 1-2 14b	22 GND	21 RD BUS CHAR 1-1 14b	20 GND	19 RD BUS CHAR 0-C 14b	18 GND	17 MBR CODE CHK 19c.02
32 RD BUS CHAR 1-B 14b	31 GND	30 RD BUS CHAR 1-A 14b	29 GND	28 RD BUS CHAR 1-8 14b	27 GND	26 RD BUS CHAR 1-4 14b	25 GND
40 GND	39 RD BUS CHAR 2-2 14a	38 GND	37 RD BUS CHAR 2-1 14a	36 GND	35 RD BUS CHAR 1-C 14b	34 GND	33 SPARE
48 RD BUS CHAR 2-B 14a	47 GND	46 RD BUS CHAR 2-A 14a	45 GND	44 RD BUS CHAR 2-8 14a	43 GND	42 RD BUS CHAR 2-4 14a	41 GND
56 GND	55 RD BUS CHAR 3-2 14a	54 GND	53 RD BUS CHAR 3-1 14a	52 GND	51 RD BUS CHAR 2-C 14a	50 GND	49 SPARE
64 RD BUS CHAR 3-B 14a	63 GND	62 RD BUS CHAR 3-A 14a	61 GND	60 RD BUS CHAR 3-8 14a	59 GND	58 RD BUS CHAR 3-4 14a	57 GND
72 GND	71 RD BUS CHAR 4-2 14a	70 GND	69 RD BUS CHAR 4-1 14a	68 GND	67 RD BUS CHAR 3-C 14a	66 GND	65 SPARE
80 RD BUS CHAR 4-B 14a	79 GND	78 RD BUS CHAR 4-A 14a	77 GND	76 RD BUS CHAR 4-8 14a	75 GND	74 RD BUS CHAR 4-4 14a	73 GND
88 GND	87 WR BUS CHAR 0-2 18b.06	86 GND	85 WR BUS CHAR 0-1 18b.07	84 GND	83 RD BUS CHAR 4-C 14a	82 GND	81 SPARE
96 WR BUS CHAR 0-B 18b.02	95 GND	94 WR BUS CHAR 0-A 18b.03	93 GND	92 WR BUS CHAR 0-8 18b.04	91 GND	90 WR BUS CHAR 0-4 18b.05	89 GND
104 GND	103 WR BUS CHAR 1-2 18b.06	102 GND	101 WR BUS CHAR 1-1 18b.07	100 GND	99 WR BUS CHAR 0-C 18b.01	98 GND	97 SPARE
112 WR BUS CHAR 1-B 18b.02	111 GND	110 WR BUS CHAR 1-A 18b.03	109 GND	108 WR BUS CHAR 1-8 18b.04	107 GND	106 WR BUS CHAR 1-4 18b.05	105 GND
120 GND	119 WR BUS CHAR 2-2 18a.06	118 GND	117 WR BUS CHAR 2-1 18a.07	116 GND	115 WR BUS CHAR 1-C 18b.01	114 GND	113 SPARE
128 WR BUS CHAR 2-B 18a.02	127 GND	126 WR BUS CHAR 2-A 18a.03	125 GND	124 WR BUS CHAR 2-8 18a.04	123 GND	122 WR BUS CHAR 2-4 18a.05	121 GND
136 GND	135 WR BUS CHAR 3-2 18a.06	134 GND	133 WR BUS CHAR 3-1 18a.07	132 GND	131 WR BUS CHAR 2-C 18a.01	130 GND	129 SPARE
144 WR BUS CHAR 3-B 18a.02	143 GND	142 WR BUS CHAR 3-A 18a.03	141 GND	140 WR BUS CHAR 3-8 18a.04	139 GND	138 WR BUS CHAR 3-4 18a.05	137 GND
152 GND	151 WR BUS CHAR 4-4 18a.05	150 GND	149 WR BUS CHAR 4-2 18a.06	148 GND	147 WR BUS CHAR 4-1 18a.07	146 GND	145 WR BUS CHAR 3-C 18a.01
160 WR BUS CHAR 4-C 18a.01	159 GND	158 WR BUS CHAR 4-B 18a.02	157 GND	156 WR BUS CHAR 4-A 18a.03	155 GND	154 WR BUS CHAR 4-8 18a.04	153 GND

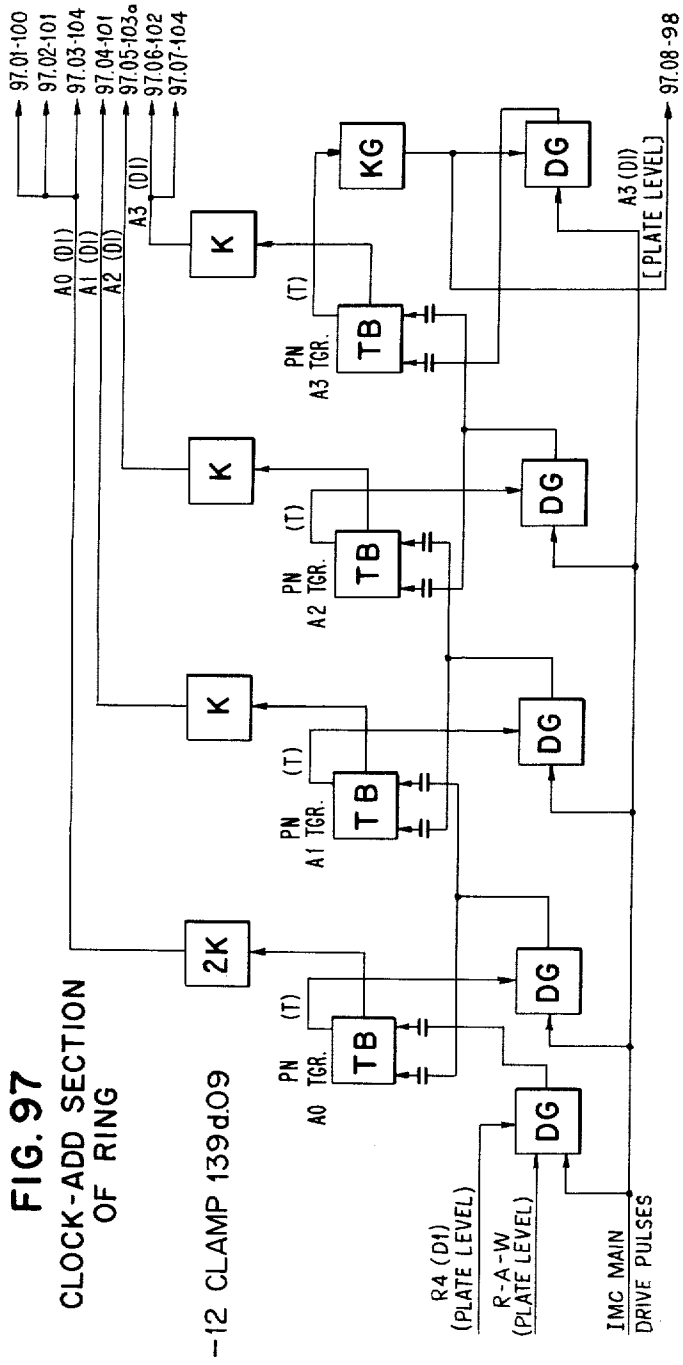


FIG. 97
CLOCK-ADD SECTION OF RING
-12 CLAMP 139d09

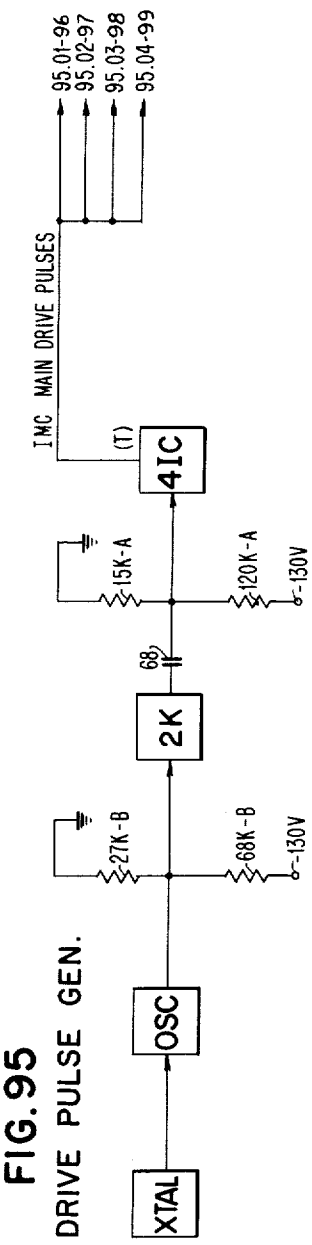


FIG. 95
IMC DRIVE PULSE GEN.

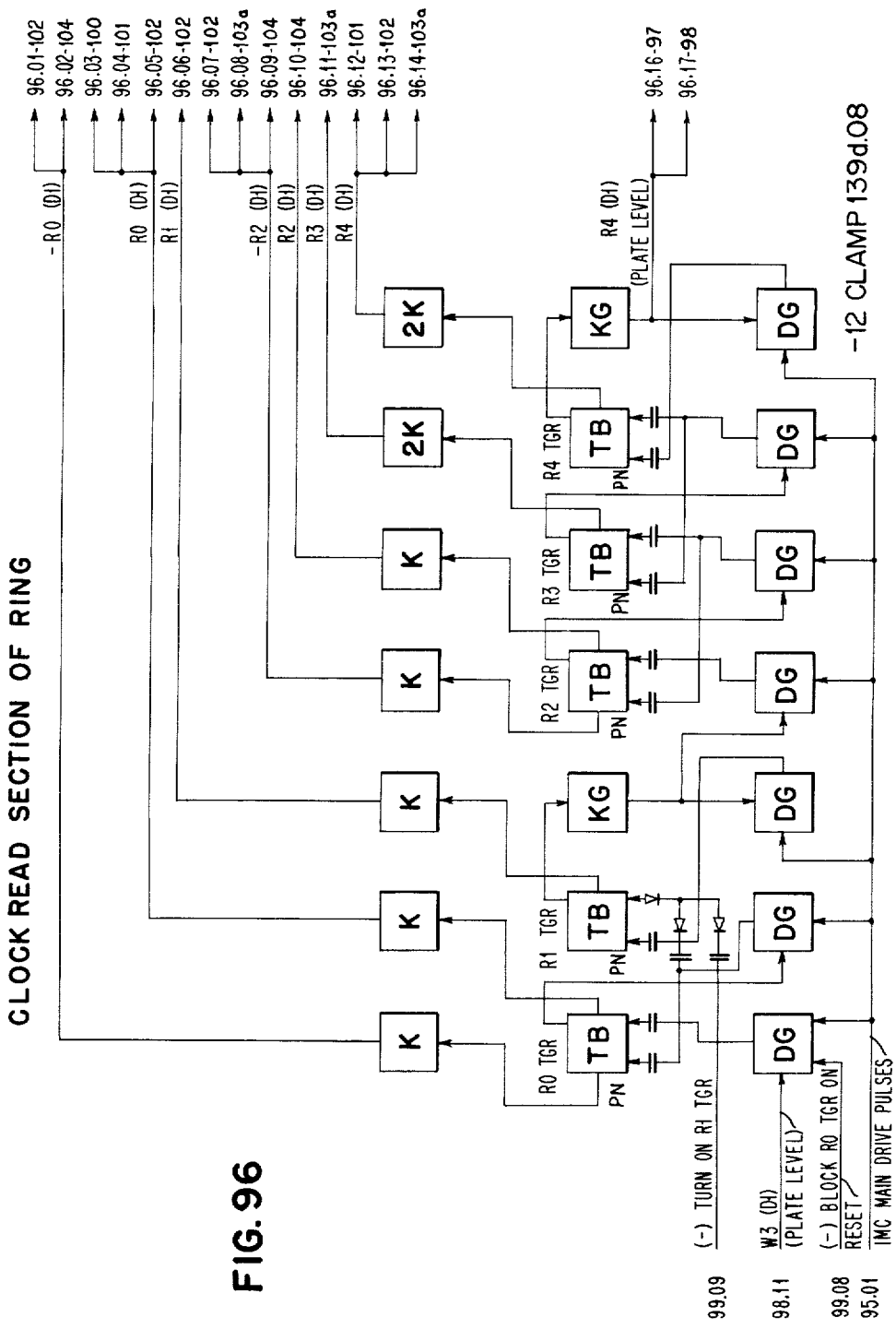

CLOCK READ SECTION OF RING
96.01-102
96.02-104
96.03-100
96.04-101
96.05-102
96.06-102
96.07-102
96.08-103a
96.09-104
96.10-104
96.11-103a
96.12-101
96.13-102
96.14-103a
96.16-97
96.17-98
-R0 (D1)
R0 (D1)
R1 (D1)
-R2 (D1)
R2 (D1)
R3 (D1)
R4 (D1)
R4 (D1) (PLATE LEVEL)
2K
K
KG
TB
DG
R4 TGR
R3 TGR
R2 TGR
R1 TGR
R0 TGR
PN
-12 CLAMP 139d.08
99.09 (-) TURN ON R1 TGR
98.11 W3 (D1) (PLATE LEVEL)
99.08 (-) BLOCK R0 TGR ON RESET
95.01 IMC MAIN DRIVE PULSES

FIG. 96

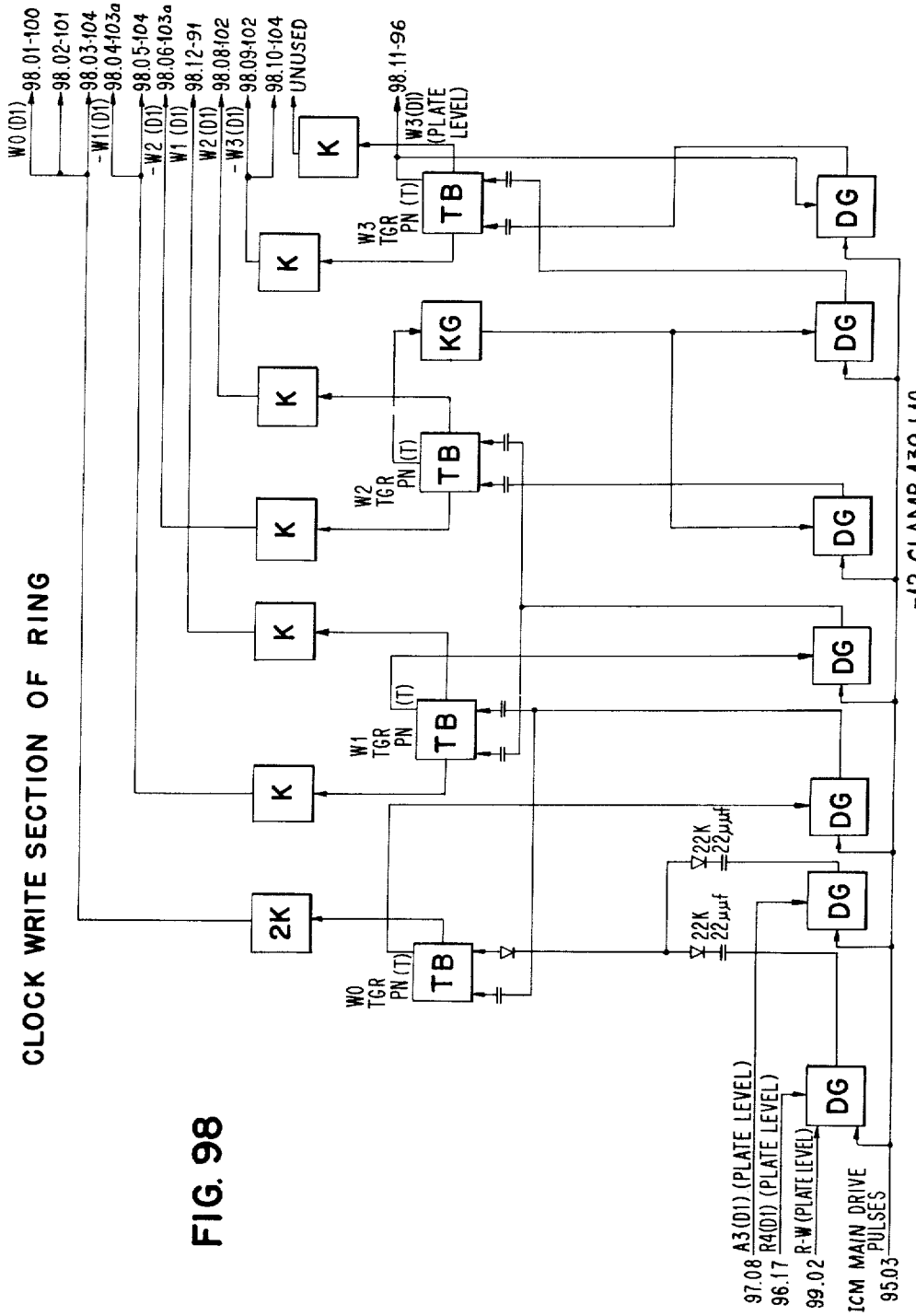

CLOCK WRITE SECTION OF RING
W0 (D1)
98.01-100
98.02-101
-W1 (D1)
98.03-104
98.04-103a
-W2 (D1)
98.05-104
98.06-103a
W1 (D1)
98.12-91
W2 (D1)
98.08-102
-W3 (D1)
98.09-102
98.10-104
UNUSED
98.11-96
W3(D1) (PLATE LEVEL)
K
TB
W3 TGR PN (T)
DG
KG
W2 TGR PN (T)
W1 TGR PN (T)
2K
W0 TGR PN (T)
22K 22μμf
-12 CLAMP 139d.10
97.08 A3(D1) (PLATE LEVEL)
96.17 R4(D1) (PLATE LEVEL)
99.02 R-W (PLATE LEVEL)
ICM MAIN DRIVE PULSES
95.03

FIG. 98

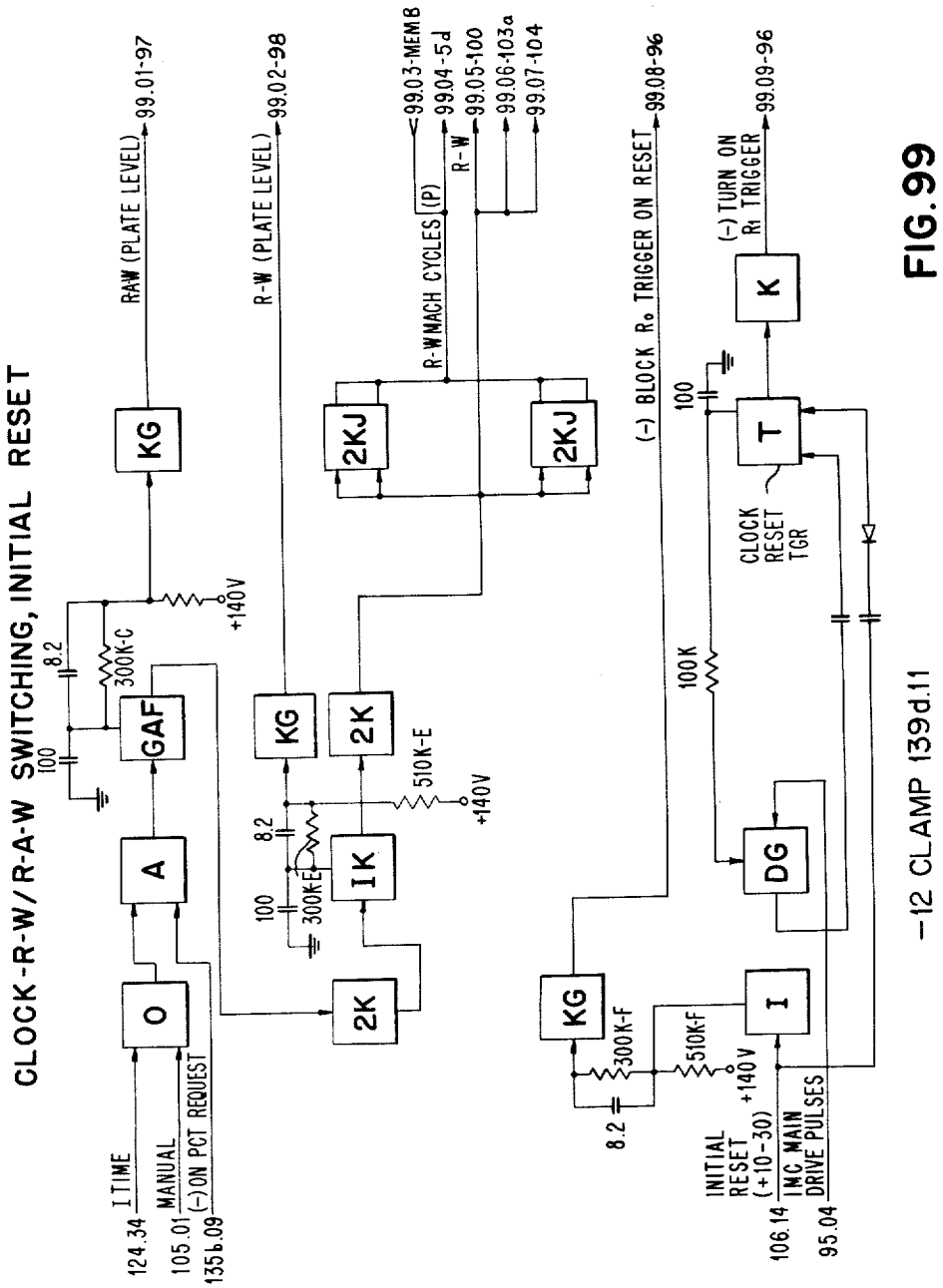


FIG. 99

-12 CLAMP 139d.11

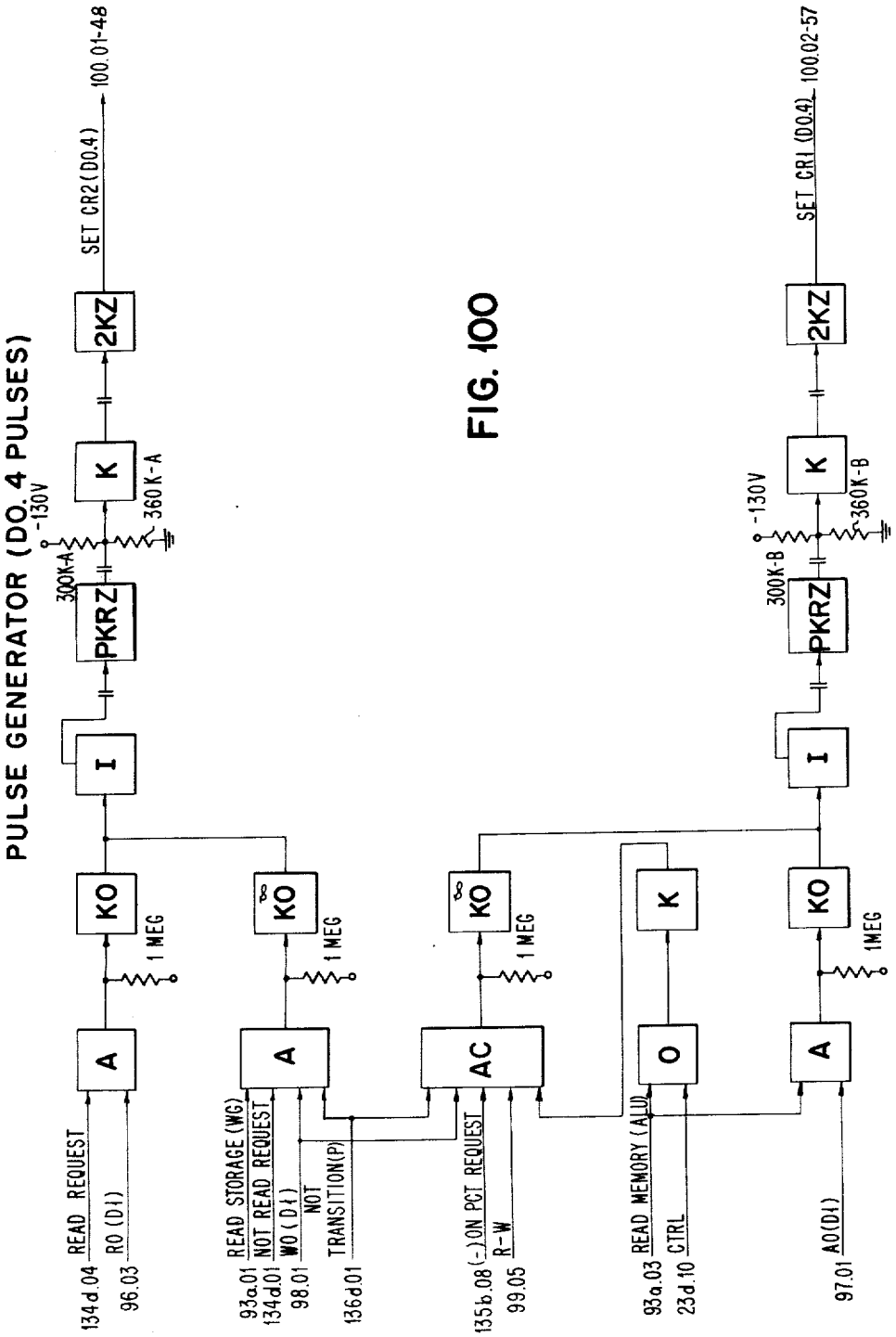
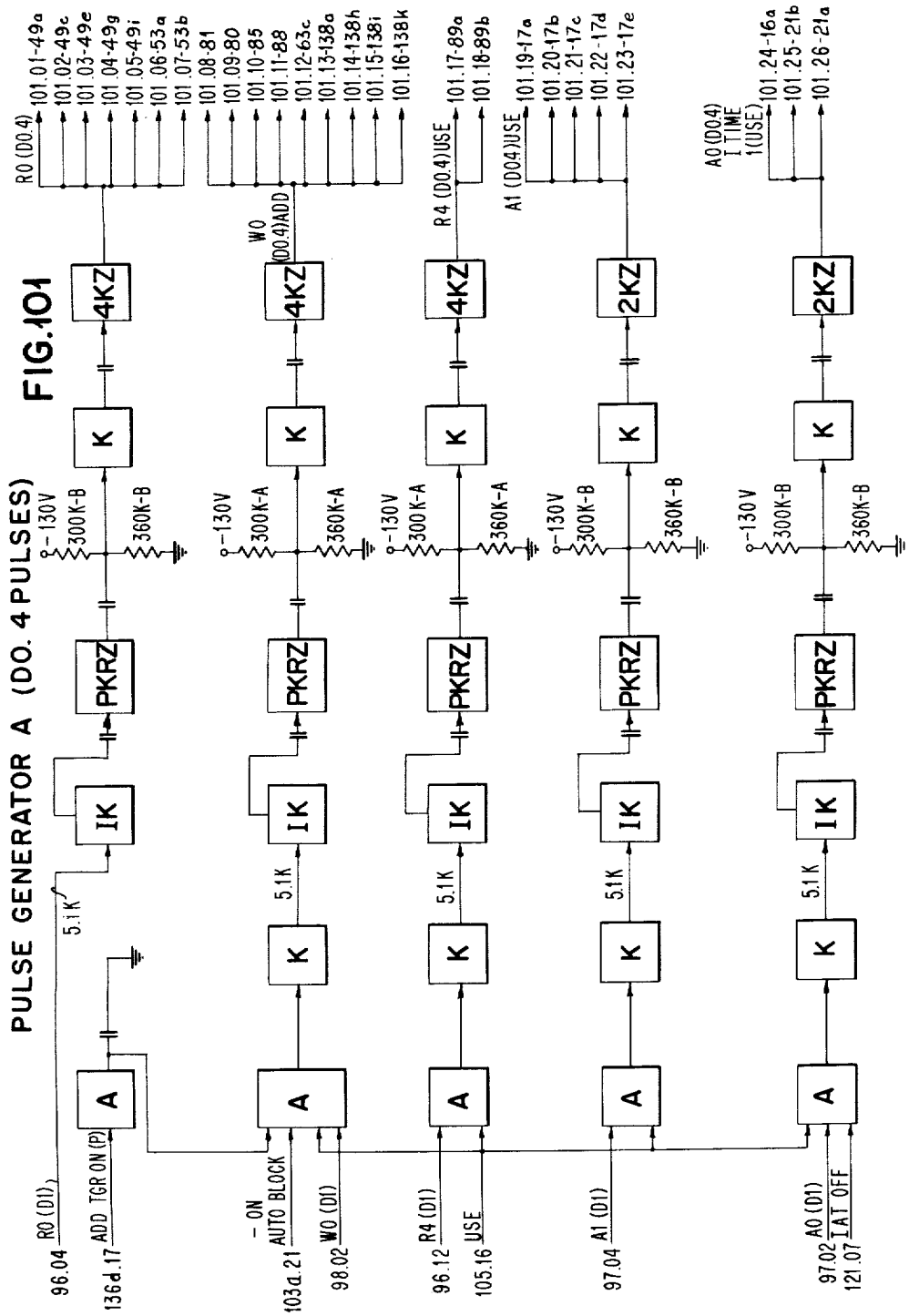

PULSE GENERATOR (DO. 4 PULSES)
READ REQUEST
134d.04
RO (D1)
96.03
READ STORAGE (WG)
93a.01
NOT READ REQUEST
134d.01
WO (D1)
98.01
NOT TRANSITION(P)
136d.01
(-) ON PCT REQUEST
135b.08
R-W
99.05
READ MEMORY (ALU)
93a.03
CTRL
23d.10
A0(D1)
97.01
A
KO
1 MEG
I
PKRZ
300K-A
-130V
K
360 K-A
2KZ
SET CR2(D0.4)
100.01-48
AC
O
1MEG
300K-B
360K-B
SET CR1 (D0.4)
100.02-57

FIG. 100

FIG. 101


PULSE GENERATOR A (DO. 4 PULSES)
R0 (D0.4)
101.01-49a
101.02-49c
101.03-49e
101.04-49g
101.05-49i
101.06-53a
101.07-53b
101.08-81
101.09-80
101.10-85
101.11-88
101.12-63c
101.13-138a
101.14-138h
101.15-138i
101.16-138k
W0 (D0.4)ADD
R4 (D0.4)USE
101.17-89a
101.18-89b
A1 (D0.4)USE
101.19-17a
101.20-17b
101.21-17c
101.22-17d
101.23-17e
A0 (D0.4) I TIME 1(USE)
101.24-16a
101.25-21b
101.26-21a
4KZ
2KZ
K
IK
PKRZ
A
-130V
300K-B
360K-B
300K-A
360K-A
5.1K
96.04 R0 (D1)
136d.17 ADD TGR ON (P)
103a.21 - ON AUTO BLOCK
98.02 W0 (D1)
96.12 R4 (D1)
105.16 USE
97.04 A1 (D1)
97.02 A0 (D1)
121.07 IAT OFF

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OVERLAP MODE CONTROL

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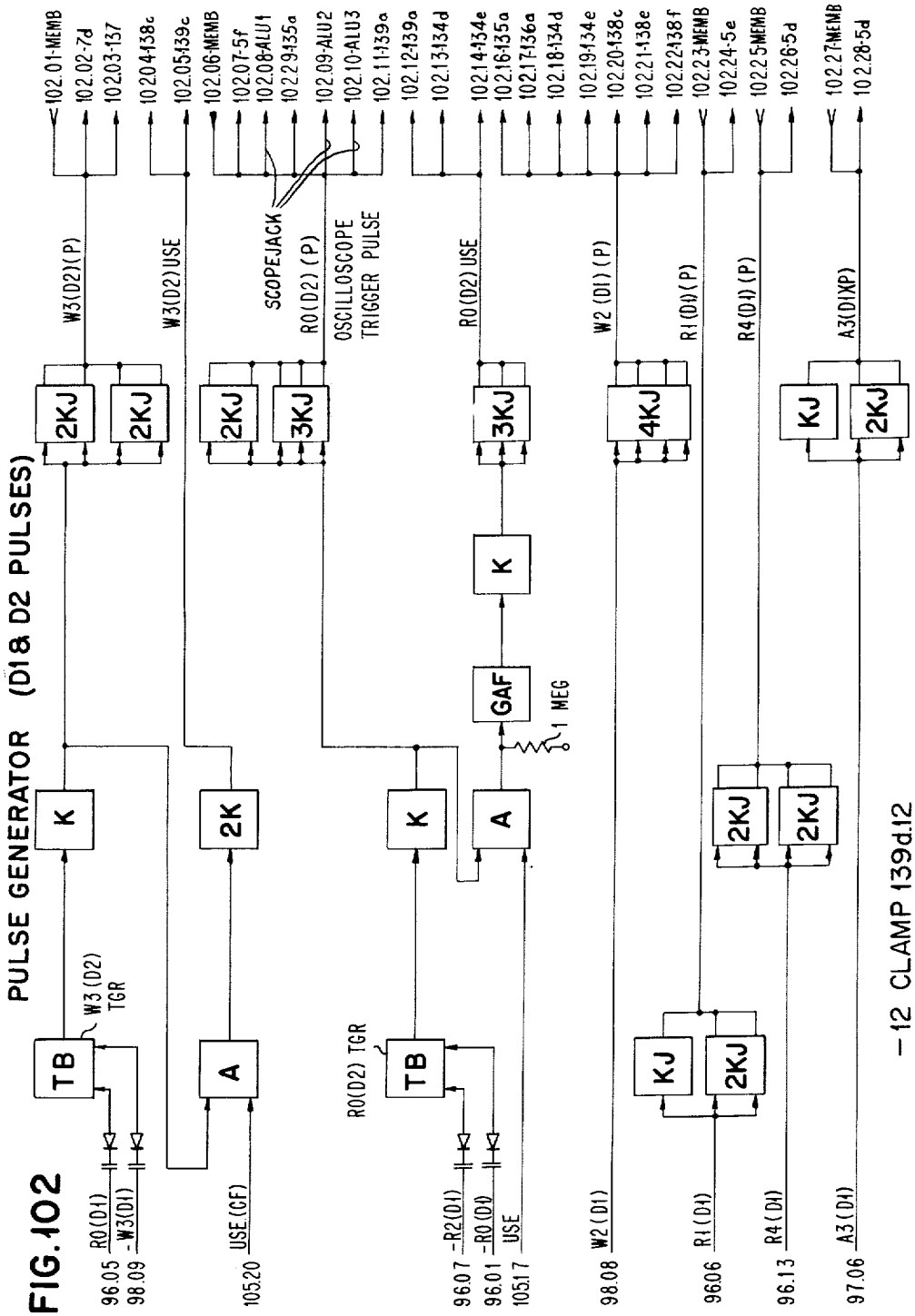


FIG. 102

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OVERLAP MODE CONTROL

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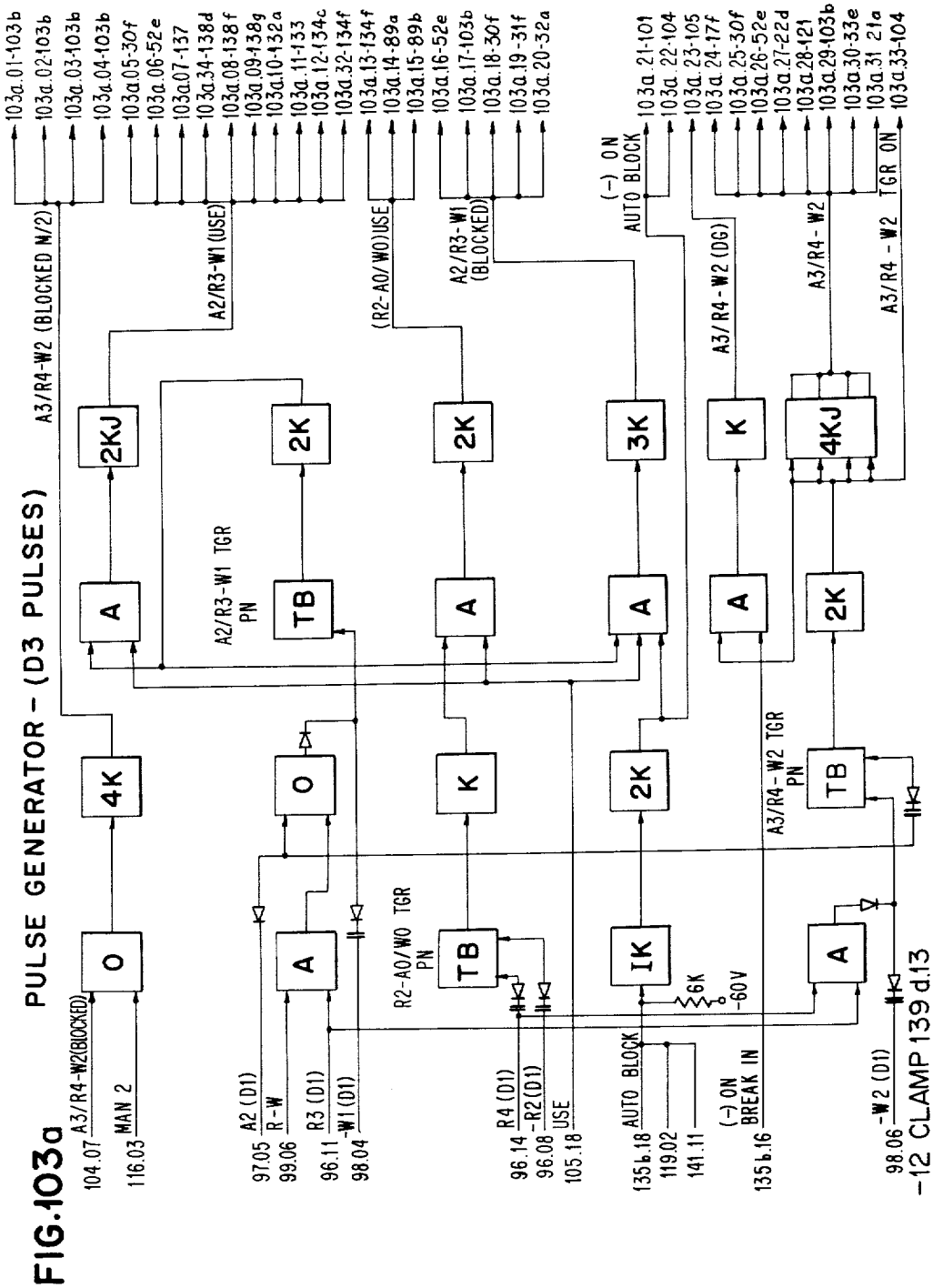
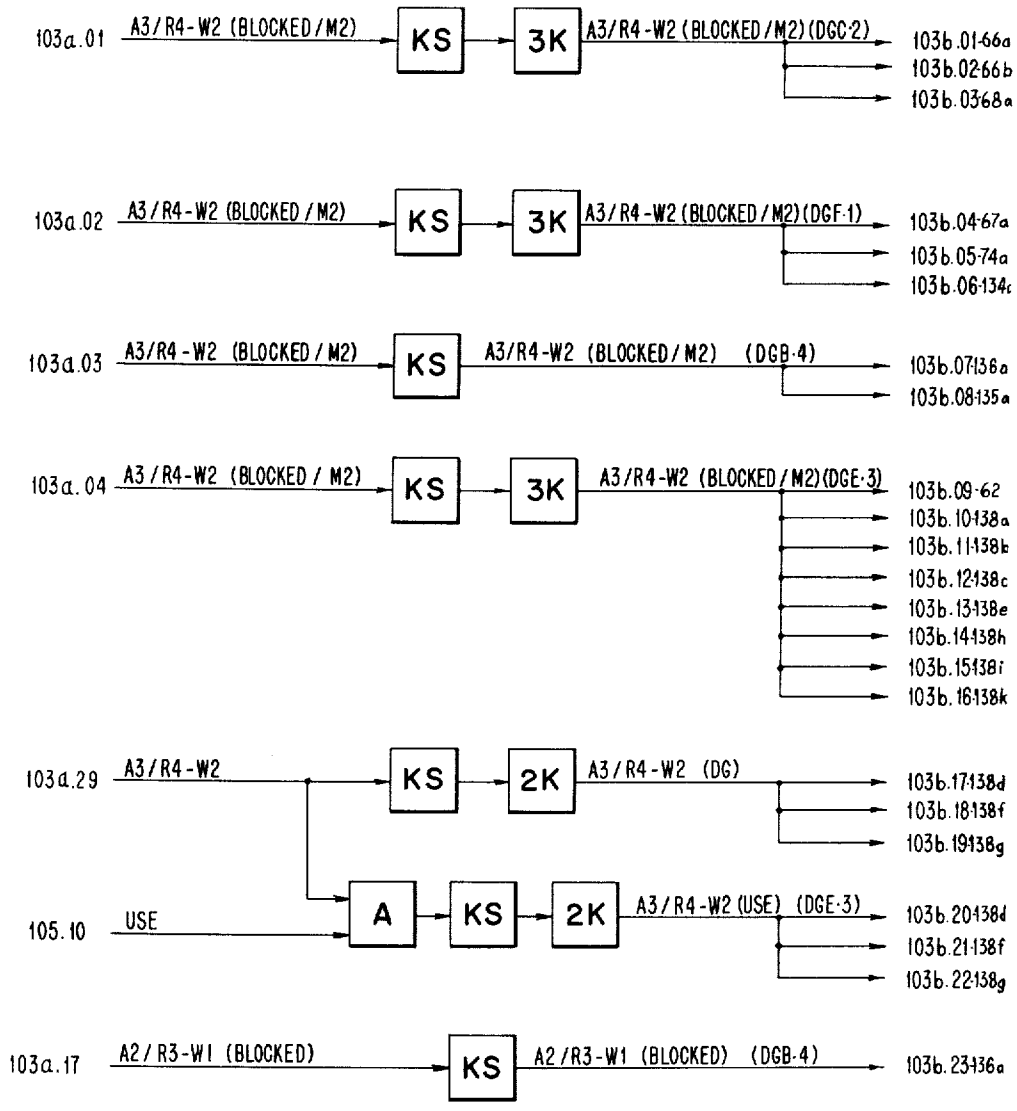


FIG.103a

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FIG. 103b

C.F. PULSE POWER



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PULSE GENERATOR (D3 & D4 PULSES)

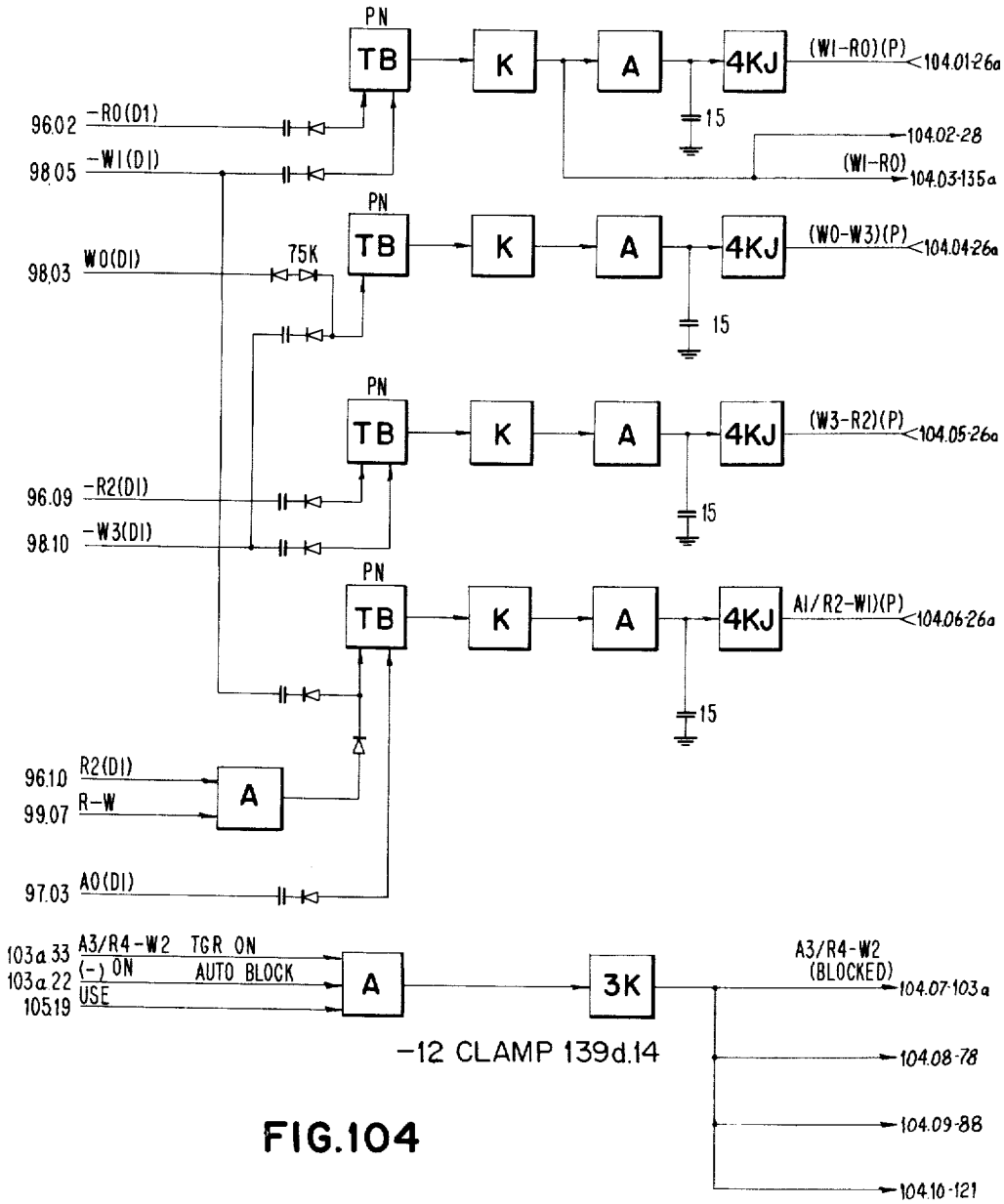
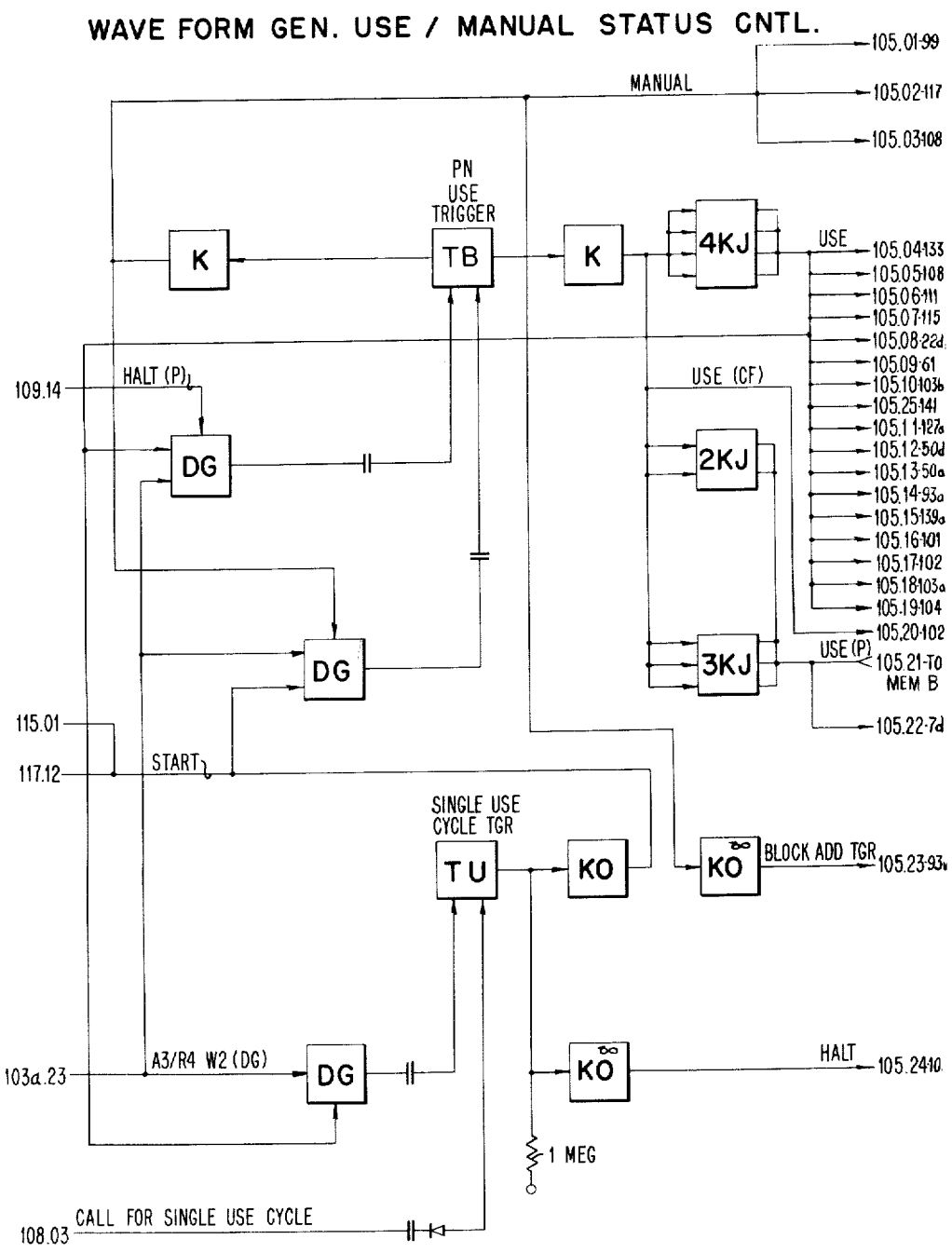


FIG.104



INITIAL RESET (U) 139c.13
−12 CLAMP 139d.15

FIG. 105

FIG. 106

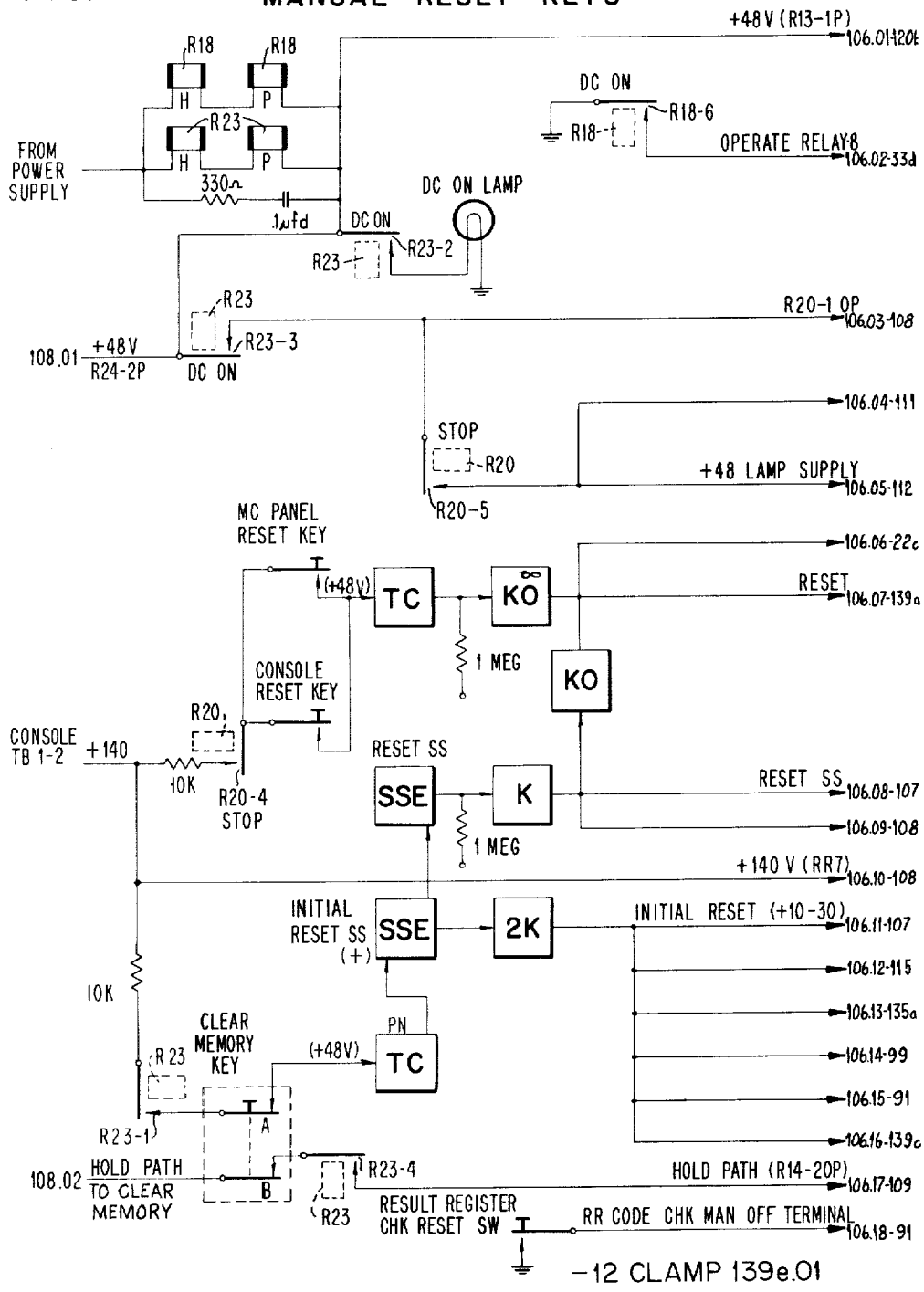
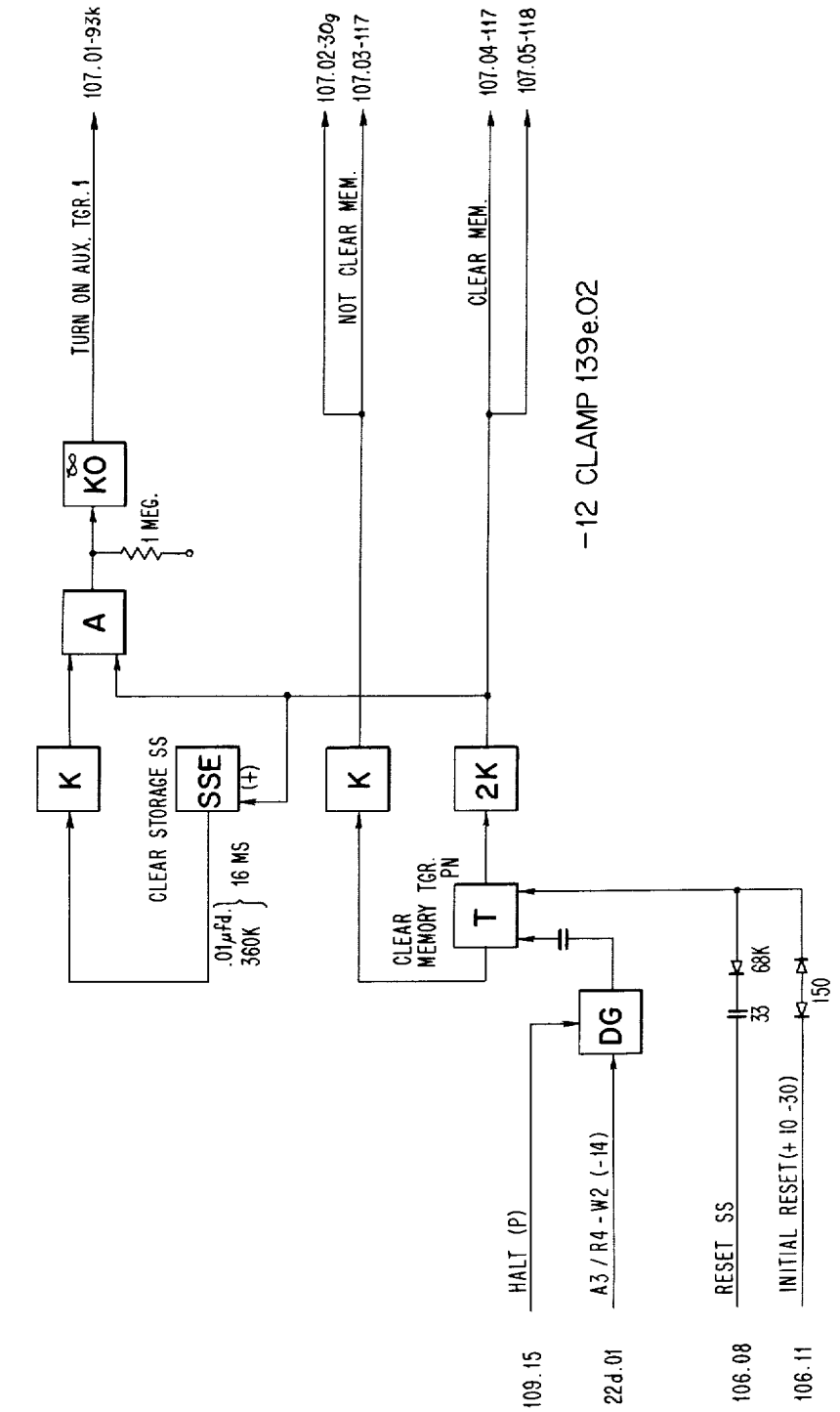

MANUAL RESET KEYS
+48 V (R13-1P)
106.01-120t
R18
R18
H
P
R23
H
P
FROM POWER SUPPLY
330Ω
.1μfd
DC ON
DC ON
R18-6
R18-
OPERATE RELAY 8
106.02-33d
DC ON LAMP
R23-2
R23
R20-1 OP
106.03-108
108.01 +48V
R24-2P
R23-3
DC ON
106.04-111
STOP
R20
+48 LAMP SUPPLY
106.05-112
R20-5
MC PANEL RESET KEY
106.06-22c
(+48V)
TC
KO
RESET
106.07-139a
1 MEG
KO
CONSOLE RESET KEY
R20
CONSOLE TB 1-2 +140
10K
R20-4 STOP
RESET SS
SSE
K
RESET SS
106.08-107
106.09-108
1 MEG
+140 V (RR7)
106.10-108
INITIAL RESET SS (+)
SSE
2K
INITIAL RESET (+10-30)
106.11-107
106.12-115
106.13-135a
106.14-99
106.15-91
106.16-139c
10K
CLEAR MEMORY KEY
PN
(+48V)
TC
R23
R23-1
A
B
108.02 HOLD PATH TO CLEAR MEMORY
R23-4
R23
HOLD PATH (R14-20P)
106.17-109
RESULT REGISTER CHK RESET SW
RR CODE CHK MAN OFF TERMINAL
106.18-91
-12 CLAMP 139e.01

FIG. 107
CLEAR MEMORY TRIGGER



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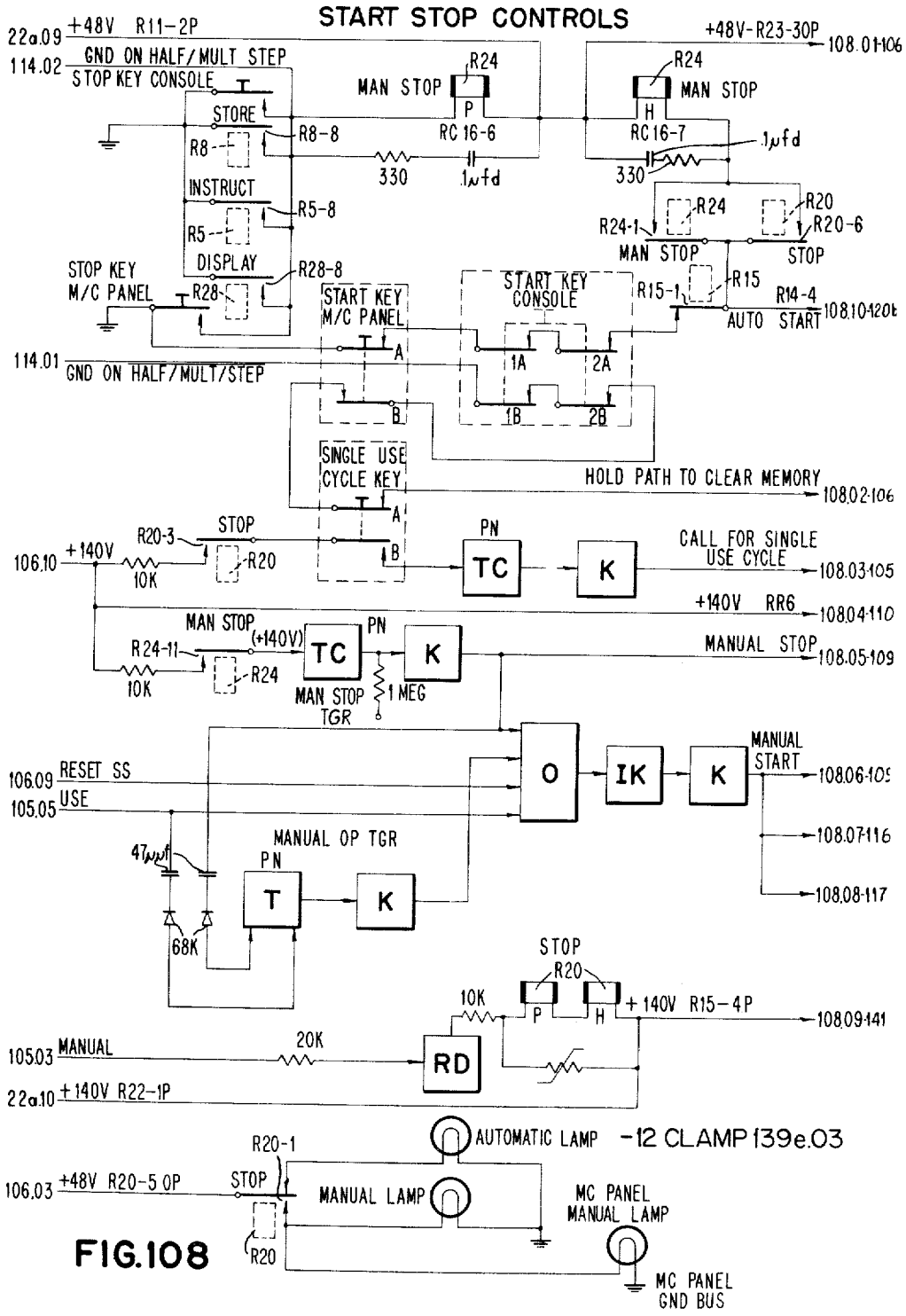


FIG.108

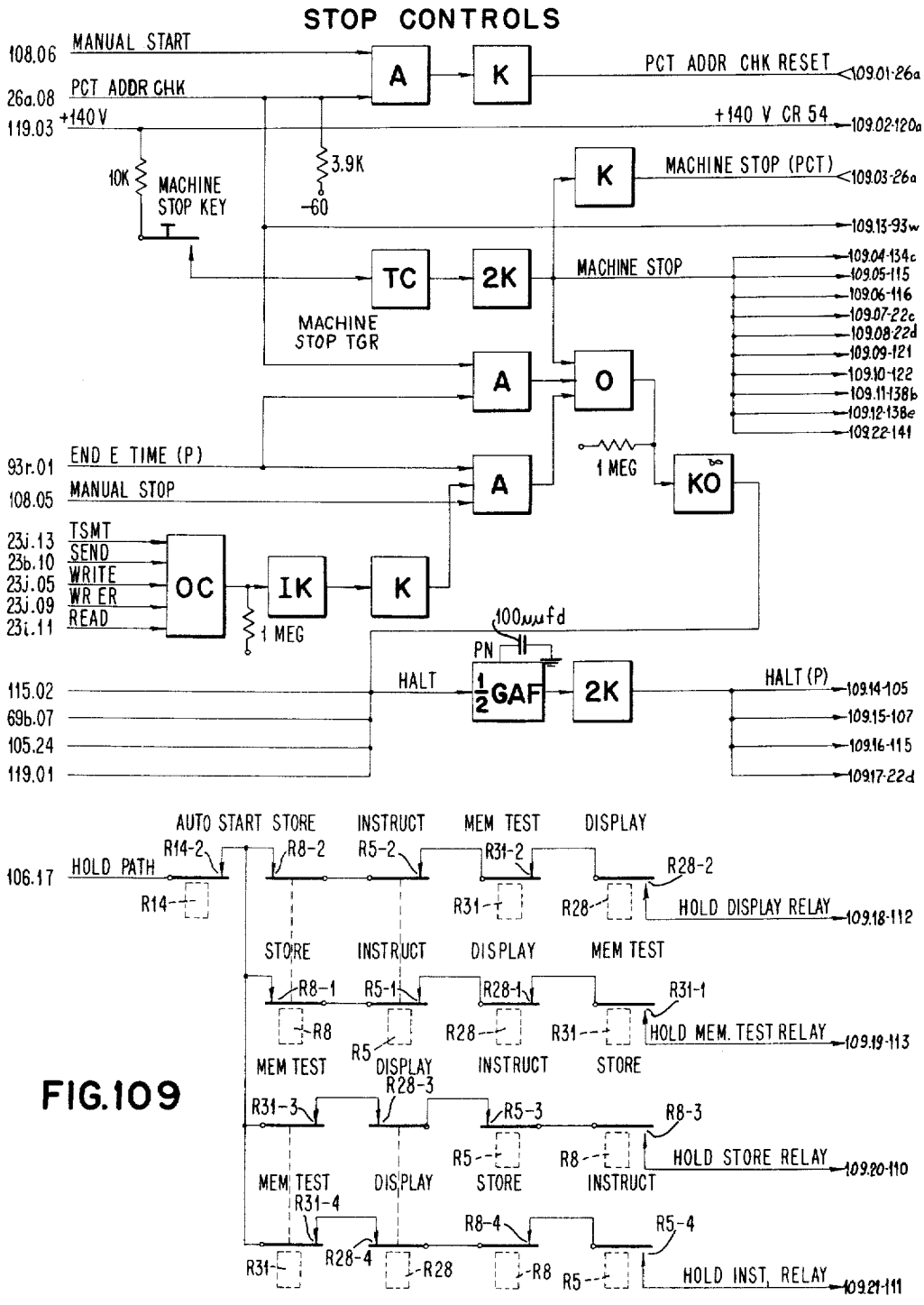

STOP CONTROLS
108.06 MANUAL START
26a.08 PCT ADDR CHK
119.03 +140 V
A
K
PCT ADDR CHK RESET
109.01-26a
+140 V CR 54
109.02-120a
10K
MACHINE STOP KEY
3.9K
-60
K
MACHINE STOP (PCT)
109.03-26a
109.13-93w
TC
2K
MACHINE STOP
MACHINE STOP TGR
109.04-134c
109.05-115
109.06-116
109.07-22c
109.08-22d
109.09-121
109.10-122
109.11-138b
109.12-138e
109.22-141
A
O
93r.01 END E TIME (P)
108.05 MANUAL STOP
A
1 MEG
KO
23j.13 TSMT
23b.10 SEND
23j.05 WRITE
23j.09 WR ER
23i.11 READ
OC
IK
K
1 MEG
100μμfd
PN
115.02
69b.07
105.24
119.01
HALT
½GAF
2K
HALT (P)
109.14-105
109.15-107
109.16-115
109.17-22d
106.17 HOLD PATH
AUTO START STORE
INSTRUCT
MEM TEST
DISPLAY
R14-2
R8-2
R5-2
R31-2
R28-2
R14
R31
R28
HOLD DISPLAY RELAY
109.18-112
STORE
INSTRUCT
DISPLAY
MEM TEST
R8-1
R5-1
R28-1
R31-1
R8
R5
R28
R31
HOLD MEM. TEST RELAY
109.19-113
MEM TEST
DISPLAY
INSTRUCT
STORE
R31-3
R28-3
R5-3
R8-3
R5
R8
HOLD STORE RELAY
109.20-110
MEM TEST
DISPLAY
STORE
INSTRUCT
R31-4
R8-4
R5-4
R31
R28-4
R28
R8
R5
HOLD INST. RELAY
109.21-111

FIG.109

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MANUAL STORE CONTROLS

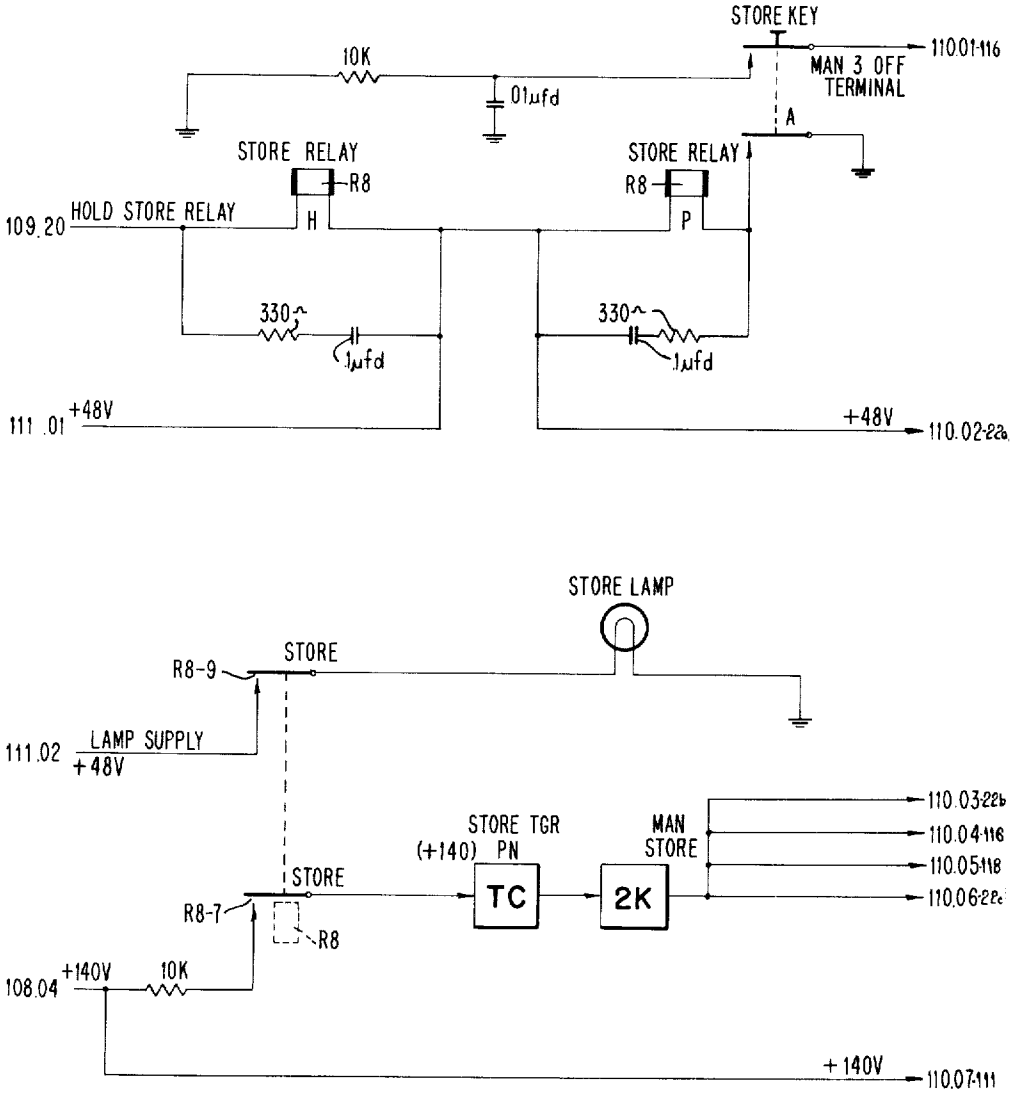


FIG. 110

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FIG. 111

MANUAL INSTRUCTION CONTROLS

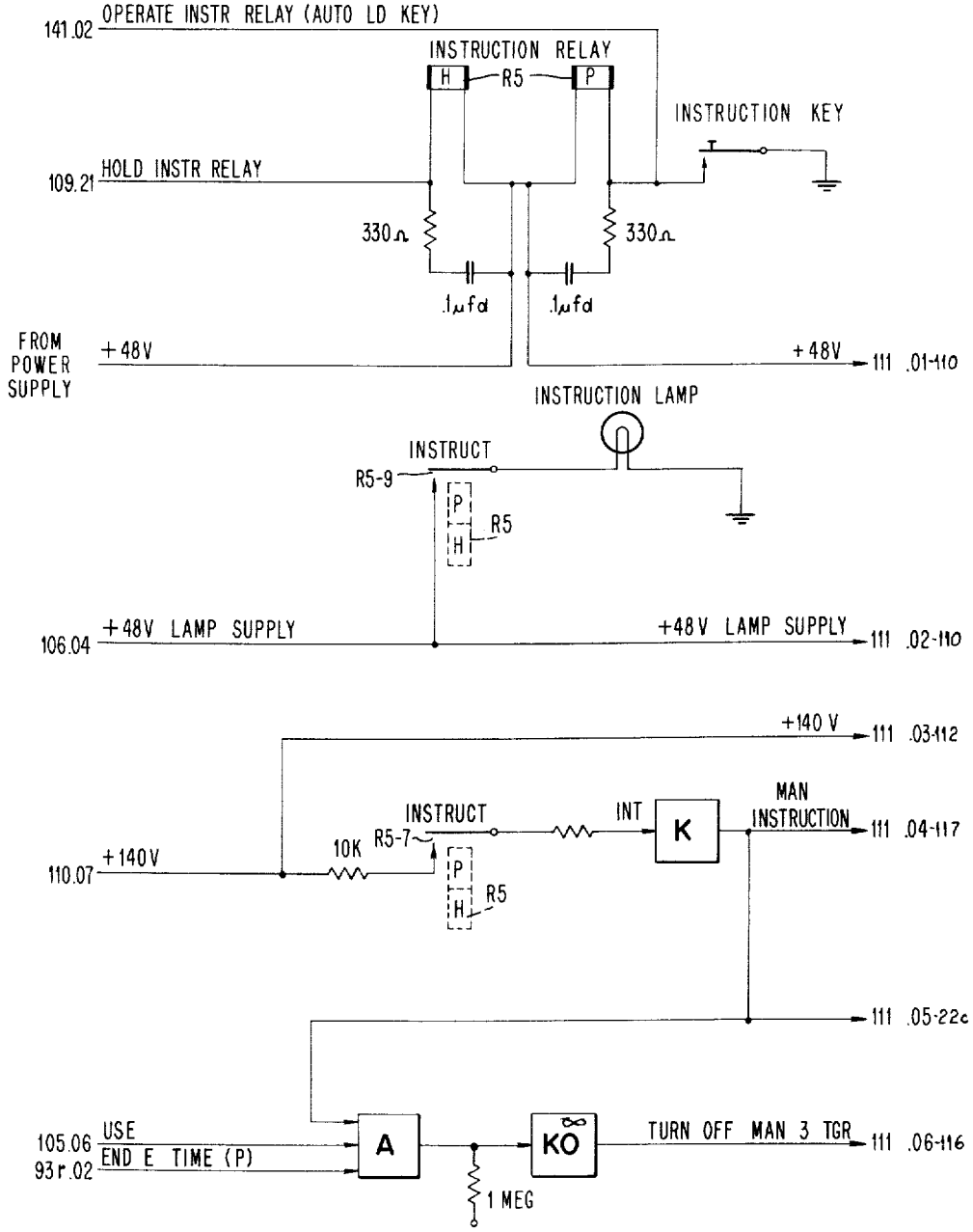
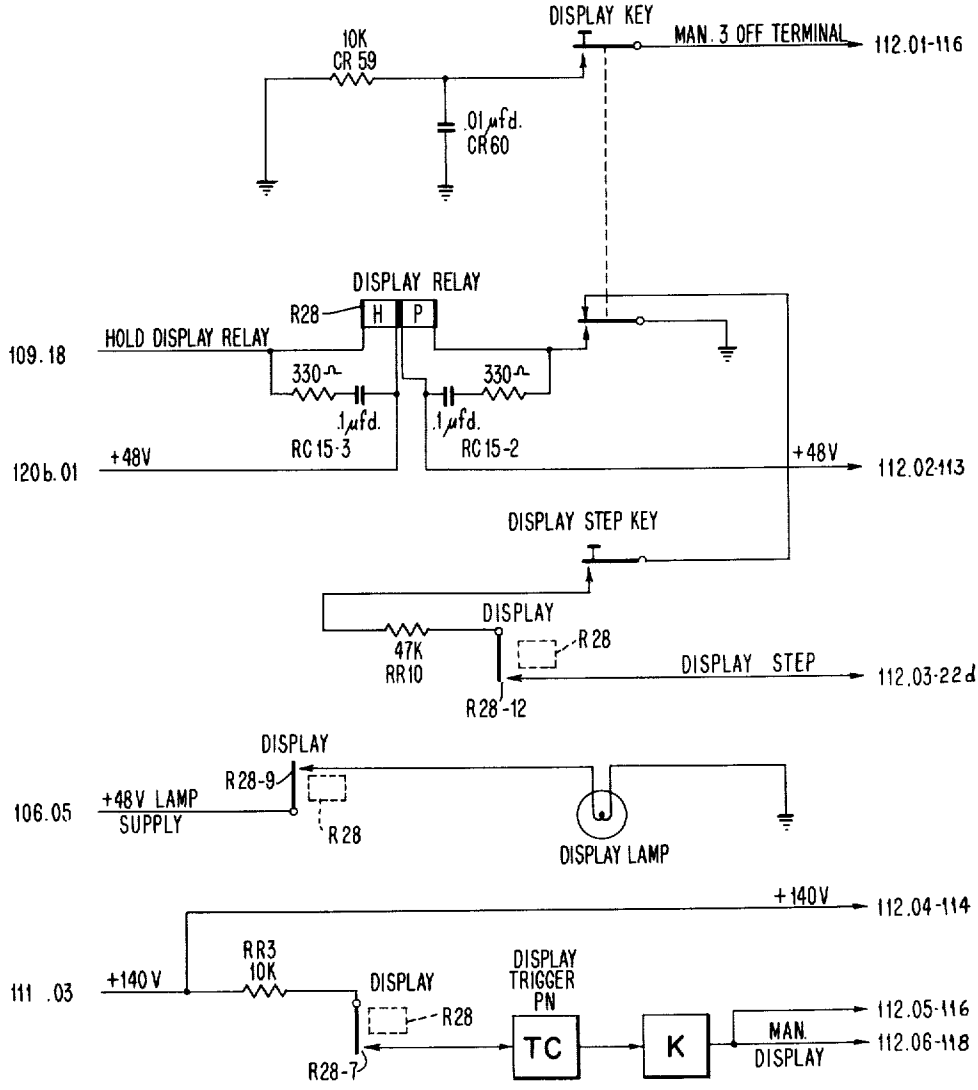


FIG. 112
MANUAL DISPLAY CONTROLS



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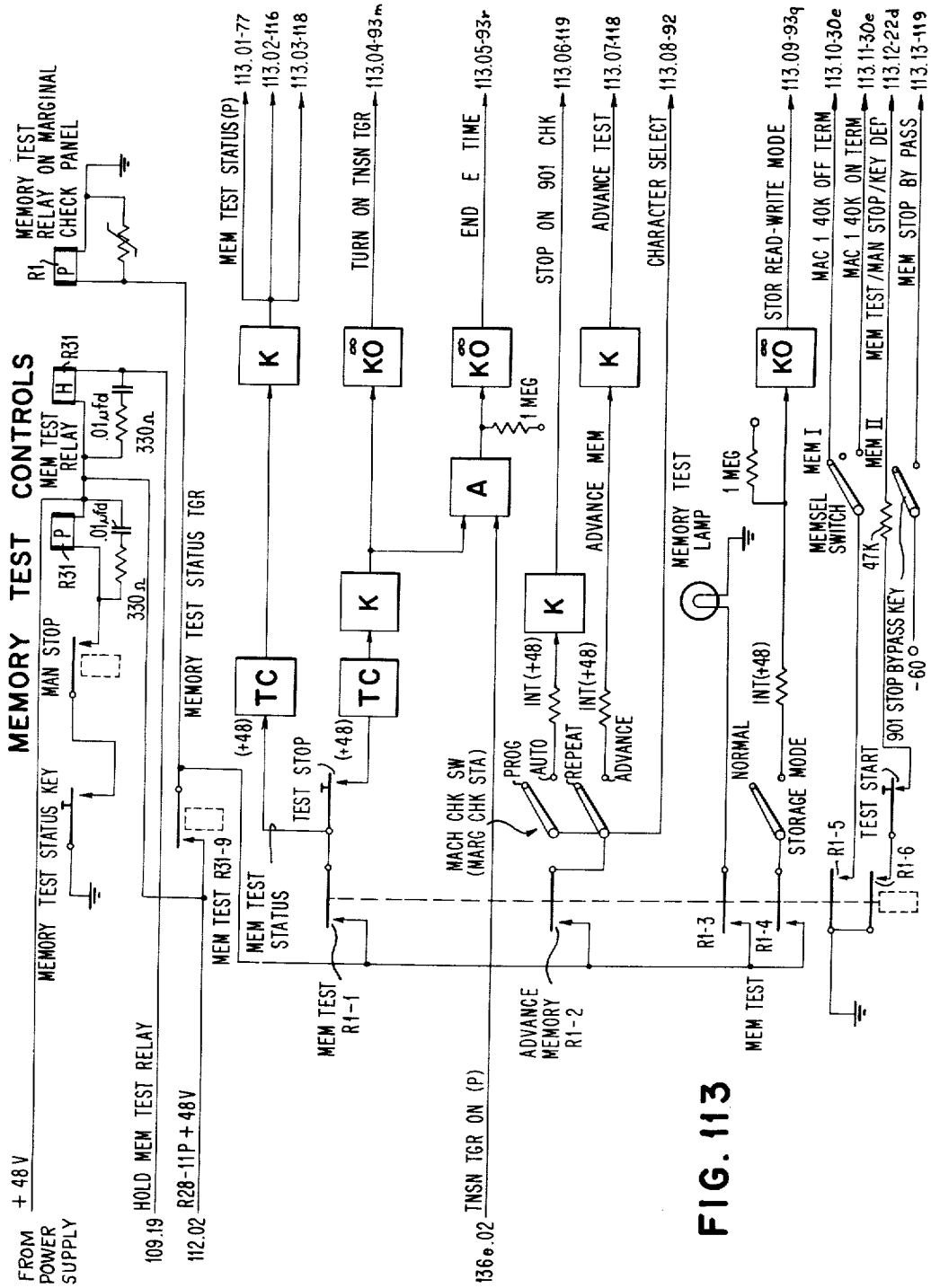


FIG. 113

FIG. 114
HALF / MULTIPLE STEP CONTROLS

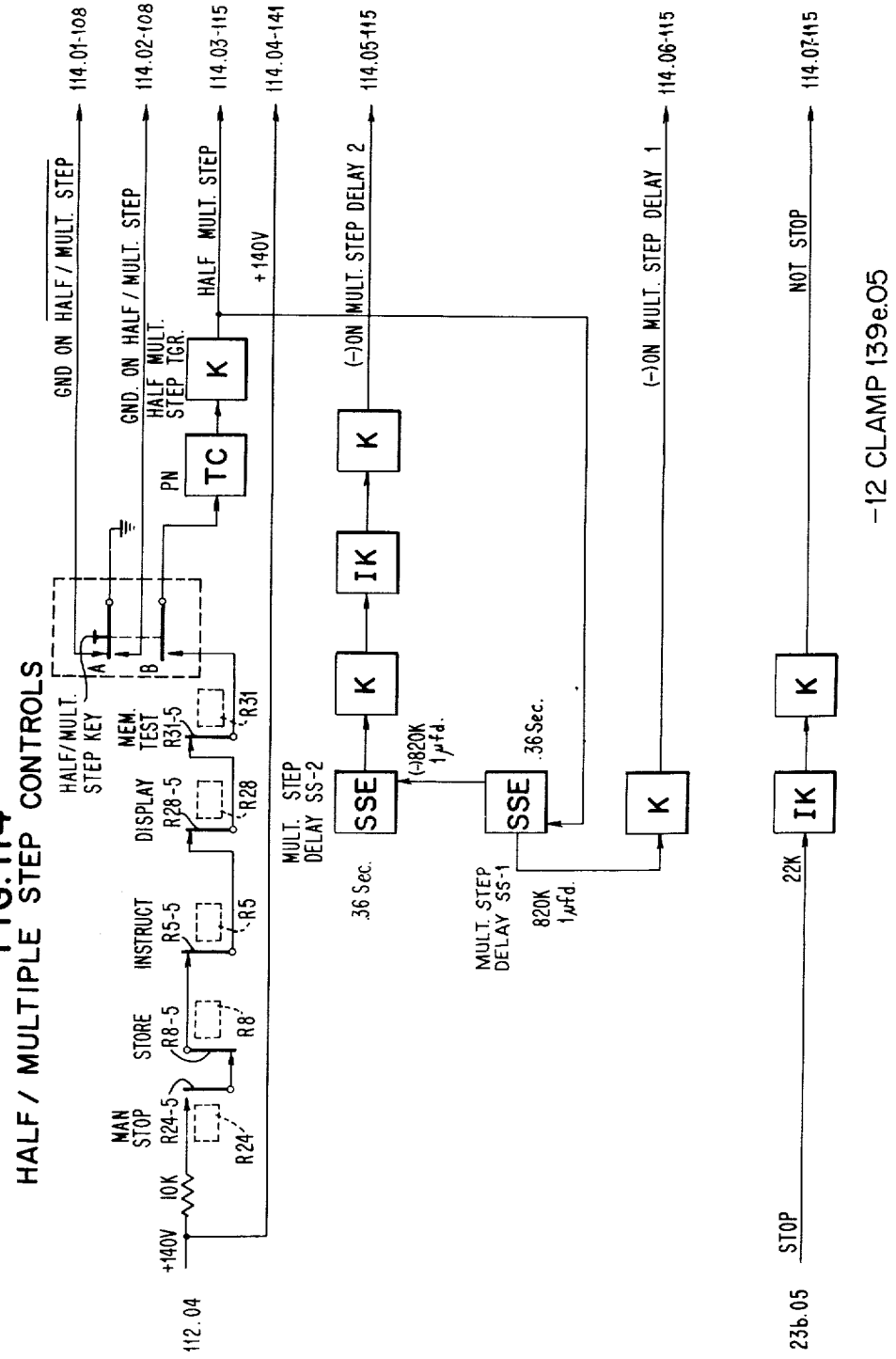
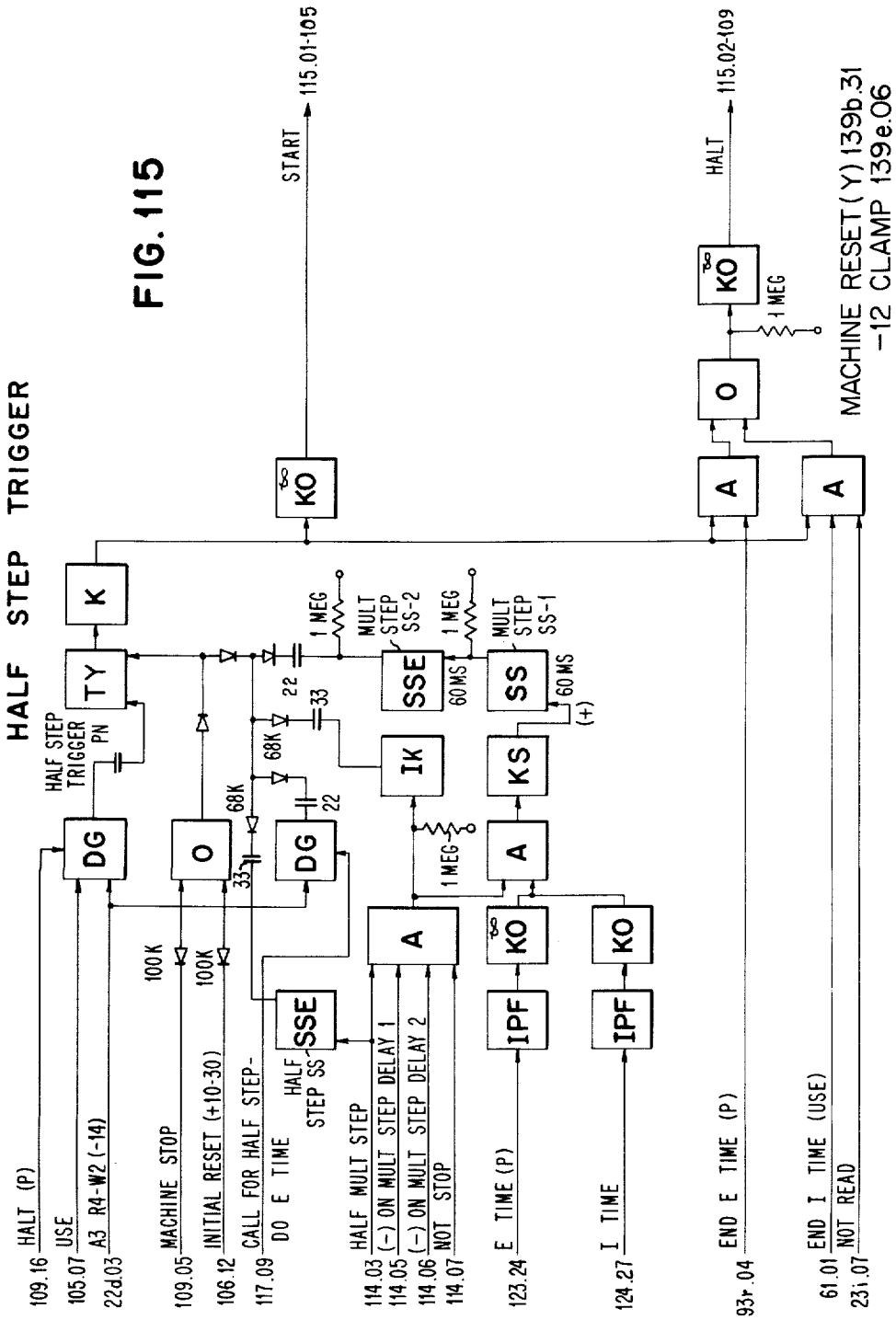
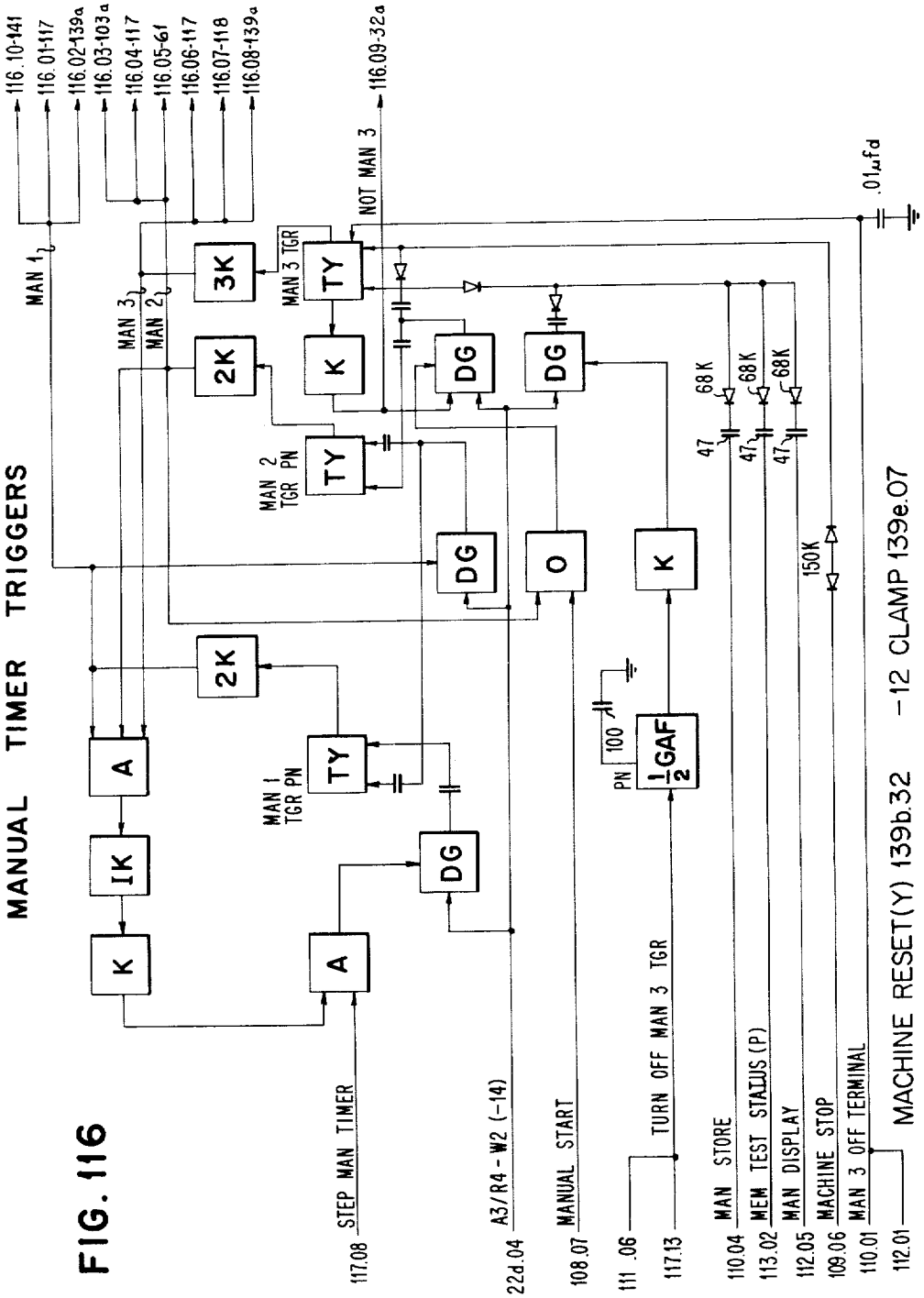


FIG. 115


HALF STEP TRIGGER
START
115.01-105
HALT
115.02-109
MACHINE RESET (Y) 139b.31
-12 CLAMP 139e.06
HALT (P)
109.16
USE
105.07
A3 R4-W2 (-14)
22d.03
MACHINE STOP
109.05
INITIAL RESET (+10-30)
106.12
CALL FOR HALF STEP-DO E TIME
117.09
HALF STEP SS
HALF MULT STEP
114.03
(-) ON MULT STEP DELAY 1
114.05
(-) ON MULT STEP DELAY 2
114.06
NOT STOP
114.07
E TIME (P)
123.24
I TIME
124.27
END E TIME (P)
93r.04
END I TIME (USE)
61.01
NOT READ
23i.07
HALF STEP TRIGGER PN
MULT STEP SS-2
MULT STEP SS-1
1 MEG
100 K
68K
22
33
60 MS
(+)
K
TY
DG
O
SSE
IK
KS
A
KO
IPF


MANUAL TIMER TRIGGERS
116.10-141
116.01-117
116.02-139a
116.03-103a
116.04-117
116.05-61
116.06-117
116.07-118
116.08-139a
116.09-32a
MAN 1
MAN 3
MAN 2
3K
2K
2K
TY
K
DG
DG
DG
O
K
A
IK
K
A
TY
TY
MAN 3 TGR
MAN 2 TGR PN
MAN 1 TGR PN
NOT MAN 3
.01μfd
68K
68K
68K
47
47
47
150K
100
PN
½GAF
117.08 STEP MAN TIMER
22d.04 A3/R4 - W2 (-14)
108.07 MANUAL START
111 .06
117.13 TURN OFF MAN 3 TGR
110.04 MAN STORE
113.02 MEM TEST STATUS (P)
112.05 MAN DISPLAY
109.06 MACHINE STOP
110.01 MAN 3 OFF TERMINAL
112.01 MACHINE RESET(Y) 139b.32 -12 CLAMP 139e.07
FIG. 116

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MAN TIMER EXECUTION CONTROLS

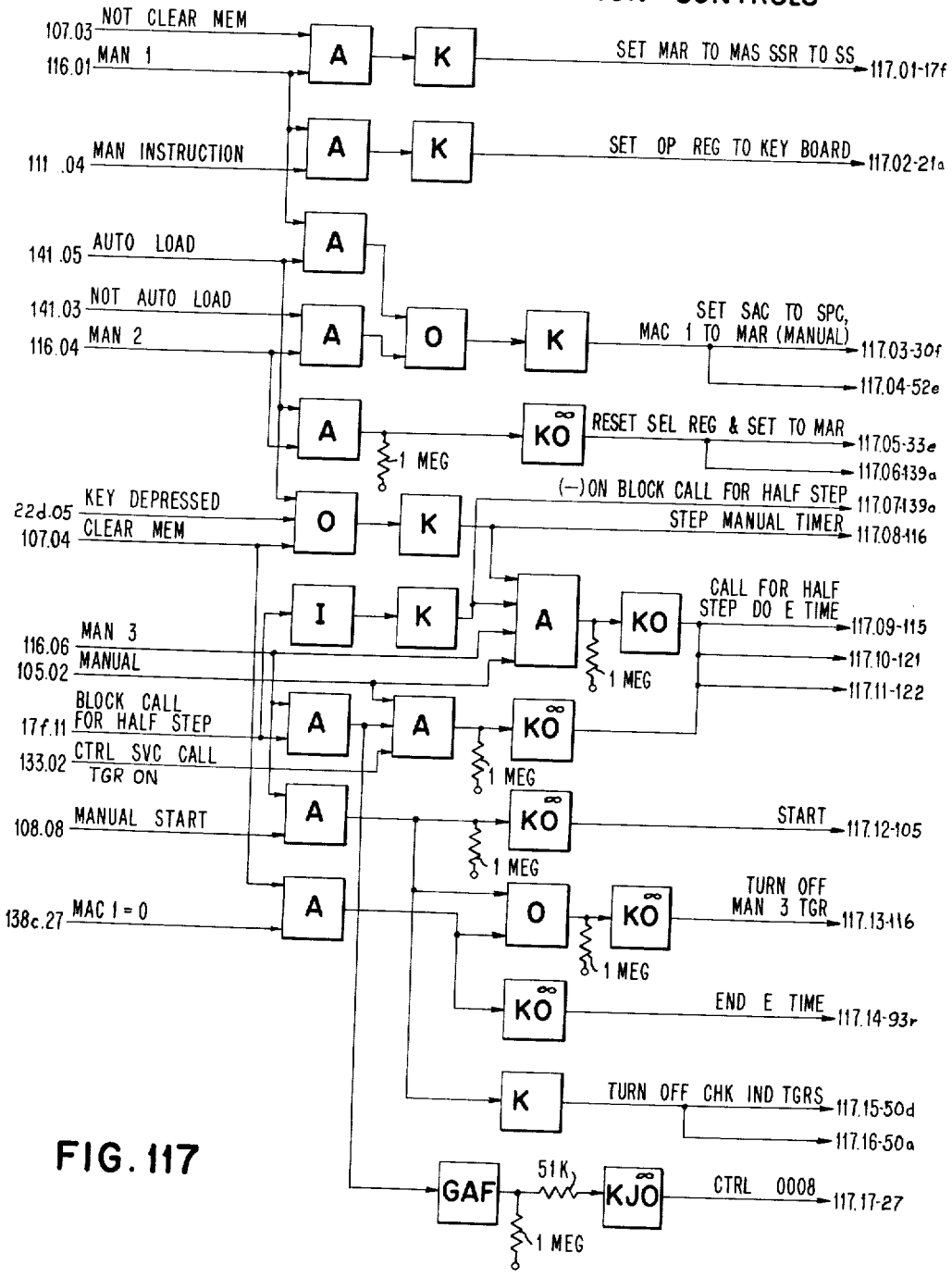


FIG. 117

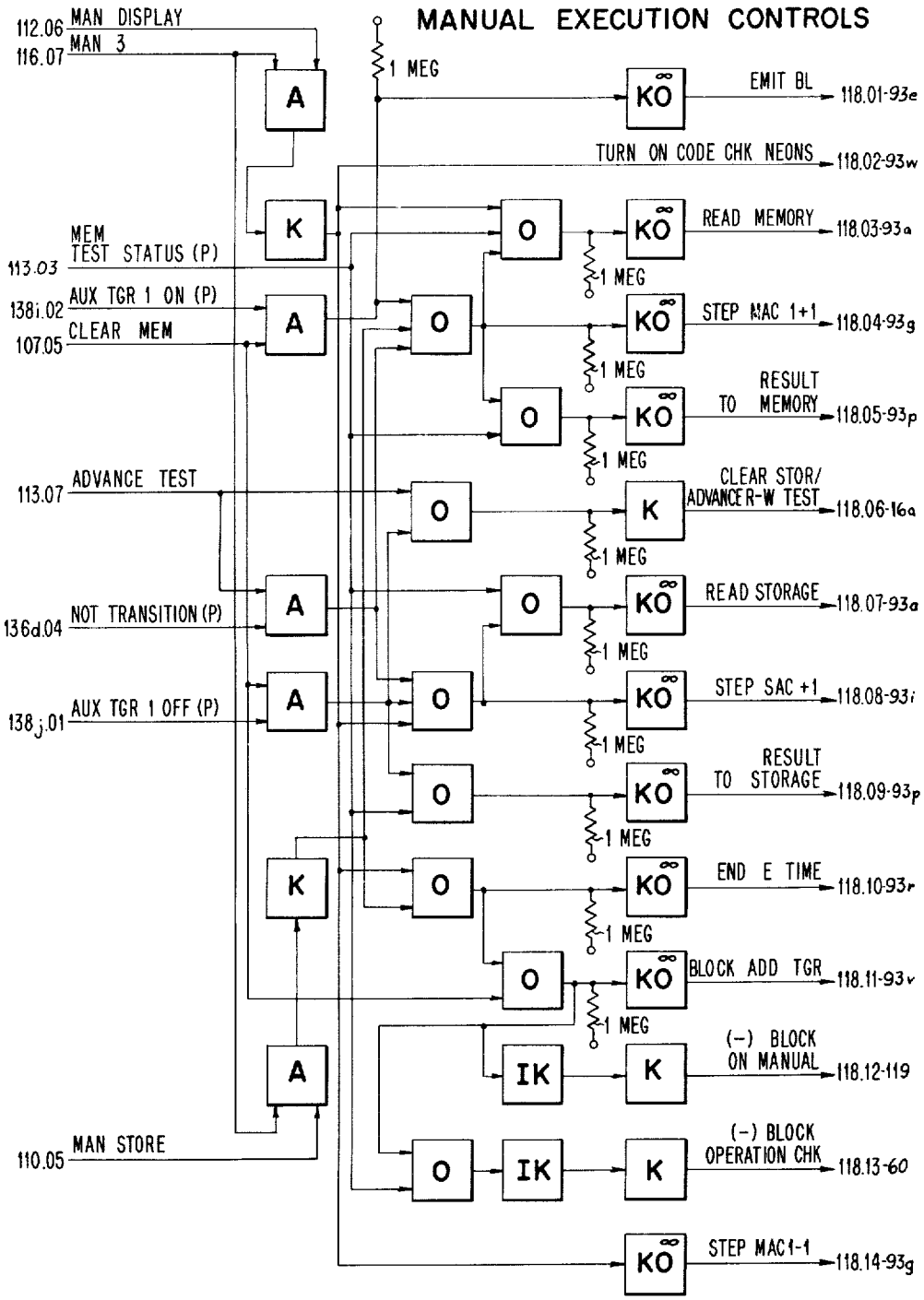

MANUAL EXECUTION CONTROLS
112.06 MAN DISPLAY
116.07 MAN 3
MEM TEST STATUS (P)
113.03
138i.02 AUX TGR 1 ON (P)
107.05 CLEAR MEM
113.07 ADVANCE TEST
136d.04 NOT TRANSITION (P)
138j.01 AUX TGR 1 OFF (P)
110.05 MAN STORE
1 MEG
EMIT BL 118.01-93e
TURN ON CODE CHK NEONS 118.02-93w
READ MEMORY 118.03-93a
STEP MAC 1+1 118.04-93g
RESULT TO MEMORY 118.05-93p
CLEAR STOR/ ADVANCE R-W TEST 118.06-16a
READ STORAGE 118.07-93a
STEP SAC +1 118.08-93i
RESULT TO STORAGE 118.09-93p
END E TIME 118.10-93r
BLOCK ADD TGR 118.11-93v
(-) BLOCK ON MANUAL 118.12-119
(-) BLOCK OPERATION CHK 118.13-60
STEP MAC1-1 118.14-93g

FIG. 118

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OVERLAP MODE CONTROL

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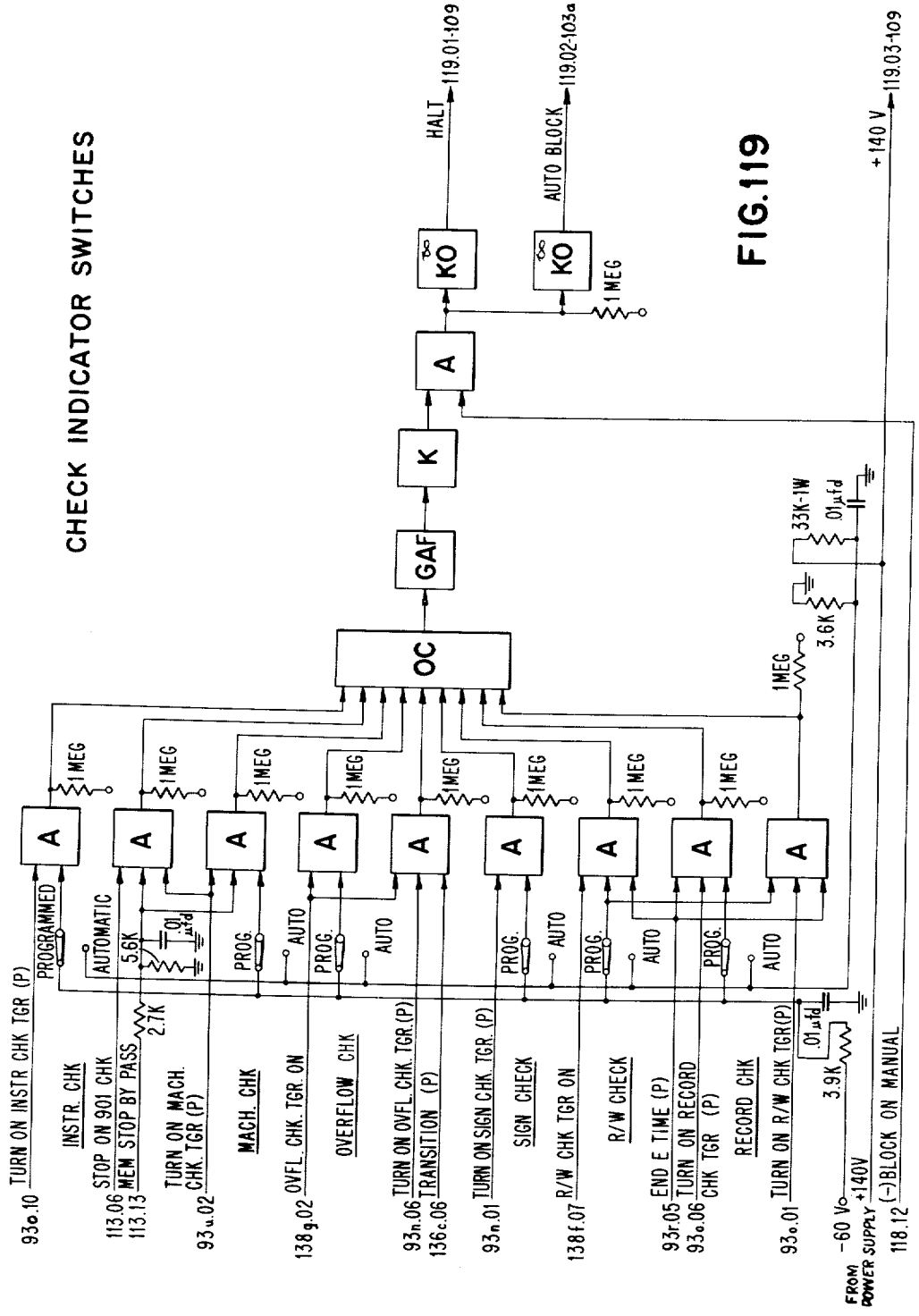
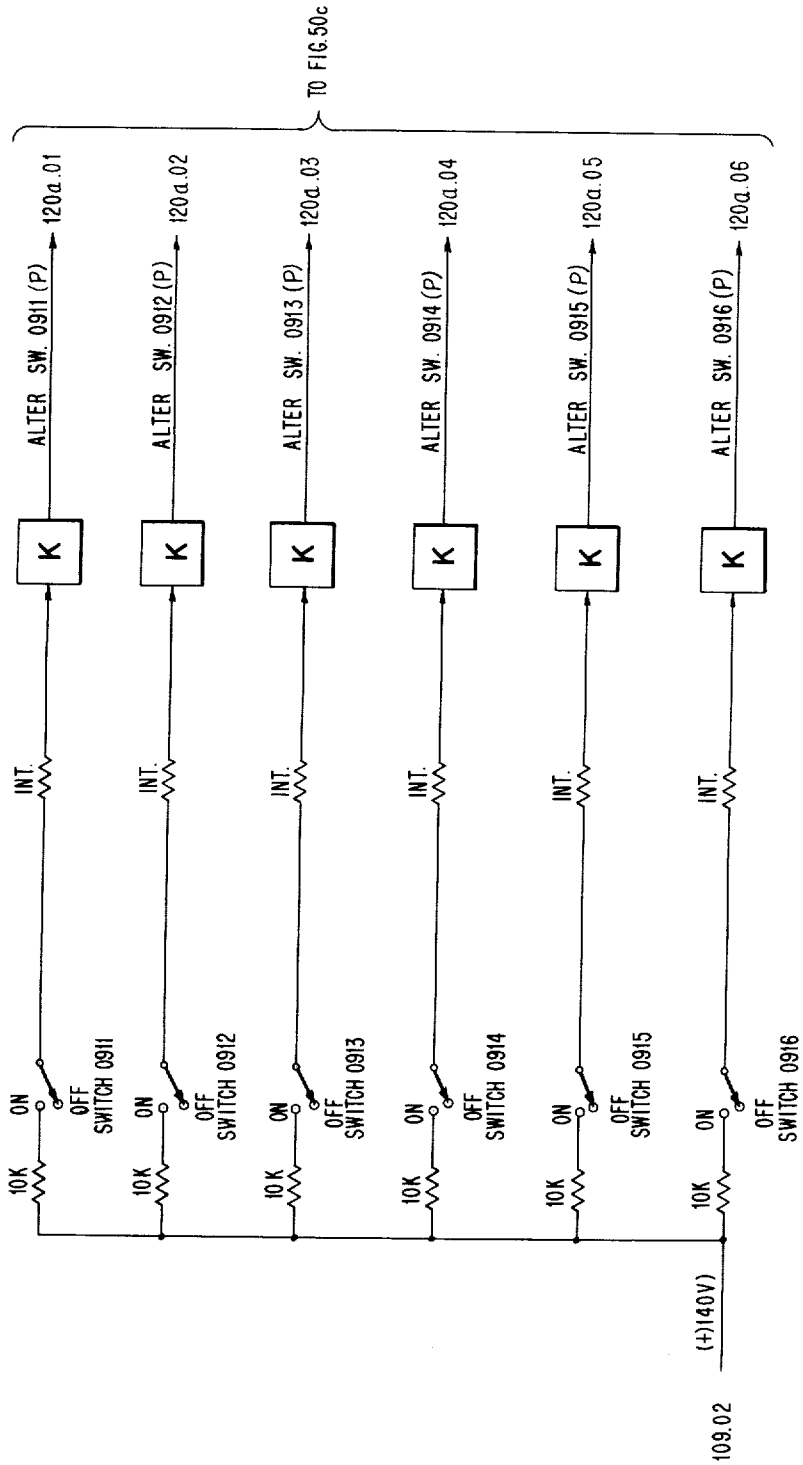


FIG.119

FIG. 120a
ALTERATION SWITCHES



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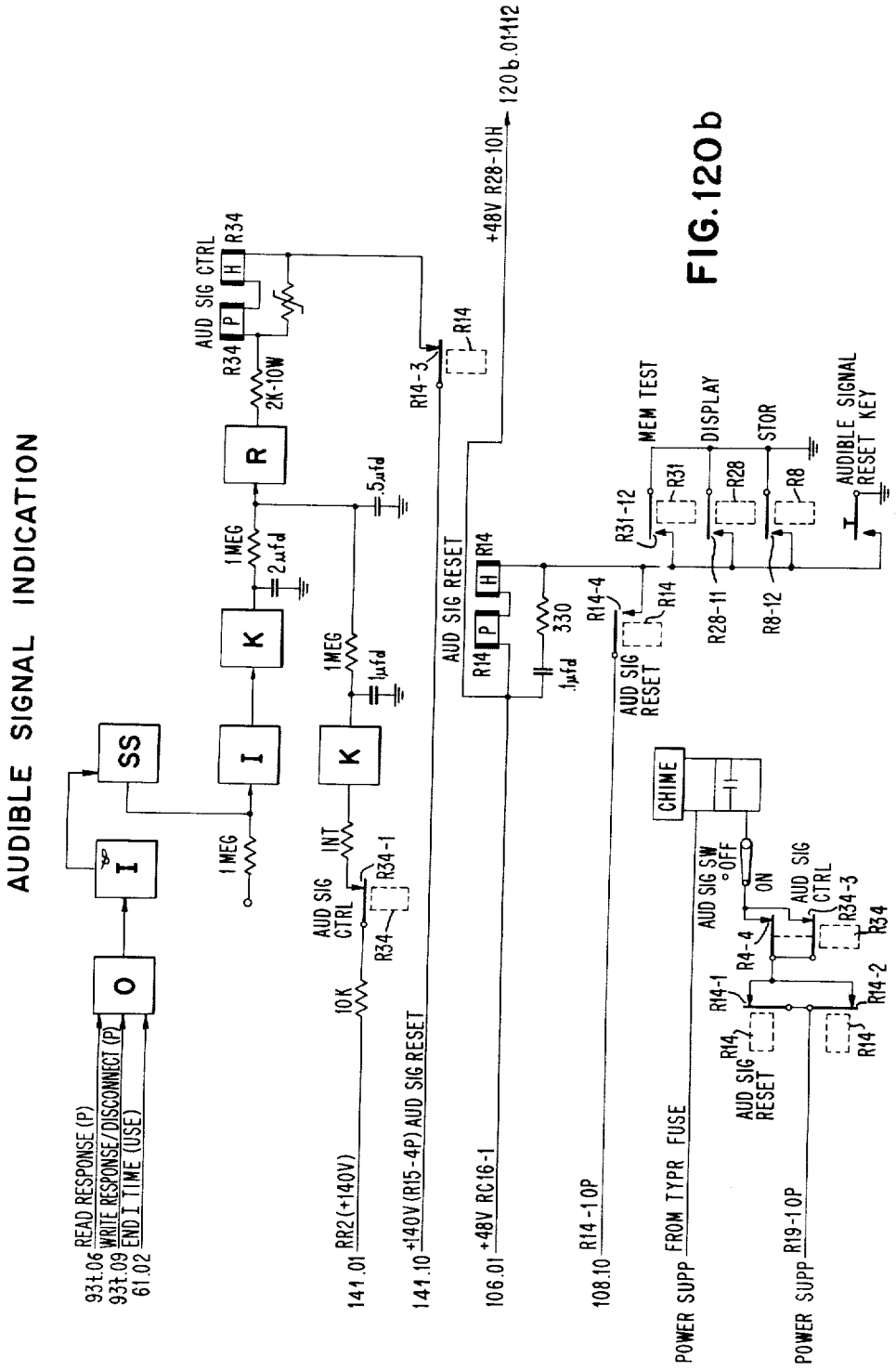


FIG. 120b

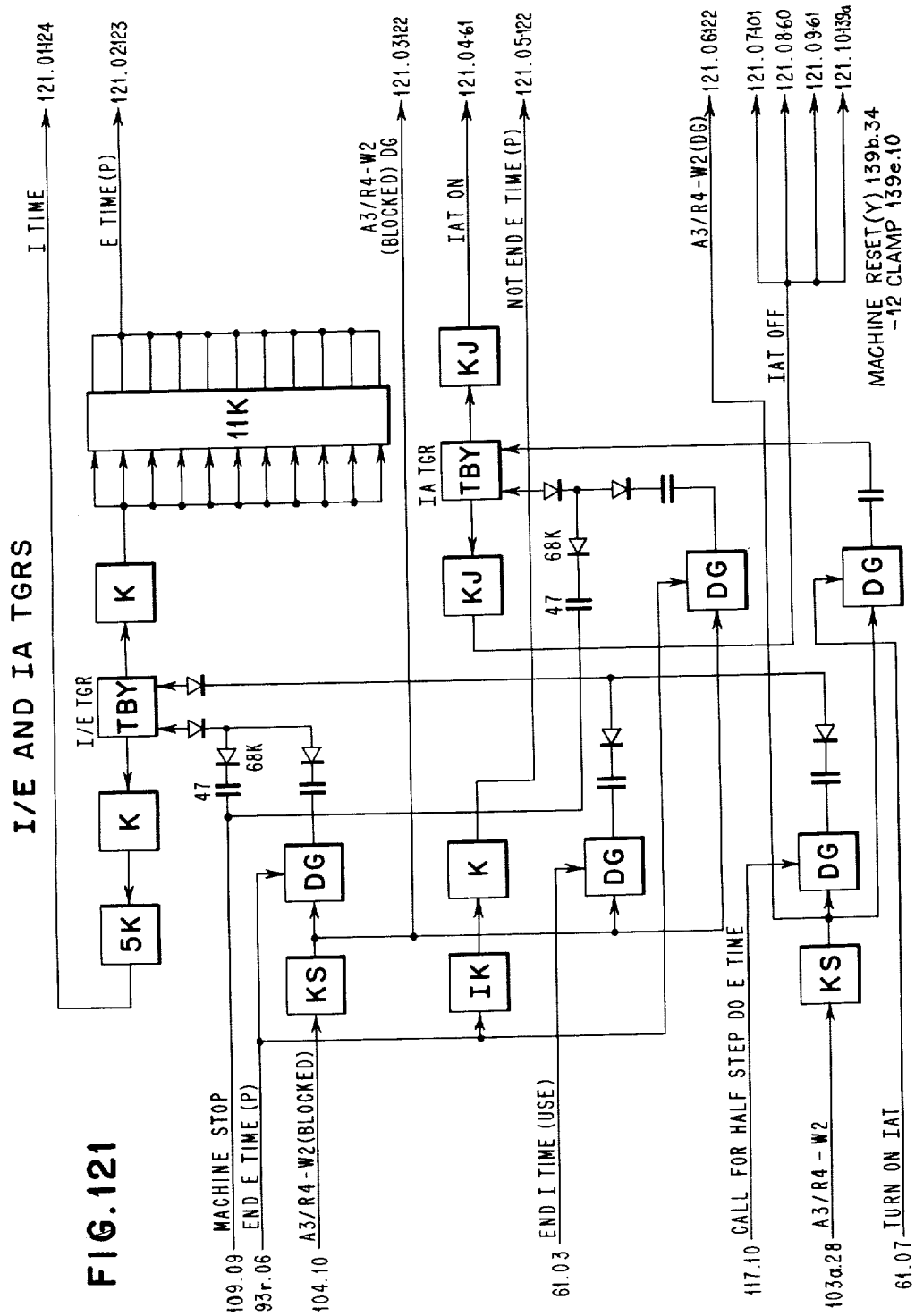

I/E AND IA TGRS
I TIME 121.01124
E TIME(P) 121.02123
A3/R4-W2 (BLOCKED) DG 121.03122
IAT ON 121.04461
NOT END E TIME(P) 121.05122
A3/R4-W2(DG) 121.06122
121.07401
121.08060
121.09461
121.10139a
IAT OFF
MACHINE RESET(Y) 139b.34
-12 CLAMP 139e.10
11K
K
TBY
I/E TGR
5K
47
68K
DG
KS
IK
KJ
IA TGR
MACHINE STOP 109.09
END E TIME (P) 93r.06
A3/R4-W2(BLOCKED) 104.10
END I TIME (USE) 61.03
CALL FOR HALF STEP DO E TIME 117.10
A3/R4 - W2 103a.28
TURN ON IAT 61.07

FIG. 121

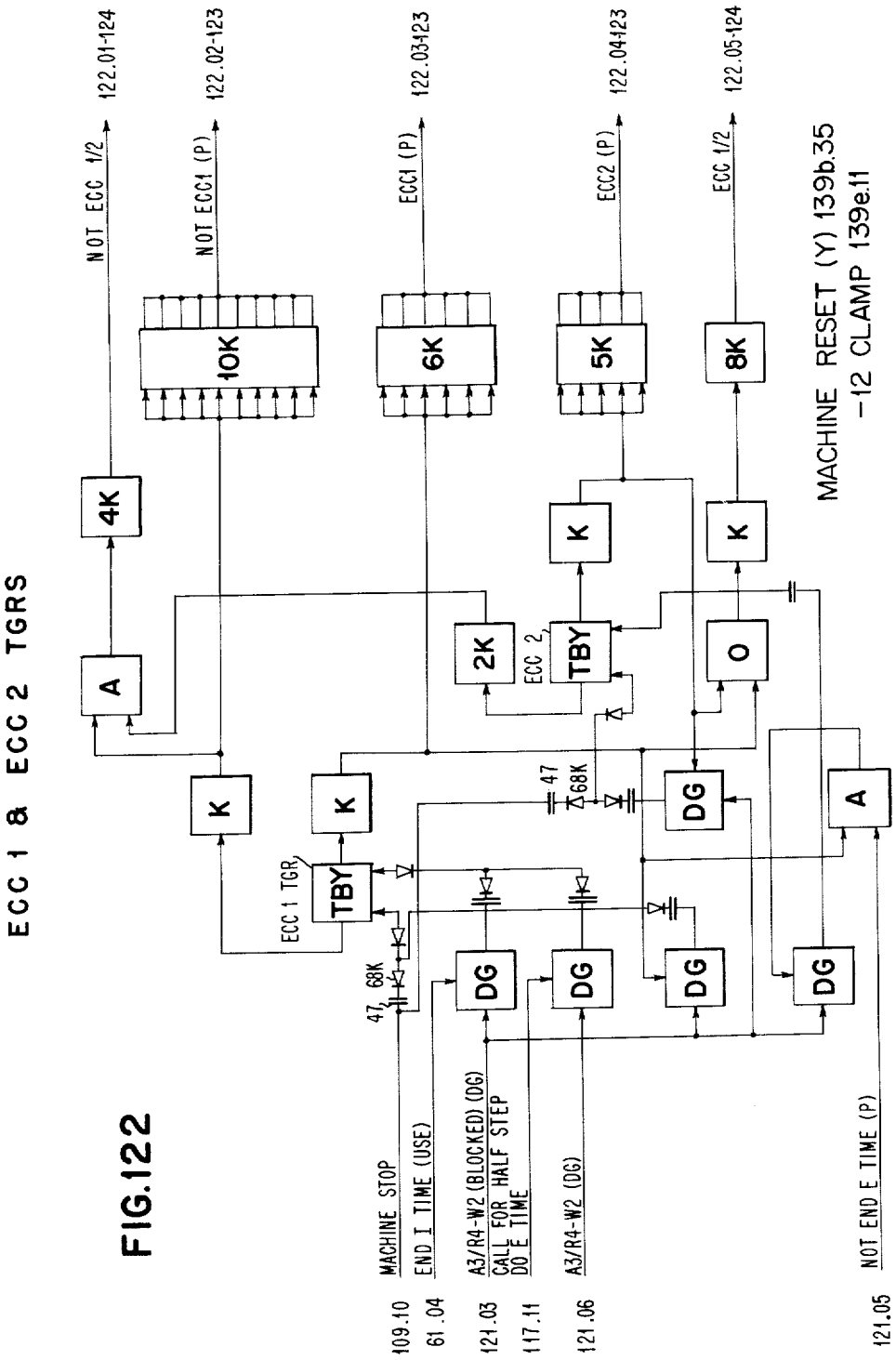

ECC 1 & ECC 2 TGRS
122.01-124
NOT ECC 1/2
122.02-123
NOT ECC1 (P)
122.03123
ECC1 (P)
122.04123
ECC2 (P)
122.05-124
ECC 1/2
10K
6K
5K
8K
4K
A
K
2K
ECC 2
TBY
O
47
68K
DG
ECC 1 TGR
MACHINE RESET (Y) 139b.35
-12 CLAMP 139e.11
109.10 MACHINE STOP
61.04 END I TIME (USE)
121.03 A3/R4-W2 (BLOCKED) (DG)
CALL FOR HALF STEP
DO E TIME
117.11
121.06 A3/R4-W2 (DG)
121.05 NOT END E TIME (P)

FIG.122

FIG. 123

I/E TIMER OUTPUTS

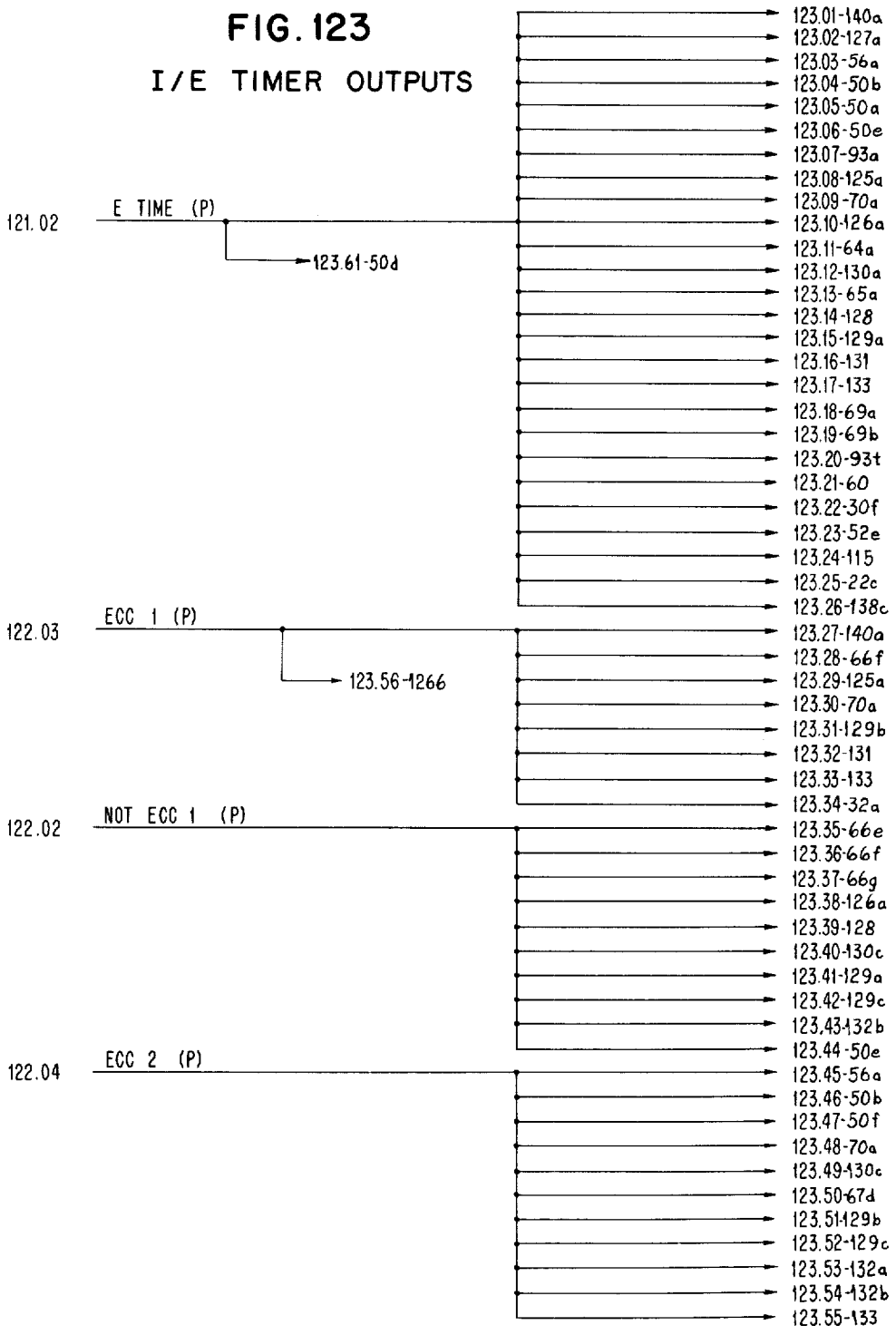
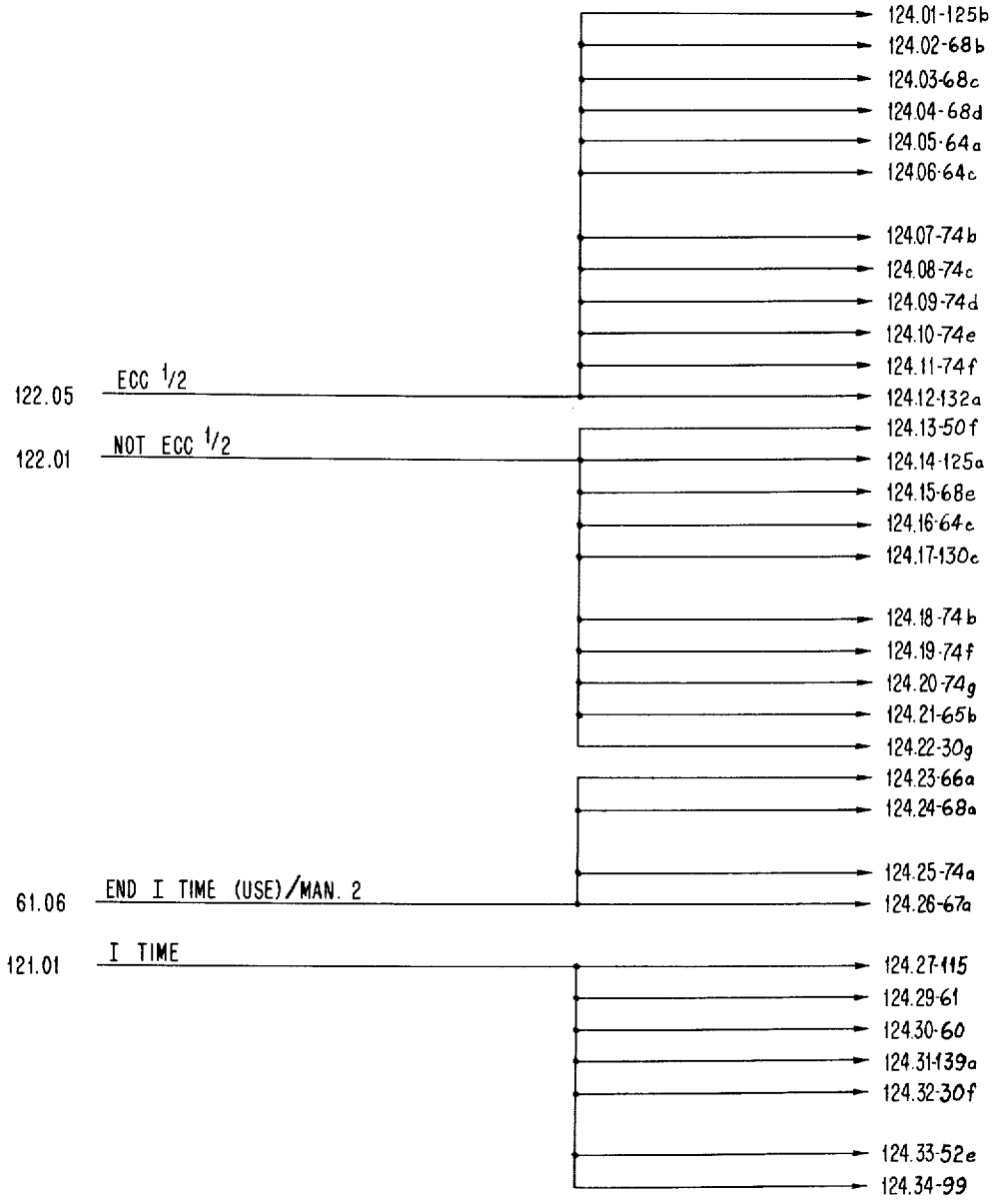


FIG. 124

I/E TIMER OUTPUTS



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LOAD, UNLOAD & STORE ROUTING CONTROLS

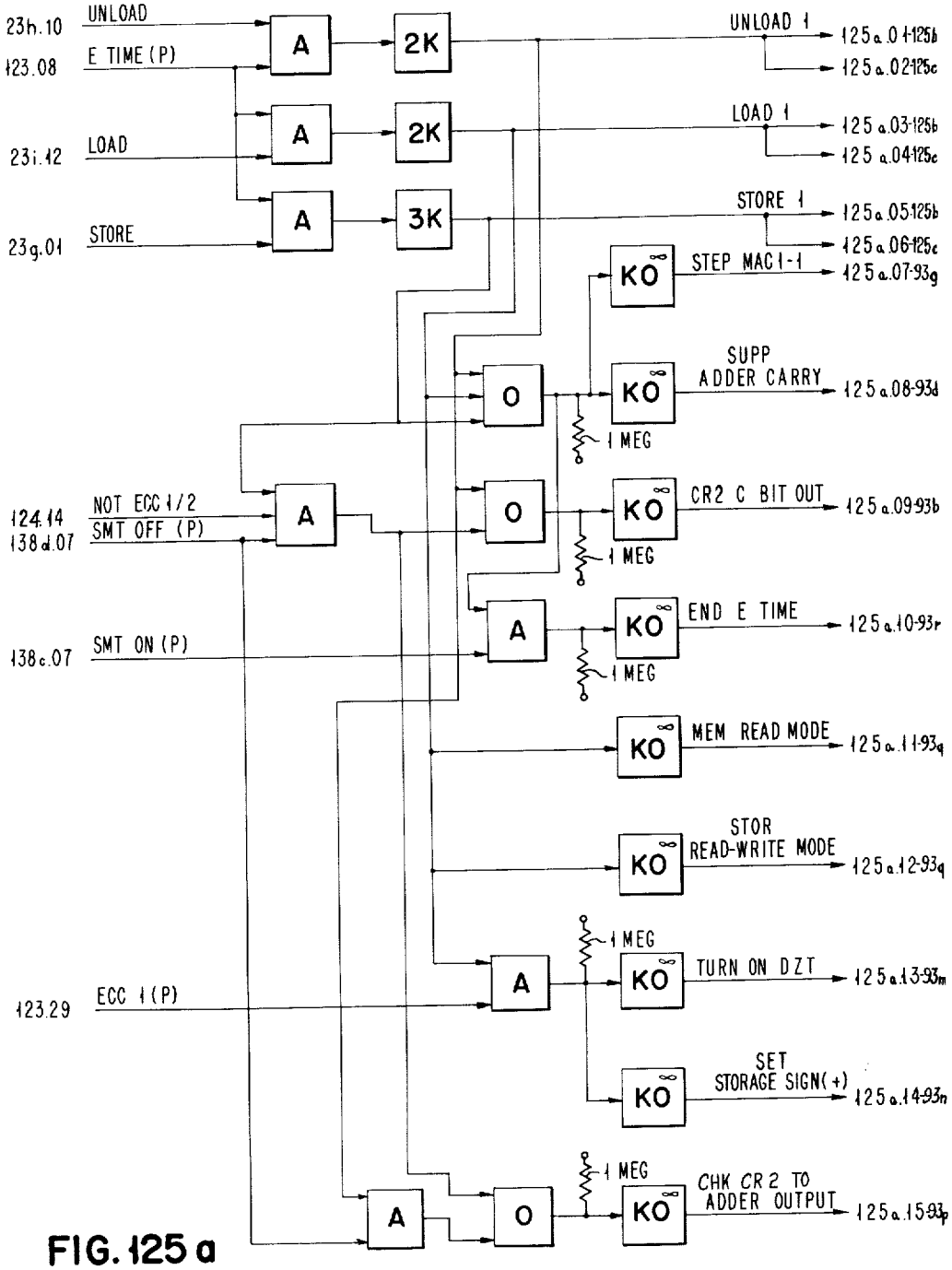


FIG. 125a

LOAD, UNLOAD & STORE ROUTING CONTROLS

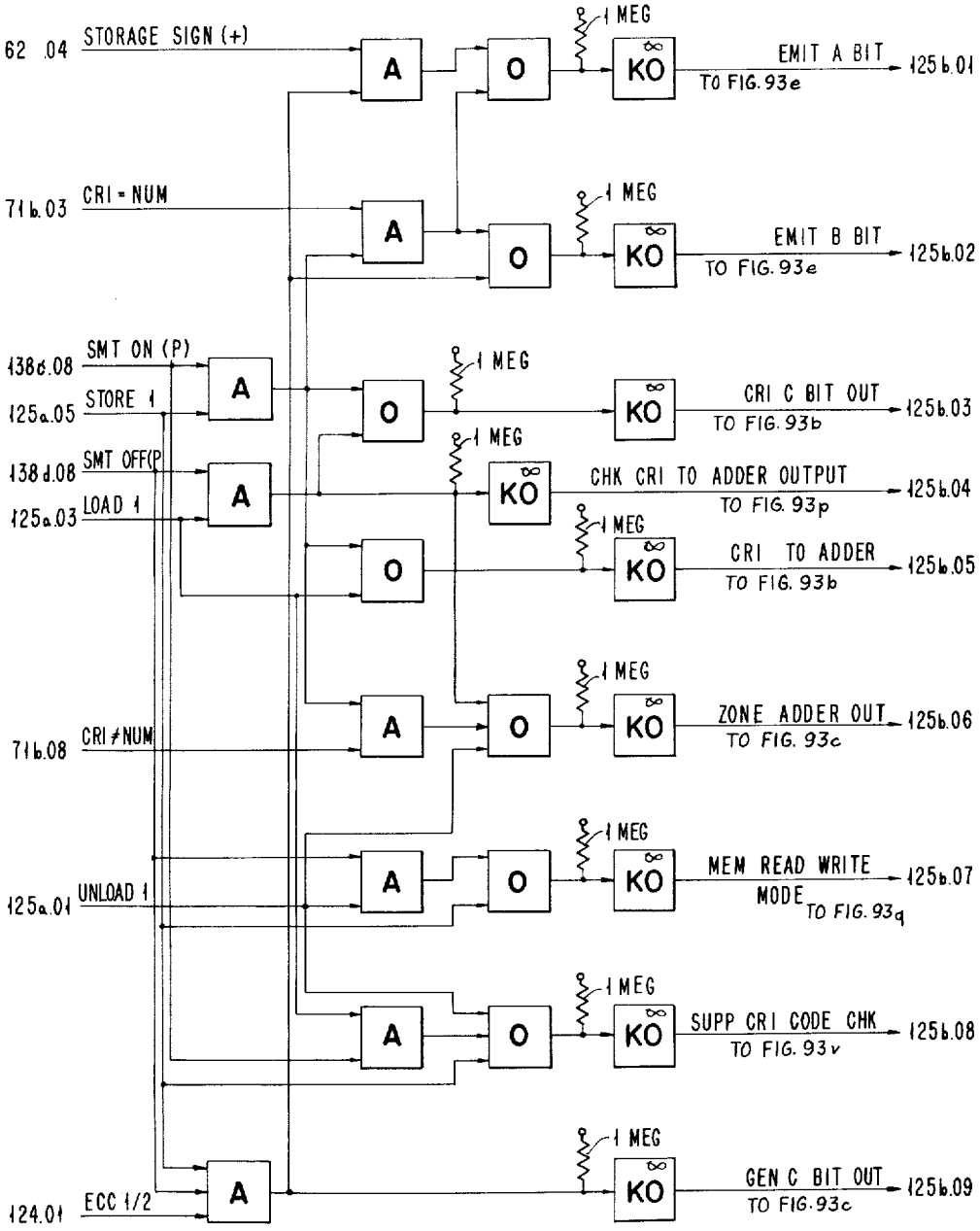


FIG. 125 b

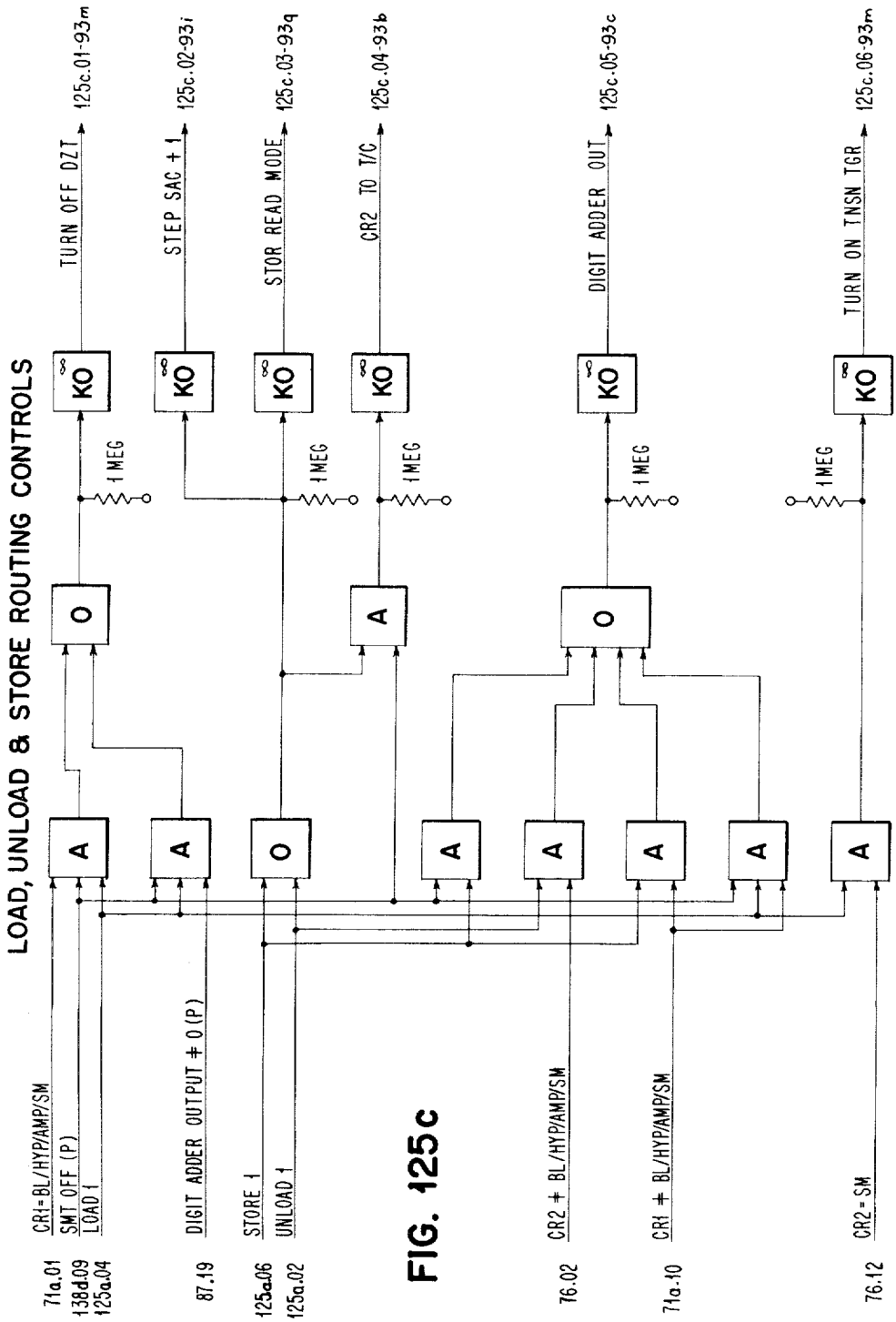

LOAD, UNLOAD & STORE ROUTING CONTROLS
TURN OFF DZT
125c.01-93m
STEP SAC + 1
125c.02-93i
STOR READ MODE
125c.03-93q
CR2 TO T/C
125c.04-93b
DIGIT ADDER OUT
125c.05-93c
TURN ON TNSN TGR
125c.06-93m
KO
1 MEG
O
A
CR1=BL/HYP/AMP/SM
SMT OFF (P)
LOAD 1
DIGIT ADDER OUTPUT ≠ 0 (P)
STORE 1
UNLOAD 1
CR2 ≠ BL/HYP/AMP/SM
CR1 ≠ BL/HYP/AMP/SM
CR2=SM
71a.01
138d.09
125a.04
87.19
125a.06
125a.02
76.02
71a.10
76.12

FIG. 125c

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FIG. 126a

STORE FOR PRINT ROUTING CONTROLS

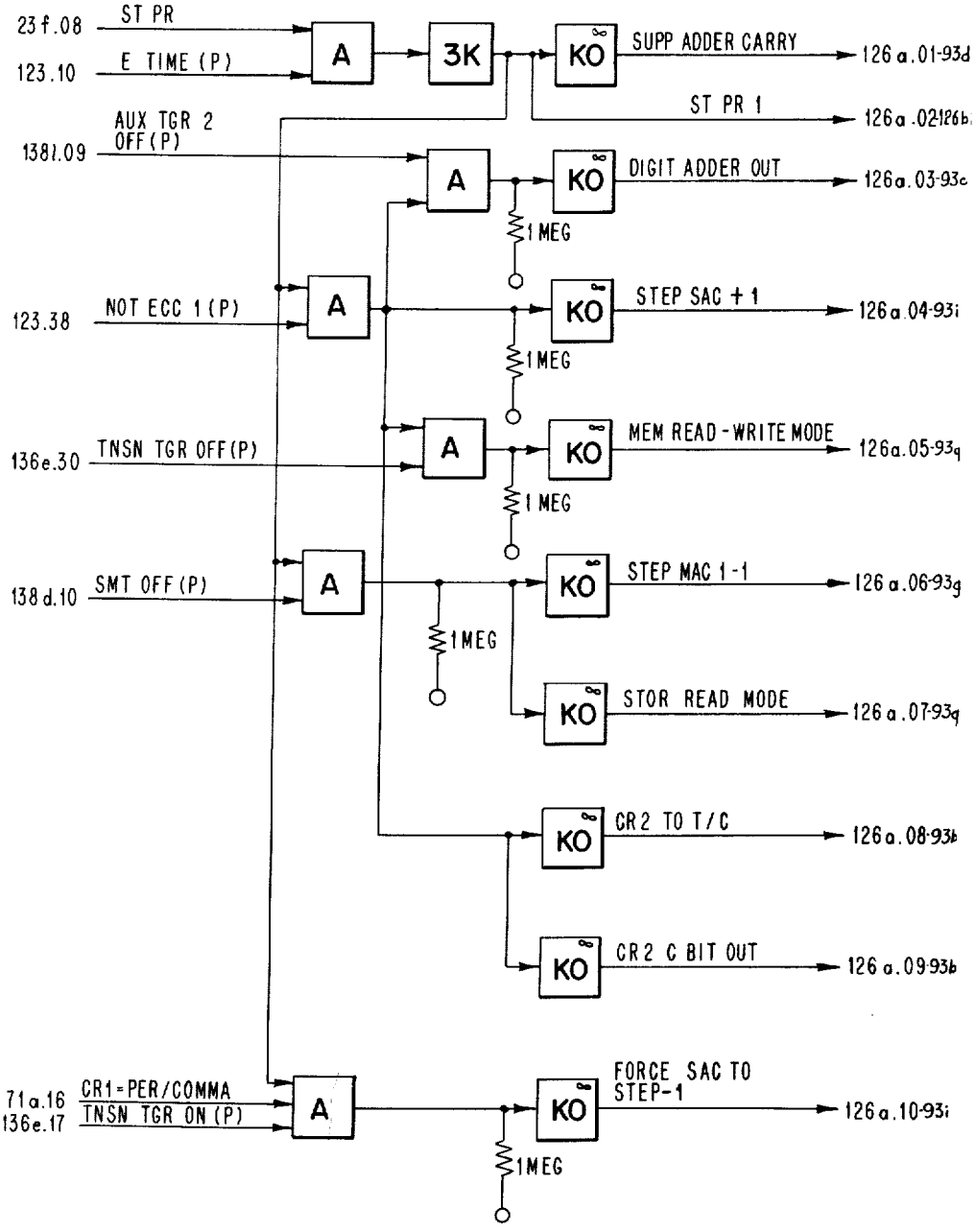
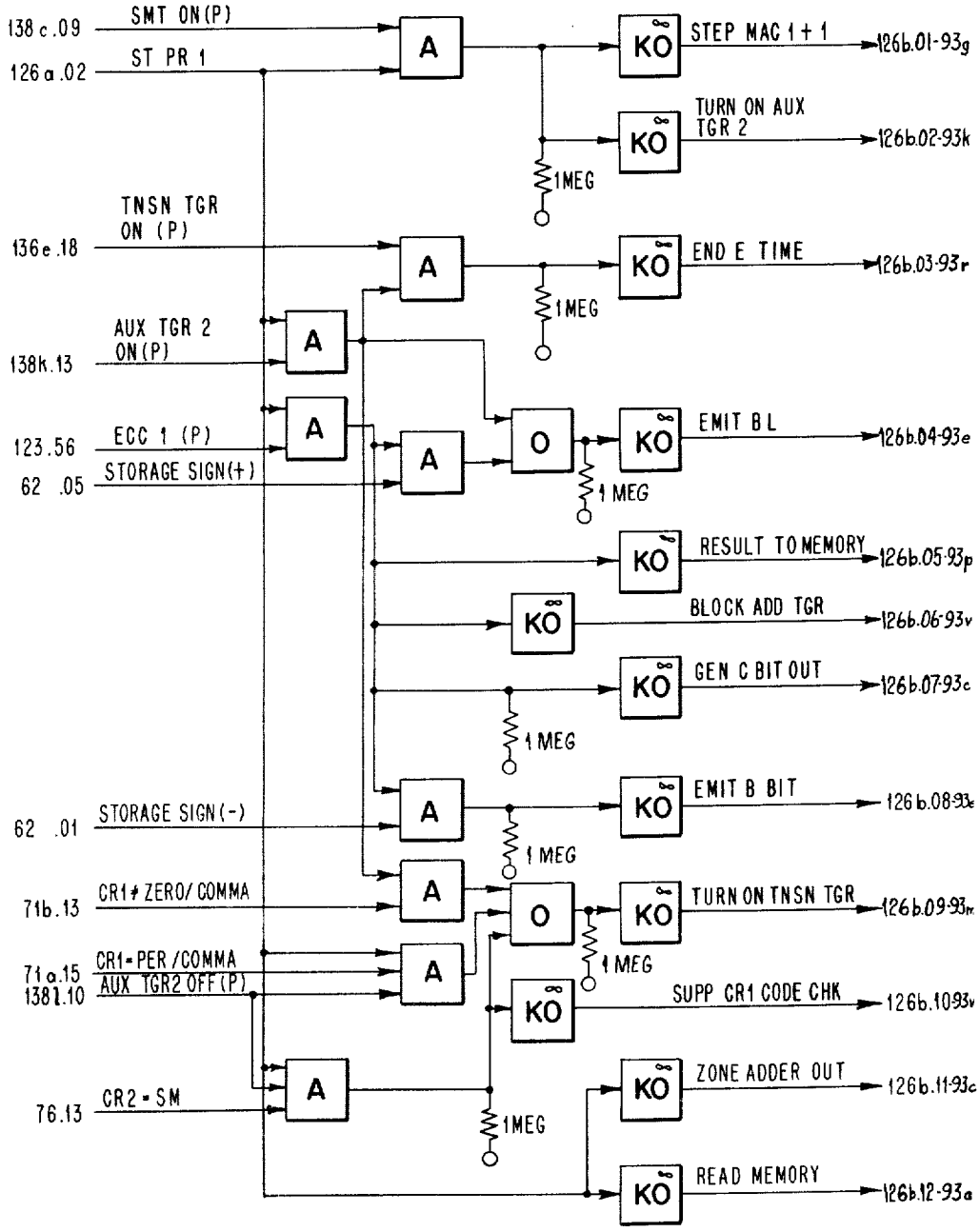


FIG. 126b

STORE FOR PRINT ROUTING CONTROLS



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OVERLAP MODE CONTROL
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FIG. 127 a

TSMT / SEND ROUTING CONTROLS

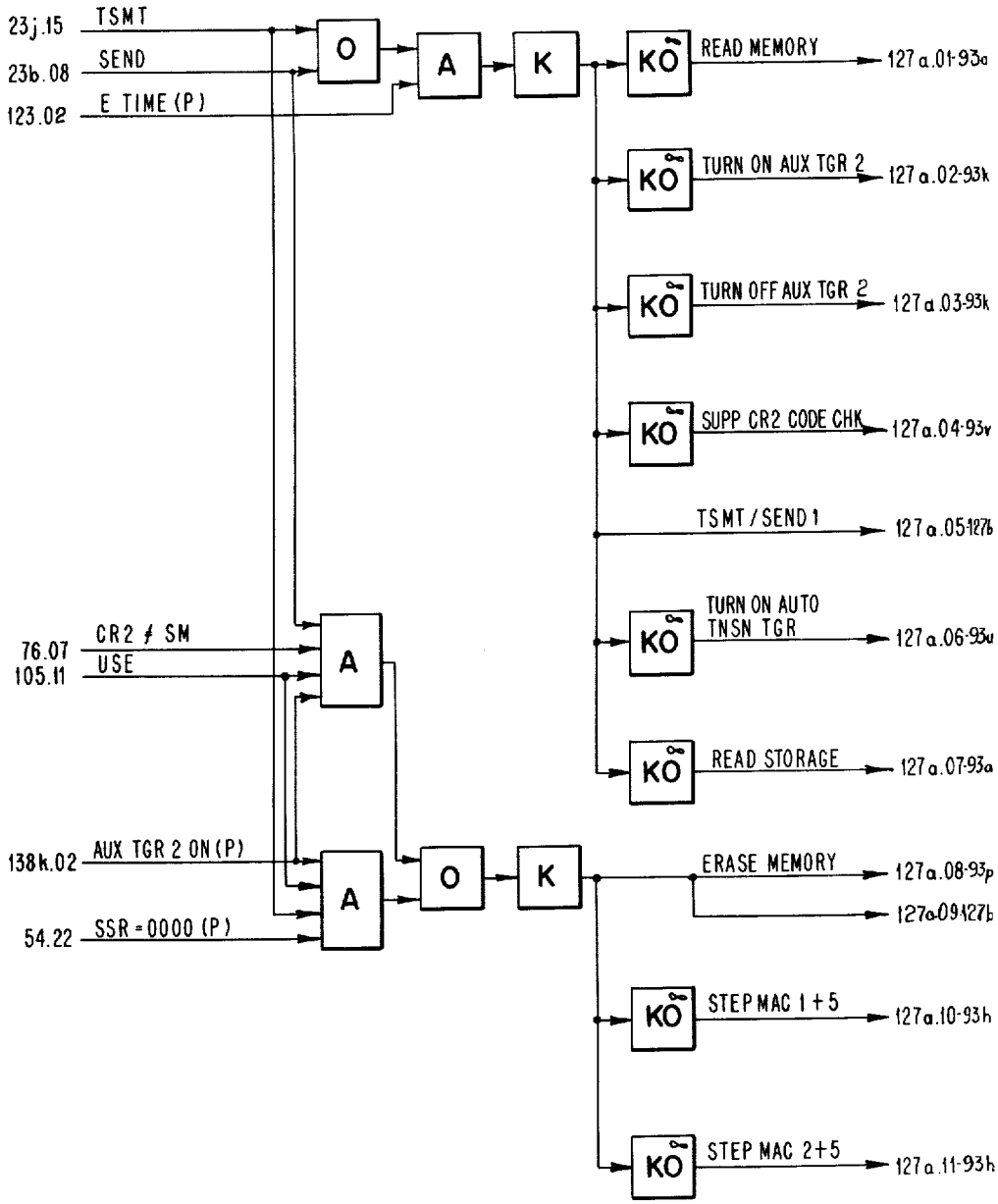


FIG. 127b TSMT / SEND ROUTING CONTROLS

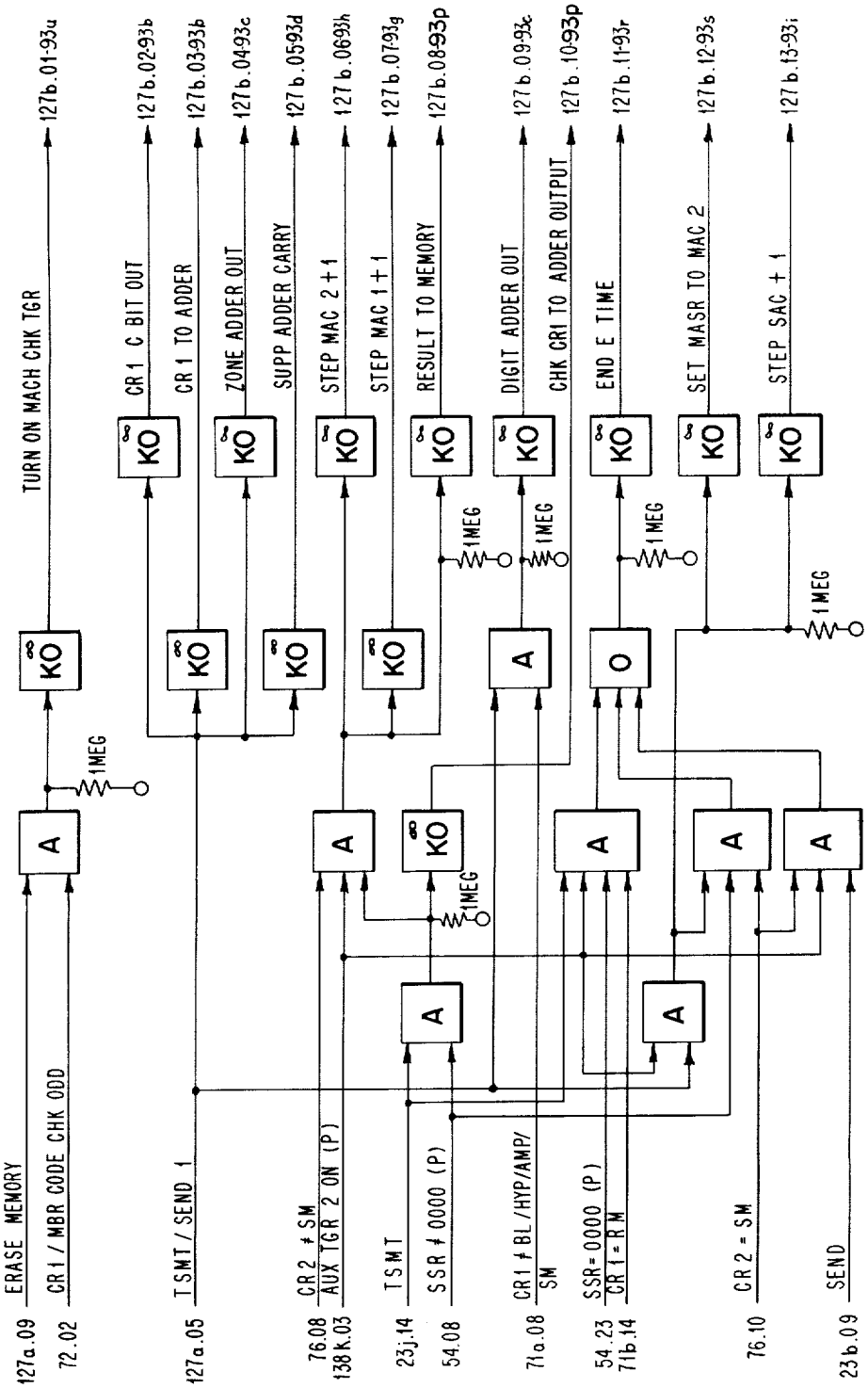


FIG. 128

BLANK MEMORY

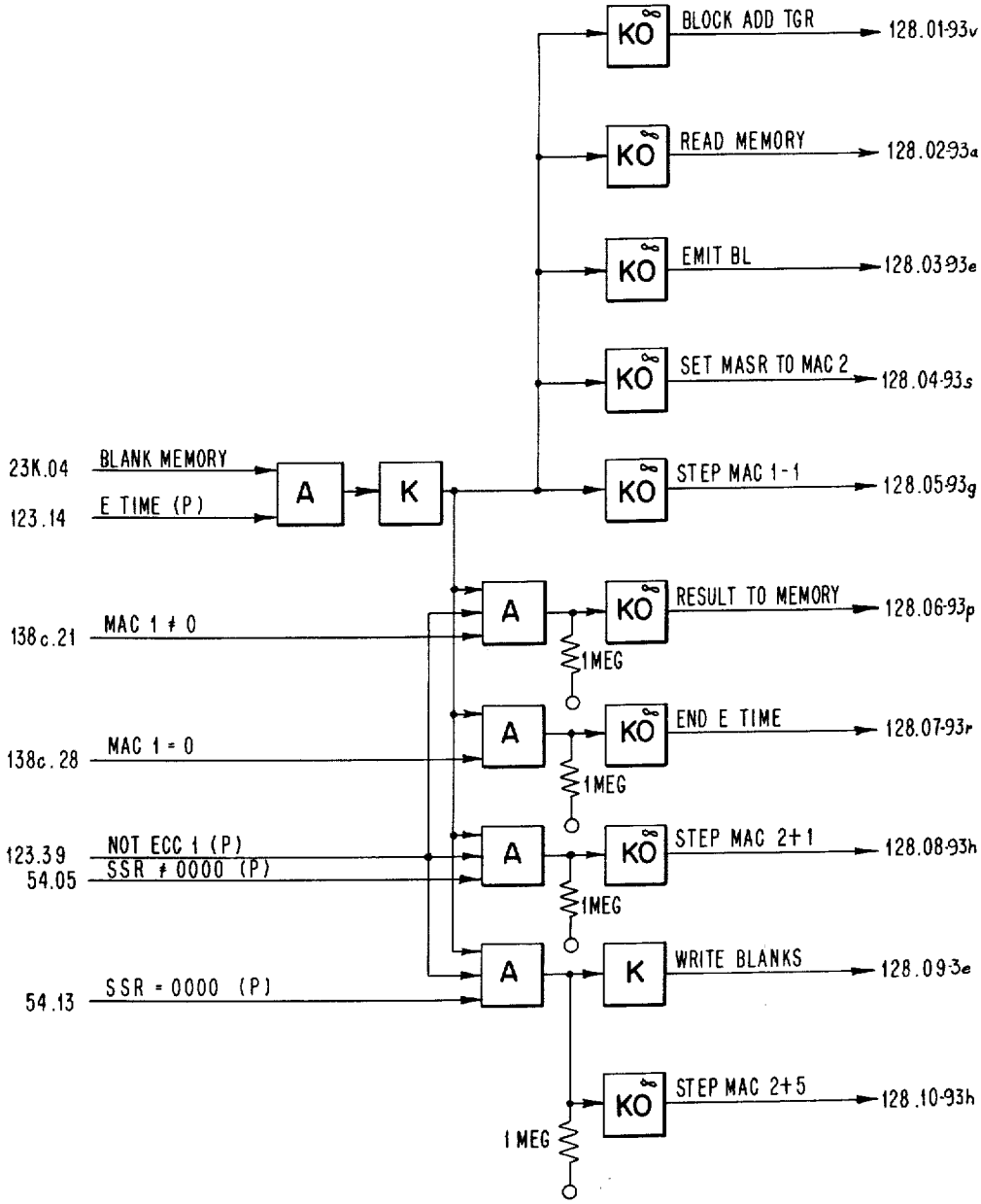
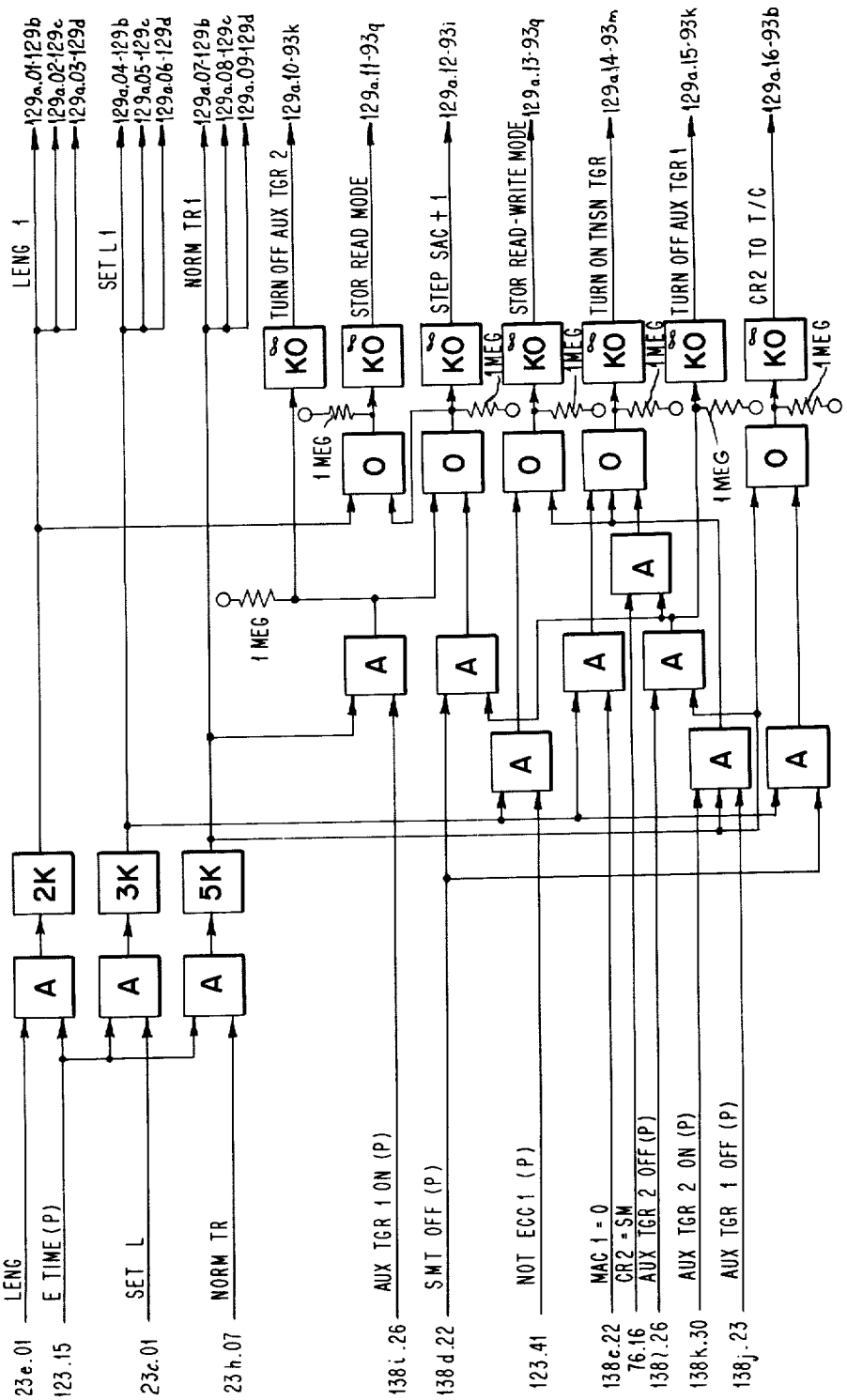


FIG. 129a


SET LEFT, LENG & NORM TR ROUTING CONTROLS
LENG 1
SET L 1
NORM TR 1
TURN OFF AUX TGR 2
STOR READ MODE
STEP SAC + 1
STOR READ-WRITE MODE
TURN ON TNSN TGR
TURN OFF AUX TGR 1
CR2 TO T/C
129a.01-129b
129a.02-129c
129a.03-129d
129a.04-129b
129a.05-129c
129a.06-129d
129a.07-129b
129a.08-129c
129a.09-129d
129a.10-93k
129a.11-93q
129a.12-93i
129a.13-93q
129a.14-93m
129a.15-93k
129a.16-93b
2K
3K
5K
A
O
KO
1 MEG
LENG
E TIME (P)
SET L
NORM TR
AUX TGR 1 ON (P)
SMT OFF (P)
NOT ECC 1 (P)
MAC 1 = 0
CR2 = SM
AUX TGR 2 OFF (P)
AUX TGR 2 ON (P)
AUX TGR 1 OFF (P)
23e.01
123.15
23c.01
23h.07
138i.26
138d.22
123.41
138c.22
76.16
138l.26
138k.30
138j.23

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FIG. 129b

SET LEFT, LENG & NORM TR ROUTING CONTROLS

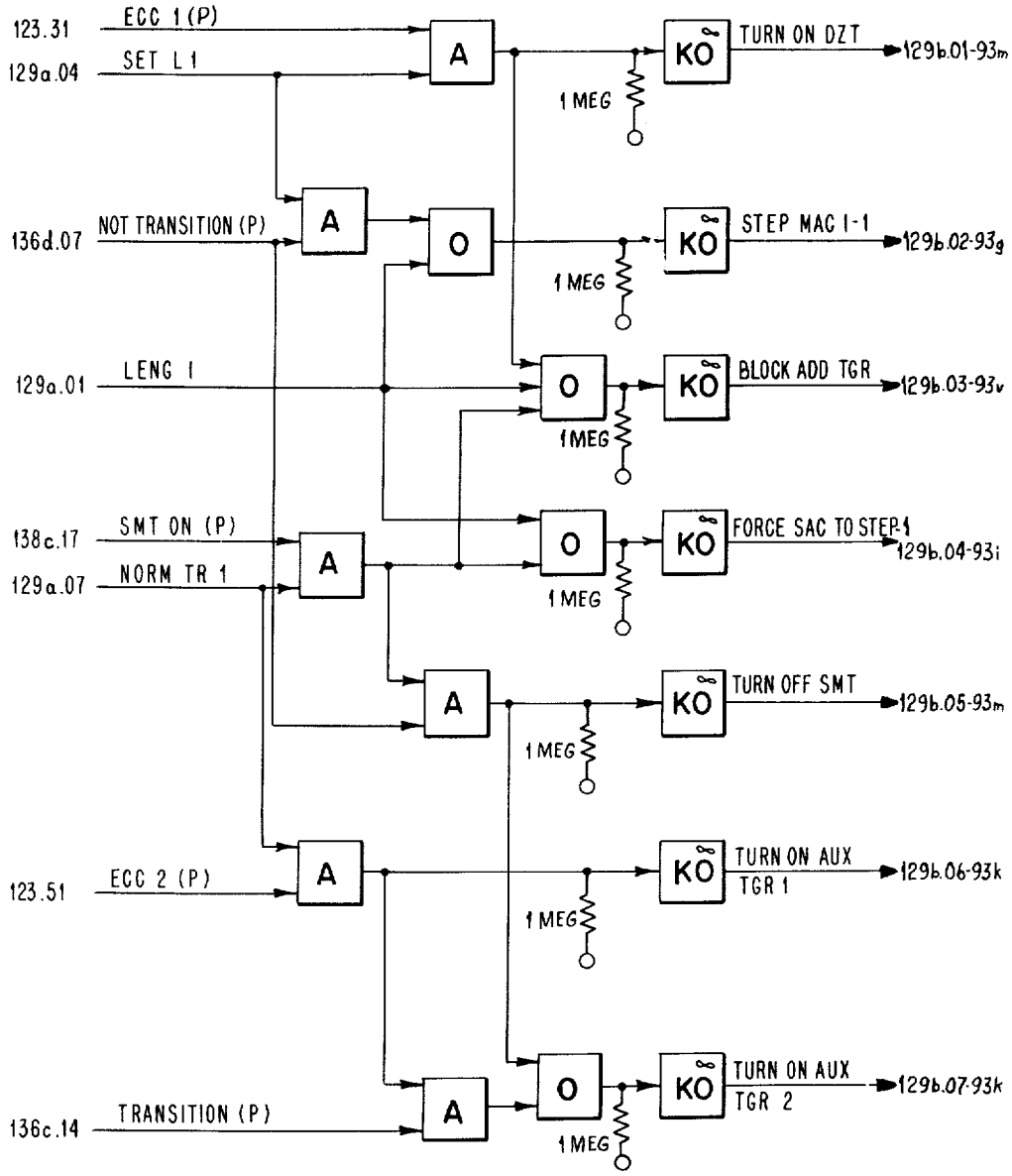


FIG. 129c

SET LEFT, LENG & NORM TR ROUTING CONTROLS

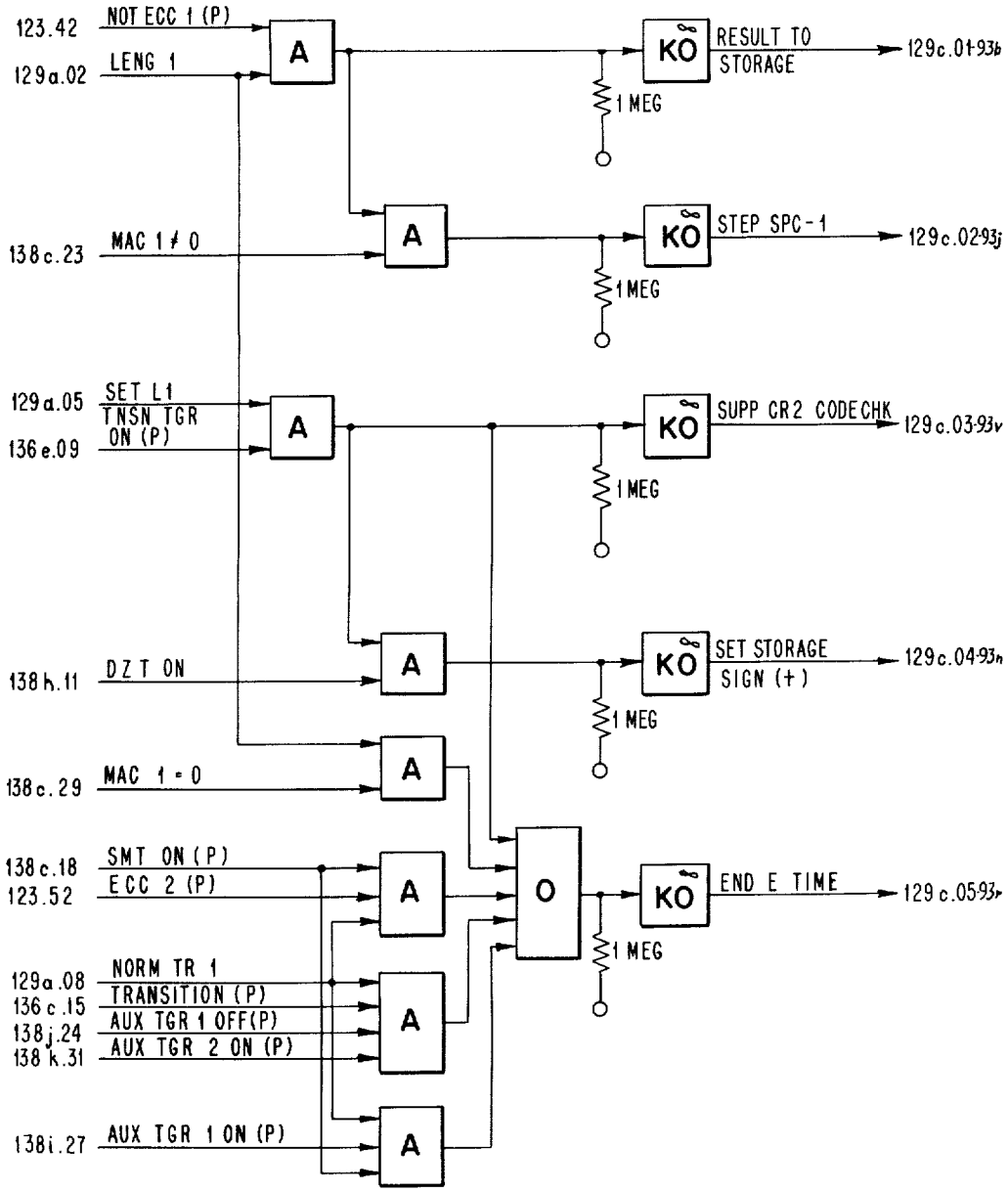
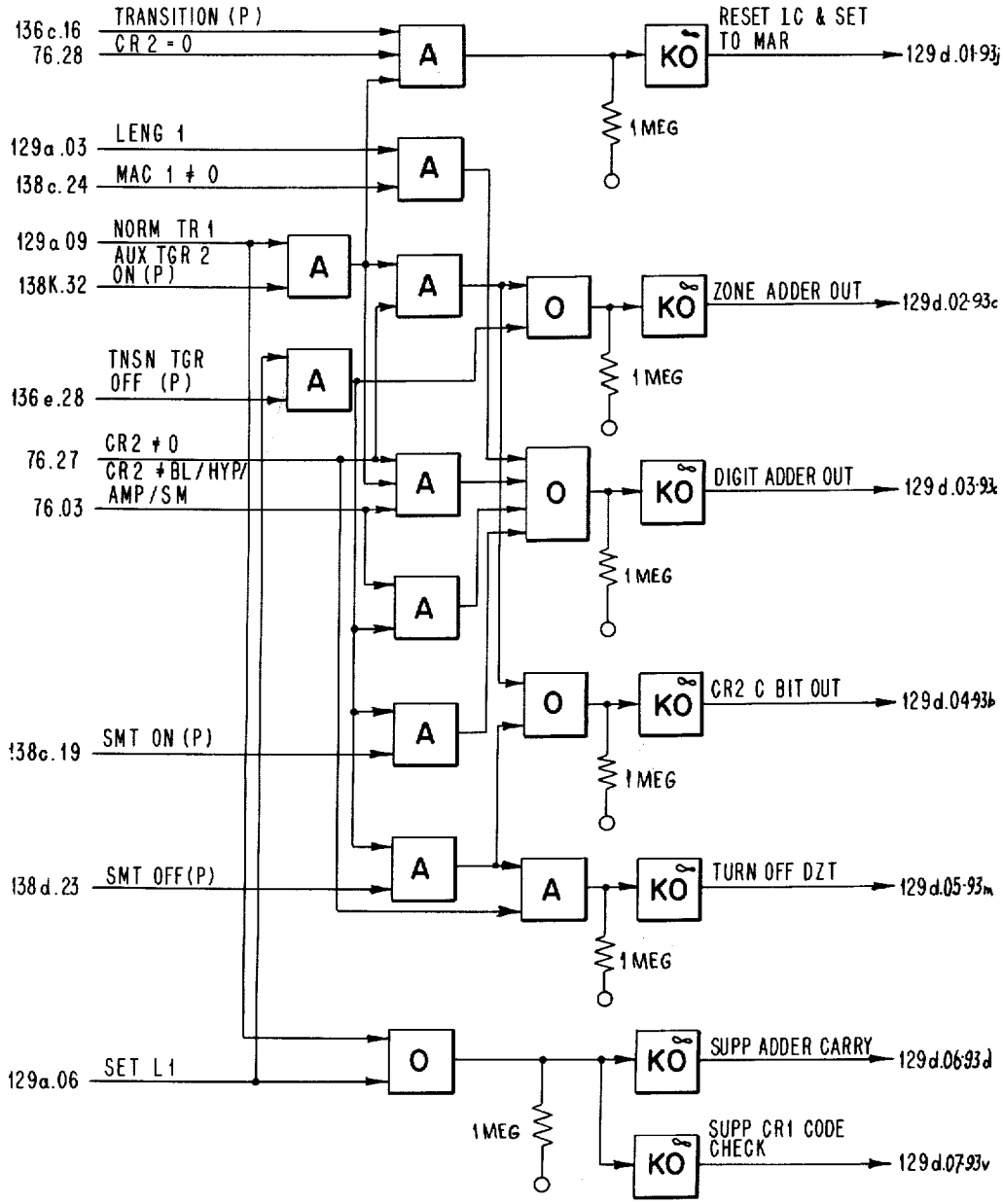


FIG. 129 d

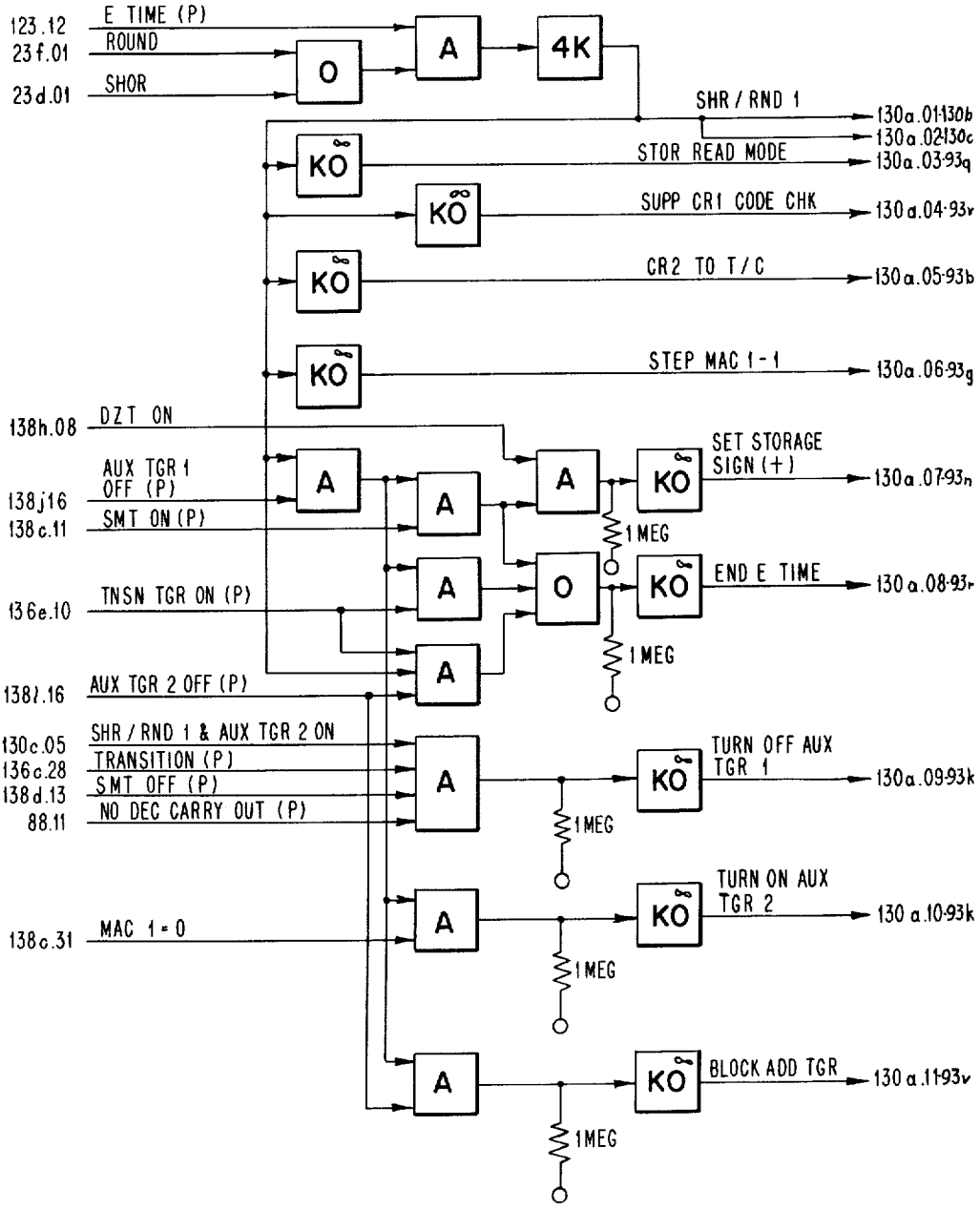
SET LEFT, LENG & NORM TR ROUTING CONTROLS



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FIG. 130a

SHORTEN RIGHT / ROUND ROUTING CONTROLS



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FIG. 130 b

SHORTEN RIGHT / ROUND ROUTING CONTROLS

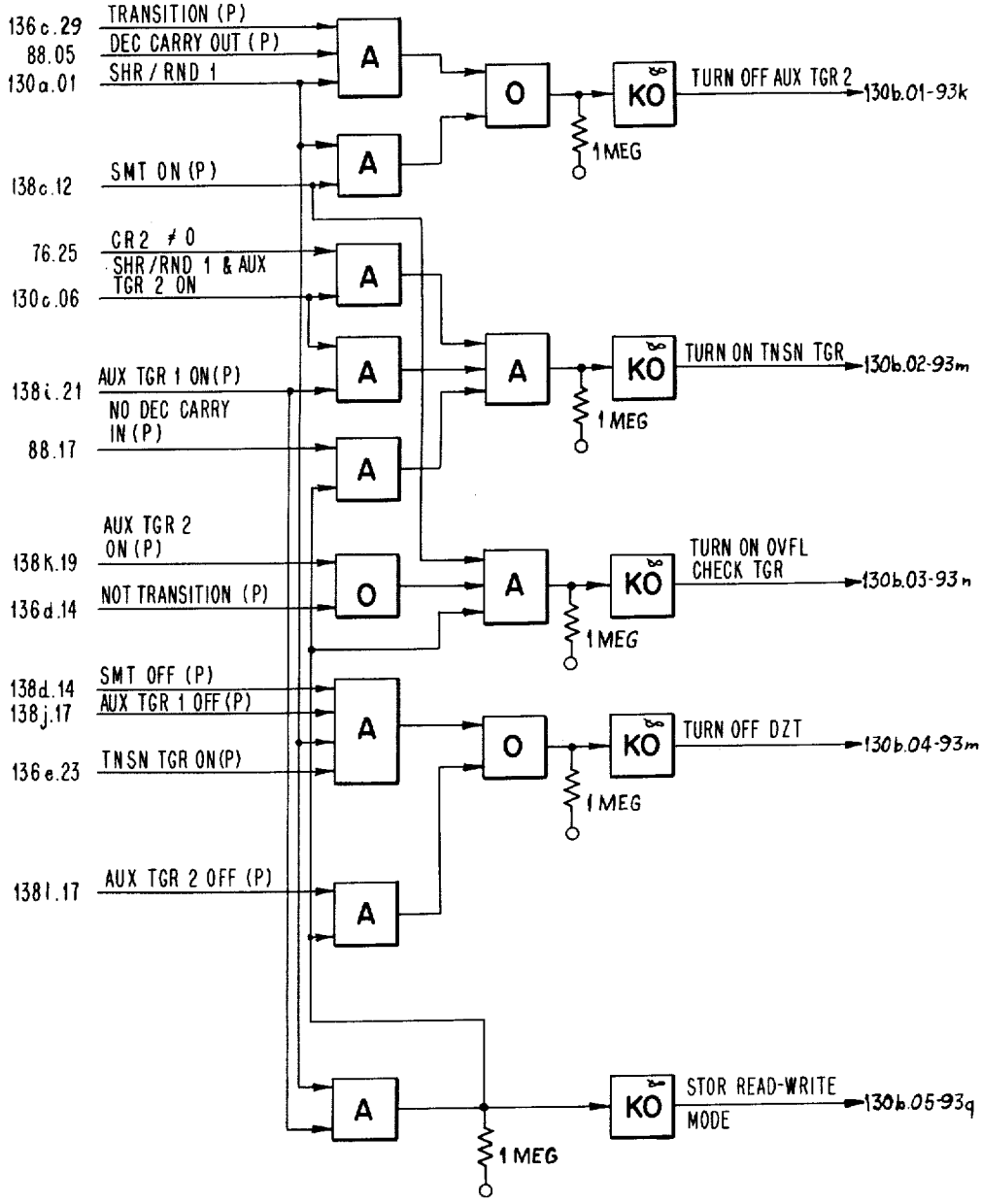
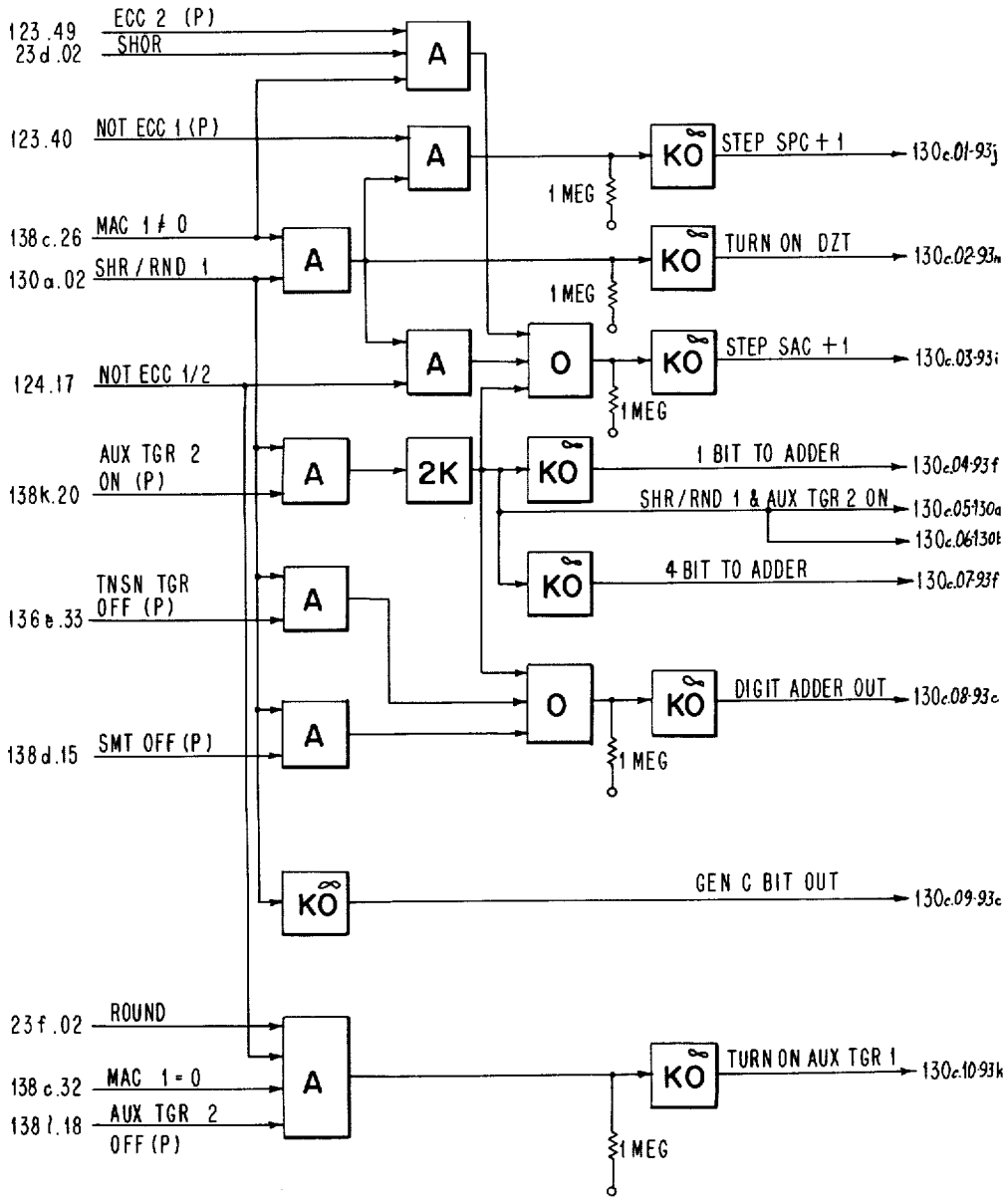


FIG. 130c

SHORTEN RIGHT / ROUND ROUTING CONTROLS



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FIG. 131

R/W AND READ ROUTING CONTROLS

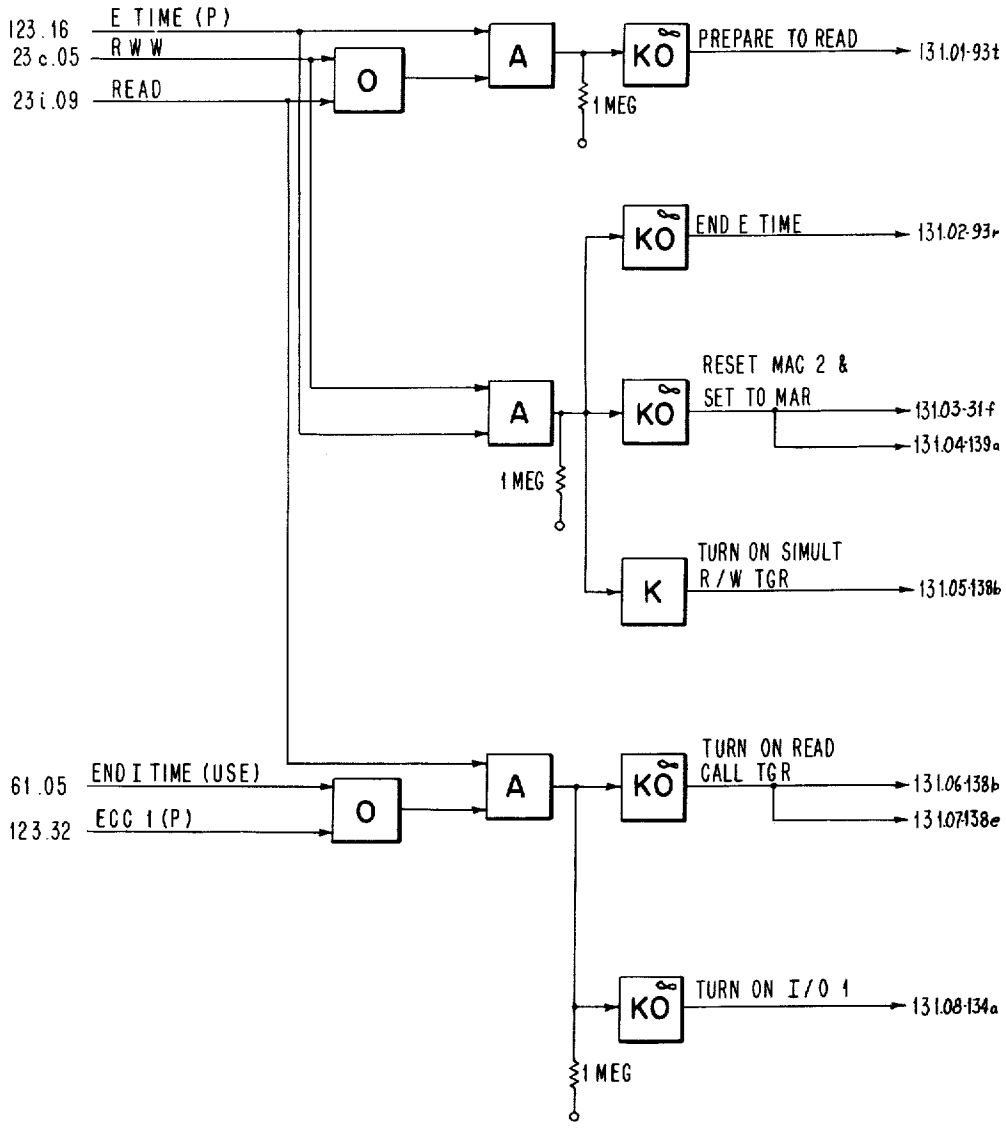


FIG. 132a WRITE-WRITE ERASE ROUTING CONTROLS

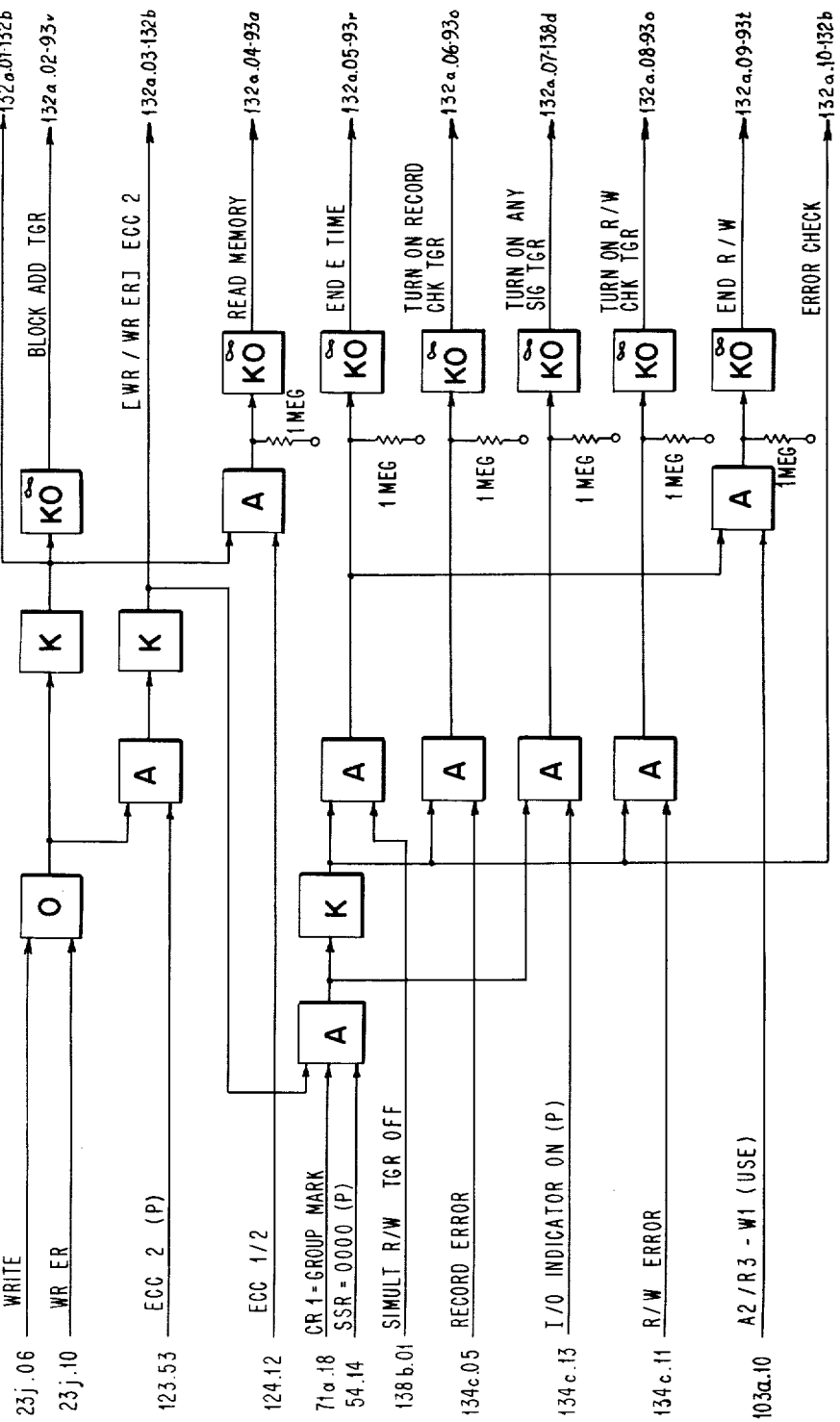
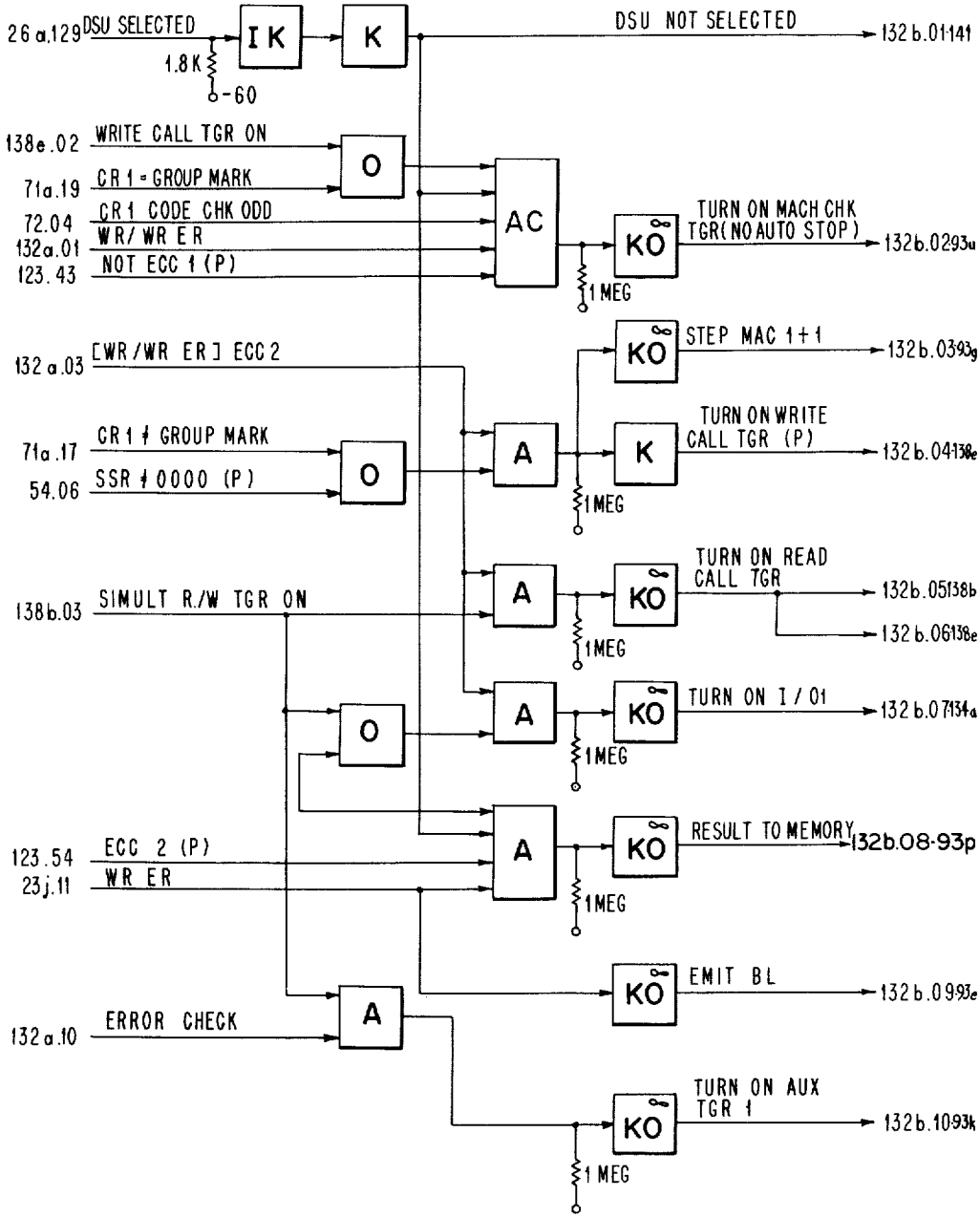


FIG. 132 b

WRITE-WR ER ROUTING CONTROLS



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FIG. 133

SELECT & CONTROL ROUTING CONTROLS

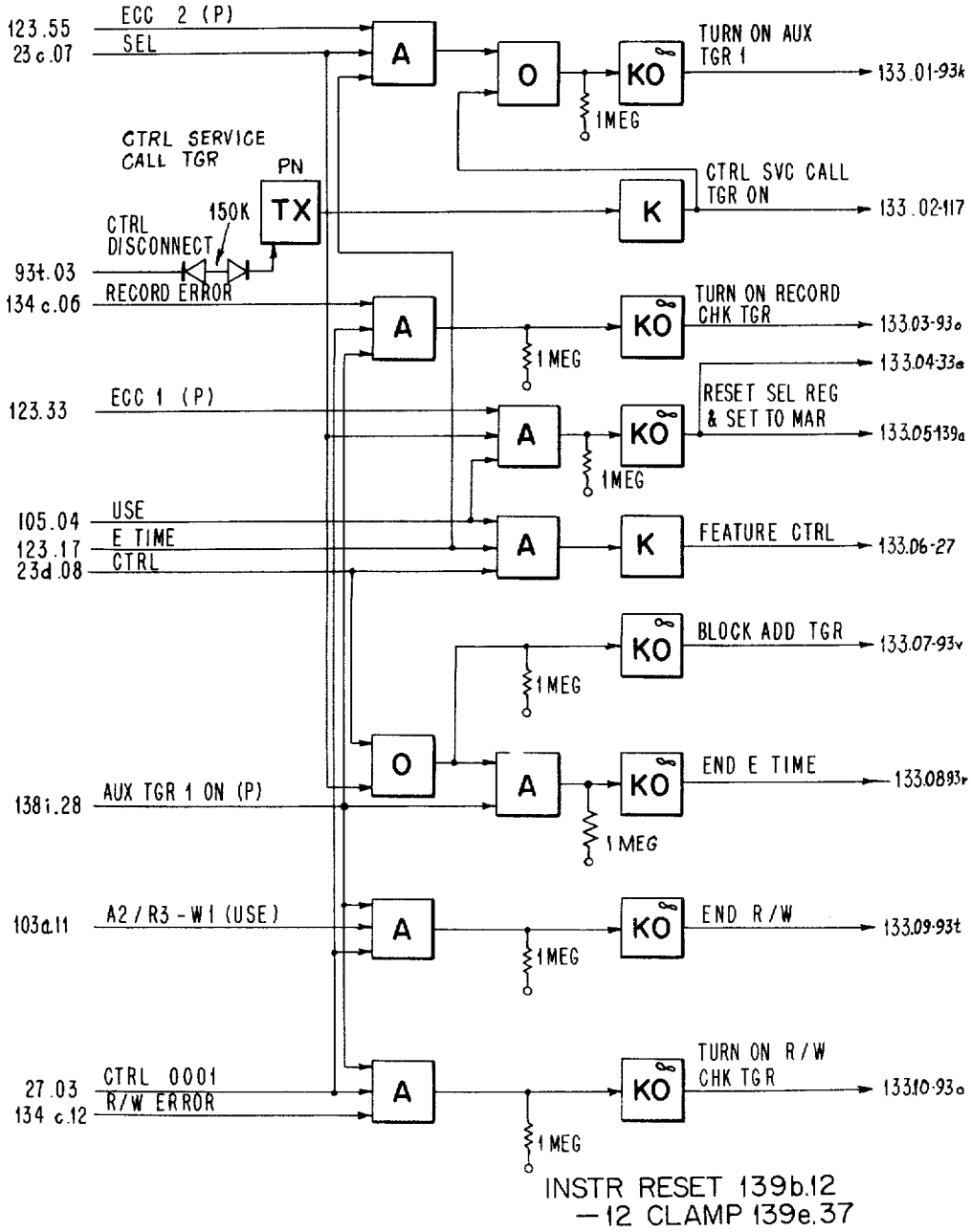


FIG. 134a

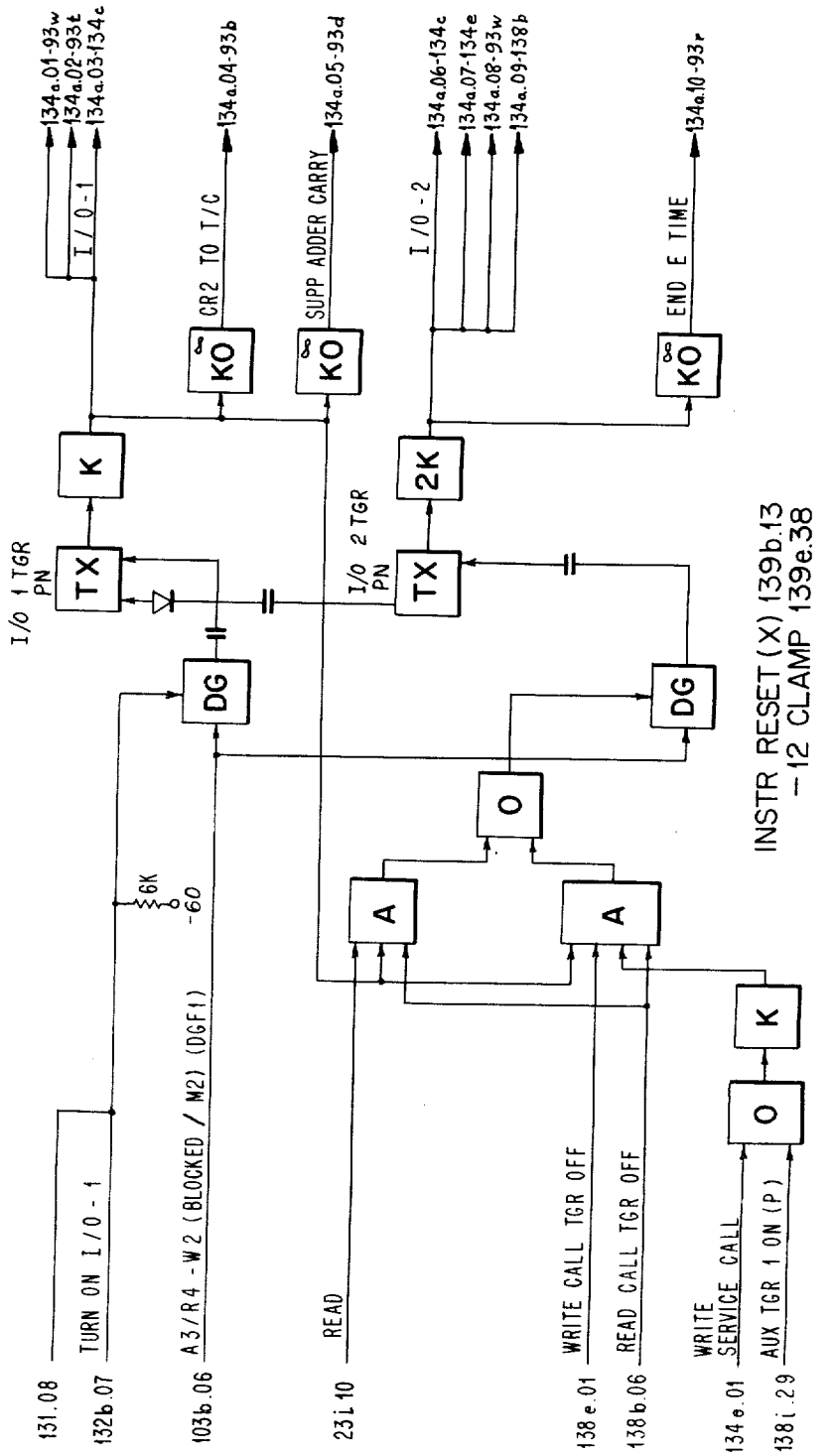

I/O SEQUENCE 1 & 2 TGRS
134a.01-93w
134a.02-93t
134a.03-134c
I/O-1
134a.04-93b
CR2 TO T/C
134a.05-93d
SUPP ADDER CARRY
134a.06-134c
134a.07-134e
134a.08-93w
134a.09-138b
I/O-2
134a.10-93r
END E TIME
K
KO
KO
2K
KO
I/O 1 TGR PN
I/O 2 TGR PN
TX
TX
DG
DG
O
A
A
K
O
6K
-60
INSTR RESET (X) 139b.13
-12 CLAMP 139e.38
131.08
132b.07 TURN ON I/O-1
103b.06 A3/R4-W2 (BLOCKED / M2) (DGF1)
231.10 READ
138e.01 WRITE CALL TGR OFF
138b.06 READ CALL TGR OFF
134e.01 WRITE SERVICE CALL
138i.29 AUX TGR 1 ON (P)

FIG. 134b

I/O SEQUENCE ROUTING

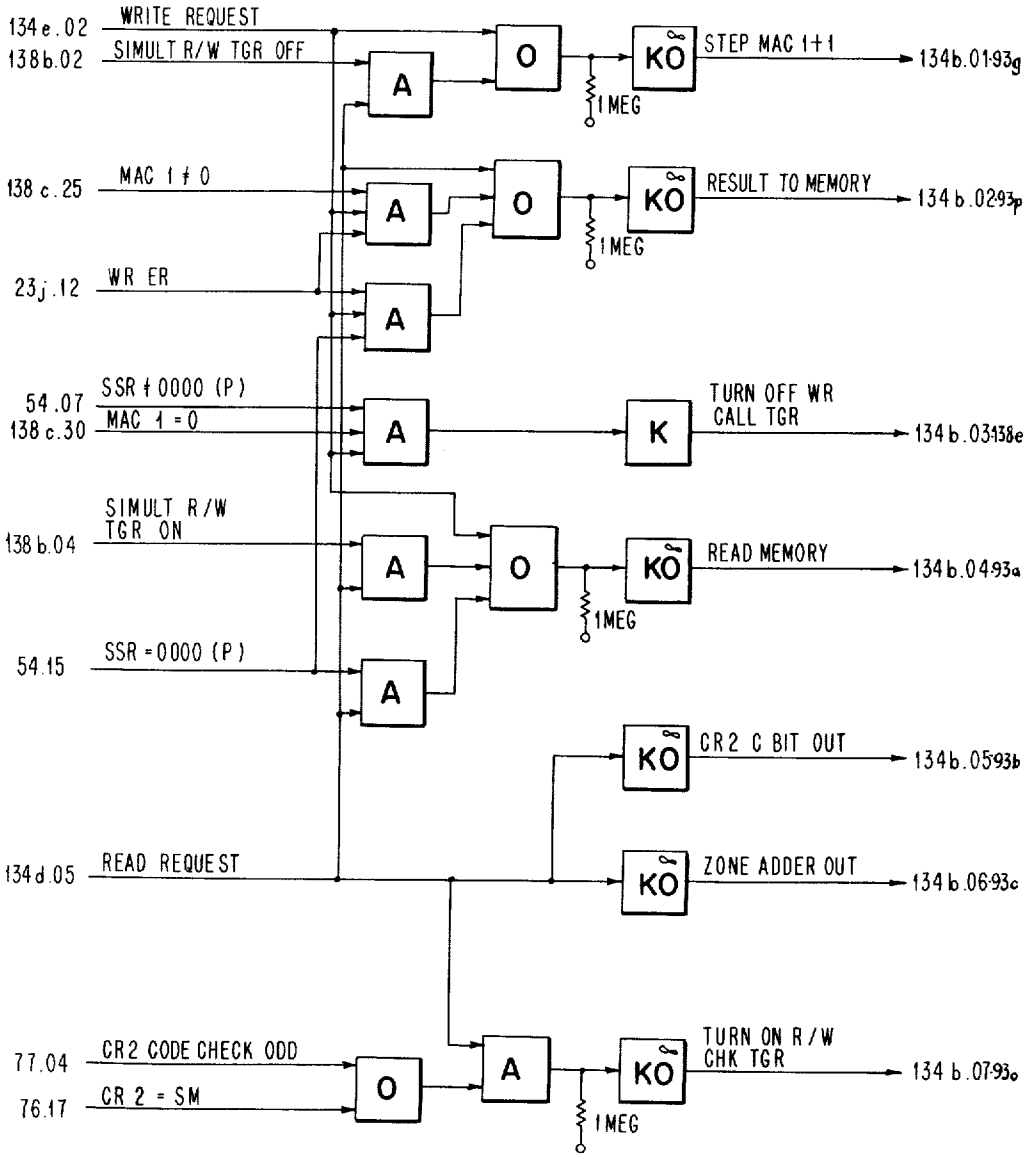


FIG. 134 c

I/O SEQUENCE ROUTING

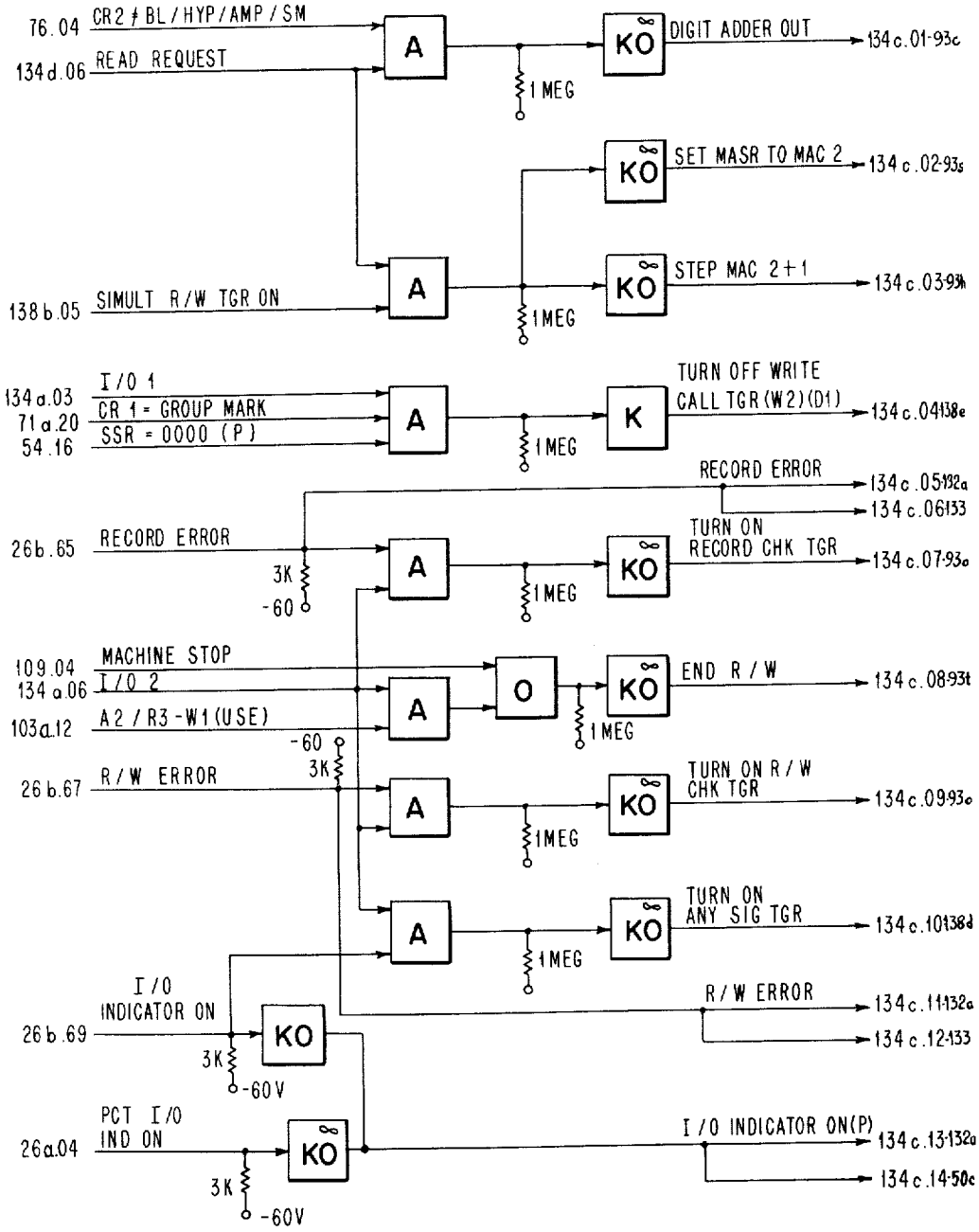


FIG. 134d

I/O SEQUENCE - READ SERVICE CALL, READ REQUEST TGRS

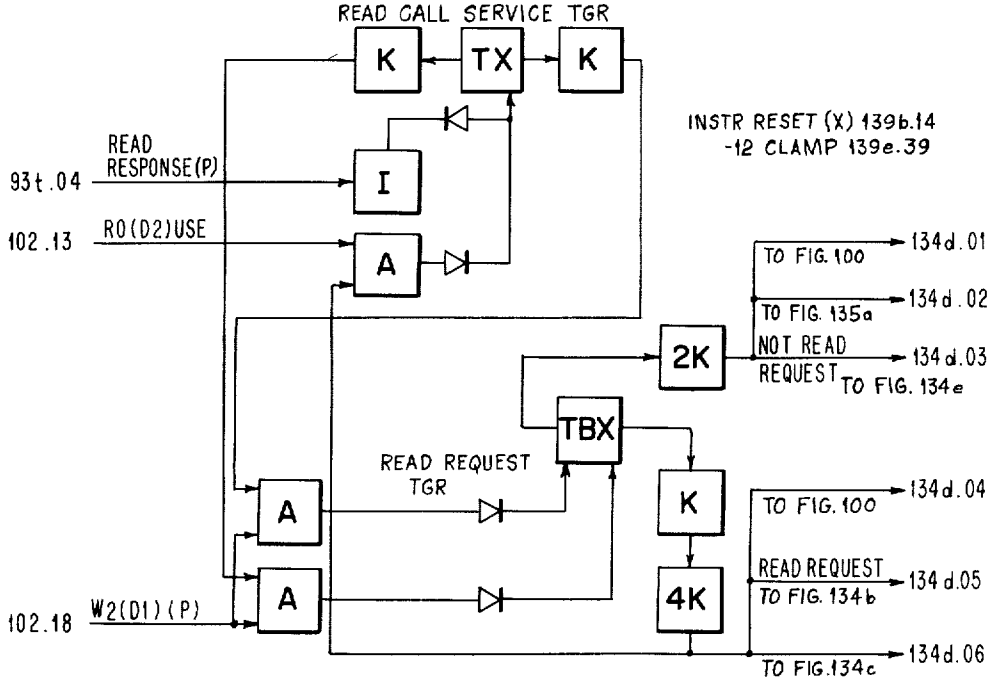


FIG. 134e

I/O SEQUENCE - WRITE SERVICE CALL, REQUEST TGRS

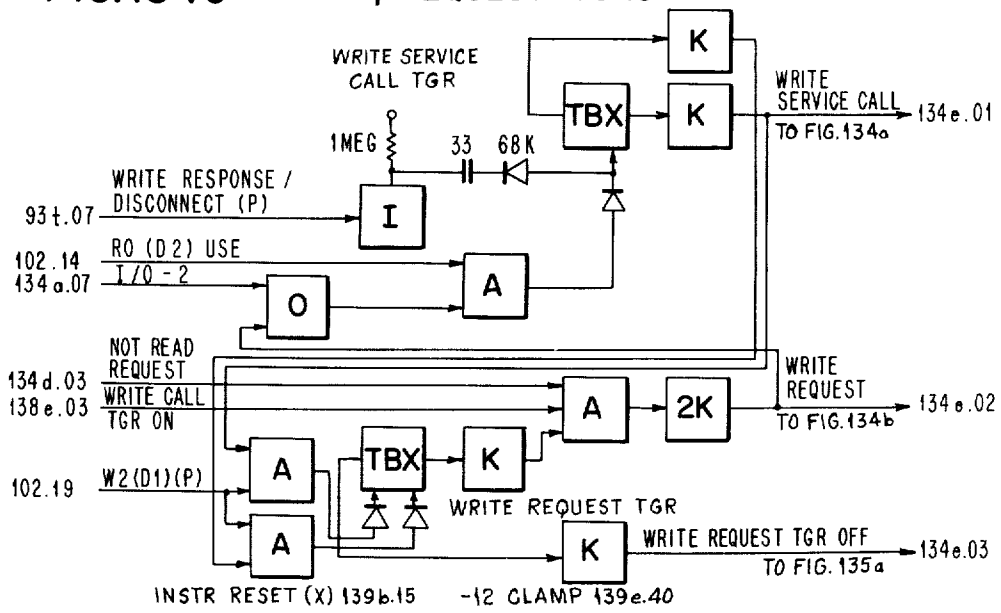


FIG. 134f TRC PULL DOWN PULSE ; I/O SYNC PULSE

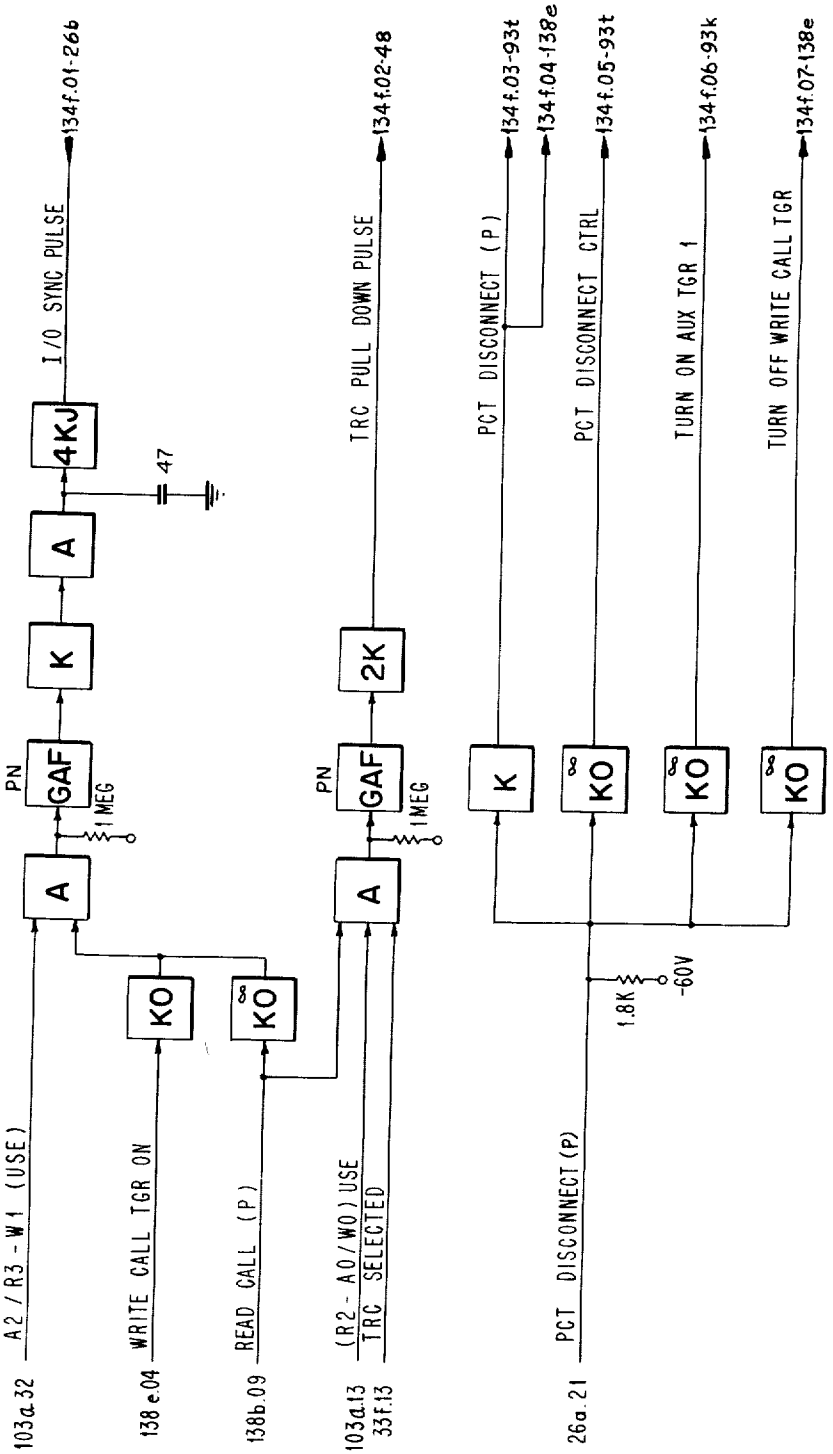
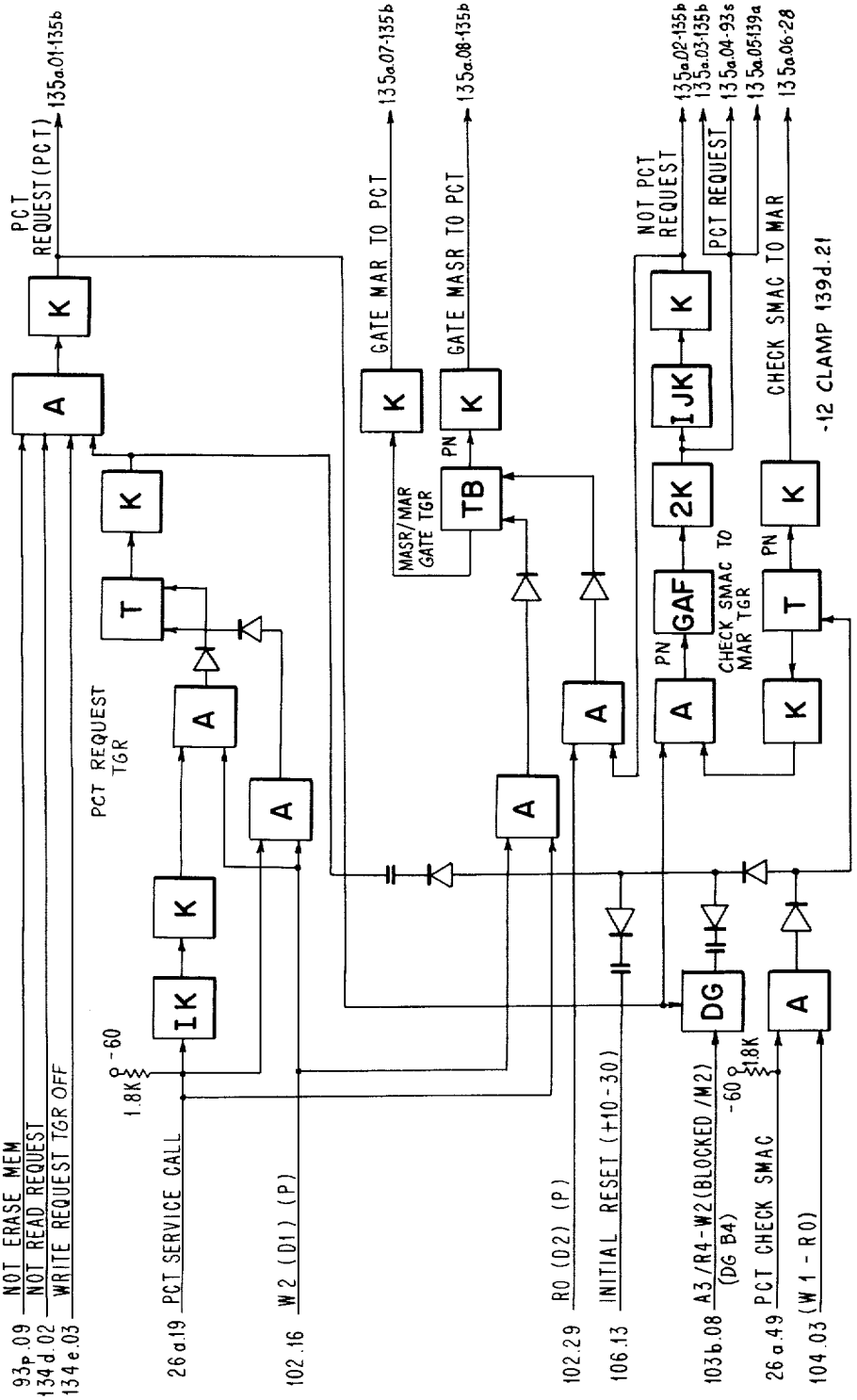


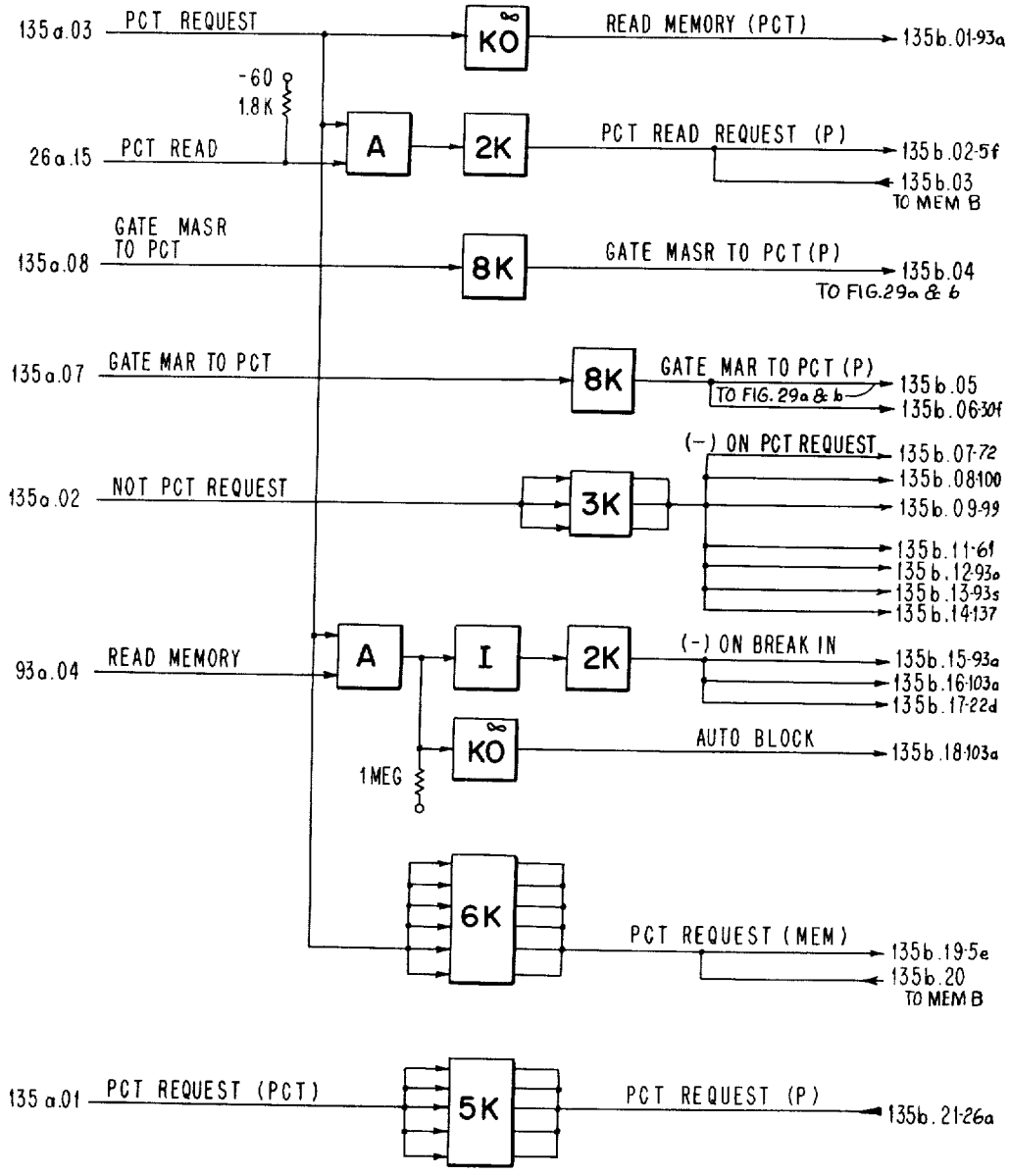
FIG. 135a


PCT REQUEST, CHK SMAC TO MAR & MASR / MAR GATE TGRS
93p.09 NOT ERASE MEM
134d.02 NOT READ REQUEST
134e.03 WRITE REQUEST TGR OFF
26a.19 PCT SERVICE CALL
102.16 W2 (D1) (P)
102.29 R0 (D2) (P)
106.13 INITIAL RESET (+10-30)
103b.08 A3/R4-W2(BLOCKED/M2) (DG B4)
26a.49 PCT CHECK SMAC
104.03 (W1-R0)
PCT REQUEST (PCT) 135a.01-135b
PCT REQUEST TGR
GATE MAR TO PCT 135a.07-135b
GATE MASR TO PCT 135a.08-135b
MASR/MAR GATE TGR
NOT PCT REQUEST 135a.02-135b 135a.03-135b
PCT REQUEST 135a.04-93s 135a.05-139a
CHECK SMAC TO MAR 135a.06-28
CHECK SMAC TO MAR TGR
-12 CLAMP 139d.21
-60
1.8K
A
K
T
IK
TB
PN
GAF
2K
IJK
DG

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FIG. 135b

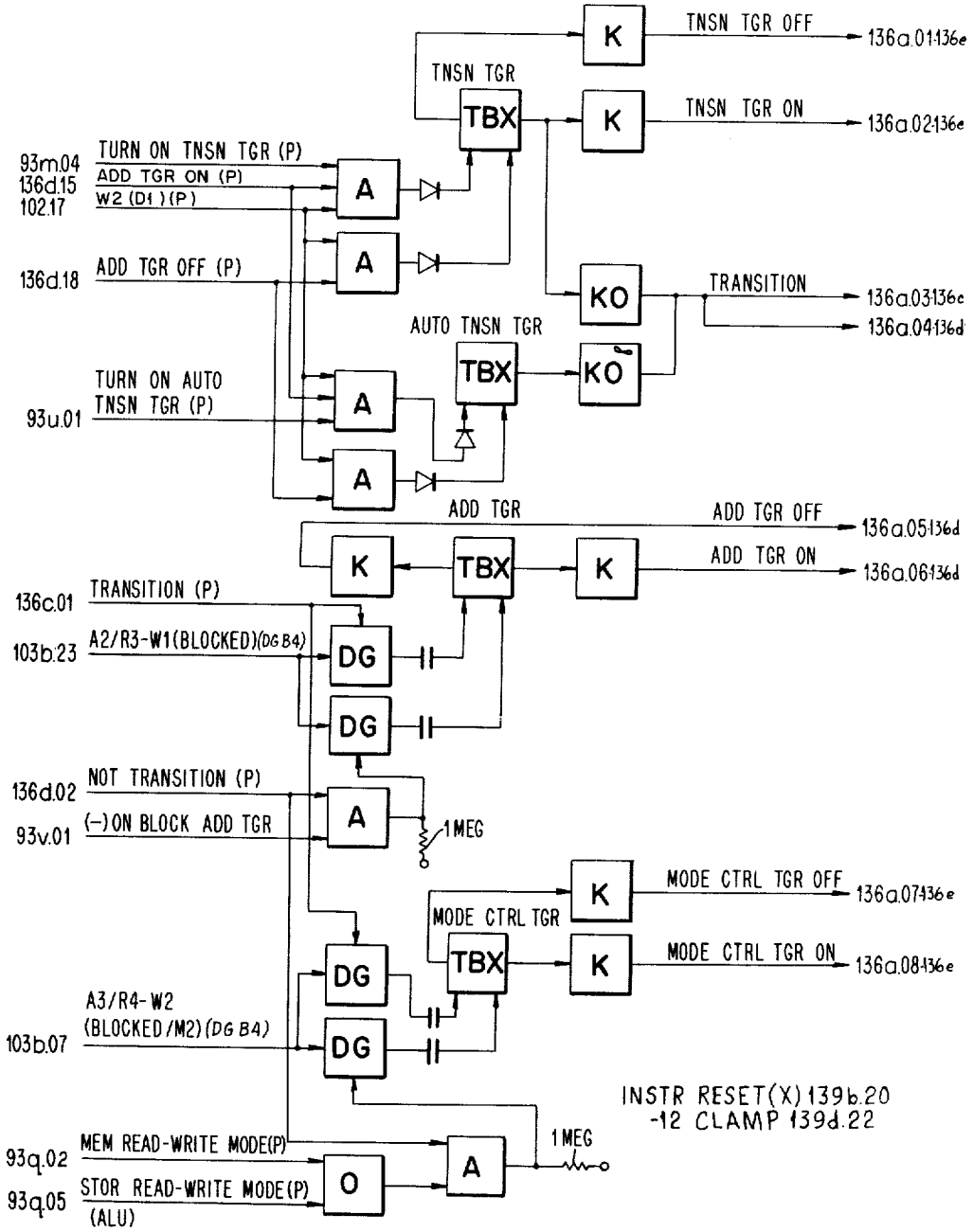
PCT REQUEST EXECUTION CONTROLS



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FIG.136a

OVERLAP CONTROL TRIGGERS



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FIG.136b

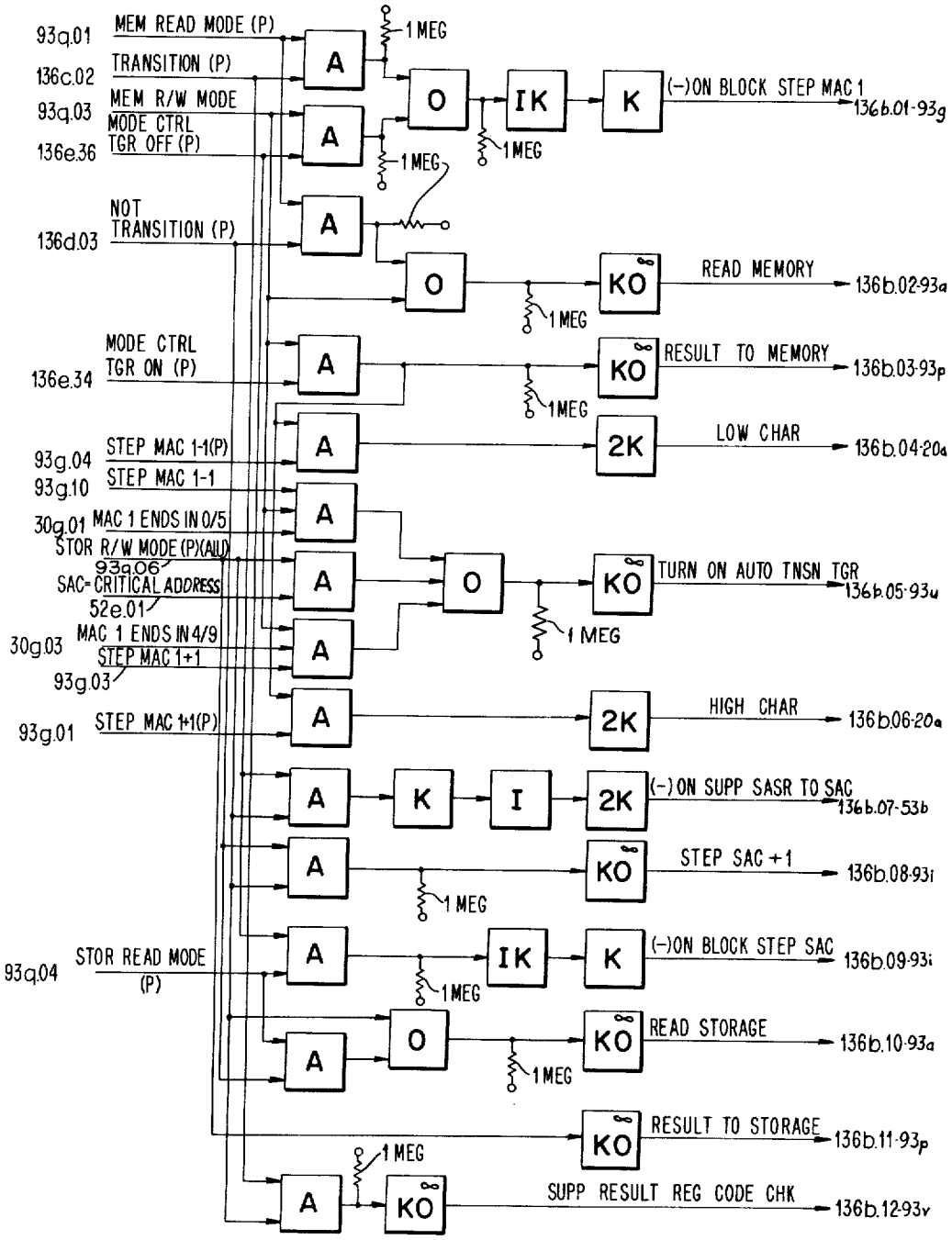


FIG.136c TRANSITION POWERING

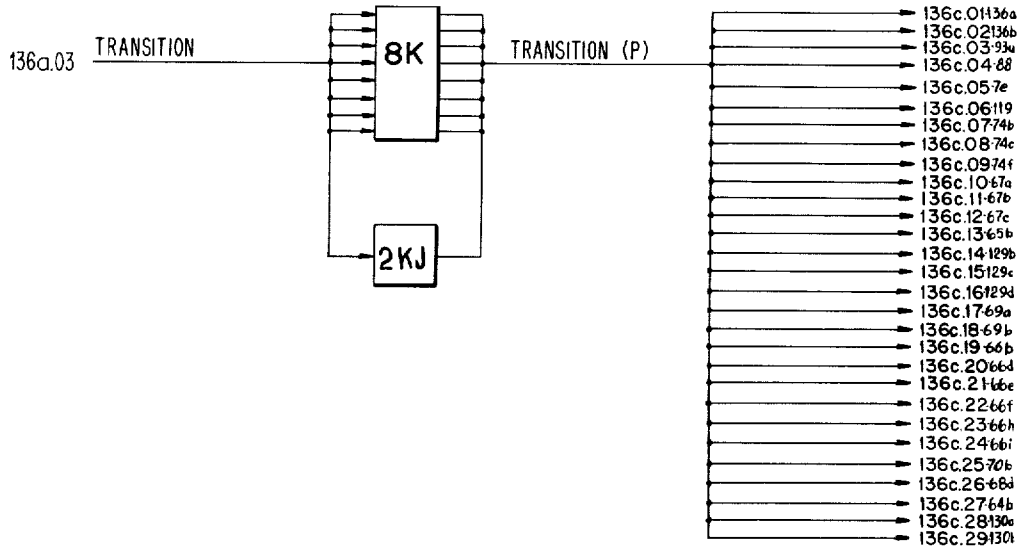


FIG.136d NOT TRANSITION & ADD TGR POWERING

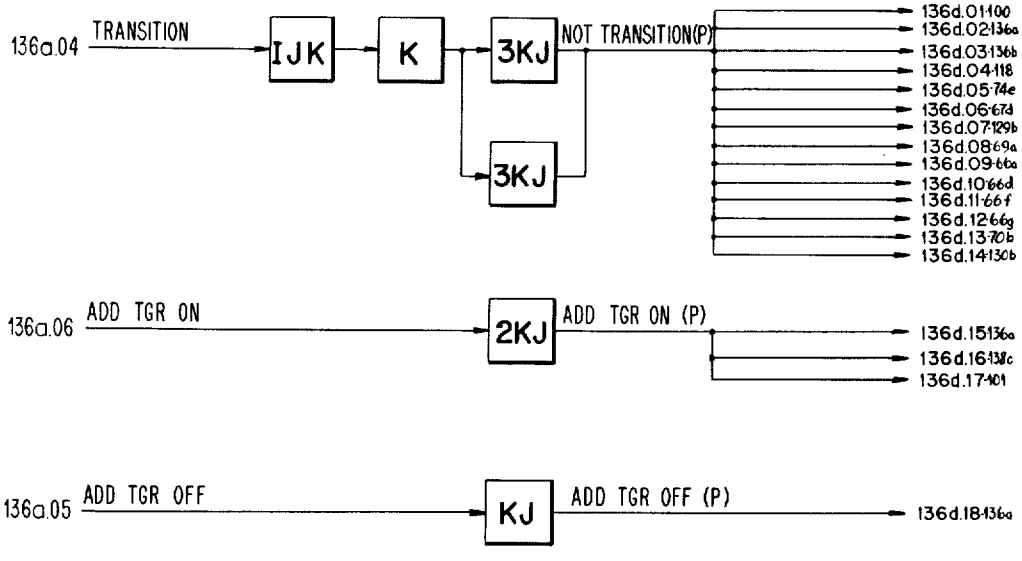


FIG. 136e

TNSN TGR, MODE CTRL TGR POWERING

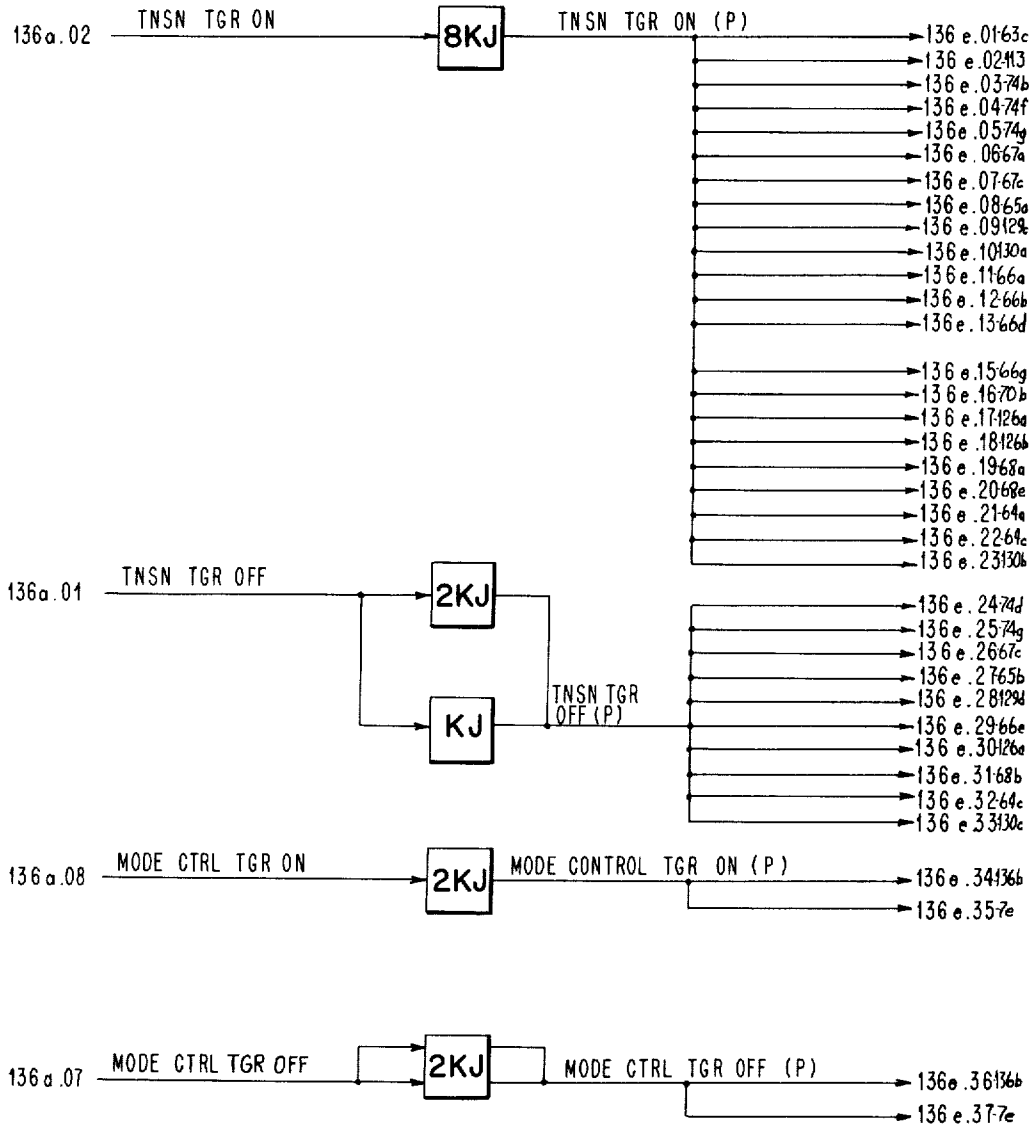


FIG. 137

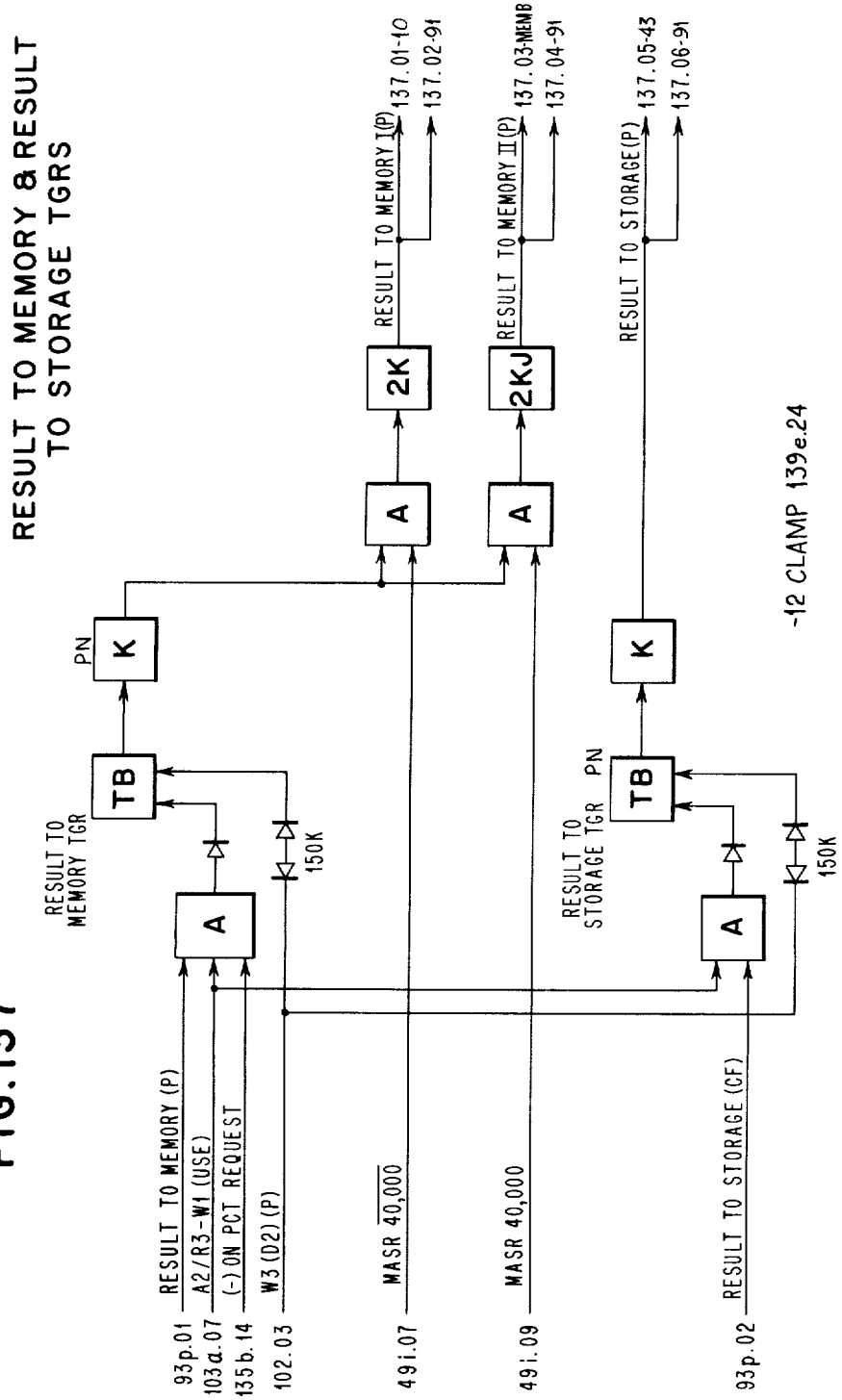
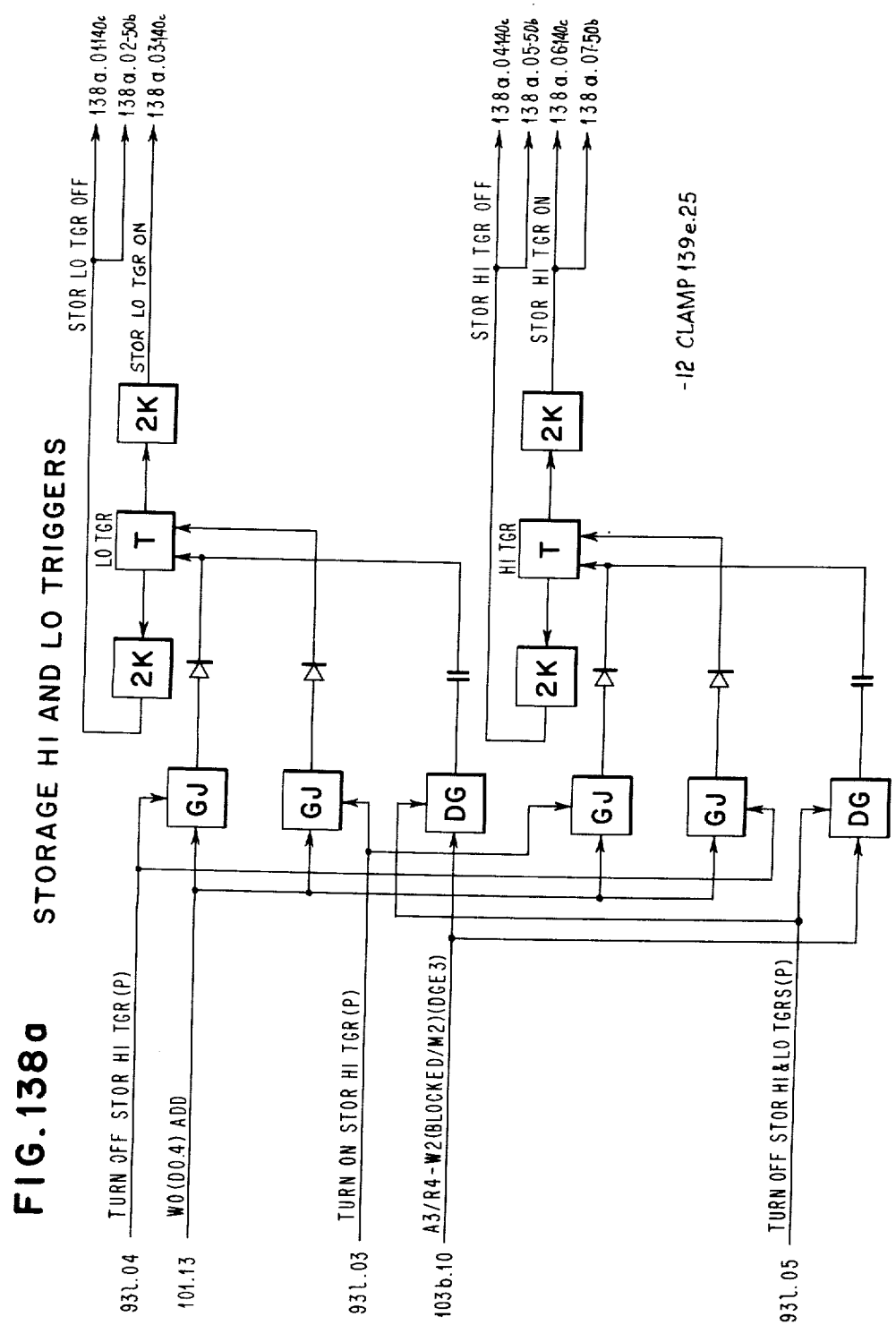

RESULT TO MEMORY & RESULT TO STORAGE TGRS
RESULT TO MEMORY (P)
A2/R3-W1 (USE)
(-) ON PCT REQUEST
W3 (D2) (P)
MASR 40,000
MASR 40,000
RESULT TO STORAGE (CF)
93p.01
103a.07
135b.14
102.03
49i.07
49i.09
93p.02
RESULT TO MEMORY TGR
RESULT TO STORAGE TGR
PN
TB
K
A
150K
2K
2KJ
RESULT TO MEMORY I(P)
RESULT TO MEMORY II(P)
RESULT TO STORAGE(P)
137.01-10
137.02-91
137.03-MEMB
137.04-91
137.05-43
137.06-91
-12 CLAMP 139e.24

FIG. 138a


STORAGE HI AND LO TRIGGERS
STOR LO TGR OFF
STOR LO TGR ON
138a.0114c
138a.0250b
138a.0344c
LO TGR
T
2K
2K
GJ
GJ
DG
TURN OFF STOR HI TGR (P)
WO(00.4) ADD
TURN ON STOR HI TGR (P)
A3/R4-W2(BLOCKED/M2)(DGE3)
931.04
101.13
931.03
1036.10
STOR HI TGR OFF
STOR HI TGR ON
138a.0444c
138a.0550b
138a.0644c
138a.0750b
HI TGR
T
2K
2K
GJ
GJ
DG
TURN OFF STOR HI&LO TGRS(P)
931.05
-12 CLAMP 139e.25

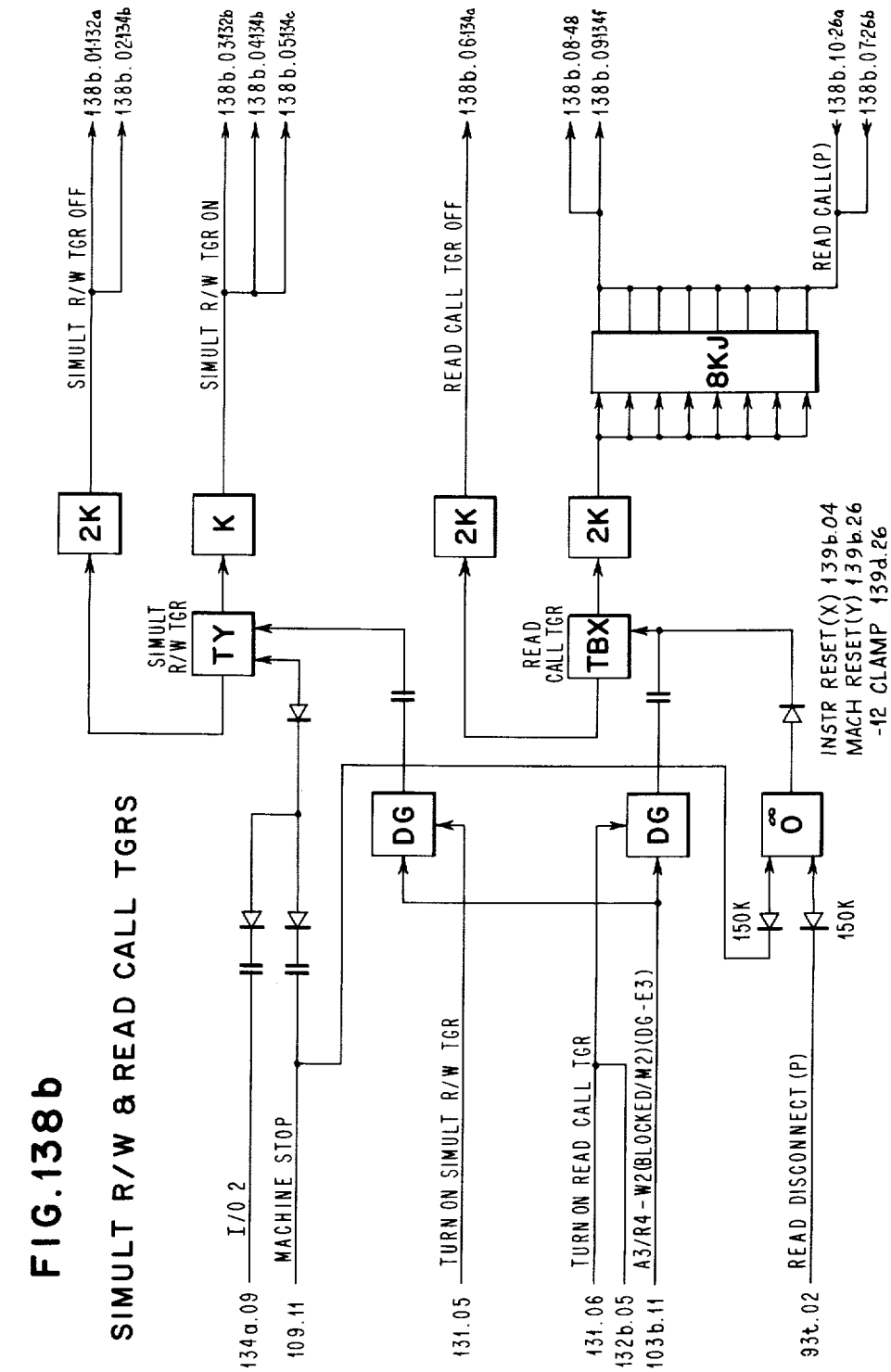


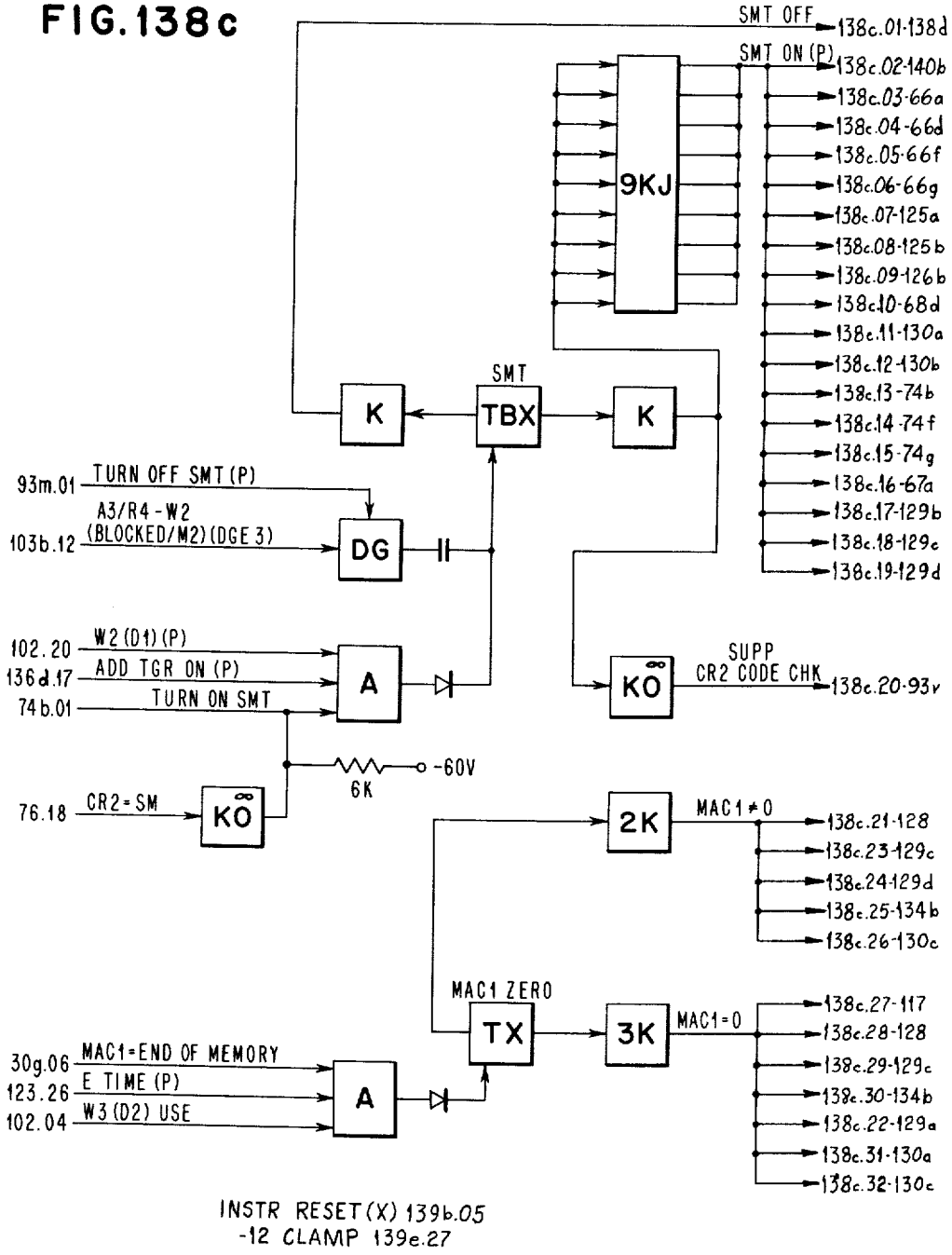
FIG. 138b

SIMULT R/W & READ CALL TGRS

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STORAGE MARK TGR & MAC1=0 TGR

FIG. 138c



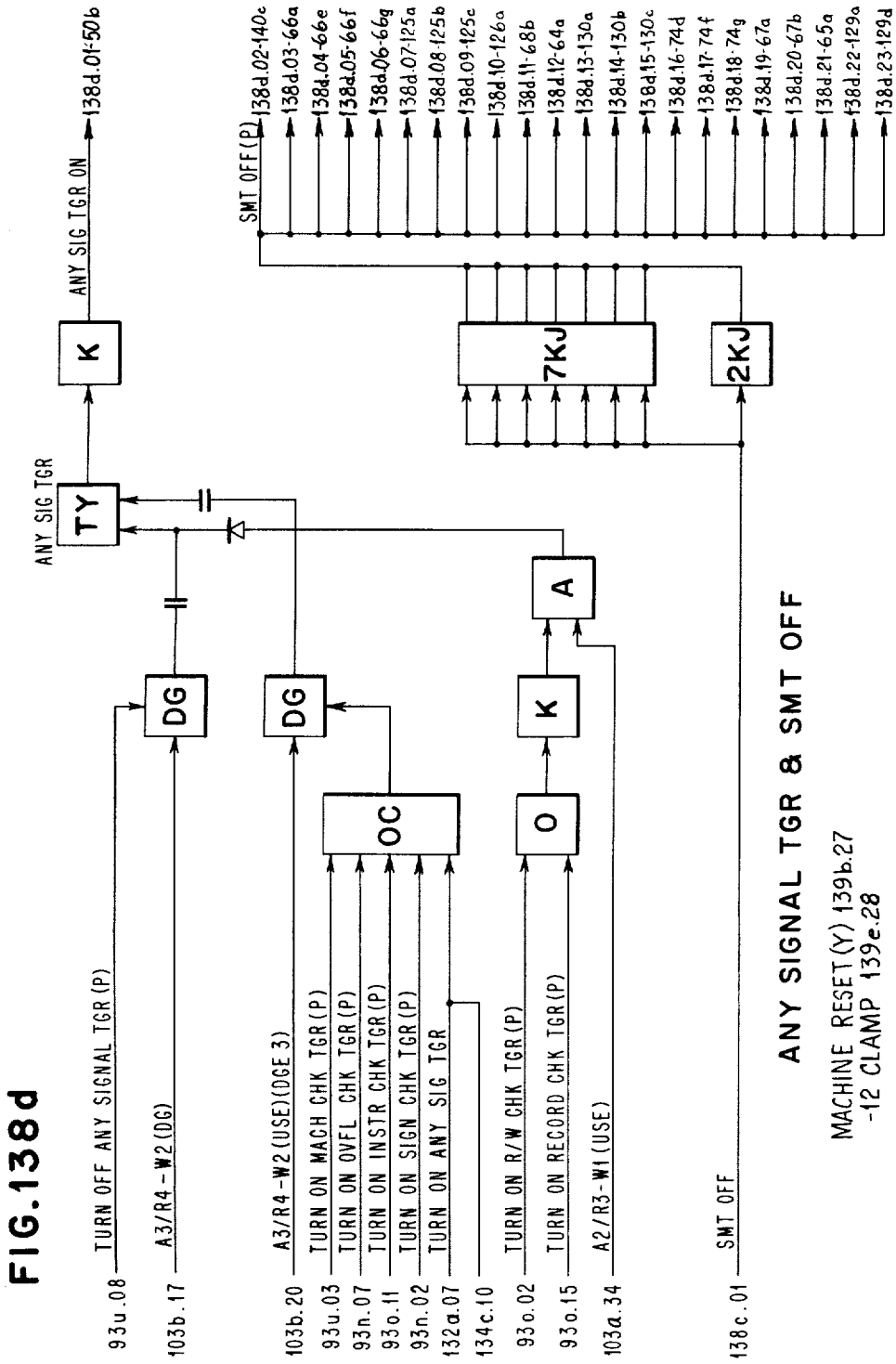

ANY SIG TGR
TY
K
ANY SIG TGR ON
138d.01-50b
SMT OFF(P)
138d.02-140c
138d.03-66a
138d.04-66e
138d.05-66f
138d.06-66g
138d.07-125a
138d.08-125b
138d.09-125c
138d.10-126a
138d.11-68b
138d.12-64a
138d.13-130a
138d.14-130b
138d.15-130c
138d.16-74d
138d.17-74f
138d.18-74g
138d.19-67a
138d.20-67b
138d.21-65a
138d.22-129a
138d.23-129d
7KJ
2KJ
DG
DG
A
K
OC
O
93u.08 TURN OFF ANY SIGNAL TGR(P)
103b.17 A3/R4-W2(DG)
103b.20 A3/R4-W2(USE)(DGE 3)
93u.03 TURN ON MACH CHK TGR(P)
93n.07 TURN ON OVFL CHK TGR(P)
93o.11 TURN ON INSTR CHK TGR(P)
93n.02 TURN ON SIGN CHK TGR(P)
132a.07 TURN ON ANY SIG TGR
134c.10
93o.02 TURN ON R/W CHK TGR(P)
93o.15 TURN ON RECORD CHK TGR(P)
103a.34 A2/R3-W1(USE)
138c.01 SMT OFF
ANY SIGNAL TGR & SMT OFF
MACHINE RESET(Y) 139b.27
-12 CLAMP 139e.28

FIG.138d

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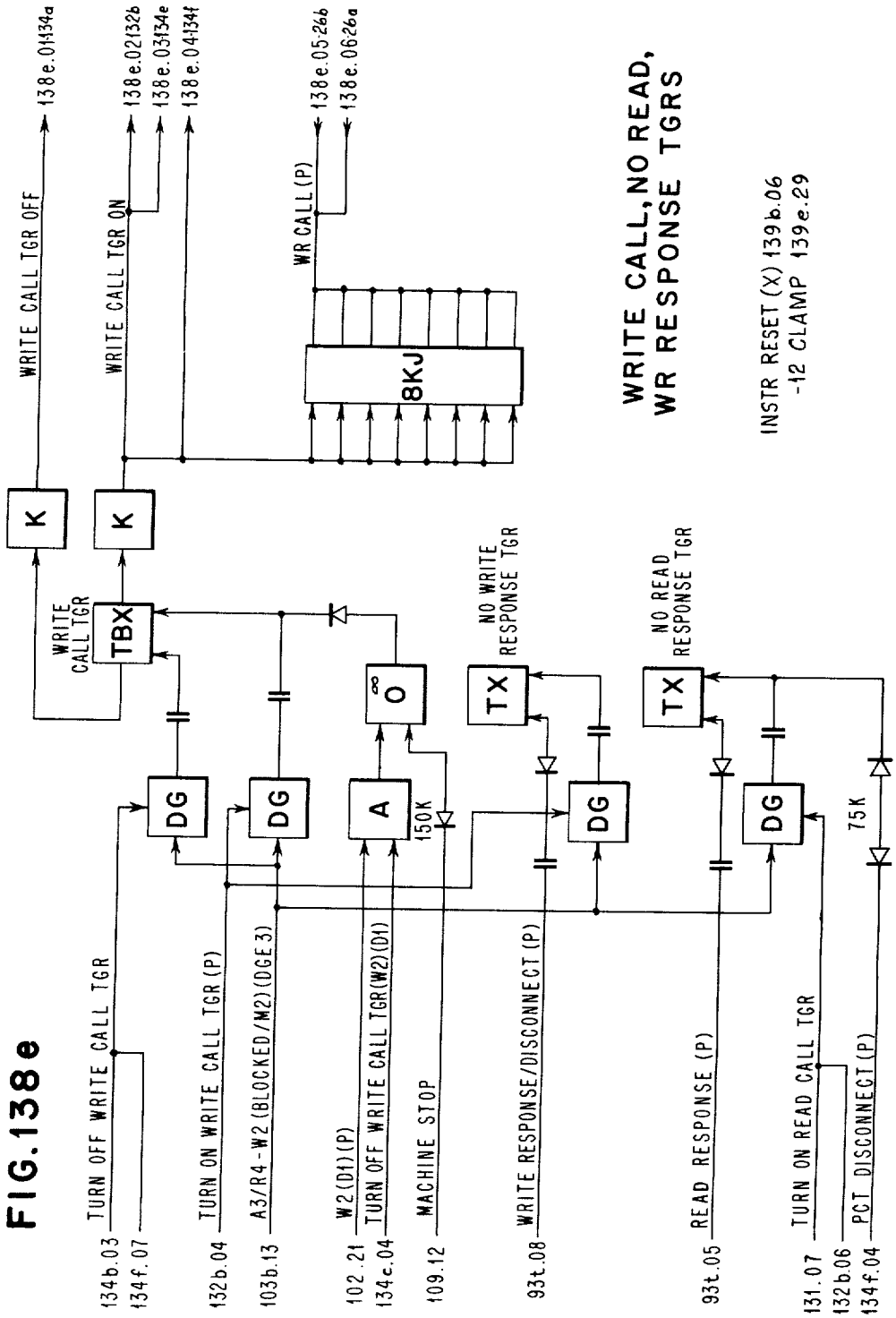


FIG. 138e

WRITE CALL, NO READ, WR RESPONSE TGRS

INSTR RESET (X) 139b.06
-12 CLAMP 139e.29

FIG. 138f

INST. CHK. MACH. CHK, & R/W CHK. TGRS.

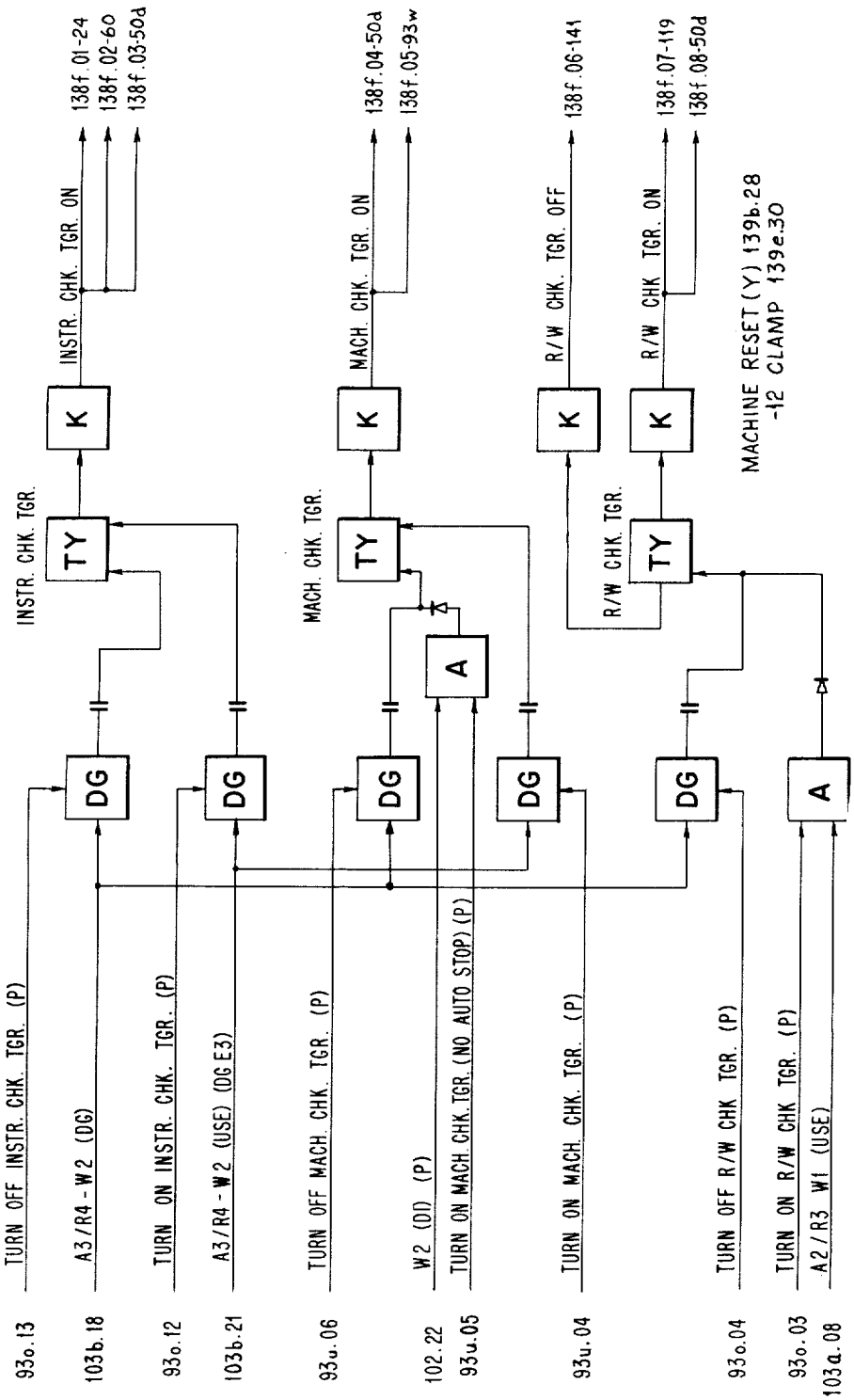
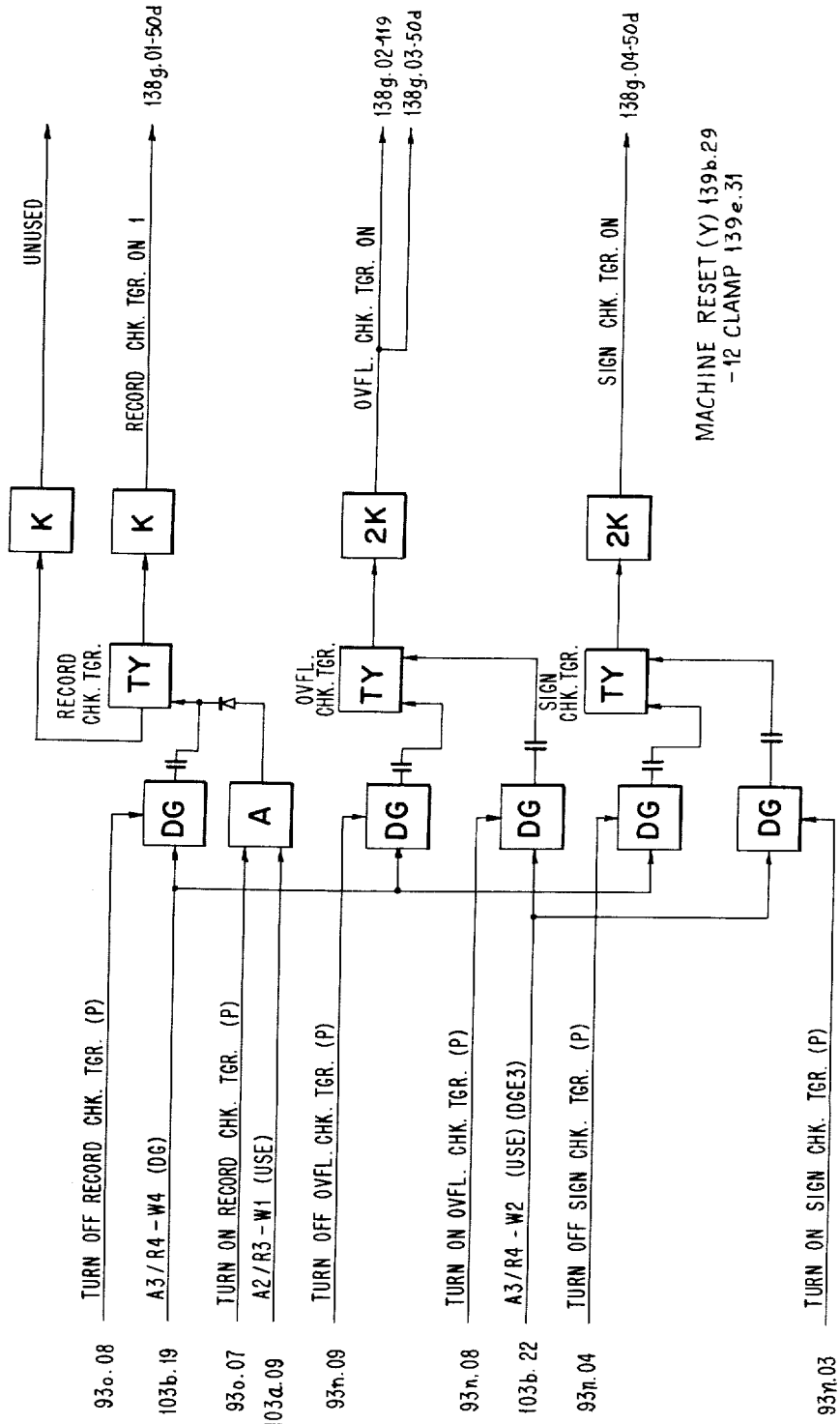


FIG. 138g
RECORD, OVFL, & SIGN-CHK. TGRS.



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FIG. 138h

DIGIT ZERO TGRS. & REMAINDER TGR

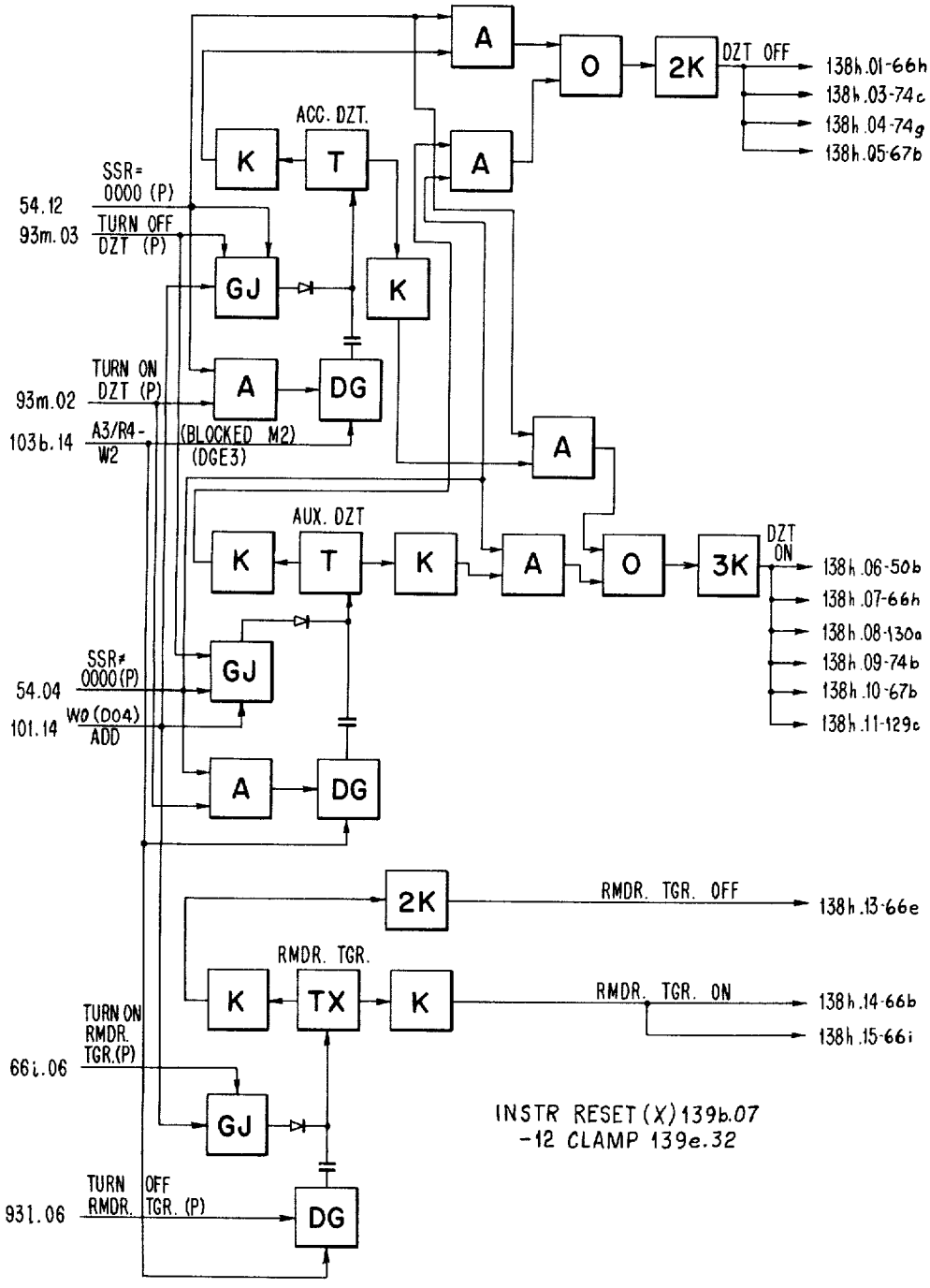
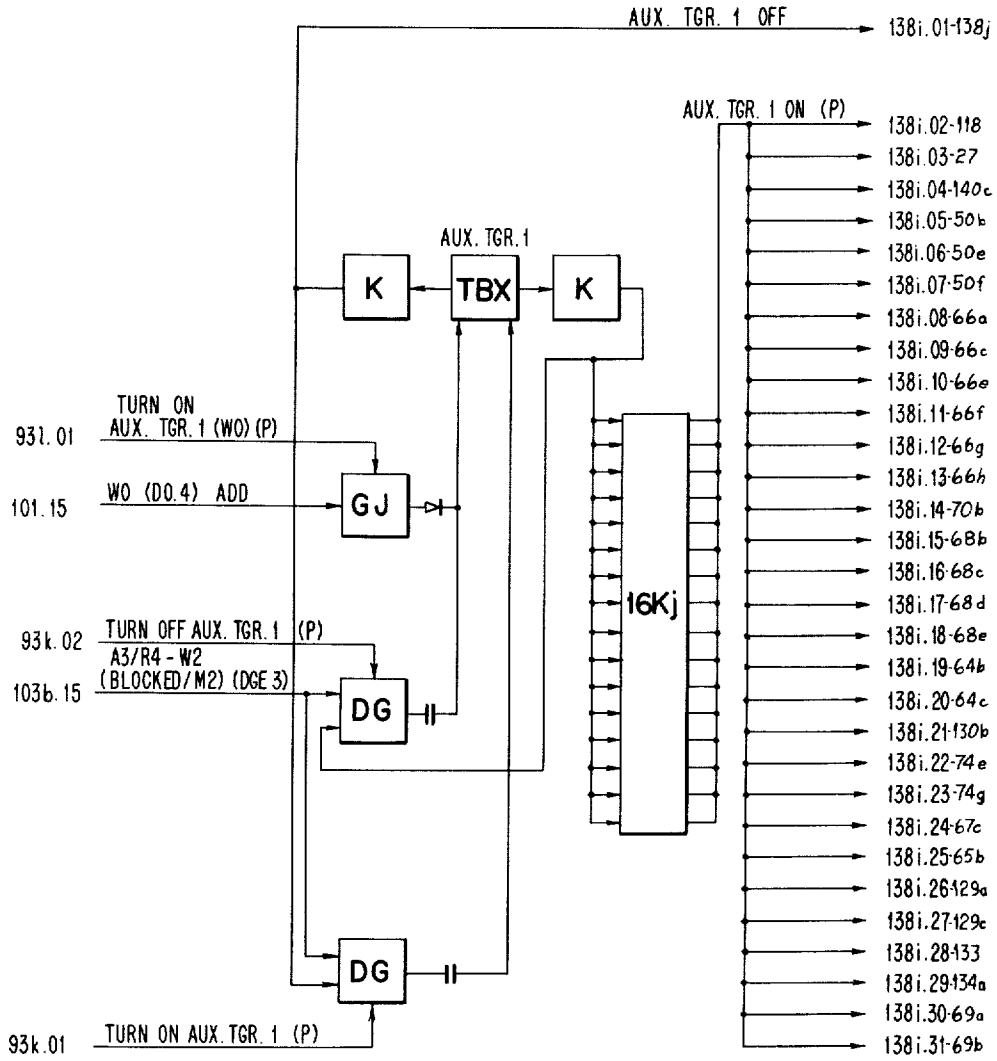


FIG. 138 i

AUXILIARY TGR. 1



INSTR RESET (X) 139b.08
-12 CLAMP 139e.33

FIG. 138j

AUXILIARY TGR. 1 OFF POWERING

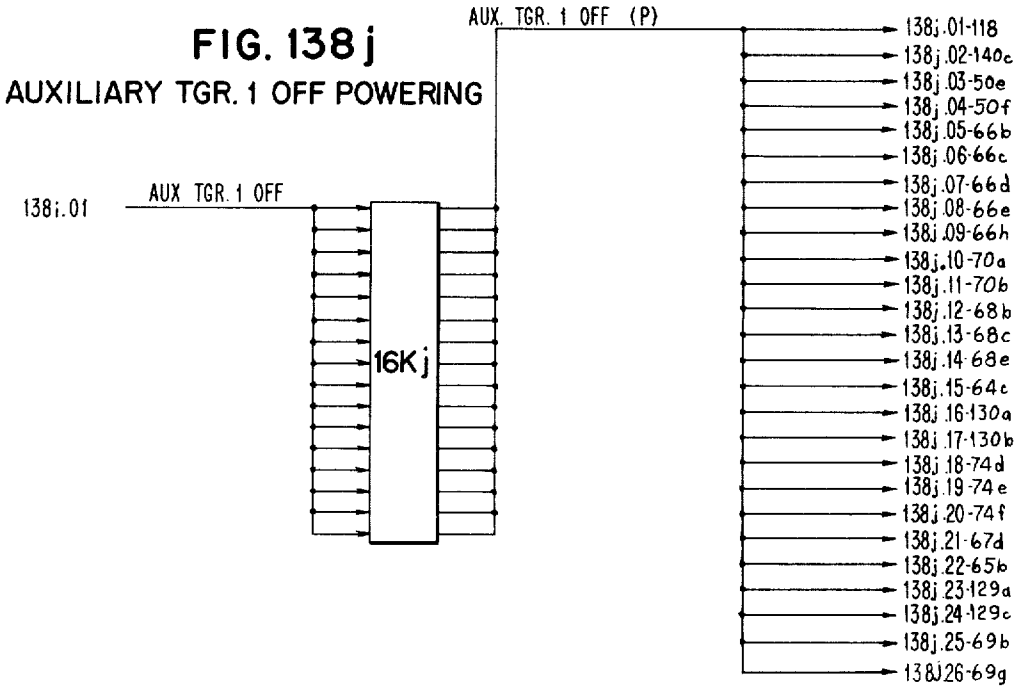
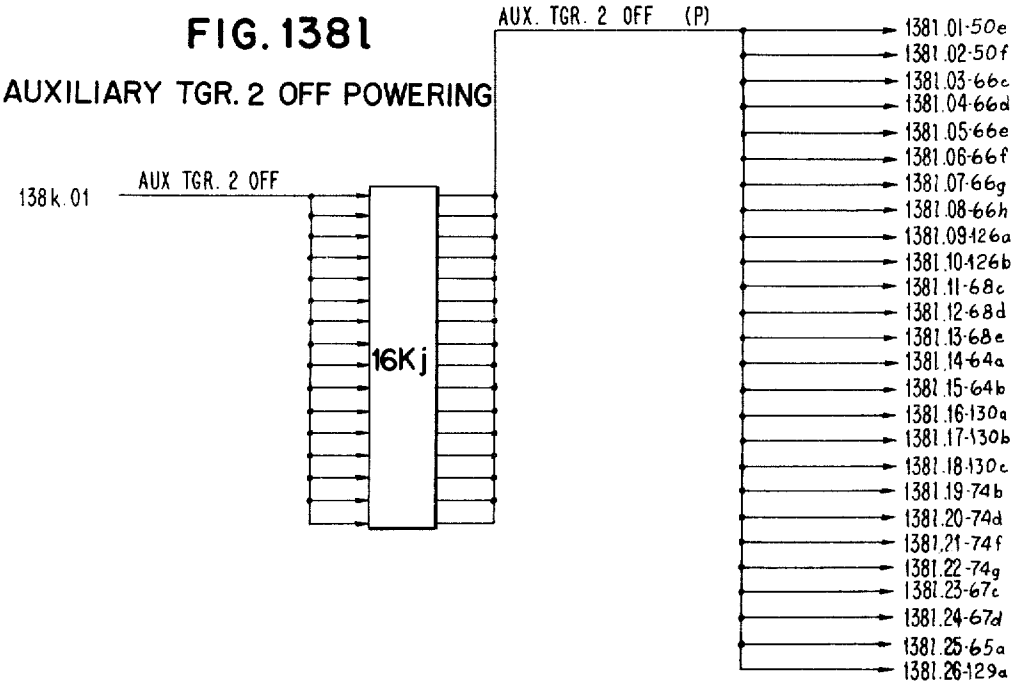


FIG. 138l

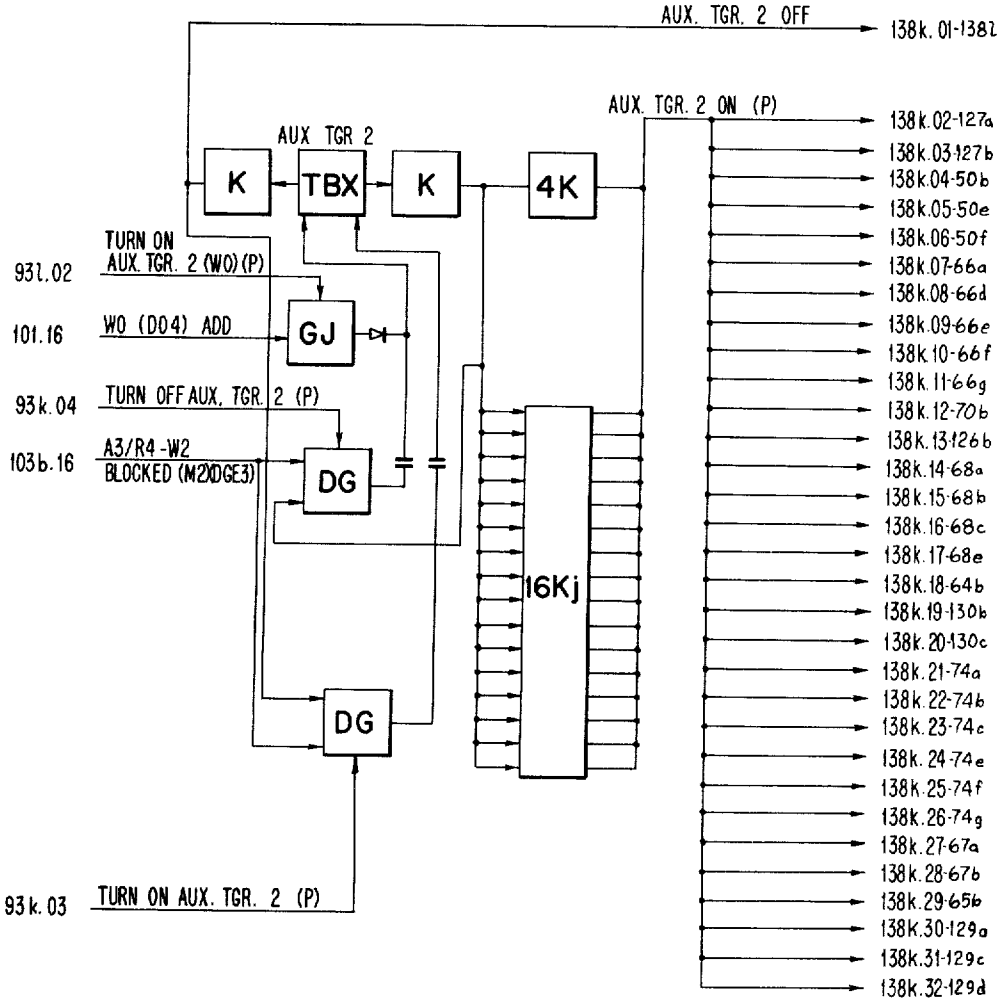
AUXILIARY TGR. 2 OFF POWERING



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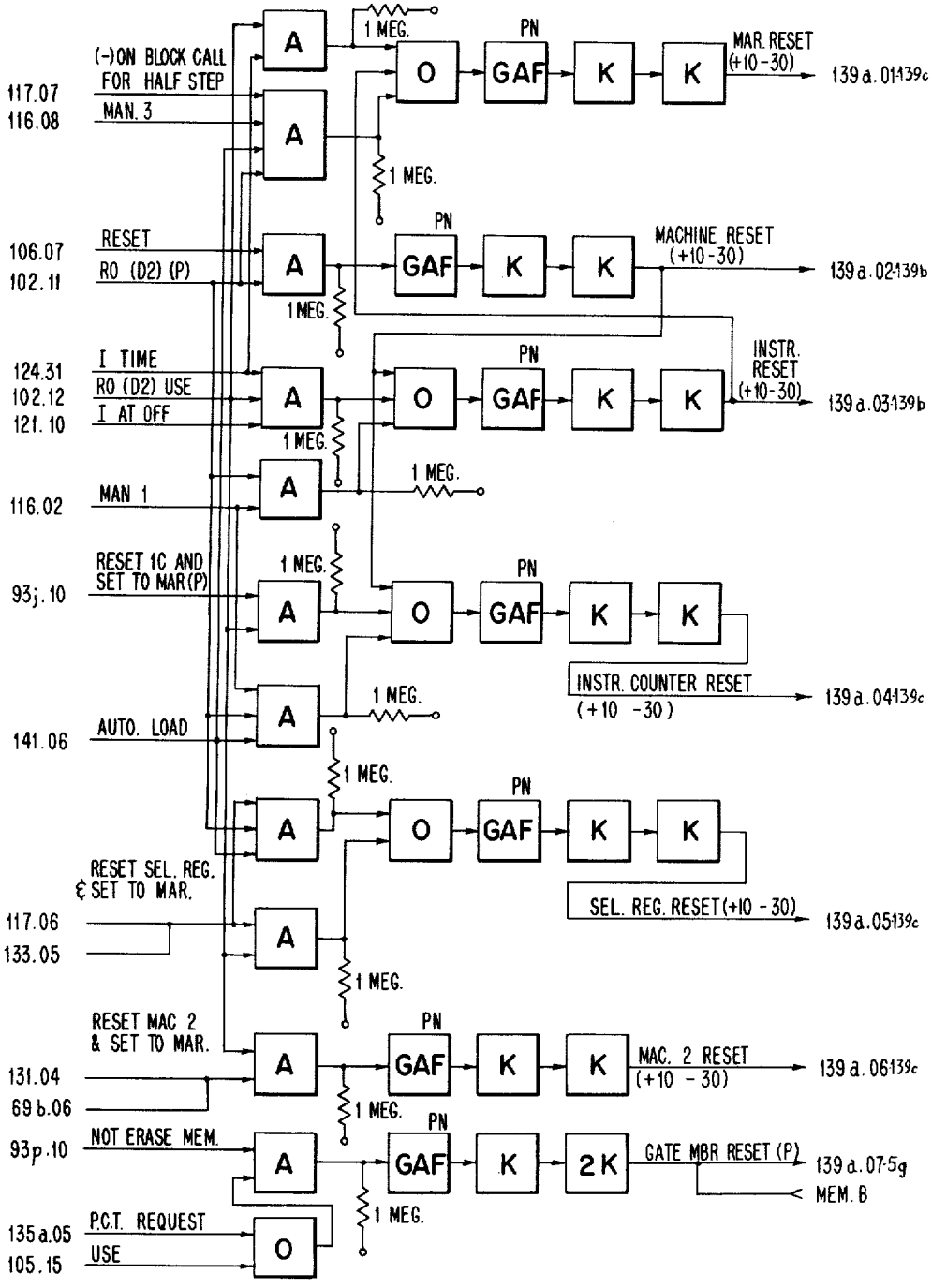
FIG. 138k

AUXILIARY TGR. 2



INSTR RESET(X) 139b.09
-12 CLAMP 139e.34

FIG. 139a
RESETS



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FIG. 139b

INSTRUCTION RESET MACHINE RESET

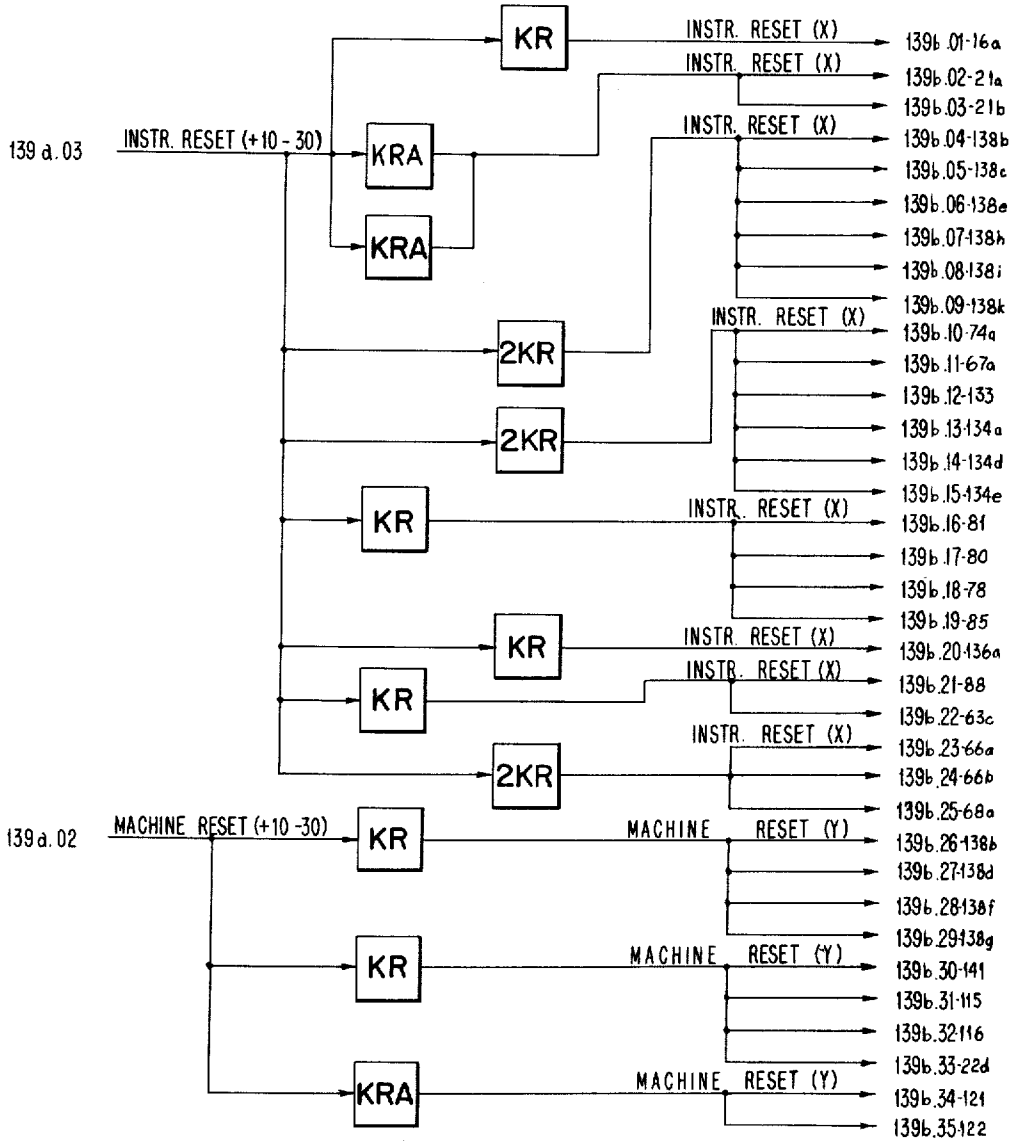


FIG. 139c

RESULT REG, MAC 2, IC, INITIAL, SELECT REG. & MAR. RESETS

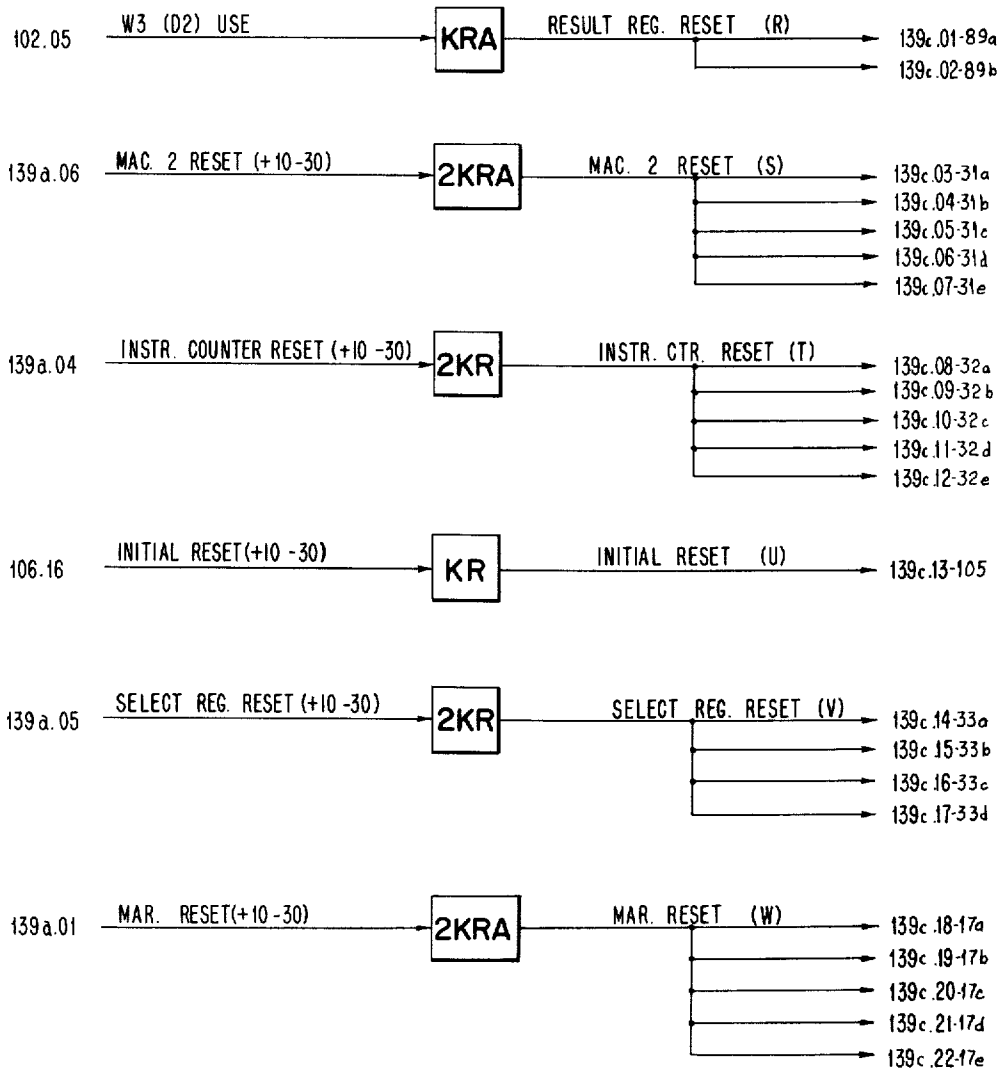
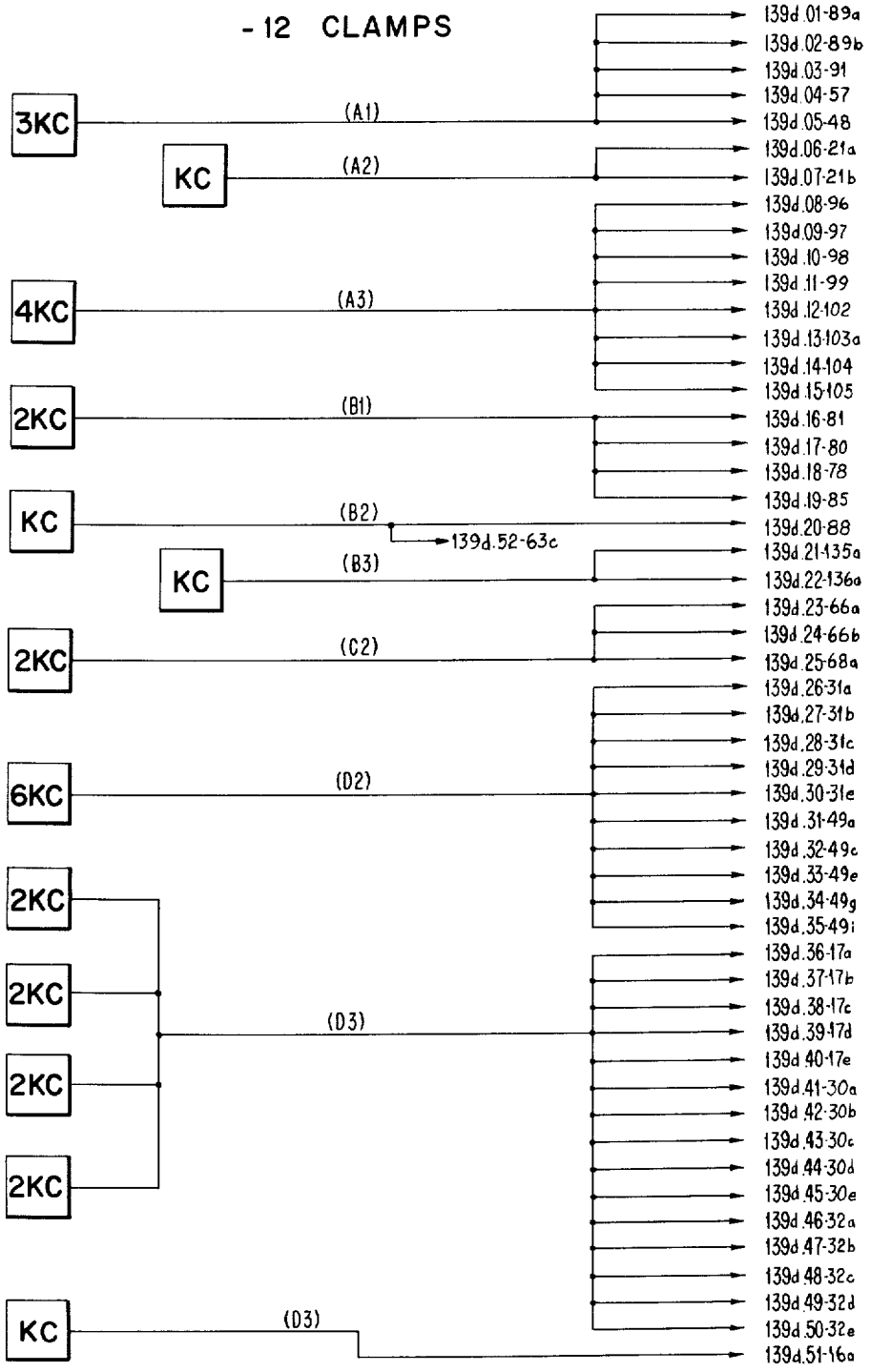


FIG. 139d

- 12 CLAMPS



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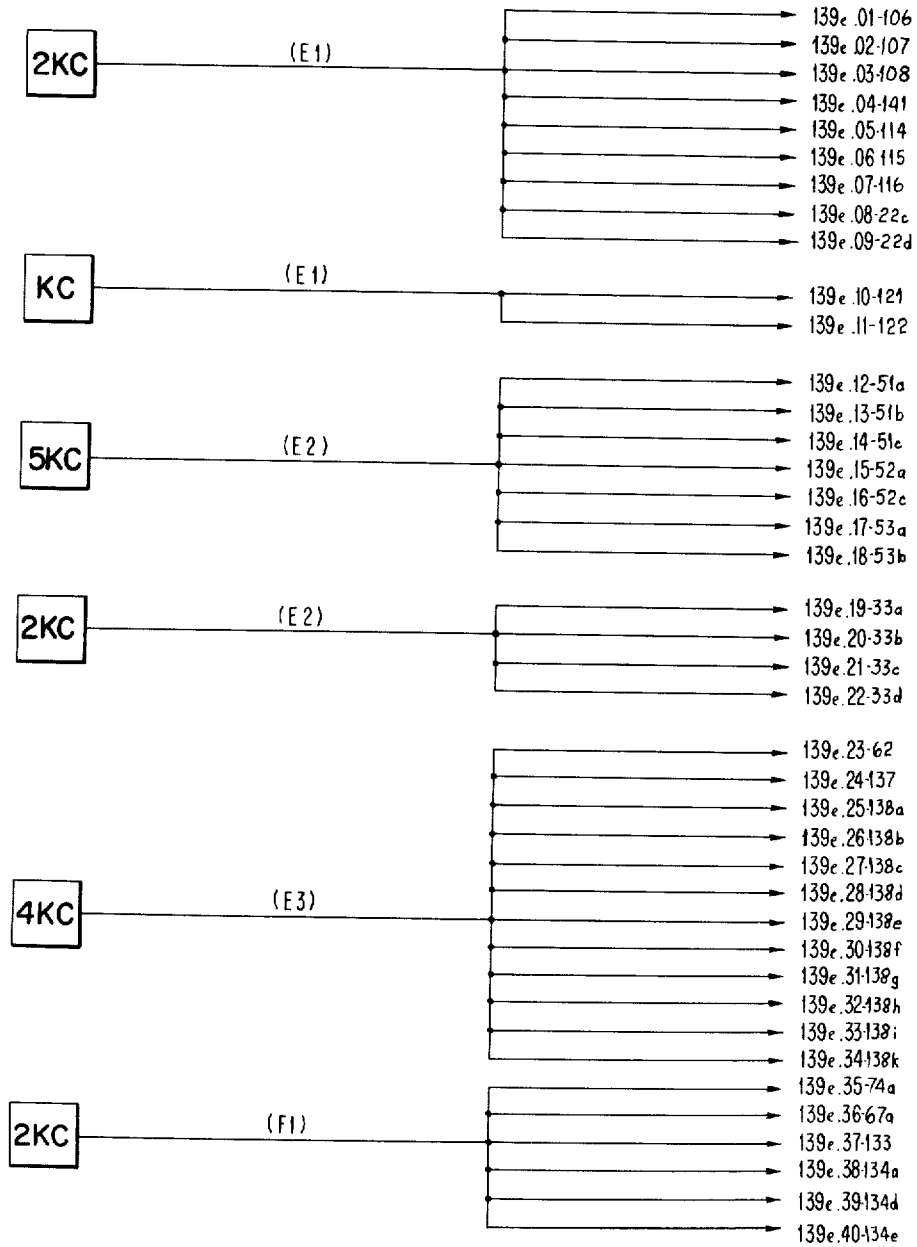
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FIG. 139e

-12 CLAMPS



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COMPARE ROUTING CONTROLS

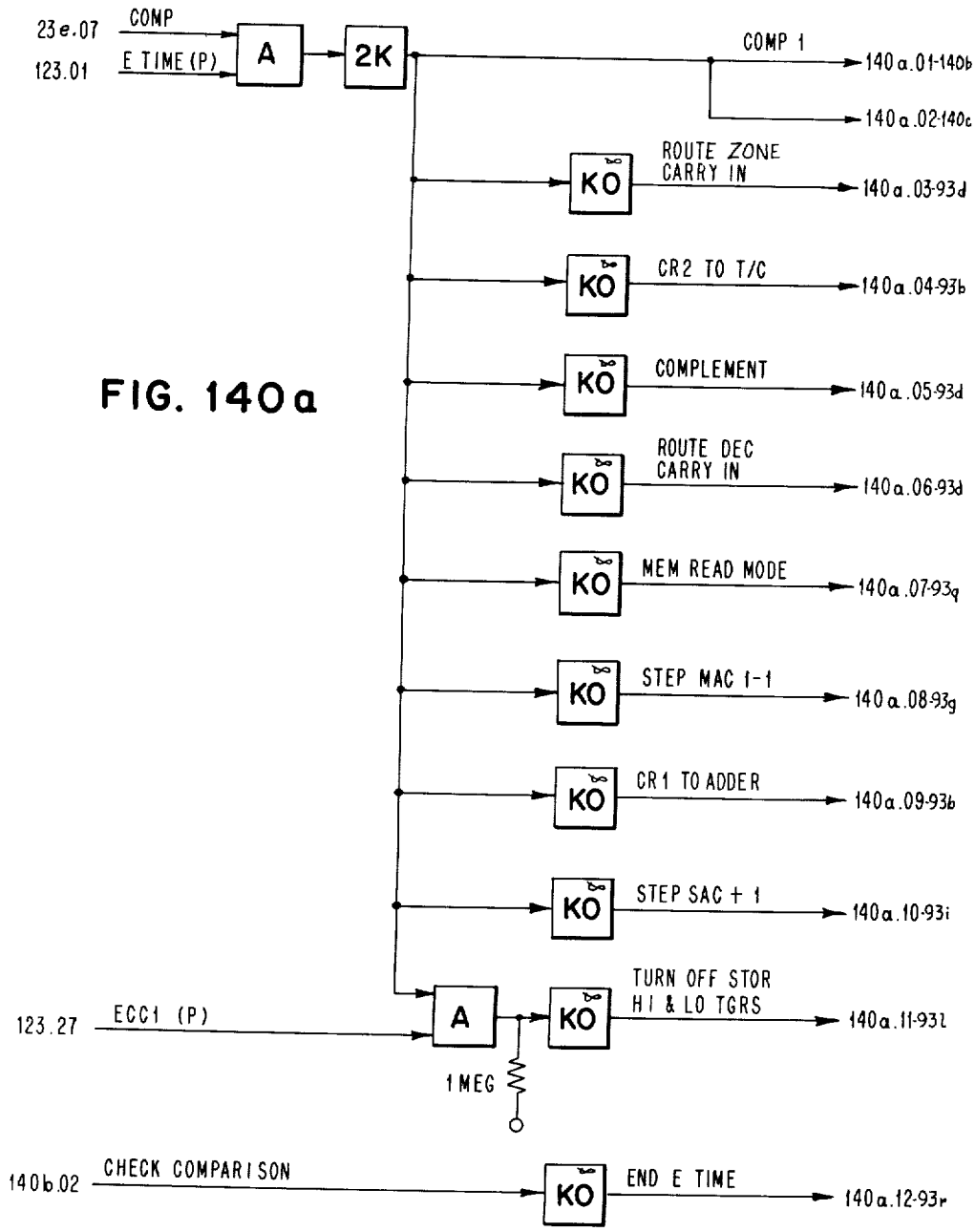
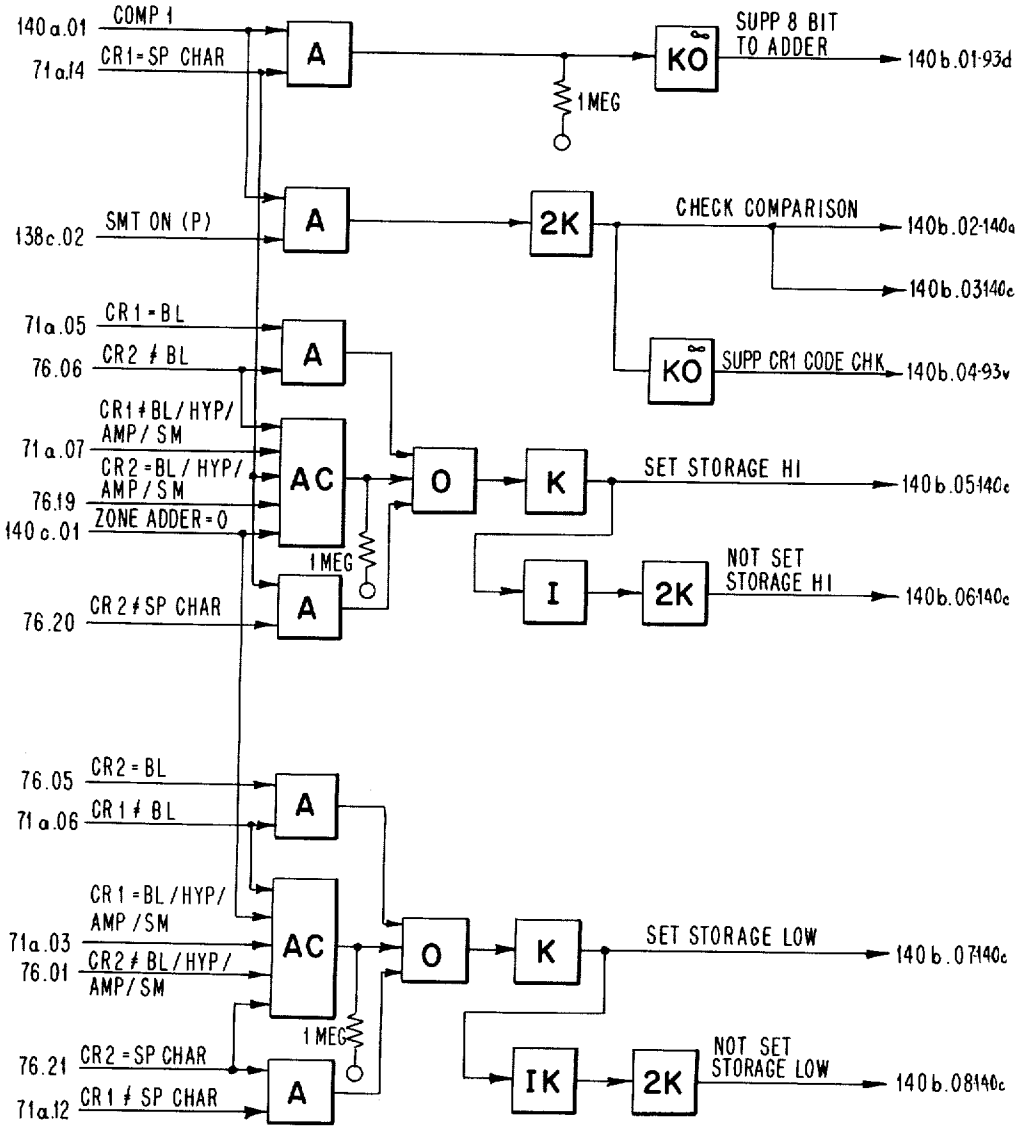


FIG. 140a

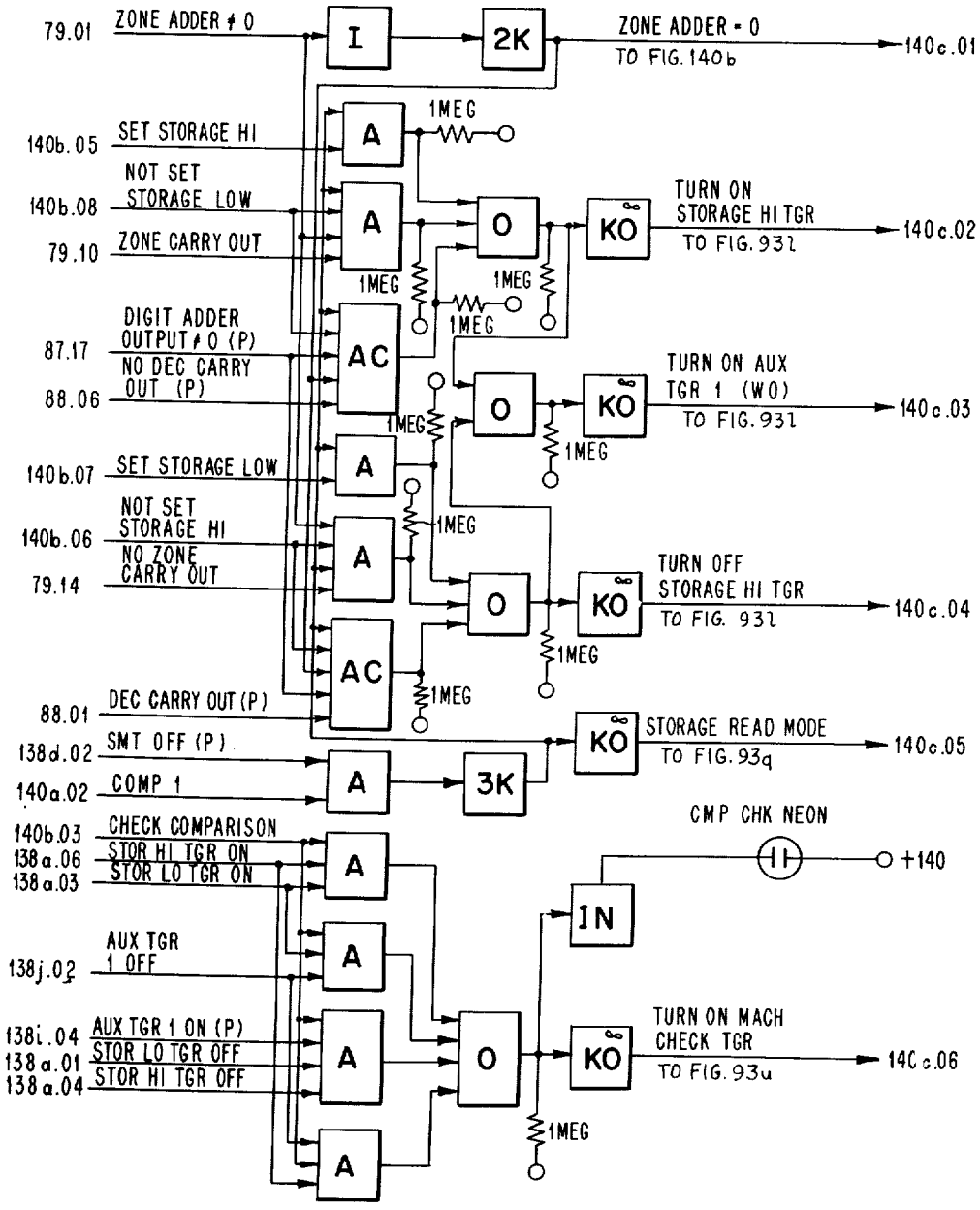
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FIG. 140b COMPARE ROUTING CONTROLS



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FIG. 140c COMPARE ROUTING CONTROLS

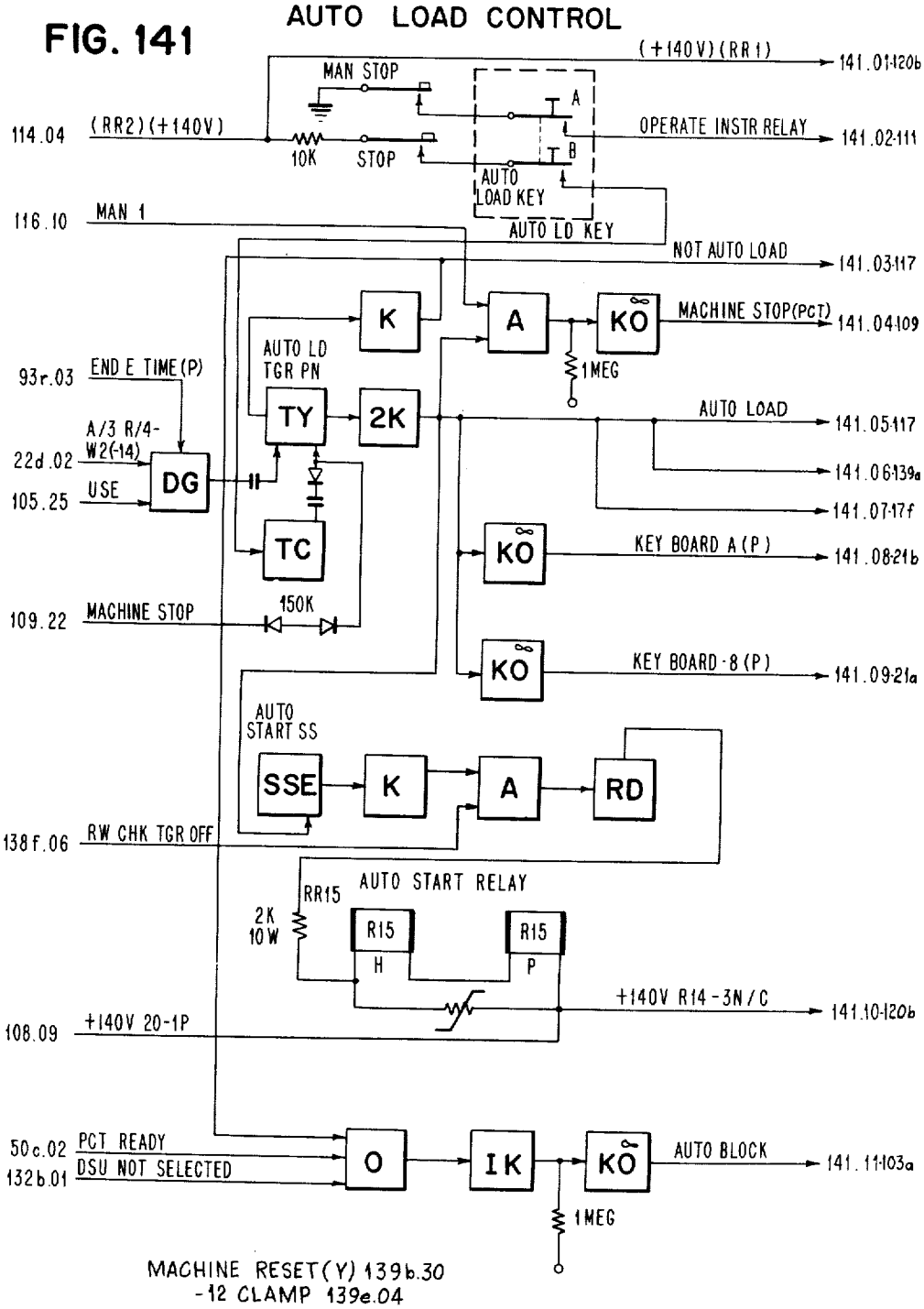


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FIG. 141



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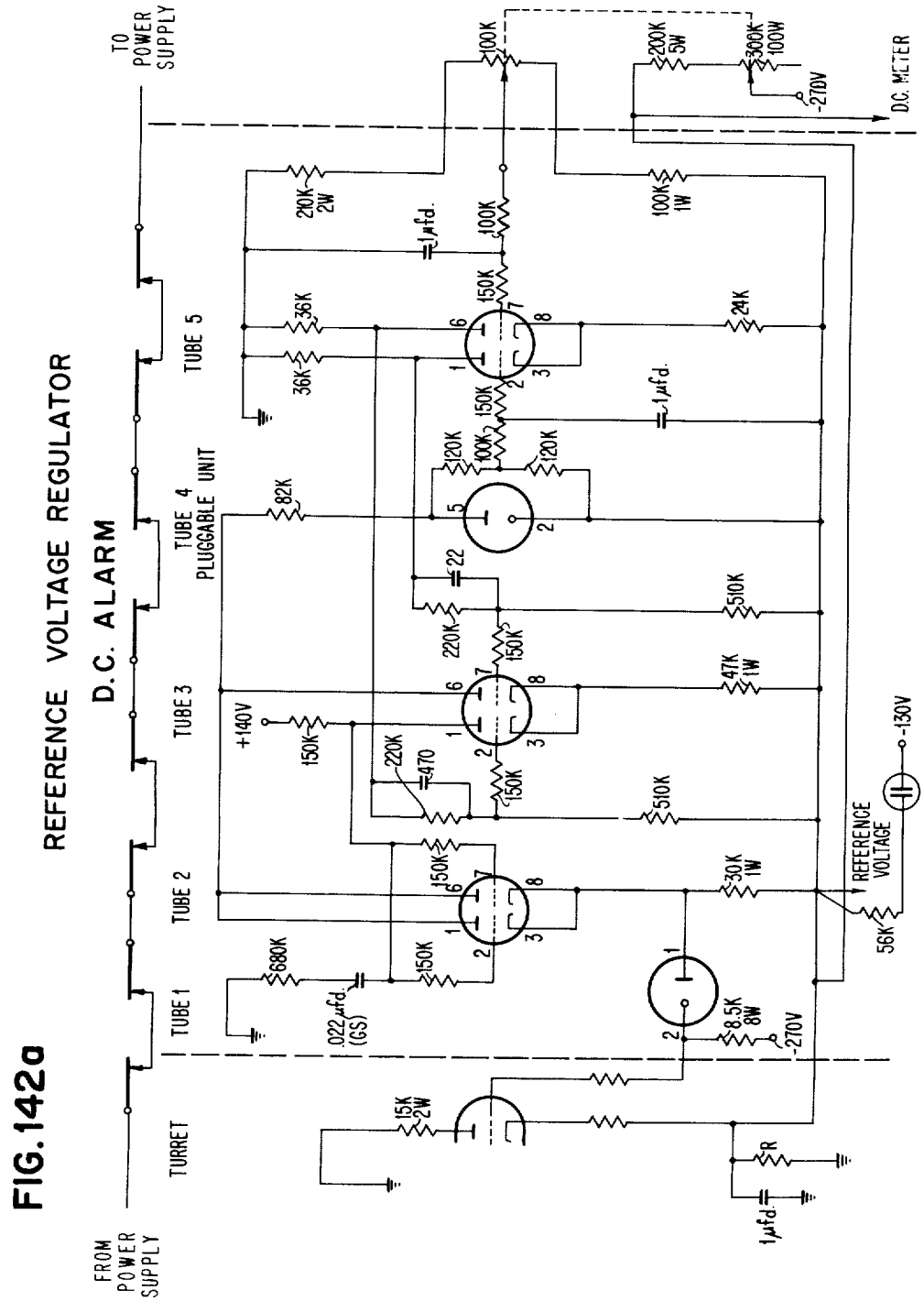


FIG. 142a

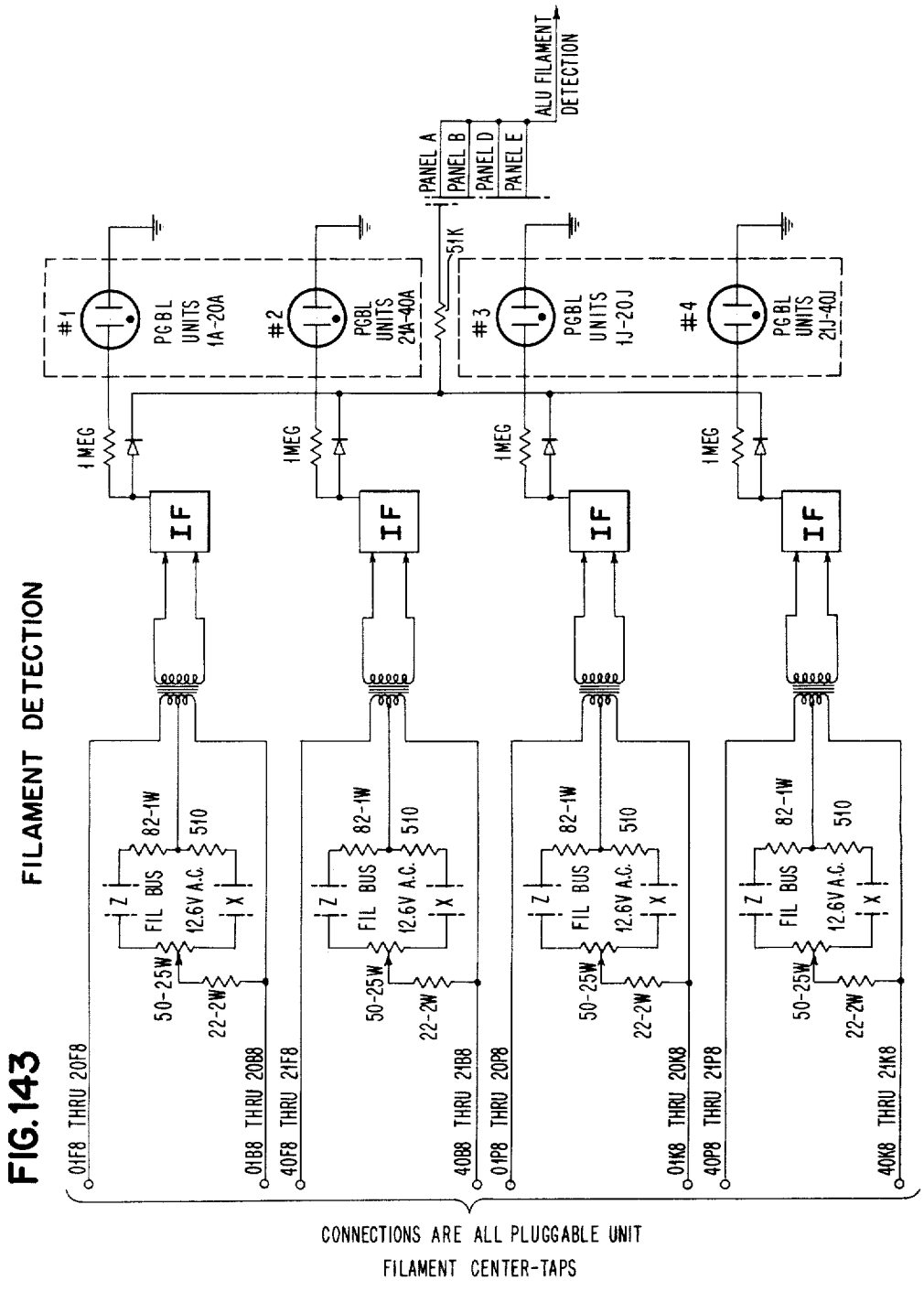


FIG. 143 FILAMENT DETECTION

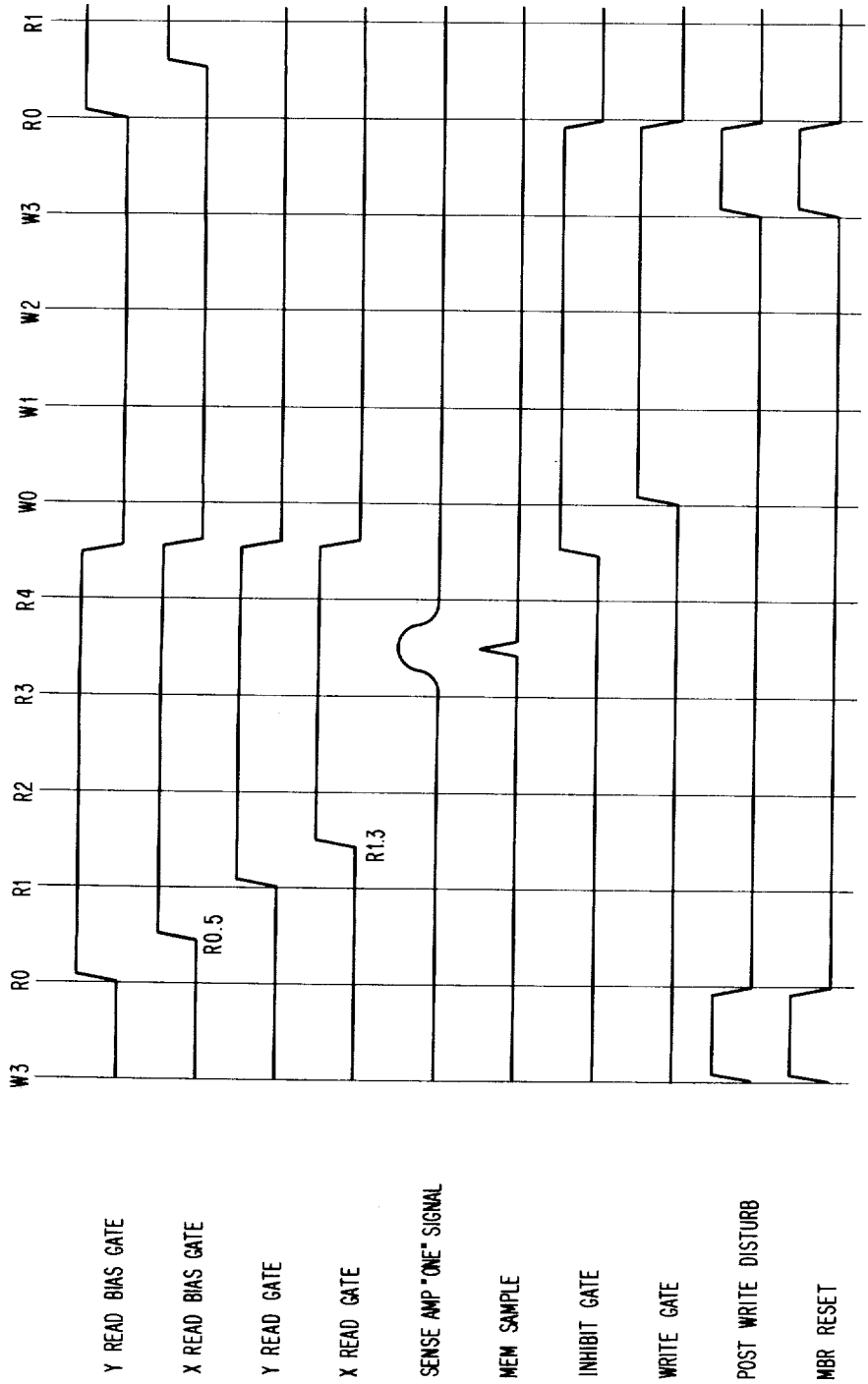


FIG. 144

MEMORY TIMING CHART

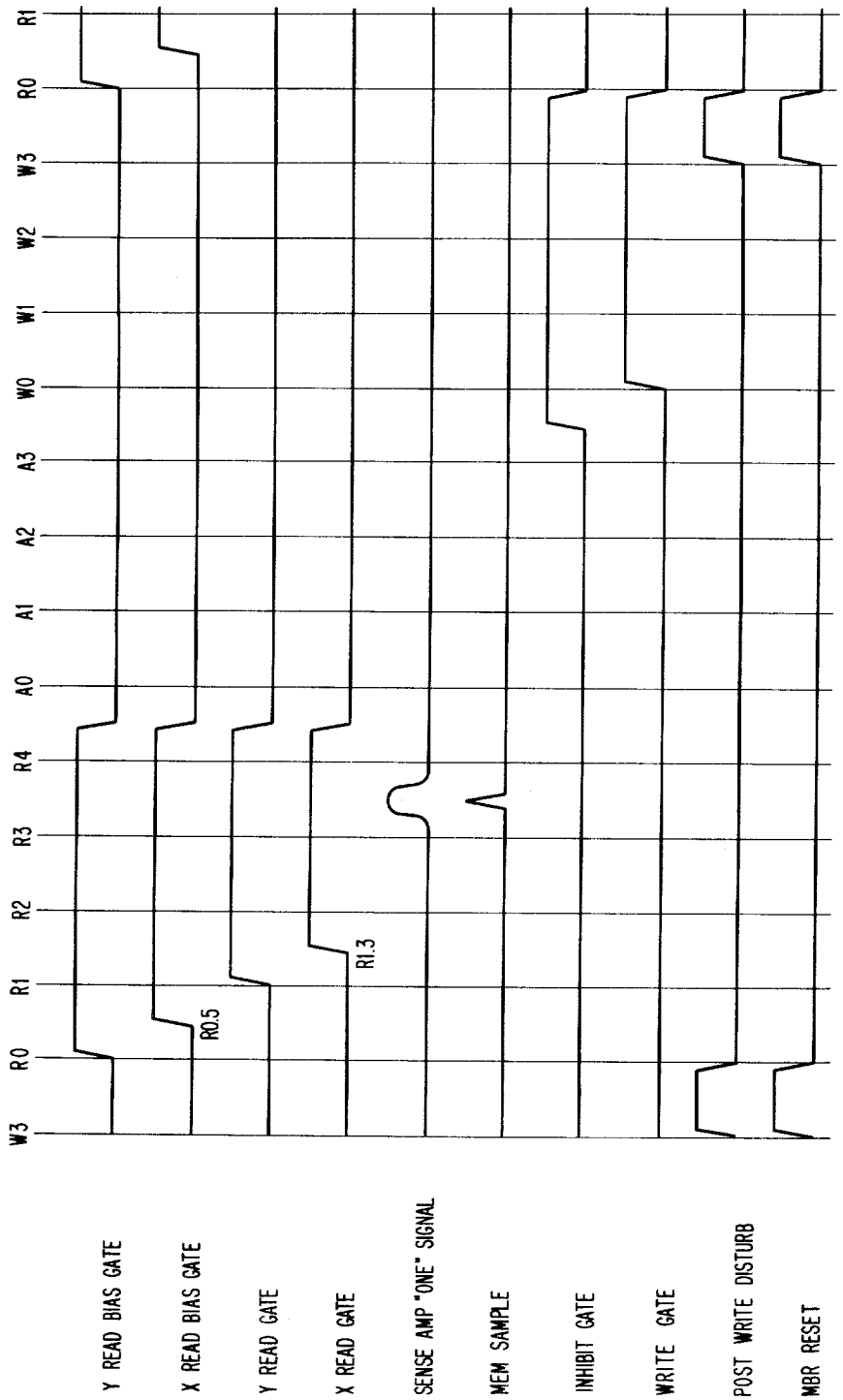


FIG. 145 MEMORY TIMING CHART

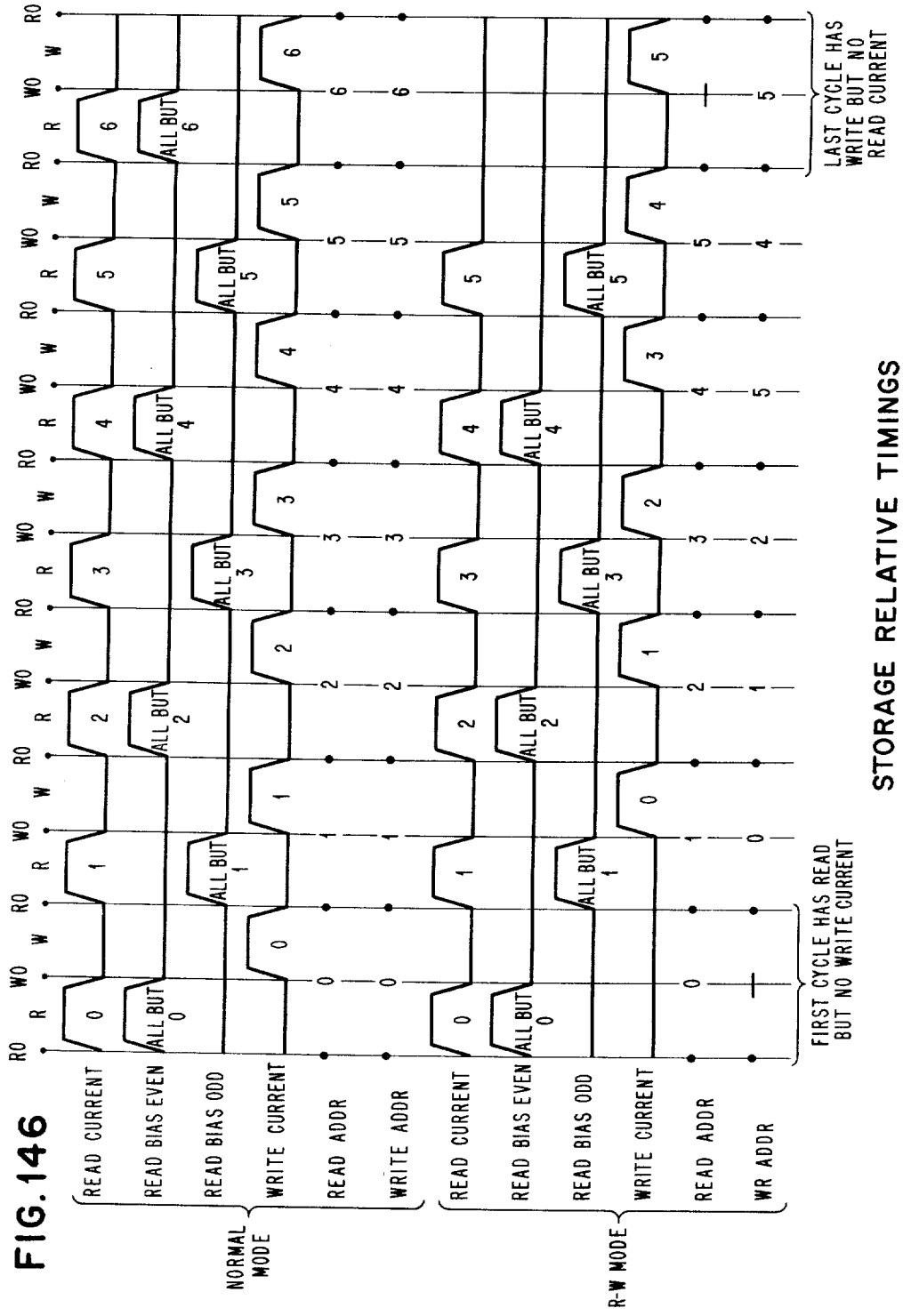
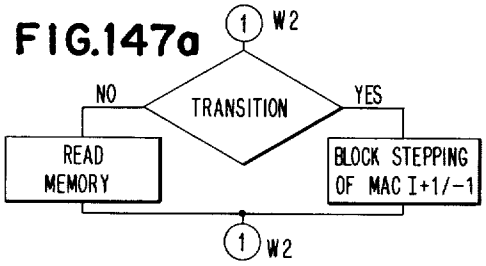

RO
R
WO
W
READ CURRENT
READ BIAS EVEN
READ BIAS ODD
WRITE CURRENT
READ ADDR
WRITE ADDR
WR ADDR
ALL BUT
NORMAL MODE
R-W MODE
FIRST CYCLE HAS READ BUT NO WRITE CURRENT
LAST CYCLE HAS WRITE BUT NO READ CURRENT
STORAGE RELATIVE TIMINGS

FIG. 146

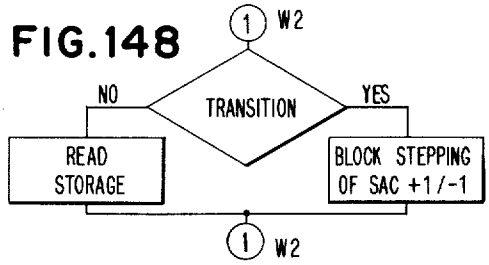
MEMORY READ MODE

FIG.147a



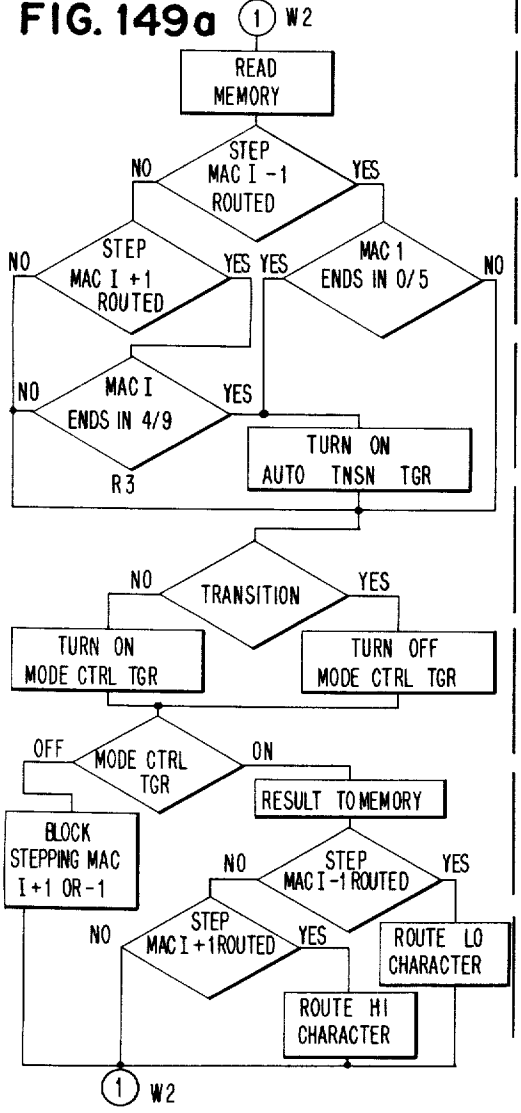
STORAGE READ MODE

FIG.148



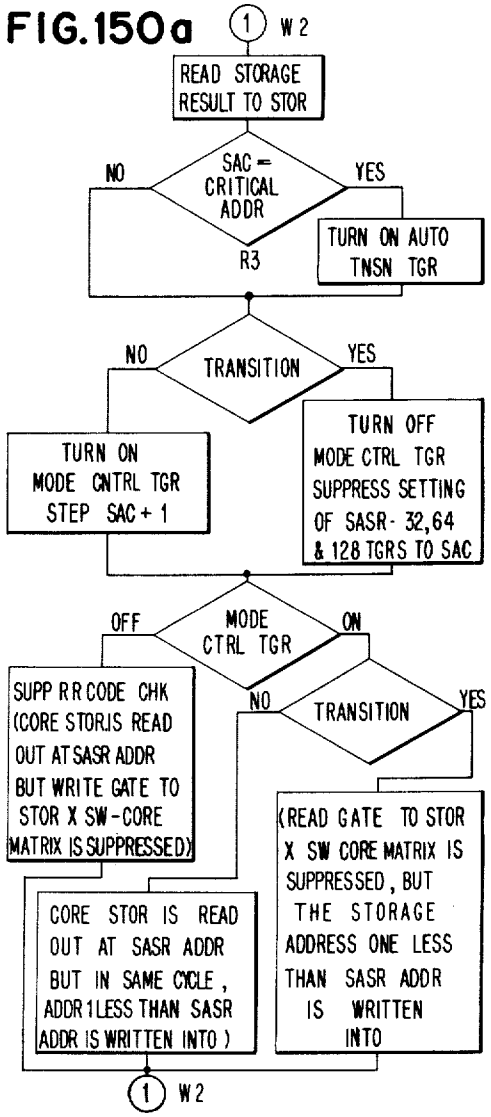
MEMORY READ-WRITE MODE

FIG. 149a



STORAGE READ-WRITE MODE

FIG.150a



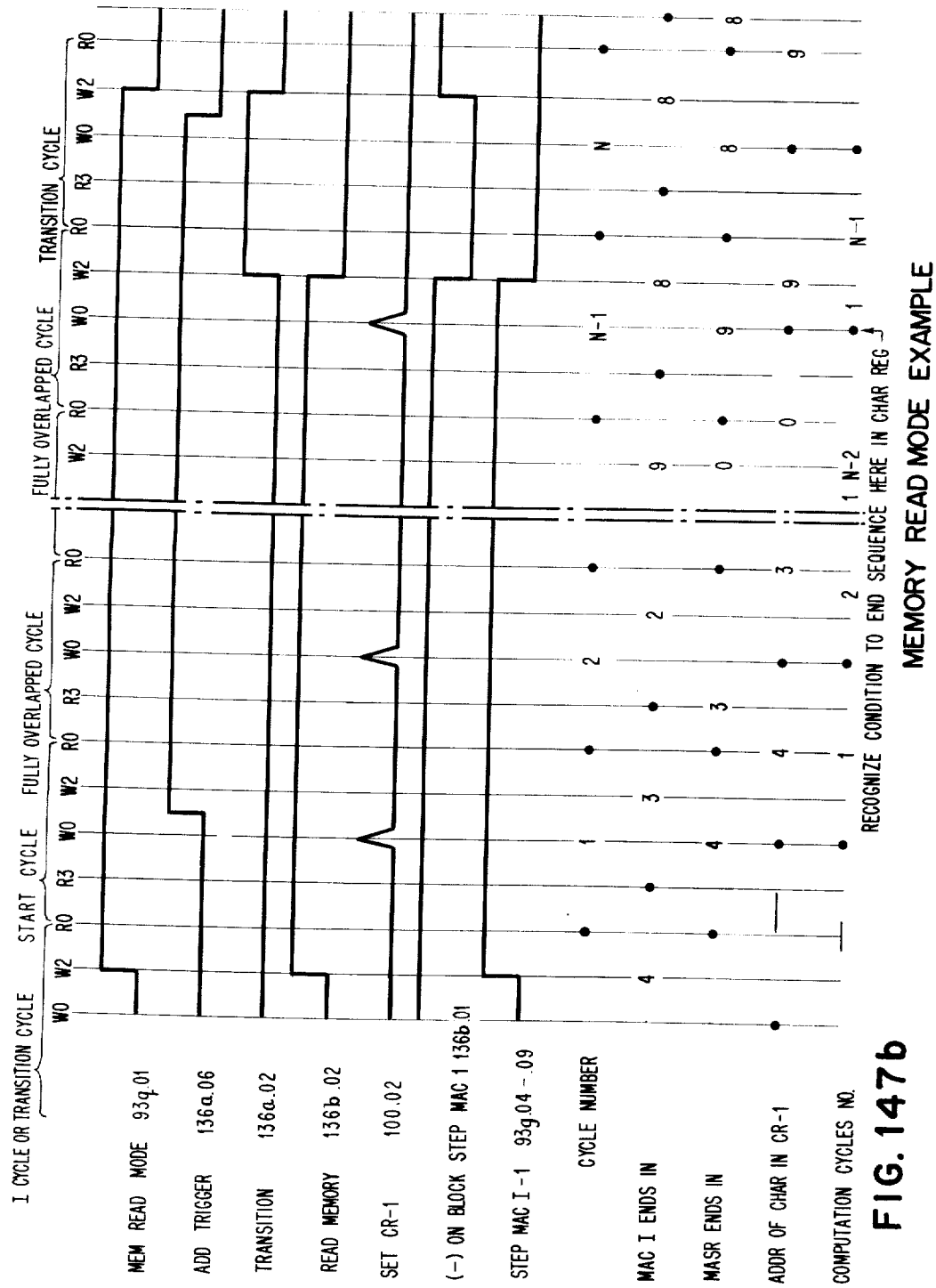
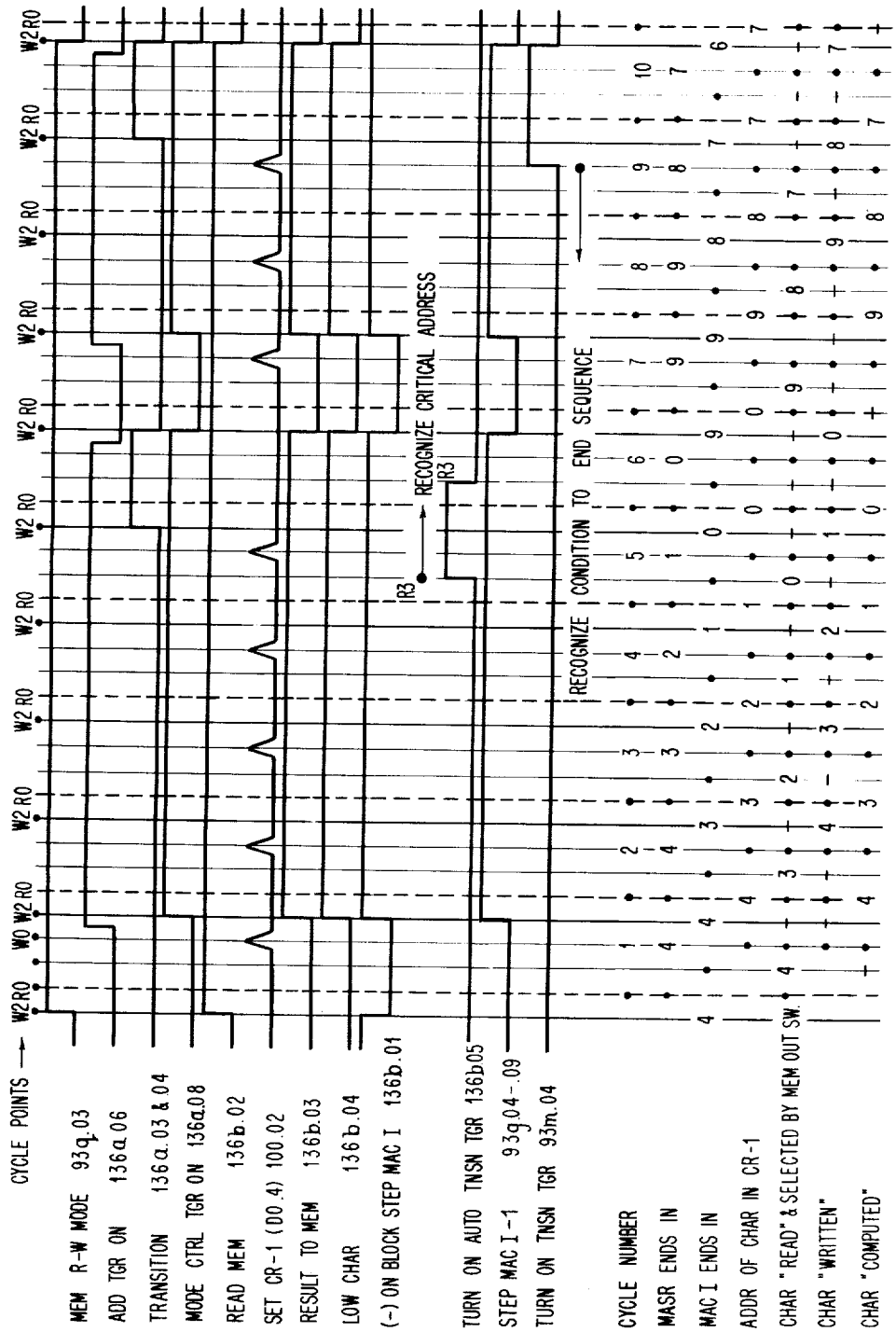

I CYCLE OR TRANSITION CYCLE
START CYCLE
FULLY OVERLAPPED CYCLE
FULLY OVERLAPPED CYCLE
TRANSITION CYCLE
W0 W2 R0 R3 W0 W2 R0
MEM READ MODE 93q.01
ADD TRIGGER 136a.06
TRANSITION 136a.02
READ MEMORY 136b.02
SET CR-1 100.02
(-) ON BLOCK STEP MAC 1 136b.01
STEP MAC I-1 93g.04 - .09
CYCLE NUMBER
MAC I ENDS IN
MASR ENDS IN
ADDR OF CHAR IN CR-1
COMPUTATION CYCLES NO.
RECOGNIZE CONDITION TO END SEQUENCE HERE IN CHAR REG
MEMORY READ MODE EXAMPLE

FIG. 147b

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MEMORY READ-WRITE MODE

FIG. 149b

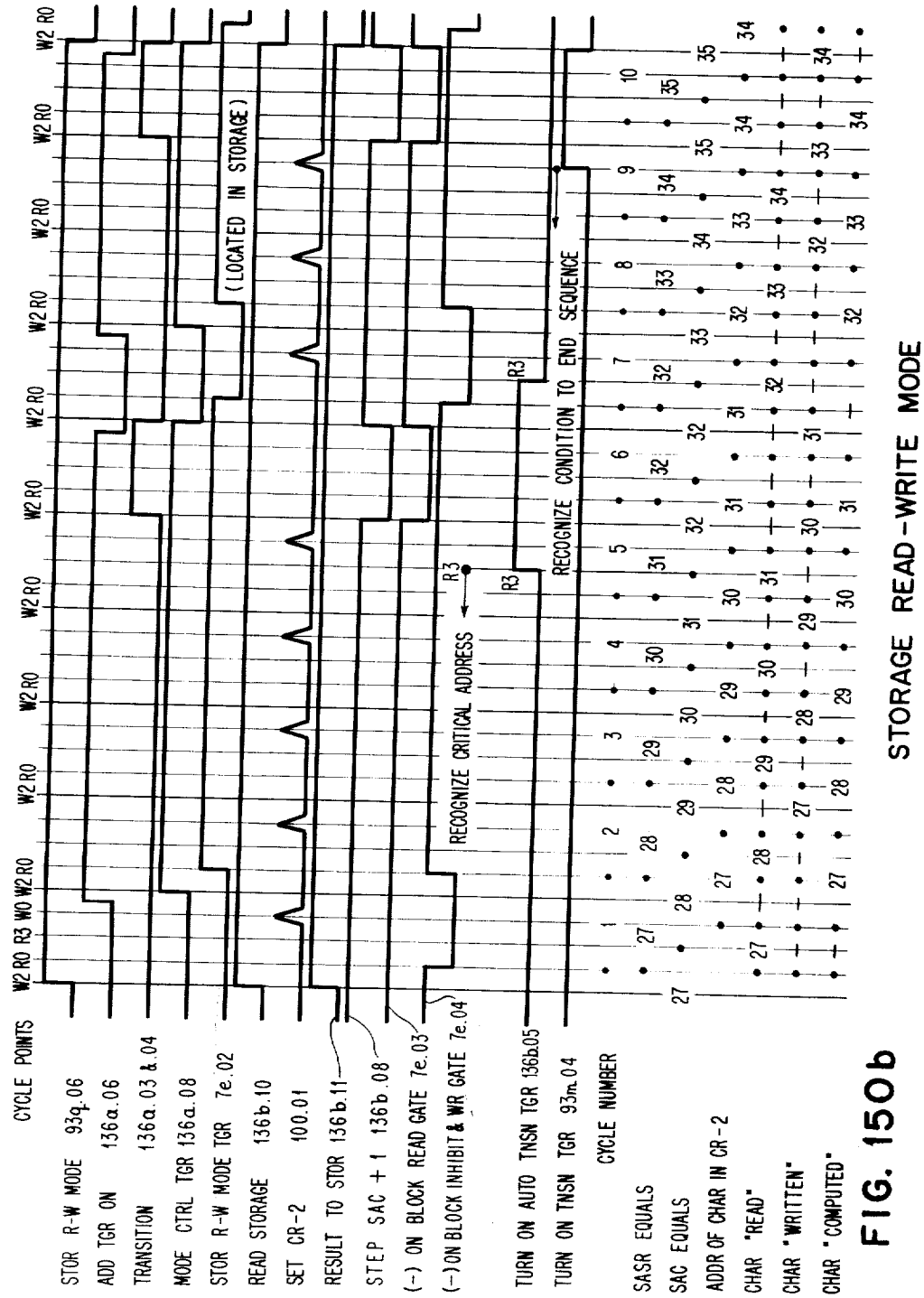


FIG. 150b

STORAGE READ-WRITE MODE

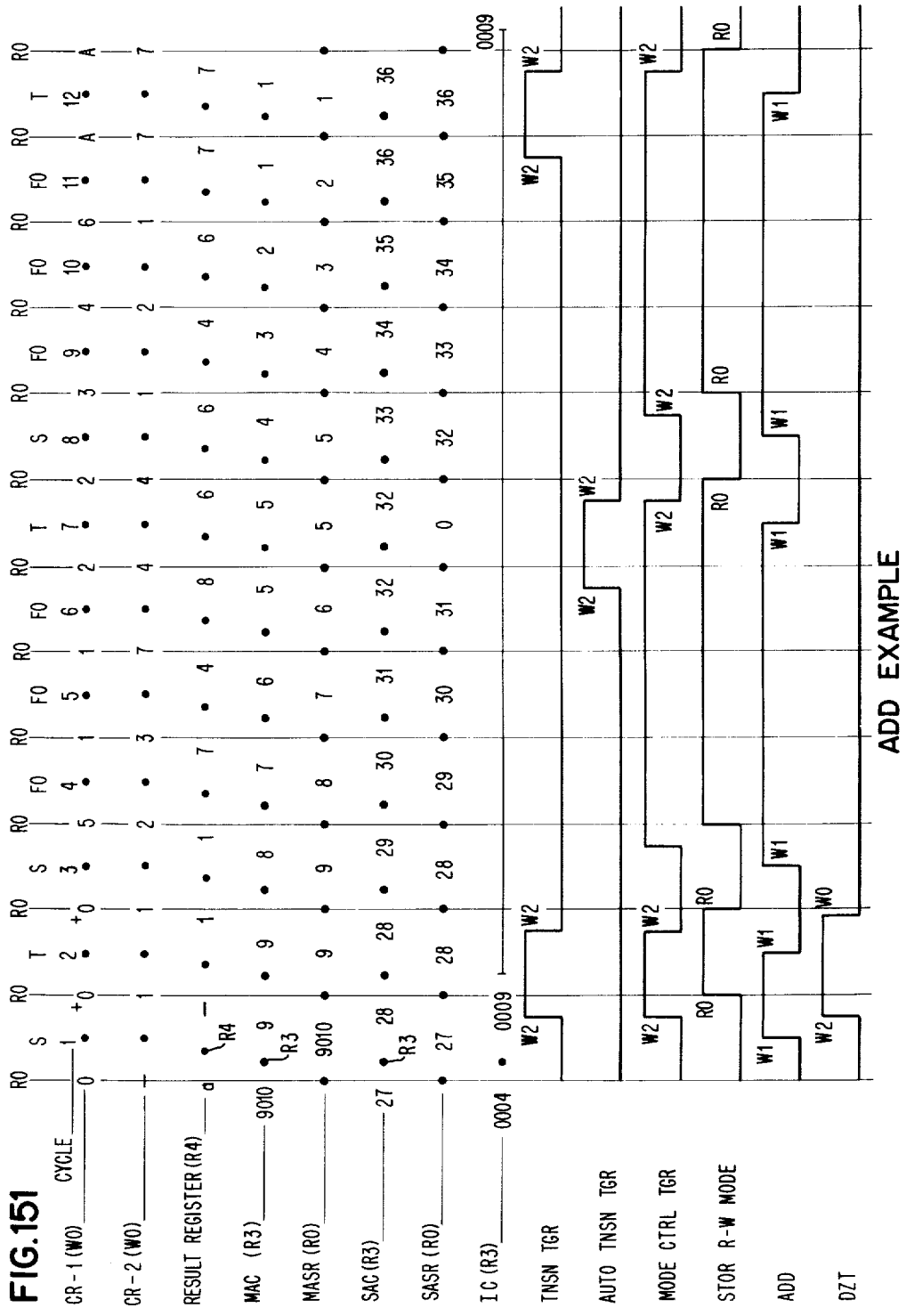

CYCLE
CR-1 (WO)
CR-2 (WO)
RESULT REGISTER (R4)
MAC (R3)
MASR (RO)
SAC (R3)
SASR (RO)
IC (R3)
TNSN TGR
AUTO TNSN TGR
MODE CTRL TGR
STOR R-W MODE
ADD
DZT
ADD EXAMPLE

FIG. 151

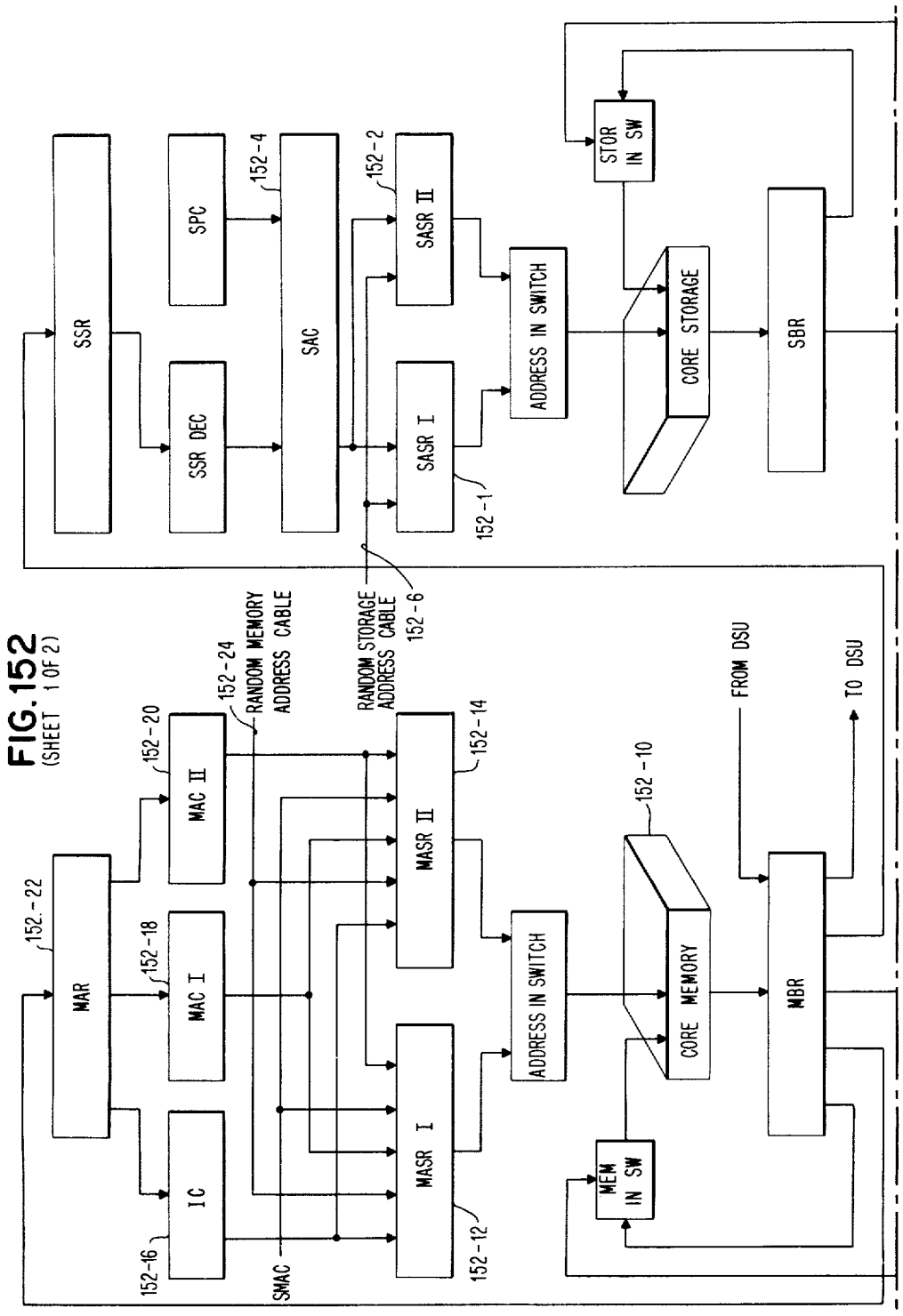


FIG. 152
(SHEET 1 OF 2)

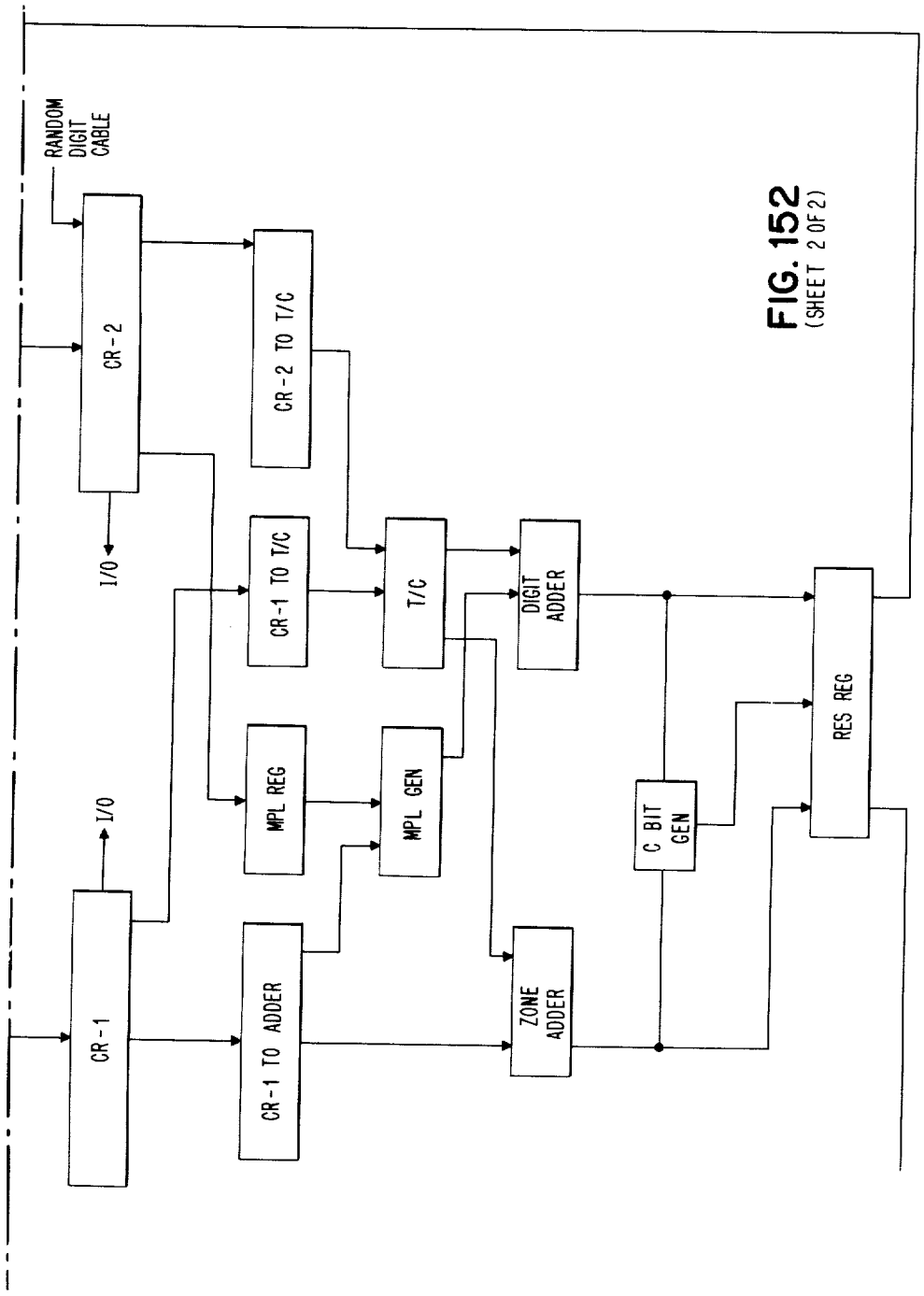
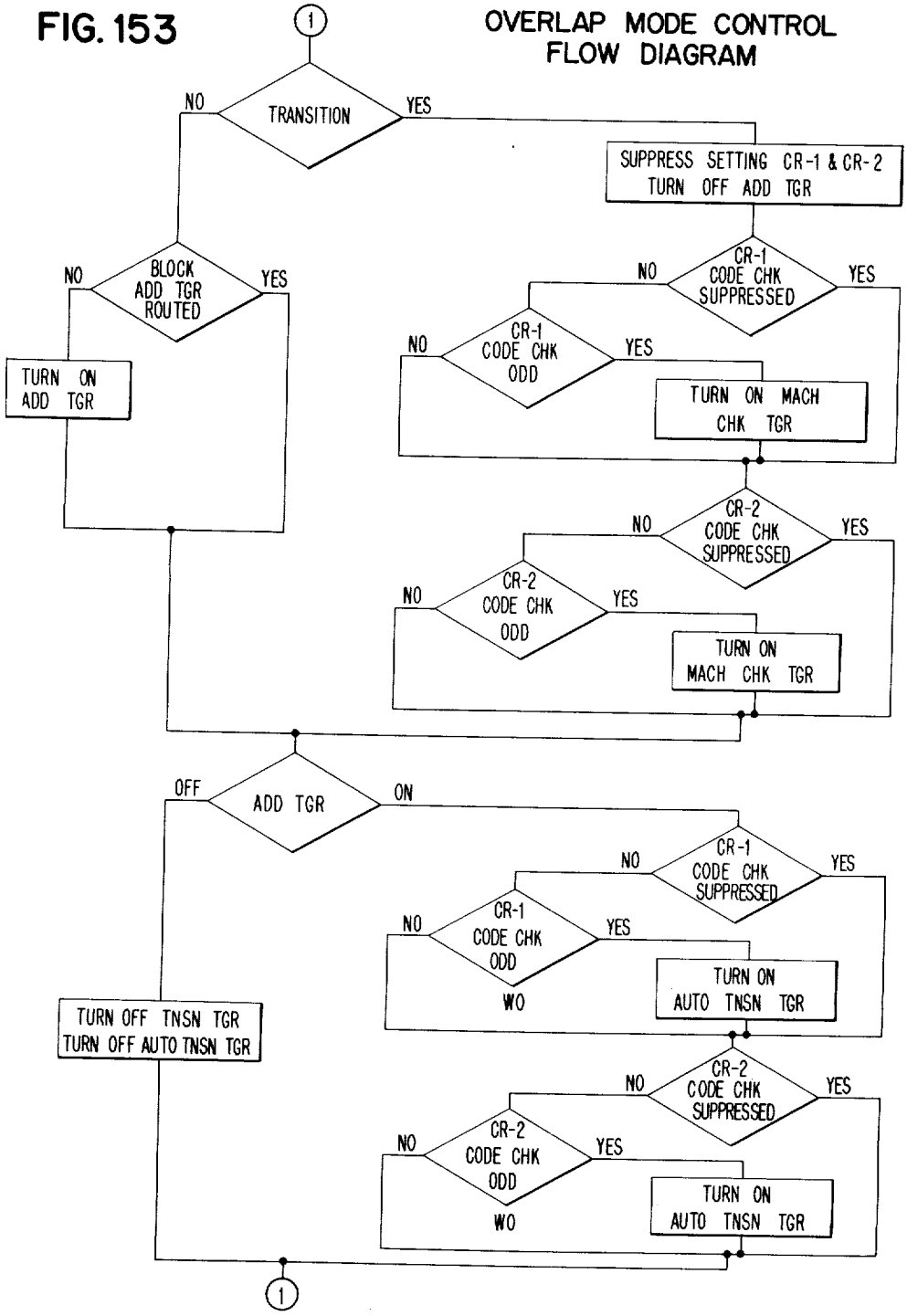


FIG. 152
(SHEET 2 OF 2)

FIG. 153

OVERLAP MODE CONTROL FLOW DIAGRAM



United States Patent Office 3,027,081
Patented Mar. 27, 1962

3,027,081

OVERLAP MODE CONTROL

Oliver D. Evans, West Park, and Frank B. Hartman, Poughkeepsie, N.Y., assignors to International Business Machines Corporation, New York, N.Y., a corporation of New York

Filed Jan. 2, 1959, Ser. No. 784,496
22 Claims. (Cl. 235—157)

This invention relates to electronic apparatus and more particularly to such apparatus which is especially useful in the operation of electronic data processing systems.

The apparatus of the invention, as described herein, employs an array of magnetic cores as principal storage designated Core Memory. It also employs an array of magnetic cores as temporary storage designated Core Storage, the latter being divided into two sections, one section comprising Accumulator Storage and another comprising Auxiliary Storage.

Characters, each of seven bits (C, B, A, 8, 4, 2, 1) with the numeric bits being coded in the binary coded decimal notation and each character in an addressable location, are combined to form words or fields whose address in Core Memory or Storage is usually designated by addressing the least significant character of the particular word or field. In Storage, the end of a field is identified by storing a Storage Mark (SM) character adjacent the most significant character in the field. In Core Memory, the sign of the field is indicated by special zoning in the A and B positions of the least significant digit. This special coding of a character in one field also serves to demarcate the length of an adjacent field or word stored at a preceding address.

The electronic data processing system provided herein is controlled by a program of instructions stored in Core Memory which prescribe the operations to be performed and the locations of data in Core Memory, which data is to be manipulated in accordance with these instructions. Instructions comprise five characters and are extracted from Core Memory and decoded to control circuits which carry out the execution of the instruction originally obtained from Core Memory before selecting another instruction. Programs may be entered into Core Memory in a number of ways. For example, the instruction may be punched in cards in the "IBM" code and read into Memory by means of a card reader or they may be recorded on tape and entered in Memory therefrom.

The Computer per se comprises Storage, arithmetic circuits and various registers which, under control of the instruction, are employed to process data which may be words, fields or portions of instructions whereby characters are added, subtracted, multiplied, revised and so forth and act on portions of instructions as if they were data. The characters may be numeric, non-numeric or mixed. Since the binary coded decimal (BCD) notation is employed for numerical information, the result of arithmetic operations on two characters may require correction which is automatic when such correction is required. It is to be noted that many of the basic elements of the Data Processing System assume one or the other of two stable states as described later and are therefore particularly well suited for the binary system of notation where one specified state is indicative of a binary "one" and the other state is indicative of a binary "zero."

The basic cycle of the machine is an Execution Character Cycle (ECC) which includes a Read portion and a Write portion. The Read portion is the time required to read a character from Core Memory and/or Storage into a Character Register. The Write portion is the time required to write or store a character or characters in Core Memory and/or Storage. The total duration of an Execution Character Cycle is nine microseconds of which

the first five microseconds comprises the Read portion and the latter four microseconds comprises the Write portion.

An Instruction Cycle, which is the time required to obtain a word from Core Memory and prepare for the operation specified by the instruction, has a duration of thirteen microseconds. For the Instruction Cycle, the Read and Write portions of the basic cycle are used and an additional four microseconds is inserted to provide a total duration of thirteen microseconds.

The stored program mentioned above contains as many Instructions as necessary to perform the intended data processing operation. The five characters of the Instruction consist of four characters designating the Address, called the Address Portion, and one character designating the Operation, called the Operations Portion. In the stored program computer of the present invention, the computer has no way of distinguishing between Instructions and Data except by the time of occurrence, either during Instruction (I) or Execute (E) time when it reads the information. If the computer is in Instruction time, then the information received from Core Memory is an Instruction; if it is Execute time, then the information is data to be operated upon. Upon completion of read-out of an Instruction, the apparatus proceeds to Execute time which consists of a number of Execution cycles, the number depending upon the length of the particular field being processed and the particular Instruction being executed.

The nine microsecond Execute cycles may be arithmetic or non-arithmetic cyles. Non-arithmetic cycles are defined as those cycles in which an Add trigger is Off during the entire cycle while arithmetic cycles are defined as those cycles in which the Add trigger is On during any portion of the cycle. Arithmetic cycles are referred to as Overlap Mode Control cycles for reasons which become apparent hereafter and are of three types: (1) a Start cycle, one in which data is read from Memory and Storage but a result is not returned to either Memory or Storage; (2) a Fully Overlapped cycle, one in which data is read from one Memory and one Storage address and the result of a computation begun during the previous cycle in the Arithmetic and Logical Unit (ALU) is placed in Memory or Storage at an address adjacent the one previously read from; (3) a Transition cycle, one in which, in effect, no data is read from Memory or Storage, but the result of the particular series of computations is placed in Memory or Storage. There may be a variable number of Overlap cycles between any given Start cycle and Transition cycle.

There are four modes of operation in which a reference is made to either Memory or Storage: (1) Memory Read Mode, (2) Memory Read/Write Mode, (3) Storage Read Mode, (4) Storage Read/Write Mode. These modes cause various sequences of operations to take place in accordance with the machine commands for the modes which are in effect. The Memory Read Mode (1) automatically returns to Core Memory information extracted that same cycle. The Memory Read/Write Mode (2) reads a character from an Address in Core Memory and the result of processing the character is written back into that Address in Core Memory during the following cycle. Storage Read Mode (3) automatically returns to Storage the information read-out that same cycle. The Storage Read/Write Mode (4) reads a character from an Address in Storage in a first cycle and writes the result of the processing of the character back into that address during the following or second cycle. Any one of the modes may be used simultaneously with any of the other modes except that only one Memory Mode and one Storage Mode normally occur in a given cycle. Of course, operations caused by Instructions which do not require the use of Core Memory or Core Storage

do not make use of any of these modes. Keeping in mind that the Data Processing Unit operates serially by character, data read from Memory during the Read portion of a cycle is used for computation during both the Write portion of that cycle and also during the Read portion of the following cycle. In the Memory Read/Write Mode the result of this computation is then returned to Core Memory during the Write portion of the second cycle. Therefore, computation time is the Write portion of a first cycle and the Read portion of a following cycle. The first cycle is a Start cycle since the Write part is only one-half of a computation cycle and the second cycle is a Fully Overlapped cycle as mentioned previously. The Read portion of the second cycle is used to obtain from Core Memory the next character to be operated upon, but the processing of the first character read from Core Memory is still taking place in the Arithmetic and Logical Unit (ALU) at Read time when the second character is being extracted from the second address. Thus, it can be seen that during the second cycle, comprising a Read and a Write portion, new data is being read from one Memory Address while the result of computation is written into an adjacent Memory Address. The data read during the second cycle is used for computation until the Write portion of the third cycle while the next Memory position is read from during the Read portion of the third cycle. This operation of overlapping the use of Memory and Storage with the time for computation is usually continued until the end of the data field is recognized, when the character in Memory beyond the final data character is not brought into the ALU, but the result of computation is returned to the Memory Address of the final data character during the Write portion of this last cycle. Alternately, results may be placed in Storage when using the Storage Read/Write Mode. Briefly, this invention is directed to the controls for providing the modes of operations as described above whereby operations including references to Memory and Storage and computing operations are performed simultaneously when such overlapping may be suitably done.

Accordingly, it is an object of this invention to provide apparatus for simultaneously operating a storage device and performing computations with the data extracted from the storage device.

It is an object of this invention to provide apparatus for obtaining units of data from locations in a storage device according to a predetermined plan, forming values related to each unit of data while obtaining data from other locations in the storage device, and storing the values in the storage device at the addresses corresponding to the related unit of data.

It is an object of this invention to provide apparatus for obtaining data sequentially from a first address and from a second address in a storage device, forming a result while obtaining data from the second address and storing the result so formed at the first address.

It is an object of this invention to obtain data from a storage device according to a predetermined plan as required for computation and to replace the data so obtained with computation results associated with the data according to the predetermined plan during a continuous computation period.

Another object of this invention is to provide apparatus for reading a first unit of data from a specified address, performing a computation with the first unit of data while securing a second unit of data from a different address, and then storing the results of the computation at the specified address.

Still another object of the invention is to provide apparatus for controlling a storage device which selectively reads data at particular addresses therefrom and writes data into particular addresses therein in a manner whereby data is read from and written into the same address on first and second cycles and data is read from another address in the storage device during the second cycle.

A further object of the invention is to provide controls for writing a result into a storage device at an address other than that read from in the same cycle.

Still another object of the invention is to provide controls for a storage matrix having X and Y address selection means wherein one of said selection means governs reading and writing into the matrix so that the address read from in a previous cycle is written into during a succeeding cycle.

Still another object of the invention is to provide a register for storing a plurality of information units and controls for the register to read out the units according to a predetermined pattern in machine cycles and to replace a unit so read with a result associated with the respective unit of information while performing computations with a succeeding unit read from the register.

Yet another object of the invention is to provide a storage array having X and Y selection matrices wherein one matrix stores a value associated with a group of addresses for information units and the other matrix stores a pair of values individually associated with discrete addresses in the group and controls whereby a unit of information is read during an initial cycle, a new unit of information is read from another address each succeeding cycle while a unit of information is written at the address read from the previous cycle, and finally a new unit of data is not read but a result is written at the address read from the previous cycle.

Other objects of the invention will be pointed out in the following description and claims and illustrated in the accompanying drawings, which disclose, by way of example, the principle of the invention and the best mode which has been contemplated of applying that principle.

In the drawings:

FIG. 1 is an overall block diagram illustrating generally the major components comprising the data processing system and their interconnections.

FIGS. 2*a* through 2*hhh* form the logical block diagrams of the principal data portions of the data processing system.

FIG. 2*iii* illustrates how FIGS. 2*a* through 2*hhh* inclusive, may be placed to form a composite block diagram of the major data portions of the data processing system.

FIG. 3*a* illustrates the Mem. 4×10 Decoder 1000 Order.

FIG. 3*b* illustrates the Mem. 4×10 Decoder.

FIG. 3*c* illustrates the Mem. 4×10 Decoder 100 Order.

FIG. 3*d* illustrates the Mem. 6×8 Decoder.

FIG. 3*e* illustrates the Mem. 4×5 Decoder.

FIG. 4 illustrates the Mem. "Y" Switch Core Read Drivers.

FIG. 5*a* illustrates the 4×10 Decoder Output Inverters.

FIG. 5*b* illustrates the Mem. "Y" Switch Core Write Drivers.

FIG. 5*c* illustrates the Mem. "Y" Switch Core Write Drivers.

FIG. 5*d* illustrates the Memory Write Gate & Memory Inhibit Gate.

FIG. 5*e* illustrates the Memory Read Gates & P.W.D. Control.

FIG. 5*f* illustrates the Memory Read Bias Gate & Mem./P.C.T. Sample Control.

FIG. 5*g* illustrates the Memory Gate Powering & M.B.R. Reset.

FIG. 5*h* illustrates the Memory Clamps & Sense Amp. Bias Voltage.

FIG. 5*i* illustrates the Storage Sample Pulse Generator.

FIG. 6 illustrates the Mem. X Switch Core Read Drivers.

FIG. 7*a* illustrates the 6×8 Decoder Output Inverters.

FIG. 7*b* illustrates the Mem. X Switch Core Write Drivers.

FIG. 7*c* illustrates the Mem. X Switch Core Write Drivers.

FIG. 7*d* illustrates the Stor. Read Bias GT, Read GT, Inhibit GT, Write GT & Buff. Reg. Reset.

FIG. 7*e* illustrates the Storage R/W Mode Ctrl.

FIG. 8 illustrates the Y Switch Core Matrix.

FIG. 9 illustrates the "X" Switch Core Matrix.

FIG. 10 illustrates the Mem. Input Select.

FIG. 11*a* illustrates the Mem. Input Switch Char. 4, 3, 2.

FIG. 11*b* illustrates the Mem. Input Switch Char. 0 & 1.

FIG. 12*a* illustrates the Mem. Inhibit Driver Circuits Char. 4, 3 & 2.

FIG. 12*b* illustrates the Mem. Inhibit Driver Circuits Char. 0 & 1.

FIG. 13 illustrates the Memory Core Plane To Terminating Resistors.

FIG. 14*a* illustrates the Memory Buffer Register Char. 4, 3 & 2.

FIG. 14*b* illustrates the Memory Buffer Register Char. 0 & 1.

FIG. 15a illustrates the Upper Sense Amplifier Circuits (Typical of all Char. 4, 3 & 2 Sense Ampl.).

FIG. 15*b* illustrates the Lower Sense Amplifier Circuits (Typical of all Char. 0 & 1 Sense Ampl.).

FIG. 16*a* illustrates the Storage Select Register.

FIG. 16*b* illustrates the Storage Selector.

FIG. 17*a* illustrates the 1st Order of Mar.

FIG. 17*b* illustrates the 2nd Order of Mar.

FIG. 17*c* illustrates the 3rd Order of Mar.

FIG. 17*d* illustrates the 4th Order of Mar.

FIG. 17*e* illustrates the 5th Order of Mar.

FIG. 17*f* illustrates the Memory Address Register Controls.

FIG. 18*a* illustrates the P.C.T. Write Busses Char. 4, 3 & 2.

FIG. 18*b* illustrates the P.C.T. Write Busses Char. 1 & 0.

FIG. 19*a* illustrates the Memory Buff. Reg. Code Check Char. 4, 3, 2.

FIG. 19*b* illustrates the Memory Buff. Reg. Code Check Char. 1, 0.

FIG. 19*c* illustrates the Memory Buff. Reg. Code Check Output.

FIG. 20*a* illustrates the Memory Output Select.

FIG. 20*b* illustrates the Output Switch Char. 1 & 0.

FIG. 20*c* illustrates the Output Switch Char. 4 & 3.

FIG. 20*d* illustrates the Output Switch Char. 2 & Memory Out Bus.

FIG. 20*e* illustrates the Memory Sample Pulse Generator & P.C.T. Sample Pulse Gen. & M.B.R. Sample Pulse Generator.

FIG. 21*a* illustrates the Operation Register 1, 2, 4, 8 Tgrs.

FIG. 21*b* illustrates the Operation Register A, B, C Triggers.

FIG. 22*a* illustrates the Manual Keyboard.

FIG. 22*b* illustrates the Keyboard Outputs.

FIG. 22*c* illustrates the Keyboard Restore Controls.

FIG. 22*d* illustrates the Key Depressed Trigger.

FIG. 23*a* illustrates the Operation Zone Decoder.

FIG. 23*b* illustrates the Operation Decoder No. Op., Stop, Tr., Send.

FIG. 23*c* illustrates the Operation Decoder Set L, Tr., Hi, RWW, Sel.

FIG. 23*d* illustrates the Operation Decoder Shor., Tr., Eq, Sign Ctrl.

FIG. 23*e* illustrates the Operation Decoder Leng., Tr., PLS, RCV, Comp.

FIG. 23*f* illustrates the Operation Decoder—Round, Tr., ZRO, MPY, ST, PR.

FIG. 23*g* illustrates the Operation Decoder Store, Tr., Sig., Div., Add Mem.

FIG. 23*h* illustrates the Operation Decoder, Add, Sub., Norm. Tr., Load.

FIG. 23*i* illustrates the Operation Decoder—R, Add, R Sub., Read, Load.

FIG. 23*j* illustrates the Operation Decoder—Tr. Any, Wr. Er., Tsmt.

FIG. 23*k* illustrates the Operation Decoder LDA, BLM, TZB.

FIG. 23*l* illustrates the Operation Decoder ULA, AAM, SB.

FIG. 24 illustrates the Operation Check Circuits.

FIG. 25*a* illustrates the Memory Address Selector Keys.

FIG. 25*b* illustrates the Memory Address Selector Key Outputs.

FIG. 26*a* illustrates the Parallel Character Transmission Capable A Connector Layout.

FIG. 26*b* illustrates the I/O Signal Cable Connector Layout SP Connector Receptacle—Wiring Side.

FIG. 27 illustrates the Control Address Decoder.

FIG. 28 illustrates the SMAC Checking.

FIG. 29*a* illustrates the MASR/MAR To DSU Powering.

FIG. 29*b* illustrates the MASR/MAR To DSU Powering.

FIG. 30*a* illustrates the 1st Order of MAC 1.

FIG. 30*b* illustrates the 2nd Order of MAC 1.

FIG. 30*c* illustrates the 3rd Order of MAC 1.

FIG. 30*d* illustrates the 4th Order of MAC 1.

FIG. 30*e* illustrates the 5th Order of MAC 1.

FIG. 30*f* illustrates MAC 1 Controls.

FIG. 30*g* illustrates the MAC 1=0/5, 4/9, 1/6, MAC 1=End of Memory.

FIG. 31*a* illustrates the 1st Order of MAC 2.

FIG. 31*b* illustrates the 2nd Order of MAC 2.

FIG. 31*c* illustrates the 3rd Order of MAC 2.

FIG. 31*d* illustrates the 4th Order of MAC 2.

FIG. 31*e* illustrates the 5th Order of MAC 2.

FIG. 31*f* illustrates the MAC 2 Controls.

FIG. 32*a* illustrates the Instruction Counter Controls & 4, 9 of IC.

FIG. 32*b* illustrates the 2nd Order of IC.

FIG. 32*c* illustrates the 3rd Order of IC.

FIG. 32*d* illustrates the 4th Order of IC.

FIG. 32*e* illustrates the 5th Order of IC.

FIG. 33*a* illustrates the 1st Order of Sel. Reg.

FIG. 33*b* illustrates the 2nd Order of Sel. Reg.

FIG. 33*c* illustrates the 3rd Order of Sel. Reg.

FIG. 33*d* illustrates the 4th Order of Sel. Reg.

FIG. 33*e* illustrates the Select Register Controls.

FIG. 33*f* illustrates the ALU Sel. Reg. Decoder.

FIG. 33*g* illustrates the ALU Sel. Reg. Decoder.

FIG. 34*a* illustrates the Storage 2×4 Decoder 128, 256.

FIG. 34*b* illustrates the Storage 2×4 Decoder 32, 64.

FIG. 34*c* illustrates the Storage 2×4 Decoder 8, 16.

FIG. 34*d* illustrates the Storage 3×8 Decoder.

FIG. 35 illustrates the X Switch Core Read Drivers.

FIG. 36*a* illustrates the 2×4 Decoder Output Inverters.

FIG. 36*b* illustrates the Y Switch Core Write Drivers.

FIG. 37 illustrates the Y Switch Core Read Drivers.

FIG. 38*a* illustrates the 3×8 Decoder Output Inverters.

FIG. 38*b* illustrates the Stor. X Switch Core Write Drivers.

FIG. 38*c* illustrates the Storage X Switch Core Write Drivers.

FIG. 39 illustrates the "Y" Switch Core Matrix.

FIG. 40 illustrates the "X" Switch Core Matrix 4×8 Diagram.

FIG. 41 illustrates the Storage Write Driver Select Circuit.

FIG. 42 illustrates the Odd-Even Gating Circuit.

FIG. 43 illustrates the Storage Input Select & Switch Ckts.
FIG. 44 illustrates the Storage Inhibit Drivers.
FIG. 45 illustrates the Storage Array.
FIG. 46 illustrates the Sense Amplifier (Storage).
FIG. 47 illustrates the Buffer Register (Storage).
FIG. 48 illustrates the CR2.
FIG. 49*a* illustrates the 1st Order of MASR.
FIG. 49*b* illustrates the 1st Order of MASR Set Circuits.
FIG. 49*c* illustrates the 2nd Order of MASR.
FIG. 49*d* illustrates the 2nd Order of MASR Circuits.
FIG. 49*e* illustrates the 3rd Order of MASR.
FIG. 49*f* illustrates the 3rd Order of MASR Set Circuits.
FIG. 49*g* illustrates the 4th Order of MASR.
FIG. 49*h* illustrates the 4th Order MASR Set Circuits.
FIG. 49*i* illustrates the 5th Order of MASR
FIG. 49*j* illustrates the 5th Order of MASR Set Circuits.
FIG. 50*a* illustrates the Transfer Routing Controls.
FIG. 50*b* illustrates the Transfer Routing Controls.
FIG. 50*c* illustrates the Transfer Routing Controls.
FIG. 50*d* illustrates the Transfer Routing Controls.
FIG. 50*e* illustrates the Transfer 01.
FIG. 50*f* illustrates the Transfer 01.
FIG. 50*g* illustrates the Transfer 01.
FIG. 51*a* illustrates the Stages 1–3 of SPC.
FIG. 51*b* illustrates the Stages 4–6 of SPC.
FIG. 51*c* illustrates the Stages 7–8 of SPC.
FIG. 52*a* illustrates the Stages 1–4 of SAC.
FIG. 52*b* illustrates the Stages 1–4 of SAC.
FIG. 52*c* illustrates the Stages 5–8 of SAC.
FIG. 52*d* illustrates the Stages 5–8 of SAC.
FIG. 52*e* illustrates the SAC Controls.
FIG. 53*a* illustrates the Storage Address Select Register Stages 1–4.
FIG. 53*b* illustrates the Storage Address Select Register Stages 5–8.
FIG. 54 illustrates the Storage Select Register Decoding.
FIG. 55*a* illustrates the SSR Decoder 1–8.
FIG. 55*b* illustrates the SSR Decoder 9–15.
FIG. 56*a* illustrates the Set Bit Routing Controls.
FIG. 56*b* illustrates the Set Bit Routing Controls.
FIG. 57 illustrates the CR–1.
FIG. 58 illustrates the CR1 Right Plate Outputs.
FIG. 59 illustrates the CR1 Left Plate Outputs.
FIG. 60 illustrates the Instruction Check Circuits.
FIG. 61 illustrates the I Time Routing Controls.
FIG. 62 illustrates the Storage Sign Tgrs. & Controls.
FIG. 63*a* illustrates the Inter-Reg. Check Routing 1.
FIG. 63*b* illustrates the Inter-Reg. Check Routing 2.
FIG. 63*c* illustrates the Inter-Reg. Check Tgr.
FIG. 64*a* illustrates the Add Address To Memory Routing Controls.
FIG. 64*b* illustrates the Add Address To Memory Routing Controls.
FIG. 64*c* illustrates the Add Address To Memory Routing Controls.
FIG. 65*a* illustrates the Unload Address.
FIG. 65*b* illustrates the Unload Address.
FIG. 66*a* illustrates the Divide Routing Controls.
FIG. 66*b* illustrates the Divide Routing Controls.
FIG. 66*c* illustrates the Divide Routing Controls.
FIG. 66*d* illustrates the Divide Routing Controls.
FIG. 66*e* illustrates the Divide Routing Controls.
FIG. 66*f* illustrates the Divide Routing Controls.
FIG. 66*g* illustrates the Divide Routing Controls.
FIG. 66*h* illustrates the Divide Routing Controls.
FIG. 66*i* illustrates the Divide Routing Controls.
FIG. 67*a* illustrates the Multiply Routing Controls.
FIG. 67*b* illustrates the Multiply Routing Controls.
FIG. 67*c* illustrates the Multiply Routing Controls.
FIG. 67*d* illustrates the Multiply Routing Controls.

FIG. 68*a* illustrates the Add To Memory Routing Controls.
FIG. 68*b* illustrates the Add To Memory Routing Controls.
FIG. 68*c* illustrates the Add To Memory Routing Controls.
FIG. 68*d* illustrates the Add To Memory Controls.
FIG. 68*e* illustrates the Add To Memory Routing Controls.
FIG. 69*a* illustrates the Sign, No Op., Receive & Stop Routing Controls.
FIG. 69*b* illustrates the Sign, No Op., Receive & Stop Routing Controls.
FIG. 70*a* illustrates the Load Address Routing Controls.
FIG. 70*b* illustrates the Load Address Routing Controls.
FIG. 71*a* illustrates the CR1 Recognition.
FIG. 71*b* illustrates the CR1 Recognition.
FIG. 72 illustrates the CR1 Code Check.
FIG. 73 illustrates the Adder Input Switching.
FIG. 74*a* illustrates the Reset Add, Reset Sub., Add-Sub. Routing Controls.
FIG. 74*b* illustrates the Reset Add, Reset Sub., Add-Sub. Routing Controls.
FIG. 74*c* illustrates the Reset Add, Reset Sub., Add-Sub. Routing Controls.
FIG. 74*d* illustrates the Reset Add. Reset Sub., Add-Sub. Routing Controls.
FIG. 74*e* illustrates the Reset Add, Reset Sub., Add-Sub. Routing Controls.
FIG. 74*f* illustrates the Reset Add, Reset Sub., Add-Sub. Routing Controls.
FIG. 74*g* illustrates the Reset Add, Reset Sub., Add-Sub. Routing Controls.
FIG. 75 illustrates the CR–2 Outputs.
FIG. 76 illustrates the CR2-Recognition.
FIG. 77 illustrates the CR2 Code Check.
FIG. 78 illustrates the Multiple Register and Decoder.
FIG. 79 illustrates the Zone Adder.
FIG. 80 illustrates the Multiplicand Doubler & Quadrupler.
FIG. 81 illustrates the Quintupler.
FIG. 82 illustrates the Multiple Selection.
FIG. 83 illustrates the True/Comp Control.
FIG. 84 illustrates the Multiple Adder.
FIG. 85 illustrates the Decimal Correction Ckts.
FIG. 86 illustrates the Digit Adder.
FIG. 87 illustrates the Decimal Correction Circuits Digit Adder.
FIG. 88 illustrates the Dec Carry Circuits & Zone Carry Tgr.
FIG. 89*a* illustrates the Result Register Mem./Storage In Bus.
FIG. 89*b* illustrates the Result Register-Mem./Storage In Bus.
FIG. 90 illustrates the C Bit Generator.
FIG. 91 illustrates the Result Register Code Check-Error Trigger.
FIG. 92 illustrates Memory Test-Character Selector.
FIG. 93*a* illustrates the Routing: Read, Storage: Read Memory.
FIG. 93*b* illustrates the Character Registers To Adder Routing.
FIG. 93*c* illustrates the Adder Out Routing.
FIG. 93*d* illustrates the Adder Carry Routing.
FIG. 93*e* illustrates the Adder Emitter and Mpl. Reg. Routing.
FIG. 93*f* illustrates the Bit To Adder Routing.
FIG. 93*g* illustrates the Step MAC 1+1 Routing.
FIG. 93*h* illustrates the Step MAC 2+1, Step MAC 1+5, Step MAC 2+5.
FIG. 93*i* illustrates the Step SAC Routing.
FIG. 93*j* illustrates the Storage, Memory and Instruction Counter Routing.
FIG. 93*k* illustrates the Auxiliary Trig's. Routing.

FIG. 93*l* illustrates the Aux. Trig. Stor. High. Trig., And Rmdr. Trig. Routing.

FIG. 93*m* illustrates the Smt. Dzt. and Tnsn. Trig. Routing.

FIG. 93*n* illustrates the Sign Chk. Tgr. Ovfl. Chk. Trig. and Stor. Sign Trig. Routing.

FIG. 93*o* illustrates the R/W Chk. Tgr. Record Chk. Tgr. and Instr. Chk. Tgr. Routing.

FIG. 93*p* illustrates the Memory Control Routing.

FIG. 93*q* illustrates the Mode Control Routing.

FIG. 93*r* illustrates the Routing: End E Time.

FIG. 93*s* illustrates the MASR Input Switching.

FIG. 93*t* illustrates the I/O Sequence Routing Control.

FIG. 93*u* illustrates the Auto Tnsn. Trig., Mach Chk. Trig. & Any Sig. Trig. Routing.

FIG. 93*v* illustrates the Block Add Tgr., Supp. Code Checking.

FIG. 93*w* illustrates the Type Cycle Neons, Par. I/O Chk. Neon, Code Chk. Neons.

FIG. 94 illustrates the P.C.T. Cable-Connector Receptacle Shown From Wiring Side.

FIG. 95 illustrates the IMC Drive Pulse Generator.

FIG. 96 illustrates the Clock Read Section of Ring.

FIG. 97 illustrates the Clock-Add Section of Ring.

FIG. 98 illustrates the Clock Write Section of Ring.

FIG. 99 illustrates the Clock-R-W/R-A-W Switching, Initial Reset.

FIG. 100 illustrates the Pulse Generator (D0.4 Pulses).

FIG. 101 illustrates the Pulse Generator A (D0.4 Pulses).

FIG. 102 illustrates the Pulse Generator (D1 & D2 Pulses).

FIG. 103*a* illustrates the Pulse Generator (D3 Pulses).

FIG. 103*b* illustrates the C. F. Pulse Power.

FIG. 104 illustrates the Pulse Generator (D3 & D4 Pulses).

FIG. 105 illustrates the Wave Form Gen. Use/Manual Status Cntl.

FIG. 106 illustrates the Manual Reset Keys.

FIG. 107 illustrates the Clear Memory Trigger.

FIG. 108 illustrates the Start Stop Controls.

FIG. 109 illustrates the Stop Controls.

FIG. 110 illustrates the Manual Store Controls.

FIG. 111 illustrates the Manual Instruction Controls.

FIG. 112 illustrates the Manual Display Controls.

FIG. 113 illustrates the Memory Test Controls.

FIG. 114 illustrates the Half/Multiple Step Controls.

FIG. 115 illustrates the Half Step Trigger.

FIG. 116 illustrates the Manual Timer Triggers.

FIG. 117 illustrates the Man Timer Execution Controls.

FIG. 118 illustrates the Manual Execution Controls.

FIG. 119 illustrates the Check Indicator Switches.

FIG. 120*a* illustrates the Alteration Switches.

FIG. 120*b* illustrates the Audible Signal Indication.

FIG. 121 illustrates the I/E And IA Tgrs.

FIG. 122 illustrates the ECC 1 & ECC 2 Tgrs.

FIG. 123 illustrates the I/E Timer Outputs.

FIG. 124 illustrates the I/E Timer Outputs.

FIG. 125*a* illustrates the Load, Unload, & Store Routing Controls.

FIG. 125*b* illustrates the Load, Unload & Store Routing Controls.

FIG. 125*c* illustrates the Load, Unload, & Store Routing Controls.

FIG. 126*a* illustrates the Store For Print Routing Controls.

FIG. 126*b* illustrates the Store For Print Routing Controls.

FIG. 127*a* illustrates the TSMT/Send Routing Controls.

FIG. 127*b* illustrates the TSMT/Send Routing Controls.

FIG. 128 illustrates the Blank Memory.

FIG. 129*a* illustrates the Set Left, Leng. & Norm. TR Routing Controls.

FIG. 129*b* illustrates the Set Left, Leng. & Norm. TR Routing Controls.

FIG. 129*c* illustrates the Set Left, Leng. & Norm. TR Routing Controls.

FIG. 129*d* illustrates the Set Left, Leng. & Norm. TR Routing Controls.

FIG. 130*a* illustrates the Shorten Right/Round Routing Controls.

FIG. 130*b* illustrates the Shorten Right/Round Routing Controls.

FIG. 130*c* illustrates the Shorten Right/Round Routing Controls.

FIG. 131 illustrates the R/W and Read Routing Controls.

FIG. 132*a* illustrates the Write-Write Erase Routing Controls.

FIG. 132*b* illustrates the Write-WR ER Routing Controls.

FIG. 133 illustrates the Select & Control Routing Controls.

FIG. 134*a* illustrates the I/O Sequence 1 & 2 Tgrs.

FIG. 134*b* illustrates the I/O Sequence Routing.

FIG. 134*c* illustrates the I/O Sequence Routing.

FIG. 134*d* illustrates the I/O Sequence-Read Service Call, Read Request Tgrs.

FIG. 134*e* illustrates the I/O Sequence-Write Service Call, Request Tgrs.

FIG. 134*f* illustrates the Trc Pull Down Pulse; I/O Sync Pulse.

FIG. 135*a* illustrates the Pct. Request, Chk. Smas. To MAR & MASR/MAR Gate Tgrs.

FIG. 135*b* illustrates the Pct. Request Execution Controls.

FIG. 136*a* illustrates the Overlap Control Triggers.

FIG. 136*b* illustrates the Overlap Execution Controls.

FIG. 136*c* illustrates the Transition Powering.

FIG. 136*d* illustrates the Not Transition & Add Tgr. Powering.

FIG. 136*e* illustrates the Tnsn. Tgr. Mode Ctrl. Tgr. Powering.

FIG. 137 illustrates the Result To Memory & Result To Storage Tgrs.

FIG. 138*a* illustrates the Storage Hi and Lo Triggers.

FIG. 138*b* illustrates the Simult R/W & Read Call Tgrs.

FIG. 138*c* illustrates the Storage Mark Tgr. & MAC 1=0 Tgr.

FIG. 138*d* illustrates the Any Signal Tgr. & Smt. Off.

FIG. 138*e* illustrates the Write Call, No Read, WR Response Tgrs.

FIG. 138*f* illustrates the Inst. Chk. Mach. Chk., & R/W Chk. Tgrs.

FIG. 138*g* illustrates the Record, Ovfl. & Sign-Chk. Tgrs.

FIG. 138*h* illustrates the Digit Zero Tgrs. & Remainder Tgr.

FIG. 138*i* illustrates the Auxiliary Tgr. 1.

FIG. 138*j* illustrates the Auxiliary Tgr. 1 Off Powering.

FIG. 138*k* illustrates the Auxiliary Tgr. 2.

FIG. 138*l* illustrates tthe Auxiliary Tgr. 2 Off Powering.

FIG. 139*a* illustrates the Resets.

FIG. 139*b* illustrates the Instruction Reset Machine Reset.

FIG. 139*c* illustrates the Result Reg. MAC 2, IC, Initial Select Reg. & MAR Resets.

FIG. 139*d* illustrates the —12 Clamps.

FIG. 139*e* illustrates the —12 Clamps.

FIG. 140*a* illustrates the Compare Routing Controls.

FIG. 140*b* illustrates the Compare Routing Controls.

FIG. 140*c* illustrates the Compare Routing Controls.

FIG. 141 illustrates the Auto Load Control.

FIG. 142*a* illustrates the Reference Voltage Regulator.

FIG. 142*b* illustrates the Driver Bias Voltage Regulator.

FIG. 143 illustrates the Filament Detection.

FIG. 144 is a Memory Timing Chart.

FIG. 145 is a Memory Timing Chart.

FIG. 146 illustrates Storage Relative Timings.

FIGURE 147*a* is a flow chart of Memory Read Mode.

FIGURE 147*b* is a sequence chart of Memory Read Mode Example.

FIGURE 148 is a flow chart of Storage Read Mode.

FIGURE 149*a* is a flow chart of Memory Read-Write Mode.

FIGURE 149*b* is a sequence chart of Memory Read-Write Mode.

FIGURE 150*a* is a flow chart of Storage Read-Write Mode.

FIGURE 150*b* is a sequence chart of Storage Read-Write Mode.

FIGURE 151 is a sequence chart of an Add Example.

FIGURE 152 (2 sheets) is a general block diagram of a Data Processing System.

FIGURE 153 is a general flow chart of Overlap Mode Control.

The Data Processing System or Central Processing Unit (CPU) shown in FIG. 1 includes a pair of core storage devices designated as Core Memory **1.10** and Storage **1.12**. Memory **1.10** is the principal storage area and is capable of storing and transmitting instructions and data by means of Memory Control **1.13**. All data coming into or going out of the Arithmetic and Logical Unit (ALU), shown generally at **1.14**, must eventually go through Core Memory. On a Read Memory operation, the contents of a specified location in Memory comprising five characters are placed in a Memory Buffer Register **1.16** and are retained there for further use. From the Memory Buffer Register, the Memory Out switch **1.17** determines which one of the five characters is placed in a Character Register 1 (CR 1) **1.18**. The numerical bits of CR 1 (8, 4, 2, 1) are sent either through Multiply circuits **1.20** by way of CR 1 to Adder controls **1.22**, or through the Digit Adder True Complement controls **1.24**, via CR 1 to True Complement control **1.26** to a Digit Adder **1.30**. Single characters are read from Core Storage **1.12** by means of Storage controls **1.32** and are placed in a Storage Buffer Register **1.34**. From the Storage Buffer Register, the information is moved to a Character Register 2 (CR 2) **1.36**. Since only one character at a time is read from storage as opposed to five characters being read from Memory, character selection controls such as Memory Out circuits **1.17** are not required for CR 2. The numerical bits of CR 2 (8, 4, 2, 1) are sent to the Digit Adder True Complement controls **1.24** by way of CR 2 to True Complement controls **1.38**. The numerical bits of the character contained in CR 2 are placed in a Multiply register **1.40** by way of CR 2 to Multiple Register controls **1.42**. The numerical portion of the contents of CR 1 and CR 2 are either complemented or passed unmodified to the Digit Adder **1.30** under control of Complement controls **1.43**. The numerical portion of the contents of CR 1 (**1.18**) are multiplied by the contents of the Multiply register **1.40** and passed to the Digit Adder **1.30** under control of CR 1 to Adder Switch **1.22**.

In the Digit Adder **1.30**, numbers are added in the binary form; however, circuits are arranged so that the numbers are always decimally corrected by Decimal Correction circuits **1.44** unless such correction is intentionally suppressed. The zone portion (B, A) of characters contained in CR 2 are either complemented or passed unmodified to a Zone Adder **1.48** under control of Zone Adder-True Complement controls **1.50**. The zone portion (B, A) of characters contained in CR 1 are passed via CR 1 to Adder controls **1.22** to zone Adder **1.48**. Normally, the Zone Adder does not add zone bits but merely passes such information through from either CR 1 or CR 2 (but not both) in unchanged form; however by the use of certain instructions, zone bits may be added or subtracted. The output of the Decimal Correction Circuits **1.44** and the Zone Adder **1.48** may be placed in a Result Register **1.52** with the proper redundancy bit inserted by a C bit Generator **1.54**.

The contents of the Result Register **1.52** may be stored in Core Memory **1.10** or the original characters read from Memory into the Memory Buffer Register **1.16** may be returned to Memory under control of a Memory In control **1.56**. Likewise, the contents of this Result Register **1.52** may be placed in Storage by way of Storage In controls **1.58**. If the contents of the Result Register are not sent to Storage, then the original character in the Storage Buffer Register **1.34** is returned to Storage by way of said Storage In controls **1.58**. Communication with Memory may be had with Input-Output storage units through the use of the Memory Buffer Register and Parallel Character Transfer Busses **1.60**.

The principle employed by Overlap Mode Control is that data read from Memory and/or Storage during the Read portion of the cycle is used for computation during the Write portion of that cycle and also during the Read portion of the following cycle. The result of this computation is then returned to Memory or Storage during the Write portion of the second cycle.

As a general introduction to operation of the Data Processing System, several examples of operations performed in response to typical instructions will be described with reference to FIG. 1.

EXAMPLE I—RESET AND ADD

A Reset and Add instruction enters a numerical field obtained from Core Memory **1.10** in Core Storage **1.12**. The address contained in the instruction specifies the location of the field in Memory and the particular part of Storage to be used. The Memory controls **1.13** cause the characters beginning with the lowest order character in the Memory field to be read from Memory into the Memory Buffer Register **1.16** in groups of five characters and the characters to be read serially into CR 1 (**1.18**) via the Memory Out controls **1.17**. The characters are transferred serially from CR 1 (**1.18**) to the Result Register **1.52** by way of CR 1 to Adder controls **1.22**, Multiply circuits **1.20**, Digit Adder **1.30**, and Decimal Correction circuits **1.44**. In response to the Storage Address contained in the instruction, the Storage controls **1.32** cause the characters to be entered serially in Core Storage **1.12** via Storage In controls **1.58** from the Result Register **1.52**. The transfer of characters continues until a non-numerical character has been extracted from Core Memory **1.10** and sensed in CR 1 (**1.18**). The upper limit of the Storage field is then identified with a Storage Mark. The contents of Core Memory remain unchanged.

EXAMPLE II—ADD

Considering now that a factor has been entered in Storage as described above, an Add instruction adds a numerical field from Core Memory **1.10** to the factor in Core Storage **1.12**. The address part of the Add instruction specifies the locations in Memory and the Core Storage unit which contain the numerical fields to be added. Starting with the lowest order of each numerical field, the characters are obtained from Memory and Storage and placed in CR 1 (**1.18**) and CR 2 (**1.36**), respectively. The numeric bits of the characters in CR 1 and CR 2 are transferred unmodified to the Digit Adder **1.30** and the sum is decimally corrected in Decimal Correction circuits **1.44** and placed in the Result Register **1.52**. The contents of the Result Register represents the sum of corresponding orders of the Memory and Storage fields and these contents replace the original factor in Storage.

Considering the timing of the operation just described,

after the Instruction cycle has been completed, Execution cycles, having Read and Write portions, occur in succession. During the Read portion of the first Execution cycle two characters are obtained, one from Memory and one from Storage respectively, to be added; and during the Write portion of the first cycle no result is returned to Storage since addition of the first two numbers is in progress. The Read portion of the second cycle is used to obtain the next characters to be operated upon. During the Write portion of the second cycle, when addition of the characters obtained during the first cycle has been completed, the result of such addition is written into the address, in Storage, read from during the first cycle. Overlapping of addition and Storage operations continues until the limit of the result is identified by a Storage Mark, except under certain conditions described in detail later. The contents of the Memory field remain unchanged.

EXAMPLE III—STORE

A numerical field in Core Storage **1.12** is placed in Core Memory **1.10** by a Store instruction having an address portion specifying the Storage unit from which data is obtained and the location in Core Memory at which the field is to be stored. In response to Storage controls **1.32**, numeric characters are placed in CR 2 (**1.36**) successively and transferred to the Result Register **1.52** via CR 2 to T/C controls **1.38**, Digit Adder T/C controls **1.24**, Digit Adder **1.30** and Decimal Correction cuits **1.44**. Under control of Memory controls **1.13**, the contents of the Result Register **1.52** are placed in Core Memory at successively lower locations via Memory In controls **1.56**. The transfer between Core Storage and Core Memory continues until a Storage Mark is detected. The Store Instruction does not affect the contents of the field in Core Storage.

What has been described in the examples above will be described in more detail with reference to FIG. 2 and still more specifically wtih reference to the figures which follow FIG. 2.

The character code system employed for representing information uses a seven bit code for each character. A numeric portion expresses numeric information in the binary coded decimal notation (BCD), as mentioned previously, and a zone portion, in combination with the numeric portion, expresses alphabetic and symbolic information. These seven bits are divided into the following groups:

Check	Zone	Numeric
C	B, A	8, 4, 2, 1

The bit structure of a character may be expressed by placing a line over a bit not present in a character, for example, the number five (5) is written $\overline{C}\ \overline{B}\ A\ \overline{8}\ 4\ \overline{2}\ 1$. Alternately, the characters may be expressed in binary form using a "1" to denote the presence of a bit and a "0" to denote the absence of a bit, for example, the number (5) is written 0000101. Often, it becomes convenient in the circuits to utilize the absence of a bit or bits within a character and when so doing, the bits of a character are inverted so that a "0" becomes a "1," or, for example, a line labeled $\overline{B}$ has a positive signal thereon when the B bit is "0."

The C bit or check bit is used when the number of Zone and Numeric bits in a character results in an odd sum so that, in all cases, the sum of all of the bits in the character, including a C bit, is an even amount. During the operations on information throughout the data processing system, the sum of the character bits is checked for an even total.

As shown in the examples, there is an absence of bits in the Zone positions when numeric information is represented and the value of the numeric portion is the sum of 8, 4, 2, 1 bits. When "0" is expressed, as a character, it is represented by an "8" bit and a "2" bit (0001010), but within the arithmetic and addressing units of the system, "0" is represented by the absence of bits. Alphabetic and symbolic characters are represented by combinations of Zone and Numeric bits. The following chart shows the bit configuration for each character and symbol.

Chart I

Alphabetic				Numerical			
Char	C	BA	8421	Char	C	BA	8421
A	1	11	0001	1	1	00	0001
B	1	11	0010	2	1	00	0010
C	0	11	0011	3	0	00	0011
D	1	11	0100	4	1	00	0100
E	0	11	0101	5	0	00	0101
F	0	11	0110	6	0	00	0110
G	1	11	0111	7	1	00	0111
H	1	11	1000	8	1	00	1000
I	0	11	1001	9	0	00	1001
J	0	10	0001	Numerical zero			
K	0	10	0010	0	0	00	1010
L	1	10	0011	Special Char.			
M	0	10	0100	.	1	11	1011
N	1	10	0101	□	0	11	1100
O	1	10	0110	$	0	10	1011
P	0	10	0111	*	1	10	1100
Q	0	10	1000	,	0	01	1011
R	1	10	1001	%	1	01	1100
S	0	01	0010	#	1	00	1011
T	1	01	0011	@	0	00	1100
U	0	01	0100	&	0	11	0000
V	1	01	0101	-	1	10	0000
W	1	01	0110	Blank	1	01	0000
X	0	01	0111	/	0	01	0001
Y	0	01	1000				
Z	1	01	1001				

	Char	C	BA	8421
Acc. and Drum Mark	0	0	00	0000
Plus Zero	0	0	11	1010
Minus Zero	0	1	10	1010
Record Mark		1	01	1010
Group Mark		0	11	1111
Tape Mark		0	00	1111

CYCLES

An operation period is defined as the period of time during which the Data Processing System reads, interprets and performs instructions. Character cycles are classified according to the time in which they occur during an operation. The first Character cycle, of each operation, is the Instruction Character Cycle, ICC and it is during this cycle that the five characters of an Instruction are obtained from Core Memory, the Operation code is recognized, various registers and controls are set, and the five characters comprising the Instruction are written back in the Core Memory. Following the Instruction cycle is a period defined as Execute time having a number of Execution Character cycles which depend, in part,

upon the type of Instruction. For some Instructions, the number of Execution Character Cycles varies according to the length of the fields involved, although at least one Execution Character Cycle (ECC 1) is always required. The first Execute Cycle, namely, Execution Character Cycle 1 (ECC 1), is characterized by certain special functions to prepare for succeeding operations. For example, in arithmetic instructions, the Sign must be removed from a character addressed in Memory. In the Store for Print Instruction, the first character placed in Core Memory is either a Blank or a Hyphen depending on the setting of the Sign trigger of the Storage unit. In some instances, an Execution Character Cycle 2 (ECC 2) follows an ECC 1 cycle for the primary purpose of identifying a second Execute cycle when the need arises for certain operations. Following ECC 1 or ECC 2 are as many Execute cycles as are necessary to complete the operation called for by the Instruction.

DESCRIPTION OF FIG. 2

Reference is made to FIGS. 2*a* through 2*hhh* which show, in block form, principal data portions of the Data Processing System of FIG. 1.

The convention employed in numbering lines in the logical block diagrams is as follows: from left to right, the first numbers and the letter, if any, to the period or point is the figure number from which the line originated; the next two numbers to the second point refer to a particular output line (these are usually numbered according to their positions on the originating sheet from top to bottom); and the last two numbers, when used, refer to either the character associated therewith or a particular bit within a character. In a few instances where one trigger is shown as an example of one bit position in a register of several character capacity, the output lines from the figure are numbered as follows from left to right: The first two digits and the letter, if any, refer to the figure, the next two numbers refer to a particular output line (usually numbered from top to bottom of the figure in numerical order), the next two numbers refer to the character number, and the last or right-hand number refers to the bit. For example, line X.**01.04** (B) originates in FIG. X, it is the first line at the top of the figure, and it refers to bit B of character 4. On rare occasions, a single output line is connected to several points and, thus, several lines may bear the same number. Each input line in the diagrams bears the number derived from its point of origin.

In the composite drawings of FIG. 2, data flows generally into the block at the top and out of the block at the bottom, and control lines which cause the movement of data enter the block from the left.

FIG. 2*a* illustrates the Memory Control **1.13** of FIG. 1 and comprises Memory Decoders, FIGS. 3*a* through 3*e*, Y and X Switch Core Write and Read Drivers, FIGS. 4, 5*a*, 5*b*, 5*c*, 6, 7*a*, 7*b* and 7*c* (controls comprising FIGS. 5*d*, 5*e*, 5*f*, 5*g*, 5*h*, 7*d* and 7*e* not shown in FIG. 2), and Y and X Switch Core Matrices, FIGS. 8 and 9. The Memory In switches **1.56** of FIG. 1 are shown in FIG. 2*b* and comprise Input Select control, FIG. 10, Input Switch, FIGS. 11*a* and *b*, and Memory Inhibit circuits, FIGS. 12*a*, *b* and *c*. The Core Memory **1.10** of FIG. 1 is shown in FIG. 2*b* and in detail in FIG. 13. Additionally, FIG. 2*bx* illustrates the Instruction format, and FIG. 2*by* illustrates diagrammatically windings on one of the cores of FIG. 13. The Memory Buffer Register (MBR) **1.16** of FIG. 1 is shown in FIGS. 2*c* through 2*e* as having five orders for storing five characters comprising 35 bits. The details of sample orders of the MBR are shown in FIG. 14. The Sense Amplifiers of FIG. 2*c* are shown in detail in FIGS. 15*a* and *b* and connect the sense windings of Core Memory, by cable, with the input lines of the Memory Buffer Register. As shown in FIGS. 2*c*–2*e*, lines **15***b*.**01.00** (C through 1) are connected from the Sense Amplifiers to Character 0 position of the MBR, lines **15***b*.**01.01** (C through 1) are connected to Character 1 position of the MBR, lines **15***a*.**01.02** (C through 1) are connected to Character 2 position of MBR, lines **15***a*.**01.03** (C through 1) are connected to Character 3 position of MBR, and lines **15***a*.**01.04** (C through 1) are connected to Character 4 position of MBR. Output lines **14***b*.**01.00** ($\overline{C}$ through $\overline{1}$), **14***b*.**01.01** ($\overline{C}$ through $\overline{1}$), **14***a*.**01.02** ($\overline{C}$ through $\overline{1}$), **14***a*.**01.03** ($\overline{C}$ through $\overline{1}$) and **14***a*.**01.04** ($\overline{C}$ through $\overline{1}$) are connected via cable to the Input Switch, FIG. 2*b*. Output lines **14***a*.**02.02** (A), **14***a*.**02.02** (B), **14***a*.**02.03** (A) and **14***a*.**02.03** (B) are provided to the Storage Select Register, FIG. 2*p* (FIGS. 16*a* through 16*d*) for Auxiliary Storage addressing. Numeric lines **14***a*.**02.03** (8), **14***a*.**02.03** (4), **14***a*.**02.03** (2), **14***a*.**02.03** (1), **14***a*.**02.02** (8), **14***a*.**02.02** (4), **14***a*.**02.02** (2), **14***a*.**02.02** (1), **14***b*.**02.01** (8), **14***b*.**02.01** (4), **14***b*.**02.01** (2) and **14***b*.**02.01** (1) are furnished from Character 1, 2 and 3 positions of MBR to the thousands, hundreds and tens orders of FIGS. 2*s* and 2*t* of the Memory Address Register, FIGS. 2*r* through 2*t* (FIGS. 17*a* through 17*e*). Numeric lines **14***a*.**02.03** (2), **14***a*.**02.03** (8), **14***a*.**02.02** (2), **14***a*.**02.02** (8), **14***b*.**02.01** (2) and **14***b*.**02.01** (8) are connected to Memory Address Register Controls of FIG. 2*u* (FIG. 17*f*). Zone lines **14***b*.**02.01** (A), **14***b*.**02.01** (B) and **14***a*.**02.04** (B) are connected to the ten thousands order of MBR of FIG. 2*t* (FIG. 17*e*). Lines **14***b*.**04.00** (C through 1), **14***b*.**04.01** (C through 1), **14***a*.**04.02** (C through 1), **14***b*.**04.03** (C through 1) and **14***a*.**05.04** (C through 1) are connected as inputs to the Parallel Character Transmission Write Bus, FIG. 2*f* (FIGS. 18*a* and *b*). Lines **14***b*.**04.00** (C through 1), **14***b*.**05.01** (C through 1), **14***a*.**05.02** (C through 1), **14***a*.**05.03** (C through 1) and **14***a*.**05.04** (C through 1) are coupled to the MBR Code Check of FIG. 2*f* (FIGS. 19*a* and *b*). Code Check Odd lines **19***a*.**01** and **19***b*.**01** are connected to MBR Code Check outputs of FIG. 19*c* (not shown in FIG. 2). Lines **14***b*.**06.00** (C through 1), **14***b*.**06.01** (C through 1), **14***b*.**06.02** (C through 1), **14***a*.**06.03** (C through 1) and **14***a*.**06.04** (C through 1) are coupled to Memory Out of FIG. 2*g* (FIGS. 20*a*, *b*, *c* and *d*). Output lines **14***b*.**02.00** (C through 1) from Character 0 position of the MBR are connected to the Operation Register of FIG. 2*v* (FIGS. 21*a* and *b*).

From the Keyboard of FIG. 2*v* (FIGS. 22*a* through *c*), output lines **22***b*.**07** (C), **22***b*.**06** (B), **22***b*.**05** (A), **22***b*.**04** (8), **22***b*.**03** (4), **22***b*.**02** (2) and **22***b*.**01** (1) are connected to corresponding bit positions of the Operation Register of FIG. 2*v* (FIGS. 21*a* and *b*). Outputs of the Operation Register are provided to an Operation Decoder, FIG. 2*v* (FIGS. 23*a* through 23*l*) and Operation Check Circuits, FIG. 2*v* (FIG. 24).

The units order of MAR, FIG. 2*r*, receives numeric input lines **20***d*.**04** (8), **20***d*.**05** (4), **20***d*.**06** (2) and **20***d*.**07** (1) from Character 4 position of the MBR via Memory Out controls, FIG. 2*g* (FIGS. 20*a* through 20*d*). The Memory Address Selector including manually operable keys, FIG. 2*q* (FIGS. 25*a* and *b*), provide numeric inputs to all orders of MAR via lines **25***b*.**01** through **25***b*.**19**. Input lines **26***a*.**126**, **26***a*.**135**, **26***a*.**133**, **26***a*.**130**, **26***a*.**128**, **26***a*.**144**, **26***a*.**142**, **26***a*.**140**, **26***a*.**138**, **26***a*.**154**, **26***a*.**151**, **26***a*.**149**, **26***a*.**147**, **26***a*.**156**, **26***a*.**158** and **26***a*.**160** are provided to all orders of MAR from the Synchronizer Memory Address Counter (not shown) via the Parallel Character Transmission cable, FIG. 2*r*, associated with a connector shown in FIG. 26*a* of a pair of connectors of FIGS. 26*a* and *b*.

Output lines **17***a*.**07**, **17***a*.**02**, **17***a*.**16**, **17***a*.**10**, **17***a*.**23**, **17***a*.**18**, **17***a*.**31** and **17***a*.**26** from the units order of MAR, FIG. 2*r*, are connected to a Control Address Decoder, FIG. 2*jj* (FIG. 27). Outputs of all orders of MAR, namely, lines **17***a*.**27**, **17***a*.**19**, **17***a*.**13**, **17***a*.**03**, **17***b*.**27**, **17***b*.**19**, **17***b*.**11**, **17***b*.**04**, **17***c*.**31**, **17***c*.**22**, **17***c*.**13**, **17***c*.**05**, **17***d*.**31**, **17***d*.**22**, **17***d*.**13**, **17***d*.**05**, **17***e*.**04**, **17***e*.**10** and **17***e*.**17**, are coupled to the Synchronizer Memory Address Counter

Checking, FIG. 2*ii* (FIG. 28). Output lines **17***a*.**12**, **17***b*.**26**, **17***b*.**18**, **17***b*.**10**, **17***b*.**03**, **17***c*.**30**, **17***c*.**21**, **17***c*.**12**, **17***c*.**04**, **17***d*.**30**, **17***d*.**21**, **17***d*.**12**, **17***d*.**04**, **17***e*.**03**, **17***e*.**09**, and **17***e*.**16** from the first through fifth order of MAR are directed to Memory Address Select Register or Memory Address Register to Data Synchronizer Unit (MASR/MAR to DSU), FIG. 2*u* (FIGS. 29*a* and *b*). Output lines **17***a*.**01**, **17***a*.**05**, **17***a*.**08**, **17***a*.**14**, **17***a*.**17**, **17***a*.**21**, **17***a*.**25**, and **17***a*.**29** from the units position of MAR are connected as inputs to the units position of MAC 1, FIG. 2*gg* (FIG. 30*a*). From the tens position of MAR, lines **17***b*.**02**, **17***b*.**05**, **17***b*.**09**, **17***b*.**12**, **17***b*.**17**, **17***b*.**20**, **17***b*.**25**, and **17***b*.**28** enter the tens position of MAC 1 (FIG. 30*b*). Lines **17***c*.**03**, **17***c*.**06**, **17***c*.**10**, **17***c*.**19**, **17***c*.**23**, **17***c*.**28**, and **17***c*.**32** from the hundreds position of MAR are connected to the hundreds order of MAC 1 (FIG. 30*c*). Lines **17***d*.**03**, **17***d*.**06**, **17***d*.**11**, **17***d*.**14**, **17***d*.**20**, **17***d*.**23**, **17***d*.**29** and **17***d*.**32** from the thousands order of MAR are connected to the thousands order of MAC 1 (FIG. 30*d*). Lines **17***e*.**02**, **17***e*.**05**, **17***e*.**08**, **17***e*.**11**, **17***e*.**15**, **17***e*.**18** from the ten thousands order of MAR are coupled to the ten thousands order of MAC 1 (FIG. 30*e*). Decoding circuits are provided for MAC 1 in FIG. 2*gg* (FIG. 30*g*) to determine the digit in the units position of MAC 1 and to determine the end of Memory. Orders of MAR are connected by cable to corresponding orders of MAC 2 of FIG. 2*hh* (FIGS. 31*a* through *e*) via lines **17***a*.**04**, **17***a*.**11**, **17***a*.**20**, **17***a*.**28**, **17***b*.**06**, **17***b*.**13**, **17***b*.**21**, **17***b*.**29**, **17***c*.**07**, **17***c*.**15**, **17***c*.**24**, **17***c*.**33**, **17***d*.**07**, **17***d*.**15**, **17***d*.**24**, **17***d*.**33**, **17***e*.**06**, **17***e*.**12**, and **17***e*.**19**. In order to obtain instructions for operation in response to the stored program, outputs are provided from MAR to an Instruction Counter, FIG. 2*ii* (FIGS. 32*a* through *e*) on the lines **17***a*.**09**, **17***a*.**07**, **17***b*.**14**, **17***b*.**22**, **17***b*.**30**, **17***c*.**08**, **17***c*.**16**, **17***c*.**25**, **17***c*.**34**, **17***d*.**08**, **17***d*.**16**, **17***d*.**25**, **17***d*.**34**, **17***e*.**07**, **17***e*.**13** and **17***e*.**20**. Outputs from the first through fourth orders of MAR are provided to the Select Register, FIG. 2*jj* (FIGS. 33*a* through *d*) on the lines **17***a*.**06**, **17***a*.**15**, **17***a*.**22**, **17***a*.**30**, **17***b*.**08**, **17***b*.**15**, **17***b*.**23**, **17***b*.**31**, **17***c*.**09**, **17***c*.**17**, **17***c*.**26**, **17***c*.**35**, **17***d*.**09**, **17***d*.**17**, **17***d*.**26** and **17***d*.**35** for selecting Input-Output units. Select Register Controls are shown in FIG. 33*e* and ALU Select Register Decoder is shown in FIGS. 33*f* and *g*. Output lines **17***c*.**20**, **17***c*.**11**, **17***c*.**29**, **17***c*.**02**, **17***d*.**28**, **17***d*.**19**, **17***d*.**10** and **17***d*.**02** from the third and fourth orders of MAR are used in MAR Controls, FIG. 2*u* (FIG. 17*f*) to provide Block Call for Half Step signals.

The Storage Controls **1.32** of FIG. 1 are shown in FIG. 2*tt* connected as shown and comprising Decoders, FIGS. 34*a* through *d*; X Switch Core Read Drivers, FIG. 35; Y Switch Core Write Drivers, FIGS. 36*a* and *b*; Y Switch Core Read Drivers, FIG. 37; X Switch Core Write Drivers, FIGS. 38*a* through *c*; Y Switch Core Matrix, FIG. 39; X Switch Core Matrix, FIG. 40; Storage Write Driver Select Circuits, FIG. 41; and Odd-Even Gating Circuits, FIG. 42.

The Storage In Controls 1.58 of FIG. 1 are shown in FIG. 2*uu* and include Storage In Select and Switching Circuits, FIG. 43, and Storage Inhibit Circuits, FIG. 44. The Core Storage **1.12** of FIG. 1 is also shown in FIG. 2*uu* and in detail in FIG. 45. Sensing outputs of the Storage Array, FIG. 2*uu*, are passed through Sense Amplifiers, FIG. 2*vv* (FIG. 46) to a Storage Buffer Register **1.34** of FIG. 1 (FIG. 2*vv*) on the lines **46.01** (C), **46.02** (B), **46.03** (A), **46.04** (8), **46.05** (4), **46.06** (2) and **46.07** (1). Logical circuits of the Storage Buffer Register are shown in FIG. 47. Outputs of the Storage Buffer Register are provided by cable to the Storage In Select and Switching circuits, FIG. 2*uu*, on the lines **47.01** ($\overline{C}$), **47.02** ($\overline{B}$), **47.03** ($\overline{A}$), **47.04** ($\overline{8}$), **47.05** ($\overline{4}$), **47.06** ($\overline{2}$) and **47.07** ($\overline{1}$). Another set of outputs are provided by cable from the Storage Buffer Register of FIG. 2*vv* to Character Register 2 in FIG. 2*kk* (**1.36** of FIG. 1) on the lines **47.08** (C), **47.09** (B), **47.10** (A), **47.11** (8), **47.12** (4), **47.13** (2) and **47.14** (1). Details of CR 2 are shown in FIG. 48.

Signals from the Memory Address Counter 1, FIG. 2*gg*, are provided by cable to a Memory Address Select Register (MASR), FIGS. 2*ww* through 2*yy* (FIGS. 49*a* through *j*) on the lines **30***a*.**03**, **30***a*.**07**, **30***a*.**10**, **30***a*.**13**, **30***b*.**02**, **30***b*.**05**, **30***b*.**06**, **30***b*.**07**, **30***c*.**02**, **30***c*.**05**, **30***c*.**06**, **30***c*.**07**, **30***d*.**02**, **30***d*.**05**, **30***d*.**06**, **30***d*.**07**, **30***e*.**01**, **30***e*.**03** and **30***e*.**05**. Also, signals from the Memory Address Counter 2, FIG. 2*hh*, are provided by cable to the MASR, FIGS. 2*ww* through 2*yy*, on the lines **31***a*.**01**, **31***a*.**03**, **31***a*.**04**, **31***a*.**05**, **31***b*.**01**, **31***b*.**03**, **31***b*.**04**, **31***b*.**05**, **31***c*.**01**, **31***c*.**03**, **31***c*.**04**, **31***c*.**05**, **31***d*.**01**, **31***d*.**03**, **31***d*.**04**, **31***d*.**05**, **31***e*.**01**, **31***e*.**02** and **31***e*.**03**.

Signals from the Instruction Counter, FIG. 2*ii* (FIGS. 32*a* through 32*e*) are provided by cable (broken) to Transfer Routing Controls, FIGS. 2*aa* (FIGS. 50*a* through 50*g*) on the lines **32***a*.**02**, **32***a*.**05**, **32***b*.**03**, **32***b*.**05**, **32***b*.**07**, **32***b*.**09**, **32***c*.**03**, **32***c*.**05**, **32***c*.**07**, **32***c*.**09**, **32***d*.**03**, **32***d*.**05**, **32***d*.**07**, **32***d*.**09**, **32***e*.**02**, **32***e*.**04** and **32***e*.**06**. Another set of outputs is provided on the lines **32***a*.**10**, **32***a*.**01**, **32***a*.**03**, **32***b*.**01**, **32***b*.**04**, **32***b*.**06**, **32***b*.**08**, **32***c*.**01**, **32***c*.**04**, **32***c*.**06**, **32***c*.**08**, **32***d*.**01**, **32***d*.**04**, **32***d*.**06**, **32***d*.**08**, **32***e*.**01**, **32***e*.**03** and **32***e*.**05** by cable to the Memory Address Select Register, FIGS. 2*ww* to 2*yy*.

Signals from the Starting Point Counter, FIG. 2*q*, (FIGS. 51*a* through **51***c*) are provided by cable on lines **51***c*.**04**, **51***c*.**03**, **51***c*.**02**, **51***c*.**01**, **51***b*.**06**, **51***b*.**05**, **51***b*.**04**, **51***b*.**03**, **51***b*.**02**, **51***b*.**01**, **51***a*.**06**, **51***a*.**05**, **51***a*.**04**, **51***a*.**03**, **51***a*.**02** and **51***a*.**01**, to all orders of the Storage Address Counter, FIG. 2*ff* (FIGS. 52*a* through *d*). SAC controls (not shown in FIG. 2) are illustrated in FIG. 52*e*. Additional inputs to stages 5 through 8 of SAC are provided by cable from the Storage Select Register, FIG. 2*p*, via lines **16***a*.**06**, **16***a*.**02**, **16***a*.**09**, **16***a*.**13**, **16***a*.**16**, **16***a*.**20**, **16***a*.**23** and **16***a*.**27**.

Outputs from all stages of SAC, FIG. 2*ff*, are furnished by cable as inputs to a Storage Address Select Register, FIG. 2*ee* (FIGS. 53*a* and *b*) on the lines **52***c*.**09**, **52***c*.**08**, **52***c*.**07**, **52***c*.**06**, **52***c*.**05**, **52***c*.**04**, **52***c*.**03**, **52***c*.**02**, **52***a*.**08**, **52***a*.**07**, **52***a*.**06**, **52***a*.**05**, **52***a*.**04**, **52***a*.**03**, **52***a*.**02** and **52***a*.**01**. In turn, SASR of FIG. 2*ee*, provides outputs on the lines **53***b*.**08**, **53***b*.**07**, **53***b*.**06**, **53***b*.**05**, **53***b*.**04**, **53***b*.**03**, **53***b*.**02**, **53***b*.**01**, **53***a*.**08**, **53***a*.**07**, **53***a*.**06**, **53***a*.**05**, **53***a*.**04**, **53***a*.**03**, **53***a*.**02** and **53***a*.**01** to the Storage Address Decoders of FIG. 2*tt*.

Two more sets of output lines from the Storage Select Register, FIG. 2*p*, are provided by separate cable to Storage Select Register Decoding, FIG. 2*ee* (FIG. 54) and SSR Decoders, FIG. 2*p* (FIGS. 55*a* and *b*). SSR lines **16***a*.**03**, **16***a*.**10**, **16***a*.**17** and **16***a*.**24** are connected to SSR Decoding and lines **16***a*.**06**, **16***a*.**02**, **16***a*.**07**, **16***a*.**08**, **16***a*.**11**, **16***a*.**12**, **16***a*.**14**, **16***a*.**15**, **16***a*.**18**, **16***a*.**19**, **16***a*.**21**, **16***a*.**22**, **16***a*.**25** and **16***a*.**26** are connected to SSR Decoders. SSR Decoding of FIG. 2*ee* (FIG. 54) furnishes outputs to the 2×4 Storage Decoder of FIG. 2*tt*. Outputs of the SSR Decoders of FIG. 2*p* (FIGS. 55*a* and *b*) are furnished by cable (broken) to Set Bit Routing Controls, FIG. 2*x* (FIGS. 56*a* and *b*) on lines **55***a*.**02**, **55***a*.**08**, **55***a*.**11**, **55***a*.**15**, **55***a*.**18**, **55***a*.**19**, **55***a*.**22**, **55***a*.**23**, **55***a*.**27**, **55***a*.**28**, **55***b*.**01**, **55***b*.**03**, **55***b*.**04**, **55***b*.**06**, **55***b*.**08**, **55***b*.**09**, **55***b*.**11** and **55***b*.**12**. Also, SSR Decoder outputs are provided to Transfer Routing Controls, FIG. 2*aa* (FIGS. 50*a* through 50*g*) on the lines **55***a*.**03**, **55***a*.**04**, **55***a*.**05**, **55***a*.**06**, **55***a*.**09**, **55***a*.**10**, **55***a*.**12**, **55***a*.**13**, **55***a*.**14**, **55***a*.**16**, **55***a*.**17**, **55***a*.**20**, **55***a*.**21**, **55***a*.**24**, **55***a*.**25**, **55***a*.**26**, **55***b*.**02**, **55***b*.**05**, **55***b*.**07**, **55***b*.**10**, **55***b*.**13** and **55***b*.**14**. Additionally, output lines from SSR Decoders 1 and 2 are sent to Input-Output Controls via the PCT bus.

Memory Out, FIG. 2*g* (FIGS. 20*a* through *d*) provide outputs to CR 1, FIG. 2*h*, on the lines **20***d*.**01** (C), **20***d*.**02** (B), **20***d*.**03** (A), **20***d*.**04** (8), **20***d*.**05** (4), **20***d*.**06** (2) and **20***d*.**07** (1). Character Register 1 (CR 1) has three sets of outputs. The Right Plate outputs are sent by cable to CR 1 Right Plate Output Distributor Circuits, FIGS. 2*k* through 2*m* (FIG. 58) on the lines **57.03** (C),

57.05 (B), 57.07 (A), 57.09 (8), 57.11 (4), 57.13 (2) and 57.15 (1). Left Plate Outputs of CR 1 are provided by cable to the Left Plate Output Distributor Circuits, FIGS. 2*i* through 2*j* (FIG. 59) on the lines 57.04 ($\overline{B}$), 57.06 ($\overline{A}$), 57.08 ($\overline{8}$), 57.10 ($\overline{4}$), 57.12 ($\overline{2}$) and 57.14 ($\overline{1}$). Outputs from $\overline{C}$ of Character Register 1 are provided on line 57.02 ($\overline{C}$) to Transfer Routing Controls, FIG. 2*aa* (FIGS. 50*a* through *g*) and on line 57.01 ($\overline{C}$) to Set Bit Controls, FIG. 2*x* (FIGS. 56*a* and *b*). A line 58.33 (A) from the Right Plate Distributor Circuits, FIG. 2*l* (FIG. 58) is sent to Instruction Time Check, FIG. 2*bb* (FIG. 60). A line 59.21 ($\overline{A}$) from the Left Plate Distributor Circuits, FIG. 2*i*, and line 58.27 (A) from the Right Plate Distributor Circuits, FIG. 2*l*, goes to Instruction Time Routing Control, FIG. 2*bb* (FIG. 61). Lines 59.22 ($\overline{A}$) and 59.03 ($\overline{B}$) from Left Plate Out, FIG. 2*i*, and lines 58.28 (A) and 58.17 (B) from Right Plate Out, FIGS. 2*k* and *l* are connected as inputs to Storage Sign Trigger controls, FIG. 2*aa* (FIG. 62). The NOT lines from code bit position of CR 1 Left Plate Outputs of FIGS. 2*i* and *j* go to Inter Register Check Routing and Trigger, FIG. 2*z* (FIG. 63). Lines 58.12 (B) and 58.26 (A) from the Right Plate Distributor, FIGS. 2*k* and *l*, are connected as inputs to Add Address to Memory Routing Controls, FIG. 2*z* (FIGS. 64*b* and *c*) and lines 58.15 (B) and 58.31 (A) originating in FIGS. 2*k* and *l* go to Unload Address Controls, FIG. 2*z* (FIG. 65*b*). Line 59.04 ($\overline{B}$) originates at CR 1 B Left Plate Out, FIG. 2*i*, and goes to FIG. 2*y*, Divide Routing Controls, FIG. 66*h*. Line 59.09 ($\overline{B}$) from FIG. 2*i*, CR 1 Left Plate Output, goes to Multiply Routing Controls, FIG. 2*y* (FIG. 67). Lines 58.09 (B), 58.10 (B), 58.11 (B) and 58.25 (A) from CR 1 Right Plate Outputs, FIG. 2*k*, and lines 59.05 ($\overline{B}$) and 59.17 ($\overline{A}$) from FIG. 2*i* are connected to Add to Memory Routing Controls, FIG. 2*x* (FIGS. 68*a* through *e*). Lines 58.05 (B), 58.22 (A) and 59.14 ($\overline{A}$) from FIGS. 2*k*, *l* and *i* are connected as inputs to Set Bit Routing Controls, FIG. 2*x* (FIGS. 56*a* and *b*). Lines 59.10 ($\overline{B}$) and 59.20 ($\overline{A}$) from FIG. 2*i* and lines 58.16 (B) and 58.32 (A) from FIGS. 2*k* and *l* furnish signals to Sign, No Operation and Stop Routing Controls, FIG. 2*x* (FIGS. 69*a* and *b*). Lines 58.07 (B), 58.08 (B) and 58.24 (A) from FIGS. 2*k* and *l* are provided by cable to Load Address Routing Controls, FIG. 2*w* (FIGS. 70*a* and *b*). Lines 58.18 (B), 58.34 (A), 58.38 (8), 58.43 (4), 58.48 (2) and 58.53 (1), one line from each data bit position of CR 1, Right Plate Outputs, FIGS. 2*k*, 1 and *m*, and NOT lines 59.11 ($\overline{B}$), 59.23 ($\overline{A}$), 59.28 ($\overline{8}$), 59.33 ($\overline{4}$), 59.38 ($\overline{2}$) and 59.43 ($\overline{1}$) from CR 1 Left Plate Outputs, FIGS. 2*i* and *j*, are provided to CR 1 Recognition Circuits, FIG. 2*n* (FIG. 71*a*). Lines 58.02 (C), 58.19 (B), 59.39 (8), 58.44 (4), 58.49 (2), and 58.54 (1) from CR 1 Right Plate Outputs and lines 59.12 ($\overline{B}$), 59.24 ($\overline{A}$), 59.29 ($\overline{8}$), 59.34 ($\overline{4}$), 59.39 ($\overline{2}$) and 59.44 ($\overline{1}$) from CR 1 Left Plate Outputs are directed to CR 1 Recognition Circuits, FIG. 2*o* (FIG. 71*b*). Lines 58.03 (C), 59.20 (B), 58.35 (A), 58.40 (8), 58.45 (4), 58.50 (2) and 58.55 (1) from CR 1 Right plate Outputs, FIGS. 2*k*, *l* and *m*, and 59.13 ($\overline{B}$), 59.25 ($\overline{A}$), 59.30 ($\overline{8}$), 59.35 ($\overline{4}$) 59.40 ($\overline{2}$) and 59.45 ($\overline{1}$) from CR 1 Left Plate Outputs, FIGS. 2*i* and *j*, are connected by cables to CR 1 Code Check, FIG. 2*o* (FIG. 72). Lines 58.06 (B), 58.23 (A), 58.37 (8), 58.32 (4), 58.47 (2) and 58.25 (1) from CR 1 Right Plate Outputs, FIGS. 2*k*, *l* and *m*, are connected by cable to inputs of Adder Input Switching, FIG. 2*qq* (FIG. 73). Lines 58.04 (C), 58.21 (B), 58.36 (A), 58.41 (8), 58.46 (4), 58.51 (2) and 58.56 (1) from CR 1 Right Plate Outputs are directed to the I/O Parallel Character Transfer Cable (broken), FIG. 2*m* (FIG. 26*b*).

Output lines 59.01 ($\overline{B}$), 59.15 ($\overline{A}$), 59.26 ($\overline{8}$), 59.31 ($\overline{4}$), 59.36 ($\overline{2}$) and 59.41 ($\overline{1}$) from CR 1 Left Plate Outputs (FIGS. 2*i*, *k* and *l*) are connected by cable to Transfer Routing Controls, FIG. 2*aa* (FIGS. 50*a* through *g*). Output lines 59.07 ($\overline{B}$), 59.06 ($\overline{B}$), 59.08 ($\overline{B}$), 58.13 (B), 58.14 (B), 59.18 ($\overline{A}$), 59.19 ($\overline{A}$), 58.29 (A) and 58.30 (A) of CR 1 Right and Left Plate Output Circuits are sent by cable to Reset Add, Reset Subtract, Add and Subtract Routing Controls of FIG. 2*y* (FIGS. 74*b*, *c*, *e*, and *f*). Output lines 59.02 ($\overline{B}$), 59.16 ($\overline{A}$), 59.27 ($\overline{8}$), 59.32 ($\overline{4}$), 59.37 ($\overline{2}$) and 59.42 ($\overline{1}$) from CR 1 Left Plate Outputs are provided by cable as inputs to Inter Register Check Routing, FIG. 2*z* (FIGS. 63*a*, *b* and *c*).

In FIG. 2*kk*, pairs of complementary output lines 48.04 through 48.15, representing the bit configurations of the zone and numeric portions of the characters in CR 2 are sent by cable to CR 2 Distribution Circuits of FIGS. 2*ll* through 2*nn* (FIG. 75).

Output lines from CR 2 Distribution Circuits, FIGS. 2*ll*, *mm* and *nn*, comprising 75.07 ($\overline{B}$), 75.10 (A), 75.14 ($\overline{A}$), 75.18 (8), 75.22 ($\overline{8}$), 75.27 (4), 75.33 ($\overline{4}$), 75.39 (2), 75.43 ($\overline{2}$) 75.49 (1) and 75.53 ($\overline{1}$) are sent by cable to CR 2 Recognition, FIG. 2*oo* (FIG. 76). Output lines from CR 2 Distribution Circuits, FIG. 2*ll*, *mm* and *nn*, comprising 75.04 (B), 75.03 ($\overline{B}$), 75.11 (A), 75.15 ($\overline{A}$), 75.19 (8), 75.23 ($\overline{8}$), 75.28 (4), 75.34 ($\overline{4}$), 75.40 (2), 75.44 ($\overline{2}$), 75.50 (1) and 75.54 ($\overline{1}$) are directed by cable to CR 2 Code Check of FIG. 2*pp* (FIG. 77). Output lines from CR 2 Distribution Circuits, FIGS. 2*mm* and 2*nn*, comprising 75.17 (8), 75.21 ($\overline{8}$), 75.32 ($\overline{4}$), 75.26 (4), 75.38 (2), 75.42 ($\overline{2}$), 75.52 ($\overline{1}$) and 75.48 (1), representing the numeric bit configuration and the complement thereof of the character in CR 2, are sent by cable to Multiplier Register and Decoder, FIG. 2*hhh* (FIG. 78), which, in turn, provides output lines 78.01, 78.02, 78.03, 78.04 and 78.06 to the Multiple Selector of FIGS. 2*rr* and 2*ss* (FIG. 82).

Output lines 73.08 (B) and 73.01 (A) from the B and A positions of Adder Input Switching, FIG. 2*qq*, are furnished as inputs to the Zone Adder, FIG. 2*ccc* (FIG. 79). Lines 73.02 (8), 73.04 (4), 73.03 (2), 73.05 (1) and 73.06 ($\overline{1}$) are sent to the Multiplicand Doubler and Quadrupler of FIG. 2*dd* (FIG. 80) from Adder Input Switching, FIG. 2*qq*. The numeric portion of the Multiplicand character is also provided to the Quintupler, FIG. 2*cc* (FIG. 81) from Adder Input Switching via lines 73.02 (8), 73.04 (4), 73.03 (2), 73.05 (1) and 73.07 ($\overline{1}$). Similarly, the numeric position of the Multiplicand character is furnished to Multiple Selection, FIGS. 2*rr* and 2*ss* (FIG. 82), via lines 73.02 (8), 73.04 (4), 73.03 (2), and 73.05 (1) from Adder Input Switching. Also, the numeric portion of the Multiplicand character, FIG. 2*qq*, is directed to True/Complement Control, FIG. 2*fff* (FIG. 83), by the lines 73.09 (8), 73.10 (4), 73.11 (2), 73.12 ($\overline{1}$) and 73.13 (1).

The Multiple Selector receives five times the multiplicand character value from the Quintupler, FIG. 2*cc*, via lines 81.01 through 81.05, two times the value on the lines 80.02 through 80.04 from the Doubler, four times the value on the lines 80.01, 80.06, 80.07 and 80.08 from the Quadrupler, FIG. 2*dd*, and one times the value from Adder Input Switching, as described previously. The desired multiples are selected by the control lines 78.01, 78.02, 78.03, 78.06 and 78.04 entering Multiple Selection of FIG. 2*rr* from the Multiplier Register and Decoder of FIG. 2*hhh*.

Output lines from the Multiple Selection, FIGS. 2*rr* and 2*ss*, comprising lines 82.04 through 82.08 are furnished by cable to the Multiple Adder of FIG. 2*hhh* (FIG. 84), which, in turn, provides output lines 84.03 through 84.06 to Decimal Correction Circuits of FIG. 2*ggg* (FIG. 85). An output line of the Multiple Adder, 84.01, is connected as an input to the Digit Adder of FIG. 2*eee* (FIG. 86) and a line 84.02 is connected to Set Bit Routing Controls, FIG. 2*x* (FIG. 56*a*).

The Decimal Correction circuits of FIG. 2*ggg* (FIG. 85) furnish output lines **85.02** (2), **85.04** (4) and **85.06** (8) to Set Bit Routing Controls of FIG. 2*x* (FIG. 56*a*), and output lines **85.01** (2), **85.03** (4) and **85.05** (8) by cable to the Digit Adder, FIG. 2*eee* (FIG. 86).

The Digit Adder has two sets of output lines. One set comprising lines **86.08** (8) Carry, **86.06** (8), **86.04** (4), **86.02** (2) and **86.01** (1) goes to Decimal Correction Circuits, Digit Adder, FIG. 2*ccc* (FIG. 87), while the other set, comprising **86.09** (8), **86.07** (8), **86.05** (4) and **86.03** (2) goes to Decimal Carry Circuits and Zone Carry Trigger, FIG. 2*ddd* (FIG. 88).

In FIG. 2*ccc*, output lines **87.09** (1), **87.02** (2), **87.06** (4) and **87.14** (8) from the Decimal Correction Circuits are furnished by cable to the Result Register, FIG. 2*aaa* (FIGS. 89*a* and *b*); lines **87.13** (8), **87.05** (4), **87.01** (2) and **87.12** (1) are sent by cable to C Bit Generator, FIG. 2*bbb* (FIG. 90); and lines **87.16** (8), **87.15** (8), **87.07** (4), **87.08** (4), **87.03** (2), **87.04** (2), **87.10** (1) and **87.11** (1) are directed by cable to Inter Register Check, FIG. 2*z* (FIGS. 63*a*, *b* and *c*).

In FIG. 2*ll* (FIG. 75), output lines **75.03** (B), **75.06** ($\overline{B}$), **75.09** (A), and **75.13** ($\overline{A}$) from CR 2 Distribution Circuits, provide the zone bits and complements to the True/Complement portion of the Zone Adder, FIG. 2*fff* (FIG. 79). Output lines **79.16** and **79.17** from the True/Complement portion of the Zone Adder, FIG. 2*fff*, are connected to the Zone Adder, FIG. 2*ccc*. The Zone Adder has three sets of output lines. One set comprising lines **79.08** (B), **79.09** (B), **79.04** (A) and **79.05** (A) go by cable to Inter Register Check Routing, FIG. 2*z* (FIGS. 63*a*, *b* and *c*); another set comprising lines **79.07** (B) and **79.03** (A) go by cable to positions B and A respectively, of the Result Register of FIG. 2*aaa* (FIGS. 89*a* and *b*); and the third set of lines **79.06** (B) and **79.02** (A) go to the Zone positions of the C Bit Generator of FIG. 2*bbb* (FIG. 90). The C Bit Generator also has inputs (not previously mentioned) **58.01** (C) from CR 1 Right Plate Out, FIG. 2*k* (FIG. 58), and **48.03** (C) from CR 2, FIG. 2*kk* (FIG. 48). Output line **90.01** (C) from C Bit Generator is connected to the C position of the Result Register, FIG. 2*aaa* (FIGS. 89*a* and *b*).

The Result Register of FIG. 2*aaa* has four sets of input lines. Two previously described are from the Decimal Correction Circuits and the Zone Adder of FIG. 2*ccc*. The third set comprising lines **22***b*.**14** (C), **22***b*.**13** (B), **22***b*.**12** (A), **22***b*.**11** (8), **22***b*.**10** (4), **22***b*.**09** (2) and **22***b*.**08** (1) is connected by cable from the Keyboard of FIG. 2*v*. The fourth set is from the Memory Test Controls, FIG. 2*zz*, and consists of lines **92.01** through **92.07**.

The Result Register of FIG. 2*aaa* provides output lines **89***b*.**11** (C), **89***b*.**07** (B), **89***b*.**08** ($\overline{B}$) **89***b*.**03** (A), **89***b*.**04** ($\overline{A}$), **89***a*.**15** (8), **89***a*.**16** ($\overline{8}$), **89***a*.**11** (4), **89***a*.**12** ($\overline{4}$), **39***a*.**07** (2), **89***a*.**08** ($\overline{2}$), **89***a*.**03** (1) and **89***a*.**04** ($\overline{1}$) to the Result Register Code Check, FIG. 2*zz* (FIG. 91). Another set of output lines **89***a*.**09** ($\overline{C}$), **89***a*.**05** ($\overline{B}$), **89***b*.**01** ($\overline{A}$), **89***a*.**13** ($\overline{8}$), **89***a*.**09** ($\overline{4}$), **89***a*.**05** ($\overline{2}$) and **89***a*.**01** ($\overline{1}$) are directed by cable to Memory Input Switch, FIG. 2*b* (FIG. 11). Finally, a set of output lines **89***b*.**10** ($\overline{C}$), **89***b*.**06** ($\overline{B}$), **89***b*.**02** ($\overline{A}$), **89***a*.**14** ($\overline{8}$), **89***a*.**10** ($\overline{4}$), **89***a*.**06** ($\overline{2}$) and 89a.**02** ($\overline{1}$) are furnished by cable to Storage In Select Circuits of FIG. 2*uu* (FIG. 43).

The Memory Test Controls of FIG. 2*zz*, shown in detail in FIG. 92, are used to place a character manually into the Result Register for entry into Memory.

As mentioned previously, a stored program is a series of coded operational steps referred to as instructions, arranged in a particular sequence and stored in Core Memory. This program is obtained from Memory, instruction by instruction, and each instruction is interpreted and executed in turn.

As shown in FIG. 2*bx*, an instruction comprises five characters and is divided into two parts, the Operations part and the Address part. The Operations part is a single character (Character 0) designating the operation to be performed. The Address part is divided into two portions. The first, comprising numeric portions of Characters 1 through 4, B and A Zone bits of Character 1, and the B Zone bit of Character 4, specifies the location of data in the Core Memory which is to be operated upon in accordance with the Operation part. The A bit of Character 1 is given a value of 10,000; the B bit of Character 1 is given a value of 20,000; and the B bit of Character 4 is given a value of 40,000. The second portion of the Address part is the Storage Address part located in the Zone portion of Characters 2 and 3, and designates the address in Core Storage to be used during the execution of the instruction. For some instructions, the presence of bits in the Storage Address portion indicates a special instruction or an address not associated with Storage, but for the present, such modifications will not be explained in detail.

The following chart shows the instructions which are performed by the Data Processing System. The Mnemonic codes are merely the shorthand designations of the instructions and it is the operations part which is contained in Character 0 of the instruction. The From and To columns refer to the movement of data when appropriate and the Remarks and Limiting Factor briefly expand on the instruction title. When necessary to the description of the invention, details of the instructions are given.

Chart II

Instruction	Mnemonic Code	Oper. Part	From—	To—	Remarks	Limiting Factor
Add	ADD	G	Mem	Acc/AS	Result in accumulation or Aux. Stor	Non-num. char. in mem. or Storage Mark in Storage, whichever is last.
Add Mem	ADM	6	Acc/AS	Mem	Signed Mem. field—algebraic addition Unsigned Mem. field—non-algebraic and zone addition	Non-num. char. in mem. Acc/Aux. Stor. mark.
Add Address Mem	AAM	@	Acc/AS	Mem	Adds 5 digits in Acc/AS to the mem. field interpreted as addr. part of an instruc.	5 characters in Acc/AS; 4 char. in Memory.
Blank Memory	BLM	$		Mem	Puts Blank characters in Mem	Address of instruction.
Compare	CMP	4			Accumulator or aux. stor. with Memory	Acc/Aux Stor. mark.
Ctrl 0000	IOF	3			Turn off input-output indicator	
Ctrl 0001	WTM	3			Record tape mark	
Ctrl 0002	RWD	3			Rewind tape unit	
Ctrl 0003	ION	3			Turn ON input-output indicator	
Ctrl 0004	BSP	3			Back space tape one record	
Ctrl 0005	SUP	3			Prevent printing or punching one cycle	

Chart II—Continued

Instruction	Mnemonic Code	Oper. Part	From—	To—	Remarks	Limiting Factor
Divide	DIV	W			Dividend in acc. 00; divisor in Mem Quotient in Acc. 00.	Non-num char in Mem. and Stor. Mark in Acc. 00.
Lengthen	LNG	D			Add zeroes to right (Acc. 00)	Address of instruction.
Load	LOD	8	Mem	Acc/AS	Loads zones as well as numbers	Acc/Aux Stor. Mark.
Load Address	LDA	#	Mem	Acc/AS	Loads Address portion of an instruction as a five-digit field in Acc/AS.	4 char. of Mem.
Multiply	MPY	V			Multiplier Acc. 00; multiplicand mem; product Acc. 00.	Non-num char in Mem and Stor. Mark in Storage.
No Oper	NOP	A			No operation	
Norm Tr	NTR	X			Left-hand zero in accum. or aux. stor. causes transfer. Zero deleted except last zero.	
Read	RD	Y	Input	Mem	From tape to Mem. From card reader to Mem. From drum to Mem. (Etc.)	¾" inter-record gap, Record Storage mark, Drum mark (by input device).
Read-Write	RWW	S			Alert reading tape unit to operate simultaneously with next write instruct.	
Receive	RCV	U			Sets MAC 2 to Addr. of Instruction	
R Add	RAD	H	Mem	Acc/AS	Resets accum. or aux. stor.; adds from Mem.	Non-num. char. in Mem.
R Sub	RSU	Q	Mem	Acc/AS	Resets accum. or aux. stor.; Subtracts Mem. field from a zero in Acc/AS.	Non-num. char. in Mem.
Round	RND	E			Drop positions from right and ½ adjust (accum. 00). Zero balance is plus.	Address of instruction.
Send	SND	1	Mem	Mem	Use with RCV for transmitting data 5 char. at a time from Mem. to Mem. if RWW tgr. is off. If RWW tgr. is on, perform redundancy chk of Mem., beginning with instruct. addr.	If RWW Tgr off Stor. Mark in Aux. If RWW Tgr on End of Mem.
Select	SEL	2			Select Input unit, Output unit, Alter Sw, or check indicator.	
Set Bit	SB	%			Transfer a zero or one bit to the char. addressed into a bit position (B, A, 8, 4, 2, 1) determined by Storage Address.	
Set Left	SET	B		Acc/AS	Place storage mark to left of field in indicated storage addr (00–15). Insert zeros if Instr. Addr. is greater than field length in Acc/AS.	Address of instruction.
Shorten	SHR	C			Drop positions from right (Acc. 00). Zero balance is plus.	Address of instruction.
Sign	SGN	T	Mem	Acc/AS	Remove zone 11, 10 or 01 from Mem., place & or minus sign in Accum. or Aux. Stor.	
Stop	HLT	J			Stop machine	
Store	ST	F	Acc/AS	Mem	Store num. field in Mem	Acc/Aux Stor. mark.
St Print	SPR	5	Acc/AS	Mem	Store field for printing. Skips decimals, prints commas. Removes left-hand zeros and commas.	Acc./Aux Stor. mark.
Subtract	SUB	P	Mem	Acc/AS	Subtract in Mem. field from Stor. field. Result in acc. or aux. storage.	Non-num. char. in Mem. or Stor. mark in Acc/AS, whichever is last.
Transfer	TR	1			Unconditional transfer.	
Tr Any	TRA	1			Trans. if condition or line specified by ASU code (00–06) is up.	
Tr Equal	TRE	L			Transfer if Equal Tgr is ON.	
Tr High	TRH	K			Transfer if High Tgr is ON.	
Tr Plus	TRP	M			Transfer if designated Acc. or Aux Stor. sign is plus.	
Tr Signal	TRS	O			Transfer if selected I 10 indicator ON (ASU 00) or line indicated by ASU Coding is ON (ASU 01–15).	
Tr Zero	TRZ	N			Transfer if designated Digit Zero Tgr is ON.	
Tr on Zero Bit	TZB	·			Tests the Bit specified by ASU coding in the char. at the MAC 2 address.	
Transmit	TMT	9	Mem	Mem	Use with RCV for Transmitting data from Mem to Mem. Code 00; 5 char. group transmission Code 01–15; single char. transmission.	R/M in Mem. pos. ending in 4 or 9 or Aux. stor. mark.
Unload	UNL	7	Acc/AS	Mem	Unload zones and numbers	Acc/Aux. Stor. mark.
Unload Address	ULA	*	Acc/AS	Mem	Unload a 5 digit field from Acc/AS into the Addrs. portion of designated instr. in Mem.	
Write 00	WR	R	Mem	Output	From Mem. to tape From Mem. to card punch or printer From Mem. to drum Etc	Group mark. Group mark. Group mark. Group mark.

Chart II—Continued

Instruction	Mnemonic Code	Oper. Part	From—	To—	Remarks	Limiting Factor
Write 01	WR	R	Mem	Output	From Mem. to card, printer, tape, drum	20,000th Mem. pos.
Write Erase 00	WRE	Z	Mem	Output	Replace each char. in Mem. with blank. To tape To card punch or printer To drum Etc.	 Group mark. Group mark. Group mark. Group mark.
Write Erase 01	WRE	Z			Same as above	Limited by end of 20,000 Mem. block.

As mentioned previously, the first address portion of the instruction may refer to any location in a number of storage devices such as Memory or to Input-Output devices. Addresses of such units are given below.

Chart III

Memory	0000–39, 999 or 0000–79, 999
Card Readers	0100–0199
Tape Units	0200–0299
Card Punches	0300–0399
Printers	0400–0499
Typewriter	0500
Tape Record Coordinator Tape Units	0600
Drum Sections	1000–9999
Alteration Switches	0911–0919
Instruction Check Indicator	0900
Machine Check Indicator	0901
Read-Write Check Indicator	0902
Printer-Punch Check Indicator	0903
Overflow Check Indicator	0904
Sign Check Indicator	0905

Referring to the composite of FIGS. 2*a* through 2*hhh*, information is read out of Memory, FIG. 2*b*, into Memory Buffer Register, FIGS. 2*c* through 2*e*. Then one of the characters of the Memory Buffer Register is selected by means of Memory Out Switches, FIG. 2*g*, and placed in Character Register 1, FIG. 2*h*. At the same time, information may be read out of Storage, FIG. 2*uu*, into the Storage Buffer Register, FIG. 2*vv*, and then into Character Register 2, FIG. 2*kk*. Character Register 1, FIG. 2*h*, has associated therewith, Character Register 1 Recognition Circuits, FIG. 2*o*, for recognizing the presence of certain characters or classes of characters in CR 1. Furthermore, a check for accuracy of information transfer is made each time a character is entered in the Character Register 1 by CR 1 Code Check, FIG. 2*o*. In like manner, Character Register 2, FIG. 2*kk*, has associated therewith, CR 2 Recognition Circuits, FIG. 2*oo*, and CR 2 Code Check Circuits, FIG. 2*pp*. The coding of each character read into the Character Registers requires an even number of binary "ones" in the seven bits of the character and the C bit is always selected so as to provide (for correct operation) this even number of binary "ones" in a character. The Adder Input Switching, FIG. 2*qq*, is effective to gate the numeric portion of the character in Character Register 1, FIG. 2*h*, or the character in Character Register 2, FIG. 2*kk*, by way of True Complement Controls, FIG. 2*fff*, to the Digits Adder, FIG. 2*eee*; to gate the numeric portion of a character in Character Register 1, directly, to the Multiple Selection Circuits of FIGS. 2*rr* and 2*ss*, and indirectly, to the Multiple Selection Circuits of FIGS. 2*rr* and 2*ss*, by way of the Multiplicand Doubler and Quadrupler, FIG. 2*dd*, and the Quintupler, FIG. 2*cc*. The Multiplicand Doubler and Quadrupler and the Quintupler, shown in detail in FIGS. 80 and 81, respectively, are effective to double, quadruple and quintuple values of the input numbers, and thus the Multiple Selection Circuits, FIGS. 2*rr* and 2*ss*, receive inputs of 1, 2, 4 and 5 times the numeric value of the character, in Character Register 1. The Multiple Selection Circuits under control of Select 1, 2, 4 and 5 multiples from the Multiplier Register and Decoding, FIG. 2*hhh*, provide the proper multiples to the Multiple Adder, FIG. 2*hhh*, during a Multiply operation. However, for most operations the one's multiple is gated. The sum output of the Multiple Adder, FIG. 2*hhh*, being the sum of binary coded decimal numbers, may require correction which is provided by the Decimal Correction Circuits, FIG. 2*ggg*, whose outputs (2, 4 and 8), in turn, are emitted to the Digit Adder, FIG. 2*eee*. The one bit (1) from the Multiple Adder, FIG. 2*hhh*, is not altered by decimal correction and so proceeds directly to the Digit Adder, FIG. 2*eee*. The Digit Adder combines the value received via the True Complement Controls, FIG. 2*fff*; the Multiple Adder Correction Circuits, FIG. 2*ggg*, and the Multiple Adder, FIG. 2*hhh*, to provide a binary coded decimal sum. This sum may also require correction, the correction being provided by the Decimal Correction Circuits for Digit Adder, FIG. 2*ccc*. The output of the Decimal Correction Circuits, Digit Adder, FIG. 2*ccc*, which is the corrected sum, is emitted to the Result Register, FIG. 2*aaa*, to the C Bit Generator, FIG. 2*bbb*, and the Inter-Register Check Routing Circuits, FIG. 2*z*.

While addition or multiplication of the numeric portion of the character is accomplished in the circuits just described, the zone bits, A and B, may also be added. The Zone Adder, FIG. 2*ccc*, receives the A and B bits of CR 1 via Adder Input Switching, FIG. 2*qq*, and the A and B bits of CR 2 by way of CR 2 to T/C Controls, FIG. 2*fff*. The C Bit Generator, FIG. 2*bbb*, serves to generate a new check bit (C) for the corrected character, and sends it to the Result Register, FIG. 2*aaa*. The decimally corrected and redundantly correct sum output from the Digit Adder, and Zone Adder, now in the Result Register, may be gated to Memory or Storage from the Result Register.

The Memory Array of FIG. 2*b* comprises 280 thousand ferrite cores in which information is magnetically stored according to the state of each individual core. Writing a "1" into a core stores flux of one polarity, while reading a "1" from a core reverses the flux and resets the core to "0." The selection of polarities corresponding to the bistable states is, of course, entirely arbitrary. The Memory Array comprises thirty-five core planes, each plane consisting of an 80×1000 rectangular Matrix, which acts as a single block of storage having addresses numbered continuously from 00000 to 39,999, where each address corresponds to a particular 7-bit character. Groups of five characters (35 bits in all) are read simultaneously from the 35 core planes. For example, five characters located at the beginning of Memory would have addresses 00000 through 00004, but all five characters would be read from Memory simultaneously, regardless of whether the given address were 00000, 00001, 00002, 00003, or 00004. Any one of the characters of a group may be selected from the Memory Buffer Register by Memory Out, FIG. 2*g*. This is accomplished as follows: If address 00000 is given, five characters are brought from addresses 00000 through 00004 of Core Memory and placed in the Memory Buffer Register. However, since address 00000 was given, only character 0 is selected from the MBR by Memory Out, FIG. 2*g*.

During the Read and Write portions of an Instruction or Execution Character cycle, the Memory Decoders, FIG. 2*a*, receive an address by way of the Memory Address Select Circuits, FIGS. 2*ww* through 2*yy*, the latter

receiving the address from either MAC 1, FIG. 2*gg*, or MAC 2, FIG. 2*hh*. Either Memory Address Counter, MAC 1 or MAC 2, may contain any of the addresses 00000 through 39,999; however, the units orders of MASR always contain a 4 or a 9 for an Instruction since five characters, the last having an address ending in 4 or 9, are required from Core Memory to be placed in the MBR and transferred in parallel to the Instruction Register and the Memory Address Register.

Referring now to FIG. 2*uu*, the Core Storage Array comprises seven planes, each plane arranged in a 16×32 matrix for the storage of 512 bits, the seven planes storing 512 characters. The addresses, then, for each character in Core Storage are 0 to 511. Individual characters are read out of Core Storage at addresses specified by means of the Storage Address Select Register and the SSR Decoding, FIG. 2*ee*, which provide outputs to the Accumulator Decoders of FIG. 2*tt* (FIGS. 34*a* through *d*). The Storage Address Select Register receives addresses from the Storage Address Counter, FIG. 2*ff*, the latter having inputs from both the Storage Select Register, FIG. 2*p*, and the Starting Point Counter, FIG. 2*q*. The Starting Point Counter keeps track of the address of the word stored in Accumulator Storage, that is, the address of the least significant digit portion. It is unnecessary that the Starting Point Counter be reset to 0 or to any particular address whenever the machine is turned On, since the 256 addresses of Accumulator Storage provide a closed loop. It will be noted in FIG. 2*ff* that the Starting Point Counter provides inputs to the Storage Address Counter positions 1, 2, 4, 8, 16, 32, 64, 128 whereas the Storage Select Register provides inputs to positions 16, 32, 64 and 128 only. The upper limit of the word stored in the Core Storage is noted and recognized by a special character called the Storage Mark. The only function of the Starting Point Counter then is to determine the starting address of the Accumulator Storage. The Starting Point Counter can count 000 through 255 and can be stepped either +1, −1 or +128. When the Counter passes 255, it starts off again at 0. The contents of addresses in the Core Storage exceeding 255, are obtained by using the Storage Select Register outputs to positions 16, 32, 64 and 128 of the Storage Address Counter and resetting the 1, 2, 4, 8 triggers to 0. It should now be apparent that Core Storage is logically divided into two portions, each having 256 characters, one portion being referred to as the Accumulator Storage and the other as Auxiliary Storage. Auxiliary Storage has addresses 0 through 255 and Accumulator Storage has addresses 256 through 511. The Storage Select Register is set from either the Memory Buffer Register or from the Console, and two lines of the Storage Select Register Decoding, FIG. 2*ee*, go directly to the Storage Decoders, FIG. 2*tt*, which perform the function of determining whether Auxiliary Storage or the Accumulator Storage is selected. Two lines, **52.24** and **52.41**, from Storage Select Register Decoding, FIG. 2*ee*, to the Storage Decoders, FIG. 2*tt*, indicate whether a position equal to or above 256 or a position lower than 256 is addressed. The 1, 2, 4, and 8 bits of the Storage Select Register are transferred via cable to the 16, 32, 64, and 128 positions, respectively, of the SAC. If the Storage Select Register is not 0, in this case, the 8, 4, 2, 1 bits of SAC are set to 0. In this way the SAC is set to the Storage Unit numbers shown in the Storage Select Register. This fixed Storage Address is 16 for Auxiliary Storage Unit 01, Address 32 for Auxiliary Storage Unit 2, etc., up to Storage Address 240 for Auxiliary Storage Unit 15. The Storage Select Register determines two things: (1) whether the Storage Address Select Circuits will be set to either the upper or lower half of Core Storage, and (2) whether the Storage Address Counter will be set to the Starting Point Counter or to the Fixed Storage Address corresponding to the Auxiliary Storage Unit indicated in the Storage Select Register. The Starting Point is simply an address in storage. When any of the Auxiliary Storage units are used the Starting Point is a fixed Address, but when the Accumulator is selected, the Starting Point may be any address of the upper 256 positions of storage. After the Starting Point Counter has determined the Starting Address of the Accumulator its only other function is to remember the location of the Starting Point in the Accumulator for reference purposes, and to change this starting point while executing certain instructions such as Divide, Multiply, Lengthen, Shorten, etc.

ROUTING LINES

As described, with reference to FIG. 2, there are two classes of lines, namely, Data and Control. Data lines are shown entering the blocks of FIG. 2 at the top and leaving at the bottom. Control lines, which cause the Storage or the Transfer of data, are shown entering the blocks at the left. There are two classes of Control lines, namely, Routing lines and Timing lines. The signals on Routing lines are derived generally from the decoding of the Operations part of an Instruction and are further modified, during Execute cycles, to cause a movement of data to be operated upon according to the Instruction. The Timing lines are combined with the Routing lines to determine when the Routing lines shall be effective to cause the transfer or the storage of data. There are a number of basic Routing lines having signals, which are prerequisites for the execution of Instructions in the Data Processing System and other Routing lines either modify operations of the basic Routing lines or control modes of operation. Numerals following the dash on the legends associated with lines leaving a figure, indicate the fig. No. of the destination.

BASIC ROUTING LINES

In FIG. 93*a*, Read Memory lines **93***a*.**03** through **93***a*.**07** condition circuits for reading five characters out of Core Memory where addresses are determined by MASR. Read Memory (ALU) line **93***a*.**03** is used in combination with timing lines to set CR 1 to the contents of one of the character positions of MBR. Read Memory line **93***a*.**04** is used for PCT Request Execution Controls. Read Memory 1 line **93***a*.**05** goes to Memory Read Gate of FIG. 5*e* to bring up Memory X Read Gate line **5***e*.**02** and Memory Y Read Gate line **5***e*.**05** to Memory Gate Powering of FIG. 5*g*. The signal on Read Memory 1 line **5***e*.**06**, derived from line **93***a*.**05**, goes to Memory Sample Pulse Generator, FIG. 20*e*, to control the MBR Sample pulse on the lines **20***e*.**01** and **20***e*.**02**. The lines just mentioned are up during Use time as determined by the Use line **105.14**.

In FIG. 93*a*, Read Storage Routing controls both the reading out of Storage and the writing into Storage. When a Read Storage signal is provided, one character is read out of Storage and normally one character is written back into Storage. Read Storage line **93***a*.**01** conditions circuits for setting CR 2 to the contents of SBR. Read Storage line **93***a*.**02** conditions circuits found in FIG. 7*d* to provide Storage Read Bias Gate signals on lines **7***d*.**01** and **7***d*.**02** to FIGS. 42 and 36*b*, respectively, Storage Read Gate signals on lines **7***d*.**03** and **7***d*.**04** to FIGS. 37 and 42, respectively, Storage Inhibit Gate signals on line **7***d*.**05** to FIG. 44, and Storage Write Gate signals on lines **7***d*.**06**, **7***d*.**07** and **7***d*.**08** (one line) to FIGS. 38*b* and *c*.

In FIG. 93*b*, CR 1 to Adder (P) line **93***b*.**01** conditions circuits found in Character Registers to Adder Routing of FIG. 73 to route the numeric outputs of CR 1 to the first Doubler, FIG. 80, to the Quintupler, FIG. 81, and the Select One Multiple, FIG. 82, and to route the Zone outputs of CR 1 to the Zone Adder of FIG. 79. CR 1 C Bit Out line **93***b*.**02** goes to the C Bit Generator, FIG. 90, where it gates Result C line **90.01** to the Result Register, FIG. 89*b*, according to the redundancy of the combined zone and numeric portions of the result character. This

permits the character in the Result Register to retain its original bit structure during a Load, Store or Transmit by 1 operation wherein the bit structure is not to be altered.

In FIG. 93*b*, CR 1 to T/C line **93***b*.**03** directs the character in CR 1 to the Digit Adder True Complement Circuits of FIG. 83, via the Adder Input Switching, FIG. 73. CR 1 to T/C line **93***b*.**03** is only up during an Add Memory 2 (Signed Field) operation as indicated in Add to Memory Routing Controls, FIG. 68*b*, when the Memory Field is to be recomplemented. As shown in FIG. 73, the line **93***b*.**03** causes the numerical outputs of the character in CR 1 to be transmitted to the complement circuits of the True Complement Controls, FIG. 83, where the Complement line **93***d*.**07** gates the Complement to the Digit Adder of FIG. 86.

In FIG. 93*b*, CR 2 to T/C lines **93***b*.**04** and **93***b*.**05** route the numerical outputs associated with the character in CR 2 to the Digit Adder True Complement circuits and the zones of the character in CR 2 to the Zone Adder True Complement circuits. The C bit is not routed by the CR 2 to T/C signal. In FIG. 73, the line **93***b*.**04** gates the input lines from CR 2 Outputs of FIG. 75, which represent the character in CR 2, to the Digit Adder True Complement circuits of FIG. 83. In the Zone Adder of FIG. 79 (Sheet 1), the line **93***b*.**05** gates the zone portion of the character in CR 2 to the Zone Adder True Complement circuits of that figure (Sheets 1 and 2).

In FIG. 93*b*, CR 2 C Bit Out line **93***b*.**06** causes the C bit from the character in CR 2, if any, to be transferred to the Result Register, thereby permitting the character in the Result Register to retain its original C bit. This line is up only during a Store for Print, Unload, Store or a Read operation where the bit structure of the character in CR 2 is not to be altered. The line **93***b*.**06** goes to the C Bit generator of FIG. 90 where it gates the CR 2 C line **48.03** onto the Result C line **90.01** to the Result Register of FIG. 89*b*.

In FIG. 93*c*, Adder Out Routing, a Digit Adder Out line **93***c*.**01** routes the output of the Digit Adder Decimal Correction circuits to both the Result Register and the C Bit Generator. If there is no output from the Digit Adder (absence of 1 bits) this line conditions the Decimal Correction circuits to generate 8 and 2 bits (numerical zero) and send these to the Result Register. The Zone Adder Out line **93***c*.**02** routes the A and B bit lines of the Zone Adder circuits of FIG. 79 (Sheet 1) to the Result Register and the C Bit Generator. The Generate C Bit Out line **93***c*.**03** conditions the C Bit Generator for generating of a check bit to the Result Register when the zone and numeric portions of the character entering the Result Register contain an odd number of bits. This line is shown entering the C Bit Generator, FIG. 90, where it is used to generate a positive signal on the Result C line **90.01** when the circuits of the C Bit Generator indicate odd redundancy thereby making the sum of all the bits of the character even.

In FIG. 93*d*, Adder Carry Routing, the Minus (—) on Suppress Adder Carry line **93***d*.**01** prevents the turning On of the decimal carry trigger of FIG. 88 (Sheet 1) to permit special characters to be sent directly through the Digit Adder Decimal Correction circuits, FIG. 87, without correction. On the upper portion of FIG. 88 (Sheet 1) the Minus on Suppress Adder Carry line **93***d*.**01** prevents a carry out resulting from an 8, 4 bit combination, an 8, 2 bit combination, and a Binary Sum 8 Carry. In FIG. 93*d* the Minus on Suppress Zone Carry In line **93***d*.**02** goes to FIG. 88 (Sheet 2) via Sheet 1 of FIG. 88 to suppress setting of the Zone Carry trigger when this line is minus. The Route Decimal Carry In line **93***d*.**05** is up whenever it is necessary to obtain the "tens" complement. This line goes to the Digit Adder, FIG. 86, where it gates a 1 into the "carry in" of the C units position of the Digit Adder.

In FIG. 93*d*, Zone Carry In line **93***d*.**06** is sent to Zone Adder, FIG. 79, (Sheet 1), where it gates a "carry in" to the A bit of the Zone Adder during an Add Memory or Compare operation. In the Add Memory instruction, the Zone Carry In signal is used to add an A bit to the Zone portion of the high order character in Memory for address modification. In the Compare instruction the Zone Carry In signal is used to obtain the "two's" complement from the "one's" complement. The Complement line **93***d*.**07** goes to the True Complement controls, FIG. 83, where it is used to condition the Digit Adder True Complement circuits for complementing the numerical outputs of the character in either CR 1 or CR 2 to effect subtraction by addition in the well known manner.

In FIG. 93*e*, Set Multiple Register to CR 2 line **93***e*.**01** is made positive to put a digit of the multiplier in the Multiple register of FIG. 78 during Multiply 1. As shown in FIG. 78, the numerical outputs of CR 2 are gated to set the Multiple Register triggers. (The Multiple Register is reset to "unity" when the machine is not executing the Multiply instruction.)

Bits can be originated for various reasons and distributed via Adder Emitter lines of FIG. 93*e* and Bit to Adder Routing lines of FIG. 93*f*. The only character emitted is the Blank under control of the lines **93***e*.**04** and **93***e*.**05**. The details of operation of the foregoing lines will not be described except when incidental to the examples of machine operations which illustrate the principles of the invention as later described.

FIG. 93*g* is concerned with routing controls for MAC 1, MAC 2, SAC and SPC. Signals are passed on output lines **93***g*.**01** through **93***g*.**10** to MAC 1, FIGS. 30*a* through *f*, and to Overlap Mode Execution Controls to step MAC 1 plus 1 and minus 1. In FIG. 93*h*, routing lines are provided to MAC 2, FIGS. 31*a* through *f*, to step MAC 2 minus 1 via line **93***h*.**01**, to step MAC 1 plus 5 via lines **93***h*.**02** and **93***h*.**03**, and to step MAC 2 plus 5 via lines **93***h*.**04** and **93***h*.**05**. In FIG. 93*i*, routing lines are provided to FIG. 52 to step SAC minus 1 via lines **93***i*.**01** and **93***i*.**02**, plus 1 via lines **93***i*.**03** and **93***i*.**04**, and plus 128 via line **93***i*.**05**. In FIG. 93j, Storage, Memory and Instruction Counter Routing, output lines provide signals to step the Starting Point Counter plus 1 via lines **93***j*.**01** through **93***j*.**03**, minus 1 via lines **93***j*.**04** through **93***j*.**06**, and plus 128 via line **93***j*.**07**. The line **93***j*.**08** is used in FIG. 52*e* to set SAC to the contents of the Starting Point Counter and the line **93***j*.**09** is used in FIG. 30*f* to set MAC 1 to MAR. Lines **93***j*.**10** and **93***j*.**11** to FIGS. 139*a* and 32*a*, respectively, are positive to reset the Instruction Counter and set the IC to the contents of the Memory Address Register, respectively. The line **93***j*.**12**, Minus (—) on Block Step IC, when positive and in combination with lines **116.09**, **123.34** and **130***a*.**20** serve in FIG. 32*a* to step the IC plus 5 at R_3 time of Execute Character Cycle 1 of each complete operation period in which a transfer is not effected.

Two additional basic routing lines are Result to Memory and Result to Storage. The former is used in the Memory Input Select Switching of FIG. 10 to control the Input Switch of FIGS. 10*a* and *b*, and the latter is used in the Storage Input Select and Switch Circuits of FIG. 43 to transfer the contents of the Result Register to the Storage Inhibit Drivers of FIG. 44. A detailed discussion of the exact use of these routing lines is given later in the description of Overlap Mode Control Circuits and examples of their operation.

TRIGGER CONVENTION

Triggers are widely used throughout the Data Processing System and are bistable devices considered to be Off when the right side is conducting (right plate down or minus) and considered On when the left side is conducting. When a trigger is On, it indicates a "1"; when the trigger is Off it indicates a "0." If a trigger is Off and the right grid is pulsed by negative shift, the trigger is turned On. Likewise, if the trigger is On and the left

grid is pulsed by negative shift, the trigger is turned Off. A negative shift to the left grid of the trigger that is Off causes no change because the pulse is applied to the side that is already Off.

When both grids are suitably coupled together the connection is described as a "Binary Input." A negative input pulse changes the state of the trigger, since the negative shift is effective only on the positive grid thereby causing the trigger to change its state.

ROUTING FOR SETTING CONTROL TRIGGERS

In FIG. 93*k*, routing lines are provided to turn On and Off Auxiliary triggers 1 and 2. FIG. 93*l* illustrates routing lines for turning On Auxiliary triggers 1 and 2 under different conditions than those of FIG. 93*k*. FIG. 93*l* also shows routing lines to turn On the Storage High trigger, to turn Off the Storage High Trigger, to turn Off the Storage High and Low triggers, and turn Off the Remainder trigger. In FIG. 93*m*, routing lines are shown to turn Off the Storage Mark trigger, turn On the Digit Zero trigger, turn Off the Digit Zero trigger, and turn On the Transition trigger used in Overlap Mode Control. FIG. 93*n* illustrates routing lines for turning On and Off the Sign Check trigger, turning On and Off the Overflow Check trigger and setting the Storage Sign plus or minus. In FIG. 93*o*, routing lines are shown to turn On and turn Off the Read/Write Check trigger, turn On and turn Off the Record Check trigger and turn On and turn Off the Instruction Check trigger. In FIG. 93*p*, routing lines are shown for Result to Memory, Result to Storage, Check CR 1 to Adder, Check CR 2 to Adder and Not Erase Memory. FIG. 93*q* illustrates Mode Control routing lines comprising Memory Read Mode, Memory Read/Write Mode, Storage Read Mode and Storage Read/Write Mode for Mode Control as previously mentioned. FIG. 93*r* shows End E Time routing lines which indicate the final Execute cycle of an operation. In FIG. 93*s*, MASR Input Switching, routing lines are shown to set MASR to the Instruction Counter, set MASR to MAC 2, set MASR to MAC 1 and set MASR to SMAC. FIG. 93*t* illustrates routing lines for controlling the Input/Output sequence of operations. FIG. 93*u* shows routing lines to turn On the Auto Transition trigger used in Overlap Mode Control, turn On the Machine Check trigger, turn Off the Machine Check trigger, and turn Off any Signal trigger. In FIG. 93*v*, Block Add Trigger, Suppress Code Checking, routing lines are provided for Minus on Block Add trigger, Minus on Suppress Result Register Code Check, Minus on Suppress CR 1 Code Check and Minus on Suppress CR 2 Code Check. FIG. 93*w* illustrates Neon Indicators which are turned On to indicate the type of cycle such as TC 1, TC 2 and so forth, Parallel Character Transfer Data Check, Parallel Character Transfer Address Check and CR 1 and 2 Code Check Odd.

PARALLEL CHARACTER TRANSMISSION CABLE CONNECTOR

In FIG. 94 a diagram of the Parallel Character Transmission cable receptacle is shown. This is the terminal for those cables shown in composite FIG. 2 and in the logical block diagrams for communicating with input/output devices which handle characters five at a time in parallel. Each of the blocks, when used, contains the name of the line and the number of the line, if any.

THE CLOCK

In FIG. 95, the 1 Megacycle Drive Pulse Generator, the circuits consist of a 1 megacycle crystal controlled oscillator, the output of which is taken from the cathode resistor. Feedback is employed to keep the oscillator running which results in positive spikes each microsecond. The voltage range of these spikes is from 0 to 80 volts and the leading edge in its linear region has a rise time of 0.1 microsecond. The output is powered and inverted yielding negative-going pulses which are distributed as main drive pulses to all sections of the Clock Ring. The main drive pulses on the output lines **95.01** through **95.04** have an amplitude of approximately 45 volts from +140 volts to +95 volts.

The drive ring comprises a Clock Read section, FIG. 96, a Clock Add section, FIG. 97, and a Clock Write section, FIG. 98. The Read section of the ring, FIG. 96, provides five sequential pulses R_0, R_1, R_2, R_3 and R_4. Only one trigger in the clock ring should be On at any one time. Assume, for example, that the R_1 trigger of FIG. 96 is On. The right plate will then be up, conditioning its associated diode gates and upon the fall of the next 1 megacycle drive pulse on the line **95.01** the R_1 trigger is turned Off and the R_2 trigger is turned On. With the R_2 trigger On the right hand plate conditions its diode gate circuits for the next fall of the 1 megacycle drive pulse which turns Off the R_2 trigger and turns On the R_3 trigger. This operation continues until the R_4 trigger is turned Off, at which time either the W_0 trigger of the Clock Write section of the ring of FIG. 98 is turned On or the A_0 trigger of the Clock Add section of the ring of FIG. 97 is turned On. During an Instruction cycle, which is of 13 microsecond duration as explained previously, the output of the R_4 trigger on the line **96.16** conditions the diode gate for the A_0 trigger of FIG. 97 which is further conditioned by the **99.01** line which is up during Instruction time. The fall of the 1 megacycle drive pulse on the line **95.02** turns the A_0 trigger On. The Clock Add section of the ring then provides A_0, A_1, A_2 and A_3 pulses in sequence. The right hand plate of the A_3 trigger conditions the diode gate associated with the W_0 trigger of the Clock Write section of the ring in FIG. 98 via the line **97.08** and upon the fall of the 1 megacycle drive pulse on the line **95.03**, the W_0 trigger is turned On. This and the W_1, W_2 and W_3 triggers in sequence generate W_0, W_1, W_2 and W_3 pulses. Therefore, it is pointed out that on Instructon cycles the Clock Add section of the ring is interposed between the Read and Write portions of the ring for providing a 13 microsecond cycle.

For Execute cycles, the Clock Add section of the ring is not used, and instead, the output of the R_4 trigger on the line **96.17** goes to FIG. 98 where it conditions a diode gate associated with the W_0 trigger. The A_3 (D1) line **97.08** is down, but the Read/Write line **99.02** is up due to the Clock Read/Write and Read/Add/Write switching of FIG. 99. It will be observed in FIG. 99 that when the I time line **124.34** is down the Read/Write line **99.02** is up to condition the diode gate in combination with the R_4 line **96.17** of FIG. 98 so that the fall of the 1 megacycle drive pulse on the line **95.03** turns On the W_0 trigger. After this, the W_1, W_2 and W_3 triggers are turned On in sequence. Then the output from the W_3 trigger is taken from the W_3 (D1) line **98.11** to the Clock Read section of the ring, FIG. 96, where it conditions the R_0 trigger which is turned On next with the 1 megacycle drive pulse. Thus, the Read and Write portions of the ring alternate to provide pulses R_0, R_1, R_2, R_3, R_4, W_0, W_1, W_2, W_3 except during an Instruction cycle when the Add portion of the ring is introduced to prolong the cycle to 13 microseconds. The Clock Reset of the lower portion of FIG. 99 puts the Clock under control of the 1 megacycle drive pulses so that it will operate continuously. When the machine is first turned On the Initial Reset line **106.14** holds the Block R_0 Trigger On Reset line **99.08** down and blocks the pulse that normally turns On the R_0 trigger. At the end of approximately 80 microseconds, the fall of the line **106.14** is used to turn On the Clock Reset trigger which in turn is turned Off by the next one megacycle main drive pulse. This fall is transmitted via line **99.09** to turn On the R_1 trigger of FIG. 96. During the 80 microseconds, the line **99.08** prevents the turning On of the R_0 trigger.

PULSE GENERATORS

Short pulses are described by using index points to designate the time of the leading edge of the wave form and the duration of the pulse to specify the time of fall. For example, if a pulse starts at W_3 and last for 2 microseconds, the description would be W_3 (D2). In the case of longer pulses, index points are used corresponding to the leading and trailing edge of the pulse, thereby designating the duration. For example, a pulse starting at R_0 and lasting for 3 microseconds would be described as R_0–R_3. All pulses are considered positive unless otherwise indicated. A negative 1 microsecond W_1 pulse would be described as a Minus (—) W_1 (D1).

The pulses in the Pulse Generators are of four different durations, 0.4, 1, 2 and 3 microseconds. The 0.4 microsecond pulses are developed by using peakers in the Pulse Generator of FIGS. 100 and 101. The 1 microsecond pulses of FIG. 102 are powered Clock pulses, and the 2 and 3 microsecond pulses of FIGS. 102 and 103*a* use the outputs of Clock controlled triggers, that is, a trigger is turned On by the fall of a Clock pulse and turned Off by the fall of another Clock pulse and the output pulse is taken from the right side of the trigger. Some of the pulses are mixed with conditioning lines such as Use and Instruction and are generally further conditioned in the logical circuits by control lines as stated previously. FIG. 103*b* shows powering for certain of the pulses generated in FIG. 103*a*, and, in one instance, a pulse is combined with Use line **105.10**. FIG. 104 illustrates the Pulse Generator for pulses having 3 and 4 microsecond durations, utilizing triggers which are set and reset by Clock pulses. FIG. 105 shows the Use trigger which sets the status of the calculator in Use or Manual. The Use trigger is On when the calculator is in automatic operation, during which it gates pulses necessary to carry out the reading and execution of Instructions in the stored program. When the machine is stopped and operated under control of the Operator's Console, it is in the Manual status, and the Use trigger is Off. However, Manual operations can generate one or more Use cycles to carry out the execution of the Manual operation via the Single Use Cycle trigger of FIG. 105, or else by causing the machine to pass from Manual status to Use status by turning On the Use trigger.

RESET AND START/STOP CONTROLS

In FIG. 106, the Reset keys and associated controls and the Clear Memory key and associated controls are shown. Depressing either of the Reset keys while the machine is in Manual status, turns Off all of the Check Indicators and the Any Signal Indicator and also sets the Instruction Counter to 0004. Depressing the Clear Memory key resets the clock, causes all of the functions ascribed to the Reset key and, in addition, sets all of the Core Storage to Storage Marks (an absence of bits) and sets all of the Core Memory to Blanks (a C and an A bit). The Clear Memory trigger associated with the Clear Memory key of FIG. 106 is shown in FIG. 107 along with the Clear Storage Single Shot. FIG. 108 illustrates the Manual Start/Stop controls. The Start key is used to place the system in Automatic status and when depressed, it turns Off all of the Check Indicators and the Any Indicator. Each of the Stop keys, when depressed, places the system in Manual status at the end of E time of the Instruction which is then being performed. The Single Use cycle key causes one cycle of an operation to be executed for each key depression. FIG. 109 illustrates the Stop controls. Depression of the Machine Stop key places the system in Manual status immediately and does not wait until the end of E time as the Manual Stop key does. The Manual Store key and controls are shown in FIG. 110. The Store key permits the operator to enter characters into Core Memory manually (Characters may not be stored directly in Storage). If the system is in Automatic status when the Store key is depressed, the system goes into Manual status at the end of E time of the Instruction which is then being performed. The Memory Address Selector must be set, then upon depression of a key on the Console Character Keyboard, the character entered in the Character Keyboard is thereby stored in Memory.

FIG. 111 illustrates the Manual Instruction controls to permit the operator to manually instruct the Data Processing System. Depressing the Manual Instruction key causes the machine to enter Manual status at the end of E time of the Instruction which is then being performed. The address of the Instruction, including the Storage unit designation, if any is needed, is then set in the Memory Address Selector Keyboard and in the Storage Selector. The key of the Character Keyboard corresponding to the Instruction to be performed is then depressed and will cause that instruction to be executed.

Manual display controls are illustrated in FIG. 112. The purpose of the Display key and Display Step key is to put the machine in Manual status and to permit the operator to observe the contents of the Core Memory and of the Core Storage units. Memory is shown in the Memory Display of CR 1, the Storage unit selected by Storage Selector keys is shown in Storage Display CR 2 and each time the Display Step key is depressed an adjacent character is displayed.

Memory Test controls are shown in FIG. 113. In FIG. 114 the Half Multiple Step controls are shown for the purpose only of completing circuits within the machine wherein depression of the Half Multiple Step key causes the computer to perform either the I time or E time of an Instruction operation each time the key is depressed. When the key is being continuously depressed, the computer goes into Automatic status for long enough to execute one half of an I or E cycle and then after a delay of about 0.75 second, proceeds to successively execute I times or E times of the Stored program, but at a rate of about eight per second. Should the key be depressed while the machine is in Automatic status, the machine will be placed in Manual status. The Half Step trigger for use with the Half Multiple Step control, FIG. 114, is shown in FIG. 115. Manual Timer triggers, FIG. 116, the Manual Timer Execution controls, FIG. 117, and the Manual Execution controls, FIG. 118, taken together, provide circuits for the manual operation of the system by the depression of the manually operated keys described above.

Check Indicator switches are shown in FIG. 119 and comprise the Instruction Check switch, Machine Check switch, Overflow Check switch, Sign Check switch, Read/Write Check switch and Record Check switch. The switches are normally kept in the Automatic position and for certain errors in machine operations the Halt line **119.01** and the Auto Block line **119.02** are made positive to place the machine in the Manual status for corrective action.

ALTERATION SWITCHES

In FIG. 120*a* six Alteration switches are shown which are used to vary the sequence of machine operations according to a predetermined plan. They are manually settable and each Alteration switch has a specific address as indicated in Chart III. If a switch is On when interrogated by the program, a transfer is made; if a switch is Off, no action takes place, except that the machine proceeds to the next Instruction.

AUDIBLE SIGNAL INDICATION

Referring to FIG. 120*b*, the purpose of the Audible Signal Indication is to attract the attention of the operator to the fact that the machine has stopped its processing because of either a planned condition due to the program or an unplanned condition due to a fault. A pleas-

ant tone sounds whenever the machine shifts from Automatic to the Manual status because of conditions above. The operator may turn Off the tone by the Audible Signal Reset key, but the tone will sound on a subsequent stop. The operator can make the device completely inoperative during checking by use of the Audible Signal switch.

FIG. 121 shows the I/E trigger which is used for defining Instruction and Execute times. The IA (Indirect Address trigger) trigger also shown in FIG. 121 is turned On for indirect address instructing. An Instruction with an indirect address can be defined as one in which the address portion does not refer directly to the position or location of the data to be processed but to a location that contains the address of data to be processed. The address contained in the Instruction is called the Indirect Address and the address to which the latter refers is called the Effective Address. Indirect Addressing is identified by a binary "1" in the A bit position of the Low Order character of the Instruction Address, and the Turn On IAT line **61.07** is up from I time routing controls of FIG. 61 due to coincidence between the Use line **105.09**, the I time line **124.29** and the CR 1 A line **59.27**.

ECC 1 AND ECC 2 TRIGGERS

ECC 1 and ECC 2 are types of Execute cycles which define portions of Execute time, as mentioned previously. The first Execute cycle (ECC 1) begins at W_2 time when the I/E trigger changes from I to E and the ECC 1 trigger is turned On. Following ECC 1 is the ECC 2 cycle, after which there occur as many Execute cycles as are necessary to complete the Instruction. FIGS. 123 and 124 show the I/E Timer outputs which are distributed from FIGS. 61, 121 and 122.

LOAD, UNLOAD AND STORE ROUTING CONTROLS

FIGS. 125*a* through 125*c* disclose the routing lines for Load, Unload and Store Instructions.

The Load instruction permits single characters, any series of characters, or fields to be entered into Storage from Memory. The number of characters or length of the field entered into Storage is determined by the position of the Storage Mark relative to the Starting Point Counter. The address part of the instruction specifies the location of the right-hand character of the field in Memory and the Storage unit to be used. Characters are entered right to left from Memory until the specified Storage space is full.

The Unload instruction is used to place a specified portion of Storage in Memory and the number of characters unloaded into Memory is equal to the number of positions in the Storage unit. The right-hand character of the designated Storage unit is unloaded into the Memory position specified by the address part of the Unload instruction and remaining characters in Storage are entered successively into Memory until a Storage Mark is sensed.

The Store instruction is used to place a specified numeric field of Storage in Memory as illustrated by example previously.

STORE FOR PRINTING

FIGS. 126*a* and *b* illustrate the logical circuits for providing signals on routing lines for carrying out the Store for Print instruction, which is normaly used to transfer a numeric field from Storage to Memory where it may be used subsequently for writing by a printer. When the sign of the specified Storage unit is plus, a blank is stored in the Memory location designated by the address part of the Instruction. When the sign of the Storage unit is Minus, a dash is stored in the Memory location designated by the address part of the Instruction. The numeric Storage field is stored in the Memory locations directly to the left of the sign position until a Storage Mark is encountered which sets the left-hand limit of the field stored.

TRANSMIT AND SEND

FIGS. 127*a* and *b* illustrate the circuits for providing routing signals for Transmit and Send instructions. A Transmit instruction is used preceded by a Receive instruction for transferring data from one portion of Memory to another.

A Send instruction is similar to the Transmit instruction in that it causes high-speed movement of data from one location in Memory to another in five character groups, but it eliminates the necessity of placing a record mark to stop the transmission since the amount of data transmitted is controlled by the length of a preset Storage unit. More specifically, if the RWW trigger is Off, data are moved, five characters at a time, starting at the address of the Instruction to a receiving location determined by the setting of MAC 2. One group of five characters is moved for each character contained in the Accumulator or designated Auxiliary Storage Unit. If the RWW trigger is On at the time the Send instruction is decoded, a high-speed redundancy check is made on the contents of Memory starting at the address of the Send instruction and continuing through the end of the respective Memory block. Detection of a redundancy error in the specified Memory block turns On the Machine Check Indicator.

BLANK MEMORY

FIG. 128 illustrates the circuits for providing routing signals for the Blank Memory instruction. A Blank Memory instruction is used to erase Memory. A Receive instruction is given which specifies a starting address in Memory and then a Blank Memory instruction is given which specifies the number of five character groups to be erased if high speed erase is indicated by Accumulator coding and the number of characters to be erased if low speed erase is indicated by ASU coding. If the address part of the Blank Memory is Accumulator coded, Memory is erased in five character groups starting at the address contained in MAC 2. The number of five character groups to be erased is specified by the Memory address portion of the Instruction. If the Instruction is coded ASU 01, single characters are erased at a time, and if ASU coding refers to an ASU other than 01, the machine interprets the ASU coding as 01.

SET LEFT, LENGTHEN AND NORMAL TRANSITION ROUTING CONTROLS

FIGS. 129*a* through 129*d* illustrate circuits for routing signals for Set Left and Lengthen instructions and for Normal Transition operations.

The Set Left instruction adjusts the length of the specified Storage field to the number of characters designated by the address part of the instruction by moving the Storage Mark. The operation starts with the character referred to by the Starting Point Counter and continues to the left of the field, character by character, until the number of Storage positions specified by the address have been examined. When a Storage Mark is detected, it is replaced by a zero and then zeros are placed to the left in all remaining high order positions of the adjusted field. If a Storage Mark is not sensed within the designated field, a Storage Mark is inserted to the left of the high order character of the field. Therefore, the number of characters in a field may be increased or decreased. The Set Left instruction may precede a Load instruction to adjust a field in Storage to the size of the field to be entered therein.

The Lengthen instruction causes the Starting Point Counter to be shifted right (minus) a number of positions specified by the address part of the Instruction. For each position moved by the SPC, a zero is inserted in the corresponding position of Storage.

SHORTEN RIGHT AND ROUND ROUTING CONTROLS

FIGS. 130*a* through 130*c* illustrate circuits for providing routing signals for Shorten Right and Round instructions.

The Shorten instruction shifts the SPC to the left the number of positions specified by the Memory address portion of the Instruction. Since the field in Accumulator Storage is defined by the position of SPC and the Storage Mark, the movement of SPC left (plus) has the effect of removing characters from the right end of the field.

The Round instruction moves the SPC to the left the number of positions specified by the Memory Address portion of the Instruction. Thus, the field remaining is defined by the Storage Mark and the new position of SPC. A five is added to the adjacent right-hand digit with respect to the SPC, and a resulting Carry is added to the units digit of the field. If a Carry is generated out of the highest order position, the field is extended one position to the left to include the Carry.

READ/WRITE SELECT AND CONTROL ROUTING CONTROLS AND INPUT/OUTPUT CONTROLS

FIGS. 131, 132*a* and 132*b* disclose circuits for providing routing signals for Reading and Writing operations of Input/Output devices. FIG. 133 illustrates the routing lines for Select and Control operations. FIGS. 134*a* through 134*f* disclose I/O Sequence triggers and controls for I/O operations and FIGS. 135*a* and 135*b* illustrate Parallel Character Transfer Request and other operations directed to parallel transmission for Input/Output devices.

OVERLAP CONTROL

FIG. 136*a* illustrates the Overlap Control triggers, namely, the Transition trigger, Auto Transition trigger, Add trigger and Mode Control trigger; FIG. 136*b* shows additional controls for the Execution of Overlap operations; FIG. 136*c* is Transition Powering for the Transition line; FIG. 136*d* is Powering for the Not Transition line and the Add trigger; and FIG. 136*e* shows Powering for Transition trigger and the Mode Control trigger. These triggers just recited are those which control the Overlap Modes of operation. Briefly, the Transition triggers define certain cycles during which complete overlapping of Memory and/or Storage operations and Arithmetic operations is not performed; the Add trigger defines the portion of Execute time when computation may be performed in the ALU; and the Mode Control trigger defines Overlap and Transition cycles where results are placed in Memory or Storage.

RESULT TO MEMORY AND RESULT TO STORAGE TRIGGERS

As mentioned previously when the Result to Memory and Result to Storage Routing lines were discussed, FIG. 137 shows the triggers which are set by positive pulses to provide the Routing signals on the lines **137.01** through **137.06.**

SPECIAL CONTROL TRIGGERS

FIG. 138*a* illustrates the Storage Low trigger and the Storage High trigger; FIG. 138*b* the Simultaneous Read/Write trigger and the Read Call trigger for I/O operations; FIG. 138*c* the Storage Mark trigger and the MAC 1=0 trigger; FIG. 138*d* the Any Signal trigger and Powering the Storage Mark trigger Off line; FIG. 138*e* the Write Call trigger, No Write Response trigger and the No Read Response trigger for I/O operations; FIG. 138*f* the Instruction Check trigger, Machine Check trigger, Read/Write Check trigger for storing indications of error conditions; FIG. 138*g* the Record Check trigger, Overflow Check trigger, the Sign Check trigger for storing indications of error conditions; FIG. 138*h* the Digit Zero trigger (DZT) and the Remainder trigger; FIG. 138*i* the Auxiliary Trigger 1; FIG. 138*j* the Auxiliary 1 Off Powering; FIG. 138*l* the Auxiliary Trigger 2 Off Powering and FIG. 138*k* the Auxiliary Trigger 2.

RESETS AND CLAMPS

FIG. 139*a* shows circuits for providing reset signals for various triggers either to establish a specific status when power is first applied, to reset to a specific status intentionally via Manual Reset Keys of FIG. 106 or to reset the triggers automatically in preparation for subsequent operations when new information may be set in the triggers. To prevent delay in changing the state of a trigger, the grids of the tubes are clamped at minus 12 volts. For those tubes without electronic reset, the grids of the tubes are clamped at minus 12 volts via a diode having its plate connected to a −12 volt supply and its cathode connected to the grid of the tube. The point for electronic reset is usually the plate of a diode, similarly connected as above, which is fed by a Reset Cathode Follower (KR) having an output of −12 volts for an input of −30 volts thereby clamping the grid at −12 volts. When the input to the KR changes to +10 volts, its output goes to 0 volts and forces a non-conducting grid up via the interconnecting diode. The notation for reset is placed in the title section of the trigger logic block; for example, in FIG. 17*a*, the W of TBW indicates a "W" reset Off. In instances where a trigger is reset On, the reset indicator appears to the left, for example WTB. Reset pulses may be applied, of course, to other portions of a trigger in manners well known in the art.

Instruction reset, those occurring during Instruction time at R_0, are provided on the lines **139***a*.**01** and **139***a*.**03**. The MAR Reset signal on the line **139***a*.**01** resets MAR to zero in preparation for its receiving the Memory address portion of the Instruction obtained from Memory during the Read portion of the Instruction cycle. The Instruction Reset line **139***a*.**03** goes to FIG. **139***b* where it is powered by cathode followers and distributed as (X) resets to the Storage Select Register, FIG. 16*a*, on the line **139***b*.**01**; the Operation Register, FIGS. 21*a* and *b*, on lines **139***b*.**02** and **139***b*.**03**; the triggers of FIGS. 139*b* through *k* on the lines **139***b*.**04** through **139***b*.**09**; the Reset Add, Reset Subtract, Add-Subtract Routing Controls of FIG. 74*a* on the line **139***b*.**10**; the Multiple Routing Controls of FIG. 67*a* on the line **139***b*.**11**; the Select and Control Routing Controls of FIG. 133 on the line **139***b*.**12**; the I/O Controls of FIGS. 134*a*, *d* and *e*, on the lines **139***b*.**13** through **139***b*.**15**; the Quintupler, Doubler and Quadrupler, and Multiple Register of FIGS. 81, 80 and 78 on the lines **139***b*.**16** through **139***b*.**18** respectively; the Decimal Correction Circuits of FIG. 85 on the line **139***b*.**19**; the Overlap Control triggers of FIG. 136*a* on the line **139***b*.**20**; the Decimal Carry and Zone Carry triggers of FIG. 88 (2 Sheets) on the line **139***b*.**21**; the Inter-Reg. Check trigger of FIG. 63*c* on the line **139***b*.**22**; the Unload Address Controls of FIGS. 65*a* and *b* on the lines **139***b*.**23** and **139***b*.**24**; and the Add to Memory Routing Controls of FIG. 68*a* on the line **139***b*.**25.**

Machine Reset line **139***a*.**02** of FIG. 139*a* goes to FIG. 139*b* for powering and distribution on the lines **139***b*.**26** through **139***b*.**35**. In FIG. 139*a*, Instruction Counter Reset, Select Register Reset, and MAC 2 Reset signals are provided on the lines **139***a*.**04** through **139***a*.**06** to powering and distribution of FIG. 139*c*. To reset the Memory Buffer Register in preparation for receiving five characters from Memory, the line **139***a*.**07** is positive during Use time or PCT Request for the Not Erase Memory condition and is combined in FIG. 5*g* with a W_3 (D2) pulse on the line **7***d*.**10** to provide signals on the lines **5***g*.**13** and **5***g*.**14**, the latter being connected to MBR triggers of FIGS. 14*a* and *b* as (Z) resets.

In FIG. 139*c*, the lines **139***c*.**01** and **139***c*.**02** are positive at W_3 (D2) during Use time to provide (R) resets to the Result Register at W_3 time after its contents are no longer required for use. The Initial Reset line **139***c*.**13**, originating in Manual Reset Keys of FIG. 106, provides

(U) reset to the Single Cycle Use trigger of FIG. 105. Other signals on input lines from FIG. 139*a* are merely powered and distributed to MAC 2, IC, Select Register and MAR.

FIGS. 139*d* and *e* disclose −12 volt supplies as mentioned previously for use in clamping the grids of triggers. Inputs (not shown) are from the power supply for the Data Processing System.

COMPARE ROUTING

FIGS. 140*a* through 140*c* illustrate the Routing lines for the Compare Instruction, which compares a specified Storage field with a Memory field designated by the Memory Address portion of the Instruction. The comparison begins with the units order of each data group and proceeds from right to left, character by character, until a Storage Mark is sensed. The results of comparison are made available to program interrogation (Transfer instructions) by means of High and Low triggers, FIG. 138*a*, which may be turned On for high or low comparison depending on whether the contents of Storage are higher or lower than the specified contents of Memory. In addition, any unequal condition turns On Auxiliary 1 trigger of FIG. 138*i*. If at the end of execution of the Compare instruction only one of the triggers is On or if both the High and Low triggers are On, the Machine Check trigger of FIG. 138*f* is turned On. High and Low triggers are changed only by execution of a subsequent comparison in the program and are not changed by interrogation.

MISCELLANEOUS

FIG. 141 discloses the circuits for the Auto Load control.

The Auto Load key, FIG. 141, when depressed, causes the following sequence of operations: Selects the Input/Output unit addressed by the keys of the Memory Address Selector, resets the registers and counters including the Check indicators, and sets the IC to 00004, reads one record into Memory starting at position 00000, and initiates Automatic operations whereby the stored program is introduced into Memory.

FIG. 142*a* illustrates circuits for the Reference Voltage Regulator and the D.C. Alarm. FIG. 143 discloses Open Filament Detection circuits for giving an indication of an open filament in the machine.

SETTING OF COUNTERS AND REGISTERS

Two general circuit schemes are used to accomplish the setting and resetting of counters and registers as follows: (1) an electronic reset is employed and one input line for each trigger is used for application of the setting pulse in response to a binary value as in the Memory Buffer Register of FIG. 14*a*, (2) the register is not reset in the manner above but instead two inputs to each trigger are employed. As an example of (2), the Character Register 1, FIG. 57, is turned On with a positive pulse to the left hand grid and is turned Off with a positive pulse at the right hand grid in response to the binary input indication. Therefore, means to reset all triggers to the Off condition before setting is not required since those triggers which are On and should be set On are unchanged, while those On which should be Off are turned Off and those triggers which are Off and should be On are set On.

An example of electronic reset as in (1) mentioned above is found in the circuits of FIG. 17*a* where a −12 volt clamp voltage is applied to the right-hand grid of one of the tubes of a trigger as indicated by "W." The clamp voltage is changed to 0 volts at reset time and the right side of the trigger goes into conduction indicating the Off condition of the trigger.

COUNTERS (GENERAL DISCUSSION)

Two types of counters are used in the Data Processing System. One type is of a modified binary arrangement in which four triggers are arranged to represent the decimal values of 0 through 9 with outputs of 8, 4, 2 and 1 as shown in the first order of MAC 1 in FIG. 30*a*. Storage Address counters comprise eight stage binary counters consisting of eight triggers arranged in tandem to represent 0 through 255, such as the Storage Address Counter of FIGS. 52*a* through *d*.

All the counters except the Instruction Counter of FIG. 32 can step up one count. FIG. 30*a* illustrates a group of four triggers in the modified binary arrangement. Assuming that all triggers are initially Off, one pulse on the MAC 1+1 or +5 line **30*f*.01** to the 1 trigger would turn the trigger On causing the right plate to rise. The positive shift on the right plate lines **30*a*.13** and **30*a*.14** has no effect on the following trigger (2 trigger) because the diode associated with the right plate of the 1 trigger and input of the 2 trigger is conditioned to pass only a negative shift. The next pulse turns the 1 trigger Off causing the right plate to drop and the negative shift turns the 2 trigger On. With the occurrence of the third pulse, the 1 trigger is turned On and the 2 trigger remains On for a count of 3. The fourth negative shift input pulse to the 1 trigger turns Off the 1 trigger, which feeds a negative shift from its plate to the 2 trigger turning it Off. As the 2 trigger goes Off, the fall of its right plate turns On the third trigger (4 trigger). A pure four stage binary counter can count from 0 to 15, but such a counter modified to count only from 0 to 9 must restore to 0 when a count of 9 is reached. To achieve this result the negative level from the left plate of the 8 trigger is arranged to block the input to trigger 2. The ninth input pulse leaves the 1 trigger and the 8 trigger On. The tenth input pulse turns Off trigger 1 and its right plate negative output turns Off trigger 8. The result is then 0.

Counting down requires that the carries from the 1, 2 and 4 triggers be taken from their left plates and the output of the left plate of 8 trigger be coupled to the left grids of the 2 and 4 triggers. Assuming that all triggers are Off, a first input pulse on the Step MAC 1–1 line to the 1 trigger turns it On causing the left plate to drop. The fall of the left plate turns On trigger 2 and then trigger 4 and then trigger 8 are turned On in like manner. Thus, for one instant, all triggers are On and the counter has counted down from 0 to 15. But, turning On the 8 trigger prevents the counter from staying 15 since the output of the left plate of trigger 8 is coupled to the left grids of triggers 2 and 4. When trigger 8 goes On, its left plate falls generating a negative shift that turns Off triggers 2 and 4. The result, then, is that triggers 1 and 8 are left On and the counter stands at 9. With the trigger standing at 9 (the 8 and the 1 triggers On) a second input pulse turns the 1 trigger Off and the counter stands at 8. The third input pulse turns On the 1 trigger which then causes the 2 trigger to turn On. The turning On of the 2 trigger then causes the 4 trigger to turn On which in turn causes the 8 trigger to turn Off. Accordingly, the counter now stands at 7. The counter continues to count down in the binary fashion.

The step plus 5 signal is introduced into the units position of the counter which must sit at either 4 or 9. Assume that the first order of MAC 1, FIG. 30*a*, is set at 4 (the 4 trigger is On). The Step MAC +5 line **93*h*.02** conditions a diode gate connected in binary fashion to the 4 trigger and the pulse on line **30*f*.06** turns Off the 4 trigger. The same pulse turns On the 1 trigger via the diode gate conditioned by the Step MAC 1+1 or +5 line **30*f*.01** and which is connected in binary fashion to the 1 trigger. The turning Off of the 4 trigger sends a negative shift to the right grid of the 8 trigger turning the latter On. The first order of MAC 1 now stands at a value of 9. A second stepping pulse on lines **30*f*.01** and **93*h*.02** turns Off the 1 trigger and turns On the 4 trigger. The turning Off of the 1 trigger sends a negative shift to the left grid of trigger 8 turning Off the latter. The

turning Off of the 8 trigger sends a negative carry pulse on the right plate to the second order of the MAC 1 and the first order stands at 4.

MEMORY CONTROLS

The Memory Address Select Register, FIGS. 49*a* through *h*, comprises seventeen triggers which contain the Memory Address that is to be interrogated to obtain five characters from Core Memory. All of the Memory Address Select Register outputs, except the $\overline{40,000}$ and the 40,000 lines of the fifth order are decoded in four Decoders of FIGS. 3*a* through *d* for X and Y selection purposes. These are the 4×10 Decoder (thousands order, FIG. 3*a*), the Memory 4×10 Decoder (tens order, FIG. 3*b*), the Memory 4×10 Decoder (hundreds order, FIG. 3*c*), and the Memory 6×8 Decoder (units order, FIG. 3*d*). Only one input from each decoder is up. The first step is to supply Read Bias and to accomplish this the 4×10 Decoder of FIG. 3*b* provides a signal on one of the output lines to its output inverters, FIG. 5*a*, the latter providing complementary outputs on the pair of lines selected to the Switch Core Write Driver circuits of FIGS. 5*b* and *c*. In FIG. 5*a*, it will be noted that only one input line is positive and the remainder are negative. The negative input signals are present on all of the odd numbered output lines except the one associated with the positive input signal, and the negative input signals are inverted by Inverters IJK to provide positive signals on all even numbered output lines (NOT lines) except the one associated with the positive input signal. The 6×8 Decoder, FIG. 3*d*, provides a signal on one of its output lines to its output inverters, FIG. 7*a*, the latter providing complementary outputs to the Switch Core Write Driver circuits of FIGS. 7*b* and *c*. In FIG. 7*a*, the circuits function as explained with reference to FIG. 5*a*. In FIGS. 7*b* and *c* the outputs from the 6×8 Decoder Output Inverters, FIG. 7*a*, are mixed with Memory Read Bias Gate pulses on the lines **5***g*.**11** and **5***g*.**12** to provide an output down signal on one of the lines to the X Switch Core Write Windings of FIG. 9. Signals from the 4×10 Decoder Output Inverters of FIG. 5*a* are mixed with Memory Read Gate Bias pulses on the lines **5***g*.**09** and **5***g*.**18** in the Memory Y Switch Core Write Drivers of FIGS. 5*b* and *c*. A single output line is thereby energized to the Y Switch Core Write Winding of FIG. 8.

To supply Read Bias Current to the X and Y Switch Core Matrices, FIGS. 8 and 9, all write inputs except one to each of the matrices are pulsed with Read Bias current. The next step is to generate Read current and to accomplish this the two 4×10 Decoders, FIGS. 3*a* and c, have one of their output lines up in response to signals from the Memory Address Select Register, FIGS. 49*g* and *e*. A signal from the 4×10 Decoder, FIG. 3*a*, and the signal from the 4×10 Decoder, FIG. 3*c*, is present on one of the input lines of the Switch Core Read Drivers, FIGS. 4 and 6, respectively. In FIG. 4, a signal on one of the output lines transfers a signal associated with the address to the Switch Core Read Windings of FIG. 8 when the Memory Y Read Gate line **5***g*.**08** is up. Similarly, a signal on one of the output lines of the Memory X Switch Core Read Drivers of FIG. 6 is transferred to the X Switch Core Read Windings of FIG. 9 when an impulse is provided on Memory X Read Gate line **5***g*.**07**. In FIG. 8, each of the switch cores has three windings, two primary input windings, Read and Write, and a secondary output winding are arranged to be approximately one to one between any of the windings. As an example, consider the switch core at the intersection of the lines **8.10** and **8.11**. The Primary Read winding is represented diagrammatically by the passage of the line **8.11** through the core. The Primary Write line is illustrated diagrammatically by the passage of the **8.10** line through the core. A secondary or output winding is illustrated diagrammatically as the line which bears the address 29,080. Secondary windings feed the Y lines for the Memory Core Array. All switch cores are normally reset and the object of providing inputs to this matrix is to set and reset one of the switch cores using the Read and Write inputs. Since Read and Write windings are connected in series by rows and columns current supplied from an input line magnetizes all cores in its row or column. As stated previously, all of the Write inputs except one are supplied with Read Bias current from the Y Switch Core Write Drivers, FIGS. 5*b* and *c*, whereas only one of the Read lines is energized by the Core Read Drivers of FIG. 3. Since all switch cores are normally reset and Read Bias current tends to reset the cores then the result of the Read operation is to set a core in response to a signal on one of the lines **8.11** through **8.20** in the absence of a signal on one of the lines **8.01** through **8.10**. The Selection process can best be shown by an example which will be given hereafter, but for the present let it be assumed that one of the secondary windings couples the signal caused by a switch core being set to the Core Memory Array of FIG. 13 on one of the hundred output lines from FIG. 8. Similarly in FIG. 9, the X Switch Core Matrix has a selected one of the switch cores set by application of Read Bias Current on all but one of the Write lines from the Write Drivers of FIGS. 7*b* and *c*, and Read current supplied on one of the Read lines in the Core Read Drivers of FIG. 6, causing one of the cores to be set and a current induced in the secondary which is provided on one of the 80 lines to the Core Memory Array of FIG. 13.

FERRITE CORE PLANES

In FIG. 13, four insulated wires pass through each ferrite core as indicated diagrammatically by the intersection of lines in the Matrix (also see FIG. 2*by*). One is an X Address line (such as 29,080) for each horizontal row, one is a Y Address line (such as 10,915) for each vertical column, another is a sense winding passing diagrammatically through the intersections as shown and common to all the cores in a plane and the last is an inhibit winding passing through the intersections parallel to the X winding as shown in the drawing and common to all cores in the plane. Only one core can be selected from a plane during any given cycle and the selected core is located at the intersection of the selected X and Y lines, which are each pulsed with half select current at Read time. This coincident current at the intersection of X and Y lines applies full Read current to the selected core tending to change it to the "0" state. During Write time the same X and Y Address lines are selected and each pulsed with half select current such that full Write current is applied to the selected core tending to change it to the "1" state. By pulsing the inhibit winding which is parallel to the X winding with current opposite to the half select current flowing in the X winding (effectively half read current), the switching of the selected core to a "1" is prohibited.

A sense winding passes through all cores in each plane, and since only one core in each plane is interrogated during a cycle, no ambiguity of output will result. At the time the selected core is changing state during reading (if it contained a "1"), the sense line is sampled and the presence of a "1" detected. The Read current sets one Switch Core in each of the X and Y Matrices and the setting of the Switch Cores generates half Read current on one X and one Y Address line feeding 35 planes of Core Memory in parallel. At the points of coincident current, 35 ferrite cores (one for each plane) are provided with full Read current which resets any of the 35 cores holding "ones." Resetting the Cores holding "ones" induces pulses on the corresponding Sense Windings which are amplified in the Sense Amplifiers of FIGS. 15*a* and *b*. The outputs of the Sense Amplifiers are sampled at approximately R_3 time, and these sampled pulses turn On those ones of the Memory Buffer Register triggers of FIGS. 14*a* and *b* corresponding to the Cores that held

"ones." Information is retained in the Memory Buffer Register until the end of the cycle when characters of the Memory Buffer Register are used for processing or rewriting back into Core Memory. Core Memory design fixes a relationship between the Core Plane configuration and the Memory Buffer Register since five characters are read at a time. Character addresses ending in 4 or 9 are placed in the Character 4 position of the Memory Buffer Register, while addresses ending in 3 or 8 are placed in Character 3 and so forth.

As mentioned previously, the Memory Buffer Register outputs are provided to six places: The PCT Write Bus, FIGS. 18*a* and *b*; the Output Switch, FIGS. 20*a*, *b*, *c* and *d*; the Memory Address Register, FIGS. 2*r*, *s* and *t*; the MBR Code Check, FIGS. 19*a* and *b*; the SSR, FIGS. 16*a*, *b*, *c* and *d*; and the Input Switch, FIG. 11. Characters are processed in the ALU serially, and therefore one character must be selected from the five characters retained in the Memory Buffer Register. The Output Switch chooses one character of the five for processing (except for Instruction cycles and Transmit by Five operations), and the one character selected by the Output Switch is gated to the Memory Out Bus and placed in CR 1. More specifically, the X and Y Switching Circuits decode the Memory Address Select Register address and select the five character group that contains the desired character. The final selection to obtain a single character is determined by the units position of the address via the Memory 4×5 Decoder, FIG. 3*e*, sometimes called the Select Character Switch which decodes the units position of the address contained in the Memory Address Select Register. In accordance with the Core Plane to Memory Buffer Register relationship, the following conditions must be met: if the units position of the address ends in 4 or 9 then the character in position 4 of the Memory Buffer Register is designated for processing. Select character 4 from the 4×10 Decoder, line **3*e*.09** comes up if the units position of Memory Address Select Register contains a 4 or 9. This gates the desired character 4 to the Memory Out Bus. If the units position of the address is 3 or 8 then the character in position 3 of the Memory Buffer Register is wanted for processing. Therefore, Select character 3 line **3*e*.07** is up for this situation.

The following table lists the units position of the address and the corresponding select character lines:

Units position of Memory Address Select Register	Select Character Line
4 or 9	3*e*.09
3 or 8	3*e*.07
2 or 7	3*e*.05
1 or 6	3*e*.03
0 or 5	3*e*.01

Each cycle using Core Memory is a complete operation with respect to Memory and Reading and Writing are both performed in one cycle during the Read and Write portions explained previously. For single character processing involving Core Memory, Memory Address Counter 1 steps through the data field sequentially. Because Core Memory reads and writes five characters simultaneously, five cycles are required to process an entire five character group. Thus, the same addresses are read out and written into Memory five times. When one group is completely processed operation shifts to the next group and so forth. However, it is pointed out that processing can start and stop anywhere in a five character group because each cycle is a complete operation with regard to Core Memory. As the Memory Address Select Register follows Memory Address Counter 1, the select character lines **3*e*.09**, **3*e*.07**, **3*e*.05**, **3*e*.03** and **3*e*.01** are routed individually as determined by the 4×5 Decoder of FIG. 3*e*. One of these select character lines **3*e*.01**, **3*e*.03**, **3*e*.05**, **3*e*.07**, **3*e*.09** remains up for the entire cycle since the Memory Address Select Register is set only at R_0.

In Instruction cycles, all five characters of the Memory Buffer Register are used. Character 0 from the MBR is placed in the Operation Register. Numeric portions of Characters 1 through 4 A and B bits of Character 1, and the B bit of Character 4 of the MBR are placed in the Memory Address Register. Numeric portions of Characters 1, 2 and 3 and the Zone bits required for addressing in Characters 1 and 4 are placed directly in MAR and the numeric portion of position 4 of MBR is transferred indirectly to the MAR via the Memory Out Bus. This latter transfer is permissible as all Instruction addresses must end in 4 or 9 which means that Select Character 4 line **3*e*.09** is always up on Instruction cycles, thus gating position 4 or MBR through the Output Switch. The Memory Out Bus feeds CR 1 as well as the units position of MAR so Character 4 in MBR is set into CR 1 in Instruction cycles and checked by CR 1 Code Check circuits of FIG. 72.

The CR 1 Code Check circuits of FIG. 72 provide code checking for serial (single character) processing. If any character is redundant, that is, has an odd number of bits, the CR 1 Code Check Odd lines **72.03** through **72.05** are positive to indicate an error. MBR Code Checking is not desirable during single character operation because unused Memory characters may be included in a five character group, and if any of the unused characters are redundant, needless error steps would occur. Accordingly, it is only when five characters from MBR are used simultaneously during Instruction cycles and Transmit by S cycles that MBR Code Checking is effective because sampling is only employed in these two instances.

The Input Switch, FIG. 10, gates characters to Memory for writing five characters into those Memory positions which have been read from previously. Six characters are available to the Input Switch, five characters held in the Memory Buffer Register and one character held in the Result Register, and five of the six characters are selected from among the Memory Buffer Register and the Result Register. Either all five characters held in the Memory Buffer Register can be written into Memory or four characters held in the Memory Buffer Register and the one character in the Result Register can be written into Memory with the Result character replacing any one Memory Buffer Register character depending upon the Input Select Gating circuits.

With reference to FIG. 10, the Input Select provides gating lines **10.01** through **10.10** to the Input Switch of FIGS. 11*a* and *b*. The Result to Memory line **137.01** and all five Select Character lines **20*a*.03**, **20*a*.02**, **20*a*.01**, **20*a*.08** and **20*a*.10** are used to control the Input Switch. The Result to Memory line, if down, causes five characters held in the Memory Buffer Register to be written into Memory exactly as they were before reading. However, if Result to Memory line is up, the Result character is written into Memory replacing one of the five characters contained in the Memory Buffer Register according to the Select Character line conditioned in FIG. 10 during that cycle. As an example, if the units position of the Address is 2, Select character 2 is up. Then, Memory Buffer Register characters 0, 1, 3 and 4 are written into the same cores in which they were read, and the Result character from the Result Register is written into the cores from which Character 2 of the Memory Buffer Register was read. The Memory Buffer Register is set at $R_{3.5}$ and the Result Register is set at R_4. Thus, characters in both are available for writing during the Write portion of the cycle.

The Off sides of the triggers of the Memory Buffer Register, FIGS. 14*a* and *b*, are coupled to the Memory Inhibit Driver Circuits of FIGS. 12*a* and *b* via the Input Switch of FIGS. 11*a* and *b*. Also, the On sides of the triggers of the Result Register, FIGS. 89*a* and *b*, are inverted and coupled to the Memory Inhibit Driver Circuits

of FIGS. 12*a* and *b* via the Input Switch of FIGS. 11*a* and *b*. (Inverting the On side signal of a trigger is equivalent to taking the signal from the Off side.) Thus, any of the lines which feed the Memory Inhibit Driver Circuits of FIGS. 12*a* and *b* that represent "zeros" have positive signals. In FIGS. 12*a* and *b*, the lines from the Input Switch mix with the Inhibit Gate on lines **5***g*.**01** and **5***g*.**02**, and when the Inhibit Gate rises, inhibit current flows into all of those Core Planes where "zeros" are to be written and, therefore, the writing of "ones" is blocked in those planes where write current is provided as hereafter described. The Write Gate rises shortly after the Inhibit Gate and mixes with the 4×8 Decoder outputs, FIG. 3*b*, and the 6×8 Decoder outputs, FIG. 3*d*, in the Switch Core Write Driver circuits of FIGS. 5*b*, *c* and 7*b*, *c*, respectively. This causes one row in each of the X and Y Switch Core Matrices to be pulsed with Write currents resetting one Switch Core in each matrix. By resetting the Switch Core, half Write current is provided on the same X and Y lines which were pulsed for reading causing "ones" to be placed in all Planes in which Inhibit current is not flowing.

Because the ferrite core's hysteresis loop is not precisely rectangular, each half selected core induces a small noise voltage in the Sense Winding having the same polarity whether the core is storing a "one" or a "zero." Therefore, a Half Selected Noise output for any core has the same polarity as the Read output for the core. The Sense Windings are so wound that the Half Selected outputs tend to cancel each other, but the noise voltage may be harmful to the desired signal. Therefore, after writing into the ferrite cores is accomplished, the cores are Post Write Disturbed. Post Write Disturbing is accomplished by resetting the Memory Buffer Register and the Result Register before the Inhibit Gate falls. Resetting these registers brings up all lines on the Off side outputs causing conduction in all 35 Inhibit Drivers. In addition, resetting the Memory Buffer Register and Result Register also prepares them for use on the following cycle.

MEMORY ADDRESS REGISTER

MAR contains the address portion of the Instruction being executed. On a Read (RD), Write (WR), Write Erase (WRE) and serial Transmit (TMT) instruction, this is the address of the high order or left-hand character of the field addressed. On the high-speed Transmit (TMT) instruction, the address is the fifth character from the high order or left-hand character addressed. On all other instructions, the address is the low order or right-hand character of the field addressed.

During Instruction time the Memory Address Register receives an address in parallel from Core Memory by way of character positions 1 through 4 of the Memory Buffer Register and retains the address during Execution. If the operation is a Transfer operation, the contents of the Memory Address Register are transferred to the Instruction Counter during Execute time so that the next Instruction will be obtained from the designated address. However, if the operation is not a Transfer operation the Memory Address Register holds the address of the data in Memory which is to be processed according to particular operation codes in Character 0 of the Instruction. The contents of the Memory Address Register may be transferred to the Memory Address Counters 1 or 2. The outputs of MAR can be sent to MAC 1, FIG. 2*gg* (FIGS. 30*a* through *e*), to MAC 2, FIG. 2*hh* (FIGS. 31*a* through *e*), to IC, FIG. 2*ii* (FIGS. 32*a* through *e*), or the Select Register, FIG. 2*jj* (FIGS. 33*a* through *d*).

Since addressing counters and registers use "zero" characters in the true binary form of no "one" bits, a "zero" from MBR represented by an 8 and 2 bit must be converted to an absence of bits. A "zero" from MBR is recognized in the form of 8 and 2 bits and causes the setting lines of its corresponding position in MAR to be blocked. For example, 8 and 2 bits from Character 4 of MBR are combined to hold down Block Set 1st order MAR line **17***f*.**07** thereby preventing setting the 8, 4 and 2 bit triggers in the first order of MAR, FIG. 17*a*.

Referring to FIG. 17*a*, a sample order of the Memory Address Register is shown comprising four triggers which are reset Off, that is, with the right side conducting, during each Instruction cycle at R_0 (D2) time (FIG. 139*a*). The digit portion of Character 4 from the Memory Buffer Register, FIG. 14*a*, is read into the units position of the Memory Address Register via the Memory Out, FIGS. 21*a* through *d*. Binary "ones" in the 1, 2, 4 and 8 positions cause lines **20***d*.**04**, **20***d*.**05**, **20***d*.**06** and **20***d*.**07** to be positive and condition Diode Gates G_j as shown in FIG. 17*a*. Then a positive signal occurs at A_1 (D0.4) time on the line **101.19** and a positive signal appears on Diode Gate output lines of the Diode Gates that are conditioned which are effective to turn On their respective triggers. Accordingly, for each binary "one" bit, a corresponding trigger in the units order of the Memory Address Register is turned On. As explained above, whenever a 0 Character is represented, i.e., a binary "one" in the 2 and 8 bit positions only, circuits are effective to block the setting of the particular order of the Memory Address Register. The negative signal on the Block Set Memory Address Register line **17***f*.**07** blocks passage of any signals through the Diode Gates which it conditions and consequently all of the triggers in that position remain Off to represent holding of binary "zeros."

MEMORY ADDRESS SELECTOR KEYS

It is also possible to manually set information into the Memory Address Register by means of the Memory Address Select Keys of FIG. 25*a* which cause positive and negative signals representing binary "ones" and binary "zeros" respectively on the MAS–8 line **25***b*.**16**, MAS–4 line **25***b*.**17**, MAS–2 line **25***b*.**18** and MAS–1 line **25***b*.**19** to condition one input of the Diode Gates and when these Diode Gates are so conditioned, a signal on the line Set MAR to MAS line **17***f*.**01** is effective to set binary "ones" into the triggers according to the keys selected.

MEMORY ADDRESS COUNTER 1 (MAC 1)

MAC 1, FIGS. 30*a* through 30*e*, is a nineteen-trigger counter that represents a five digit binary coded decimal address in the range of 00000 to 39,999 for a 40K Memory (00000 through 79,999 for an 80K Memory) which is received from the Instruction Counter or Memory Address Register. An initial address is set into MAC 1 from the Memory Address Register in each Instruction cycle, and MAC 1 is also set to MAR during some Execute cycles in the Multiply, Divide, and Add to Memory instructions. During each Execute cycle of certain parts of instructions such as Add, Subtract, Multiply, Compare and so forth, MAC 1 is stepped to contain the address of data in Core Memory that is to be processed in the next cycle. During certain parts of other instructions such as Shorten, Lengthen, and so forth, MAC 1 is not needed to refer to Memory information and is used to determine the number of cycles required for the operation. MAC 1 can be stepped by three values: plus one (+1) by the line **93***g*.**01**, minus one (−1) by the line **93***g*.**07**, and plus 5 (+5) by the line **93***h*.**02**. Both the stepping pulse gated by the foregoing lines and the setting pulse, lines **30***f*.**07** through **30***f*.**11**, are blocked pulses.

On Execute cycles for Write, Write Erase, and Serial Transmit instructions, the stepping of MAC 1 is gated by an I/O Request and by NOT Transition. MAC 1 is also stepped plus one for all Read instructions when a Read Request is made from an I/O device. During a high speed Transmit operation, MAC 1 and MAC 2 are stepped plus five on alternate cycles. The Instructions set forth above are the only ones where addressing is from high order to low order of a field, and for all other instructions (except where no stepping at all is required) MAC 1 is stepped minus one. Instructions which do not require MAC 1 to be stepped include No Operation, Transfer

Any, Halt, Transfer High, Transfer Equal, Transfer Plus, Transfer Zero, Transfer Signal, Read While Writing, Sign, Receive, Normalize Transfer, Transfer, Select and Control.

If an automatic check stop occurs, MAC 1 is not set or stepped but displays on the operator's console the address where the check stop occurred. At R_0, the contents of MAC 1 are automatically set into MASR, FIGS. 49*a* through *j*, if MASR is not set to the contents of either the IC, MAC 2, or SMAC (see FIG. 93*s*). During the Execution of Multiply, Divide and Add to Memory, some steps in the operations let Memory information be used more than once. In all instances, the Memory Address Register is not altered during the execution of an instruction, so when necessary the Set MAC 1 to MAR signal can be used during the operation to set MAC 1 to MAR and use the information over again.

By stepping MAC 1 down one each cycle at R_3 time, MAC 1 reaches 00000 then 39,999 (for 40K Memory) when the outputs are decoded to recognize MAC 1=0. This indication may be used to complete or alter the operation. Also, when MAC 1 reaches the address 39,999 (for 40K Memory), an End of Memory indication is given. During a Write 01 instruction, this indication causes completion of the operation.

FIGS. 30*a* through 30*e* are diagrams of the orders of the Memory Address Counter 1. For the purpose of explanation, the units order of FIG. 30*a* is described although it will be understood that all of the orders will, as required, receive the contents of the Memory Address Register. The contents of the Memory Address Register are represented by signals on the MAR–$\overline{8}$ line **17***a*.**01**, MAR–$\overline{4}$ line **17***a*.**08**, MAR–$\overline{2}$ line **17***a*.**17** and MAR–$\overline{1}$ line **17***a*.**25**, which lines are positive if the respective bits of the Memory Address Register contain binary "zeros," and also on the MAR–8 line **17***a*.**05**, MAR–4 line **17***a*.**14**, MAR–2 line **17***a*.**21** and MAR–1 line **17***a*.**29**, which lines are positive if the respective bits of the corresponding order of the Memory Address Register contain binary "ones." These output lines from the Memory Address Register feed the Diode Gates as shown in the drawings. Thus, as the trailing edge of the signal on the Set MAC 1 to MAR line **30***f*.**07** goes negative, a signal is gated through the proper Diode Gate to cause the required binary "ones" or "zeros" to be set into the triggers. For example, if the 1 bit of MAR contains a binary "one," the signal on the Set MAC 1 to MAR would pass the Diode Gate connected to the MAR–1 line **17***a*.**29** to turn On the trigger thereby entering a binary "one" in the one-bit position of the Memory Address Counter 1. However, if the one-bit position of MAR had contained a binary "zero," the MAR–$\overline{1}$ line would be positive and the signal on the line Set MAC 1 to MAR would pass the other Diode Gate to turn Off the trigger, thereby entering a binary "zero" in the Memory Address Counter one-bit position. Thus, it is evident that there is no need for providing a reset for the Memory Address Counter before entering the contents of MAR therein, as setting is accomplished by the trailing edge of the Set MAC 1 to MAR signal combined with a signal on one or the other of two input lines per trigger which is effective to set each trigger to either "one" or "zero" regardless of the previous states. When the Step MAC 1+1 or +5 line **30***f*.**01** is positive, the Diode Gates (DG) are conditioned for a negative A_2/R_3–W_1 pulse on the line **30***f*.**06** to the binary input of the 1 trigger which is effective to step the counter one count by changing the condition of the latter trigger. When the 1 trigger goes from an Off to an On condition, it has no effect on the succeeding 2 trigger. However, as the 1 trigger is shifted from an On to an Off condition, its output (by way of the cathode follower on the line MAC 1–1) passes via a conditioned gate to the binary input of the 2 trigger and thereby shifts the condition of the latter trigger. The Diode Gate having an input from MAC 1–$\overline{8}$ must be conditioned by a positive signal on the line **30***f*.**01**, a signal on the line MAC 1–1, and also by a positive signal on the line MAC 1–$\overline{8}$ signifying that the 8 trigger representing the 8 bit contains a binary "zero." A signal MAC 1–8 on the line **30***a*.**04** feeds to the succeeding higher order of the Memory Address Counter via a Diode Gate conditioned by Step MAC 1+1 or +5 line **30***f*.**02** to enter a 1 (carry) into the lower order position of the second order of MAC 1.

The Memory Address Counter must also be capable of counting +5 which is accomplished by changing the contents of the 4 and the 1 trigger by way of the Step MAC 1+5 line **93***h*.**02** combined with the A_2/R_3–W_2 line **30***f*.**06** which sets the 4 trigger to the opposite state, and by the Step MAC 1+1 or +5 line **30***f*.**01** and the **30***f*.**06** line which sets the 1 trigger to the opposite state. The units order of MAC 1 must sit at 4 or 9 when MAC 1 is stepped +5.

The Memory Address Counter must also be capable of counting down as mentioned previously. This is effected by a positive signal Step MAC 1–1 on the line **93***g*.**05** which conditions Diode Gates which are effective to couple the left plate output of each trigger to the binary input of the succeeding higher trigger. Thus, when any trigger goes from an Off to an On condition, the succeeding higher trigger is shifted from one condition of stability to another. As any trigger shifts from an On to an Off condition, the output signal to a Diode Gate is positive and therefore has no effect on the succeeding trigger. It should be noted however, that when the 8 trigger shifts from an Off to an On condition, a carry signal is emitted on the line **30***a*.**01**. This carry signal besides feeding the succeeding higher order, also operates via 33 micromicrofarad condensers and a diode to shift the 4 and 2 triggers Off. Briefly, the Step MAC 1–1 line **93***g*.**05** conditions Diode Gates associated with the Off sides of the triggers and connected to lines MAC 1–$\overline{1}$, MAC 1–$\overline{2}$ and so forth, the signals on the respective lines being positive when the corresponding triggers contain binary "zeros." MAC 1 controls are shown in FIG. 30*f* and their operation will be easily understood when a typical operation of the computer is described.

MEMORY ADDRESS COUNTER 2 (MAC 2)

MAC 2, FIGS. 31*a* through 31*e*, is a nineteen trigger counter having the purpose of determining one address used during instructions requiring two addresses, where MAC 2 indicates the address of the information being entered into Memory. This address is set into MAC 2 from the Memory Address Register at W_1 time of the Execute cycle of the Receive (RCV) or Read-While-Writing (RWW) instruction on the fall of the lines **31***f*.**02**, **31***f*.**03**, **31***f*.**04**, **31***f*.**05** and **31***f*.**06**. The setting of MAC 2 is preceded by reset at R_0 time on lines **139***c*.**03** through **139***c*.**07** which is generated by the Reset MAC 2 and Set to MAR lines **131**.**04** and **69**.**06** in combination with R_0 (D2) Use line **102**.**12** (FIG. 139*a*.). MAC 2 can be stepped +1 via the line **31***f*.**07** or +5 via the lines **93***h*.**04** and **31***f*.**07** during Execute cycles so that the next character to be operated upon may be located. The outputs of MAC 2 are provided to the Memory Address Select Register, FIGS. 49*a* through *j*, and the contents of MAC 2 are set into MASR by way of the set MASR to MAC 2 line **93***s*.**02**.

INSTRUCTION COUNTER

The Instruction Counter, FIGS. 32*a* through *e*, is stepped five for each Instruction cycle so as to contain the address of the next instruction. In normal operations, Instructions are referred to sequentially, five addresses removed from each other since each Instruction requires five characters. During a Transfer instruction,

the Instruction Counter is set to a designated address obtained from the Memory Address Register.

The Instruction Counter is reset to 0004 for Initial Reset, Machine Reset and Clear Memory operations before the Instruction Counter is set to the contents of the Memory Address Register. The Instruction Counter is a sixteen trigger counter (for 80K Memory), and the units position of the Instruction Counter, FIG. 32*a*, has only one trigger which is Off for a 4 and On for a 9. The Off side of the 4 trigger line **17***a*.**09** in the first order of MAR, FIG. 17*a*, controls the setting of the Instruction Counter units position trigger of FIG. 32*a*. If the $\overline{4}$ line **17***a*.**09** is plus, the units position of the Instruction Counter trigger is turned On to represent a 9. This is so because an Instruction must be located at an address with a 4 or a 9 in the units position, as previously described, in order to bring out five characters of an Instruction. The Instruction Counter can receive an address from the Memory Address Register or be stepped +5 at R_3 of every ECC 1 cycle (except for Transfer operations) by changing the state of the first order trigger with the fall of a stepping $-A_2/R_3-W_1$ pulse of the blocked type.

The Instruction address in the IC is sent to the Memory Address Select Register at R_0 time of each Instruction cycle to obtain the five Instruction characters. When the Instruction Counter is stepped +5 after being set to the original address, 00004, the trigger is turned Off causing the fall of the right plate to send the carry to the first position of the tens order of IC. An auto check stop caused by an Instruction Check Error condition blocks the $-A_2/R_3-W_1$ stepping pulse so that the Instruction Counter remains at the address of the Instruction Error.

More specifically, the IC triggers are reset to 00004 and then the contents of Memory Address Register are emitted via output lines from MAR. Those particular bits holding binary "ones" condition the Diode Gates, the signals on the Set IC to MAR lines **32***a*.**06**, **32***a*.**07**, **32***a*.**08** and **32***a*.**09** are applied and the trailing edge is effective via conditioned Diode Gates (DG) to turn On their respective triggers. In this manner, the contents of Memory Address Register are transferred into the Instruction Counter.

During the first Execute cycle after the Instruction cycle, ECC 1 line **123.34** in FIG. 32*a* is positive and is combined with NOT Manual 3 line **116.09**, Minus on Block Step IC line **93***j*.**12** and A_2/R_3-W_1 (blocked) line **103***a*.**20** to provide a positive output from the AND circuit. The fall of the output of Inverter (IK) switches the trigger to the alternate state at R_3 time. The connections between the stages of the counter are such that when one trigger is turned Off it is effective to shift the condition of the succeeding higher trigger, for example, IC–9 line **32***a*.**04** to IC–10 trigger of FIG. 32*b*. Assume that the 80 trigger and 10 trigger of the second order of IC, FIG. 32*b*, are On and the IC–80 and IC–10 lines are up to indicate a count of 90 when the IC–9 line **32***a*.**04** goes negative. The latter line turns Off the 10 trigger whose IC–10 line drops and turns Off the 80 trigger. The fall of the IC–80 line **32***b*.**02** provides a carry to the third order of IC, FIG. 32*c*. The second order of IC now stands at 0. The outputs of the 10, 20, 40 and 80 triggers pass through the cathode followers to line IC–10, IC–20, IC–40 and IC–80, respectively, which lines are negative when respective triggers are Off, signifying holding of a binary "zero." The hundreds, thousands and ten thousands orders of the Instruction Counter operate similarly, receiving inputs from the corresponding orders in the Memory Address Register and further receiving inputs on lines which are carry signals from the succeeding lower stages.

MEMORY ADDRESS SELECT REGISTER (MASR)

MASR, FIGS. 49*a* through 49*j*, is an eighteen trigger register (for 80K Memory) for the purpose of driving the selection circuits of Core Memory. It may be set to either MAC 1, MAC 2, IC, or SMAC at R_0 time, and retains the address of the information being operated on in Core Memory for a complete character cycle from R_0 to R_0. It is pointed out that MAC 1, MAC 2, the Instruction Counter or the Memory Address Register may change status during a machine cycle without effecting the five characters being selected in Memory since MASR is unchanged. The outputs of the Memory Address Select Register, FIGS. 2*ww* through 2*yy*, are sent to the X and Y Switching circuits, FIG. 2*a*, to select five characters from Core Memory as described previously. Outputs in the first order triggers of the Memory Address Selection Register, FIG. 2*ww* (FIGS. 49*a* and *b*) are also sent to the Memory 4×5 Decoder, otherwise known as the Character Select Switch, FIG. 3*e*, to determine which of the five characters is to be sent to CR 1, FIG. 2*h*, by way of Memory Out, FIG. 2*g* (FIGS. 20*a* through *d*).

Referring now to FIG. 49*a*, the first order of the Memory Address Select Register is shown and its description will serve as a description of the other orders. The Diode Gates (G_j) serve to change the state of the trigger with a positive shift when conditioned by positive signals on lines representing binary "ones" or the complements thereof. The set circuits for the first order of the Memory Address Select Register are shown in FIG. 49*b* as having inputs from Memory Address Counter 1, Memory Address Counter 2, the Instruction Counter, and the SMAC, line **17***a*.**24**). The set circuits are selection circuits for selecting the contents of MAC 1, MAC 2, the Instruction Counter, or the SMAC, in response to signals on the Set MASR to MAC 1 line **93***s*.**02**, Set MASR to MAC 2 line **93***s*.**03**, Set MASR to IC line **93***s*.**01** and Set MASR to SMAC line **93***s*.**04**, which condition the AND circuits for the passage of binary "one" values to the outputs of the cathode followers. Positive outputs are provided on the 8 line **49***b*.**02**, the 4 line **49***b*.**04**, the 2 line **49***b*.**06**, the 1 line **49***b*.**08**, whenever the binary value of "one" is represented. When the last mentioned lines are down indicating binary "zeroes," Inverters attached to each line provide positive outputs on the $\overline{8}$ line **49***b*.**01**, $\overline{4}$ line **49***b*.**03**, $\overline{2}$ line **49***b*.**05** and $\overline{1}$ line **49***b*.**07**. Each of the pairs of lines are connected to input lines of the first order of MASR, FIG. 49*a*, where the lines representing binary "one" values are connected via Diode Gates to the On side of the triggers and the complement lines representing binary "zeros" having positive signals are connected via Diode Gates to the Off side of the triggers. With these connections it will be noted that it is unnecessary to reset the MASR since pairs of lines are effective to set the triggers to the required values regardless of their previous state. The R_0 (D0.4) line **101.01** conditions the Diode Gates for the passage of positive signals on the input lines from the first order of MASR set circuits, FIG. 49*b*. The other four orders of MASR and their associated MASR set circuits are provided in the remaining FIGS. 49*c* through *j* and they operate in a manner similar to the first order of MASR.

STORAGE SELECT REGISTER

The Storage Select Register (SSR), FIG. 16*a*, consists of four triggers that select a particular Storage unit by way of the Storage Address Counter, FIGS. 52*a* through *d*, and SSR Decoding, FIG. 54, or that identify a special type of Instruction by way of SSR Decoders, FIGS. 55*a* and *b*. The SSR is Instruction reset by means of a line **139***b*.**01** from Instruction Reset Controls of FIG. 139*b*, and then the Zone Bit configurations of characters 2 and 3 of the Memory Buffer Register are set into the SSR. The Memory Buffer Register character 2–B line **14***a*.**02**, Memory Buffer Register character 2–A line **14***a*.**02**, MBR character 3–B line **14***a*.**02** and MBR character 3–A line **14***a*.**02** condition Diode Gates (G_j), and at A_0 of I time, a positive signal on the line **101.24** causes those outputs of the Diode Gates to go positive which are conditioned by signals of the Memory Buffer Register indicating binary "ones" to

set the corresponding triggers On. During manual operations, the Storage Select Register is reset during Manual 1 time by a manual timer via line **116.02** which causes Instruction reset, FIG. 139*a*. Keyed outputs indicative of binary "ones" are present on the SS–8 lines **16*b*.01**, SS–4 line **16*b*.02**, SS–2 line **16*b*.03** and SS–1 line **16*b*.04** where binary "ones" are desired. These lines feed diode gates (D_G) and upon the fall of the Set SSR to SS line **17*f*.06**, the negative shift at the outputs of diode gates (D_G) sets to the On state those triggers where binary "zeros" are desired. Lines **16*a*.01**, **16*a*.04**, **16*a*.07**, **16*a*.11**, **16*a*.14**, **16*a*.18**, **16*a*.21** and **16*a*.25** go to Storage Select Register Decoder stages 1 through 8 of FIG. 55*a* and lines **16*a*.05**, **16*a*.08**, **16*a*.12**, **16*a*.15**, **16*a*.19**, **16*a*.22** and **16*a*.26** go to Storage Select Register Decoder stages 9 through 15 of FIG. 55*b* to modify certain instructions. The lines **16*a*.03**, **16*a*.16**, **16*a*.17** and **16*a*.24** go to Storage Select Register Decoding of FIG. 54, for distinguishing Storage Addresses in the Accumulator from Storage Addresses in Auxiliary Storage. The lines **16*a*.02**, **16*a*.06**, **16*a*.09**, **16*a*.13**, **16*a*.16**, **16*a*.20**, **16*a*.23** and **16*a*.27** go to stages 5 through 8 of the Storage Address Counter, FIG. 52*d*, for setting stages 5 through 8 of SAC in FIG. 52*c* to the SSR bits 1, 2, 4 and 8, respectively. Since there are no bits in the zone portions of characters 2 and 3 of the Instruction when the Accumulator is used, SSR is then 0 making SASR 256 line **54.24** positive and SSR=0000 lines positive in FIG. 54. SASR 256 line **54.24** goes to FIG. 34*a* to select the Accumulator portion of Storage and in combination with the Storage Address Counter address, which is set in the Storage Address Select Register, locates a particular character. The SSR=0000 lines allow SAC to be set to the Starting Point Counter, conditions the Accumulator DZT and Accumulator Sign trigger, identifies Instructions which have no bits in the zone portion of the second and third characters. When an Auxiliary Storage unit is used, one or more of the SSR triggers would be On bringing up SASR $\overline{256}$ line **54.01** and the SSR≠0000 lines, FIG. 54. SASR $\overline{256}$ line **54.01** selects the Auxiliary portion of Storage. The SSR≠0000 lines allow the four high order positions of the Storage Address Counter to be set by Storage Select Register and resets the four low order positions of SAC. When the Storage Address Select Register is set to SAC combined with SASR $\overline{256}$, the units position of the proper Auxiliary Storage unit is selected. The SSR≠0000 lines of FIG. 54 also condition the Auxiliary Storage DZT and Auxiliary Sign trigger and identify Instructions with zone bits in the second and third order positions of the Instruction.

STARTING POINT COUNTER (SPC)

The Starting Point Counter of FIGS. 51*a*, *b* and *c*, is an eight stage binary counter of capacity 256 which keeps track of the starting or reference point of a field in the Accumulator. The Starting Point Counter has no reset to 0 and no means to be set to any particular address. When the machine is turned On, SPC may contain any number 0 through 255, depending upon the way in which the individual triggers establish their stable states. The SPC can be stepped up or down one unit completely around to and beyond its original starting point and can be stepped 128 positions, also. The Starting Point Counter determines the location of the units position of the field in the Accumulator, the other limit being determined by the Storage Mark. As in the case of MAC 1, if an Auto Check Stop occurs, the stepping pulses to the Starting Point Counter are blocked to prevent altering the contents of SPC from the error position.

Referring to stages 1 through 3 of the Starting Point Counter in FIG. 51*a*, the SPC may be stepped up one count by means of the line **93*j*.01** and down one count by the Step SPC–1 line **93*j*.03** which conditions diode gates sampled at A_2 time by the $-A_2/R_3-W_1$ line **52*e*.02**. If the Starting Point Counter is to be stepped up, a signal on the Step SPC+1 line **93*j*.01** goes positive to condition the upper diode gate in each position. With the line **93*j*.01** positive, a negative signal is provided on the line **52*e*.02** which is passed to the binary input of the 1 trigger causing the latter to shift from one condition of stability to another. As the 1 trigger shifts from an On to an Off condition, a negative signal is emitted from its right plate and is fed via the cathode follower and a conditioned diode gate to a binary input of the next adjacent trigger, the 2 trigger, thereby causing the latter to shift from one condition to another. Likewise, succeeding bit triggers of the counter receive inputs from the adjacent lower order. Positive going outputs from the triggers have no effect on succeeding stages.

To step the SPC down on count, the Step SPC–1 line **93*j*.03** is positive to condition the lower diode gates in each stage, and the negative signal on the line **52*e*.02** is then passed via the diode gate to the binary input of the 1 trigger. However, in this instance, only when this trigger shifts from an Off to an On condition is a negative signal emitted and passed via the conditioned diode gate to provide a binary input to the next adjacent trigger, the 2 trigger. The same type of circuits and explanation applies to succeeding higher stages.

On occasion it is desired to step the Starting Point Counter by a count of 128. This is accomplished at W_1 time by conditioning a diode gate with a signal Step SPC+128 on the line **93*j*.07** and sampling with an A_2/R_3-W_1 signal on the line **52*e*.08** to the eighth order of the SPC. The output of this gate is applied to the trigger so that a negative input is effective to cause a shifting of its condition.

STORAGE ADDRESS COUNTER

The Storage Address Counter (SAC), shown in FIGS. 52*a* through 52*d*, is an eight stage binary trigger counter that designates the address of the Storage character to be processed the next cycle. In FIGS. 52*b* and 52*d*, the contents of the Starting Point Counter can be set into SAC via the lines **52*a*.01** through **52*a*.08** in combination with the Set SAC to SPC line **52*e*.04** and the lines **51*b*.03** through **51*b*.06** and **51*c*.01** through **51*c*.04** in combination with the Set SAC to SPC line **52*e*.05**. Output lines **52*b*.01** through **52*b*.08** and **52*d*.01** through **52*d*.08** are connected as inputs to the SAC triggers of FIGS. 52*a* and 52*c* respectively. When the Storage Select Register equals zero, indicating that Accumulator Storage is being used, all eight stages of SAC are set to the contents of SPC. When the Storage Select Register is not equal to zero, indicating that an Auxiliary Storage unit is being used, however, the Set SAC to SSR lines **52*e*.06** and **52*e*.07** are positive to cause the four high order positions of SAC to be set to the bit pattern of the SSR and to cause the four low order positions, stages 1 through 4, of SAC to be reset to "zero."

In FIGS. 52*a* and *c*, SAC can be stepped plus one by a positive signal on the lines **93*i*.03** and **93*i*.04** in combination with the fall of the $-A_2/R_3-W_1$ Blocked pulse on the line **52*e*.03**, the latter being connected to the units order diode gate. In FIG. 52*a*, the line **93*i*.03** conditions a diode gate (in the upper row of diode gates) for each trigger, and, similarly, in FIG. 52*c* the line **93*i*.04** conditions a diode gate for each trigger of the higher orders. The output of each diode gate is connected to the binary input of each trigger, and the right plate output of each trigger is applied as an input to the diode gate of each higher order trigger. Keeping in mind that it is the fall of the pulse supplied to a conditioned diode gate that provides an output, it will be evident that it is only the change from "one" to "zero" of a trigger that can be supplied to the binary input of the next higher order trigger when the Step SAC+1 line is positive. For example, assume that SAC is zero (all triggers Off) and that the diode gates are conditioned by a positive pulse on the lines **93*i*.03** and **93*i*.04**. When the $-A_2/R_3-W_1$ pulse falls the 1 trigger is turned On. The right-hand plate of the 1 trigger goes positive but the rise is ineffective to provide

an output from the upper diode gate feeding the binary input to the 2 trigger. The count is now 1 as indicated by the 1 trigger being On and all others Off. When the Step SAC+1 lines **93***i*.**03** and **93***i*.**04** are positive during the next cycle and the line **52***e*.**03** falls, the 1 trigger is turned Off and the fall of the right-hand plate of the 1 trigger is passed to the binary input of the 2 trigger via the diode gate to turn On the 2 trigger. The count is now 2 as indicated by only the 2 trigger being On. On the third cycle, the 1 trigger is turned On and its right-hand plate rises which is ineffective to turn Off the 2 trigger. The 4 trigger and other higher orders cannot be turned On since the right plate of the 4 trigger remains positive and the other higher orders are still Off. The count is now 3 as indicated by the 1 and 2 triggers being On and the remaining triggers being Off. In the fourth cycle, the fall of the Blocked pulse on the line **52***e*.**03** turns Off the 1 trigger and the fall of its right plate turns Off the 3 trigger. The fall of the right plate of the 3 trigger turns On the 4 trigger. Thus, the count is now 4 as indicated by the 4 trigger being On and all other triggers being Off. Counting up continues in the manner described. Although the example of operation was given starting from a count of zero, it will be understood that SAC may be set to any value as previously described and then stepped up by one as required.

SAC can also be stepped minus one by the Step SAC–1 lines **93***i*.**01** and **93***i*.**02** and the $-A_2/R_3-W_1$ Blocked line. The Step SAC–1 lines condition the lower rows of diode gates in FIGS. 52*a* and *c* and the Blocked pulse is applied only to the 1 trigger diode gate. The left plates of all triggers, except the one of the highest order, are connected as inputs to the lower row of diode gates. As an example of operation, assume that SAC contains a count of 4, that is, the only trigger On is the 4 trigger. With the Step SAC–1 line positive, the fall of the Blocked pulse on line **52***e*.**03** turns On the 1 trigger, the fall of the left plate of the 1 trigger turns On the 2 trigger, and the fall of the left plate of the 2 trigger turns Off the 4 trigger. Since the left plate of the 4 trigger rises, the 8 trigger is not turned On and the remaining higher order triggers are not affected. Of course, any value may be set into SAC and then decreased in steps by one as desired.

SAC can also be stepped plus 128 by the Step SAC+128 line **93***i*.**05** and the A_2/R_3-W_1 (Blocked) line **52***e*.**09**. This is accomplished by changing the state of the 128 trigger of FIG. 52*e*. A positive voltage on the Step SAC+128 line conditions a diode gate for the fall of the pulse on line **52***e*.**09** which provides a negative signal to the binary input of the 128 trigger thereby reversing its condition of stability to the opposite sense.

As mentioned previously, the eight triggers of SAC count **256** addresses, and if all triggers are On indicating address **255**, stepping the counter plus one turns all triggers Off to register address zero.

The output lines **52***c*.**02** through **52***c*.**09** and **52***a*.**01** through **52***a*.**08** are used to set Storage Address Select Register, FIGS. 53*a* and *b*, at R_0 time of every cycle. Therefore, the address can be altered during each cycle in preparation for the next cycle while the Storage Address Select Register holds the location of the character being processed. The output lines **52***a*.**11**, **52***a*.**12**, **52***a*.**13** and **52***a*.**14** from FIG. 52*a* and the line **52***c*.**01** from FIG. 52*c* are used in the SAC controls of FIG. 52*e* to recognize critical addresses by bringing up the output line **52***e*.**01**. The output lines **52***a*.**09** and **52***a*.**10** from FIG. 52*a* to FIG. 52*c* are those lines previously described as being used to propagate carries while stepping SAC plus one or minus one.

The SAC controls are illustrated in the lower portion of FIG. 52*e* where the minus A_2/R_3-W_1 pulse is generated, the Set SAC to SPC pulse is derived from A_2/R_3-W_1 line **103***a*.**16**, E time line **123.23**, Set SAC to SPC line **93***j*.**08** and SSR=0000 line **54.10**. The Set SAC to SSR pulse is derived by combination of the Set SAC to SPC line **93***j*.**08**, A_2/R_3-W_1 Use line **103.06**, I time line **124.33** and Storage Select Register ≠0000 line **54.02**. It is particularly pointed out that the Set SAC to SPC lines **52***e*.**04** and **52***e*.**05** are brought up during the Execute or Instruction cycle while the Set SAC to SSR line **52***e*.**06** is brought up during Instruction cycle.

STORAGE ADDRESS SELECT REGISTER

The Storage Address Select Register (SASR) of FIGS. 53*a* and *b* is an eight trigger register that contains the address of the character being processed in Storage. Its output lines **53***a*.**01** through **53***a*.**08** and **53***b*.**01** through **53***b*.**08** are decoded in the Decoders of FIGS. 34*a* through 34*d* to select the X and Y Switching circuits which locate the character to within a factor of two in Storage. SASR is set to the contents of the Storage Address Counter at R_0 time by pairs of output lines from each position of SAC which, when positive, condition plus diode gates gated by the R_0 (D0.4) lines **101.06** and **101.07** for every Execute cycle, except during certain Transition cycles associated with critical addresses. A Minus on Suppress SASR to SAC line **136***b*.**07** conditions the plus diode gates for the 32, 64 and 128 triggers of FIG. 53*b* for an Auto Transition cycle in the Read/Write mode as will be explained hereafter. The Storage Address Select Register retains the selected address from R_0 to R_0 time allowing SAC to obtain another address without affecting the chaacter addressed in Storage.

SUMMARY OF SETTING COUNTERS AND REGISTERS

At W_2 time of an End Execute cycle, the I/E trigger changes to I. The Memory Buffer Register resets at W_3 time preparing to receive five new characters. At R_0 of each Instruction cycle the Memory Address Select Register is set to the Instruction address in IC and drives the X and Y switching circuits of Memory. At the same time the Memory Address Register, Storage Select Register and Operation Register are reset to receive new information. The Read Memory operation begins at R_0. A Read Sample pulse conditions the Sense Amplifiers at approximately $R_{3.5}$ and sets the **35** triggers in the Memory Buffer Register to the bit configuration of the five characters. At A_0 time the Operation Register is set with character 0 from the Memory Buffer Register, the Storage Select Register $R_{3.5}$ and sets the 35 triggers in the Memory Buffer Regis- and Character Register 1 is set to Character 4 of the Memory Buffer Register. The Memory Address Register is set to certain bits of the Memory Buffer Register at A_1 of an Instruction cycle and the Instruction Counter is stepped at R_3 time of ECC 1 to prepare for the next Instruction. Writing the instruction characters back into Memory is initiated by the Write Gate at W_0. At W_1 time, MAC 1 is set to the Memory Address Register so that the address of the data field is available from MAC 1 during the next machine cycle.

The first Execute cycle, ECC 1, begins at W_2 when the I/E trigger changes from I to E and the ECC 1 trigger is turned On. At W_3 time, the MBR and SBR are reset to prepare for receiving new characters. At R_0, the MASR is set to MAC 1, MAC 2, IC or SMAC and the SASR is set to SAC. At R_3 of ECC 1, there is a conditional operation in which the IC is stepped plus five provided an instruction Check Stop or a Transfer operation is not indicated. If the Read Memory and Read Storage Routing lines are brought up in this cycle, the Read Sample pulse conditions the Sense Amplifiers and sets the triggers in the MBR and SBR accordingly at $R_{3.5}$. At W_0 time of ECC 1, one character is set into each Character Register, CR 1 and CR 2. At W_2, depending upon whether the SSR is equal to zero or not, SAC is set to either the SPC or the SSR. Also, at W_1, MAC 1 is set to MAR.

Summarizing Executive cycles generally, each cycle has cycle points R_0, R_1, R_2, R_3, R_4, W_0, W_1, W_2 and W_3, where R_0 to W_0 is Read time and W_0 to R_0 is Write time

as previously described. At R_0, MASR and SASR are set to their respective counters, and R_3 is stepping time for the counters. The Buffer Registers are set at about $R_{3.5}$ and R_4 is the setting time for the Result Register. W_0 is the setting time for the Character Registers and is the usual switching time for triggers associated with the ALU. W_1 is the switching time for the Add triggers which defines an arithmetic cycle. W_2 is switching time for the I/E trigger, Use trigger, ECC 1 trigger, Type Cycle triggers, Transition triggers and Mode Control triggers among others. W_3 is the switching time for the MAC 1 Equals Zero trigger and is reset time for the Result Register, Memory Buffer Register and Storage Buffer Register.

EXAMPLE OF CORE MEMORY OPERATION

Assume that the Memory Address of 19,955 is set in the triggers of the Memory Address Select Register of FIGS. 49*a* through 49*j*. Accordingly, the Memory Address Select Register $\overline{8}$ lines **49***a*.**01** and **49***a*.**02** are up, the Memory Address Select Register 4 lines **49***a*.**07** and **49***a*.**08** are up, the MASR $\overline{2}$ lines **49***a*.**10** and **49***a*.**11** are up, and MASR 1 lines **49***a*.**16** and **49***a*.**17** are up. In FIG. 49*c*, the MASR $\overline{80}$ line **49***c*.**01** is up, the line MASR 40 line **49***c*.**05** is up, the MASR $\overline{20}$ line **49***c*.**07** is up, and the MASR 10 line **49***c*.**11** is up. In FIG. 49*e*, MASR 800 line **49***e*.**02** is up, MASR $\overline{400}$ line **49***e*.**04** is up, MASR $\overline{200}$ line **49***e*.**07** is up, and MASR 100 line **49***e*.**11** is up. In FIG. 49*g*, the MASR 8000 line **49***g*.**02** is up, the MASR $\overline{4000}$ line **49***g*.**04** is up, the MASR $\overline{2000}$ line **49***g*.**06** is up, and the MASR 1000 line **49***g*.**10** is up. In FIG. 49*i*, the MASR 10,000 line **49***i*.**02** is up, the MASR $\overline{20,000}$ line **49***i*.**04** is up, and the MASR $\overline{40,000}$ lines **49***i*.**07** and **49***i*.**08** are up. In FIG. 3*b*, the Memory 4×10 Decoder, the lines **49***i*.**04**, **49***c*.**07** and **49***c*.**05** from the Memory Address Select Register, FIG. 49*c*, are combined in an AND circuit to provide an output on 40 (P) line **3***b*.**05**. The line **3***b*.**05** goes to the Y Switch Core Write Drivers of FIG. 5*a* where it provides an output on the 40 (P) lin **5***a*.**05** and brings down the $\overline{40}$ line **5***a*.**06** due to the inverter in the latter line. All of the NOT output lines are up except $\overline{40}$ line **5***a*.**06** since the input line **3***b*.**05** is the only one up. In FIGS. 5*b* and *c*, these lines $\overline{00}$, $\overline{20}$, $\overline{60}$, $\overline{80}$, $\overline{20,000}$, $\overline{20,020}$, $\overline{20,040}$, $\overline{20,060}$ and $\overline{20,080}$ are combined with Memory Read Bias Gates on lines **5***g*.**09** and **5***g*. **18** to provide outputs on the lines **5***b*.**01**, **5***b*.**02**, **5***b*.**03**, **5***b*.**04**, **5***b*.**05**, **5***c*.**01**, **5***c*.**02**, **5***c*.**03**, **5***c*.**04** and **5***c*.**05** and R_0 as shown in the Memory Timing Chart of FIG. 144. An output is not provided on the line **5***b*.**03** at this time since the 40 (P) line **5***a*.**05** is up, but the line **5***g*.**03** is down. The $\overline{40}$ line **5***a*.**06** is down so the pulse on line **5***g*.**09** does not bring up the line **5***b*.**03**. The lines just described go to the Y Switch Core Write windings of FIG. 8 where the lines enter from the bottom and drive each column of the Switch Cores except the column associated with the 40 line **5***b*.**03**.

In FIG. 3*d*, Memory 6×8 Decoder, the $\overline{8}$ line **49***a*.**01**, the $\overline{2}$ line **49***a*.**10**, the 4 line **49***a*.**07**, the 1 line **49***a*.**16**, the 10 line **49***c*.**11** and the 10,000 line **49***i*.**02** are up. The outputs of these lines are decoded to provide an output on the 10,015–10,019 line **3***d*.**15** which goes to the X Switch Core Write Drivers, FIG. 7*a*, bringing up the 10,015–10,019 (P) line **7***a*.**15** and bringing down the $\overline{10,015}$—$\overline{10,019}$ line **7***a*.**16**. Since none of the other inputs to the 6×8 Decoder are up the $\overline{0}$–$\overline{4}$ line **7***a*.**02**, the $\overline{5}$–$\overline{9}$ line **7***a*.**04**, the $\overline{10}$–$\overline{14}$ line **7***a*.**06**, the $\overline{15}$–$\overline{19}$ line **7***a*.**08**, the $\overline{10,000}$–$\overline{10,004}$ line **7***a*.**10**, the $\overline{10,005}$–$\overline{10,009}$ line **7***a*.**12** and the $\overline{10,010}$–$\overline{10,014}$ line **7***a*.**14** are up. These lines go to the X Switch Core Write Drivers of FIGS. 7*b* and *c* where they are combined with the Memory Read Bias Gate on lines **5***g*.**11** and **5***g*.**12** to provide outputs on the lines **7***b*.**01**. **7***b*.**02**, **7***b*.**03**, **7***b*.**04**, **7***c*.**01**, **7***c*.**02** and **7***c*.**03** at $R_{0.5}$ as shown in FIG. 144. The 10,015–10,019 line **7***c*.**04** is down since the $\overline{10,015}$–$\overline{10,019}$ line **7***a*.**16** and the Memory Write Gate line **5***g*.**06** are down. The output lines from Memory X Switch Core Write Drivers, FIGS. 7*b* and *c*, go to the X Switch Core Write winding of FIG. 9, entering the figure from the top and passing through the rows of switch cores, carrying reset current (except for the 10,015–10,019 line **7***c*.**04**).

The output lines of FIG. 49*g* go to Memory 4×10 Decoder, FIG. 3*a*, where the lines **49***g*.**04**, **49***g*.**06**, **49***g*.**02** and **49***g*.**10** are up. The only lines effective are the 8000 and 1000 lines **49***g*.**02** and **49***g*.**10**, respectively, which are combined to provide an output on the 9000 (P) line **3***a*.**19**. The line **3***a*.**19** goes to the Memory Y Switch Core Read Drivers of FIG. 4 and when the Memory Y Read Gate line **5***g*.**08** comes up at R_1 as shown in FIG. 144, an output is provided on the 9000 line **4.10**. The line **4.10** goes to Y Switch Core Matrix, FIG. 8, to drive the 9000 line through the upper row of switch cores, tending to set the switch cores of the top row. Reset current is flowing in all of the columns except the one associated with the 40 line **5***b*.**03** as explained previously. Accordingly, the top row of switch cores have set and reset current applied thereto except for the core at the intersection of the 9000 line **4.10** and the 40 line **5***b*.**03**. Accordingly, this Switch Core 9040 is set and an output is provided on the secondary coil 9040 which goes to the Core Array of FIG. 13 to provide half-select current on the line 9040.

In FIG. 3*c*, Memory 4×10 Deroder, the $\overline{400}$ line **49***e*.**04**, the $\overline{200}$ line **49***e*.**07**, the 800 line **49***e*.**02** and the 100 line **49***e*.**11**, from the Memory Address Select Register, FIG. 49*e*, are up. The only two lines effective are the 800 line **49***e*.**02** and the 100 line **49***e*.**11**, which are combined in an AND circuit to provide an output on the 900 (P) line **3***c*.**19**. The 900 (P) line **3***c*.**19** goes to the Memory X Switch Core Read Drivers of FIG. 6 and when the Memory X Read Gate (P) line **5***g*.**07** comes up at $R_{1.3}$ as shown in FIG. 144, an output is provided on the 900 line **6.10** which goes to the X Switch Core Read windings of FIG. 9. In FIG. 9, the X Switch Core Matrix, the line **6.10** passes from left to right through the upper row of the Switch Cores providing set current therefor and returns to FIG. 6 as line **9.01** providing feedback into the Amplifiers as shown in FIG. 6. Accordingly, the only core set is the 10915–10919 one at the intersection of lines **7***c*.**04** (also labeled line **9.11** at the bottom of the sheet) and **6.10** (also labeled line **9.01** at the bottom of the sheet), providing an output on the secondary winding for the addresses 10,915–10,919. This output goes to the Memory Core Array of FIG. 13 to provide half select current to the cores linked by the 10,915 line. The core at the intersection of the 10,915 line and the 9040 line receives full select current. It will be recognized the sum of these two addresses, 10,915 and 9040, is equal to the address 19,955. As described previously, the two half select currents tend to reset the core and if the core at the intersection of the lines just mentioned is a "1," then an output is detected on the sense line to give an indication of such as shown in FIG. 144. If the core contains a "0," the reset current is of no practical effect and a signal is not produced on the sense line. It has been pointed out that the Memory Core Planes of FIG. 13 are stacked such that thirty-five planes are arranged one above the other. The 9040 line and the 10,915 line provide the half select current not only to the Memory Core Plane as illustrated, FIG. 13, but to all thirty-five of the core planes in parallel such that thirty-five bits are read out on the sense windings, lower and upper, which are directed to the Sense Amplifier circuits of FIGS. 15*a* and *b*. The outputs of the Amplifier circuits are sampled at $R_{3.5}$ and if the core is changing from a "1" to a "0" outputs are provided on the lines **14***a* and *b* to the Memory Buffer Register of FIGS. 14*a* and *b*. In an example to follow, it will be assumed that the contents of the Memory Buffer Register are read back into the same address in Core Memory.

The inputs to the Sense Amplifiers are full wave rectifiers (TMS), comprising a pulse transformer and two diodes (not shown). The two diode plates are tied to the opposite ends of the secondary windings of the pulse transformer, the diode cathodes are tied together to ground making a full wave rectifier. The full wave rectifier feeds the first stage of a pair of amplifiers which are RC coupled pentode stages (AMS) which feed a cathode follower (K). The grid of the cathode follower (K) is diode clamped to keep it from going below a bias voltage of approximately −27 volts on the line **5***h*.**09**.

Sample positions of the Memory Buffer Register are shown in FIGS. 14*a* and *b* for the characters 4, 3 and 2 and 0 and 1 respectively. The Memory Buffer Register has thirty-five triggers and is set to the outputs of the sense amplifiers by the Memory Sample pulse at $R_{3.5}$ on the lines **20***e*.**03** and **20***e*.**04**. Information once set into the Memory Buffer Register is held by the triggers until W_3 of the character cycle. Thus, information in the MBR is available either for processing or writing back into Memory. The Memory Buffer Register output lines are connected as best illustrated in FIGS. 2*c* through 2*e* and furnish inputs to the Memory Buffer Register Code Check circuits, FIGS. 19*a* and *b*, the Memory Address Register, FIGS. 17*a* through *e*, the Input Switch, FIG. 11, and the Output Switch, FIGS. 20*a* through *d*. On Instruction cycles character 0 position of MBR furnishes a character to the Operation Register, FIGS. 21*a* and *b*; character positions 1, 2 and 3 provide numeric bits and character 1 provides B and A bits also to the Memory Address Register, FIGS. 17*a* through *e*; and the MBR character 4 position passes numeric bits through the output switch to the Memory Address Register but the B bit character position 4 goes directly to MAR. As previously mentioned, when it is desired to Write the information contained in the Memory Buffer Register of FIGS. 14*a* and *b* into the Core Array of FIG. 13, the half select currents on the lines 9040 and 10,915 are reversed for all thirty-five planes to set the cores to the "one" state. However, in those core planes where it is desired to store "zeros" in a particular core according to the state of the triggers in the Memory Buffer Register, inhibit current is supplied which counteracts the set currents thereby preventing the setting of the selected core in that plane in the "one" state.

In FIG. 10, Memory Input Select, the Result to Memory 1 line **137.01** is down since in the operation to be described the contents of the Memory Buffer Register are to be written back into the Core Memory Array. Accordingly, all of the outputs of the AND circuits of FIGS. 10 are down, and the inverters cause the Buffer Register to Memory output lines **10.01**, **10.03**, **10.05**, **10.07** and **10.09** to be up. These signals are provided to the Input Switches of FIGS. 11*a* and *b* and the NOT outputs on lines **14***a*.**01** ($\overline{N}$) and **14***b*.**02** ($\overline{N}$) of FIGS. 14*a* and *b*, are supplied to FIGS. 11*a* and *b*, respectively, for the characters 4, 3, 2, 1 and 0. Therefore, for each bit position of the Memory Buffer Register containing a "zero" the $\overline{N}$ output will be up. In FIGS. 11*a* and *b*, when the Buffer Register to Memory lines **10.09** and **10.01** are up, outputs will be provided on the lines to the Inhibit Driver circuits of FIGS. 12*a* and *b* for each bit position of the characters 0 through 4 which contain a "zero." Referring now to FIGS. 12*a* and *b*, the lines from the input switch of FIGS. 11*a* and *b* are up according to the "zero" bit configurations of the characters in the Memory Buffer Register, and when the Memory Inhibit Gate is applied on the lines **5***g*.**02** and **5***g*.**01**, between R_4 and W_0, as shown in FIG. 144, outputs are provided from FIGS. 12*a* and *b* to the Inhibit windings of FIG. 13 for those planes where it is desired to write "zeros." In FIG. 13, the inhibit current applied to each selected plane where a "zero" is to be written opposes that current through the X Driver line tending to set the core to a "one." At W_0 the Write Gate is provided, as shown in FIG. 144, to the Y Switch Core Write Drivers of FIGS. 5*b* and *c* on the lines **5***g*.**03** and **5***g*.**04** respectively, bringing up only the 40 line **5***b*.**03** which, as mentioned previously, was not energized during the Read portion of the cycle. In FIG. 8, the only core in the set condition prior to Writing is the core 9040 at the intersection of the 9000 line **4.10** and the 40 line **5***b*.**03**, and the 40 line **5***b*.**03** provides reset current to the core 9040 and provides feedback current to the Y Switch Core Write Drivers of FIG. 5*b* on the line **9.03**. In FIG. 4, Memory Y Switch Core Read Drivers, the Read Gate on line **5***g*.**08** is down and, therefore, the signal formerly provided on the 9000 line **4.10** during Reading is absent during Writing. Referring to FIG. 8 once again, it is pointed out that the 9000 line **4.10** is not driven and that the 9040 core is reset from 1 to 0 thereby providing half select current in FIG. 13 in a direction tending to set each core in the 9040 row of each of the thirty-five planes to a "one."

In FIGS. 7*b* and *c*, X Switch Core Write Drivers, the output lines which were up during the Read portion of the cycle are down since the Read bias gate is down. However, the 10,015–10,019 output line **7***c*.**04** is up due to Memory Write Gate line **5***g*.**06** which comes up at W_0. Accordingly, in FIG. 9 only the 10,015–10,019 line **7***c*.**04** is carrying current tending to reset the cores linked thereby, and the only core which is affected by the reset current is the core corresponding to the Address 10,915–10,919 which was set during Reading. Current is not provided on the 900 line **6.10** from the Switch Core Read Drivers and therefore, the secondary of the Switch Core associated with Address 10,915–10,919 supplies half select current to the Array of FIG. 13 on the line labelled 10,915. In the absence of inhibit current, the core in FIG. 13 at the intersection of the lines 9040 and 10,915 is set to a "one," and, as previously described, inhibit current is applied to those cores corresponding to MBR positions which contain "zeros."

It will be noted that although the Memory Address Select Register, FIG. 49, contained the address 19,955, for the operations just described, the characters were read into the Memory Buffer Register corresponding to addresses 19,955 to 19,959 and the same characters would have been read into the Memory Buffer Register for addresses 19,956; 19,957; 19,958; and 19,959. However, as mentioned previously, the Memory Out of FIG. 20 selects the character from the Memory Buffer Register for processing which corresponds to the units position of the address Select Register. Accordingly, the address of 19,955 specifies character "zero" to be read from the Memory Buffer Register. In this regard, the Memory 4×5 Decoder of FIG. 3*e* determines which of the characters shall be selected according to the units position of the Address. The $\overline{8}$ line **49***a*.**02**, the $\overline{2}$ line **49***a*.**11**, the 4 line **49***a*.**08** and the 1 line **49***a*.**17** are up. These signals are decoded to provide an output on Select Character 0 line **3***e*.**01** which goes to the Memory Output Select, FIG. 20*a*. In FIG. 20*a* assume, for the present, that low character line **36***b*.**04** and high character line **36***b*.**06** are down, in which case the Normal line from the OR circuit, the Inverter, and the two cathode followers is up which gates the Select Character 0 line **3***e*.**01** to provide an output on Select Character 0 Out line **20***a*.**04**. The latter line goes to Output Switch (Characters 1 and 9) of FIG. 20*b* where the character 0 lines **14***b*.**06** (C) through **14***b*.**06** (1) from FIG. 14*b*, are gated with the Select Character 0 Out line **20***a*.**04** to provide outputs on the C bit line **20***b*.**01**, B bit line **20***b*.**02**, A bit line **20***b*.**03**, 8 bit line **20***b*.**04**, 4 bit line **20***b*.**05**, 2 bit line **20***b*.**06** and the 1 bit line **20***b*.**07**, for those positions of character 0 containing binary "ones." The Memory Out Bus of FIG. 20*d* receives the character 0 signals which are passed through on the lines **20***d*.**01** through **20***d*.**07** to CR 1, FIG. 57, where they are gated to the triggers by the Set CR 1 pulse (D0.4) on the line **100.02** to set the triggers according to the bit configuration of the character 0.

What has been described in the example of Reading

from and Writing into Memory concerns a R/W cycle of 9 microseconds, but it will be appreciated that a similar operation occurs during an Instruction cycle of 13 microseconds. In FIG. 145, the sequence of events will be recognized as the one of FIG. 144 except that the period A_0 through A_3 has been inserted between R_4 and W_0. The time $A_{3.5}$ of FIG. 145 corresponds to $R_{4.5}$ of FIG. 144.

In the foregoing example where the address 19,955 was employed, it will be appreciated that the address is improper for an Instruction since only character 0 was addressed and all Instruction addresses must end in either a 4 or a 9.

GENERAL DESCRIPTION OF AUXILIARY AND ACCUMULATOR STORAGE

As mentioned previously, Auxiliary and Accumulator Storage provide 512 character positions of Storage, divided into one 256 character capacity Accumulator unit, fourteen 16 character capacity Auxiliary Storage units and one 32 character capacity Auxiliary Storage unit. The addresses for Auxiliary Storage units are 0 through 255 inclusive, and the addresses for Accumulator Storage are 256 to 511 inclusive. Only one character position in Accumulator or Auxiliary Storage can be addressed during one cycle, and it follows that Auxiliary and Accumulator Storage cannot be used simultaneously.

Since seven Core Planes such as the one shown in FIG. 45 are used in the Storage Array, seven ferrite cores (one for each core plane) are interrogated each cycle when reading Storage. Each Storage core plane comprises a 16×32 matrix (FIG. 45), interrogated by Y inputs comprising 16 address lines and X inputs comprising 32 address lines. The Storage Address Select Register, FIGS. 53*a* and *b*, is set only from the Storage Address Counter, FIGS. 52*a* through *d*, with a pulse at R_0 time that occurs at the same time that the Memory Address Register is set to the Memory Address Counter 1. The Address of the Storage Address Select Register is immediately decoded in the four decoders, namely, the 2×4 Decoder, FIG. 34*a*; the 2×4 Decoder, FIG.34*b*; the 2×4 Decoder, FIG. 34*c*; and the 3×8 Decoder, FIG. 34*d*. The decoder outputs are mixed with Read Bias, Read and Write Gates to control the Switch Core Matrices of FIGS. 39 and 35. The Y Switch Core Matrix, FIG. 39, contains sixteen switch cores in a 4×4 array and the X Matrix, FIG. 40, contains thirty-two switch cores in two 4×4 arrays and on a Read operation, one X and one Y switch core are selected from the X and Y Switch Core Matrices respectively. These two matrices selectively energize the sixteen Y Address lines and thirty-two X Address lines which are provided in parallel to the seven planes of the Storage Array for which FIG. 45 is a sample plane.

Each core plane, such as the one illustrated in FIG. 45, has a Sense Winding linking all cores of the plane and each Sense Winding feeds a one of seven Sense Amplifiers of FIG. 46. During Reading, the Sense Amplifier outputs are sampled to place the character into the seven character capacity Storage Buffer Register, FIG. 47. One set of Storage Buffer Register output lines is connected to CR 2, FIG. 48, via the Storage Out Bus, and another set of output lines is connected to the Storage In Select and Switching Circuits, FIG. 43. Two possibilities exist for writing a character into Accumulator Storage: (1) The character retained in the Storage Buffer Register may be rewritten into Storage at the Address from which it was taken, or (2) the Result character from the Result Register available on the Storage In Bus may be written into Storage. The line which selects one or the other of the previously mentioned characters is the Result to Storage line **137.05**, and if Result to Storage line is down, the Storage Buffer Register character is gated to the Input Switch of FIG. 43 for rewriting into Storage; otherwise, with the Result to Storage line up, the character on the Storage Bus from the Result Register is gated through the Input Switch and written into Storage.

The Storage Address Select Register of FIGS. 53*a* and *b* comprises triggers 1, 2, 4, 8, 16, 32, 64 and 128, having a capacity to store any Address 000 through 255. This is adequate to address the Auxiliary Storage positions; however, to permit addressing Accumulator Storage (256 through 511), the SASR 256 line **54.24** is required. This line **54.24** originates in Storage Select Register Decoding, FIG. 54, and is under the control of the Storage Select Register Triggers, FIG. 16*a*, lines **16*a*.24**, **16*a*.17**, **16*a*.16** and **16*a*.03**.

The Storage Select Register Triggers of FIG. 16*a* are set during Instruction cycles according to the zoning over the tens and hundreds position of characters 2 and 3 of the Instruction. With no zoning present, the Accumulator Storage is addressed, and, in this case, the four Storage Select Register triggers of FIG. 16*a* are Off, and the Storage Address Select Register 256 line **54.24** and the SSR=0000 lines are up. If the address contains zoning in the tens and hundreds order, Auxiliary Storage is addressed, in which case, one or more of the SSR triggers will be On thereby causing the 256 line **54.24** to be down and the $\overline{256}$ line **54.01** and the SSR≠0000 lines to be up. If the 256 line is up, the Storage position addressed will be 256 plus the address in the Storage Address Select Register, which addresses will be in Accumulator Storage. If the $\overline{256}$ line **54.01** is up, only the address held in the Storage Address Select Register is interrogated and Auxiliary Storage is addressed.

The 256 line **54.24** and the $\overline{256}$ line **54.01** go to Storage Decoding System of FIG. 34*a*, where they are mixed with the Storage Address Select Register 128 line **53*b*.08** and the SASR $\overline{128}$ line **53*b*.07**. The SSR=0000 lines of FIG. 54 allow SAC to be set to SPC, and identifies Instructions which have no bits in the zone portions of characters 2 and 3. SSR≠0000 allows the four high order positions of SAC to be set by SSR and resets to "zero" the four low order positions of SAC. When SASR is set to SAC and combined with SASR $\overline{256}$, the units position of the proper Auxiliary Storage Unit is selected. In FIG. 34*a*, if Auxiliary Storage is addressed either 000 line **34*a*.01** or 128 line **34*a*.02** will be up, because the 256 line **54.24** is down. With the 256 line **54.24** up for addressing Accumulator Storage, either the 256 line **34*a*.03** or 384 line **34*a*.04** will be up. The Read Bias, Read and Write currents occur essentially in the same timing relation as those generated for Core Memory; however, duplicate generators are required because Storage and Memory may be used either simultaneously or individually and controlled accordingly.

The X and Y Switch Core addresses are each obtained by adding the numbers of the intersecting Drive lines in FIGS. 39 and 40. The addition of the X and Y Switch Core addresses so obtained produce the number contained in the Storage Address Select Register that causes the selection of the character at that address in Storage.

STORAGE ARRAY

Seven core planes such as the one shown diagrammatically in FIG. 45 plus a dummy plane make up the Storage Array. The core planes are designated C, B, A, 8, 4, 2 and 1 according to the bit position which they individually store. The dummy plane is used for connection purposes only. The X and Y Address lines link rows and columns of cores in Storage as explained with reference to Core Memory so that for each character address a particular core in each of the seven planes is interrogated to provide binary indications for seven bits of a character. Each of the thirty-two X address lines and sixteen Y Address lines form one closed loop including the secondary winding of the appropriate switch core for each address line and the selected core is at the intersection of a driven X and a driven Y line as explained

with reference to operation of Memory. Since the Storage Array is functionally, but not physically, divided into two parts, the division is effected along the Y axis by assigning to Accumulator Storage the Y lines from 256 to 480 inclusive and assigning to Auxiliary Storage the Y lines from 0 to 224 inclusive (see top of FIG. 45). Auxiliary Storage Unit 1 uses positions 16 through 31 of the Y Address line 0; Auxiliary Storage Unit 2 uses positions 0 through 15 of the Y Address line 32; Auxiliary Storage Unit 15 uses positions 16 through 32 of the Y Address line 224 and positions 0 through 15 of the Y Address line 0. The operation of Accumulator Storage utilizing a particular address follows.

OPERATION OF STORAGE

Normal operation of Storage is best illustrated by example assuming a particular address such as Unit 6 of Auxiliary Storage which is addressed by a "one" in the A bit position of character 2 and a "one" in the B bit position of character 3.

Referring now to the Storage Select Register of FIG. 16*a*, the SSR–4 and SSR–2 triggers are turned On via MBR Character 2–A line **14***a*.**02**, MBR Character 3–B line **14***a*.**02**, and the A_0 (D0.4) I time line **101.24**. With this setting of the SSR triggers, the SSR–8 Off lines **16***a*.**01** and **16***a*.**02**, the SSR–4 On lines **16***a*.**10** through **16***a*.**13**, the SSR–2 On lines **16***a*.**17** through **16***a*.**20** and the SSR–1 Off lines **16***a*.**21** through **16***a*.**23** are up. In FIG. 54, lines **16***a*.**17** and **16***a*.**16** are up, so the SASR $\overline{256}$ line **54**.**01** and the SSR≠0000 lines **54**.**02** through **54**.**08** are up. As mentioned previously with respect to FIG. 2, On and Off output lines from each position of SSR are connected to positions 128, 64, 32 and 16 of SAC, FIG. 52. In FIGS. 52*d*, SSR–1 Off line **16***a*.**23**, SSR–2 On line **16***a*.**20**, SSR–4 On line **16***a*.**13** and SSR–8 Off line **16***a*.**02** are up. Upon the occurrence of a pulse on the Set SAC to SSR line **52***e*.**06** at W_1, the Set SAC–$\overline{16}$ line **52***d*.**01**, Set SAC–32 line **52***d*.**04**, Set SAC–64 line **52***d*.**06** and Set SAC–$\overline{128}$ line **52***d*.**07** are up to FIG. 52*c* where the SAC triggers 64 and 32 are turned On and the SAC triggers 18 and 128 are turned Off if On previously. Since the SPC is not used when addressing Auxiliary Storage, the four lower order positions of SAC are reset Off by the Set SAC to SSR line **52***e*.**07** from SAC controls of FIG. 52*e*, which results from signals on the I time line **124**.**33**, SSR≠0000 line **54**.**02**, A_2/R_3–W_1 (Use) line **103**.**06** and Set SAC to SPC line **93***j*.**08**.

The outputs of SAC are used to set the SASR at R_0 time of each Execute cycle. Therefore, the address in SAC can be altered during each cycle in preparation for the next cycle while SASR holds the location of the character being processed. In FIG. 53*a*, all of the SASR triggers are turned Off by the SAC–$\overline{1}$, SAC–$\overline{2}$, SAC–$\overline{4}$ and SAC–$\overline{8}$ lines being up when the R_0 (D0.4) pulse appears on the line **101**.**06**. In stages 5–8 of SASR, FIG. 53*b*, the 32 and 64 triggers are turned On by the SAC–32 line **52***c*.**05** and the SAC–64 line **52***b*.**07** at R_0 (D0.4). The 16 and 128 triggers are turned Off at the same time via the SAC–$\overline{16}$ line **52***c*.**02** and the SAC–$\overline{128}$ line **52***b*.**08**.

In the 2×4 Decoder of FIG. 34*b*, the SASR–64 line **53***b*.**06** and the SASR–32 line **53***b*.**04** are up causing the 96 line **34***b*.**04** to be up. In FIG. 36*a*, the signal on the 96 line **34***b*.**04** is inverted to bring down the $\overline{96}$ line **36***a*.**04**. Since the 00 line **34***b*.**01**, the 32 line **34***b*.**02**, and the 64 line **34***b*.**03** are down, the $\overline{00}$ line **36***a*.**01**, $\overline{32}$ line **36***a*.**02** and the $\overline{64}$ line **36***a*.**03** are up. In FIG. 36*b*, the last mentioned lines are combined with Storage Read Bias Gate on line **7***d*.**02** to provide positive signals on the output lines **36***b*.**01**, **36***b*.**02** and **36***b*.**03** at R_0. The 96 line **34***b*.**04** is not gated at this time since the Storage Write Gate on line **7***d*.**08** is down at this time. In FIG. 39, reset current flows through the columns linked by the lines **36***b*.**01**, **36***b*.**02** and **36***b*.**03** and is fed back to FIG. 36*b* on the lines **39**.**04**, **39**.**03** and **39**.**02**.

In the 3×8 Decoder of FIG. 34*d*, the SASR $\overline{4}$ line **53***a*.**05**, the SASR $\overline{2}$ line **53***a*.**03** and the SASR $\overline{1}$ line **53***a*.**01** are up providing a positive signal on the Decimal 0 line **34***d*.**01** to FIG. 38*a*, where the output $\overline{0}$ line **38***a*.**01** is brought down. The remaining output lines are up because of Inverters since their inputs are down. The output signals of FIG. 38*a* are provided to the Storage X Switch Core Write Drivers of FIGS. 38*b* and *c* whereupon at $R_{0.5}$ the Storage Read Bias Gate Even on line **42**.**03** provides outputs on the 2 line **38***b*.**03**, 4 line **38***e*.**01** and 6 line **38***c*.**03**. The Storage Read Bias Gate Even is derived from Odd and Even Gating circuits of FIG. 42 where the SASR $\overline{1}$ line **34***d*.**10** and Storage Read Bias Gate line **7***d*.**01** are combined. In FIG. 40, the X Switch Core Matrix, the columns linked by the 6 line **38***c*.**03**, the 4 line **38***c*.**01** and the 2 line **38***b*.**03** are driven by reset current which is fed back to FIGS. 38*b* and *c* on the lines **40**.**07**, **40**.**05** and **40**.**03**.

In FIG. 34*a*, the SASR $\overline{128}$ line **53***b*.**07** and SASR $\overline{256}$ line **54**.**01** are positive as previously described bringing up the 000 line **34***a*.**01**, the latter going to the Y Switch Core Read Drivers of FIG. 37. In FIG. 37, the Storage Read Gate is provided on the line **7***d*.**03** at R_1 and, as a result, the 000 output line **37**.**01** is made positive to drive the 000 row of the Y Switch Core Matrix of FIG. 39 with set current and provide feedback to FIG. 37 on the line **37**.**08**. Since reset current is being applied on the 00 line **36***b*.**01**, the 32 line **36***b*.**02** and the 64 line **36***b*.**03** and set current is now supplied on the line **37**.**01**, the Switch Core at the intersection of the 96 line **36***b*.**04** and 000 line **37**.**01** is set causing an output on the secondary winding **96** to the Storage Array of FIG. 45.

In FIG. 34*c*, Storage 2×4 Decoder, the SASR $\overline{16}$ line **53***b*.**01** and the SASR $\overline{8}$ line **53***a*.**07** are up providing a positive signal on the 0 line **34***c*.**01** to the X Switch Core Read Drivers of FIG. 35. In the latter figure, the 0 Even output line **35**.**01** is brought up at $R_{1.5}$ by the line **34***c*.**01** and the Storage Read Gate Even line **42**.**04**. In FIG. 40, the 0 Even line **35**.**01** furnishes set current to the cores linked thereby and feedback current to FIG. 35 on the line **40**.**16**. Since reset current is flowing in the 6 line **38***c*.**03**, the 4 line **38***c*.**01** and the 2 line **38***b*.**03** and set current is flowing in the 0 Even line **35**.**01**, the core at the intersection of the lines **38***b*.**01** and **35**.**01** is set causing an output in the secondary winding 0.

In FIG. 45, half-select currents in directions for changing the state of a core from "one" to "zero" are flowing through the 0 and 96 lines in each of the seven planes of which FIG. 45 is a sample. Accordingly, for each plane containing a binary "one" an output is provided on the Sense Windings to the Sense Amplifiers of FIG. 46.

The Sense Amplifiers of FIG. 46 are biased by the line **5***h*.**11** and provide positive outputs on those lines where corresponding cores switch from "one" to "zero." The outputs, if any, on the C, B, A, 8, 4, 2 and 1 lines **46**.**01** through **46**.**07** are furnished to the Storage Buffer Register, FIG. 47, where signals indicating binary "ones" are gated to turn On the corresponding triggers by the Sample Pulse on line **5***i*.**01** at $R_{3.5}$.

The contents of either the Storage Buffer Register or the Result Register may be written back into the same address in Storage during the Write position of the R/W cycle. Assume as an illustration that the bit configuration contained in the Storage Buffer Register of FIG. 47 is to be written into Auxiliary Storage unit 6 (location 96) which is the same address read from previously. In the same manner as explained with reference to Memory, half-select currents are applied to each core plane on the X and Y drive lines in a direction such that binary "ones" are written into the specified address in all bit positions except those where inhibit current is provided as a result of positions in the SBR containing binary "zeros." In this regard, the Off sides of the triggers of SBR, FIG. 47, are used by connecting the lines **47**.**01** through **47**.**07** to

the Input Switch of FIG. 43. In FIG. 43, the Result to Storage line **137.05** is down (the unused line is always up) and the Inverter associated therewith supplies a positive voltage to the Add circuits fed by the input lines from SBR. Those output lines, among the group lines **43.01** through **43.07**, are up for each bit position of SBR which contains a "zero." In FIG. 44, the indications of the "zeros" in the SBR are received and gated by the Storage Inhibit Gate line **7***d*.**05** at $R_{4.5}$ to FIG. 45 where the Inhibit winding of each plane in which "zeros" are to be written is driven.

In FIGS. 36*a*, the lines **36***a*.**01**, **36***a*.**02**, **36***a*.**03** are up but cannot be gated to the Y Switch Core Windings of FIG. 39 via the Y Switch Core Write Drivers of FIG. 36*b* since the Storage Read Bias Gate line **7***d*.**02** is down. However, the 96 line **34***b*.**04** is up, and at W_0 the Storage Write Gate on the line **7***d*.**08** brings up the 96 line **36***b*.**04** to FIG. 39 where it provides reset current to the cores 96, 224, 352 and 480. The 96 core is the only one previously set and, therefore, the only one reset to provide an output from its secondary.

In FIG. 41, the 0 line **41.01** is up to the X Switch Core Write Drivers of FIG. 38*b*. In FIG. 7*e*, the output line **7***e*.**04** is up because of the Inverter, and in FIG. 7*d*, the Storage Write Trigger has been turned On by Read Storage line **93***a*.**02** and R_5 or A_4 (W_0) bringing up the Storage Write Gate lines **7***d*.**06** through **7***d*.**08**. Referring now to FIG. 38*b*, the 0 line **41.01** from FIG. 41 is gated by lines **7***e*.**04** and **7***d*.**06** to drive the 0 line **38***b*.**01** thereby providing reset current to the 0, 8, 16 and 24 cores of the X Switch Core Matrix of FIG. 40. In the latter figure, the 0 core was set to "one" during Read time and is now reset by the **38***b*.**01** line providing an output signal on the secondary coil 0. Referring once again to FIG. 45, half-select current is flowing in both the Y winding 96 and the X winding 0 tending to set the fully selected core in each plane to a "one," but, inhibit current prevents such a setting in those planes where a "zero" should be written according to the setting of the SBR as described previously.

Assume now that it is desired to read from an address in Accumulator Storage. The B and A bit positions of characters 2 and 3 of the Instruction address are "zeroes" and, therefore, the SSR contains "zeros." Whether an Instruction cycle or an Execute cycle, the SPC determines the Accumulator address. For this example, an address of 356 set in the SPC will be used.

In FIG. 16*a*, Storage Select Register, the four triggers are Off because of the absence of zone bits in the Accumulator Address coding and accordingly, in FIG. 54, the SSR=0000 and SASR 256 lines are up since SSR–1 On line **16***a*.**24**, SSR–2 On line **16***a*.**17**, SSR–4 On line **16***a*.**16** and SSR–8 On line **16***a*.**03** are all down. It is the SASR 256 line **54.26** in this instance that addresses the Accumulator generally since the SPC can only count from 0 to 255 (Recall addresses 0 through 255 are in Auxiliary Storage). Therefore, the SPC contains a count of 100 which, in effect, is added to 256 to address location 356 in Accumulator Storage.

The SPC of FIGS. 51*a*, *b* and *c* contain a count of 100 so SPC–$\overline{1}$ line **51***a*.**01**, SPC–$\overline{2}$ line **51***a*.**03**, SPC–4 lines **51***a*.**06** through **51***a*.**07**, SPC–$\overline{8}$ line **51***b*.**01**, SPC–$\overline{16}$ line **51***b*.**03**, SPC–32 lines **51***b*.**06** through **51***b*.**08**, SPC–64 line **51***c*.**02** and SPC–$\overline{128}$ line **51***c*.**03** are up. These signals are provided to SAC, FIGS. 52*b* and 52*d*, to turn On the 64, 32 and 4 triggers and turn Off the remaining triggers when the Set SAC to SPC pulse is provided on the lines **52***e*.**04** and **52***e*.**05**. In FIGS. 53*a* and *b*, SASR, the SAC–$\overline{1}$ line **52***a*.**01**, the SAC–$\overline{2}$ line **52***a*.**03**, the SAC–4 line **52***a*.**06**, the SAC–$\overline{8}$ line **52***a*.**07**, the SAC–$\overline{16}$ line **52***c*.**02**, the SAC–32 line **52***c*.**05**, the SAC–64 line **52***b*.**07** and the SAC–$\overline{128}$ line **52***b*.**08** are up and at R_0 (D0.4) the lines **101.07** and **101.06** set SASR to the contents of SAC. The SASR now contains the value 100.

The principles of reading and writing into address 356 are the same as those described in the example pertaining to Auxiliary Storage and will not be repeated. From the description above, the differences of addressing Accumulator and Auxiliary Storage are apparent.

CHARACTER REGISTERS

At A_0 or W_0, a character read out of Memory is set into Character Register 1 of FIG. 57 where it remains until A_0 or W_0 of the next character cycle. Since CR 1 is not provided with a reset to "zero," a new character is merely written "over" the previous character at set time. At W_0, a character read out of Storage is set into Character Register 2 of FIG. 48 where it remains until W_0 of the next character cycle when another character may be set into the CR 1 triggers. Storage is not read from during Instruction cycles so provision is not made for setting CR 2 at A_0 as in the case of CR 1.

Refer now to the CR 1 circuits of FIG. 57. The circuits for Storage of each bit in a trigger are identical and only the details of the circuits for the 1 bit position of the character will be described.

If a binary "one" is contained in the 1 bit position of a character read from Memory and to be entered in CR 1, the Memory Out Bus 1 line **20***d*.**07** is positive to condition one input of a gate (GJ) for the left side of the 1 trigger which passes the Set CR 1 signal on a line **100.02** to turn On the 1 trigger bringing up the CR 1–1 line **57.15**. If a binary "zero" has been read out of Memory instead, the Memory Out Bus–1 line **20***d*.**07** is down, but the output of an Inverter (IK) is up to condition a diode gate (GJ) for the right side of the 1 trigger. Thus, the Set CR 1 pulse on line **100.02** sets the 1 trigger to "zero," and the CR 1–1 line **57.14** is made positive.

The 1 trigger, when On, provides a positive signal on the CR 1–1 line **57.15** to the Right Plate Outputs of FIG. 58, and the 1 trigger, when Off, provides a positive signal on the CR 1–$\overline{1}$ line **57.14** to the Left Plate Outputs of FIG. 59.

The circuits of Character Register 2 of FIG. 48 are similar to those shown and described for Character Register 1 and the description will not be duplicated.

ADDER INPUT SWITCHING

In FIG. 73, the output signals representing the numeric portions of the character in CR 1 are present on the CR 1–8 line **58.37**, CR 1–2 line **58.47**, CR 1–4 line **58.42** and CR 1–1 line **58.52**. For those bits in Character Register 1 which contain binary "ones," positive signals are present on these respective lines. The Zone bits, A and B, of CR 1 are fed from CR 1 Right Plate Outputs to Adder Input switching on the CR 1–A line **58.23** and the CR 1–B line **58.06** respectively where the zone bit lines are gated by the CR 1 to Adder line **93***b*.**01** onto the output lines **73.01** and **73.08** to the Zone Adder of FIG. 79.

If the contents of CR 1 are not "zero" as signified by the CR 1≠0 line **71***b*.**11** being positive or the machine is executing a Set Bit instruction as indicated by the Set CR 1≠ line **231.01** being positive, then, as the CR 1 to Adder line **93***b*.**01** goes positive, those AND circuits which are otherwise conditioned furnish positive output signals to FIGS. 80, 81 and 82 on the CR 1 to Adder (A) line **73.01**, CR 1 to Adder (8) line **73.02**, CR 1 to Adder (2) line **73.03**, CR 1 to Adder (4) line **73.04**, CR 1 to Adder (1) line **73.05** and CR 1 to Adder (B) line **73.08**. The Minus on Suppress 8 bit to Adder line **93***d*.**04**, Minus on Suppress 2 bit to Adder line **56***b*.**06**, Minus on Suppress 4 bit to Adder line **56***b*.**07**, Minus on Suppress 1 bit to Adder line **56***b*.**05**, are normally positive to condition their respective AND circuits. In those instances where it is desired to suppress a bit, one of the lines just mentioned is down, thereby prohibiting the passage of the signal through one AND circuit to the output lines. When the contents of CR 1 equals zero (CBA8421=0001010), provision is made for changing the 8 and 2 bits to "zero." The AND circuits controlling the 8 and 2 bits are condi-

tioned by the CR 1≠ zero line **71***b*.**11**, and when this line is down (indicating CR 1=0), the 8 and 2 bits are not passed but are blocked from the output thereby making all bits of the character "zero" for numeric processing within the ALU.

When CR 1 holds a value greater than 10 during a Compare instruction, the 8 bit from CR 1 must be blocked, and this is accomplished by bringing down the (—) On Suppress 8 bit to Adder line **93***d*.**04**.

The lower portion of FIG. 73 illustrates circuits for switching either the numeric contents (8, 4, 2, 1 bits) of CR 1 or the numeric contents of CR 2 to the True/Complement Controls of FIG. 83 via OR circuits having gated inputs from the numeric portions of CR 1 and CR 2. When CR 1 to T/C line **93***b*.**03** and CR 1≠0 line **71***b*.**12** are positive, the numeric contents of CR 1 are gated onto the output lines **73***b*.**09** through **73***b*.**14**. When CR 2 to T/C line **93***b*.**04** and CR 2≠0 line **76.22** are positive, the numeric contents of CR 2 are gated onto the output lines.

Although a character in which the bits are all "zero" (Storage Marks) is a legitimate character in CR 2, "zero" expressed as a character (0001010) is not processed in the ALU and must be converted to all "zero" bits. Accordingly, the CR 2≠0 line **76.22** is brought down to block the 8 and 2 bits from the output of Adder Input Switching when CR 2=0.

MULTIPLICATION

As mentioned previously, multiplication is accomplished by means of a multiple generator shown generally in the Multiply circuits **1.20** and Multiply Register **1.40**, in FIG. 1. More specifically, the foregoing circuits are shown in FIGS. 2*cc*, 2*dd*, 2*rr*, 2*ss*, 2*ggg* and 2*hhh*, comprising a Multiplicand Doubler and Quadrupler, FIG. 80, a Quintupler, FIG. 81, Multiple Selection Circuits, FIG. 82, Multiple Register, FIG. 78, Multiple Adder of FIG. 84, and Decimal Correction Circuits, FIG. 85. The Multiple Generator provides multiples of each digit of the Multiplicand, specifically, one times, two times, four times and five times the digit contained in Character Register 1. Proper multiples are selected in the Multiple Selection Circuit of FIG. 82 which is controlled by Multiple Register and Decoder of FIG. 82, the latter containing the digits of the Multiplier derived from CR 2. After selection, the multiples of the digit are added in the Multiple Adder of FIG. 84 and are then passed through Multiple Adder Correction Circuits, FIG. 2*ggg* (FIG. 85), to the Digit Adder. In the Digit Adder the sum of the multiples are added to digits of the previous partial product.

Since a doubled, quadrupled or quintupled multiple of a multiplicand digit may produce a carry, means are employed to store the carry so that they may be added to the generated multiples of the succeeding higher order digit during the next character cycle, FIGS. 2*cc* and 2*dd*. More specifically, in FIGS. 80 and 81, the doubled, quadrupled and quintupled values of each digit gated from Character Register 1, are generated whether or not multiplication is being performed. The Multiplier Control circuits contain the Multiple Register, FIG. 78, which during multiplication contains a multiplier digit, but is otherwise reset to represent the value of decimal 1, and thereby is effective as explained hereafter to gate a one times multiple for operations other than Multiply.

In FIG. 80, Multiplicand Doubler and Quadrupler (2 sheets) the Doubler portion comprises the lower portion of Sheet 1 of FIG. 80 where inputs from CR 1 to Adder are shown entering on the left. The two multiple is derived from the output lines **80.02** through **80.05**. The Doubler emits signals representing the double value of the character input thereto which signals are emitted to the Multiple Selection circuits of FIG. 82 and also the Quadrupler circuits of Sheet 2 of FIG. 80. The Quadrupler is, in effect, another doubler, so that upon doubling the doubled value a quadruple value is produced. Operation of the Multiply circuits is set forth in detail in the application "Electronic Multiplier," Serial No. 512,636, filed June 2, 1955, and assigned to the assignee of this application.

TRUE/COMPLEMENT CONTROLS

Referring to FIG. 83, the True/Complement Control circuits are shown consisting of switching circuits necessary to generate a 9's complement of the input thereto and also to gate either the True or Complement representation of the particular digit to the Digit Adder of FIG. 86. The input signals to the T/C Control circuits are emitted from the Adder Input Switching circuits, described above, and may represent characters from either Memory or Storage.

The 9's complement of a digit is that digit when added to the digit being complemented which results in a sum of 9. Consider the example where the digit 3 (0011) is complemented to result in 6 (0110). In this instance, the input T/C–2 line **73.11** and the 1 to T/C line **73.13** are positive and the 8 to T/C line **73.09** and 4 to T/C line **73.10** are negative. When the Complement line **93***d*.**07** goes positive, the T/C–4 line **83.03** and the T/C–2 line **83.04** become positive. However, if the Complement line is negative, the line **83.01** is positive and the True signals are passed unmodified on the lines **83.04** and **83.05** to the Digit Adder, FIG. 86. It will be noticed that the T/C–2 line **83.04** passes directly from input to output since the binary "ones" or "zeros" for the 2 bit are the same in both True and Complement form.

DIGIT ADDER

The Digit Adder is shown in FIG. 86 and adds digits (parallel by bit and serial by digit) from CR 2 via Adder Input Switching (FIG. 73) and True/Complement Controls (FIG. 83) and from CR 1 via Adder Input Switching (FIG. 73), Multiple Selection (FIG. 82), Multiple Adder (FIG. 84) and Decimal Correction circuits (8, 4 and 2 bits only) (FIG. 85). In FIG. 86, the Digit Adder comprises four full binary adders connected in combination so that the sum of two binary coded decimal digits may be obtained. A carry from each binary order is connected to an input of the succeeding higher order except for the "one" bit carry input which is a decimal carry resulting from the previous addition of the succeeding lower order of BCD digits. Each full adder has three inputs, a pair for corresponding bit values of the digits to be added and a carry input, for example, MPL 4 line **85.03**, T/C–4 line, and Binary Sum 2 Carry line. If binary "zeros" are supplied at all three inputs, both sum and carry outputs are binary "zeros." When one input only contains a binary "one," the sum output only contains a binary "one." When any two inputs simultaneously contain binary "ones," the carry output only contains a binary "one." When all three inputs contain binary "ones," both sum and carry outputs contain binary "ones." The full adder circuits are conventional and their operation is so well known to those skilled in the art that a description of their operation is unnecessary.

The arithmetic circuits of the ALU cannot perform subtraction directly but achieve the same result by complementary addition. The True/Complement Control circuits of FIG. 83 produce only the 9's complement, and the 10's complement is required in the units order of the field being added to arrive at the correct result. Consider the following example:

The number 14 is to be subtracted from the number 48 which should give a result of 34. Accordingly, the 9's complement of 14, which is 85, is added to 48.

```
 48
 85
---
133 (carry neglected)
```

Since the 10's complement of a digit is the 9's complement plus 1, addition of 1 to 33 provides the required answer of 34. Therefore, when subtracting, a decimal carry is

supplied to the Digit Adder on the line **93***d*.**05** during the first Execution Character Cycle (ECC 1).

The output of the entire Digit Adder, comprising four full binary adders, may represent a sum of 0 through 19. A sum of 19 would result from the addition of digit 9 (lines **85.05** and **84.01** positive) and digit 9 (lines **83.02** and **83.05** positive) plus a carry from a succeeding lower order on the Decimal Carry In line **88.23**. Because the Digit Adder is a pure binary adder, correction is necessary since the sum must be represented in the BCD form. The correction is provided by the Decimal Correction circuits of the Digit Adder of FIG. 87.

As stated previously, the character from Memory to be added is passed unmodified through CR 1 (FIG. 2*h*), Adder Input Switching (FIG. 2*qq*), Multiple Selection circuits (FIGS. 2*rr*–2*ss*), Multiple Adder (FIG. 2*hhh*) and Multiple Adder Decimal Correction Circuits (FIG. 2*ggg*) to the Digit Adder (FIG. 2*eee*). In FIG. 78, the Multiple Register triggers are Instruction reset to the value "one" with the trigger at the top of the drawing having its left side in conduction and the remaining triggers having their right sides in conduction. Thus, the Select 1 Multiple line **78.01** is positive throughout the addition. In FIG. 82, the last-mentioned line gates the signals from CR 1 on the lines **73.05** (1), **73.03** (2), **73.04** (4) and **73.02** (8) onto the output lines **82.01** through **82.04**. In FIG. 84, the value represented by the signals present on the MPL–1B line **82.04**, MPL–2B line **82.03**, MPL–4B line **82.02** and MPL–8B line **82.01** is, in effect, added to zero and passed to the output lines **84.01** through **84.05** and, in turn, to the Decimal Correction circuits. In FIG. 85, if the Multiple Register contains a "zero" or a "one" as indicated by the MPL Reg≠0/1 line **98.05** being down, the Correction circuits are blocked, the MPL Carry Out line is down, and the No MPL Carry Out line is up, and the digit value is passed to the output lines **85.01** through **85.06**. The latter lines are connected as inputs to the Digit Adder of FIG. 86 and the Set Bit Routing Controls of FIG. 56*a*.

DECIMAL CORRECTION CIRCUITS, DIGIT ADDER

Chart IV below shows all of the inputs and outputs of the Digit Adder. It can be seen that any sum greater than nine must be corrected and that any sum equal to, or greater than, 16 produces a carry from the 8 bit adder on the lines **86.08** and **86.09**.

Chart IV

Dec Sum of Input		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
		Bi 8 Carry ⟶																1	1	1	1
Output of Adder	8	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
	4	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
	2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
		Dec Carry Out										1	1	1	1	1	1	1	1	1	1
Output of Correction Circuits	8	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1
	4	0	0	0	0	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	
	2	1	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

In FIG. 87, circuits are arranged to correct a digit represented by signals on the input lines **86.02**, **86.04**, **86.06** and **86.01** for the present cycle when the Digit Adder Out line **93***c*.**01** is made positive. Assume the decimal sum of the Adder is 12 as signified by the inputs on Binary Sum 8 line **86.06** and a Binary Sum 4 line **86.04** being positive and the Binary Sum 8 Carry line **86.08** being down. The Decimal Carry Out line **88.02** to FIG. 87 is positive because in FIG. 88 the Binary Sum 4 line **86.05**, Binary Sum 8 line **86.07** and (—) On Suppress Adder Carry line **93***d*.**01** are up. On Sheet 2 of FIG. 88 it will be observed that the positive signal on Decimal Carry Out lines **88.01** through **88.05** is inverted by IJK to make the lines **88.06** through **88.12** negative. Thus, in FIG. 87, the Binary Sum 8 and 4 signals are blocked by the No Decimal Carry Out line **88.07**, while the negative signal on the Binary Sum 2 line **86.02** is inverted and gated by the positive Decimal Carry Out line **88.02** to bring up the Result 2 lines **87.01** through **87.04**. In this manner, the 8 and 4 bit signals are corrected to a 2 bit signal (see Chart IV). Of course, correction of the value 12 requires that a carry be generated and preserved for use in the next cycle.

In FIG. 88 (Sheet 2), the positive signal on the lines **88.01** through **88.05** is directed to the gate (GJ) associated with the left side of the Decimal Carry trigger of FIG. 88 (Sheet 1). The gate is further conditioned by a positive signal on the MPY 2/NOT Transition line **67***d*.**15**, and at W_0 the line **101.11** goes positive and places the left-hand side of the Decimal Carry trigger in conduction. Therefore, the Decimal Carry In lines **88.23** through **88.32** of FIG. 88 (Sheet 2) go positive. During the next cycle, the Decimal Carry In signal on line **88.23** is used as the Carry In to the 1 bit Adder of FIG. 86 where it is added to the next digits.

In FIG. 88 (Sheet 1), the (—) On Suppress Adder Carry line **93***d*.**01** is brought down to block the AND circuits it feeds and thereby prevents the Decimal Carry Out line **88.02** (among others) from coming up. Thus, in FIG. 87, the line **88.02** is down and the No Decimal Carry Out line **86.06** is up permitting combinations of bits greater than 9 to pass to the output Result lines without being corrected. Such an operation is required in Load and Unload instructions where, for example, a $ sign having a numerical portion of the value 11 must pass through the Digit Adder and Decimal Correction circuits unchanged.

A zero output (8421=0000) from the Digit Adder must be converted to a decimal 10 (8421=1010) before entry in Memory or Storage, and this conversion is done in the Decimal Correction circuits of FIG. 87 by recognizing no bits from the Digit Adder. In the lower portion of FIG. 87, an OR circuit is fed by Sum-1, Sum-2, Sum-4 and Sum-8 lines to provide a Digit Adder Output ≠0 indication by a positive signal on the lines **87.17** through **87.23**. When none of the inputs to the OR circuit are positive, the last mentioned lines are negative, but the inverter (I) gates the Digit Adder Out signal on the line **93***c*.**01** onto the Result 2 and Result 8 output lines. Blank, Hyphen and Ampersand characters, whose numerical portions consist of 8421=0000, are recognized in either CR 1 or CR 2 and routing lines are conditioned to block the Digit Adder outputs which have the effect of sending 8421=0000 to the Result Register from the Digit Adder Correction circuits. Output signals from the Decimal Correction circuits, FIG. 87, are provided to the C Bit Generator of FIG. 90, the Result Register of FIG. 89, the Inter Register Check Routing of FIG. 63 and other circuits as previously described with reference to FIG. 2.

CHARACTER RECOGNITION CIRCUITS

Character Recognition Circuits are provided both for CR 1, FIGS. 71*a* and *b*, and for CR 2, FIG. 76. Both of these Recognition circuits operate in a similar manner for providing positive signals on output lines to indicate various classes of characters. By way of example, refer to FIG. 76, CR 2 Recognition, wherein an AND circuit receives inputs via CR 2–$\overline{1}$ line **75.49**, CR 2–2 line **75.39**, CR 2–$\overline{4}$ line **75.33**, and CR 2–8 line **75.18**. A section of the Code Chart given previously shows that a decimal 0 is

represented by a binary 10, i.e., binary 1 in the 2 and 8 positions. Thus, if all four lines just described are positive, it signifies a holding of a decimal 0 in Character Register 2, and an output is provided on the CR 2=0 lines **76.28** and **76.29**. When a digit other than a decimal 0 is provided in CR 2, it will be noted that the lines **76.22** through **76.27** are positive due to the Inverter in the line to indicate CR 2≠0.

The reference characters used to identify outputs of the Character Recognition circuits, although abbreviated, indicate the holding of the associated Character Registers. In FIG. 76, lines **76.01** through **76.04**, when positive, signify that the character in Character Register 2 is neither a Blank nor a Hyphen, nor an Ampersand. CR 2=BL line **76.05** signifies that CR 2 contains a Blank and CR 2≠BL line **76.06** signifies that CR 2 does not contain a Blank. A signal on CR 2=SM lines **76.09** through **76.18** indicated a Storage Mark. CR 2=BL/HYP/AMP/SM line **76.19** signifies a Blank, Hyphen, Ampersand or Storage Mark. CR 2≠SP CHAR line **76.20** indicates by positive signal that CR 2 does not contain a special character.

Referring to FIGS. 71*a* and *b*, CR 1 Recognition Circuits, output lines **71***a*.**01** through **71***a*.**03** indicate that Character Register 1 contains a Blank, Hyphen, Ampersand, or Storage Mark. CR 1 Odd line **71***a*.**04** indicates that the contents of CR 1 contain a Storage Mark, an invalid character in Memory. Lines **71***a*.**05** and **71***a*.**06**, when positive, give an output indicating that the contents of Character Register 1 are a Blank and that the contents of Character Register 1 are not a Blank respectively. Lines **71***a*.**07** through **71***a*.**10**, when positive, signify that Character Register 1 contents are not a Blank, Hyphen, Ampersand or Storage Mark. Line **71***a*.**11** indicates that the contents of the Zone bit positions of CR 1 are $\overline{B}$ and A. Lines **71***a*.**12** and **71***a*.**13** indicate the contents of CR 1 are not a special character. Lines **71***a*.**15** and **71***a*.**16**, when positive, indicate that the contents of CR 1 to be either a period or a comma. Lines **71***a*.**18** through **71***a*.**20** are positive to indicate that the contents of CR 1 represent a Group Mark and line **71***a*.**17** is the complement of those lines, **71***a*.**18** through **71***a*.**20**.

In FIG. 71*b*, lines **71***b*.**01** through **71***b*.**04** are positive when CR 1 is a numeric character. Alternately, the lines **71***b*.**05** through **71***b*.**09** are up to give an indication when CR 1 is not a numeric character. The line **71***b*.**10** is positive to indicate those instances when CR 1 is not equal to a 4 or 9. The line **71***b*.**11** is positive to indicate that CR 1≠0 or that the instruction is a Set Bit instruction. The line **71***b*.**12**, when positive, indicates CR 1≠0, the line **71***b*.**13** indicates that CR 1≠zero or a comma and CR 1=RM line **71***a*.**14** signifies CR 1 contains a Record Mark.

CODE CHECKING CIRCUITS

Referring now to the Memory Buffer Register Code Check circuits for characters 4, 3, 2 of FIG. 19*a*, signals for the 4, 2 and 1 bits of each character representing binary "ones" or binary "zeros," as the case may be, are fed in various combinations to AND circuits so that if only a single binary "one" is contained in the three bits or if binary "ones" are contained in all three bits, the outputs of one or more of the AND circuits are positive. In an identical manner, signals representing bits B, A and 8 are fed to AND circuits to provide a positive output if an odd number of binary "ones" are contained in the combination of bits of the B, A and 8 positions. The remaining circuits in FIG. 19*a*, are utilized to determine whether an odd or even number of binary "ones" are contained in the total count of bits in Character 4. If the sum of B, A, 8, 4, 2 and 1 bits are even, then the C bit should be zero. Otherwise, the C bit should be a binary "one" to provide a sum of the character bits which is even. If a correct code exists no signal is developed on the line **19***a*.**01** but if an odd number of binary "ones" are contained in a particular seven bits, the Character 4 Code Check Odd line **19***a*.**01** is made positive and this positive signal is utilized to signify an error. Like circuits are provided in FIG. 19*b* to check the redundancy characters 1 and 0.

Similarly, circuits are provided in CR 1 Code Check, FIG. 72, to ascertain that proper redundancy exists in the bits contained in Character Register 1, and CR 2 Code Check Circuits are provided in FIG. 77 for ascertaining that the proper redundancy exists in the character contained in CR 2.

ZONE ADDER

FIG. 79 (2 sheets) discloses circuits comprising the Zone Adder and the Zone True/Complement Controls shown in block form in FIGS. 2*ccc* and 2*fff* respectively.

The Zone T/C Controls for the A bit comprises a pair of AND circuits, FIG. 79 (Sheet 1), one AND circuit having inputs on CR 2–A line **75.09**, CR 2 to T/C line **93***b*.**05** and True line **83.01** and the other having inputs on CR 2–$\overline{A}$ line **75.13**, Complement line **93***d*.**08** and CR 2 to T/C line **93***b*.**05**. The outputs of these AND circuits feed an OR circuit which supplies an output on line **79.16** (A) to the Zone Adder circuits. The Zone T/C Controls for the B bit comprise a pair of AND circuits, FIG. 79 (Sheet 2), one AND circuit having inputs on True line **83.01**, CR 2 to T/C line **93***b*.**05** and CR 2–B line **75.03** and the other having inputs on the CR 2 to T/C line **93***b*.**05**, Complement line **93***d*.**08**, and CR 2–$\overline{B}$ line **75.06**. The outputs of these AND circuits feed an OR circuit which supplies an output on line **79.17** (B). Under control of the Complement and True lines these circuits either complement or pass unaltered the Zone bit inputs of CR 2. The Zone bits of CR 1 are directed to the Zone Adder via Adder Input Switching, FIG. 73.

Complementing of the Zone bits is accomplished by merely revising the state of the bits. For example, if the Zone bits are BA=01, the Complement is BA=10. The output of the A bit position of Character Register 2 causes CR 2–A line **75.09** to be positive for a binary "one" in the A bit position, and although CR 2 to T/C line **93***b*.**05** is positive, the True line **83.01** is down thereby presenting a negative signal to the Zone Adder on the line **79.16** (A) indicative of the complement of the input. The output of the B bit position of CR 2 causes CR 2–$\overline{B}$ line **75.06** to be positive for a binary "one" in the B bit position, and CR 2 to T/C line **93***b*.**05** and Complement line **93***d*.**08** are positive thereby providing a positive signal to the Zone Adder on the line **79.17** (B) indicative of the Complement of the binary "zero" in the B bit position of CR 2.

The Zone Adder comprises two full adder orders, one for the A bit and one for the B bit. The operation of the Adders is identical to those used in the Multiple Adder of FIG. 84 and the Digit Adder of FIG. 86, and no purpose would be served by a detailed explanation. It suffices to say that the Zone Adder receives two sets of inputs, an A bit and B bit from CR 1 and/or an A bit and B bit in True or Complement form from CR 2. If the sum of the Zone bits represented by signals on the input lines generates a binary carry, the Zone Carry Out lines **79.10** through **79.12** are positive. In FIG. 88 (Sheet 1), the line **79.11** and (−) On Suppress Zone Carry In line **93***d*.**02** condition a positive gate (GJ) in FIG. 88 (Sheet 2) for the passage of a pulse on the W_0 (D0.4) Add line **101.11** to turn On the Zone Carry trigger. When the Zone Carry trigger is On, the Zone Carry In line **88.33** provides a binary "one" to the Zone Adder of FIG. 79 (Sheet 1) in the next cycle. A binary "one" can also be added into the Zone Adder via the Zone Carry In line **93***d*.**01** for certain operations such as Add to Memory, Add Address to Memory, and Compare. Outputs on Result A line **79.03** and Result B line **79.07** are sent to the Zone Bit triggers of the Result Register, FIG. 89*b*, and

outputs on Result B line **79.06** and Result A line **79.02** are sent to the C Bit Generator of FIG. 90.

C BIT GENERATOR

As stated previously, the checking system utilized in the Data Processing System is that the number of binary "ones" comprising each character must be even. Thus, as characters are transmitted from one portion of the machine to another, a check is made to ascertain that each character contains an even number of binary "ones." If an odd number of binary "ones" is received to represent a character, the machine may be stopped or an error indicated. It is pointed out, however, that when two digital values are added, subtracted, multiplied or changed in any way that the sum, difference, product or result may not contain an even number of binary "ones." Also, the number of binary "ones" in a particular character may be the result of addition of two digits by the Digit Adder and/or addition by the Zone Adder. Consequently, a Check Bit Generator is provided in order that a new check bit (C) or redundancy bit may be generated as required.

Circuits for generating this check bit (C) are shown in FIG. 90 and also shown are circuits for gating the C bit of either the character in CR 1 or CR 2 to the Result Register of FIG. 89*b*.

The Check Bit Generator receives inputs from the Decimal Adder Correction circuits on the lines **87.13** (8), **87.05** (4), **87.01** (2) and **87.12** (1), the Zone Adder on the lines **79.06** (B) and **79.02** (A), CR 1 on the line **58.01** (C) and CR 2 on the line **48.03** (C). The circuits shown in FIG. 90 consist mainly of two full adders in which only the sum lines are used, one adder which combines the B, A and 8 bits on the lines **79.06** (B), **79.02** (A) and **87.13** (8) respectively, and another which combines the 4, 2 and 1 bits on the lines **87.05** (4), **87.01** (2) and **87.12** (1) respectively. The rules of addition, stated previously, apply, and the two adders determine whether or not the three particular inputs thereto comprise an even sum (indicated by a binary "zero") or an odd sum (indicated by a binary "one"). When the outputs of both adders agree, that is, both outputs are positive or both outputs are negative, the redundancy bit (C) should be negative signifying a binary "zero." When the outputs of the adders are unlike, a binary "one" output or C bit is required. A positive signal on the Generate C Bit Out line **93***c*.**03** gates a binary "one" or positive signal onto the Result C line **90.01** to the Result Register when a C bit is required, and otherwise the Result C line is negative.

At times, it is desired to gate the C bit of the character in either CR 1 or CR 2 to the Result Register. A positive signal on the CR 1–C line **58.01**, indicating a binary "one" in the C bit position of CR 1, conditions one input of an AND circuit and another line CR 1–C Bit Out, when positive, gates the C bit onto the Result C line **90.01**. Similarly, a positive signal on the CR 2–C Bit Out line **93***b*.**06** gates the C bit, if any, from CR 2 onto the Result C Output line. If the C bit position of either CR 1 or CR 2 were negative to represent a binary "zero," then the Result C line would be negative in each case.

The Emit Blank line **93***e*.**05**, when positive, causes the output Result C line **90.01** to go positive in combination with the emission of an A bit from the Zone Adder.

For some instructions, such as Load and Unload, characters that are passed through the adders unchanged also have their C bits transmitted independently to the Result Register via the input line **56***a*.**07** instead of having a C bit generated by the circuits of FIG. 90. Thus, the gaining or dropping of a bit during the transmission of a character through the arithmetic circuits is detected if the original C bit is supplied independently to Result Register when the character (C, B, A, 8, 4, 2, 1 bits assembled in the Result Register) are redundancy checked in the Result Register Code Check circuits of FIG. 91.

RESULT REGISTER

In FIGS. 89*a* and *b*, circuits of the Result Register are illustrated which comprise seven triggers, one for each bit position of a character. The Result Register provides a buffer storage between the arithmetic circuits and Memory or Storage and furnishes signals indicative of a particular character on output busses to the Input Switch of FIG. 11 and the Storage In Selection and Switching circuits of FIG. 43 for writing into Memory or Storage respectively.

The right plate outputs (On sides) of the triggers are inverted so that the Memory/Storage In Bus lines **89***a*.**01**, **89***a*.**02**, **89***a*.**05**, **89***a*.**06**, **89***a*.**09**, **89***a*.**10**, **89***a*.**13**, **89***a*.**14**, **89***b*.**01**, **89***b*.**02**, **89***b*.**05**, **89***b*.**06**, **89***b*.**09** and **89***b*.**10** are positive when their respective triggers are Off indicating binary "zeros." These positive signals are combined with the Inhibit Gate, in the manner described previously with reference to Memory and Storage, to cancel the effect of the Write Gate in those core planes where it is desired to write "zeros" according to the bit configuration of the Result Register. When a Result Register trigger is set to a "one," the positive signal from the right plate is inverted to provide a negative output signal which blocks the Inhibit Gate to that particular core plane where a "one" is to be written.

Pairs of output lines for each trigger representing the state of each trigger and the complement thereof, for example, RR–A line **89***b*.**03** and RR–$\overline{A}$ line **89***b*.**04**, are furnished to the Result Register Code Check circuits of FIG. 93.

Input lines are provided to the Result Register from the Keyboard of FIGS. 22*a*, *b*, and *c*, the Digit Adder Decimal Correction circuits of FIG. 87, the Zone Adder of FIG. 79, the Memory Test Controls of FIG. 92, and the C Bit Generator of FIG. 90.

The triggers of the Result Register are reset Off at W_3 of each cycle during Use time via the lines **139***c*.**01** and **139***a*.**02**. The input data lines are gated at R_2 by the lines **103***a*.**15** and **103***a*.**14** which is late enough to allow time for the input lines from the adders to become stable; however, the triggers are not set until R_4 when the lines **101.18** and **101.17** become positive. It will be noted that the input Result lines by-pass the triggers and may be utilized from R_2 to R_4 before the triggers are set. After the triggers are set at R_4 time, the triggers control the output lines until reset time at W_3 and, since the input Result lines are no longer required after R_4 time, they are blocked by the fall of the R_2–A_0/W_0 lines **103***a*.**15** and **103***a*.**14**. Thus blocked, any changes in the adders due to changing the states of the Carry triggers at W_2 are not reflected in the Result Register outputs. Those triggers which are set to "ones" at R_4 are reset to "zeros" at W_3 time, and those inhibit lines blocked from R_2 to W_3 become positive for the remainder of the Inhibit Gate to furnish Post Write Disturb pulses from W_3 to R_0 as shown in FIG. 144.

OVERLAP MODE CONTROL TRIGGERS

The four triggers, Mode Control, Add, Transition and Auto Transition, shown in FIG. 136*a*, define the type of Overlap Mode Control cycle in which the system is operating and control communications between the Arithmetic and Logical Unit, Memory and Storage.

ADD TRIGGER

The function of the Add Trigger is to define the period of time in which computation may be carried on in the ALU. If the Add trigger is On, then the ALU may generate results; if the Add trigger is Off, then no computation is permitted. Accordingly, the Add trigger provides a gate signal for all of those triggers associated with the ALU, such as the Multiple Carry Triggers, FIGS. 80 and 81, Multiple Carry trigger, FIG. 85, Zone Carry trigger and Decimal Carry trigger, FIG. 88, Inter Register Check trigger, FIG. 63*c*, Low and High triggers, FIG. 138*a*, Ac-

cumulator Digit Zero trigger, Auxiliary Digit Zero trigger and Remainder trigger, FIG. 138*h*, Auxiliary Trigger 1, FIG. 138*i*, and Auxiliary trigger 2, FIG. 138*k*. Under certain conditions, the triggers just enumerated are not permitted to change state unless the Add trigger is On. Another function of this trigger is to control the turning On and Off of the Transition and Automatic Transition triggers.

In FIG. 136*a* the Add trigger is turned On if Block Add trigger is Off causing line **93***v*.**01** to be up and the Transition triggers are Off causing the line **136***d*.**02** to be up thereby conditioning the Diode Gate for the fall of the line **103***b*.**23** at W_1. If either the Transition trigger or Automatic Transition trigger is On, the line **136***c*.**01** is up to condition the associated Diode Gate and the fall of the line **103***b*.**23** at W_1 turns Off the Add trigger. Even when the Transition triggers are Off, the Add trigger is prevented from being turned On in some instances by the line Block Add trigger. Instruction reset is provided from FIG. 139*b*.

TRANSITION TRIGGER

The Transition trigger is used to define Transition cycles caused by recognition of certain conditions depending upon the type of operation being performed in response to a particular instruction and requiring a change in operation. The change required may be a transition from one type of operation to another during different operations caused by the same instructions or it may be a transition out of one operation due to an instruction into another operation brought about by a new instruction. Usually, the end of a sequence of operations is recognized by a special character such as a Storage Mark set in one of the character registers at W_0. The Transition trigger is turned On at W_2 in order that the On condition of this trigger may provide for a Transition cycle in the next cycle. The main features of a Transition cycle are:

(1) Computation ceases at W_1 by turning Off the Add trigger.
(2) CR 1 and CR 2 retain the characters set therein.
(3) SAC is prevented from counting.
(4) Mode Control trigger is turned Off at the end of the Transition cycle.
(5) The Transition trigger is turned Off at the end of the Transition cycle.

It is pointed out that this trigger must be Off to have full overlap operation, and that the trigger cannot be On for two consecutive cycles.

AUTOMATIC TRANSITION TRIGGER

The Automatic Transition Trigger is turned On to define Transition cycles when special conditions are recognized which are independent of the instruction being executed and such cycles constitute delays in processing. Some of these conditions are functions of either the Storage Read/Write Mode or of the Memory Read/Write Mode when MAC 1 or SAC is stepped to a "critical" address to be explained in detail later. Other conditions are those imposed in processing Sign Checks, Instruction Checks and Overflow Checks, but only the last two can be regarded as automatic. When the Auto Transition trigger is On, the same features of a Transition cycle are present as enumerated above and additionally this trigger being On causes the Machine Check trigger to be turned On if there is a Code Check and causes the system to stop operation if the Machine Check switch of FIG. 119 is set to Automatic.

In FIG. 136*a*, the Auto Transition trigger is turned On by positive signals on the Add Trigger On line **136***d*.**15**, Turn On Transition trigger line **93***u*.**01**, and W_2 (D1) line **102**.**17**. The trigger is turned Off by the Add trigger Off line **136***d*.**18** and the W_2 (D1) line **102**.**17**. When On, the trigger provides a positive signal on the Transition line **136***a*.**03** to FIG. 136*c* and line **136***a*.**04** to FIG. 136*d*.

MODE CONTROL TRIGGER

The Mode Control trigger is turned On at the end of a Start cycle when the machine is either in the Memory R/W Mode or the Storage R/W Mode to cause computed results to be placed in Memory or Storage, as the case may be, at the address from which data was obtained during the previous cycle. As shown in FIG. 136*a*, either the Memory Read/Write Mode line **93***q*.**01** or the Storage Read/Write Mode line **93***q*.**05** along with Not Transition line **136***d*.**02** conditions a Diode Gate for the fall of the line **103***b*.**07** to turn On the trigger at W_2. The trigger is turned Off by the Transition line **136***c*.**01** which conditions a Diode Gate for the fall of the line **103***b*.**07** to turn Off the trigger at W_2.

OVERLAP MODE CONTROL TRIGGERS

The following statements apply to the extent that control is exerted among the triggers. The Add trigger cannot be turned On if either the Transition trigger or the Auto Transition trigger is On, but the Add trigger must be turned Off if either of the Transition triggers is On. Neither the Transition trigger nor the Auto Transition trigger can be turned On if the Add trigger is Off, and both must be turned Off if the Add trigger is Off. The Mode Control trigger cannot be turned On if either of the Transition triggers is On and they must be turned Off if either of the Transition triggers is On.

Computation normally begins in the first cycle of the execution of an instruction, and the Add trigger is automatically turned On in this cycle unless the particular operation specifically blocks the trigger from being turned On (Block Add trigger). In most arithmetic operations, a Transition cycle causes termination of the operation, and, thus, the recognition of a Transition cycle causes the Add trigger to be turned Off. The Transition trigger comes On at W_2, causing the Add trigger to be turned Off at the next W_1 time, which, in turn, insures that the Transition trigger will be turned Off at the next W_2 time.

Chart V.—Overlap Mode Control Triggers

Trigger	Function	Turned On		Turned Off By—
		By—	If—	
Add	Defines cycles during which computation takes place.	First cycle of execution of each instruction unless specifically blocked.	Both Transition triggers are Off.	Either Transition trigger being On
Transition	Controls Memory sequence during change in type of operation being performed in ALU.	Recognition by individual instruction of a need to change.	Add trigger is On	Add trigger being Off.
Auto transition	Controls Memory sequence during automatic processing of redundancy checks or special conditions which are functions of the Read/Write modes.	Recognition of redundancy check or special conditions of the Read/Write modes.	Add trigger is On	Add trigger being Off.
Mode control	Defines those cycles in which results are placed into Memory or Storage at the address read from in the previous cycle.	First cycle of either the Storage or Memory Read/Write Mode.	Both Transition triggers are Off.	Either Transition trigger being On.

CONDITIONS FOR OVERLAPPING

The conditions may now be set forth under which computing is done at an effective rate of 9 microseconds per character, or more specifically, when the computation is fully overlapped with Reading and Writing of Memory or Storage. If during a Memory cycle from R_0 to R_5, the Add trigger is On for the entire cycle and if, in addition, Memory or Storage cores are being driven and a switching path has been established to the arithmetic circuits, then the operation is said to be fully overlapped. If the Add trigger is Off for all of a Memory cycle, that cycle will be a non-arithmetic cycle. A Memory cycle during which the Add trigger is turned On is defined as a Start cycle and a Memory cycle during which the Add trigger is turned Off is called a Transition cycle, as previously mentioned. The last cycle of an execution sequence must be either a Transition cycle or a non-arithmetic cycle.

OPERATION IN THE OVERLAP MODE

Many of the arithmetic operations performed by the Data Processing System place results in Storage, which results are derived from data taken from both Memory and Storage. Examples of these instructions are found in Chart II, for example, Add and Subtract. In this type of operation, it is only necessary to extract data from Memory character by character, provide each in turn to the arithmetic circuits, and return each character unmodified from the MBR to the same address in Memory. Returning an unmodified character to Memory is accomplished during the Write portion of the cycle during which the character was extracted from Memory since a result of computation is not being entered in Memory. Thus, the Memory Read Mode is employed. Computation with a pair of characters, one from Memory and one from Storage, takes place during the Write portion of the cycle in which the characters were read and during the Read portion of the succeeding cycle. The result of this computation is then placed in Storage during the Write portion of the succeeding cycle at the address read from the previous cycle. To read data from Storage and place a result (derived in part from the data) in Storage at the same address requires that the Storage Read/Write Mode be used. Chart VI illustrates Memory and Storage operations for arithmetic instructions such as Add and Subtract, where subscripts denote relative addresses in Memory and Storage, R is for Read, W is for Write and C is for Compute.

Chart VI

MEMORY AND STORAGE OPERATIONS

	Start		Overlap		Overlap		Overlap		Transition	
Memory	R_{x1}	W_{x1}	R_{x2}	W_{x2}	R_{x3}	W_{x3}	R_{x4}	W_{x4}	--	--
Storage	R_{y1}	--	R_{y2}	W_{xy1}	R_{y3}	W_{xy2}	R_{y4}	W_{xy3}	--	W_{xy4}
		C_{xy1}		C_{xy2}		C_{xy3}		C_{xy4}		

A pair of characters are read from address 1 in Memory and Storage and computation takes place while the character read from Memory is returned to its previous address (address 1) and a second pair of characters are read from address 2. Upon completion of the computation, the result is written into Storage at address 1 while computation begins on data read from address 2. Calculations involving data from address 2 continue through the time taken to read characters from address 3 and then the result of the calculation just completed is stored at address 2 in Storage. The operation continues in like manner until the end of the operation is anticipated when a Transition cycle occurs. Reading from and Writing into Memory is not required during the Transition cycle since the final character was handled during the last fully Overlapped cycle. Reading from Storage is not required during the Transition cycle, but Writing must be accomplished to store the results of computation completed during the Transition cycle at address *xy*4.

As mentioned above, other instructions available in the Data Processing System place new results in Memory while using Storage and Memory for interrogation. An instruction of this type is Add to Memory. The diagram above applies to this type of operation simply by interchanging the words Memory and Storage. Other instructions, such as Load and Store, use both Memory and Storage only for extracting information, while still others make no reference at all to either Memory or Storage, such as Lengthen, Shorten, Read While Writing, Transfer and so forth. Thus, it is necessary to provide several Modes of Operation for all of the types of operations mentioned above. Accordingly, the four Modes mentioned previously, namely, Memory Read Mode, Storage Read Mode, Storage Read/Write Mode and Memory Read/Write Mode are provided for those situations where Memory, Storage, or Memory and Storage are utilized in the operations.

Instructions, such as Add that require use of data from both Memory and Storage and place the results of the processing in Storage, use both the Memory Read Mode and the Storage Read/Write Mode. An instruction, such as the Store instruction, which places data from Storage in Memory, uses the Memory Read/Write Mode and the Storage Read Mode. An instruction, such as Compare, only extracts information from the Memory and Storage fields; therefore, the Memory Read Mode and Storage Read Mode are used. Many of the instructions do not use Memory or Storage and, therefore, do not use any of the four modes. Thus, recognition of individual instructions causes the machine to enter various combinations of modes which then take over the control of the Memory, Storage and Arithmetic operations.

Comparison of operation in the non-arithmetic mode and operation in the Overlap mode is best understood with reference to the Sequence Chart of FIG. 146. The upper portion of the Sequence Chart illustrates a typical operation in the non-arithmetic mode such as the one described previously by example utilizing an assumed address in Storage. Let the address contained in SAC now be 0. In the non-arithmetic mode, it will be noted that during the Read portion of the first cycle a character is read from Storage and on the Write portion of the cycle the same character or another character from the Result Register is returned to address 0. Similarly, in all of the cycles which follow, a character is read from a succeeding address and is either returned thereto or a character in the Result Register is returned to that address during the same cycle. Referring now to the Read/Write Mode Sequence Chart of FIG. 146, lower portion, for the purposes of comparison, a character is read during the first cycle from an address 0. During the Read portion of the second cycle, the contents of address 1 are read; and during the latter portion of the second cycle (the Write portion), the contents of the Result Register are read into address 0. This result was computed during the Write portion of the first cycle and the Read portion of the second cycle. The Read and Write addresses are shown in the two bottom rows of the lower portion and indicate during the first cycle that the Read address is 0, whereas the Write address is blank. During the second cycle the Read address is 1 and the Write address is 0. This scheme of addressing continues until the last cycle when Read current is not provided to Storage since the last character to be processed was read during the previous cycle. However, Write current is provided to write into address 5 the result of computation, which result was derived during the Write portion of the next-to-the-last cycle and the Read portion of the last cycle. It will will be recognized from what has been previously said that the first cycle is a Start cycle, that the last cycle is a Transition cycle, and that the intervening cycles are all Fully Overlapped cycles.

Before proceeding with a description of the specific circuits for providing these modes of operation which cause

operation of the address controls, each of the Modes will be discussed.

MEMORY READ MODE

In FIG. 93*a*, the control line that causes information to be read from Memory and makes it available for computation in the ALU is designated Read Memory line **93***a*.**05**. This line is up during the Memory Read Mode as long as both Transition triggers are Off. In order that the same information read from Memory also be returned to Memory, it is not necessary to energize any other control lines; because whenever the Result to Memory line **137.01** is not up the information read from Memory is automatically returned to the same address in any given cycle.

The addresses read from in Memory are normally governed by the Memory Address Counter 1 (MAC 1) which is initially set to the address of the instruction and data may be read from Memory addresses in ascending or descending order in successive cycles by stepping MAC 1 up one step or down one step each cycle. It is necessary that the signal on the Step MAC 1 control lines of FIG. 93*g* be governed by the individual instruction due to the direction of stepping required for the instruction. During an Auto Transition or a Transition cycle, MAC 1 should not be stepped as Memory is not interrogated this cycle and allowing the stepping of MAC 1 during one or the other of the Transition cycles would cause the omission of reading one Memory character during the sequence. Thus, in FIG. 136*b*, signals on the Memory Read Mode line **93***q*.**01** and Transition line **136***c*.**02**, brought up by either Transition trigger being On, cause the stepping of MAC 1 in either direction to be blocked. The operation just described is summarized in the Memory Read Mode Flow Diagram of FIG. 147*a* where it is shown that in the absence of recognizing the need for a Transition cycle, Read Memory is continued until there is a need for a Transition cycle. Thereafter, stepping of MAC 1 is prohibited for one cycle, since two successive Transition cycles cannot occur, as previously mentioned.

Referring now to FIG. 136*b*, Memory Read Mode line **93***q*.**01** is up and the Not Transition line **136***d*.**03** is up to furnish a positive signal on the Read Memory line **136***b*.**02**. The latter line goes to Read Memory Routing of FIG. 93*a* where it is combined with various routing lines and the Use line **105.14** to bring up the Read Memory lines **93***a*.**03** and **93***a*.**04** to FIGS. 100 and 135*b* respectively. The Read Memory I line **93***a*.**05** is also brought up under those conditions when the MASR address is below 40,000 to indicate Memory 1 is to be used. The line **93***a*.**03** goes to a Pulse Generator, FIG. 100, to set CR 1 at W_0 time of an execute cycle, or at A_0 time of an Instruction cycle. The line **93***a*.**04** goes to the Parallel Character Transmission Request Execution controls, FIG. 135*b*, where it is gated with the PCT Request to establish control for break-in by Input/Output devices. If a Transition cycle occurs, then MAC 1 is prevented from stepping by the Minus On Block Step MAC 1 line **136***b*.**01** which is made positive by the Transition line **136***c*.**02**.

The Sequence Chart of FIG. 147*b* illustrates how the Memory Read Mode would be used in a typical operation. Assume MAC 1 starts at an address ending in 4 and is stepped down. The first Execute cycle from R_0 to R_0 is a Start cycle. The Memory Read Mode line **93***q*.**01** comes up at W_2 of the previous cycle and Minus On Block Step MAC 1 line **136***b*.**01** is up since the Transition line **136***c*.**02** is down. Both lines remain up through the W_2 of the Transition cycle. Due to the Memory Read Mode line **93***q*.**01** and the Not Transition line **136***d*.**03**, the Read Memory line **136***b*.**02** goes positive at W_2 as shown in the sequence chart. The Read Memory line **136***b*.**02** in combination with Use line **105.14** in FIG. 93*a* brings up the Read Memory line **93***a*.**03** at W_2 to set CR 1 at W_0. The Minus On Block Step MAC 1 is shown as being up from the beginning of time in the chart, FIG. 147*b*, since in FIG. 136*b* the Transition line **136***c*.**02** and the Memory R/W Mode line **93***q*.**03** are down. The add trigger of FIG. 136*a* is turned On at W_1 by the Not Transition line **136***d*.**02**, the Minus On Block Add trigger line **93***v*.**01** and the A_2/R_3–W_1 line **103***b*.**23**.

The first character of the field is read out of Memory and placed in CR 1 at W_0, and then the character is returned to Memory unaltered since the Result to Memory line **136***b*.**03** is down due, in turn, to the Mode Control trigger On line **136***e*.**34** being down. The Mode Control trigger is not On during a Memory Read Mode operation (see FIG. 136*a*) since the Memory Read/Write Mode line **93***q*.**01** remains down. Subsequent cycles are Overlap cycles with MAC 1 stepping down one each cycle at R_3 time and MASR retaining the previous address of MAC 1 until R_0 so that the result of computation is entered at the proper address. Overlap cycles continue until a condition is recognized which causes the Transition trigger of FIG. 136*a* to go On by virtue of Turn On Transition trigger line **93***m*.**04**, Add Trigger On line **136***d*.**15** and W_2 (D1) line **102.17**. The machine now enters a Transition cycle due to some condition which requires a termination of the Overlap cycle routine. During the Transition cycle, the Add trigger is turned Off at W_1, and then at W_2 the Transition trigger is turned Off via Add Trigger Off line **136***d*.**18** and the W_2 (D1) line **102.17**. The Minus On Block Step MAC 1 line **136***b*.**01** is down from W_2 to W_2 of this cycle to prevent stepping MAC which would cause an address to be skipped should it remain up. In FIG. 93*q*, the fall of Minus On Block Step MAC 1–1 line **136***b*.**01** brings down Step MAC 1–1 lines **93***g*.**04**–**93***g*.**09**. As shown in the Sequence Chart of FIG. 147*b* and in FIG. 136*b*, the Not Transition line **136***d*.**03** brings down the Read Memory line **136***b*.**02** since data from Memory is not extracted during a Memory Read Mode Transition cycle.

STORAGE READ MODE

Generally, this mode is identical to that of the Memory Read Mode. Specifically, the controls for Reading from and Writing into Storage are necessarily different because Storage operates serial by character instead of in parallel by five character groups as Memory does.

The two control lines affected in this instance are the Read Storage line **136***b*.**10** and the Minus On Block Step SAC line **136***b*.**09**. The Read Storage line is made positive by the coincidence of signals on Storage Read Mode line **93***q*.**04** and Not Transition line **136***d*.**03**, the latter line being up if both Transition triggers are Off. The Minus On Block Step SAC line **136***b*.**09** is down when the Storage Read Mode line **93***q*.**04** and the Transition line **136***c*.**02** are up, the latter line being up when a one or both of the Transition triggers are On.

The operation is summarized in the Storage Read Mode Flow Diagram of FIG. 148 where it is shown that in the absence of recognizing the need for a Transition cycle, Read Storage is continued until there is a need for a Transition cycle. Thereafter, a Transition cycle is initiated during which stepping of SAC is prevented to avoid skipping an address.

MEMORY READ/WRITE MODE

A critical address will now be defined generally as an address which requires a Transition cycle (Automatic Transition trigger On) to adjust the operation for some condition imposed by the addressing structure of a device which stores information. More specifically and with particular reference to Memory, if MAC 1 is stepping down (minus) and refers to character 0 (MAC 1 ends in a 0 or 5), this is a critical address for Memory since there is no character in MBR to the left of zero and another group of five characters must be brought from Memory for new data, but the result of computations with character 0 must be returned to the same address. If MAC 1 is stepping up (plus), critical addresses are those referring to character 4 (MAC 1 ends in a 4 or a

9), since there is not a character to the right in the MBR. In both instances, the following cycle cannot be an Overlap cycle but must be a Transition cycle which, in effect, is a one cycle delay introduced upon recognition of a crtical address.

In all other modes of operation involving Memory, except the Memory Read/Write Mode, the character sent to the ALU is that character located at the address contained in the MASR, but in Memory R/W Mode where it is necessary to read from one address and write into another address in the same cycle, the stepping of MAC 1 is suppressed in the Start cycle and the MASR contains the address of the result being placed in Memory. If MAC 1 is stepping up (plus) this means that during Fully Overlapped cycles, the address of the character sent to ALU must be one higher than that contained in the MASR. Decoding of the Memory R/W Mode line **93***q*.**03**, Mode Control trigger On line **136***e*.**34**, and Step MAC 1+1 line **93***g*.**01** brings up the High Character line **136***b*.**06**, which line causes the character that is one position higher than the address contained in the MASR to be sent to the ALU for processing and prevents the character at the address contained in the MASR from being transmitted to the ALU.

If MAC 1 is stepping down (minus), then during Overlap cycles, the address of the character sent to ALU must be one lower than that contained in the MASR. The Memory R/W Mode line **93***q*.**03**, the Mode Control trigger On line **136***e*.**34**, and the Step MAC 1–1 line **93***g*.**04** are combined to furnish a positive signal on the Low Character line **136***b*.**04**, the latter causing the character that is one position lower than the address of the MASR to be sent to the ALU for processing and prevents the character at the address contained in MASR from being transmitted to the ALU.

During the Transition cycle, the result of computation is placed in the Memory location specified by the address in MASR, which address is the Critical Address and the one from which data was taken for the computed result.

The sequence of operation is shown in the Memory Read/Write Mode Flow Diagram of FIG. 149*a* which begins and ends at W_2 time. Starting at 1, the Read Memory action is indicated initially. If the instruction calls for an operation where MAC 1 is stepping down on each Execute cycle, then it must be determined if MAC 1 units position stands at 0 or 5 (A Critical Address). If a Critical Address is not detected, and a Transition cycle is not required due to the operation imposed by the particular instruction being executed, then the Mode Control trigger is turned On. When the Mode Control trigger is On, then the Result to Memory action is initiated. As stated above, MAC 1 was being stepped down, so the Low Character condition is required to gate the next character of the ALU for processing. The sequence of operation begins again in like manner. Assuming that MAC 1 ends in a 0 or 5, the Auto Transition trigger is turned On to call for a Transition cycle which specifies that the Mode Control trigger shall be turned Off for the cycle following the Transition cycle. Remaining in the Transition cycle with the Mode Control trigger On, Result to Memory action is specified which provides for transmission to Core Memory of the result computed during the Write portion of the last Overlap cycle and the Read portion of the Transition cycle. Step MAC 1–1 condition remains and the Low Character condition remains although it is of no effect. Starting at the top of the Flow Chart, FIG. 149*a*, once again for a Start cycle, which follows the Transition cycle if Read Memory condition still exists and brings out another five character group from Memory, MAC 1 is still stepped down but no longer contains a Critical Address. The cycle is not a Transition cycle so the Mode Control trigger must be turned On near the end of the Start cycle. With the Mode Control trigger still Off, Minus On Block Stepping MAC 1 is down to prevent stepping of MAC 1 during the Start cycle which would cause skipping of an address. Overlap cycles occur as described previously. If the Transition trigger is turned On, then the operation proceeds via the Yes path from the Transition block.

Stepping of MAC 1 up (plus) will not be discussed with reference to the Flow Chart since the operation is evident from the chart and what has been said previously.

Referring now to the Memory Read/Write Mode Sequence Chart of FIG. 149*b*, a hypothetical situation is given for ten cycles during which there occurs two Start cycles (1 and 7), two Transition cycles (6 and 10) and a number of intervening Overlap cycles. The lower portion of the chart shows the contents of the units position of both MASR and MAC 1, the address units position only from which the character in CR 1 was taken, the units address of the character read from Memory and MBR during a cycle and placed on the input to CR 1, the units position address of the character written from the Result Register via the MBR during a cycle, the units position address of the computed character which is formed from a character associated with the same address. MAC 1 starts at an address ending in 4 and steps downwardly (minus). At the top of the chart certain of the cycle points are shown, and it will be recognized that a Memory cycle (Read and Write portions in that order) begins at R_0 and ends at R_0. An Arithmetic cycle (ALU machine cycle) occurs approximately from W_0 to W_0 which is the Write portion of one cycle and the Read portion of a succeeding cycle. For the purposes of this explanation, cycles will be defined as the time between successive R_0 point.s

Referring generally to the Sequence Chart and specifically to FIG. 93*q*, the Memory R/W Mode is specified by decoding those instructions where such a mode is applicable, such as Unload Adress, Store, Add to Memory, Add Address to Memory, and so forth. In this instance the instruction is one which keeps the Memory R/W Mode line **93***q*.**03** positive from W_2 of cycle 1 to W_2 of the cycle following cycle 10. In FIG. 136*a*, all of the Overlap Control triggers are Off at the beginning of a Start cycle. In FIG. 136*b*, the Read Memory line **136***b*.**02** is up due to Memory Read/Write Mode line **93***q*.**03** previously mentioned. As shown in FIG. 149*b*, the line **136***b*.**02** remains up until W_2 of cycle 10. A pulse on the Set CR 1 at W_0 line **100**.**02** occurs at W_2 before the first Start cycle and occurs periodically for a number of cycles until it is desired to block the setting of CR 1 during the first Transition cycle. Because the Mode Control trigger is Off and the line **136***e*.**36** is up, the Minus On Block Step MAC 1 line **136***b*.**01** is down via the inverter of FIG. 136*b*. The Step MAC 1–1 line **93***g*.**10** is up from W_2 before the Start cycle until W_2 of cycle 10 because the particular instruction for this sequence of operations requires stepping MAC 1 in the negative direction. In FIG. 136*a*, the Not Transition line **136***d*.**02** is up and the Minus On Block Add trigger line **93***v*.**01** is up conditioning a diode gate for the fall of the A_2/R_3–W_1 (Blocked) line **103***b*.**23** which turns On the Add trigger at W_1. Attention is now directed especially to the Start cycle of the Sequence Chart of FIG. 149*b* where the conditions of the lines are indicated in the upper portion and the operations are summarized in the lower portion. A character having a units position address of 4 is read, but a result has not been computed and connt be written into Memory. For this reason, Result to Memory line **136***b*.**03** is down and remains so until the Mode Control trigger is turned On. At W_1 of the Start cycle (cycle 1), the Add trigger is shown turned On as a result of the Not Transition line **136***b*.**02** and Minus On Block Add trigger line **93***v*.**01** combined with the fall of the A_2/R_3–W_1 line **103***b*.**23** as described with reference to FIG. 136*a*. The Add trigger provides an arithmetic cycle from R_0 to R_0 in keeping with the definition that an arithmetic cycle is one in which the Add trigger is On for at least a portion of the cycle.

At W_2 of the Start cycle, the Mode Control trigger is turned On by the Memory R/W Mode line **93***q*.**01** and the fall of the A_3/R_4–W_2 line **103***b*.**07** thereby defining cycles in which results of computation are placed in Memory at the address read from in the previous cycle. Accordingly, this trigger being On brings up the Mode Control trigger On line **136***a*.**08** as indicated in the Sequence Chart of Memory R/W Mode, FIG. 149*b*, and the powered line **136***c*.**34** in combination with Memory R/W Mode line **93***q*.**03** makes positive the Result to Memory line **136***b*.**03** in FIG. 136*b*. Because MAC 1 is stepping down to the operation and the units position of MASR contains a 4, it is necessary to bring up the Low Character line **136***b*.**04** so that the character having a units position address of 3 is brought into ALU for processing during the Read portion of cycle 2 (first Fully Overlapped cycle). In FIG. 136*b*, the Mode Control trigger On line **136***e*.**34**, Memory R/W Mode line **93***q*.**03** along with Step MAC 1–1 line **93***g*.**04** makes the Low Character line positive at approximately W_2 in time to condition Memory Out circuits of FIG. 20*a* to gate character 3 during the Read portion of cycle 2.

Stepping of MAC 1 was suppressed during the Start cycle and upon entry into the Fully Overlapped cycle sequence it becomes necessary to step MAC 1 down one count for each Fully Overlapped cycle. In FIG. 136*b*, the Mode Control trigger Off line **136***e*.**36** goes negative when the Mode Control trigger is turned On at W_2 and as a result the Minus On Block Step MAC 1 line **136***b*.**01** goes positive as shown in the Sequence Chart of FIG. 149*b*.

Operations proceed from left to right in the Memory R/W Mode Sequence Chart for four cycles (cycles 2 through 5) in which Memory and ALU operations are fully overlapped. During cycle 5 a Critical Address is recognized in that the units position of MAC 1 is "0." In FIG. 30*g*, MAC 1–$\overline{1}$ line **30***a*.**12**, MAC 1–$\overline{2}$ line **30***a*.**09**, MAC 1–$\overline{4}$ line **30***a*.**06** and MAC 1–$\overline{8}$ line **30***a*.**02** are combined to indicate MAC 1 ends in 0/5 by a positive signal on lines **30***g*.**01** and **30***g*.**02**. In FIG. 136*b* the line **30***g*.**01** is combined with Memory R/W Mode line **93***q*.**03** and Step MAC 1–1 line **93***g*.**10** to bring up the Turn On Auto Transition trigger line **136***b*.**05**. The latter line passes through FIG. 93*u* and leaves as line **93***u*.**01** for entry in FIG. 136*a*. As stated previously, the Auto Transition trigger cannot be turned On unless the Add trigger is On; accordingly, in FIG. 136*a*, the combination of Add trigger On line **136***d*.**15**, W_2 (D1) line **102.17** and line **93***u*.**01** turn On the Auto Transition trigger with a positive pulse at W_2. In the Sequence Chart it will be realized that while the Turn On Auto Transition trigger line **136***b*.**05** is up, the trigger is not turned On until W_2, as indicated by Transition lines **136***a*.**03** and **04**. Inspecting the lower portion of the sequence chart, it will be observed that in cycle 6, no character is read into the ALU because each of the five characters has either been processed or is being processed. In the case of character 0, it is involved in the computation which ends in the Read portion of cycle 6, and it is during the Write portion of this cycle that the computed character is written into the address having a units position of zero. Even though the low character line **136***b*.**04** remains up until W_2 of the Transition cycle, the low character in the MBR (character 0) is not set into CR 1 since the Set CR 1 at W_0 line **100.02** provides no pulse, as shown. In FIG. 100 the Not Transition line **136***d*.**01** is down and the pulse is not applied to the positive Diode Gates of CR 1, FIG. 57.

Result to Memory line **136***b*.**03** remains up during the Transition cycle so that the computed result from the Result Register is entered in the address having a units position value of "zero."

It will be recalled that the Add trigger is turned Off when either the Transition or Auto Transition trigger is On. Therefore, in FIG. 136*a*, the Transition line **136***c*.**01** conditions the Diode Gate for the fall of the A_2/R_3–W_1 line **103***b*.**23** which turns Off the Add trigger at W_1. The Off condition of the Add trigger defines the next cycle as one in which computation does not take place. The cycle is an arithmetic cycle nevertheless. Since MAC 1 steps to an address having a units value of 9 at W_1, the Turn On Transition trigger line **136***b*.**05** is down.

In the assumed operation, the Instruction has specified use of a number of addresses which include a Critical Address. Thus, when the Transition cycle routine mentioned above is over, the machine proceeds with the execution of the Instruction by taking a Start cycle for entry into a Fully Overlapped condition thereafter.

With the Add trigger Off, the line **136***d*.**18** in FIG. **136***a* is up and at W_2 the line **102.17** comes up to turn the Auto Transition trigger Off thereby causing the Transition lines **136***a*.**03** and **136***a*.**04** to come down. During cycles 2 through 6 the Mode Control trigger has been On but during cycle 6 (Transition cycle) the Transition line **136***c*.**01** is up to condition its Diode Gate (DG) and the fall of the A_3/R_4–W_2 line **103***b*.**07** turns the Mode Control Trigger Off to define a cycle (Start cycle) where results of computation are not placed in Memory. Accordingly, the Mode Control trigger On line **136***a*.**08** falls and brings down the Result to Memory line **136***b*.**03** and the Low Character line **136***b*.**04**. The Mode Control trigger Off line **136***e*.**36** rises and brings down the Minus On Block Step MAC 1 line **136***b*.**01** to prevent stepping MAC 1 during the Start cycle. During cycle 7 (Start cycle), the character having a units position address of 9 is Read from Memory into CR 1 via MBR, but a result character is not Written into Memory since one is not then available. The rise of the Not Transition line **136***d*.**01** provides for setting this character into CR 1 via line **100.02**. During the Write portion of this Start cycle, computation begins with the character just read so at W_1 the Add trigger is turned On by the Not Transition line **136***d*.**02**, Minus On Block Add trigger line **93***v*.**01** and A_2/R_3–W_1 line **103***b*.**23**. Since a result will be available at the end of Read time of the 8th cycle, the Mode Control trigger is turned On via the Memory R/W Mode line **93***q*.**01**, Not Transition line **136***d*.**02** and A_3/R_4–W_2 line **103***b*.**07** at W_2. At about the same time, the Result to Memory line **136***b*.**03** and Low Character line **136***b*.**04** are positive due to Mode Control trigger On line **136***e*.**34** becoming positive. The Minus On Block Step MAC 1 line **136***b*.**01** goes positive at approximately W_2 as the Mode Control trigger Off line **136***e*.**36** goes negative.

Once again Memory and ALU operations are completely overlapped, and Overlap cycles continue as shown in the Chart of FIG. 149*b*. At W_0 of cycle 9, some condition is recognized which depends upon the operation being performed due to the particular instruction, such as the Memory field, in which case the Turn On Transition trigger line **93***m*.**04** is positive, the Add trigger On line **136***d*.**15** is positive and upon the occurrence of a pulse on the W_2 (D1) line **102.17**, the Transition trigger is turned On at W_2 to control the Memory sequence during change in operation from the Fully Overlapped condition. Thus, lines **136***a*.**03** and **136***a*.**04** are up. Since a character is not to be transferred into the ALU during the Read portion of the Transition cycle, the pulse on the Set CR 1 line **100.02** in inhibited at W_2 by the fall of the Not Transition line **136***d*.**01**. Next, the Add trigger is turned Off (computation ceases after the Read portion of the Transition cycle) by the Transition line **136***c*.**01** and the A_2/R_3–W_1 line **103***b*.**23** in FIG. 136*a*. The Memory Read/Write Mode line **93***q*.**03** comes down at W_2 of the Transition cycle (cycle 10) under control of the Instruction to end the overall sequence of operations. The Transition trigger is turned Off by the Add trigger Off line **136***d*.**18** and W_2 (D1) line **102.17**. The Mode Control trigger is turned Off by the A_3/R_4–W_2 line **103***b*.**07** and Transition line **136***c*.**01**, and the Read Memory line **136***b*.**02** goes down due to Memory R/W Mode line

93*q*.03. The Result to Memory line 136*b*.03 and Low Character line 136*b*.04 go down due to the drop of Mode Control trigger On line 136*e*.34 and Memory R/W Mode line 93*q*.03. The Step MAC 1–1 line 93*g*.10 drops due to the instruction routing controls, and the Add trigger Off line 136*d*.18 and W_2 (D1) line 102.17 cooperate to turn Off the Transition trigger. Cycle 11 is an Instruction cycle and the execution sequence has ended with cycle 10.

STORAGE READ/WRITE MODE

Previously, a Critical Address was defined generally as an address which requires a Transition cycle (Automatic Transition trigger On) to adjust operations for some condition imposed by the addressing structure of a device which stores information. The Critical Addresses of Storage are different from those described for Memory because of the apparatus employed in the operation of Storage, but before specifically pointing out these Critical Addresses and the reason therefor, the similarities and differences between the Storage Read/Write Mode and Memory Read/Write Mode will be discussed.

In both Modes adjacent addresses are Read from and Written into during the same Fully Overlapped cycle; the Add, Auto Transition, Transition and Mode Control triggers are employed in precisely the same manner and for like purpose; and the sequence of Start, Overlap and Transition cycles is identical. Broadly, the description given heretofore with reference to Memory applies with equal facility to Storage. The differences arise in the addressing controls of Storage and in the arrangement of core planes whereby seven bits (a single character) are read from and written into Storage in the same cycle. By way of review, in the Read portion of a non-arithmetic or Storage Read Mode cycle, a Y Switch Core, FIG. 39, selected by decoding the output of the SASR is changed from the reset state to the set state and the switching of this core causes a half-select output from its secondary winding to pass through one row of cores in each plane of the Storage Array of FIG. 45. Similarly, the half-selected output pulse from a switch core of the X Switch Core Matrix, FIG. 40, passes through a row of cores in each plane at right angles to the row linked by the selected Y Core output. Thus, coincidence occurs only in one core in each of the seven core planes comprising the Storage Array of FIG. 45 thereby causing one character to be read from the Array into the Storage Buffer Register of FIG. 47 via the Sense Amplifiers of FIG. 46. Because the address read from in a non-arithmetic or Storage Read Mode cycle is normally written into during the same cycle, the two switch cores changed to the set state are caused to be reset in the Write portion of the same cycle whereby the same character is returned to the Storage Address read from in that cycle.

The Y Matrix, FIG. 39, is used to designate a particular block of thirty-two addresses of the total of 512 addresses in the Storage Array and, accordingly, the Y Matrix contains sixteen switch cores. The X Matrix, FIG. 40, designates which one of the thrity-two addresses of the block mentioned above will be interrogated. Since this is the case, the Storage Read/Write Mode operation is accomplished by altering the Read and Write pulse arrangement of the X Matrix since it is the X Matrix which controls the reading from and writing into adjacent addresses.

Referring now to FIG. 40, it is pointed out that the Matrix comprises two logically independent 4×4 switch core sub-matrices, the top one being for odd values of 1, 3, 5 and 7, etc., and the bottom one for even values of 0, 2, 4 and 6, etc. This logical division between odd and even addresses permits a single core in each of the sub-matrices to be utilized during the same cycle in the following manner.

During a Start cycle in the Storage R/W Mode, set one of the switch cores, say the core 21 in the Odd Matrix of FIG. 40, in the Read portion of this cycle and suppress the Write pulse to core 21. During the following cycle (an Overlap cycle), read from switch core 22 and apply the Write pulse to the switch core remaining in the set state from the previous cycle, core 21. This resets one switch core (core 21), but leaves another (core 22) in the set state until the following cycle. Therefore, reading from one address and writing into an adjacent address in the same cycle is accomplished. During a Transition cycle, the Read pulse to the next higher switch core is suppressed and the Write pulse is applied to the core set in the previous cycle to reset the core and write into the lower adjacent address. This leaves all switch cores reset at the end of a Transition cycle.

As mentioned earlier, Critical Addresses are present in the Storage R/W Mode and arise because if an attempt is made to Write into address 31 in one block of thirty-two addresses and to Read from address 0 in the next block of thirty-two addresses in the same cycle, it would become necessary to furnish Read and Write pulses to two different switch cores in the Y Switch Core Matrix of FIG. 39 in the same cycle. The result is best illustrated by example. Assume first and second Fully Overlapped cycles in which address 31 was Read from during the first cycle and accordingly core 31 of FIG. 40 remains set during the Read portion of the second cycle. During the first cycle, the 0 core of the Y Switch Core Matrix of FIG. 39 has been set and reset in the usual manner. The SASR goes to address 32 to read out of address 32 during the Read portion of the second cycle by setting core 32 of FIG. 39 and core 0 of FIG. 40 which is accomplished without difficulty and as expected. However, during the Write portion of the second cycle, core 32 of FIG. 39 is reset and core 31 (still set) is reset causing the result to be written into address 63 instead of 31. It is now apparent that whenever a one of the Storage addresses 00, 32, 64, 96, 128 . . . 480 is recognized as being the next address to be interrogated that there must be a Transition cycle for the reason stated above, and, therefore, these addresses are the Critical Addresses for the Storage R/W Mode.

It will be apparent now that during the Transition cycle caused by recognition of a Critical Address, the setting of SASR 32, 64 and 128 triggers to the contents of SAC positions 32, 64 and 128 must be suppressed so that the proper block of thirty-two addresses is used. Referring back to FIG. 39 and the previous example, the core 0 must be set and reset during the Transition cycle to provide address 31, and the core 32 must not be set and reset from SAC until the next cycle. The address 31 receives only a half-select Read current due to switching of core 0 (FIG. 39), but receives a full Write current because of resetting Core 0 (FIG. 39) and core 31 (FIG. 40).

Referring now to the Storage Read/Write Mode Flow Chart of FIG. 150*a*, Read Storage and Result to Storage actions prevail throughout the Storage Read/Write Mode. If SAC is not a Critical Address and a Transition condition due to the type of operation does not exist, then the Mode Control trigger is turned On and SAC is stepped +1. (All Overlap operations using this Mode pertain to instructions wherein SAC is stepped up.) The Mode Control trigger is not turned On until W_2 of the Start cycle so the Off side of the Mode Control trigger block prescribes that Storage is interrogated at the address contained in the SASR, but the Write Gate to the Storage X Switch Core Array is suppressed. Returning to the top of the diagram for the first Overlap cycle and assuming no Critical Address and no Transition condition, the Mode Control trigger is now On and the No side of the second Transition block signifies that Storage is read at the address contained in SASR but in the same cycle an address one less than the address contained in the SASR is written into. Overlap cycles may continue as described, but when a Critical Address is detected, the Auto Transition trigger is turned On causing a Transition cycle. Going

off the Yes side of the first Transition block, the Mode Control trigger is to be turned Off at W_2 of the Transition cycle, but the setting of SASR triggers 32, 64 and 128 from SAC is suppressed immediately. The Mode Control trigger is still On and a Transition condition exists; therefore, the Read Gate to the Storage X Switch Core Matrix is suppressed, but the Storage address one less than the address in SASR is written into.

The next cycle is a Start cycle. Since SAC is no longer at a Critical Address and a Transition condition does not exist, the Mode Control trigger is to be turned On at W_2 of the Start cycle and SAC is to be stepped +1 at R_3 time. The Mode Control trigger is Off during the Start cycle, so Storage is Read at the address specified by SASR but the Write Gate to the X Switch Core Matrix is suppressed. Overlap cycles begin and continue as described above. When a condition due to the operation called for by the Instruction exists, a Transition cycle is taken in the manner described with reference to recognizing a Critical Address except that the Auto Transition trigger is not turned On. Instead, it is the Transition trigger which is turned On, causing a Transition cycle, which controls the procedure whereby the operation is completed and another begins in response to a new instruction.

In FIG. 136*b*, the Read Storage line **136***b*.**10** and the Result to Storage line **136***b*.**11** are positive throughout the Storage Read/Write Mode because these two lines are directly connected to Storage Read/Write Mode line **93***q*.**06**. As stated previously, a Memory or Storage cycle is from R_0 to R_0, but the switching time in the ALU is generally two microseconds earlier at W_2 time. Therefore, to modify Read Storage and Result to Storage operations for the Overlap Mode and provide switching time at the proper Storage reference points, a trigger is provided to control operations in the normal Storage switching time. This trigger is the Storage Read/Write Mode trigger of FIG. 7*e*, where it will be observed that the Mode Control trigger On line **136***e*.**35**, the Storage Read/Write Mode line **93***q*.**07** and the R_0 (D2) line **7***d*.**09** cooperate to turn On the Storage Read/Write Mode Control trigger at R_0 which occurs at the end of the Start cycle (R_0 to R_0). By way of the Mode Control trigger Off line **136***e*.**37** and the R_0 (D2) line **7***d*.**09**, the Storage Read/Write Mode Control trigger is turned Off at the end of the Transition cycle. The manner in which the output lines **7***e*.**01** and **7***e*.**02** condition the Storage Write Driver Select circuits of FIG. 41, the manner in which the line **7***e*.**04** conditions circuits of the X Switch Core Write Drivers of FIG. 38*b* and *c*, and the manner in which the line **7***e*.**03** controls the Odd/Even Gating circuit of FIG. 42, will be discussed in detail later.

At this time it is convenient to refer to the Sequence Chart of FIG. 150*b* for an example of the manner in which the Storage Read/Write Mode is used. Assume that SAC starts at address 27. Those instructions adapted to the use of Overlap Mode Control operate in the Storage field from right to left and, therefore SAC will always step plus in this mode. The first cycle is a Start cycle, the sixth cycle is a Transition cycle due to recognition of a Critical Address, and the tenth cycle is a Transition cycle due to a condition recognized previously which causes the end of the sequence.

The Storage Read/Write Mode line **93***q*.**06** is up throughout the operations, as a result of decoding the instruction. The Add trigger is turned On at W_1 by the Not Transition line **136***d*.**02**, the Minus On Block Add trigger line **93***v*.**01** and the A_2/R_3–W_1 line **103***b*.**23** which brings up the Add trigger On line **136***a*.**06** at W_1 as shown in the Sequence Chart. The Read Storage line **136***b*.**10** and Result to Storage line **136***b*.**11** are up throughout the operation because the Storage Read/Write Mode line **93***q*.**06** is up as previously described. The Set CR 2 pulse occurs at W_0 of each Start cycle and of each Fully Overlapped cycle, but does not occur in Transition cycles because during the Transition cycle it is not required that characters be read from Storage, but only that one be returned to Storage. The Step SAC+1 line **136***b*.**08** is up except during the Transition cycle, since the Storage R/W Mode line **93***q*.**06** is up throughout the operation and the Not Transition line **136***d*.**03** remains up until the Transition cycle. The Minus On Block Read Gate line **7***e*.**03** is up during the Start cycle and remains up until the Transition cycle because during this time it is required that a character be read during the Read portion of each of the cycles. The Minus On Block Write Gate line **7***e*.**04** is brough down at W_2 preceding the Start cycle since the result will not be returned to Storage during the Start cycle. The Minus On Block Storage X Write Gate line **7***e*.**04** will be up until the Storage Read/Write Mode trigger Off line **7***e*.**01** is up during the Storage Read/Write Mode. The Minus On Block Step X Read Gate line **7***e*.**03** is up during the Storage Read/Write Mode when the Transition line **136***c*.**05** is down. In the SAC controls, FIG. 52*e*, the SAC–$\overline{1}$ line **52***a*.**13**, the SAC–$\overline{2}$ line **52***a*.**12**, SAC–$\overline{4}$ line **52***a*.**11**, SAC–$\overline{8}$ line **52***a*.**14** and SAC–$\overline{16}$ line **52***c*.**01** are combined to provide SAC Equals Critical Address on the line **52***e*.**01**. Therefore, for addresses 0, 32, 64, 96, and so forth, the SAC Equal Critical Address line **52***e*.**01** will be positive and will signify this condition to the Overlap Execution controls of FIG. 136*b*. The Turn On Auto Transition Trigger line **136***b*.**05** is up during the Storage Read/Write Mode as indicated by line **93***q*.**06** when SAC contains a Critical Address. In the example, SAC initially contains an address at 27 and the Turn On Auto Transition Trigger line **93***u*.**01** is down. As indicated in the Sequence Chart, FIG. 150*b*, the Storage Address Select Register is set from SAC, a character is read from the address 27, but a character is not written during the Start cycle since a result has not been computed.

With SAC set at address 27, the 128, 64 and 32 triggers of FIG. 52*c* are Off and the 16 trigger is On. In FIG. 52*a*, the 4 trigger is Off and the 8, 2 and 1 triggers are On. In FIG. 53*a*, SAC–1 line **52***a*.**02**, SAC–2 line **52***a*.**04**, SAC–$\overline{4}$ line **52***a*.**05** and SAC–8 line **52***a*.**07** are positive, and at R_0 when the line **101.06** goes positive the SASR 8, 2 and 1 triggers are turned On and the 4 trigger is turned Off. In FIG. 53*b*, the SAC–16 line **52***c*.**03**, the SAC–$\overline{32}$ line **52***c*.**04**, the SAC–$\overline{64}$ line **52***b*.**06** and the SAC–$\overline{128}$ line **52***b*.**08** are positive, the Minus On Suppress SASR to SAC line **136***b*.**07** is positive (this is not a Transition cycle) and at R_0 the line **101.07** causes the 16 trigger to be turned On and the 32, 64 and 128 triggers to be turned Off.

Referring now to the Decoder of FIG. 34*b*, the SASR $\overline{64}$ and $\overline{32}$ lines **53***b*.**05** and **53***b*.**03**, respectively, are positive and the 00 line **34***b*.**01** is positive. In FIG. 36*a*, the $\overline{00}$ line **36***a*.**01** is down and the $\overline{32}$, $\overline{64}$ and $\overline{96}$ lines **36***a*.**02**, **36***a*.**03** and **36***a*.**04** are up. In FIG. 36*b*, the Storage Read Bias Gate on the line **7***d*.**02** provides outputs on the 32 line **36***b*.**02**, the 64 line **36***b*.**03** and the 96 line **36***b*.**04**, to the Y Switch Core Matrix of FIG. 39 at R_0.

In FIG. 34*d*, the SASR $\overline{4}$ line **53***a*.**05**, the SASR 2 line **53***a*.**04** and the SASR 1 line **53***a*.**02** are up to furnish an output on the Decimal 3 line **34***d*.**04**. In FIG. 38*a*, the line **34***d*.**04** brings down the $\overline{3}$ line **38***a*.**04** and the remaining output lines stay positive. These output lines go to the X Switch Core Write Drivers of FIGS. 38*b* and *c* where they are gated by the Storage Read Bias Gate Odd lines **42.01** and **42.05** to provide outputs on the 1 line **38***b*.**02**, the 5 line **38***c*.**02** and the 7 line **38***c*.**04**. In FIG. 40, all of the columns in the Odd Matrix are driven with bias current, except the 3 line **38***b*.**04**, at $R_{0.5}$.

In FIG. 34*a*, the SASR $\overline{256}$ line **54.01** and the SASR $\overline{128}$ line **53***b*.**07** are positive and provide an output on the 000 line **34***a*.**01**, the latter going to FIG. 37 where the Storage Read Gate On line **7***d*.**03** proides an output on the 000 line **37.01** at R_1. In FIG. 39, the 000 line **37.01** is being driven with set current but reset current is fur-

nished on the lines **36***b*.**02**, **36***b*.**03** and **36***b*.**04**, as previously described, so the 0 core is set and a half-select output signal is induced on the secondary winding.

In FIG. 34*c*, the SASR 16 line **53***b*.**02** and the SASR 8 line **53***a*.**08** are up and the 24 line **34***c*.**04** is made positive. In FIG. 35, the 24 line, in combination with Storage Read Gate Odd line **42.02**, furnishes a signal on the 24 Odd line **35.08**, the latter going to FIG. 40 where it drives the upper row of switch cores with set current at $R_{1,3}$. As described previously, the lines **38***c*.**04**, **38***c*.**02** and **38***b*.**02** are providing reset current so the 27 core is set thereby inducing half-select current in the secondary 27.

In FIG. 45, the 0 line of the Y axis and the 27 line of the X axis each carry half-select current and the character from the seven planes is read into the SBR as previously described. Thus, address 27 has been read from during the Read portion of the Start cycle. Writing into address 27 is suppressed by the circuits of FIG. 7*e* where the Storage R/W Mode Control trigger is Off. (Also see chart of FIG. 150*b*.) Because the Minus On Block Storage X Write Gate line **7***e*.**04** is down due to line **7***e*.**01** and line **93***q*.**07**, the Core Write Drivers of FIGS. 38*b* and *c* are not energized during the Write portion of the Start cycle which leaves the core 27 in the set condition.

The Storage Write Gate is generated in FIG. 7*d* at R_5 and is supplied to the Y Matrix of FIG. 39 via the Y Switch Core Write Drivers of FIG. 36*b* in the usual manner. Accordingly, the 00 line **36***b*.**01** resets core 0 of FIG. 39, the latter furnishing half-select current to the Y axis of the Array of FIG. 45 where it is of no effect in the absence of half-select current to the X axis.

At W_1 of the Start cycle, the Add trigger is turned On by the Not Transition line **136***d*.**02**, the Minus on Block Add trigger line **93***v*.**01** and the A_2/R_3–W_1 line **103***b*.**23** which brings up the Add Trigger On line **136***a*.**06**. At W_2, the Mode Control trigger is turned On by the Storage Read/Write Mode line **93***q*.**05**, the Not Transition line **136***d*.**02** and the A_3/R_4–W_2 line **103***b*.**07** bringing up the Mode Control Trigger On line **136***a*.**08** to define those cycles in which results are placed in Memory at the address read from in the previous cycle. In FIG. 7*e*, the Storage Read/Write Mode Control trigger is turned On at R_0 (beginning of the first Overlap cycle) by the Mode Control trigger On line **136***e*.**35**, the Storage Read/Write Mode line **93***q*.**07** and the R_0 (D2) line **7***d*.**09**. The Storage Read/Write Mode trigger On line **7***e*.**02** is not positive.

During the Read portion of cycle 2 (the first Overlap cycle) it is required that address 28 be read from. Therefore, core 28 of the Even Matrix of FIG. 40 will be set and core 27 preserved in its set condition until the Write portion of cycle 2 when it will be utilized for writing into address 27.

In FIG. 34*c*, the 24 line **34***c*.**04** is up and goes to the X Switch Core Read Driver of FIG. 35 which, in turn, furnishes an output on 24 Even line **35.04**. In FIG. 40, the row of switch cores linked by the line **35.04** is driven with set current.

In FIG. 34*d*, the SASR 4 line **53***a*.**06**, the SASR $\overline{2}$ line **53***a*.**03** and the SASR $\overline{1}$ line **53***a*.**01** are up to furnish a signal on the Decimal 4 line **34***d*.**05**. In FIG. 38*a*, the signal on the latter line is inverted and presented as a down condition on the $\overline{4}$ line **38***a*.**05** and the remaining output lines are positive. In FIG. 38*c*, the Storage Read Bias Even line **42.06** brings up the 6 line **38***c*.**03**; and in FIG. 38*b*, the Read Bias Even line **42.03** brings up the 0 line **38***b*.**01** and the 2 line **38***b*.**03**. In FIG. 40, reset current is provided to the columns of cores accordingly to overcome the effect of set current on the cores 24, 26 and 30. The result is that core 28 is set and current induced in its secondary winding is applied to the Storage Core Array.

In FIG. 34*a*, the 000 line **34***a*.**01** is up as before, and in FIG. 37 the 000 line **37.01** is driven at R_1 to provide set current to the lower row of cores in FIG. 39. In FIG. 34*b*, the 00 line **34***b*.**01** is up as before and in FIG. **36***a*, the $\overline{00}$ line **36***a*.**01** is down and the remaining output lines are up. In FIG. 36*b*, the latter lines are gated by the Storage Read Bias on line **7***d*.**02** to furnish reset current to FIG. 39 on the 32 line **36***b*.**02**, the 64 line **36***b*.**03** and the 96 line **36***b*.**04**. The 0 core is set as before and the secondary winding furnishes half-select current to the Array of FIG. 45. Referring to the sample plane of FIG. 45, the 0 line for the Y axis and the 28 line for the X Axis cause the contents of Storage at address 28 to be read into the SBR.

At the end of the Read portion of the first Overlap cycle, three switch cores are in the set condition, namely, the 0 core of the Y Switch Core Matrix, the 27 core of the Odd portion of the X Switch Core Matrix of FIG. 40, and the 28 core of the Even portion of the X Switch Core Matrix. It is pointed out that the 0 core of the Y Switch Core Matrix, FIG. 39, was set due to address 28, but will be reset to Write into address 27.

In FIGS. 38*b* and *c*, the Storage Write gate is supplied on the lines **7***d*.**06** and **7***d*.**07** respectively, and an input from Write Driver Select Circuits of FIG. 41 should provide a reset signal on the 3 line **38***b*.**04**. In FIG. 41, the Decimal 4 line **34***d*.**05** is up because of address 28 being used, but with the Storage R/W Mode trigger On, the line **7***e*.**02** gates the 4 input to the 3 output line **41.04**. Thus, in FIG. 38*b*, the 3 line is combined with the lines **7***e*.**04** and **7***d*.**06** to drive the 3 line **38***b*.**04**. In FIG. 40, the latter line resets the 27 core which then provides half-select current to the Array of FIG. 45. The 0 core of the Y Switch Core Matrix of FIG. 39 is reset as previously described and furnishes half-select current from the secondary winding to the Array of FIG. 45. Address 27 is thereby selected and binary "ones" are written into those planes where inhibit current is not supplied in the manner previously described. However, the character written into Storage at address 27 is the one computed during the Write portion of cycle 1 and the Read portion of cycle 2 and received from the Result Register. In this regard, the triggers of the Result Register of FIGS. 89*a* and *b* are set according to the bit configuration of the character contained therein. The NOT values are fed to the Storage Input Select Circuits of FIG. 43 on the lines **89***b*.**10**, **89***b*.**06**, **89***b*.**02**, **89***a*.**14**, **89***a*.**10**, **89***a*.**06** and **89***a*.**02**. With the Result to Storage line **137.05** positive the inputs from the SBR are blocked and the inputs from the Result Register gated to the Storage Inhibit Drivers of FIG. 44. The Storage Inhibit Gate on line **7***d*.**05** furnishes signals to the inhibit windings wherever it is desired to write "zeros." If the $\overline{C}$ line **43.01** is positive, such condition indicates the absence of a binary "one" in the C trigger of the Result Register.

Additional Overlap cycles are taken as indicated in the sequence chart of FIG. 150*b* until SAC steps to 32 which is a Critical Address. Referring now to SAC controls of FIG. 52*e*, the SAC Equals Critical Address line **52***e*.**01** becomes positive the instant that the five lower order SAC triggers are turned Off. In FIG. 136*b*, the line SAC Equals Critical Address is combined with Storage R/W Mode line **93***q*.**06** to bring up the Turn On Auto Transition Trigger line **136***b*.**05**. The latter line goes to FIG. 93*u* and leaves as line **93***u*.**01**. The Auto Transition trigger of FIG. 136*a* is turned On by the line **93***u*.**01** and Add Trigger On line **136***d*.**15** when the W_2 (D1) line **102.17** goes positive thereby defining a Transition cycle. During the Transition cycle CR 2 is blocked from being set to the character in SBR. This is caused by the fall of the NOT Transition line **136***d*.**01** in FIG. 100. During the Transition cycle, it is desired to prevent stepping SAC from address 32 to address 33 since the character at address 32 must be read during the Start cycle. This is accomplished in FIG. 136*b* by the fall of the NOT Transition line **136***d*.**03** which brings down one leg of its

AND Circuit also fed by the Storage Read/Write Mode line **93***q*.**06**. The result is that Step SAC+1 line **136***b*.**08** is down. In FIG. 7*e*, the Minus On Block Storage X Read Gate line **7***e*.**03** has been positive via the Inverter because the Transition line **136***c*.**05** was down; however, when the Auto Transition trigger is On, the Minus On Block Storage X Read Gate is held down to prevent Odd/Even Gating in FIG. 42 during the Transition cycle.

It will be noted that the Add trigger has remained On for the Read portion of the Transition cycle since computation is taking place involving the character at address 31, but at W_1, the fall of the A_2/R_3–W_1 line **103***b*.**23** at the diode gate conditioned by Transition line **136***c*.**01** turns the Add trigger Off.

At W_2, the Add trigger Off line **136***d*.**18** in combination with the W_2 (D1) pulse on the line **102.17** turns the Auto Transition trigger Off and the Transition lines **136***a*.**03** and **136***a*.**04** go negative. As the Transition line **136***c*.**01** goes negative the fall of the A_3/R_4–W_2 line **103***b*.**07** turns the Mode Control trigger Off to indicate that no results are to be placed in Storage during the Start cycle (cycle 7) which follows the Transition cycle (cycle 6). In FIG. 7*e*, the Mode Control trigger Off line **136***e*.**37** is combined with the R_0 (D2) pulse to turn Off the Storage R/W Mode trigger which then signifies that during the Start cycle information is not written into Storage at an address read from in the previous cycle. At W_2, the Step SAC line **136***b*.**08** goes positive in FIG. 136*b* due to NOT Transition line **136***d*.**03** to allow SAC to step from 31 to 32 during the Start cycle (cycle 7). Also at W_2, the Minus On Block Read Gate line **7***e*.**03** goes positive due to the fall of Transition line **136***c*.**05** in FIG. 7*e* to provide Odd and Even Gating in FIG. 42 during the Read portion of the Start cycle.

During the Read portion of the Start cycle the character at address 32 is read so NOT Transition line **136***d*.**01** in FIG. 100 permits the Set CR 1 pulse to be formed on the line **100.02**.

The Write Gate to the X Switch Core Array must be blocked during the Start cycle to preserve the set status of the switch core; therefore, in FIG. 7*e*, the lines **7***e*.**01** and **93***q*.**07** being positive hold down the line **7***e*.**04** to the Storage X Switch Core Write Drivers of FIGS. 38*b* and *c*.

At W_1 of the second Start cycle (cycle 7), the Add trigger is turned On by the Minus On Block Add trigger line **93***v*.**01**, the NOT Transition line **136***d*.**02** and the A_2/R_3–W_1 line **103***b*.**23**. Then at W_2, the Mode Control trigger is turned On by the Storage R/W Model line **93***q*.**05**, the NOT Transition line **136***d*.**02** and the A_3/R_4–W_2 line **103***b*.**07**. Subsequently, the Storage R/W Mode trigger of FIG. 7*e* is turned On at R_0 by the Mode Control trigger On line **136***e*.**35**, the Storage R/W Mode line **93***q*.**07** and the R_0 (D2) line **7***d*.**09**. Since these actions initiate a Fully Overlapped cycle, it is now desired to Write into Storage at an address Read from previously, namely, address 32. The Minus On Block Storage X Write Gate line **7***e*.**04** is made positive by the fall of the Storage R/W Mode trigger Off line **7***e*.**01**. Conditions now prevail due to the states of the Overlap Mode Control triggers for a fully overlapped operation during cycles 8 and 9 and characters are Read and Written as shown at the bottom of the sequence chart of FIG. 150*b*.

At W_0 of cycle 9, some condition imposed by the instruction signifies the end of this sequence of operations by making the Turn On Transition trigger line **93***m*.**04** in FIG. 93*m* positive. As a result, in FIG. 136*a*, the Transition trigger is turned On by the Turn On Transition trigger line **93***m*.**04**, the Add trigger On line **136***d*.**15** and the W_2 (D1) line **102.17**. Thus, the lines **136***a*.**02** through **136***a*.**04** are positive. (Certain "housekeeping" operations are performed with the lines **136***e*.**01** through **136***e*.**23** such as calling for an Instruction cycle after the Transition cycle. These operations are concerned with ending the sequence rather than those associated with Transition cycles generally, such as those controlled by the Transition lines **136***a*.**03** and **136***a*.**04** which further distribute signals according to FIGS. 136*c* and *d*.)

When the Transition trigger is turned On, the setting of CR 2 is blocked in FIG. 100 since, in effect, the Read portion of the Transition cycle is not utilized to introduce data to the ALU. Stepping of SAC from address 35 is suppressed by the line **136***b*.**08** which falls with the NOT Transition line **136***d*.**03**. Line **7***e*.**03** of FIG. 7*e* is down, but the Write Gate on line **7***e*.**04** stays up to write the results of computation into address 34.

At W_1, the Add trigger is turned Off as previously described. In FIG. 93*q*, the Storage Read/Write Mode line **93***q*.**06** comes down at W_2 to finish the Mode operation.

At W_2 the Transition trigger is turned Off by the Add trigger Off line **136***d*.**18** and the W_2 (D1) line **102.17**. The Transition line **136***c*.**01** and the A_3/R_4–W_2 line **103***b*.**07** cooperate to turn Off the Mode Control trigger at W_2. In FIG. 7*e*, the Storage R/W Mode Control trigger is turned Off by the Mode Control Trigger Off line **136***e*.**37** and the R_0 line **7***d*.**09**. Read Storage line **136***b*.**10** and Result to Storage line **136***b*.**11** drop with the Storage R/W Mode line **93***q*.**06**. SAC is prevented from stepping to 35 by the fall of the Step SAC+1 line **136***b*.**08** due to the fall of the line **93***q*.**06**. The Minus On Block Storage X Read Gate line **7***e*.**03** is made positive by lines **93***q*.**07** and **136***c*.**05**, now down, thereby permitting an Instruction to be read on the next cycle.

EXAMPLE OF ADDITION

As previously described, the Add instruction adds a numerical field in Memory to a factor in Storage. The address part of the instruction specifies the units position of the field in Memory and the Storage unit to be used.

Digits are added starting with the specified units position of the Memory field, and as a digit result is obtained, it replaces the digit in Storage which was used to form the digit result. Addition of digits continues through higher order positions until a non-numeric character is sensed in Memory. The non-numeric character is not placed in Storage. The sign of the result is determined according to the rules of algebra for addition from the signs of the fields which are contained in the Zone portion of the character in the units order in the case of the Memory field, and in the status of the Sign Trigger in the case of the Storage field.

The left hand limit of the result in Storage is automatically set by a Storage Mark (SM), mentioned previously, placed adjacent the highest order digit.

Assume that the number SM45712147321 has been previously place in Accumulator Storage by a Reset and Add instruction, and that the Storage Sign Trigger is set to plus. The SM indicates a Storage Mark of a single character (see character code chart) placed adjacent the highest order of the number. Since this factor is in Accumulator Storage, its address is determined by the Starting Point Counter.

The other factor to be added is A64321150+, which is located in Memory at discrete addresses, the units order of which is specified by the address part of the Add instruction. The A indicates a non-numeric character which defines the field length, but it may be any character with Zone bits. For purposes of field definition, it is interpreted merely as a non-numeric character. The sign of the number to be added is located in the Zone bits of the units order. A plus sign is indicated by binary "ones" in the B and A positions and a minus sign is indicated by a binary "one" in the B position and a binary "zero" in the A position.

Let it be assumed that the units order of the Memory field is located at address 9010 in Memory. Then the number 64321150 is contained in addresses 9003 through 9010. As shown in the Instruction Chart, the operation

part of the instruction (character 0) would be a G which has the bit configuration of

C	B	A	8	4	2	1
1	1	1	0	1	1	1

Address 9010 would be contained in characters 1 through 4 as follows:

	C	B	A	8	4	2	1
Character 1 has a value of 9	0	0	0	1	0	0	1
Character 2 has a value of 0	0	0	0	1	0	1	0
Character 3 has a value of 1	1	0	0	0	0	0	1
Character 4 has a value of 0	0	0	0	1	0	1	0

Note that in characters 2 and 3 the Zone bits contain zeros since Accumulator Storage is addressed. Summarizing, the Add instruction has the following format: G9010.

At W_2 of the last Execute cycle of a sequence, the I Time lines **124.27** through **124.34** are made positive. The line **124.29** goes to I Time Routing Controls of FIG. 61 where it brings up Read Memory line **61.08** to extract the instruction from Memory, the Block Add Trigger line **61.09** to prevent turning the Add trigger On, the Set MAC 1 to MAR line **61.10**, the Set SAC to SPC line **61.11** and the Set MASR to IC line **61.12** if the Indirect Address Trigger is Off and no PCT request is made. The **124.30** line goes to Instruction Check Circuits of FIG. 60, and the line **124.31** goes to Resets of FIG. 139*a* to provide appropriate resets at R_0. The line **124.32** goes to MAC 1 Controls of FIG. 30*f*, and the line **124.33** goes to SAC Controls of FIG. 52*e*. The line **124.34** goes to Clock R–W/R–A–W Switching of FIG. 99 to provide the additional (A) portion between Read and Write portions which make up the 13 microsecond Instruction cycle.

The Instruction G9010 is extracted from a Memory location, for example, 00004 according to the stored program during the Read portion of an Instruction cycle and decoded during the A and Write portions of the same cycle. Recall that an Instruction cycle is 13 microseconds long, having the A portion inserted in the clock as described above.

In view of the examples of Memory previously given, the explanation of reading this instruction from Memory will be omitted and the assumption made that this Add Instruction is now located in the Memory Buffer register and that the Instruction Counter contains the value 00004.

Referring now to FIGS. 21*a* and *b*, the operation code G is stored in the Operation Register trigger at A_0 during Instruction time by a positive pulse on an A_0 (D0.4) I Time 1 (Use) line **101.26**. (The pulse on line **101.26** is generated in FIG. 101 by the Use line **105.16**, Indirect Addressing Trigger Off line **121.07** and A_0 (D1) line **97.02**.) Memory Buffer Register character 0–1 line **14***b*.**02**, MBR character 0–2 line **14***b*.**02** and Memory Buffer Register character 0–4 line **14***b*.**02** are up indicating binary "ones," and the Memory Buffer Register character 0–8 line **14***b*.**02** is down indicating a binary "zero." In FIG. 21*b*, the Memory Buffer Register character 0–A line **14***b*.**02**, Memory Buffer Register character 0–B line **14***b*.**02** and Memory Buffer Register character 0–C line **14***b*.**02** are up. Accordingly, at A_0 time, the 1, 2, 4, A, B and C triggers are turned On, and the Operation Register 1 lines **21***a*.**07** through **21***a*.**11** are up, the Operation Register 2 lines **21***a*.**17** through **21***a*.**22** are up, the Operation Register 4 lines **21***a*.**28** through **21***a*.**33** are up, the Operation Register $\overline{8}$ lines **21***a*.**34** through **21***a*.**37** are up, the Operation Register A line **21***b*.**02** is up, the Operation Register B line **21***b*.**04** is up and the Operation Register C line **21***b*.**06** is up. In the Operation Zone Decoder, FIG. 23*a*, the Operation Register A line **21***b*.**06** and the Operation Register B line **21***b*.**04** are up; the Operation Register $\overline{A}$ line **21***b*.**01** and the Operation Register $\overline{B}$ line **21***b*.**03** are down. A negative AND circuit is identical with the positive OR circuit, the latter giving a plus output if any input is plus, and, thus, the negative AND circuit requires that all inputs be minus for a minus output. Since only one input to a negative AND circuit may be up to provide a positive output, then the Minus Operation Register A, B lines **23***a*.**01** through **23***a*.**10** are down and the remaining lines **23***a*.**11** through **23***a*.**43** are positive. The line **23***a*.**07** to FIG. 23*h* is the only line effective for the Add instruction.

Referring now to the Add, Subtract, Normal Transfer, Load Operation Decoder of FIG. 23*h*, the Operation Register $\overline{1}$ line **21***a*.**04**, Operation Register $\overline{2}$ line **21***a*.**15**, Operation Register $\overline{4}$ line **21***a*.**26** and the Operation Register 8 line **21***a*.**44** are down. Also, the Minus Operation Register A, B line **23***a*.**07** is down causing the Add lines **23***h*.**01** through **23***h*.**03** to be up by way of an Inverter. In FIG. 61, the Use line **105.09**, the I Time line **124.29**, and CR 1 $\overline{A}$ line are up to make positive the End I Time Use lines **61.01** through **61.06**. An A bit in CR 1 during Instruction time controls an Indirect Addressing operation and is not present in this instruction example. Line **61.06** goes to I/E Timer outputs of FIG. 124 where it brings up the lines **124.23**, **124.24**, **124.25** and **124.26**. In FIG. 74*a*, the Add line **23***h*.**01** is up and End I Time (Use) line **124.25** is up to condition the diode gate for the fall of the A_3/R_4–W_2 line which turns On the Add/Sub. 1 trigger at W_2. Thus, the Add/Sub. 1 lines **74***a*.**01** through **74***a*.**07** are positive.

In the I Time Routing Controls of FIG. 61, the End I Time (Use) line **61.03**, now positive, goes to I/E and IA triggers of FIG. 121 where it conditions the diode gate (DG) for the fall of the A_3/R_4–W_2 (Blocked) line **104.10** to turn On the I/E trigger, i.e., render the right side non-conducting, to make the E Time line **121.02** positive at W_2. The latter line goes to I/E Timer Outputs of FIG. 123, and lines **123.01** through **123.26** and line **123.56** are rendered positive to specify Execute time throughout the machine. The End I Time (Use) line **61.04** goes to ECC 1 and ECC 2 triggers of FIG. 122 where it conditions a diode gate for the fall of the A_3/R_4–W_2 line **121.03** to turn On the ECC 1 trigger and make positive the ECC 1 line **122.03** and the ECC ½ line **122.05** at W_2. The signals on these lines are distributed via FIGS. 123 and 124.

From the Operation Decoder of FIG. 23*h*, the line **23***h*.**03** goes to the Operation Check circuits, FIG. 24, where the Operation Register C line **21***b*.**06** is up. Accordingly, the Add line **23***h*.**03** and the Operation Register C line **21***b*.**06** cannot combine to provide an operation check on the line **24.01**. Thus, it will be noted that those operations associated with the upper Cascaded OR circuit are those in which the C bit is a 1, whereas those operation lines associated with the lower cascaded OR circuit are associated with the $\overline{C}$ line and in this manner a check of the operation code is provided.

At A_0, the Storage Select Register is set to the contents of the zone portions of characters 2 and 3 of the Memory Buffer Register. Accumulator Storage is addressed when the zone bits of characters 2 and 3 contain "zeros," and in FIG. 16*a*, the MBR Character 2–B line **14***a*.**02**, the MBR character 2–A line **14***a*.**02**, the MBR Character 3–B line **14***a*.**02** and the MBR Character 3–A line **14***a*.**02** are down. At A_0, the A_0 (D0.4) I Time (Use) line **101.24** pulse appears, but because of the absence of bits indicated by the down condition of the lines just mentioned none of the triggers of the Storage Select Register are set On.

At A_0, the contents of the Memory Buffer Register Character 4 position are set into CR 1 of FIG. 57. Since character 4 of the Memory Buffer Register has a value of 0 designated by 10 (8 and 2 bits), only the Memory Out Bus 8 line **20***d*.**04** and the Memory Out Bus 2 line **20***d*.**06** are up, and these lines condition positive diode gates associated with the On sides of the 8 and 2 triggers respectively. The Memory Out Bus C line **20***d*.**01**, the

Memory Out Bus B line **20***d*.**02**, the Memory Out Bus A line **20***d*.**03**, the Memory Out Bus 4 line **20***d*.**05** and the Memory Out Bus 1 line **20***d*.**07** are down. However, these last-mentioned lines are inverted to condition positive diode gates (GJ) associated with the Off sides of the C, B, A, 4 and 1 triggers respectively. Accordingly, the Set CR 1 (D0.4) pulse on line **100.02** sets CR 1 to the value 0 expressed as 10 (8 and 2 bits) at A_0 of the Instruction cycle.

Although it is not essential to set character 4 in the Character Register 1 during the Instruction cycle, code check circuits are provided for normally checking the redundancy of those characters placed in CR 1 for processing. Therefore, it is convenient to allow character 4 of the Instruction to be set into CR 1 to supply outputs to the Code Check Circuits for redundancy checking the character. Also, where such outputs are supplied they may be used conveniently for sensing bits for any purpose desired, such as, for example, Indirect Addressing which is indicated by a binary "one" in the A bit of character 4. Accordingly, outputs with CR 1 are used when convenient for any purpose in analyzing character 4.

During the Write portion of the Instruction cycle, the contents of the MBR are written back into Memory at addresses 00000–00004, and the MBR is reset at W_3 by Gate MBR Reset line **139***a*.**07** and the W_3 (D2) line **7***d*.**10** of FIG. 5*g*.

At the beginning of ECC 1, MASR contains the value 09010, MAC 1 contains the value 09010, MAR the value 09010, SSR the value 0000, SPC the value 27, SAC the value 27, IC the value 00004 and CR 1 the value 0 (8 and 2 bits). During subsequent Execute cycles of this operation MAR, SPC and SSR do not change.

The first Execute cycle (ECC 1) is defined by the ECC 1 trigger being On. Overlap Mode Control is used and, thus, ECC 1 is a Start cycle. In FIG. 122, the End I Time (Use) line **61.04** is up, as described previously, and the fall of the A_3/R_4–W_2 line **121.03** turns On the ECC 1 trigger which makes the ECC 1 line **122.03** positive. This signal is distributed via the lines **123.27** through **123.34** of FIG. 123 to control those functions peculiar to the first Execute cycle of certain instructions. The line **123.34** goes to the IC of FIG. 32*a* where it is combined with the Not Manual 3 line **116.09**, Minus On Block Step IC line **93***j*.**12** and A_2/R_3–W_1 line **103***a*.**20** to change the state of the units order of IC from 4 to 9 at R_3 of ECC 1.

In FIG. 74*d*, the Add/Subtract 1 line **74***a*.**03** is positive at W_2 and the Auxiliary Trigger 1 is Off thereby making the Aux. Trigger 1 Off line **138***j*.**18** positive so the Memory Read Mode line **74***d*.**01** is positive. The Memory Read Mode line is routed through Mode Control Routing, FIG. 93*q*, to Overlap Execution Controls of FIG. 136*b*. In the latter figure, Memory Read Mode line **93***q*.**01** is combined with the Not Transition line **136***d*.**03** (both Transition triggers are Off) to make positive the Read Memory line **136***b*.**02**, the latter going to FIG. 93*a* where, in combination with the Use line **105.14** and MASR $\overline{40,000}$ line **49***j*.**08** respectively, it makes positive the Read Memory lines **93***a*.**03** through **93***a*.**05**. The line **93***a*.**03** goes to the Pulse Generator of FIG. 100 where it will provide the Set CR 1 pulse on the line **100.02** at W_0 of ECC 1. The Read Memory line **93***a*.**04** goes to FIG. 135*b* where it is ineffective since a PCT Request is not made. The Read Memory line **93***a*.**05** goes to FIG. 5*e* where it furnishes the Read Gates.

CR 1 to Adder line **74***d*.**02** of FIG. 74*d* is positive by either the Add/Sub. 1 and ECC 1/2 line **74***e*.**01** or the Memory Read Mode line and Transition Trigger Off line **136***e*.**24**. Line **74***d*.**02** goes to FIG. 93*b* where it leaves as line **93***b*.**01**, the latter going to Adder Input Switching of FIG. 73 where it gates CR 1 to Adder. The signal on Add/Sub. 1 and ECC 1/2 line **74***e*.**01** of FIG. 74*d* passes through the cascaded OR circuit (OC) to bring up the Digit Adder Out line **74***d*.**04**. The Storage Mark trigger is Off (it was reset by Instruction Reset and a Storage Mark has not been sensed) so the line **138***d*.**16** of FIG. 74*d* is up and in combination with Add/Sub. 1 line **74***a*.**03** brings up the CR 2 to T/C line **74***d*.**05** to FIG. 93*b*.

In FIG. 74*f*, Add/Sub. 1 line **74***a*.**05** is up and Aux. Trigger 1 Off line **138***j*.**20** is up to specify Storage Read/Write Mode by a positive signal on the line **74***f*.**01**. In FIG. 93*q*, the signal is distributed on line **93***q*.**05** to FIG. 136*c*; on line **93***q*.**06** to FIG. 136*b*; and on line **93***q*.**07** to FIG. 7*e*.

In FIG. 136*a*, the Storage Read/Write Mode line **93***q*.**05** and the Not Transition line **136***d*.**02** condition a diode gate for the fall of the A_3/R_3–W_2 line **103***b*.**07** which turns On the Mode Control trigger at W_2 of ECC 1 (a Start cycle).

In FIG. 136*b*, the Storage R/W Mode line **93***q*.**06** brings up the Result to Storage line **136***b*.**11** for use in ECC 2 as will be described later. The Storage Read/Write Mode line **93***q*.**07** goes to Storage R/W Mode Control of FIG. 7*e* to turn On the Storage R/W Mode trigger at R_0, 2 microseconds after the Mode Control trigger is turned On at W_2 of ECC 1.

In FIG. 93*g*, the (—) On Block Step MAC 1 line **136***b*.**01** is positive because, in FIG. 136*b*, the Transition line **136***c*.**02** is down, Memory R/W Mode line **93***q*.**03** is down, and the Mode Control Trigger Off line **136***e*.**36** is down. The Step MAC 1–1 line **74***c*.**03** is up because in FIG. 74*c* the Add/Sub. 1 line **74***a*.**01** is up, Step MAC 1 lines **93***g*.**04** through **93***g*.**10** are positive. The lines **93***f*.**05** through **93***g*.**09** step MAC 1–1 at R_3 of ECC 1; the line **93***g*.**04** goes to FIG. 136*b* where its signal is blocked by Memory R/W Mode line **93***q*.**03** and Mode Control Trigger On line **136***e*.**34**; and the line **93***g*.**10** goes to FIG. 136*b* where its signal is blocked by Memory R/W Mode line **93***q*.**03**.

As previously mentioned, Add/Sub. 1 line **74***a*.**04** and ECC 1/2 line **124.10** provide a positive signal on Turn On Transition Trigger line **74***e*.**03** to FIG. 93*m* where it is routed on the line **93***m*.**04** to FIG. 136*a*. In the latter figure, it will be realized that the Transition trigger cannot be turned On until the Add trigger is turned On and a W_2 pulse is provided. Accordingly, the Transition trigger remains Off until W_2 of ECC 1. Also, in FIG. 136*a*, the Not Transition line **136***d*.**02** and the (—) On Block Add Trigger line **93***v*.**01** are up to condition the diode gate for the fall of the A_2/R_3–W_1 line **103***b*.**23** to turn On the Add trigger and bring up the Add Trigger On line **136***a*.**06** at W_1 of ECC 1 thereby defining ECC 1 as an Arithmetic cycle. The signal on line **136***a*.**06** is routed onto the lines **136***d*.**15** through **136***d*.**17**. Line **136***d*.**15** is that line referred to previously which assists in turning On the Transition trigger at W_2; the line **136***d*.**16** conditions circuits in FIG. 138*c* to turn On the SM trigger for Reset Add or Subtract operations or when CR 2 contains a Storage Mark; the line **136***d*.**17** is used in FIG. 101, Pulse Generator, to provide W_0 Add signals on the lines **101.08** through **101.16**. These W_0 Add signals are distributed to condition circuits for the 5 MPL Carry 4 trigger of FIG. 81, the 2 MPL Carry trigger of FIG. 80, the MPL Carry trigger of FIG. 85, the Decimal Carry trigger of FIG. 88, the Inter-Register Check trigger of FIG. 63*c*, the Storage Hi and Lo triggers of FIG. 138*a*, the Auxiliary DZT trigger of FIG. 138*h*, Auxiliary trigger 1 of FIG. 138*i*, and the Auxiliary trigger 2 of FIG. 138*k*.

Since SAC must step *up* through the addresses of Storage field, positive signals on the Storage R/W Mode line **93***q*.**06** and Not Transition line **136***d*.**03** bring up the Step SAC+1 line **136***b*.**08** to step SAC at R_3 of ECC 1 via FIG. 93*i*, Step SAC Routing.

Referring now to FIG. 52*b*, the SPC–1 line **51***a*.**02**, the SPC–2 line **51***a*.**04**, the SPC–$\overline{4}$ line **51***a*.**05** and SPC–8 line **51***a*.**08** are up. In FIG. 52*d*, the SPC–16 line **51***b*.**04**, the SPC–$\overline{32}$ line **51***b*.**05**, the SPC–$\overline{64}$ line **51***c*.**01** and the SPC–$\overline{128}$ line **51***c*.**05** are up. All of the lines taken to-

gether indicate a value of 27 in the Starting Point Counter. The Set SAC to SPC pulse on the lines **52***e*.**04** and **52***e*.**05** is derived from the SAC controls of FIG. 52*e*, and places the value of 27 in SAC at W_1.

As stated previously, the Starting Point Counter contains the address in the units position of the field in Accumulator Storage. This may be any address as determined by the arbitrary contents of the Starting Point Counter when the machine is turned On. As the value of the Starting Point Counter is changed in response to operations, it is always returned to the Starting address for the next operation. The value 27 will be arbitrarily selected as the Starting Point location of the field in Accumulator Storage, and it is this value which will be set into the Storage Address Counter during the Instruction cycle in this example.

In the Storage Address Select Register of FIGS. 53*a* and 53*b*, the SAC–1 line **52***a*.**02**, the SAC–2 line **52***a*.**04**, the SAC–$\overline{4}$ line **52***a*.**05**, the SAC–8 line **52***d*.**08**, the SAC–16 line **52***c*.**03**, the SAC–$\overline{32}$ line **52***c*.**04**, the SAC–$\overline{64}$ line **52***b*.**06** and the SAC–$\overline{128}$ line **52***b*.**08** are positive, and at R_0, the 1, 2, 8 and 16 triggers are turned On (if Off previously) and the 4, 32, 64 and 128 triggers are turned Off (if On previously).

In FIG. 34*b*, the SASR $\overline{64}$ line **53***b*.**05** and SASR $\overline{32}$ line **53***b*.**03** are positive to bring up the 00 line **34***b*.**01**. In FIG. 36*a*, the $\overline{00}$ line **36***a*.**01** is pulled down and the $\overline{32}$, $\overline{64}$ and $\overline{96}$ lines remain positive. In FIG. 36*b*, the Storage Read Bias Gate on line **7***d*.**02** drives the 32 line **36***b*.**02**, the 64 line **36***b*.**03** and the 96 line **36***b*.**04**, and in FIG. 39 reset current is provided to all columns except the one linked by the 00 line **36***b*.**01**.

In FIG. 34*d*, the SASR $\overline{4}$ line **53***a*.**05**, the SASR 2 line **53***a*.**04** and the SASR 1 line **53***a*.**02** are positive to bring up the Dec. 3 line **34***d*.**04** which goes to the 3×8 Decoder of FIG. 38*a* to pull down the $\overline{3}$ line **38***a*.**04**. The Dec. 3 line **34***d*.**04** also goes to FIG. 41 where it is gated by the Storage R/W Mode Trigger On line **7***e*.**01** to make positive the 3 line **41**.**04**. In FIG. 42, the SASR 1 line **34***d*.**09** and the Storage Read Bias Gate line **7***d*.**01** make positive the Storage Read Bias Gate Odd lines **42**.**01** and **42**.**05** to FIGS. 38*b* and *c*, where all of the Odd Output lines except the 3 line **38***b*.**04** are driven with reset current.

In the 2×4 Decoder of FIG. 34*a*, the SASR $\overline{256}$ line **54**.**01** and SASR $\overline{128}$ line **53***b*.**07** furnish a positive level on the 000 line **34***a*.**01** to FIG. 37 where the level is gated by the Storage Read Gate at R_1 on the line **7***d*.**03**. In FIG. 39, set current is provided to the cores linked by the 000 line **37**.**01** which sets the 0 core and provides half-select current from the 0 secondary to the Storage Array of FIG. 45.

In FIG. 34*c*, Storage 2×4 Decoder, the SASR 16 line **53***b*.**02** and the SASR 8 line **63***a*.**08** are positive and provide a positive level on the 24 line **34***c*.**04** to the X Switch Core Read Drivers of FIG. 35. In FIG. 42, the Storage Read Gate at $R_{1.3}$ on line **7***d*.**04** is combined with (−) On Block Storage (X) Read Gate on line **7***e*.**03** and SASR 1 on line **34***d*.**09** to furnish a positive signal on the Storage Read Gate Odd line **42**.**02**. In FIG. 35, X Switch Core Read Drivers, the 24 line **34***c*.**04** is gated by the Storage Read Gate Odd line **42**.**02** to drive the 24 Odd line **35**.**08**. In FIG. 40, the 7 line **38***c*.**04**, the 5 line **38***c*.**02** and the 1 line **38***b*.**02** being driven with reset current and the 24 Odd line **35**.**08** being driven with set current, sets the 27 core to "one" and provides a half-select reset current to the Storage Array of FIG. 45.

In FIG. 45, coincident currents are applied to those cores of 7 planes at address 27 and the value 1 (CBA8421 =1000001) is set into the SBR, FIG. 47, at $R_{3.5}$ via the Sense Amplifiers of FIG. 46.

The Memory Address Register receives the Memory address 9010 from the MBR at A_1 of the Instruction cycle. The numeric bit configuration of the Memory Address is as follows:

Character	1	2	3	4
Value	9	0	1	0
BCD form	1001	1010	0001	1010

In the Memory Address controls of FIG. 17*f*, the 8 and 2 bits of character 4 are present on the Memory Out Bus–8 line **20***d*.**04** and Memory Out Bus–2 line **20***d*.**06** by way of the Memory Out Switch which selects character 4. Character 4 is always selected during Instruction cycles because characters 1 through 4 are always required to be placed in MAR. Therefore, in FIG. 3*e*, either the lines **49***a*.**04** and **49***a*.**17** or the lines **49***a*.**08**, **49***a*.**15** and **49***a*.**11** are up since the units position of the Memory Address Select Register of FIG. 49*a* must contain an address for the Instruction ending in 4 or 9 as mentioned previously. Thus, one or the other combination of signals renders Select Character 4 lines **3***e*.**09** and **3***e*.**10** positive.

In FIG. 20*a*, the 8 and 2 bits of character 4 are gated onto the lines **20***c*.**04** and **20***c*.**06** by the Select Character 4 line **20***a*.**09**. In FIG. 20*d*, the 8 and 2 signals are present on the 8 bit line **20***d*.**04** and 2 bit line **20***d*.**06**. The C, B, A, 8, 4, 2 and 1 lines go to CR 1, FIG. 57; the 8, 4, 2 and 1 lines go to FIG. 17*a*; and the 8 and 2 lines go to FIG. 17*f*. In FIG. 17*f*, the Memory Out Bus 2 line **20***d*.**06** and Memory Out Bus line **20***d*.**04** are positive, and the Block Set First Order MAR line **17***f*.**07** is brought down via the inverter (IK). Remember that zero is expressed as 10 in Memory, but must be converted to zero in the ALU. Thus, in FIG. 17*a*, the Block Set 1st Order MAR line **17***f*.**07**, being down, blocks the 8 and 2 bits from being set in the triggers when the A_1 (D0.4) Use line **101**.**19** becomes positive.

In FIG. 17*f*, neither the MBR Character 3–2 line nor the 3–8 line is up so the Block Set 2nd Order MAR line **17***f*.**08** is positive. In FIG. 17*b*, the MBR Character 3–1 line **14***a*.**02** is positive (recall character 3 in MBR is 0001), and the A_1 (D0.4) Use line goes positive at A_1 and turns On the MAR–10 trigger to bring up the MAR–10 lines **17***b*.**26** through **17***b*.**31**. The remaining triggers in the 2nd Order of MAR are Off and the NOT lines are positive.

In FIG. 17*f*, the MBR Character 2–2 line and 2–8 line are positive since character 2 in MBR is 10 (1010) and the Block Set 3rd Order of MAR line **17***f*.**09** is made negative. In FIG. 17*c*, the MBR Character 2–8 line **14***a*.**02** and the MBR Character 2–2 line **14***a*.**02** are positive, but the Block Set 3rd Order MAR line **17***f*.**09** is down to block the setting of the 800 and 200 triggers. When the A_1 (D0.4) Use line **101**.**21** goes positive at A_1 all of the 3rd Order triggers are Off and the NOT lines are positive.

In FIG. 17*f*, the MBR Character 1–2 line is down and the MBR Character 1–8 line is up, and, accordingly, the Block Set 4th Order MAR line **17***f*.**10** is positive. In FIG. 17*d*, the MBR Character 1–8 line, the MBR Character 1–1 line and the Block Set line **17***f*.**10** are positive so the A_1 (D0.4) Use line **101**.**22**, when positive, turns On the 8000 and 1000 triggers to bring up the lines **17***d*.**04** through **17***d*.**09** and lines **17***d*.**30** through **17***d*.**35**. Since the remaining triggers of the 4th Order are Off, their NOT lines are positive.

The 5th Order of MAR, FIG. 17*e*, is employed for Memory addresses of 10,000 and above. Since the chosen Memory address is 9010, the A and B bits of MBR character 1 and the B bit of MBR character 4 are "zeros" and all of the triggers of the 5th Order of MAR are Off providing positive signals on the NOT lines.

As a result of setting MAR to the Memory Address of the MBR at A_1 of the Instruction cycle, MAR now has triggers set representing the address

9010 (8000+1000+10)

At W_1, MAC 1 is set to the contents of MAR. In FIG. 61, the I Time line **124.29** is positive from W_2 time of the cycle preceding the Instruction cycle to W_2 time of the Instruction cycle and the Set MAC 1 to MAR line **61.10** (among others) is positive. In FIG. 93*j*, the signal on the line **61.10** passes to the Set MAC 1 to MAR line **93***j*.**09**, the latter line going to FIG. 30*f*, MAC 1 Controls, where it is combined with A_2/R_3–W_1 (Use) line **103.05**, Gate MAR to PCT line **135***b*.**06** and I Time line **124.32** to bring up the Set MAC 1 to MAR lines **30***f*.**07** through **30***f*.**11**, each of which goes to an order of MAC 1. The 1st or Units Order of MAC 1 is shown in FIG. 30*a*, where the MAR–$\overline{8}$ line **17***a*.**01**, MAR–$\overline{4}$ line **17***a*.**08**, MAR–$\overline{2}$ line **17***a*.**17** and MAR–$\overline{1}$ line **17***a*.**25** are positive to condition gates for the fall of the signal on Set MAC 1 to MAR line **30***f*.**07** at W_1 (see FIG. 30*f*, line **103.05**). The outputs of these diode gates, so conditioned by the NOT lines, turn any of the triggers Off which were On previously.

In FIG. 30*b*, the 2nd Order of MAC 1, the MAR–$\overline{80}$ line **17***b*.**02**, the MAR–$\overline{40}$ line **17***b*.**09**, the MAR–$\overline{20}$ line **17***b*.**17** and the MAR–10 line **17***b*.**28** are positive to condition diode gates for the fall of the signal on Set MAC 1 to MAR line **30***f*.**08** at W_1. As a result, the MAC 1–$\overline{80}$ line **30***b*.**01** and the MAC 1–10 lines **30***b*.**07** and **30***b*.**08** are positive.

In FIG. 30*c*, the 3rd Order of MAC 1, the MAR–$\overline{800}$ line **17***c*.**03**, the MAR–$\overline{400}$ line **17***c*.**10**, the MAR–$\overline{200}$ line **17***c*.**19** and the MAR–$\overline{100}$ line **17***c*.**32** are positive to condition diode gates for the fall of the Set MAC 1 to MAR line **30***f*.**09**. Thus, the only output line which is positive is the MAC 1–$\overline{800}$ line **30***c*.**01**.

In the 4th Order of MAC 1, FIG. 30*d*, the MAR 8000 line **17***d*.**06**, the MAR $\overline{4000}$ line **17***d*.**11**, the MAR $\overline{2000}$ line **17***d*.**20** and the MAR 1000 line **17***d*.**32** are positive to condition diode gates for the fall of the Set MAC 1 to MAR line **30***f*.**10**. The 8000 and 1000 triggers are turned On (if Off) and the 4000 and 2000 triggers are turned Off (if On). Thus, MAC 1–8000 lines **30***d*.**02** through **30***d*.**04** and MAC 1–1000 lines **30***d*.**07** and **30***d*.**08** are positive.

In FIG. 30*e*, the 5th Order of MAC 1, MAR–$\overline{40,000}$ line **17***e*.**15**, MAR–$\overline{20,000}$ line **17***e*.**08** and MAR $\overline{10,000}$ line **17***e*.**02** are positive to condition diode gates for the fall of the Set MAC 1 to MAR line **30***f*.**11**. If any of these triggers are On, they are turned Off at W_1.

Outputs of MAC 1 are supplied to the FIG. 30*g* where the value of the units order of MAC 1 is determined and where End of Memory is sensed. In this instance, the MAC 1–$\overline{1}$ line **30***a*.**12**, the MAC 1–$\overline{2}$ line **30***a*.**09**, MAR 1–$\overline{4}$ line **30***a*.**06** and MAC 1–$\overline{8}$ line **30***a*.**02** are positive to provide a positive signal on the MAC 1 Ends in 0/5 lines **30***g*.**01** and **30***g*.**02** to FIGS. 136*b* and 70*b*, respectively.

Outputs of MAC 1 are also supplied to the Memory Address Select Register set circuits of FIGS. 49*b*, *d*, *f*, *h* and *j*. In FIG. 49*b*, MAC 1–8 line **30***a*.**03**, MAC 1–4 line **30***a*.**07**, MAC 1–2 line **30***a*.**10** and MAC 1–1 line **30***a*.**13** are negative and are not gated by the positive signal on the Set MASR to MAC 1 line **93***s*.**02**. Therefore, the 8 line **49***b*.**02**, the 4 line **49***b*.**04**, the 2 line **49***b*.**06** and the 1 line **49***b*.**08** are negative and the $\overline{8}$ line **49***b*.**01**, the $\overline{4}$ line **49***b*.**03**, the $\overline{2}$ line **49***b*.**05** and the $\overline{1}$ line **49***b*.**07** are positive via the inverters (IK). In FIG. 49*a*, the lines $\overline{8}$, $\overline{4}$, $\overline{2}$ and $\overline{1}$ condition positive diode gates for the positive signal on the R_0 line **101.01** to turn Off all of the 1st order triggers of MASR.

In FIG. 49*d*, the MAC 1–80 line **30***b*.**02**, the MAC 1–40 line **30***b*.**05**, and the MAC 1–20 line **30***b*.**06** are down and the MAC 1–10 line **30***b*.**07** is up. The signal on the latter line is gated by the Set MASR to MAC 1 line **93***s*.**03** to bring up the 10 line **49***d*.**08**. The 80 line **49***d*.**02**, the 40 line **49***d*.**04** and the 20 line **49***d*.**06** are down so the $\overline{80}$ line **49***d*.**01**, the $\overline{40}$ line **49***d*.**03** and the $\overline{20}$ line **49***d*.**05** are positive via inverters (IK). In FIG. 49*c*, the positive outputs from FIG. 49*d* condition positive diode gates for the positive pulse on the R_0 line **101.02** to turn On the 10 trigger and turn Off the 80, 40 and 20 triggers.

In FIG. 49*f*, the MAC 1–800 line **30***c*.**20**, the MAC 1–400 line **30***c*.**05**, the MAC 1–200 line **30***c*.**06** and the MAC 1–100 line **30***c*.**07** are negative, and although the Set MASR to MAC 1 line **93***s*.**03** is positive, the 800 line **49***f*.**02**, the 400 line **49***f*.**04**, the 200 line **49***f*.**06** and the 100 line **49***f*.**08** are down. However, the $\overline{800}$ line **49***f*.**01**, the $\overline{400}$ line **49***f*.**03**, the $\overline{200}$ line **49***f*.**05** and the $\overline{100}$ line **49***f*.**07** are up due to inverters (IK). In FIG. 49*e*, the $\overline{800}$, $\overline{400}$, $\overline{200}$ and $\overline{100}$ lines are positive to condition diode gates for the passage of the pulse on the R_0 line **101.03** to turn Off all of the 3rd order triggers.

In FIG. 49*h*, the MAC 1–8000 line **30***d*.**02** and the MAC 1–1000 lines are positive and the MAC 1–4000 line **30***d*.**05** and the MAC 1–2000 line **30***d*.**06** are negative. The positive signals are gated onto the 8000 line **49***h*.**02** and the 1000 line **49***h*.**08** by the Set MASR to MAC 1 signal on the line **93***s*.**03**. The $\overline{4000}$ line **49***h*.**03** and the $\overline{2000}$ line **49***h*.**06** are positive due to inverters (IK). In FIG. 49*j*, the 8000, $\overline{4000}$, $\overline{2000}$ and 1000 lines are positive to condition diode gates for the positive signal on the R_0 line **101.04** to turn On the 8000 and 1000 triggers and turn Off the 4000 and 2000 triggers.

In FIG. 49*j*, the MAC 1–40,000 line **30***e*.**01**, the MAC 1–20,000 line **30***e*.**03** and the MAC 1–10,000 line **30***e*.**05** are down and output signals are not gated by the Set MASR to MAC 1 line **93***s*.**03**. Thus, the 40,000 line **49***j*.**02**, the 20,000 line **49***j*.**04** and the 10,000 line **49***j*.**06** are negative and the $\overline{40,000}$ line **49***j*.**01**, the $\overline{20,000}$ line **49***j*.**03** and the $\overline{10,000}$ line **49***j*.**05** are positive via the inverters. In FIG. 49*i*, the $\overline{10,000}$, $\overline{20,000}$ and $\overline{40,000}$ lines are positive to condition diode gates for the signal on the R_0 line **101.05** to turn Off all of the 5th order triggers of MASR.

Positive signals are provided on the $\overline{20,000}$ line **49***j*.**04**, the $\overline{80}$ line **49***c*.**01**, the $\overline{40}$ line **49***c*.**04** and the $\overline{20}$ line **49***c*.**07** from MASR to the 4×10 Decoder of FIG. 3*b*, where they are combined to make positive the 00 lines **3***b*.**01** and **3***b*.**02**. In FIG. 5*a*, the only positive input line is the 00 line **3***b*.**01**, so the $\overline{00}$ line **5***a*.**02** is negative and the 00 line **5***a*.**01** is positive. All remaining NOT lines are positive via inverters (IJK). In FIGS. 5*b* and *c*, all of the output lines are driven at R_0 of ECC 1 except for the 00 line **5***b*.**01**. In FIG. 8, the Y Switch Core Matrix, all of the columns are driven with reset current except for the column associated with the 00 line **5***b*.**01**.

Positive signals are provided on the $\overline{10,000}$ line **49***i*.**04**, the $\overline{4}$ line **49***a*.**05**, the $\overline{8}$ line **49***a*.**01**, the $\overline{1}$ line **49***a*.**14**, the $\overline{2}$ line **49***a*.**10** and the 10 line **49***c*.**11** from MASR to the 6×8 Decoder of FIG. 3*d*, where they are combined to make positive the 10–14 lines **3***d*.**05** and **3***d*.**06**. In FIG. 7*a*, the (10–14) line provides a positive signal on the 10–14 line **7***a*.**05** and brings down the $\overline{10}$–$\overline{14}$ line **7***a*.**06**. All of the remaining NOT lines are positive. In FIGS. 7*b* and *c*, all of the output lines are driven with reset current except the 10–14 line **7***b*.**03** when the Memory Read Bias Gate comes up at $R_{0.5}$ of ECC 1 on lines **5***g*.**11** and **5***g*.**12**. In FIG. 9, all of the columns are driven with reset current except the column linked by the 10–14 line **7***b*.**03**.

Positive signals are provided on the $\overline{4000}$ line **49***g*.**04**, the $\overline{2000}$ line **49***g*.**07**, the 8000 line **49***g*.**02** and the 1000 line **49***g*.**11** making the 9000 lines **3***a*.**19** and **3***a*.**20** positive. In FIG. 4, when the Memory Y Read Gate goes positive at R_1 of ECC 1 the 9000 line **4.10** is driven. In FIG. 8 the 9000 line **4.10** is driven with set current, so the 9000 core at the intersection of the 9000 line **4.10** and the 00 line **5***b*.**01** is set providing half-select current on its secondary winding to the Core Array of FIG. 13.

In FIG. 3*c*, the $\overline{100}$ line **49***e*.**10**, the $\overline{200}$ line **49***e*.**07**, the $\overline{400}$ line **49***e*.**04** and the $\overline{800}$ line **49***e*.**01** are positive

which make positive the 000 lines **3***c*.**01** and **3***c*.**02**. In FIG. 6, the 000 line **6.01** is driven when the Memory X Read Gate goes positive at $R_{1.3}$ of ECC 1. In FIG. 9, the bottom row of cores are driven with set current by the 000 line **6.01**, and the core at the intersection of this line and the 10–14 line **7***b*.**03** is set thereby furnishing half-select current to the Core Array of FIG. 13.

In FIG. 13, the 9000 and the 10 lines read out the thirty-five planes at addresses 9010 through 9014. For those planes in which a binary "one" is stored, a signal is provided on the appropriate sense winding which is sampled at $R_{3.5}$ of ECC 1 to turn On those MBR triggers of FIGS. 14*a* and *b* where "ones" are sensed. Although five characters are read into MBR from addresses 9010 through 9014, it is only the character of address 9010 which is selected since this character is in the units order of the Memory field.

During the latter portion of ECC 1, the signs of the Memory and Accumulator Storage field are checked to determine whether they are alike or not. When the data was entered in the Accumulator, the Accumulator Sign trigger was set plus to indicate the sign of the field for later operations. Thus, in FIG. 62, the left plate of this trigger is up and with a positive signal on SSR=0000 line **54.11**, the Storage Sign (+) lines **62.03** through **62.06** are up. Further, the A and B bits of the units order of each field are available on the lines **52.28**, **52.17**, **59.22** and **59.03**. In this instance, both A and B bits of the units order characters are "ones" indicating positive fields so the Signs Alike lines **62***a*.**07** and **62***a*.**09** are made positive at W_0 when CR 1 and CR 2 are set to their respective values during ECC 1. The line **62***a*.**07** goes to FIG. 74*c* where it routes Complement line **74***c*.**02** during ECC 1 and ECC 2 for a subtract operation, the line **62.08** goes to Divide Routing Controls, FIG. 66*h*, and the line **62.09** goes to Multiply Control of FIG. 67*b*. These lines are not pertinent in this example.

CR 1 and CR 2 were set to 0 and 1 respectively at W_0 of ECC 1 (a Start cycle). The contents of CR 1 are passed to the Digit Adder via Multiply Circuits (1 Multiple selected), and the contents of CR 2 are passed via T/C Controls to the Digit Adder for addition during the Write portion of ECC 1 and the Read portion of ECC 2.

It will be recalled that during the Start cycle of Storage R/W Mode operation writing into Storage is inhibited. In FIG. 7*e*, the Storage R/W Mode Control trigger is not turned On until the end of ECC 1 at R_0. Accordingly, the Off side signal of the trigger combined with the signal on the Storage R/W Mode line **93***q*.**07** pulls down the (—) On Block Storage X Write Gate line **7***e*.**04**. In FIGS. 38*b* and *c*, the Write Gate to Storage X Switch Core Matrix is inhibited, thus leaving the switch core **27** in the set state without writing in Storage at address 27.

In FIG. 74*e*, positive signals on Add/Sub. 1 line **74***a*.**04**, ECC 1/2 line **124.10** and Not Transition line **136***d*.**05** bring up the Turn On DZT line **74***e*.**02**, which signal is directed through FIG. 93*m* as line **93***m*.**02** to FIG. 138*h*. The SR=0000 line **54.12** is positive (an Auxiliary Storage unit is not addressed) so the Accumulator DZT trigger is turned On at W_2 bringing up the DZT On lines **138***h*.**06** through **138***h*.**11**.

Referring now to the ECC 1 and ECC 2 triggers of FIG. 122, the right plate of the ECC 1 trigger is up to condition an AND circuit also fed by Not End E Time line **121.05**. The positive output of the AND circuit conditions a diode gate for the fall of the A_3/R_4–W_2 line **121.03** which turns On the ECC 2 trigger at W_2 of the ECC 1 cycle thereby making the ECC 2 line **122.04** positive. The ECC 1 trigger is On prior to W_2 and its right plate conditions a gate for the fall of the line **121.03** at W_2 which turns the ECC 1 trigger Off. At W_2 of ECC 1, the Not ECC 1 line **122.02**, the ECC 2 line **122.04** and the ECC 1/2 line **122.05** are positive. By way of review, the Transition trigger, Mode Control trigger, Add trigger and DZT trigger were turned On at W_2 of ECC 1 and the Storage R/W trigger was turned On at R_0 (the beginning of ECC 2). ECC 2 is now defined as a Transition cycle.

During the Read portion of ECC 2, Memory Read Mode, Storage Read/Write Mode, CR 1 to Adder, Digit Adder Out, Step MAC 1, and CR 2 to T/C conditions remain in effect. MAC 1 retains the address 9009 during the Transition cycle (ECC 2) because, in FIG. 136*h*, Memory Read Mode line **93***q*.**01** and Transition line **136***c*.**02** are positive making (—) On Block Step MAC 1 line **136***b*.**01** negative. At R_0, MASR is set to 9009. Stepping of SAC is suppressed since ECC 2 is a Transition cycle and an address must not be skipped. In FIG. 136*b*, the Storage R/W Mode line **93***q*.**06** is positive, but the Not Transition line **136***d*.**03** is negative thereby making Step SAC+1 line **136***b*.**08** negative. Accordingly, SAC retains address 28 during ECC 2 and the Storage Address Select Register sets to the contents of SAC at R_0 as usual except that during ECC 2 the setting of the 32, 64 and 128 triggers of SASR are blocked by the line **136***b*.**07** being negative which, actually, is only necessary when SAC contains a critical address and is permissive in other instances such as this. The reason for such blocking will become apparent when a critical address is reached. The IC remains at 0009 as stepped in ECC 1.

Referring now to FIG. 122, the ECC 1/2 line **124.09** goes to FIG. 74*d* where, in combination with Add/Sub. 1 line **74***a*.**03** and Digit Adder Output≠0 line **87.21**, it makes positive the Turn Off DZT line **74***d*.**06** for use at W_0 to turn Off the DZT. In FIG. 74*e*, ECC 1/2 line **124.10** and Add/Sub. 1 line **74***a*.**04** furnish positive signals on Add/Sub. and ECC 1/2 line **74***e*.**01** and Turn On Transition Trigger line **74***e*.**03**. Turn On DZT line **74***e*.**02** is not up during ECC 2 because Not Transition line **136***d*.**05** is down. Add/Sub. and ECC 1/2 lines **74***e*.**01** goes to FIG. 74*d* where it is used to make positive the CR 1 to Adder line **74***d*.**02** and Digit Adder Out line **74***d*.**04**. Turn On Transition Trigger line **74***e*.**03** is routed to FIG. 136*a* (via FIG. 93*m*) where it will be of no effect since the Add Trigger On line **136***d*.**15** falls at W_1 before the W_2 line **103.17** becomes positive. The ECC 1/2 line **124.11** goes to FIG. 74*f* where it is ineffective to bring up the Turn On Sign Check Trigger line **74***f*.**06** even though Transition Trigger On line **136***e*.**04** and Add/Sub. 1 line **74***a*.**05** are positive because the CR 1–$\overline{B}$ line **59.08** is negative (B bit in position of CR 1 contains a binary "one").

In FIG. 74*d*, Aux. Trigger 1 Off line **138***j*.**18** and Add/Sub. 1 line **74***a*.**03** provide a Memory Read Mode signal on line **74***d*.**01** and Add/Sub. 1 line **74***a*.**03** and SMT Off line **138***d*.**16** provide a positive signal on CR 2 to T/C line **74***d*.**05**.

At this stage in the description, a question may arise concerning the reason for making ECC 2 a Transition cycle, and, in this regard, it is pointed out that the units order of the Memory field is a non-numeric character and operations must be such as to differentiate between this non-numeric character and those which cause the end of the operation, i.e., a non-numeric character adjacent the highest order of the Memory field. Since only the numeric portion of this character of the units order is of interest, a positive signal on Zone Adder Out line **93***c*.**02** is not provided simply because the line is not routed during the Add instruction.

When operating in the Storage Read/Write Mode, reading out of Storage is suppressed during Transition cycles; accordingly, reading out of Storage is suppressed during ECC 2. In FIG. 7*e*, the Storage R/W Mode line **93***q*.**07** and the Transition line **136***c*.**05** are positive to bring down the (—) On Block Storage X Read Gate line **7***e*.**03**. In FIG. 42, the latter line blocks the AND circuit also fed by SASR $\overline{1}$ line **34***d*.**10** and Storage Read Gate line **7***d*.**04**, and the Storage Read Gate Even lines **42.04** and **42.06**

are down. In FIG. 35, the 24 Even Output line is not driven and switch core 28 of FIG. 40 is not set.

More specifically, during ECC 2, SASR contains the value 28 so decoder signals are present on the 000 line **34***a*.**01** of FIG. 34*a*, the 00 line **34***b*.**01** of FIG. 34*b*, the 24 line **34***c*.**04** of FIG. 34*c*, and the Dec. 4 line **34***d*.**05** of FIG. 34*d*. In FIG. 36*a*, the $\overline{00}$ line **36***a*.**01** is down and the $\overline{32}$ line **36***a*.**02**, the $\overline{64}$ line **36***a*.**03**, and the $\overline{96}$ line **36***a*.**04** are up. In FIG. 36*b*, the $\overline{32}$, $\overline{64}$ and $\overline{96}$ lines are gated by the Storage Read Bias on line **7***d*.**02** so that the 32, 64 and 96 lines of the Y Switch Core Matrix of FIG. 39 are driven with reset current. In FIG. 37, the 000 line **34***a*.**01** is gated by the Storage Read Gate on line **7***d*.**03** to drive the 000 line **37.01**, and in the Y Switch Core Matrix, FIG. 39, the row of cores linked by the latter line is driven with set current which sets the 0 core and provides half-select current on the 0 secondary to the Storage Array of FIG. 45.

In FIG. 38*a*, the Dec. 4 line **34***d*.**05** is up so the $\overline{4}$ line **38***a*.**05** is down and the remaining output lines are up. In FIG. 38*b*, the Storage Read Bias Gate Even gates the $\overline{0}$ and $\overline{2}$ signals to the 0 Even line **38***b*.**01** and the 2 line **38***b*.**03**, and in FIG. 38*c*, the Storage Read Bias Gate Even gates $\overline{6}$ signals to the 6 line **38***c*.**03**. In FIG. 40, the columns linked by the 6, 2 and 0 Even lines are driven with reset current. In FIG. 35, the 24 line **34***c*.**04** is positive, but the Storage Read Gate Even on line **42.04** is suppressed by the (—) On Block Storage X Read Gate line **7***e*.**03** of FIG. 42. Thus, in FIG. 40, set current is not provided on the 24 Even line **35.04** and core 28 is not set. However, the 27 core of the Odd Matrix remains undisturbed (set) and the 0 core of the Y Switch Matrix is set for use with the 27 core for writing into address 27 during the write portion of ECC 2. In the Storage Array of FIG. 45, the 0 line of the Y Axis received half-select current which was ineffective in the absence of half-select current to the X Axis lines.

The contents of CR 1 and CR 2 are not set at W_0 of the Transition cycle, but retain their previous contents. This is accomplished by not providing signals on the Set CR 1 line **100.02** and Set CR 2 line **100.01**. In FIG. 136*b*, the Read Memory line **136***b*.**02** is down as described above. In FIG. 93*a*, the line **136***b*.**02** being down, brings down the Read Memory (ALU) lines **93***a*.**03** and **93***a*.**04**. In FIG. 100, line **93***a*.**03** being down prevents passage of the A_0 (D1) pulse on the line **97.01** and the Set CR 1 pulse is not developed. CR 1 is not provided with electronic reset, and in the absence of a set pulse retains the value 0. Similarly, the Not Transition line **136***d*.**01** in FIG. 100 is down and the pulse on CR 2 line **100.01** is not developed. Thus, CR 2 retains the value 1.

At R_2 of ECC 2, the result of adding 0 and 1 is available to the 8, 4, 2 and 1 triggers of the Result Register of FIG. 89*a*. The Result 1 line **87.09** is up and is gated by the R_2–W_0/A_0 Use line **103***a*.**14** to the RR–1 line **89***a*.**03** and to a positive diode gate (G_1). A signal on the R_4 (D0.4) Use line **101.17** turns On the 1 trigger at R_4. As stated previously, the Zone Adder outputs are blocked so the Result A and Result B input lines of FIG. 89*a* are negative. Referring now to FIG. 74*f*, the ECC 1/2 line **124.11** and Add/Sub. 1 line **74***a*.**05** make positive the Generate C Bit Out line **74***f*.**04** and in FIG. 93*c*, the signal is transmitted via line **93***c*.**03** to the C Bit Generator of FIG. 90. In the latter figure, the Result 1 line **87.12** is up and the Result 2 line **87.01**, the Result 4 line **87.05**, the Result 8 line **87.13**, the Result A line **79.02** and the Result B line **79.06** are down. With the Generate C Bit Out line **93***a*.**03** positive, a positive signal is present on the Result C line **90.01**. In FIG. 89*a*, this signal, in combination with R_2–A_0/W_0 line **103***a*.**15** and R_4 (D0.4) line **101.18**, turns On the Result C trigger. The Result Register now contains the digit 1 (CBA8421=1000001).

In FIG. 74*d*, the Digit Adder Output≠0 line **87.12** is positive as determined by the Decimal Correction circuits of FIG. 87, the Add/Sub. 1 line **74***a*.**03** is positive, and the ECC 1/2 line **124.19** is positive. These signals make positive the Turn Off DZT line **74***a*.**06** which goes to FIG. 93*m* to bring up the line **93***m*.**03**. In FIG. 138*h*, the SSR=0000 line **54.12** and Turn Off DZT line **93***m*.**03** condition a positive diode gate for the signal on the W_0 (D0.4) Add line **101.14** which turns Off the Accumulator Digit Zero trigger thereby bringing up the lines **138***h*.**01** through **138***h*.**05**.

During the Write portion of ECC 2, the result having a value of 1 is written from the Result Register into address 27 of Accumulator Storage. In FIG. 136*b*, the Result to Storage line **136***b*.**11** is positive due to Storage Read/Write Mode line **93***q*.**06**. In FIG. 93*p*, the Result to Storage line **93***p*.**02** is positive and goes to the Result to Storage trigger of FIG. 137 where it is combined with a signal on the A_2/R_3–W_1 (Use) line **103***a*.**07** to turn On the trigger at R_3 and bring up the Result to Storage lines **137.05** and **137.06**. In FIG. 43, the signal on line **137.05** passes through the AND circuit (unused input positive) and gates the positive signals on the $\overline{B}$ line **89.06**, $\overline{A}$ line **89***b*.**02**, $\overline{8}$ line **89***a*.**14**, $\overline{4}$ line **89***a*.**10** and $\overline{2}$ line **89***a*.**06** onto their respective output lines for passage to the Storage Inhibit Drivers of FIG. 44. The Result to Storage line **137.06** goes to Result Register Code Check circuits of FIG. 91 where the character is checked for redundancy. At $R_{4,5}$ inhibit current is supplied from the Storage Inhibit Drivers of FIG. 44 on the $\overline{B}$ line **44.02**, the $\overline{A}$ line **44.03**, the $\overline{8}$ line **44.04**, the $\overline{4}$ line **44.05** and the $\overline{2}$ line **44.06** to those planes of the Storage Array of FIG. 45 where it is desired to write "zeros," namely, the B, A, 8, 4, and 2 planes. Each of the seven planes receives coincident current at the selected address 27 for setting the selected core of each to a "one" at W_0. Therefore, the 27 core of the X Switch Core Matrix, FIG. 40, and the 0 core of the Y Switch Core Matrix, FIG. 39, must be reset. In FIG. 36*b*, the 00 line **34***b*.**01** is positive from FIG. 34*b* and the Storage Write Gate line **7***d*.**08** goes positive at W_0 to drive the 00 line **36***b*.**01**. In FIG. 39, reset current flows through the column linked by the latter line to reset core 0 which provides half-select current on the Y axis line 0 in FIG. 45. In FIG. 7*e*, the Storage R/W Mode Trigger Off line **7***e*.**01** is down so the (—) On Block Storage X Write Gate line **7***e*.**04** is up. In FIGURE 34*d*, the Dec. 4 line **34***d*.**05** is positive because the address in SASR is 28 and the SASR $\overline{2}$ line **53***a*.**03**, SASR $\overline{1}$ line **53***a*.**01**, and the SASR 4 line **53***a*.**06** are positive. In FIGURE 41, the Storage R/W Mode Trigger On line **7***e*.**01** gates the Dec. 4 signal onto the Dec. 3 line **41.04**. In FIG. 38*b*, the 3 line from FIG. 41, the Storage Write Gate line **7***d*.**06** and the Storage X Write Gate line **7***e*.**04** are up to drive the 3 output line **38***b*.**04**. In FIG. 40, this line **38***b*.**04** drives the column of cores linked thereby with reset current which resets core 27. The output from core 27 is coupled to the Storage Array of FIG. 45 to provide half-select set current on the 27 line. Thus, all seven cores of address 27 have coincident set current applied thereto, but the cores for representing B, A, 8, 4 and 2 have inhibit current applied as well. The result is that only the C and 1 bits at address 27 are set to "ones."

Referring to the Overlap Control triggers of FIG. 136*a*, the Transition line **136***c*.**01** is positive to condition a diode gate for the fall of the A_2/R_3–W_1 line **103***b*.**23** which turns Off the Add trigger at W_1. The Transition line **136***c*.**01** also conditions a diode gate for the fall of the A_3/R_4–W_2 line **103***b*.**07** which turns Off the Mode Control trigger at W_2. The Mode Control trigger Off line **13***a*.**07** becomes positive and the signal is distributed in FIG. 136*e* via lines **136***e*.**36** and **136***e*.**37**. The Add Trigger Off line **13***a*.**05**, now positive, goes to FIG. 136*d*, and leaves as line **136***d*.**18**. In FIG. 136*a*, it is combined with the signal on W_2 (D1) line **102.17** to turn Off the Transition trigger and make positive the Transition Trigger Off line

136*a*.01. The latter line goes to FIG. 136*e* where the signal is distributed via lines 136*e*.24 through 136*e*.33. The Mode Control Trigger Off line 136*e*.37 goes to FIG. 7*e* where it is combined with the R_0 (D2) pulse on line 7*d*.09 to turn Off the Storage R/W Mode Control trigger and make positive the Storage R/W Mode Trigger Off line 7*e*.01.

In FIG. 122, the right plate output, indicating ECC 2, conditions a diode gate for the fall of the A_3/R_4–W_2 pulse on the line 121.03, which turns Off the ECC 2 trigger at W_2. Therefore, Not ECC 1/2 line 122.01 and NOT ECC 1 line 122.02 are positive.

In FIG. 74*g*, none of the combinations of signals yield a signal on the End E Time line 74*g*.03, and in FIG. 121, the I/E trigger remains set to E time and operations are maintained with the Overlap Mode Controls governing the mode of operation.

E Time line 123.07 maintains Read Storage in FIG. 93*a*, E Time line 123.22 conditions MAC 1 Controls of FIG. 30*f*, and E Time line 123.23 conditions SAC Controls of FIG. 52*e*. In FIG. 74*d*, Auxiliary Trigger 1 Off line 138*j*.18 and Add/Sub. 1 line 74*a*.03 are positive to maintain Memory Read Mode line 74*d*.01 positive. The Transition Trigger Off line 136*e*.24 maintains CR 1 to Adder line 74*d*.02 positive. Add/Sub. 1 line 74*a*.03 and SMT Off line furnish a positive signal on the Digit Adder Out line 74*d*.04 and CR 2 to T/C line 74*d*.05. Turn Off DZT line 74*d*.06 remains positive although its use is not required.

In FIG. 74*f*, Add/Sub. 1 line 74*a*.05 and SMT Off line 138*d*.17 provide positive output signals on the Storage R/W Mode line 74*f*.01 to FIG. 93*q* and on the Gen. C Bit Out line 74*f*.04. Note that Turn On Auxiliary Trigger 1 line 74*f*.05 is not made positive even though Add/Sub. 1 line 74*a*.05 and Not ECC 1/2 line 124.19 are positive since Transition Trigger On line 136*e*.04 is negative. It is Auxiliary Trigger 1 which is used to recognize the end of the Memory field and continue operations if there is a carry which requires another addition with the next digit of the Storage field. In the absence of such a carry, Aux. Trigger 1 is turned On at W_2 of the last Execute cycle and is reset at R_0, two microseconds later.

With the Storage Read/Write Mode line positive and the Storage Read/Write Trigger Off, a Start cycle is defined which is in third Execute cycle of the sequence. Memory is read from and written into at address 9009 in the Memory Read Mode; Storage is read from at address 28 and the Write pulse to the X Switch Core Matrix is suppressed leaving the 28 Switch Core in the set state without putting any result into Storage at the address 28.

The selection of the 5 line begins at the MASR which now contains 9009. The units order contains 9 for Execute cycle 3 instead of 10 for ECC 1, so only output lines from FIG. 49*a* need be considered. In FIG. 3*e*, the $\overline{8}$ line 49*a*.02, the $\overline{2}$ line 49*a*.11, the 4 line 49*a*.08 and the 1 line 49*a*.17 are positive to bring up the Select Character 4 line 3*e*.09. In FIG. 3*d*, the $\overline{10,000}$ line 49*i*.01, the $\overline{10}$ line 49*c*.10, the $\overline{8}$ line 49*a*.01, the $\overline{2}$ line 49*a*.10, the 4 line 49*a*.07 and the 1 line 49*a*.16 are positive to bring up the 5–9 lines 3*d*.03 and 3*d*.04. In FIG. 7*a*, the $\overline{5}$–$\overline{9}$ line 7*a*.04 is brought down, and the 5–9 line 7*a*.03 is brought up. The remaining NOT lines are up and their complements down.

In FIGS. 7*b* and *c*, all output lines are driven except the 5–9 line 7*b*.02 when the Memory Read Bias Gate becomes positive. In FIG. 9, all of the columns of cores receive reset current except the column linked by the 5–9 line 7*b*.02. In FIG. 6, the 000 line 6.01 is driven when the Memory X Read Gate goes positive since the 000 line 3*c*.01 is positive as it was during ECC 1. Thus, in FIG. 9, the row of cores linked by the 000 line 6.01 and the 5–9 core is set thereby providing half-select current to FIG. 13 on the 5 line. Coincident currents are supplied to the thirty-five cores at the intersection of the 9000 and the 5 lines to read out addresses 9005 through 9009.

The Memory Buffer Register is set as previously described, and character 4 is selected by the Select Character 4 line 3*e*.09 described above. In FIG. 20*a*, the Low Character line 136*b*.04 and High Character line 136*b*.06 are down since the Memory Read/Write Mode is *not* employed for the Add instruction. Therefore, the Normal line and Select Character 4 line 3*e*.09 make positive the Select Character 4 Out line 20*a*.09. In FIG. 20*c*, the character 4–4 line and the character 4–1 line are positive indicating a 5, and the Select Character 4 line 20*a*.09 gates the signals onto the 4 Bit line 20*c*.05 and 1 Bit line 20*c*.07. In FIG. 20*d*, the signals are passed directly onto the 4 Bit line 20*d*.05 and 1 Bit line 20*d*.07 to CR 1 of FIG. 57 and the 1st order of MAR of FIG. 17*a*.

The contents of SASR have remained at the address 28 set therein at R_0 of ECC 2 and the digit 2 is read from this address. Briefly, SASR $\overline{2}$, SASR $\overline{1}$ and SASR 4 lines in FIG. 34*d* make the Dec. 4 line 34*d*.05 positive. In FIG. 38*a*, the positive signal on Dec. 4 line is inverted and the remaining output lines remain positive. In FIGS. 38*b* and *c*, the Even output lines are driven and in FIG. 40, the 6 line 38*c*.03, the 2 line 38*b*.03 and 0 line 38*b*.01 are driven with reset current. In FIG. 35, the positive signal on the 24 line 34*c*.05 remains as before but is now gated by the Storage Read Gate Even On line 42.04 derived from the SASR $\overline{1}$ signal on line 34*b*.10 in FIG. 42. The 24 Even line 35.04 furnishes set current to the X Switch Core Matrix of FIG. 40 where the 28 core is set. In FIG. 45, the 0 line of the X Axis is driven as before and the 28 line is driven as described above to furnish coincident currents to the 7 cores of address 28, thereby reading out the digit 2 (CBA8421=1000010) into SBR. At W_0, CR 1 and CR 2 are set to 5 and 2 respectively because Read Memory of FIG. 136*b* is up (Not Transition line 136*d*.04 is positive) to furnish a Set CR 1 signal and because, in FIG. 100, Not Transition line 136*d*.01 is positive to furnish a Set CR 2 signal.

Since the third Execute cycle is a Start cycle, writing into Storage is prohibited in the manner described for ECC 1. The 0 Switch Core of the Y Switch Core Matrix is reset, but the 28 core of the X Switch Core Matrix remains set because of the (—) On Block Storage X Write Gate line 7*e*.04 which is negative thereby preventing reset current from being supplied on the 4 line 38*c*.01 to the X Switch Core Matrix of FIG. 40 where it should reset core 28 if permitted to flow. Core 28 must be preserved in the set state until the Write portion of the 4th Execute cycle.

During Execute Cycle 3 MAC 1 is stepped —1 at R_3. In FIG. 94*c*, the Add/Sub. 1 line 74*a*.01 is up to provide a positive signal on the Step MAC 1–1 line 74*c*.03. In FIG. 93*g*, the Minus On Block Step MAC 1 line 136*b*.01 is positive since in FIG. 136*b* the Memory Read Mode line 93*q*.01 is positive but the Transition line 136.02 is negative. In FIG. 93*g*, the lines 93*g*.05 through 93*g*.09 go to MAC 1 and step it to 9008 at R_3. SAC is stepped +1 at R_3 of Execute Cycle 3 to contain the value 29. In FIGURE 136*b*, Not Transition line 136*d*.03 and Storage R/W Mode line 93*q*.06 are positive to bring up the Step SAC+1 line 136*b*.08, which goes to FIG. 93*i*, where the Step SAC+1 lines 93*i*.03 and 93*i*.04 are positive because the Minus On Block Step SAC line 136*b*.09 is positive. In FIG. 136*b*, the Storage Read Mode line 93*q*.04 is negative, and therefore, the Minus On Block Step SAC line 136*b*.09 is positive. Thus, at R_3 of Execute Cycle 3, MAC 1 contains the value 9008 and SAC contains the value 29. The Memory Address Select Register and Storage Address Select Register contain their previous contents 9009 and 28 respectively. Since the Memory Address Select Register and Storage Address Select Register are set at R_0 and the contents of MAC and SAC are not changed until R_3, MASR and SASR remain unchanged after R_3.

In FIG. 93*b*, the Minus On Block Add Trigger line **93***b*.**01** is positive since none of the inputs to the Inverter are positive. The latter is true because the input lines are associated with those instructions in which Overlap Mode Control is not employed and, therefore, for an Add operation, all of these input lines will be down. FIG. 136*a*, the NOT Transition line **136***d*.**02** is positive and the Minus On Block Add Trigger line **93***v*.**01** is positive to condition the diode gate for the fall of the A_2/R_3–W_1 line **103***b*.**23**, to turn On the Add Trigger and bring up the Add Trigger On line **136***a*.**06**. The Storage Read/Write Mode line **93***q*.**05** is up and the NOT transition line **136***d*.**02** is up to condition a diode gate for the fall of the A_3/R_4–W_2 line **103***b*.**07** to turn On the Mode Control trigger and bring up the Mode Control Trigger On line **136***a*.**08**. The Add Trigger On line **136***b*.**17** goes to the Pulse Generator of FIG. **101** where it is combined with Minus On Auto Block line **103***a*.**21**, the Use line **105.16** and the W_0 (D1) line **98.02** to provide the W_0 Add Pulse on the lines **101.08** through **101.16**. These pulses are used in the arithmetic circuits such as the Multiplicand Doubler and Quadrupler, the Quintupler, the Decimal Correction Circuits, the Decimal Carry Trigger, the Inter-Register Check Trigger and other triggers used in arithmetic operations. The Mode Control Trigger On line **136***e*.**35** goes to the Storage Read/Write Mode Control, FIG. 7*e*, where its positive signal is combined with the Storage Read/Write Mode Signal on line **93***q*.**07** and the R_0 pulse on the line **7***d*.**09** to turn On the Storage Read/Write Mode Trigger at R_0, which is the beginning of Execute Cycle 4. Storage Read/Write Mode Trigger On line **7***e*.**02** goes to Storage Write Driver Select Circuits of FIG. 41, where it is used to gate one less than the decimal value at the inputs from the 3×8 Decoder when operating in the Storage Read/Write Mode.

Execute Cycle 4 will be a Fully Overlapped cycle because the Mode Control Trigger and the Add Trigger are On throughout the cycle. Since the Add/Subtract 1 trigger is On, the cycle is NOT ECC 1/2, the Storage Mark Trigger is Off, and the Digit Adder output is $\neq 0$. Turn Off DZT is made positive again (DZT is Off). The Storage Read/Write Mode, CR 2 to T/C, Generate C Bit Out and Digit Adder Out signals are provided as in the previous cycle. With the Auxiliary Trigger 1 Off, the Memory Read Mode is specified and with the Transition trigger Off, CR 1 to Adder and Step MAC–1 are provided. With CR 1=a numeric character and Auxiliary Trigger 2 Off, Turn On Transition Trigger and Complement are not routed.

During Execute Cycle 4, Memory operates in the Memory Read Mode. The contents of Memory Addresses 9005 through 9009 are read into the Memory Buffer Register and the digit 1 of Address 9008 is selected and set to CR 1 at W_0. Thus, during the Write portion of Execute Cycle 4, CR 1 contains the digit 1, and its previous contents, the digit 5, has been passed to the Digit Adder. During the Write portion of Execute Cycle 4, the contents of Memory Buffer Register are written back into the Memory Addresses 9005 through 9009 in the conventional manner. Storage is operating in the Storage Read/Write Mode, so in Execute Cycle 4, which is a Fully Overlapped cycle, Storage Address 29 is read from, but the result of the adding of the digit 5 from CR 1 and the digit 2 from CR 2 is written into Storage Address 28 which is the address read from the previous cycle, Execute Cycle 3. During the Read portion of Execute Cycle 4, Switch Core 0 of the Y Switch Core Matrix of FIG. 39 is set in the manner previously described to provide a half-select current to the Storage Array of FIG. 45. In FIG. 40, the X Switch Core Matrix, the 7 line **38***c*.**04**, the 3 line **38***b*.**04** and the 1 line **38***b*.**02** are driven with reset current. The 24 Odd line is driven with set current which sets Switch Core 29 to the 1 state and provides half-select current on the line 29 to the Storage Array of FIG. 45. Thus, in FIG. 45, the 0 line of the Y axis is driven with half-select reset current and the 29 line on the X axis is driven with half-select reset current. Digit 3 is read into the Storage Buffer Register and set into CR 2 at W_0 in the manner previously described. Referring once again to FIG. 40, the Switch Core 28 was previously set in Execute Cycle 3 and has remained in the set condition for use during the Write portion of Execute Cycle 4. Reset current is provided on the 4 line **38***c*.**01** which switches the Core 28 to the 0 state and provides half-select outputs on the line 28 in the direction for setting the cores at Address 28 to the 1 state. In the Y Switch Core Matrix of FIG. 39, reset current is provided on the 00 line **36***b*.**01** which resets the 0 core to provide half-select set current to the Storage Array of FIG. 45. In FIG. 45, with the 0 line of the Y axis and the 28 line of the X axis energized the seven cores of Address 28 are receiving set current. However, Result Register contains the digit 7 (CBA8421=1000111) and inhibit current is provided to those Storage planes where it is desired to write "zeros," in this instance, the B, A and 8 planes. The result of this operation is that Storage Address 29 has been read, the contents thereof provided to the arithmetic circuits, and the result of computations with the digits 5 and 2 have been stored at the address read from previously which was Address 28. W_0 of Execute Cycle 4, the digits 1 and 3 are available in CR 1 and 2 respectively and are sent to the arithmetic circuits for computation during the Write portion of Execute cycle 4 and the Read portion of Execute cycle 5. The results of computations taking place during the Write portion of Execute cycle 3 and the Read portion of Execute cycle 4 have been placed in storage at Address 28. Thus, Execute Cycle 4 is a Fully Overlapped cycle.

Execute Cycles 5 and 6 are Fully Overlapped cycles and operations are identical with operations of Execute Cycle 4. In Execute Cycle 5, MASR contains 9007 and the digit 1 at this address is placed in CR 1 at W_0. MAC 1 is stepped to 9006 at R_3. SASR is set to 30 (the contents of SAC) at R_0 and this address is used to extract the digit 7 from Storage Address 30 and place this digit in CR 2 at W_0. Switch Core 30 remains set and Switch Core 29 is reset to store the sum 4 from the Result Register in Storage Address 29.

During Execute Cycle 6 MASR is set to Address 9007 at R_0, and at R_3 MAC is stepped to Address 9006. SASR is set to Address 31 at R_0, and at R_3 SAC is stepped to Address 32, which is a critical address. During the Read portion of Execute Cycle 6, the digit 2 is extracted from Memory Address 9006 and placed in CR 1 at W_0, and the digit 4 is extracted from Storage Address 31 and is placed in CR 2 at W_0. Results of computation during the Read portion of Execute Cycle 5 and the Write portion of Execute Cycle 6, namely, the result 8 of adding 7 and 1, is placed in the Result Register at R_4. The 0 Switch Core of the Y Switch Core Matrix was set during the Read portion of Execute Cycle 6, and Switch Core 30 of the X Switch Core Matrix remains set from the previous cycle. During the Write portion of Execute Cycle 6 Switch Cores 0 and 30 are reset, and the digit 8 from the Result Register is entered in Storage at Address 30. Fully overlapped cycles cease due to the recognition of the Critical Storage Address 32, and the Auto Transition trigger is turned On at W_2 of Execute Cycle 6.

In the SAC controls of FIG. 52*e*, the SAC $\overline{1}$ line **52***a*.**13**, the SAC $\overline{2}$ line **52***a*.**12**, the SAC $\overline{4}$ line **52***a*.**11**, the SAC $\overline{8}$ line **52***a*.**14** and the SAC $\overline{16}$ line **52***a*.**01** are up since SAC contains the Address 32. Accordingly, the SAC Equal Critical Address line **52***e*.**01** is positive. This signal is supplied to FIG. 136*b* where it is combined with the Storage Read/Write Mode Signal on the line **93***q*.**03** to bring up the Turn On Auto Transition Trigger line **136***b*.**05**. The signal is passed through FIG. 93*u* onto line **93***u*.**01** which goes to FIG. 136*a* where it is combined with positive signals on the Add Trigger On line

136*b*.15 and the W_2 (D1) line 102.17 to turn On the Auto Transition Trigger and bring up the Transition lines 136*a*.03 and 136*a*.04. The Transition line 136*c*.01 is up to condition the diode gate for the fall of the A_2/R_3–W_1 line 103*b*.23 which turns the Add Trigger Off and brings up the Add Trigger Off line 136*a*.05. The Transition line 136*c*.01 also conditions the diode gate for the fall of the A_3/R_4–W_2 line 103*b*.07 which turns the Mode Control Trigger Off at W_2. The Mode Control Trigger Off lines 136*a*.07 is now positive. In FIG. 7*e*, the Mode Control Trigger Off line 136*a*.07 and the R_0 (D2) line 7*b*.09 turn Off Storage Read/Write Mode Trigger and bring up the line 7*e*.01.

During the Transition cycle, Execute Cycle 7, MAC 1 and SAC are prevented from stepping in the manner previously described. In SAC, the 16, 8, 4, 2 and 1 triggers are Off and the 32 trigger is On. Since 32 refers to another block of addresses, 32 must not be set into the Storage Address Select Register, as this would cause the 32 Switch Core in the Y Switch Core Matrix of FIG. 39 to be set, and although reading of Storage is not performed during the Transition cycle, it is the reset of the switch core in the Y Switch Core Matrix which furnishes half-select current during the Write portion of the Transition cycle for writing into the address previously read from. Therefore, the setting of the Storage Select Register 128, 64 and 32 triggers is blocked which results in the contents of SASR being 0. Thus, the 0 core of the Y Switch Core Matrix, FIG. 39, is set during the Read portion of the transition cycle and reset during the Write portion of the Transition cycle. In the X Switch Core Matrix of FIG. 40, the 31 core, which was set during Execute Cycle 6, is reset during the Write portion of the Transition cycle to write the digit 6 into address 31. More specifically, in FIG. 136*b*, the Storage Read/Write Mode line 93*q*.06 and the Transition line 136*c*.02 are positive which brings down the Minus On Suppress SASR to SAC line 136*b*.07. This line goes to SASR of FIG. 53*b* where its down condition prevents the SASR 32 trigger from being turned On. Note here that the Minus On Suppress SASR to SAC line also conditions diode gates associated with the 64 and 128 triggers to prevent their setting to SAC. Entering the Transition cycle, Execute Cycle 7, CR 1 and CR 2 contain 2 and 4 respectively and are not set at W_0 as previously explained since this is a Transition cycle. The result of adding 2 and 4 is available during the Read portion of Execute Cycle 7 and is set into the Result Register at R_4. MAC 1 remains at the setting of 9005 and Memory Address Select Register is set to Address 9005 at R_0. SAC contains 32 and is blocked from stepping at R_3 and, therefore, remains at the value of 32 throughout the Transition cycle. 32 is prevented from being set in Storage Address Select Register and, therefore, its contents are 0.

At the beginning of Execute Cycle 7, SAC contains the value 32 and SAC is not stepped at R_3 as described previously. SASR contains 0 as explained previously, but Storage Address 0 is not read from during the Transition Cycle because in FIG. 7*e* the Transition line 136*c*.05 and the Storage Read/Write Mode line 93*q*.07 are up, which brings down the Minus On Block Storage X Read Gate line 7*e*.03 to Odd and Even Gating Circuits of FIG. 42 to prevent the Storage Read Gate Even line 42.04 from becoming positive. There is nothing to prevent the setting of the 0 core in the Y Switch Core Matrix of FIG. 39. And in the X Switch Core Matrix of FIG. 40, even though the 6 line 36*c*.03, the 4 line 34*c*.01 and the 2 line 38*b*.03 are driven with reset current, set current is not provided on the 0 Even line 35.01 and, accordingly, the 0 core is not set. The core 31 remains in the set condition of the previous cycle. In FIG. 41, the Storage Write Driver Select Circuits, the Decimal 0 line 34*d*.01 is now positive since SASR contains 0. The Storage Read/Write Mode Trigger is On and the line 7*e*.01 is positive. Therefore, the 7 line 41.08 is up and goes to the Storage X Switch Core Write Drivers of FIG. 38*c* where it is gated by the Storage X Write Gate on line 7*e*.04 and the Storage Write Gate line 7*d*.07 to provide an output on the 7 line 38*c*.04. In FIG. 40, the column of cores driven by the line 38*c*.04 are driven with reset current. The 31 core is the only one in the set state, and it will be reset to provide half-select set current to the Storage Array of FIG. 45. FIG. 45, the 0 line of the Y axis and the 31 line of the X axis drive the 7 cores of address 31 with set current. However, the Result Register contains the digit 6 (CBA8421=0000110) and for those planes which are to contain "zeros," inhibit current is provided in the manner described previously. Accordingly, "ones" are set into the 4 and 2 planes and "zeros" are set in the C, B, A, 8 and 1 planes.

It is during the Write portion of Execute Cycle 7 that the Add Trigger, Mode Control Trigger, Storage Read/Write Mode Trigger are turned Off as previously described (see FIG. 151). In addition, the Auto Transition Trigger is turned Off by a positive signal on the Add Trigger Off line 136*d*.18, the positive signal on the W_2 (D1) line 102.17.

The Add operation was interrupted upon recognition of the critical address, the Transition cycle was taken in order to refer to a different group of addresses on the subsequent cycle, and the Add operation may now be resumed in Execute Cycle 8. At the beginning of Execute Cycle 8, CR 1 contains the digit 2 and CR 2 contains the digit 4, the digits which were used previously to compute the result 6. MAC 1 contains 9005, MASR contains 9005, SAC contains 32 and SASR contains 0. At R_0, the contents of SAC are set into SASR which then contains address 32 throughout the Start cycle. During the Read portion of Execute Cycle 8, Memory addresses 9009 through 9005 are read from as described previously. However, in this instance the digit 3 is set into CR 1 at W_0. At R_3, MAC 1 is permitted to step down 1 resulting in address 9004. Since Execute Cycle 8 is a Start cycle, all of the switch cores in the X Switch Core Matrix of FIG. 40 are in the reset condition and the digit 1 will be read from address 32 of Storage, which is accomplished by setting the 32 core of FIG. 39, the Y Switch Core Matrix, and the 0 Even Core of the X Switch Core Matrix of FIG. 40. Writing into Storage is prohibited during a Start cycle. Consequently, the set state of the 0 Even core of FIG. 40 is preserved for writing into address 32 during Execute Cycle 9. In FIG. 136*a*, the Add trigger is turned On at W_1 by positive signals on the NOT Transition line 136*d*.02 and Minus On Block Step Add Trigger line 93*z*.01 and the fall of the A_2/R_3–W_1 line 103*b*.23. Next, the Mode Control Trigger is turned On at W_2 by positive signals on the NOT Transition line 136*d*.02, Storage Read/Write Mode line 93*q*.03 and the fall of the A_3/R_4–W_2 line 103*b*.07. At R_0, the Storage Read/Write Mode Trigger of FIG. 7*e* is turned On by the positive signals on the Mode Control Trigger On line 136*e*.35, Storage Read/Write Mode line 93*q*.07 and R_0 (D2) line 7d.09. During the Start cycle, Execute Cycle 8, it was the Storage Read/Write Mode Trigger Off line which inhibited the Storage X Write Gate on the line 7*e*.04, and in Execute Cycle 9 a Fully Overlapped cycle, this line becomes positive to permit writing into Storage.

Since SASR contains 33 during Execute Cycle 9, the 32 core of the Y Switch Core Matrix, FIG. 39, is set during Read time and the 1 Switch Core of the X Switch Core Matrix of FIG. 40 is set by reset current flowing through the 3 line 38*b*.04, the 5 line 38*c*.02 and the 7 line 38*c*.04 while set current flows through the 0 Odd line 35.05. In FIG. 45, the 32 line of the Y axis and the 1 line of the X Axis are driven with half-select reset current so that the digit 2 is read from Storage Address 33 and set into CR 2 at W_0. Accordingly, at W_0 of Execute cycle 9, the 32 core of the Y Switch Core Matrix,

FIG. 39, and the 0 and 1 cores of the X Switch Core Matrix of FIG. 40, are in the set condition.

At R_0 of Execute Cycle 9, MASR was set to 9004 which was contained in MAC 1. Normal Memory Read Mode operation prevails and the character at address 9004, which is a 4, is set in the CR 1 at W_0 of Execute Cycle 9. At R_4, the results of adding the digits 3 and 1 are set into the Result Register which then contains the digit 4. To read the digit 4 into Storage address 32 refer to the Storage Write Driver Select Circuits of FIG. 41 where the Decimal 1 line **34***d*.**02** is positive. The Storage Read/Write Mode Trigger On line **7***e*.**01** is positive and an output is provided on the 0 line **41.01** to FIG. 38*b* where it is gated by the Storage X Write Gate on the line **7***e*.**04** and the Storage Write Gate on the line **7***d*.**06**, to drive the 0 line **38***b*.**01** with reset current. In FIG. 40, the 0 core is reset to provide half-select set current on its secondary winding. FIG. 39, the 32 Switch Core is reset by current on the 32 line **36***b*.**02** which then provides half-select set current on the secondary of core 32. In FIG. 45, the 32 line of the Y axis and the 0 line of the X axis are driven and all 7 planes of address 32 receive current tending to set them in the "1" state. A Result Register contains the digit 4 (CBA8421=1000100), and in those planes where "zeros" are desired, inhibit current is furnished which prohibits the setting of these cores in the "1" state.

Two more Fully Overlapped cycles follow, Execute Cycles 10 and 11, as shown in the sequence chart of FIG. 151. In Execute Cycle 10, MASR is set to 9003 at R_0 and MAC 1 is reduced to 9002 at R_3, SASR is set to the contents of SAC 34, and at R_3, SAC is advanced to the value 35. Memory addresses 9004 through 9000 are read from and written into during Execute Cycle 10 and the digit 6 at Memory address 9003 is set into CR 1 at W_0. The digit 1 is read from Storage Address 34 and is set in CR 2 at W_0. At R_4, the result 6 (of adding 4 and 2) is set into the Result Register and thereafter written into Storage Address 33.

In Execute cycle 11, MASR is set to 9002 at R_0, and MAC 1 is stepped to 9001 at R_3. Memory operations in the Memory Read Mode prevail, and at W_0, the digit A is set into CR 1. Since addition proceeds until a non-numeric character is sensed, it is the digit A which will initiate the End operation sequence. At R_0 of Execute Cycle 11, SASR is set to address 35, at R_3 SAC is advanced to the value 36. The digit 7 is read from Storage Address 35 and is set into CR 2 at W_0. The Result 7 (of adding 6 and 1) is set into the Result Register at R_4, and during the Write portion of Execute Cycle 11 the digit 7 is written into address 34. After W_0 of Execute Cycle 11, CR 1 contains the character A (CBA8421=1110001) and outputs of CR 1 are provided to CR 1 Recognition Circuits of FIGS. 71*a* and *b*. FIG. 71*a*, the CR 1–$\overline{8}$ line **59.28**, the CR 1–$\overline{4}$ line **59.33**, the CR 1–$\overline{2}$ line **58.53**, CR 1–1 line **58.53**, CR 1–A line **58.34**, and CR 1–B line **58.19** are positive. These circuits detect the presence of special characters, and A (decoded) provides an output on the CR 1 Not Equal Special Character lines **71***a*.**12** and **71***a*.**13** since the CR 1 Equal Special Character line **71***a*.**14** is down. In FIG. 71*b*, CR 1 Not Equal Special Character line **71***a*.**13**, the CR 1–$\overline{2}$ line **59.39**, the CR 1–1 line **58.54**, the CR 1–$\overline{4}$ line **59.34**, the CR 1–B line **58.19**, the CR 1–$\overline{8}$ line **59.29** and the CR 1–$\overline{C}$ line **58.02** are up. The CR 1 Equal Numeric line is down, therefore, the CR 1 Not Equal to Numeric lines **71***b*.**05** to **71***b*.**09** are positive. In FIG. 74*e*, the Add/Subtract 1 line **74***a*.**04**, the Auxiliary Trigger 1 Off line **138***j*.**19** and the CR 1 Not Equal to Numeric line **71***b*.**05** are positive which bring up the Turn On Transition Trigger line **74***e*.**03**. The Turn On Transition Trigger line goes to FIG. 93*m*, and the signal is transferred to the line **93***m*.**04** which goes to FIG. 136*a*. FIG. 136*a*, the Turn On Transition Trigger line **93***m*.**04** and Add Trigger On line **136***d*.**15** are positive, and at W_2, the W_2 (D1) line **102.17** becomes positive to turn On the Transition Trigger to provide positive outputs on the lines **136***a*.**02**–**136***a*.**04**.

In FIG. 74*b*, the Add/Subtract 1 line **74***a*.**02**, the Transition Trigger On line **136***e*.**03** and the NOT ECC 1/2 line **124.18** are positive. However, the SMT On line **138***c*.**13** is negative and prevents the End of Addition lines from becoming positive. In FIG. 74*f*, the Add/Subtract 1 line **74***a*.**05**, the NOT ECC 1/2 line **124.19**, the Transition Trigger On line **136***e*.**04** are positive to bring up the Turn On Auxiliary Trigger 1 line **74***f*.**05**. The latter line provides a signal to FIG. 93*k* which is passed to the Turn On Auxiliary Trigger 1 line **93***k*.**01**. In FIG. 138*i*, the Turn On Auxiliary Trigger 1 line **93***k*.**01** conditions a diode gate for the pulse at W_2 on the line **103***b*.**15** to turn On Auxiliary Trigger 1 at W_2 of Execute Cycle 12. In FIG. 74*f*, the Storage Read/Write Mode was maintained by Add/Subtract 1 line **74***a*.**05** and either Auxiliary Trigger 1 Off line **138***j*.**20** or Storage Mark Trigger Off line **138***d*.**17**. When the Auxiliary Trigger 1 Off line **138***j*.**20** goes negative at W_2 Storage Read/Write Mode is maintained by either SMT Off line **138***d*.**17** or the Transition line **136***c*.**09**. In FIG. 74*d*, Add/Subtract 1 line **74***a*.**03** and SMT Off line **38***d*.**06** make positive the Digit Adder Out line **74***d*.**04** and the CR 2 to T/C line **74***d*.**05**. The Memory Read Mode line **94***d*.**01** is positive during Execute Cycle 12 by Auxiliary Trigger 1 Off line **138***j*.**18** and Add/Subtract 1 line **74***a*.**03** until the Auxiliary Trigger 1 Off line falls at W_2. Therefore, the Memory Read Mode is in effect during Execute Cycle 12, and Addresses 9000 through 9004 are read into the Memory Buffer Register and returned to Memory from the Memory Buffer Register during Execute Cycle 12. However, CR 1 does not receive a set pulse at W_0. Since Execute Cycle 12 is a Transition cycle, address 36 is not read from although the 32 core of the Y Switch Core Matrix of FIG. 39 is set. Switch core 3 of the X Switch Core Matrix of FIG. 40 is in the set condition from the previous cycle and will be used during the Write portion of Execute Cycle 12 to read into address 35. Note that the Memory field is smaller than the Storage field and that computations may cease when the 6 and 1 have been added since the 4, 5 and 7 in the high order positions of the Storage field are not affected in any way and a decimal carry is not provided by the addition of 6 and 1. The 7 of the Storage field must remain unaltered. In Execute Cycle 11 the result of adding 6 and 1 was stored in address 34 and the digit 7 from address 35 was placed in CR 2 at W_0 of Execute Cycle 11. Since it takes a portion of a cycle to detect that CR 1 is Not Equal to a number, operations cannot cease until one cycle after the result 7 has been placed in address 34. Therefore, in cycle 12 the digit 7 in CR 2 is transferred by way of the True/Complement controls to the Digit Adder, and the contents of CR 1, the digit A are blocked by the CR 1 to Adder line being down. Therefore, the Storage digit 7 passes unmodified through the Adder and is set into the Result Register at R_4 of Execute Cycle 12. Address 36 is not read from during the Transition cycle, but during the Read portion of the Execute Cycle 12, the 32 core of the Y Switch Core Matrix of 39 is set and the 3 core of the X Switch Core Matrix of FIG. 40 is in the set condition from the previous cycle. The switch core 4 is not set during the Read portion of the cycle because the Zero Even line **35.01** is not driven with set current. In FIG. 41, the Decimal 4 line **34***d*.**05** is positive; however, the Storage Read/Write Mode Trigger On line **7***e*.**01** provides an output on the 3 line **41.04** which is effective during the Write portion of Execute cycle 12 to reset the core 3 of the X Switch Core Matrix of FIG. 40. Therefore, the contents of the Result Register are placed in Storage Address 35 during the Write portion of Execute Cycle 12 unmodified by the addition circuits. In FIG. 136*a*, the Add trigger is turned Off by the Transition line **136***c*.**01** and the A_2/R_3–W_1 line **103***b*.**23**, and the Mode

Control trigger is turned Off by the Transition line **136***c*.**01** and the A_3/R_4–W_2 line **103***b*.**07**. Then, at W_2, the Transition trigger is turned Off by the Add Trigger Off line **136***d*.**18** and the W_2 (D1) line **102.17**. In FIG. 7*e*, Storage Read/Write Mode Control trigger is turned Off by the Mode Control Off line **136***e*.**37** and the R_0 line **7***d*.**09**.

In FIG. 74*g*, positive signals on Add/Subtract 1 line **74***a*.**06**, Transition Trigger On line **136***e*.**05**, No Decimal Carry Out line **88.12**, NOT ECC 1/2 line **124.20** and SMT Off line **138***d*.**18** provide a positive output from the Cascaded AND circuit to condition another AND circuit fed by positive signals on the Digit Adder Output Not Equal to Zero line **87.22** and Auxiliary Trigger 2 Off line **138***l*.**22** to bring up the End E Time line **94***g*.**03**. In FIG. 93*r*, the End E Time lines **93***r*.**01** through **93***r*.**06** are made positive. The line **93***r*.**06** goes to the I/E trigger of FIG. 121 where it conditions a diode gate for the fall of the A_3/R_4–W_2 line **104.10** which switches the I/E trigger from E time to I time at W_2 thereby defining the next cycle as an Instruction cycle in which the next instruction is taken from address 0009 as indicated by the Instruction Counter contents.

EXAMPLE OF ADD ADDRESS TO MEMORY

The instruction Add Address to Memory (AAM) adds a five-character field in Storage to a four-character field in Memory. The addition is non-algebraic (signs ignored). The numerical portions of the first four low order digits in the Storage field addressed are added to the numerical portion of the four characters of the four-character field in Memory. The "1" and "2" bits of the highest order digit (ten-thousands order) in the Storage field is added by means of the Zone adder to the A and B bits of the thousands order of the Memory field, respectively, and the "4" bit is added to the B bit of the units order of the Memory field. The A bit of the thousands order of the Memory field is assigned an address weight of 10,000, the B bit of the thousands order is assigned a weight of 20,000, and the B bit of the units order of the Memory field is assigned a weight of 40,000. Taken together these bits form a BCD digit equivalent to the ten-thousands order of the Memory field since the maximum value that can be expressed in the four orders of the BCD notation is 9,999. By using the 4, 2 and 1 bits as described above as the ten-thousands order the maximum value that can be expressed is increased to 79,999 which is adequate for addressing Core Memory of this Data Processing System which has a capacity of 80,000 characters.

The zone bits over the tens and hundreds orders of the Memory field (the ASU designation) are added in binary fashion with the zoning of the corresponding orders of the Storage field. The addition of these zone bits is independent of Zone addition of the other orders and any carry from the hundreds order is ignored.

To execute this instruction the numeric portions of the units orders of the Memory and Storage fields are added together and the carry out, if any, is applied to the numeric portion of the tens orders. The sum is placed in the units order of the Memory field. The numeric portions of the tens orders and the carry in, if any, from the units order are added and the carry, if any, is applied to the numeric part of the hundreds orders. The Zone bits (ASU coding) of the tens orders are added as binary numbers and the carry out, if any, is applied to the Zone bits of the hundreds orders. The sums are placed in the tens orders of the Memory field. The numerical portion of the hundreds orders and the carry in, if any, are added and the carry out, if any, is applied to the thousands orders. The Zone bits of the hundreds orders and the carry in, if any, for the tens order are added together as binary numbers, and any carry out is ignored. The sums are placed in the hundreds orders of the Memory field. The numeric portions of the thousands orders and the carry in, if any, from the hundreds order are added and the carry, if any, is retained for use as described below. The 1 and 2 bits of the ten-thousands order of the Storage field and the A and B bits of the addition of the numeric portion of the thousands orders are added. The sum of the numeric portions of the thousands orders and the sum of the 1 and 2 bits of the ten-thousands order of the Storage field and the A and B bits of the thousands order of the Memory field are placed in the thousands order of the Memory field as numeric and zone bits respectively. If there is a 4 bit in the ten-thousands order of the Storage field or if there is a carry in from the zone addition (immediately above), but not both, the state of the B bit in the units order of the Memory field is reversed. If there is neither a 4 bit nor a carry in or both a 4 bit and a carry in, execution operations cease.

The address of the Memory field must end in either a 4 or a 9. If the addressed Storage field is greater than five digits, only the first five low order digits are used and the remainder is ignored. The field in Storage may be less than five digits if desired. A "one" in the A bit position of the units order of the Memory field, indicating an indirect address, is unaffected by the AAM instruction.

In this example the Add Address to Memory instruction has the following format:

Character		0	1	2	3	4		
			0	0	0	4		
			or					
			C	B	A	8	4	2	1
Character	0		0	0	0	1	1	0	0
Character	1	0	0	0	0	1	0	1	0
Character	2	0	0	0	0	1	0	1	0
Character	3	0	0	0	0	1	0	1	0
Character	4	4	1	0	0	0	1	0	0

The operations part @, specifies Add Address to Memory, the numeric portions of characters 1 through 4 contain the address of the augend, and absence of B and A bits in characters 2 and 3 specify that the addend is contained in Accumulator Storage. Let character 4 of the instruction be located at address 00009.

At the Memory address specified by the AAM instruction shall be

	1	1	1	0	— B
	1	0	0	1	— A
G	9	4	3	2	

or more specifically

Character		C	B	A	8	4	2	1
0	G	1	1	1	0	1	1	1
1	9 and B & A bits	0	1	1	1	0	0	1
2	4 and B & $\overline{A}$ bits	0	1	0	0	1	0	0
3	3 and B & $\overline{A}$ bits	0	1	0	0	0	1	1
4	2 and $\overline{B}$ & A bits	0	0	1	0	0	1	0

The numeric portions of characters 1 through 4 specify address 9432 and the zone portions of characters 1 and 4 specify 30,000 since

Character 1	A — 10, 000
Character 1	B — 20, 000
Character 0	$\overline{B}$ — 00, 000
	30, 000

The Memory address is therefore, 39,432.

The zone portions of characters 2 and 3 specify Auxiliary Storage Unit 10 as follows:

	B bit, Character 2	A bit, Character 2	B bit, Character 3	A bit, Character 3
Binary state	1	0	1	0
BCD value	8	4	2	1

Having binary "ones" in the 8 and 2 positions results in the decimal number 10.

At the Accumulator Address specified by the AAM instruction shall be

		0	1	−B
		0	1	−A
a	1	2	3	45

The SPC shall contain the address 27 which refers to the units order of the Storage field. The address and bit format of the Storage field is as follows:

Address	Contents	C	B	A	8	4	2	1
27	5	0	0	0	0	1	0	1
28	4	1	1	1	0	1	0	0
29	3	0	0	0	0	0	1	1
30	2	1	0	0	0	0	1	0
31	1	1	0	0	0	0	0	1
32	a (SM)							

The numeric portions of the characters in Accumulator Storage addresses 27 through 31 specify the number 1 2 3 4 5 to be added to the Memory Address 38,432.

The zone portions of the characters at Storage addresses 28 and 29 specify Auxiliary Storage Unit 3 as follows:

	B bit, address 29	A bit, address 29	B bit, address 28	A bit, address 28
Binary State	0	0	1	1
BCD value	8	4	2	1

Having binary "ones" in the 2 and 1 positions results in the decimal number 3.

The result of adding 39,432 and 12,345 is 51,777 and the result of adding ASU coding of 10 and 3 is 13. To better understand the adding of the ASU zone bits consider the following:

10=1010 (zones of characters 2 and 3)
3=0011 (zones of Storage Addresses 28 & 29)

13=1101

The result stored in addresses 0000 and 0004 of Memory will be

	0	1	0	1	−(B)
	1	1	1	1	−(A)
G	1	7	7	7	

More specifically:

	C	B	A	8	4	2	1
G	1	1	1	0	1	1	1
1 and $\overline{B}$ & A bits	0	0	1	0	0	0	1
7 and B & A bits	1	1	1	0	1	1	1
7 and $\overline{B}$ & A bits	0	0	1	0	1	1	1
7 and B & A bits	1	1	1	0	1	1	1

During the Read portion of the Instruction cycle, Memory Address 00009 is interrogated and the Add to Memory Instruction extracted and placed in the Memory Buffer Register at $R_{3,5}$. At A_0, the contents of character 0 position of the Memory Buffer Register is set into the Operations Register. The Zone portions of characters 2 and 3 of MBR are set into the Storage Select Register of FIG. 16*a*, CR 1 is set to the contents of character 4 position of MBR, and at A_1 the Memory address portion of the instruction, namely 00004, is placed in MAR.

In FIG. 101, the Use line **105.16**, the Indirect Address Trigger Off line **121.07**, the A_0 (D1) line **97.02** provide an A_0I Time 1 Use signal on the lines **101.24** through **101.26** to furnish A_0 Set pulses to the Storage Select Register of FIG. 16*a* and to the Operation Register of FIGS. 21*a* and *b*.

In the Operations Register of FIG. 21*a*, MBR character 0–1 line **14***b*.**02** is down, the MBR character 0–2 line **14***b*.**02** is down, the MBR character 0–4 line **14***b*.**02** is up and MBR 0–8 line **14***b*.**02** is up and the A_0 pulse on the I Time 1 Use line **101.26** turns On the 8 and the 4 triggers. The 2 and the 1 triggers remain Off indicating "zeros" since they were Instruction reset at R_0 of the Instruction cycle.

The MBR character 0–A line **14***b*.**02**, the MBR character 0–B line **14***b*.**02** and MBR character 0–C line **14***b*.**02** are down and the C, B and A triggers remain in the Off condition as reset at R_0 of the Instruction cycle. The Operation Zone Decoder of FIG. 23*a*, the Op. Register $\overline{A}$ line **21***b*.**01** and the Op. Register $\overline{B}$ line **21***b*.**03** are up and condition the negative AND circuits to bring up the Minus Operation Register −AB lines **23***a*.**01** through **23***a*.**10**. In the Operation Decoder of FIG. 23*l*, the Minus Operation Register $-\overline{A}-\overline{B}$ line **23***a*.**21** is down. The Operation Register −1 line **21***a*.**11**, Operation Register −2 line **21***a*.**22**, Operation Register $-\overline{4}$ line **21***a*.**27** and Operation Register $-\overline{8}$ line **21***a*.**37** are negative. Therefore, the Add Address to Memory lines **231.05** through **231.07** are positive by way of the Inverter. Add Address to Memory line **231.05** goes to FIG. 64*a* where it is used in combination with the E Time line which is made positive later to provide routing for Add Address to Memory Controls. The Add Address to Memory line **231.06** goes to FIG. 24 where it is used with the Op. Register −C line **21***b*.**06** to prevent operations check. The Add Address to Memory line **231.07** goes to FIG. 60 where it is used in the Instruction Check circuits.

Since the zones are 0 in the units and hundreds orders of the Instruction, the Storage Select Register of FIG. 16*a* contains "zero." That is, all of the triggers have their left plates up providing signals SSR–8 Off, SSR–4 Off, SSR–2 Off and SSR–1 Off on the output lines. In the Storage Select Register Decoding of FIG. 54, the SSR–1 On line **16***a*.**24**, SSR–2 On line **16***a*.**17**, SSR–4 On line **16***a*.**16** and SSR–8 On line **16***a*.**03** are down. Therefore, SSR–0 lines **54.10** through **54.23** are positive. In the SAC Controls of FIG. 52*e*, the SSR–000 line **54.10** is positive. The set SAC to SPC line **73***j*.**08** is positive during Instruction Time. The I Time line **124.33** is positive and the A_2/R_3–W_1 (Use) line **103.05** provides an output on the Set SAC to SPC pulse lines **52***e*.**04** and **52***e*.**05**. In FIGS. 52*b* and *d*, the SPC–1 line **51***a*.**02**, the SPC–2 line **51***a*.**04**, the SPC–8 line **51***a*.**08**, the SPC–$\overline{4}$ line **51***a*.**05**, the SPC–16 line **51***b*.**04**, the SPC–$\overline{32}$ line **51***b*.**05**, the SPC–$\overline{64}$ line 51*c*.**01** and the SPC–$\overline{128}$ line **51***c*.**03** are positive to condition diode gates associated with each of the SAC triggers. The fall of the Set SAC to SPC pulse lines **52***e*.**05** and **52***e*.**04** turn On the SAC 1, 2, 8 and 16 triggers and turn Off the 4, 32, 64 and 128 triggers if they are On. Therefore, SAC now contains the address of the units order of the Storage field. The Memory Address Register contains the address of the units order of the Memory field, namely, 0004. Character 4 of the Memory Buffer Register is selected by the Memory Out Switch of FIGS. 20*a* through *d*, and the digit 4 is presented at the inputs of the 1st order of MAR in FIG. 17*a*. The Memory Out Bus–8 line **20***d*.**04** is down, the Memory Out Bus–4 line **20***d*.**05** is up, the Memory Out Bus–2 line **20***b*.**06** is down and the Memory Out Bus–1 line **20***b*.**07** is down. The Block Set First Order MAR line **17***f*.**07** is positive since in FIG. 17*f*, the Memory Out Bus–2 line **20***d*.**06** and the Memory Out Bus–8 line **20***d*.**04** are negative. At A_1 the A_1 (D.04) Use line **101.19** turns On the 4 trigger of the 1st order of MAR. The 8, 2 and 1 triggers remain Off as reset. Accordingly, the MAR–$\overline{8}$ lines **17***a*.**01** and **17***a*.**02**, the MAR–$\overline{4}$ lines **17***a*.**11** through **17***a*.**16**, MAR–$\overline{2}$ lines **17***a*.**17** and **17***a*.**18** and the MAR–$\overline{1}$ lines **17***a*.**25** and **17***b*.**26** are positive. In the 2nd Order of MAR, FIG. 17*b*, the MBR character 3–8 line **14***a*.**02** is positive, the MBR character 3–4 line **14***a*.**02** is negative, the MBR character 3–2 line **14***a*.**02** is positive and the MBR character 3–1 line **14***a*.**02** is negative. Since the 8 and 2 lines are

positive this indicates a "0" expressed as a 10 and therefore this digit must be converted to all "zeros." In FIG. 17*f*, the MBR character 3–2 and MBR character 3–8 lines are positive so the Block Set 2nd Order MAR line **17***f*.**08** is down. In FIG. 17*b*, the Block Set 2nd Order MAR line **17***f*.**08** blocks the 8 and 2 bits and therefore the A_1 Use pulse on the line **101.20** is of no effect and all of the triggers of the 2nd Order of MAR remain Off as reset. The NOT output lines are positive. In the 3rd Order of MAR, FIG. 17*c*, MBR character 2–8 line and the MBR character 2–2 line are up and are blocked by the Block Set 3rd Order MAR line **17***f*.**09** since the MBR character 2–2 and MBR character 2–8 lines are positive in FIG. 17*f*. Accordingly, all of the triggers of the 3rd Order of MAR remain Off and the NOT lines are positive. The 4th Order of MAR, FIG. 17*d*, has the MBR character 1–8 line and the MBR character 1–2 line positive. The Block Set 4th Order MAR line **17***f*.**10** is negative since in FIG. 17*f* MBR character 2–2 and MBR character 2–8 lines are positive. Therefore, the triggers remain in the Off condition and the Not lines are positive. No zoning was present in the units and thousands orders of the Instruction and therefore in the 5th Order of MAR, FIG. 17*e*, MBR character 1–A line, MBR character 1–B line, MBR character 4–B line are down. The triggers remain Off and the NOT lines remain positive. Therefore, at A_1 MAR is set to the Memory Address 0004.

In FIG. **93***j* the **64***b*.**01** line is positive from the Add Address to Memory Instruction, and therefore the Set MAC 1 to MAR line **93***j*.**09** is positive. In the MAC 1 controls of FIG. 30*f*, the Set MAC 1 to MAR line **93***j*.**09** is used to gate, the MAR to PCT line **135***b*.**06**, the I Time line **124.32** and the A_2R_3–W_1 Use line **103.05** to make positive the Set MAC 1 to MAR lines **30***f*.**07** and **30***f*.**11** from A_2 to W_1. In the 1st Order of MAC 1, FIG. 30, the MAR–$\overline{8}$ line **17***a*.**01**, the MAR–4 line **17***a*.**14**, the MAR–$\overline{2}$ line **17***a*.**17**, the MAR–$\overline{1}$ line **17***a*.**25** are positive and the fall of the Set MAC 1 to MAR line **30***f*.**07** at W_1 turns On the 4 trigger and turns Off the 8, 2 and 1 triggers if On previously. For the 2nd, 3rd, 4th and 5th Orders of MAC 1, in FIGS. 30*b* through e respectively, the NOT inputs from MAR are positive. Accordingly, the fall of the Set MAC 1 to MAR lines **30***f*.**08**, **30***f*.**09**, **30***f*.**10** and **30***f*.**11** turn Off any of the triggers that were On. As a result MAC 1 contains the Memory Address 0004.

In the I Time Routing Controls, FIG. 61, the Use line **105.09**, the I Time line **124.29** and the CR 1–$\overline{A}$ line **59.21** are positive to bring up the End I Time Use lines **61.01** through **61.05**. The line **61.03** goes to the I/E trigger of FIG. 121 where it conditions a diode gate for the fall of the A_3R_4–W_2 line **104.10** which switches the I/E trigger from I to E and brings up the E Time line **21.02**. The end I Time line **61.04** goes to ECC 1 and 2 triggers of FIG. 120 where it conditions a diode gate for the fall of the A_3/R_4–W_2 line **102.03** to turn On the ECC 1 trigger and bring up the ECC 1 line **122.03**, and the ECC 1/2 line **122.05**. At W_3, the Memory Buffer Register and Storage Buffer Register are reset to 0.

At R_0 the Memory Address Select Register is set to the contents of MAC 1 and the Storage Address Select Register is set to the contents of SAC. In FIG. 49*b*, the MAC 1–8 line **30***a*.**03** is down, the MAC 1–4 line **30***a*.**07** is up, the MAC 1–2 line **30***a*.**10** is down, the MAC 1–1 line **30***a*.**13** is down. The Set MASR to MAC 1 line **93***s*.**02** is up and therefore the $\overline{8}$ line **49***b*.**01**, the 4 line **49***b*.**04**, the $\overline{2}$ line **49***b*.**05** and the $\overline{1}$ line **49***b*.**07** is up. In FIG. 49*a*, the 1st Order of MASR the $\overline{8}$ line **49***b*.**02**, the 4 line **49**b.**04**, the $\overline{2}$ line **49***b*.**05** and the $\overline{1}$ line **49***b*.**07** condition diode gates for the R_0 pulse on the line **101.01** to turn On the MASR 4 trigger and turn Off the 8, 2, and 1 triggers if On. The setting of the 2nd, 3rd, 4th and 5th orders of MASR will not be described in detail since the contents of MAC 1 are "zero" for these orders or for corresponding orders of MASR, the input lines of MAC 1 are all negative. Therefore, the tens, hundreds, thousands and ten thousands order of MASR will be set to 0 and the $\overline{80}$, $\overline{40}$, $\overline{20}$, $\overline{10}$, $\overline{800}$, $\overline{400}$, $\overline{200}$, $\overline{100}$, $\overline{8000}$, $\overline{4000}$, $\overline{2000}$, $\overline{1000}$, $\overline{10,000}$, $\overline{20,000}$, and $\overline{40,000}$ are positive.

In the Storage Address Select Register of FIGS. 53*a* and *b*, the SAC–1 line **52***a*.**02**, the SAC–2 line **52***a*.**04**, the SAC–$\overline{4}$ line **52***a*.**05**, the SAC–8 line **52***a*.**08**, the SAC–16 line **52***c*.**03**, the SAC–$\overline{32}$ line **52***c*.**04**, the SAC–$\overline{64}$ line **52***b*.**06** and the SAC–$\overline{128}$ line **52***b*.**08** are positive. The Minus On Suppress SASR to SAC line **136***b*.**07** is positive since the critical address in Storage has not been sensed and the R_0 (D0.4) line **101.07** goes positive to set the Storage Address Select Register to the contents of SAC. Accordingly, the 16, 8, 2 and 1 triggers are On providing positive signals on the SASR–1 line **53***a*.**02**, the SASR–2 line **53***a*.**04**, the SASR–8 line **53***a*.**08**, and the SASR–16 line **53***b*.**02**. The 4, 32, 64 and 128 triggers are Off providing positive signals on the SASR–$\overline{4}$ line **53***a*.**05**, the SASR–$\overline{32}$ line **53***b*.**03**, the SASR–$\overline{64}$ line **53***b*.**05** and the SASR–$\overline{128}$ line **53***b*.**07**. The contents of MASR are now 0004 and the contents of SASR are now 27. These addresses will be used during the Read portion of ECC 1 to extract characters from Memory for the first Execute operation of Add Address to Memory.

Referring now to the Add Address to Memory Routing Controls of FIG. 64*a*, the Add Address to Memory line **231.02** is formerly described and the E Time line **123.11** is up, accordingly, the Memory Read/Write Mode line **64***a*.**01**, CR 1 to Adder line **64***a*.**02**, and Digit Adder Out line **64***a*.**03** are up. Also, Add Address to Memory lines **64***a*.**04**, **64***a*.**05**, and Generate C Bit Out line **64***a*.**06** step SAC+1 line **64***a*.**07** are up. The Storage Read Mode is specified by positive signal on the line **64***a*.**08** since Auxiliary Trigger 2 Off line **138***l*.**14**, SMT Off line **138***b*.**12**, Add Address to Memory line **23***l*.**02** and E Time line **123.11** are positive. Suppress Zone Carry In line **64***a*.**10** is positive since Add Address to Memory line **23***l*.**02**, E Time line **123.11** and ECC 1/2 line **124.05** are positive. In FIG. 64*c*, Step MAC–1 line **64***c*.**02** is positive since Add Address to Memory 1 line **64***a*.**05** and Auxiliary Trigger 1 Off line **138***j*.**15** and Transition Trigger Off line **136***e*.**32** are positive. The CR 2 to T/C line **64***c*.**03** is positive since AAM 1 line **64***a*.**15** and Auxiliary Trigger 1 Off line **138***j*.**15** are positive. Since Memory Read/Write Mode and Storage Read Mode are specified, subsequent operations will be governed by these modes. Therefore, when reading and writing from Memory and Storage are described the result of the addition of the Memory and Storage fields will replace the contents of the Memory field.

Refer now to the Memory 4×10 Decoder of FIG. 3*b* where the $\overline{20,000}$ line **49***i*.**04**, the $\overline{80}$ line **49***c*.**01**, $\overline{40}$ line **49***c*.**04**, the $\overline{20}$ line **49***c*.**07** are positive. Thus, the 00 output lines **3***b*.**01** and **3***b*.**02** are positive. In FIG. 5*a*, the 00 line **3***b*.**01** is positive, therefore, the $\overline{00}$ line **5***a*.**02** is negative and the 00 line **5***a*.**01** is positive. Since none of the other input lines are positive, the NOT output lines, $\overline{20}$ line **5***a*.**04** through $\overline{20,080}$ line **52.20** are positive, and their complements 20 line **5***a*.**03** to 20,080 line **5***a*.**19** are negative. In FIGS. 5*b* and *c*, the Memory Read Bias Gate on the lines **5***g*.**09** and **5***g*.**18** goes positive at R_0 to drive the 00 line **5***b*.**01**, the 20 line **5***b*.**02**, the 40 line **5***b*.**03**, the 60 line **5***b*.**04**, the 80 line **5***b*.**05**, the 20,000 line **5***c*.**01**, the 20,020 line **5***c*.**02**, the 20,040 line **5***c*.**03**, the 20,060 line **5***c*.**04** and the 20,080 line **5***c*.**05**. In FIG. 8, the Y Switch Core Matrix, all of the lines linking columns of cores are being driven with reset current except for the 00 line **5***b*.**01**. In the Memory 6×8 Decoder of FIG. 3*b*, the $\overline{10,000}$ line **49***i*.**01**, the $\overline{10}$ line **49***c*.**10**, the $\overline{8}$ line **49***a*.**01**, the $\overline{1}$ line **49***a*.**14**, the $\overline{2}$ line **49***a*.**10** and the 4 line **49***a*.**07** make positive the 0–4 lines **3***b*.**01** and **3***b*.**02** to the X Switch Core Write Drivers of FIG. 7*a*. In the

latter figure, since the 0–4 line **3***b*.**01** is positive, the $\overline{0\text{–}4}$ line **7***a*.**02** is down and the 0–4 line **7***a*.**01** is up. Since none of the other input lines are positive all of the NOT lines $\overline{5\text{–}9}$ line **7***a*.**04** through $\overline{10{,}015\text{–}10{,}019}$ line **7***a*.**16** are positive. Their complements, the 5–9 line **7***a*.**03** through 10,015–10,019 line **7***a*.**15** are down. In FIGS. 7*b* and *c*, the Memory Read Bias Gate comes up at $R_{0.5}$ as the 5–9 line **5***b*.**02** to 10–14 line **7***b*.**03**, the 15–19 line **7***b*.**04**, the 10,000–10,004 line **7***c*.**01**, the 10,005–10,009 line **7***c*.**01**, the 10,005–10,009 line **7***c*.**02**, the 10,010–10,014 line **7***c*.**03**, and the 10.015–10,019 line **7***c*.**04**. In FIG. 9 all of the columns except the one linked by the 0.4 line **7***b*.**01** are carrying read bias current. In FIG. 3*a*, the Memory 4×10 Decoder $\overline{8000}$ line **49***g*.**01**, the $\overline{4000}$ line **49***g*.**04**, the $\overline{1000}$ line **49***g*.**10**, and the $\overline{2000}$ line **49***g*.**07** are positive to bring up the 000 line **3***a*.**01**. In FIG. 4, the 0000 line **3***a*.**01** and the Memory Y Read Gate at R_1 on the line **5***g*.**08** provide a positive signal on the 0000 line **4.01** to FIG. 8. In FIG. 8, the columns of cores linked by the 20, 40, 60, 80, 20,000, 20,020, 20,040, 20,060 and 20,080 lines are driven with reset current and set current is provided on the 0000 line **4.01**. Therefore, the 0000 core is set and an output on the secondary is provided to the Memory Core Array of FIG. 13. In FIG. 3*c*, the Memory 4×10 Decoder, the $\overline{800}$ line **49***e*.**01**, the $\overline{400}$ line **49***e*.**04**, the $\overline{100}$ line **49***e*.**10** and the $\overline{200}$ line **49***e*.**07** are positive to make positive the 00 line **3***c*.**01**. In FIG. 6, when the Memory X Read Gate on the line **5***g*.**07** goes positive at $R_{1.5}$ the 000 line **6.01** is driven. In FIG. 9, the X Switch Core Matrix, the columns of cores linked by the 5–9, the 10–14, the 15–19, the 10,000–10,004, the 10,005–10,009, the 10,010–10,014, the 10,015–10,019 lines are driven with reset current and set current is provided on the 000 line **6.01**. Accordingly, the 0–4 Switch Core is set to the "one" state and half-select current is provided on the secondary. In FIG. 13, half-select reset current is provided on the 0 lines and thirty-five core planes at addresses 0000–0004 are driven with reset current. For those core planes containing "ones" outputs are provided on the sense winding and corresponding positions of the Memory Buffer Register are set to binary "ones." The contents of the Memory Buffer Register are now the following:

	Character	C	B	A	8	4	2	1
0	G	1	1	1	0	1	1	1
1	9 and B & A bits	0	1	1	1	0	0	1
2	4 and B & $\overline{A}$ bits	0	1	0	0	1	0	0
3	3 and B & $\overline{A}$ bits	0	1	0	0	0	1	1
4	2 and $\overline{B}$ & A bits	0	0	1	0	0	1	0

At the same time that Memory Addresses 0000–0004 are being read into the Memory Buffer Register the contents of Accumulator Storage Address 27 are read into the Storage Buffer Register.

Refer now to FIG. 34*b*, the Storage 2×4 Decoder, where the SASR $\overline{64}$ line **53***b*.**05** and the SASR $\overline{32}$ line **53***b*.**03** are positive, providing a positive output on the 00 line **34***b*.**01**. In FIG. 36*a*, the 00 line **34***b*.**01** is positive, therefore, the $\overline{00}$ line **36***a*.**01** is negative and the $\overline{32}$ line **36***a*.**02**, the $\overline{64}$ line **36***a*.**03** and the $\overline{96}$ line **36***a*.**04** are positive. In FIG. 36*b*, the Storage Read Bias Gate on the line **7***b*.**02** becomes positive at R_0 and drives the 32 line **36***b*.**02**, the 64 line **36***b*.**03**, and the 96 line **36***b*.**04** with reset current. In FIG. 39, the columns of cores linked by the 32, 64 and 96 lines are driven with current tending to reset the Switch Cores.

In FIG. 34*d*, the SASR $\overline{4}$ line **53***a*.**05**, the SASR 2 line **53***a*.**04**, and the SASR 1 line **53***a*.**02** are positive to provide an output on the Decimal 3 line **34***d*.**04**. In FIG. 38*a*, the Decimal 3 line **34***d*.**04** is positive so the $\overline{3}$ line **38***a*.**04** is negative. All of the other output lines are positive by way of the Inverters. In FIG. 42, the Storage Read Bias Gate on the line **7***d*.**01** is positive at $R_{0.5}$, the SASR 1 line is positive to provide an output on the Storage Read Gate Odd lines **42.01** and **42.05**. In FIGS. 38*b* and *c*, the 1 line **38***b*.**02**, the 5 line **38***c*.**02** and the 7 line **38***c*.**04** are made positive. In FIG. 40 the columns of cores linked by the 1, 5 and 7 lines are driven with reset current tending to set the Switch Cores to the "zero" state.

In FIG. 34*a*, the SASR $\overline{256}$ line **54.01** and the SASR $\overline{128}$ line **53***b*.**07** are positive to make positive the 00 line **34***a*.**01**. In FIG. 37, the Storage Read Gate on the line **7***b*.**03** becomes positive at R_1 and the 000 line **37.01** is made positive. In FIG. 39, the latter line drives the row of cores linked thereby with set current. As a result the 0 core is switched from "zero" to the "one" state and half-select reset current is provided from the secondary.

FIG. 34*c*, the SASR 16 line **53***b*.**02** and the SASR 8 line **53***a*.**08** are positive to make positive the 24 line **34***c*.**04**. In FIG. 42, the SASR 1 line **34***d*.**09** is positive and the Storage Read Gate line **7***b*.**04** becomes positive at $R_{1.5}$ to bring up the Storage Read Gate Odd line **42.02**. In FIG. 35, the 24 line **34***c*.**04** and the Storage Read Gate Odd line **42.02** drive the 24 Odd line **35.08**. In FIG. 40, Set current is now provided on the 24 Odd line **35.08** while reset current is provided on the 1 line **38***b*.**02**, the 5 line **38***c*.**02** and the 7 line **38***c*.**04**. As a result the "27" core switches from the "zero" to the "one" state providing half-select reset current on its secondary winding. FIG. 45, the 0 line at the Y Axis and the 27 line of the X Axis are driven with reset current and the seven planes of the Storage Array at address 27 receive full select current. The address 27 contains the digit 5, thus the 4 and the 1 planes contain binary "ones" and the C, B, A, 8 and 2 planes contain binary "zeros." The sense windings are sampled at $R_{3.5}$ and the 4 and the 1 triggers of the Storage Buffer Register of FIG. 47 are turned On.

Referring now to the Instruction Counter of FIGS. 32*a*–32*e*, the units order of the Instruction Counter contained 00009 during Instruction Time. At R_3 of ECC 1 the Instruction Counter is stepped to 00014 by switching the units order trigger, the Not Manual 3 line **116.09**, the ECC 1 line **123.34** and the Minus On Block Step IC line **93***j*.**12** become positive at R_3 and the negative shift is provided to the binary input of the trigger which then switches so that the IC–4 lines **32***a*.**03**–**32***a*.**05** are positive. The fall of the IC–9 line **32***a*.**04** causes the IC–10 trigger, FIG. 37*g*, to be turned On, bringing up IC–10 lines **32***b*.**08** and **32***b*.**09**.

In FIG. 100, the Read Memory line **93***a*.**03**, the Read/Write line **99.05**, the Minus On PCT Request line **135***b*.**08**, the Not Transition line **136***b*.**01** and the W_0 (D1) line **98.01** make positive the Set CR 1 line **100.02** which sets character 4 of the Memory Buffer Register into CR 1 via the Memory Out Controls. CR 1 now contains the digit 2 in the numeric portion, a B Zone Bit=0 and A zone bit=1 (CBA8421=0010010). Also, in FIG. 100, the Read Storage line **93***a*.**01**, the Not Read Request line **134***d*.**01**, the Not Transition line **136***d*.**01** and the W_0 (D1) line **98.01** provide an output signal on the Set CR 2 line **100.01** which sets CR 2 to the contents of the Storage Buffer Register, namely, the digit 5 (CBA8421=0000101).

In FIG. 5*d*, the Read Memory 1 line **5***e*.**06** is positive. Therefore, the Memory Inhibit Gate on the line **5***d*.**05** is up from $R_{4.5}$ to R_0 and the Memory Write Gate on the line **5***d*.**07** is up from W_0 to R_0. Accordingly, the Y Switch Core Matrix of FIG. 8, the 00 line **5***b*.**01** is driven with reset current which provides half-select set current on the secondary of the 0000 core. FIG. 9, the X Switch Core Matrix, reset current is provided on the 0–4 line **7***b*.**01** which resets the 0–4 core and provides half-select set current on the secondary to the Core Array of FIG.

13 where all cores of addresses 0000–0004 are driven with current to set the cores in all thirty-five planes. As described previously, inhibit current is generated in the Memory Inhibit Driver Circuits of FIGS. 12*a* and *b*, for those planes in which the writing of "zero" is desired. Accordingly, the characters read from Memory during the Read portion of ECC 1 are read back into Memory during the Write portion of the same cycle.

In the Y Switch Core Matrix of FIG. 39, the 0 core is in the set condition and in the X Switch Core Matrix of FIG. 40 the 37 core is in the set condition. In FIG. 7*e*, the Storage Read/Write Mode trigger is Off and remains Off throughout this operation since the Storage Read/Write Mode is not employed. Accordingly, the Minus On Block Storage X Write Gate line **7***e*.**04** and the Minus On Block Storage X Read Gate line 7*e*.**03** remain positive. In FIG. 43, the Result to Storage line **137.05** is down, the Storage $-\overline{C}$ line **47.01**, the Storage $-\overline{B}$ line **47.02**, the Storage $-\overline{A}$ line **47.03**, the Storage $-\overline{8}$ line **47.04**, and the Storage $-\overline{2}$ line **47.06** are positive and positive signals are present on the Storage $-\overline{C}$ bit line **43.01**, Storage $-\overline{B}$ bit line **43.02**, Storage $-\overline{8}$ bit line **43.03**, the Storage $-\overline{4}$ bit line **43.04**, and the Storage $-\overline{2}$ bit line **43.06**. In FIG. 44, the Storage Inhibit Gate on the line **7***d*.**05** comes up at $R_{4.5}$ and drives the $\overline{C}$ line **44.01**, the $\overline{B}$ line **44.02**, the $\overline{A}$ line **44.03**, the $\overline{8}$ line **44.04** and the $\overline{2}$ line **44.06**. In FIG. 36*b*, the 00 line **34***b*.**01** is positive. The Storage Write Gate on the line **7***b*.**08** comes up at W_0 to drive the 00 line **36***b*.**01**. In the Y Switch Core Matrix of FIG. 39, the 0 core was previously set and now reset current flows from 00 line **36***b*.**01** which provides sufficient current to reset this core.

Thus the 0 core is switched from "one" to "zero" and half-select set current is provided on the secondary to the Core Array of FIG. 45. In FIG. 41, the Decimal 3 line **34***d*.**04** is positive, the Storage Read/Write Mode Trigger Off line **7***e*.**01** is positive and therefore, the 3 line **41.04** is positive to the Storage X Switch Core Write Drivers of FIG. 38*b*. At W_0 the 3 line **38***b*.**04** is made positive by the 3 line **41.04**, the Minus On Block Storage X Read Gate line **7***e*.**04** and the Storage Write Gate line **7***d*.**06**. In the X Switch Core Matrix of FIG. 40, reset current is provided on the 3 line **38***b*.**04** which resets the 27 core and provides half-select set current to the Storage Array of FIG. 45. In FIG. 45, the 0 line of the Y Axis and the 27 line of the X Axis are driven by the currents previously described and those seven planes of address 27 receive set current. However, inhibit current is provided to those cores where it is desired to write "zeros" and accordingly, the digit 5 is written into the Storage Array at address 27.

EEC 1 is a Start cycle since Memory Read Mode and Storage Read/Write Mode are specified and it is during the Start cycle that the Overlap Mode Control conditions the machine for Fully overlapped operation. In FIG. 136*a*, the Minus On Block Add Trigger line **93***z*.**01** is positive since the Add Address to Memory operation is one in which Overlap Mode Control is used. The Not Transition line **136***d*.**02** is positive, the fall of the A_2/R_3–W_1 line **103***b*.**23** the Add trigger is turned On and the line **136***a*.**06** is made positive. The Memory Read/Write Mode line **93***q*.**01** is positive, the Not Transition line **136***b*.**02** is positive and the fall of the A_3/R_4–W_2 trigger On line **136***a*.**08** positive. At R_3 MAC 1 was prevented from stepping by the Minus On Block Step MAC 1 line **136***b*.**01** being negative. However, when the Mode Control Trigger Off line **136***e*.**36** falls at W_2 of ECC 1 the Minus On Block Step MAC 1 line **136***b*.**01** becomes positive. The Memory Read/Write Mode line **93***q*.**03** and the Mode Control Trigger On line **136***e*.**34** bring up the Result to Memory line **136***b*.**03**. Since the Step MAC 1–1 line **93***g*.**04** is positive and the Result to Memory line **136***b*.**03** is positive the Low Character line **136***b*.**04** comes up.

At the end of ECC 1, CR 1 contains the digit 2, CR 2 the digit 5, MAC 1 contains 4, SAC contains 28, MASR contains 4, SASR contains 27, the Instruction Counter contains 14, the Add trigger and Mode Control trigger are On. It is during the Write portion of ECC 1 and the Read portion of ECC 2 that the digit 2 is being added to the digit 5 to provide a result which is written into Memory during the Write portion of ECC 2, the result being entered in Memory Address 0004.

In FIG. 122, the right side of the ECC 1 trigger conditions the diode gate for the fall of the A_3/R_4–W_2 pulse on the line **121.03** which turns Off the ECC 1 trigger at W_2 of ECC 1. The right plate of the ECC 1 trigger also conditions an AND circuit which has another positive input Not End E Time on the line **121.05** and the fall of the A_3/R_4–W_2 line **121.03** turns On the ECC 2 trigger. Therefore, the Not ECC 1 line **122.02**, the ECC 2 line **122.04**, the ECC 1/2 line **122.05** are positive.

In FIG. 64*a*, the Memory Read/Write Mode line **64***a*.**01**, CR 1 to Adder line **64***a*.**02**, Digit Adder Out line **64***a*.**03**, Add Address to Memory lines **64***a*.**04** and **64***a*.**05**, generate C Bit Out line **64***a*.**06** and Step SAC+1 line **64***a*.**07** are positive. Since the latter lines are positive, and the Auxiliary Trigger 2 Off line **138***l*.**14** and SMT line **138***b*.**12** are positive, the Storage Read Mode is specified by a positive signal on the line **64***a*.**08**. In FIG. 64*c*, Add Address to Memory 1 line **64***a*.**05**, Auxiliary Trigger 1 Off line **138***j*.**15**, the Transition Trigger Off line **136***e*.**32** are positive so the Step MAC 1–1 line **64***c*.**02** is positive to cause MAC 1 to step to 0003 at R_3 of ECC 2. CR 2 to T/C line **64***c*.**03** is positive due to positive signals on the Add Address to Memory 1 line **64***a*.**05** and Auxiliary Trigger 1 Off line **138***j*.**15**. Recall that the character in CR 1 contains a 1 bit in the A bit position which specified Indirect Addressing and this bit must be preserved throughout the Add Address to Memory operation. Accordingly, in FIG. 64*c*, the CR 1–A line **58.26** is positive, the ECC 1/2 line **124.05** is positive, Add Address to Memory 1 line **64***a*.**05** is positive and Auxiliary Trigger 1 Off line **138***j*.**15** is positive. Therefore, the Emit A Bit line **64***c*.**01** is positive. In FIG. 93*e*, the Emit A Bit line **93***e*.**02** is positive and in FIG. 79, the Zone Adder, the Emit A Bit line makes positive the Result A lines **79.02–79.05**. The Result A line **79.02** goes to the C Bit Generator of FIG. 90. The Result A line **79.03** goes to FIG. 89*b* where it will be gated out subsequently to the Result Register.

Since MASR contains 0004 it is this address which will govern reading of Memory during the Read portion of ECC 2. Reading from Memory addresses 0000–0004 proceeds in the manner described previously with reference to ECC 1 with the exception that character 3 of MBR is selected. In FIG. 136*b*, the Low Character line **136***b*.**04** remains positive since Memory Read/Write Mode line **93***q*.**03** is positive, Mode Control Trigger On line **136***e*.**34** is positive and Step MAC 1–1 line **93***g*.**04** is positive. In FIG. 20*a*, Low Character line **136***b*.**04** brings down the Normal line thereby blocking the Select Character 4 output. In FIG. 3*e*, the $\overline{2}$ line **49***a*.**11**, the $\overline{1}$ line **49***a*.**15**, and the 4 line **49***a*.**08** are positive to bring up the Select Character 4 line **3***e*.**09**. In FIG. 20*a*, this signal is gated onto the Select Character 3 Out line **20***a*.**07** due to the Low Character line **136***b*.**04** being positive. In FIG. 20*c*, the Select Character 3 Out line **20***a*.**07** gates character 3 of the MBR onto the output lines and therefore the C Bit line **20***c*.**01**, the B Bit line **20***c*.**02**, the 2 Bit line **20***c*.**06** and the 1 Bit line **20***c*.**07** are positive. In FIG. 20*d*, these signals are presented on the output lines which are connected to the input to Character Register of FIG. 57. And at W_0 the character is set into CR 1.

At R_3 of ECC 1, SAC was stepped to 28 and at R_0 the beginning of ECC 2 Storage Address Select Register was set to the contents of SAC. Therefore, during the Read portion of ECC 2 address 28 will be read from Accumu-

lator Storage. In FIG. 34*b*, the SASR $\overline{64}$ line **53***b*.**05**, the SASR $\overline{32}$ line **53***b*.**03**, are positive to bring up the 00 line **34***b*.**01**. In FIG. 36*a*, the 00 line **34***b*.**01** brings down the $\overline{00}$ line **36***a*.**01** and the $\overline{32}$, $\overline{64}$, and 96 lines remain positive. In FIG. 36*b*, the Storage Read Bias Gate on the line **7***d*.**02** makes positive the 32, 64, and 96 lines which go to FIG. 39 to drive the columns of cores linked thereby with reset current at R_0. In FIG. 34*d*, the SASR $\overline{2}$ line **53***a*.**03**, the SASR $\overline{1}$ line **53***a*.**01** and SASR 4 line **53***a*.**06** are positive to bring up the Decimal 4 line **34***d*.**05**. In FIG. 42, the SASR $\overline{1}$ line **34***d*.**10**, the Storage Read Bias Gate line **7***b*.**01** are positive at $R_{0.5}$ to drive the Storage Read Bias Gate Even lines **42.03** and **42.06**. In FIGS. 38*b* and *c*, the 0 line **38***b*.**01**, the 2 line **38***b*.**03**, and the 6 line **38***c*.**03** are driven and in FIG. 40 the columns of cores linked thereby are driven with reset current. In FIG. 34*a*, the SASR $\overline{256}$ line **54.01** and the SASR $\overline{128}$ line **53***b*.**07** are positive to bring up the 000 line **34***a*.**01**. In FIG. 37, Storage Read Gate line **7***d*.**03** is made positive at R_1 to drive the 000 line **37.01**. In FIG. 39, the 32 line **36***b*.**02**, the 64 line **36***b*.**03** and the **96** line **36***b*.**04** are being driven with reset current and the 000 line **37.01** is driven with set current. Therefore, the 0 core will be changed to the "one" state and half-select reset current provided on the 0 secondary. In FIG. 34*c*, the SASR 16 line **53***b*.**02** and the SASR 8 line **53.08** are positive. Therefore, the 24 line **34***c*.**04** is positive. In FIG. 35 the Storage Read Gate Even line **42.04** is positive at $R_{1.3}$ and the 24 Even line **35.04** is driven. In FIG. 40, the 0 line **38***b*.**01**, the 2 line **38***b*.**03** and the 6 line **38***c*.**03** are being driven with reset current and the 24 Even line **35.04** is being driven with set current. Accordingly, the core **28** is set and half-select reset current is provided on the secondary. In FIG. 45, the 0 line of the Y Axis and the 28 line of the X Axis are energized and, therefore, the 7 cores of address 27 are driven with reset current. Those cores containing binary "ones" will provide an output on the sense winding which is sampled at $R_{3.5}$ to set the triggers of the Storage Buffer Register according to the bit configuration, present in address 28 of Accumulator Storage. The contents of address 28 of Accumulator Storage are CBA8421=1110100 and it is this number which is set into the Storage Buffer Register of FIG. 47 and placed in CR 2 at W_0 of ECC 2.

In FIGURE 64, the Suppress Zone Carry In line **64***a*.**10** is positive throughout ECC 1/2 due to the Add Address to Memory line **23***l*.**01**, the E time line **123.11** and the ECC 1/2 line **124.05**. And the A Bit on the Result A line **79.03** is set into the Result Register of FIG. 89*b* at R_4 of ECC 2 and in the Digit Adder of FIG. 86, the sum of the digits 2 and 4 is present on the outputs for entry into the Result Register at R_4 of ECC 2. The MPL 2 line **84.01** provided presentation of the digit 2. The T/C 4 line **83.03** and the T/C line **85.05** represented the digit 5. Thus, the Sum 1 line **86.01**, the Binary Sum 2 lines **86.02** and **86.03** and the Binary Sum 4 lines **86.04** and **86.05** are positive and the Decimal Correction Circuits of FIG. 87, the Binary Sum 2 line **86.02**, the Binary Sum 4 line **86.04** and the Sum 1 line **86.01** are positive. The Digit Adder Out line **93***c*.**01** is up as previously mentioned. Therefore, the output lines Result 2, Result 4, Result 1 and Digit Adder outputs=0 are positive. The Result Register of FIG. 89*a*, Result 1, Result 2 and Result 4 lines are positive and are gated by the R_2–W_0/A_0 Use line **103***a*.**14**. At R_4 the line **101.07** becomes positive and sets the 1, 2 and 4 trigger to the On state. The Result Register now contains the bit configuration of CBA8421=0010111.

In FIG. 137, the Result to Memory line **93***t*.**01** is up as mentioned previously. The Minus On PCT Request line **135***b*.**14** is positive and at A_2 the A_2/R_3–W_1 Use line **103***a*.**07** becomes positive to turn On the Result to Memory trigger at R_3 of ECC 2. The MASR $\overline{40,000}$ line **49***i*.**07** is positive. Therefore, the Result to Memory 1 lines **137.01** and **137.02** are up. In FIG. 10, the Select Character 4 line **20***a*.**10** is positive, the Result to Memory 1 line **137.01** makes positive the Result 4 to Memory line **10.10**. In FIG. 11*a*, the $\overline{C}$ line **89***b*.**09**, the $\overline{B}$ line **89***b*.**05** and the $\overline{8}$ line **89***a*.**13** are positive so the character 4–$\overline{C}$ Bit line **11***a*.**01**.**04**, the character 4–$\overline{B}$ Bit line **11***a*.**02**.**04** and the character 4–$\overline{8}$ Bit line **11***a*.**04**.**04** are positive. In FIG. 12*a*, Memory Inhibit Driver Circuits, the $\overline{C}$ line **11***a*.**01**, the $\overline{B}$ line **11***a*.**02** and the $\overline{8}$ line **11***a*.**04** are positive and the Memory Inhibit Gate line **5***g*.**02** becomes positive at $R_{4.5}$. In the Y Switch Core Matrix of FIG. 8, 0000 core was set during the Read portion of ECC 2. In FIG. 9, the 0–4 core was set during the Read portion of ECC 2. In FIG. 5*b*, the 00 line **5***a*.**01** is positive and the Memory Write Gate line **5***g*.**03** becomes positive at W_0 to drive the 00 line **5***b*.**01**. In FIG. 8, the 00 line **5***b*.**01** is driven with reset current which resets the 0000 core and provides a half-select set current on the secondary. In FIG. 7*b*, 0–4 line **7***a*.**01** is positive and the Memory Write Gate line **5***g*.**05** becomes positive at W_0 and drives the 0–4 line **7***b*.**01**. In FIG. 9, the column of cores linked by the 0–4 line **7***b*.**01** is driven with reset current and the 0–4 core is reset thereby providing half-select set current on its output to the Storage Array of FIG. 13. Cores at address 0–4 of thirty-five planes are provided with current which will set each core to the "one" state in the absence of inhibit current. However, inhibit current is provided to those cores in which it is desired to write "zeros." Therefore, characters 0, 1, 2 and 3 are written from the Memory Buffer Register into their former locations. The contents of the Result Register is written into address 0004. Thus, Memory addresses 0000–0004 now contain the following:

Memory Address	C	B	A	8	4	2	1
0000	1	1	1	0	1	1	1
0001	0	1	1	1	0	0	1
0002	0	1	0	0	1	0	0
0003	0	1	0	0	0	1	1
0004	0	0	1	0	1	1	1

During the Write portion of ECC 2 the contents of the Storage Buffer Register are written back into Accumulator Storage Address 28 to the Y Switch Core Matrix of FIG. 39, the 0 core is in the set condition and in the X Switch Core Matrix of FIG. 40, the core 28 is in the set condition. In FIG. 43, the Result to Storage line **137.05** is down. Therefore, the contents of the Storage Buffer Register, FIG. 47, is gated onto the output lines. The Storage —$\overline{8}$ line **47.04**, the Storage —$\overline{2}$ line **47.06** and the Storage —$\overline{1}$ line **47.07** are positive since the Storage Buffer Register contains the character CBA8421=1110100 and positive signals on the Storage —$\overline{8}$ Bit line **43.04**, the Storage —$\overline{2}$ Bit line **43.06** and the Storage —$\overline{1}$ Bit line **43.07** are provided to the Storage Inhibit Drivers of FIG. 44. In the latter figure, the Storage Inhibit Gate on the line **7***d*.**05** is present at $R_{4.5}$ to drive the output lines $\overline{8}$ line **44.04**, $\overline{2}$ line **44.06** and $\overline{1}$ line **44.07**. In FIG. 36*b*, the 00 line **34***b*.**01** is positive, the Storage Write Gate line **7***d*.**08** becomes positive at W_0 to drive the 0 line **36***b*.**01**. In FIG. 39, the 00 line **36***b*.**01** is driven with reset current which resets the 0 Switch Core and provides half-select set current on the secondary. In FIG. 38*c*, the 4 line **41.05** is positive and the Minus On Block Storage X Write Gate line **7***e*.**04** and the Storage Write Gate line **7***b*.**07** provide an output on the 4 line **38***c*.**01** at W_0. In FIG. 40, the 4 line **38***c*.**01** is driven with reset current and the core 28 is reset to 0 thereby providing half-select set current on its secondary to Storage Array of FIG. 45. In FIG. 45, the 0 line of the Y Axis, the 28 line of the X Axis are driven with current tending to set the 7 cores of address 27 to the "one" state and inhibit current is

provided in those planes where it is desired to write "zeros," namely the 8, 2 and 1 planes. Accordingly, the contents of the Storage Buffer Register previously extracted from Accumulator Storage Address 28 are now returned during the Write portion of ECC 2 to the same address.

ECC 2 has been a Fully Overlapped cycle. The result of computations occurring during the Write portion of ECC 1 and the Read portion of ECC 2 have been stored in Memory Address 0004 and during the Read portion of ECC 2 the next pair of characters have been selected for addition from the Memory Address 0003 and the Storage Address 28 at R_3 of ECC 2, MAC 1 has been stepped down to address 0003 and SAC has been stepped up to address 29. At R_0, the start of Execute cycle 3, MASR is set to MAC 1 and SASR is set to SAC. MASR contains 0003 throughout Execute cycle 3 and SASR contains 29 throughout Execute cycle 3.

In FIG. 122, the right plate of the ECC 2 trigger conditions a diode gate for the fall of the A_3/R_4–W_2 line **121.03** which turns Off the ECC 2 trigger. Therefore, the Not ECC 1/2 line **122.01** is positive. The Not ECC 1 line **122.02** is positive and the ECC 1 line **122.03**, the ECC 2 line **122.04** and the ECC 1/2 line **122.05** are negative. In FIG. 64*a*, the Add Address to Memory line **23***l*.**02** and the E time line **123.11** maintain the Memory Read/Write Mode, CR 1 to Adder, Digit Adder Out, Add Address to Memory, Generate C Bit Out and Step SAC+1 lines in the up condition. Auxiliary Trigger 2 Off line **138***l*.**14** and Storage Mark Trigger Off line **138***b*.**02** maintain the Storage Read Mode line positive and with both the Transition Trigger On line **136***e*.**21** and the ECC 1/2 line **124.05** down, Suppress Zone In line **64***a*.**10** is down. CR 2 contains the digit 4 and also has binary "ones" in the B and A positions. Therefore, the digit 4 is passed to the Digit Adder and the zones are passed to the Zone Adder. CR 1 contains the digit 3 and a binary "one" in the B position, a binary "zero" in the A position. The numeric portion is passed to the Digit Adder and the Zone portion is passed to the Zone Adder. In FIG. 64*c*, the Add Address Memory 1 line **64***a*.**05**, Auxiliary Trigger 1 Off line **138***j*.**15** and Transition Trigger Off line **136***e*.**32** are positive to bring up the Step MAC 1–1 line **64***c*.**02**. The Add Address Memory 1 line **64***a*.**05** and Auxiliary Trigger 1 Off line **138***j*.**15** make positive CR 2 to T/C line **64***c*.**03**. Add Address Memory 1 line **64***a*.**05**, Transition Trigger Off line **136***e*.**32**, Not ECC 1/2 line **124.16** provide Zone Adder Out on the line **64***c*.**05**.

In FIG. 3*b*, the $\overline{20{,}000}$ line **49***i*.**04**, the $\overline{80}$ line **49***c*.**01**, the $\overline{40}$ line **49***c*.**04**, the $\overline{20}$ line **49***c*.**07** are positive as in the previous cycle. The 00 line **3***b*.**01** is up. In FIG. 5*a*, the 00 line **3***b*.**01** brings down the $\overline{00}$ line **5***a*.**02**. The remaining NOT lines are positive. In FIGS. 5*b* and *c*, the Memory Read Bias Gate on the line **5***g*.**09** is positive at R_0 to drive the 20, 40, 60, 80, 20,000, 20,020, 20,040, 20,060 and 20,080 lines. In FIG. 8, all of the columns of cores are driven with reset current except the 00 line **5***b*.**01**. In FIG. 3*d*, the $\overline{10{,}000}$ line **49***i*.**01**, $\overline{10}$ line **49***c*.**10**, the $\overline{4}$ line **49***a*.**05**, the $\overline{8}$ line **49***a*.**01**, the 1 line **49***a*.**16** and the 2 line **49***a*.**12** are positive to provide an output on the 0–4 line **3***b*.**01**. In FIG 7*a*, the 0–4 line **3***d*.**01** is positive making the $\overline{0\text{–}4}$ line **7***a*.**02** negative. The remaining NOT lines are positive. In FIGS. 7*b* and *c*, the Memory Read Bias Gate is provided on the lines **5***g*.**11** and **5***g*.**12** at $R_{0.5}$ to drive the 5–9, the 10–14, 15–19, 10,000–10,004, 10,005–10,009, 10,010–10,014 and 10,015–10,019 lines. In FIG. 9, all of the columns of cores are driven with reset current except for the column linked by the 0–4 line **7***b*.**01**. In FIG. 3*a*, the $\overline{8000}$ line **48***g*.**01**, the $\overline{4000}$ line **49***g*.**04**, the $\overline{1000}$ line **49***g*.**10** and the $\overline{2000}$ line **49***g*.**07** are positive and the 000 line **3***a*.**01** is positive. In FIG. 4, the Memory Y Read Gate on the line **5***g*.**08** comes up at R_1 and drives the 000 line **4.01** with set current. In FIG. 8 all of the columns of cores are being driven with reset current except the one linked by the 00 line **5***b*.**01**. The 000 line **4.01** is driven with set current, therefore, the 0000 Switch Core is set to the "one" state providing an output on the secondary to the Core Array. In FIG. 3*c*, the $\overline{800}$ line **49***e*.**01**, $\overline{400}$ line **49***e*.**04**, $\overline{100}$ line **49***e*.**10** and $\overline{200}$ line **49***e*.**07** provide an output on the 000 line **3***c*.**01**. In FIG. 6, the Memory X Read Gate on the line **5***g*.**07** becomes positive at $R_{1.3}$ and drives the 000 line **6.01**. In FIG. 9, all of the columns of cores are driven with reset current except the one linked by the 0–4 line **7***b*.**01**. Set current is flowing in the 000 line **6.01** and as a result the 0–4 core will be switched to the "one" state providing reset current on the secondary to the Core Array. In FIG. 13, each of the thirty-five cores at addresses 0000–0004 are being driven with reset current. The outputs are sampled at $R_{3.5}$ and the contents of these Memory addresses is placed in the Memory Buffer Register. In FIG. 3*e*, the $\overline{8}$ line, the $\overline{4}$ line, the 2 line and the 1 line are positive to bring up the Select Character 3 line **3***e*.**07**. In FIG. 20*a*, the Low Character line **36***b*.**04** is positive so the Normal line is down and the Select Character 2 output becomes positive. In FIG. 20*d*, the bits of character 2 are gated onto the output lines. The numeric portion is the digit 4 and the zone portion of the B bit is a 1 and the A bit is a 0. The bit configuration is thus CBA8421=0100100 and at W_0 this bit configuration is set into the triggers of CR 1.

In FIG. 34*b*, SASR $\overline{64}$ and SASR $\overline{32}$ lines are up to provide an output on the 00 line **34***b*.**01** which causes the 32, 64 and 96 lines in FIG. 39 to be driven with reset current as previously described. In FIG. 34*d*, the SASR $\overline{2}$ line, SASR 1 line and SASR 4 line are positive to bring up the Decimal 5 line **34***d*.**06**. Therefore, in FIG. 40 the 1, 3 and 7 lines are driven with reset current. In FIG. 34*a*, the SASR 256 and SASR $\overline{128}$ lines are positive to bring up the 256 line **34***a*.**03**. And, therefore, in FIG. 39, the 256 line **37.03** is furnished with set current and the 256 core is set to "one" and an output is provided on its secondary. In FIG. 34c, the SASR 16 and SASR 8 lines are positive to bring up the 24 line **34***c*.**04**. And, therefore, in FIG. 40, the 24 Odd line **35.08** is driven with set current and the core 29 is caused to switch to the "one" state and provide an output on its secondary. In FIG. 45, the seven cores at address 285 are driven with reset current. The output of the Sense Windings is sampled at $R_{3.5}$ and the bit configuration at Accumulator Storage Address 29 is placed in CR 2 at W_0. The character at address 29 has a numeric portion of 3 and 0 bits in the B and A positions. Accordingly, CR 2 is not CBA8421=0000011.

At R_4 the result of addition taking place during the Write portion of ECC 2 and the Read portion of Execute cycle 3 is available. The numeric portions 4 and 3 have been added to provide 7 and the zone bits have been added to provide a result of binary "zero" for the B position and a "one" for the A position and a zone carry out of the B position is stored.

In the Zone Adder of FIG. 79, the CR 1 to Adder A line **73.01** is down, CR 1 to Adder B line **73.08** is up, CR 2–A line **75.09** is up, and CR 2–B line **75.03** is up prior to W_0. Zone Adder Out line **93***b*.**02** is positive as mentioned previously, and the True line **83.01** is positive. CR 2 to T/C line **93***b*.**05** is positive as described previously. Zone Carry In line **93***d*.**01** is down. The Result A lines **79.02** through **79.05** become positive indicating a binary "one" which is the sum of the A bits, a binary "zero" from CR 1 and a binary "one" from CR 2. The Result B lines **79.06** through **79.09** are down indicating the Result binary "zero" of adding the B bits, a binary "one" from CR 1 and a binary "one" from CR 2. However, this addition results in a Zone Carry Out which makes positive the lines **79.10** through **79.12**. The line **79.11** goes to FIG. 88 where its positive signal is used with a

positive signal on the Minue On Suppress Zone Carry In line **93***d*.**02** to condition a diode gate for a pulse on the W_0 Add line **101.11** which turns On the Zone Carry trigger at W_0 of Execute cycle 3 in order to preserve the carry for use during Execute cycle 4. The positive signal on Result A line **79.03** goes to FIG. 89*b* where it is gated by the R_2/A_0–W_0 Use line **103***a*.**15** to turn On the Result A trigger when the R_4 Use line **101.18** goes positive. The Result B line **79.07** also goes to FIG. 89*b*, but since this line is negative the Result B trigger remains Off to indicate a binay "zero" in the B position of the Result Register.

Summarizing, prior to W_0 of Execute cycle 3, CR 1 contains the digit 4, a binary "one" in the B bit position and a binary "zero" in the A bit position. CR 2 contains the digit 3 with "zeros" in both the B and A bit positions. After R_4 the Result Register contains the digit 7 with a "zero" bit in the B bit position and a "one" bit in the A bit position. MAC 1 contains the value 2, MASR the value 3, SAC the value 30 and SASR the value 29.

During the Write portion of Execute cycle 3, the contents of the Result Register are stored in Memory Address 3 and the contents of the Storage Buffer Register are returned to Accumulator Storage address 29.

In FIG. 3*e*, the $\overline{8}$, $\overline{4}$, 2 and 1 lines are positive to bring up the Select Character 3 line **3***e*.**07**. In FIG. 20*a*, the signal is passed via the Select Character 3 line **20***a*.**08** to FIG. 10 where it is combined with Result to Memory on the line **137.01** to make positive the Result 3 to Memory line **10.08**. In FIG. 11*a*, the $\overline{C}$, $\overline{B}$ and $\overline{8}$ signals are gated by the Result 3 to Memory line to the Memory Inhibit Driver Circuits of FIG. 12*a* for furnishing inhibit current for those planes in which it is desired to record "zeros."

In the Y Switch Core Matrix of FIG. 8, the 0000 core was set during the Read portion of Execute cycle 3. In FIG. 9, the X Switch Core Matrix, the 0–4 core was set during the Read portion of Execute cycle 3. In FIG. 5*b*, the 00 line **5***a*.**01** is positive and the Memory Write Gate on line **5***g*.**03** goes positive at W_0 to drive the 00 line **5***b*.**01**. In FIG. 8, the column of cores linked by the 00 line **5***b*.**01** is driven with reset current which resets the 0000 core and provides half-select current on the secondary. In FIG. 7*b*, the 0–4 line **7***a*.**01** is positive and the Memory Write Gate on the line **5***g*.**05** comes up at W_0 to drive the 0–4 line **7***b*.**01**. In FIG. 9, the column of cores linked by the 0–4 line **7***b*.**01** is driven with reset current which resets the 0–4 core and provides half-select set current on the secondary. In FIG. 13, set current is applied to the thirty-five cores of addresses 0000–0004 and inhibit current is supplied to those core planes where it is desired to write "zeroes." The contents of these addresses is now as shown below:

Memory Address	C	B	A	8	4	2	1
0000	1	1	1	0	1	1	1
0001	0	1	1	1	0	0	1
0002	0	1	0	0	1	0	0
0003	0	0	1	0	1	1	1
0004	0	0	1	0	1	1	1

	1 1 0 0	(B)
	1 0 1 1	(A)
G	9 4 7 7	

At R_3 of Execute cycle 3, MAC 1 is stepped down to 0002 and at R_0 of Execute cycle 4 the Memory Address Select Register is set to the contents of MAC. At R_3 of Execute cycle 3, SAC is stepped to 30 and at R_0 of Execute cycle 4 the Storage Address Select Register is set to the contents of SAC. During the Read portion of Execute cycle 4, Memory addresses 0000–0004 are read from in the manner described previously. However, in this cycle it is character 1 which is selected and set into CR 1. Briefly, in FIG. 3*b*, the 00 line **3***b*.**01** is positive which causes all of the columns of cores of the Y Switch Core Matrix of FIG. 8 to be driven with reset current except for the column linked by the 00 line **5***b*.**01** at R_0. In FIG. 3*d*, the 0–4 line **3***d*.**01** is made positive which causes all of the columns of cores of the X Switch Core Matrix of FIG. 9 to be driven with reset current except for the 0–4 line **7***b*.**01** at $R_{0.5}$. In FIG. 3*a*, the 0000 line **3***a*.**01** is made positive which causes the 0000 line **4.01** of the Y Switch Core Matrix of FIG. 8 to drive its rows of cores with set current. Accordingly, the 0000 switch core will be set and provide half-select reset current on its secondary. In FIG. 3*c*, the 000 line **3***c*.**01** is made positive which causes the 000 line **6.01** in the X Switch Core Matrix of FIG. 9 to drive its row of cores with set current. The 0–4 core is set providing half-select reset current at its secondary. In FIG. 13, the 0 lines are driven with reset current to switch those cores storing binary "ones" at addresses 0000–0004 to the "zero" state. The sense windings are sampled at $R_{3.5}$ and at W_0 character 1 is set into CR 1. In FIG. 3*e*, the 2, $\overline{4}$ and $\overline{1}$ lines are positive which makes Select Character 2 lines **3***e*.**05** positive. In FIG. 20*a*, Select Character 2 line **3***e*.**05** and the Low Character line **136***b*.**04** provide a positive signal on the Select Character 1 Out line **20***a*.**05**. The Character 1–B line, the Character 1–A line, the Character 1–8 line and the Character 1–1 line are positive and are gated onto the output lines by the Select Character 1 Out line **20***a*.**05** which goes to FIG. 20*d* where they are passed to CR 1. At W_0, CR 1 is set to CBA8421=0111001.

SASR contains the address 30. In FIG. 34*b*, the SASR–$\overline{64}$ and SASR–$\overline{32}$ lines provide a positive output on the 00 line **34***b*.**01** which causes the columns of cores of the Y Switch Core Matrix of FIG. 39 to be driven with reset current except for the column linked by the 00 line **36***b*.**01**. In FIG. 34*d*, the SASR–$\overline{1}$ line, the SASR–2 line and the SASR–4 line make positive the Decimal 6 line **34***d*.**07** which causes all of the columns of cores of the Even portion of the X Switch Core Matrix of FIG. 40 to be driven with reset current except for the column linked by the 6 line **36***c*.**03**. In FIG. 34*a*, the SASR–256 line, the SASR–$\overline{128}$ line make positive the 256 line **34***a*.**03** which causes set current to flow in the Y Switch Core Matrix of FIG. 39 in the 256 line **37.03** which sets the 256 core to the "one" state and provides half-select reset current on its secondary. In FIG. 34*c*, the SASR–16 line and the SASR–8 line provide a positive level on the 24 line **34***c*.**04** which causes set current to flow in the 24 Even line **35.04** which sets the switch core 30 to set state and provides half-select reset current on its secondary. In the Storage Array of FIG. 45, the 256 line of the Y Axis and the 30 line of the X Axis are driven with reset current which provides indications of binary "ones" on the sense windings of the C and the 2 planes and at W_0, CR 2 is set to CBA8421=1000010.

During the Write portion of Execute cycle 3 and the Read portion of Execute cycle 4, the digits 4 and 3 have been added in the Digit Adder and the Zone bits are added in the Zone Adder along with the zone carry generated from the previous addition. In the Digit Adder of FIG. 86, the Multiple 4 line **85.03** is positive to indicate the digit 4 and the T/C 1 line **83.05** and the T/C 2 line **83.04** are positive to indicate the digit 3. Thus, the Sum 1 line **86.01**, the Sum 2 lines **86.02** and **86.03** and the Sum 4 lines **86.04** and **86.05** are positive. These signals are passed through the Decimal Correction circuits of FIG. 87 onto the Result 2, the Result 4 and the Result 1 lines which go to the Result Register of FIG. 89*a*. In the Zone Adder of FIG. 79, the CR 1 to Adder B line **73.08** is positive to indicate a binary "one." The CR 2–B line **75.03**, the CR 2–A line **75.09** and the CR 1 to Adder A line **73.01** are negative to indicate binary "zeros." The Zone Carry In Line **93***d*.**06** is positive to indicate a carry in from the previous addition. The results of adding the A bit is "zero" and of adding the B bit is "one" and with the zone carry into the A bit position the result is 11. Thus, the Result A lines **79.02**

through **79.05** and the Result B lines **79.06** through **79.07** are positive. In this instance the Zone Carry Out lines **79.10** through **79.12** are negative and the No Zone Carry Out lines **79.13** through **79.15** are positive. In FIG. 88 the No Zone Carry Out line **79.15** conditions a diode gate for the pulse on the W_0 Add line **101.00** which turns Off the Zone Carry trigger at W_0 of Execute cycle 4. In the Result Register of FIGS. 89*a* and *b*, the Result 1 line, the Result 2 line, the Result 4 line, the Result A line, the Result B line and the Result C line are positive and are gated by the R_2–W_0/A_0 Use lines **103***a*.**14** and **103***a*.**15** to condition diode gates for the R_4 pulse on the lines **101.17** and **101.18** which sets the Result Register to CBA8421=1110111. During the Write portion of Execute cycle 4, the contents of the Result Register are written into Memory address 0002.

In the Y Switch Core Matrix of FIG. 8, the 0000 core was set during the Read portion of Execute cycle 4. In the X Switch Core Matrix of FIG. 9, the 0–4 core was set during the Read portion of Execute cycle 4. In FIG. 5*b*, the 00 line **5***a*.**01** and the Memory Write Gate line **5***g*.**03** are positive to bring up the 00 line **5***b*.**01** which goes to the Y Switch Core Matrix and resets the 0000 core which provides half-select set current to the Core Array. In FIG. 7*b*, the 0–4 line **7***a*.**01** is positive and the Memory Write Gate on the line **5***g*.**05** is provided to bring up the 0–4 line **7***b*.**01** which goes to the X Switch Core Matrix of FIG. 9 and resets the 0–4 core which provides half-select set current on its secondary. Thus, in FIG. 13, the thirty-five cores at addresses 0000–0004 are driven with set current. In FIG. 20*a*, the Select Character 2 line **3***e*.**05** is positive and, therefore, the Select Character 2 Output line **20***a*.**06** is positive. In FIG. 10, the Result to Memory 1 line **137.01** and the Select Character 2 line **20***a*.**01** bring up the Result 2 to Memory line **10.06**. In FIG. 11*a*, the $\overline{8}$ line **89***a*.**03** is positive and is gated by the Result 2 to Memory line onto the Character 2–$\overline{8}$ line of FIG. 12*a*. In the latter figure, the $\overline{8}$ line **11***a*.**04** is positive and the Memory Inhibit Gate line **5***g*.**02** makes the $\overline{8}$ line **12***a*.**04** positive. Thus, writing a "one" into the 8 plane of address 0002 of the Memory Core Plane of FIG. 13 is prohibited and the character

CBA8421=1110111

has been written into Memory at address 0002.

The 0 core of the Y Switch Core Matrix of FIG. 39 and the 30 core of the X Switch Core Matrix of FIG. 40 are in the set condition and during the Write portion of Execute cycle 4 the character read from Storage Address 30 and placed in the Storage Buffer Register is read back into address 30.

At R_3 of Execute cycle 4, MAC 1 is stepped down to 0001 and in FIG. 30*g*, the MAC 1 Ends in 1/6 lines **30***g*.**04** and **30***g*.**05** are positive. In FIG. 64*c*, the MAC 1 Ends in 1/6 line **30***g*.**05** and the Add Address to Memory 1 line **64***a*.**05** provide an output on the Turn On Transition Trigger line **64***c*.**06**. In FIG. 136*a*, the Turn On Transition Trigger line **93***m*.**04**, Add Trigger On line **136***d*.**15** and the W_2 (D1) line **102.17** turn On the Transition trigger and bring up the lines **136***a*.**02** through **136***a*.**04**, to define Execute cycle 5 as a Transition cycle.

At R_0 of Execute cycle 5, CR 1 contains the digit 9 and 1 bits in the B and A positions. CR 2 contains the digit 2 with "zeros" in the B and A positions. The Result Register is reset to all "zero" bits. MAC 1 contains 0001 and SAC contains 31. At R_0 MASR is set to 0001 and SASR is set to 31. During a Transition cycle, when operating in the Memory Read/Write Mode, reading from Memory into CR1 is not performed, but the results of computations taking place during the Write portion of the previous cycle and the Read portion of the Transition cycle are written into Memory at the address read from the previous cycle. In the Read portion of Execute cycle 5, the set pulses for CR 1 and CR 2 are inhibited. The results are read into Memory Address 0001.

In FIG. 100 the NOT Transition line **136***d*.**01** is down. Therefore, the Set CR 1 and Set CR 2 pulses are not provided during Execute cycle 5, which is a Transition cycle. And, accordingly, CR 1 and CR 2 retain their contents until the following cycle. In FIG. 64*a*, Add Address to Memory line **23***l*.**02** and E Time line **123.11** are positive and Memory Read/Write Mode line **64***a*.**01**, CR 1 to Adder line **64***a*.**02**, Digit Adder Out line **64***a*.**03**, Add Address to Memory lines **64***a*.**04** and **64***a*.**05**, Generate C Bit Out line **64***a*.**06** and Step SAC+1 line **64***a*.**07** are up. Since the foregoing lines are positive and the Auxiliary Trigger 2 Off line **138***l*.**14** and the SMT Off line **138***b*.**12** are positive the Storage Read Mode line **64***a*.**08** is positive. Add Address to Memory line, E Time line and Transition Trigger On line **136***e*.**21** bring up the Turn On Auxiliary Trigger 1 line **64***a*.**09**. In FIG. 64*c*, CR 1–A line **58.26** is positive and, therefore, with Transition Trigger On line **136***a*.**22** Add Address to Memory 1 line **64***a*.**05** and Auxiliary Trigger 1 Off line **138***j*.**15** positive, the Emit A Bit line **64***c*.**01** is up and goes to FIG. 93*e* for generating an A bit in the Result Character. The Transition Trigger Off line **136***e*.**32** is down which prevents the Step MAC 1–1 line **64***c*.**02**, CR 2 to T/C line **64***c*.**03** is maintained positive, and CR 1–B line **58.12** is positive. The Transition Trigger On line **136***e*.**22**, Add Address to Memory 1 line **64***a*.**05** and Auxiliary Trigger 1 Off line **138***j*.**05** are positive to bring up the Emit B Bit line **64***c*.**04** to FIG. 93*e* where it is used to generate a B bit in the Result Character. Since Auxiliary Trigger 1 On line **138***i*.**20** and Transition Trigger Off line **136***e*.**32** are down the Zone Adder Out line **64***c*.**05** is negative. MAC 1 has not changed and, therefore, the MAC 1 Ends in 1/6 line **30***g*.**05** is positive, the Add Address to Memory 1 line **64***a*.**05** is positive to maintain positive the Turn On Transition Trigger line **64***c*.**06**. During Execute cycle 5, the MASR sits at 1 and during the Read portion of the cycle Memory addresses 0000–0004 are read from in order to set the switch cores for writing into Memory during the Write portion of the cycle, but, as stated before, no character is selected and placed in CR 1. In effect, the contents of Memory Buffer Register are ignored. In FIG. 8, the 0000 switch core is set in the manner previously described and in FIG. 9, X Switch Core Matrix, the 0–4 switch core is set. At R_4 the results of adding the digit 9 and the digit 2 are entered into the Result Register together with the binary "ones" in the A and B bit positions of CR 1, which were emitted onto the result lines, as described above. In the Digit Adder of FIG. 86, the Digit 9 was represented by the Multiple 1 line **84.01** and the Multiple 8 line **85.05** being positive. The digit 2 was represented by the T/C–2 line **83.04** being positive. Accordingly, the Sum 1 line **86.01**, the Binary Sum 2 lines **86.02** and **86.03**, and the Binary Sum 8 lines **86.06** and **86.07** are positive. In FIG. 88, the Binary Sum 2 line **86.03**, the Binary Sum 8 line **86.07**, and the Minus On Suppress Adder Carry line **93***d*.**01** are positive to condition a diode gate for the fall of the A_3/R_4–W_2 line **104.09** when NOT Mutiply 2 line **67***a*.**05** is positive and Transition line **136***c*.**04** is positive, to turn On the Decimal Carry trigger to store the carry for later use.

Since the digit 9 and the digit 2 were added in binary fashion—

1001	9
0010	2
1011	11

The sum must be corrected in the decimal correction circuits of FIG. 87. In the latter figure, the Binary Sum 2 line **86.02**, the Binary Sum 8 line **86.06**, the Sum 1 line **86.01** and the Digit Adder Out line **93***c*.**01** are positive. The Sum 1 signal is passed directly to the Result 1 lines **87.09** through **87.12**. The Binary Sum 2 signal is blocked

by the No Decimal Carry Out line **88.07**, the Binary Sum 4 line **86.04** and the Binary Sum 8 Carry line **86.08**. The Binary Sum 8 line **86.06** is blocked by the No Decimal Carry Out line **88.07**. Thus, the Result 2, Result 4 and Result 8 lines are negative and the Result 1 lines are positive as desired.

In the Result Register of FIG. 89*a*, the Result 1 line is positive, the Result A line is positive, the Result B line is positive and the Result C line is positive and at R_4 the triggers of the Result Register are set to the bit configuration CBA8421=1110001.

In FIG. 136*b*, the Transition line **136***c*.**02** being up, the Storage Read Mode line **93***q*.**04** being up brings down the Minus On Block Step SAC line **136***b*.**09** which goes to FIG. 93*r* where it prevents the Step SAC+1 lines **93***r*.**03** and **93***r*.**04** from becoming positive. In Execute cycle 5 stepping of SAC is suppressed which is required in order that an address not be skipped in the sequence of operations.

In FIG. 3*e*, the $\overline{8}$, $\overline{2}$, $\overline{4}$ and 1 lines are positive and Select Character 1 line **3***e*.**03** is made positive. In FIG. 20*a*, the signal on the Select Character 1 line is passed to the Select Character 1 line **20***a*.**02**, the latter going to FIG. 10 where it is used with Result to Memory on the line **137.01** to bring up Result 1 to Memory line **10.04**. In FIG. 11*b*, the $\overline{8}$, $\overline{4}$ and $\overline{2}$ lines of the Result Register are positive and Result 1 to Memory line feeds these signals onto the output lines to the Inhibit Driver Circuits of FIG. 12*b* where inhibit current is supplied to those Memory Core Planes in which it is desired to write "zeros." In FIG. 5*b*, the 00 line **5***a*.**01** is positive, the Memory Read Gate line **5***g*.**03** goes positive at W_0 to drive the 00 line **5***b*.**01**. In FIG. 8, the column of cores linked by the 00 line **5***b*.**01** is driven with reset current which resets the 000 core to provide half-select set current on the secondary. In FIG. 7*b*, the 0–4 line **7***a*.**01** is positive and the Memory Write Gate line **5***g*.**05** becomes positive at W_0 to drive the 0–4 line **7***b*.**01**. In FIG. 9, the column of cores linked by the 0–4 line **7***b*.**01** is driven with reset current which resets the 0–4 switch core and provides half-select current on the secondary. Thus, in FIG. 13, thirty-five cores of addresses 0000–0004 are provided with set current and inhibit current is provided to those core planes in which it is desired to write "zeros." If the result of writing character 1 into Memory the contents of Memory addresses 0000–0004 are now:

```
      1 1 0 0 . . . . (B)
      1 1 1 1 . . . . (A)
G     1 7 7 7
```

Address	C	B	A	8	4	2	1
0000	1	1	1	0	1	1	1
0001	1	1	1	0	0	0	1
0002	1	1	1	0	1	1	1
0003	0	0	1	0	1	1	1
0004	0	0	1	0	1	1	1

In FIG. 136*a*, the Transition line **136***c*.**01** conditions a diode gate for the fall of the A_2/R_3–W_1 line **103***b*.**23** which turns Off the Add trigger at W_1 and conditions a diode gate for the fall of the A_3/R_4–W_2 line **103***b*.**07** which turns Off the Mode Control trigger at W_2. The Add Trigger Off line **136***b*.**18** is positive after W_1 and the pulse on the W_2 (D1) line **102.17** turns Off the Transition trigger. At the beginning of Execute cycle 6, CR 1 contains the digit 9 with binary "ones" in the B and A positions, CR 2 contains the digit 2 with binary "zeros" in the B and A positions. MAC 1 remains at address 0001, Memory Address Select Register is set to MAC 1 at R_0, SAC contains the Storage Address 31, and at R_0 the Storage Address Select Register contains address 31. The Transition trigger and the Add trigger are Off, the Decimal Carry trigger is On the Auxiliary Trigger 1 is On due to Turn On Auxiliary Trigger 1 line **93***k*.**01** which conditions a diode gate in FIG. 138*i* for the fall of the A_3/R_4–W_2 pulse line **103***b*.**15**, to turn On Auxiliary Trigger 1 at W_2 of Execute cycle 5.

As pointed out previously it is the zone bits of the thousands order of the Memory field and the B bit of the units order of the Memory field which are added to the ten thousands order of the Storage field. Therefore, during addition of the 9 and 2 digits the zone bits associated with the 9 digit were passed unmodified to the Result Register and stored with the digit 1 at address 0001. It is during Execute cycles 6 and 7, a Start cycle and Transition cycle respectively, that the zone bits of the thousands order of the Memory field are added to the ten thousands order digit of the Storage field from address 31 and also the Decimal Carry out of the thousands order must be added into the ten thousands order. During Execute cycle 6 the Memory Read/Write Mode, CR 1 to Adder, Digit Adder Out and Generate C Bit Out conditions prevail. Auxiliary Trigger 1 is On, Auxiliary Trigger 2 is Off, the Storage Mark Trigger is Off, so the Storage Read Mode is specified. Furthermore, the following routing lines are brought up: the Zone Adder Out, Suppress Zone Carry In, Block Decimal Carry Into Adder, and Turn On Transition Trigger. Since there is a decimal carry in from the previous computation the Route Zone Carry In line is made positive. CR 2 contains a "one," so an A bit is emitted to the True/Complement Controls. More specifically, in FIG. 64*a*, Add Address to Memory line **23***l*.**02** and E Time line **123.11** are positive to bring up Memory Read/Write Mode line CR 1 to Adder, Digit Adder Out line, Add Address to Memory line, Generate C Bit Out line and Step SAC+1 line. Add Address to Memory and E Time lines, with Auxiliary Trigger 2 Off line and SMT Off line positive, bring up the Storage Read Mode line. In FIG. 64*b*, the Add Address to Memory 1 line **64***a*.**04**, Auxiliary Trigger 1 On line **138***i*.**19**, and Auxiliary Trigger 2 Off line **138***l*.**15** and the Decimal Carry In line **88.27** bring up the Route Zone Carry In line **64***b*.**05**. When Storage Address 31 is read CR 2 will contain a 1 bit and the CR–2 line **75.46** will become positive and with the AAM 1 line, the Auxiliary Trigger 1 On line and the Auxiliary Trigger 2 Off line will provide a positive signal on the A bit to T/C line **64***b*.**06**.

In FIG. 3*b*, the $\overline{20{,}000}$ line, $\overline{80}$ line, $\overline{40}$ line and $\overline{20}$ line are positive to bring up the 00 line **3***b*.**01**. In FIG. 5*a*, the 00 line **3***b*.**01** makes negative the $\overline{00}$ line **5***a*.**02**. The remaining NOT lines are positive. In FIGS. 5*b* and *c*, all of the output lines are driven except the 00 line **5***b*.**01** when the Memory Read Bias Gate comes up. In FIG. 8, all of the columns are driven with reset current except the column linked by the 00 line **5***b*.**01**. In FIG. 3*d*, the $\overline{10{,}000}$ line, $\overline{10}$ line, $\overline{4}$ line, $\overline{8}$ line, $\overline{2}$ line and the 1 line are positive to bring up the 0–4 line **3***d*.**01**. In FIG. 7*a*, the 0–4 line **3***d*.**01** makes negative the $\overline{0\text{–}4}$ line **7***a*.**02**. The remaining NOT lines are positive. In FIGS. 7*b* and *c*, all of the output lines except the 0–4 line **7***b*.**01** are driven. In FIG. 9, all of the columns of cores are driven with reset current except the column linked by the 0–4 line **7***b*.**01**. In FIG. 3*a*, the $\overline{8000}$, $\overline{4000}$, $\overline{1000}$, and $\overline{2000}$ lines are positive and the 0000 line **3***a*.**01** is up. In FIG. 4, the 0000 line **3***a*.**01** is positive and when the Memory Y Read Gate is supplied on the line **5***g*.**08** the 0000 line **4.01** is positive. In FIG. 8, the row of cores linked by the 0000 line **4.01** is driven with set current. Accordingly, the 0000 switch core is set to the "one" state and an output is provided on its secondary. In FIG. 3*c*, the $\overline{800}$, $\overline{400}$, $\overline{100}$ and $\overline{200}$ lines are positive and the 000 line **3***c*.**01** is up. The latter line and the Memory X Read Gate line **5***g*.**07** provide a positive output on the 000 line **6.01**. In FIG. 9, the row of cores linked by the 000 line **6.01** is driven with set current and accordingly, the 0–4 switch core is set and an output is provided on the secondary to the Core Array of FIG. 13. In FIG. 13, the 0 lines are

driven with reset current and those cores of the thirty-five planes of addresses 0000–0004 which contain "ones" are reset and the sense windings are sampled at $R_{3.5}$ and the triggers of the Memory Buffer Register are set according to the bit configurations read. In FIG. 3*e*, the $\overline{8}$, $\overline{2}$, $\overline{4}$ and 1 lines are positive to bring up Select Character 1 line **3***e*.**03**. In FIG. 136*b*, the Mode Control Trigger On line **136***e*.**34** is down, bringing down the Low Character line **136***b*.**04**. In FIG. 20*a*, this line, plus the positive signal on the Select Character 1 line **3***e*.**03** brings up the Select Character 1 Out line **20***a*.**05**. The signal on Select Character 1 line **3***e*.**03** is gated onto the Select Character 1 Out line **20***a*.**05**. In FIG. 20*b*, the Character 1–C line, the Character 1–B line, the Character 1–A line and the Character 1–1 line are positive and the Select Character 1 Out line **20***a*.**05** gates the bits onto the C, B, A and 1 bits lines of FIG. 20*b* where the signals are passed to CR 1 which is then set to the bit configuration at W_0.

During Execute cycle 6, a Start cycle, SASR remains at 31 and this address is read from as in previous cycles except in this instance CR 2 is set to the Digit 1 with binary "zeros" in the B and A bit positions. Accordingly, at W_0, CR 2 contains the digit 1, binary "zeros" in the B and A bit positions. CR 1 contains the digit 1 and binary "ones" in the B and A bit positions. Since the ten thousands order of the Memory address is to be formed, the digit 1 in CR 2 is to be added to the zone bits present in CR 1 and the Decimal Carry In is to be added as well. This addition is accomplished in the Zone Adder during the Write portion of Execute cycle 6 and the Read portion of Execute cycle 7. In FIG. 64*b*, the Decimal Carry In line **88.27** is positive since the decimal carry trigger is On. The CR 2–1 line **75.46** is positive to represent the digit 1 in CR 2. Add Address to Memory 1 line **64***a*.**04**, Auxiliary Trigger 1 On line **138***i*.**09** and Auxiliary Trigger 2 Off line **138***l*.**15** are positive to bring up the Route Zone Carry In line **64***b*.**05** and the A bit to T/C line **64***b*.**06**. The signal on the Route Zone Carry In line is routed to FIG. 93*d* to FIG. 79. The A bit to T/C signal is routed to FIG. 93*f* to FIG. 79 and the Zone Adder of FIG. 79. The Zone Carry In line **93***b*.**06**, CR 1 to Adder A line, CR 2–A line **75.09** and CR 1 to Adder B line **73.08** are positive. The result of adding the binary "one" bits B and A of CR1, the binary "one" A bit of CR2 and the Carry In is 101=5. This is expressed on the output lines of the Zone Adder as Result A lines **79.02** through **79.05** positive to indicate a binary "one" for the A bit position. Result B lines **79.06** through **79.09** are negative to indicate a binary "zero" in the B bit position and Zone Carry Out lines **79.10** and **79.12** are positive to indicate a Zone Carry Out. Since it is only the zone portions of the character at address 0001 of Memory which are to be added the digit 1 contained in the numeric portion of the character must remain unmodified. Accordingly, CR 2 to T/C is down so that the digit 1 passes unmodified to the Adder circuits to the Result Register. This is accomplished in FIG. 64*c* where the Auxiliary Trigger 1 Off line **138***j*.**15** is down to prevent CR 2 to T/C line **64***c*.**03** from being positive. At W_0 the outputs from the Zone Adder and the Digit Adder are set into the Result Register and the contents are then CBA8421=0010001.

Execute cycles 6 and 7 are Start and Transition cycles respectively since Turn On Transition Trigger has been maintained. Accordingly, in FIG. 136*a* the Transition trigger, Add trigger and Mode Control trigger have been turned On in the manner previously described. Since Execute cycle 7 is then specified as a Transition cycle the results contained in the Result Register are written into Memory at address 0001. Stepping of MAC 1 has been suppressed by the Auxiliary Trigger 1 Off line and MAC 1 retains address 0001. MASR retains the same address. The details of writing the contents of the Result Register into Memory will be omitted in view of the explanations given previously. The contents of Memory addresses 0000–0004 are now:

Address	C	B	A	8	4	2	1
0	1	1	1	0	1	1	1
1	0	0	1	0	0	0	1
2	1	1	1	0	1	1	1
3	0	0	1	0	1	1	1
4	0	0	1	0	1	1	1

Referring now to the chart immediately above, it is pointed out that the B bit position of character 4 contains a 0 and it is this bit which must be changed in response to the Zone Carry Out provided during the last computation.

In FIG. 88, the Zone Carry Out was provided on the line **79.11** and set into the Zone Carry trigger at W_0 of Execute cycle 7. It now becomes necessary to refer to the character in Memory address 0004 in order to modify the B bit according to the setting of the Zone Trigger and this implies that Execute cycles 8 and 9 must be taken to perform this final manipulation.

During Execute cycle 7, the Transition line **136***c*.**01** is positive so the Add trigger is turned Off by the A_2/R_3–W_1 pulse on the line **103***b*.**12**. Also, the same transition line conditions a diode gate for the passage of the A_3/R_4–W_2 pulse on the line **103***b*.**07** which turns Off the Mode Control trigger. The Add Trigger Off line **136***b*.**18**, now positive, is used with the W_2 (D1) line **102.17** to turn Off the Transition trigger. However, during Execute cycle 7 and prior to the Transition trigger being turned Off, at W_2, Set MAC 1 to MAR line **64***b*.**01** and Turn On Auxiliary Trigger 2 line **64***b*.**02** are made positive in FIG. 64*b* by the AAM **1** line **64***a*.**04**, the Transition line **136***c*.**07** and the Auxiliary Trigger 1 On line **138***i*.**19**. As mentioned previously, MAR remains unchanged throughout the Add to Memory operation. Accordingly, the Set MAC 1 to MAR line is effective to set 0004 into MAC 1 at W_1 of Execute cycle 7. In FIG. 138*k*, the Turn On Auxiliary Trigger 2 line **93***k*.**03** is positive and at W_2 of Execute cycle 7 the pulse on the line **103***b*.**16** turns On Auxiliary Trigger 2.

During Execute cycle 7, the Storage Read Mode was in effect as mentioned previously. Accordingly, Storage address 32 was read and the Storage Mark was placed in CR 2. This Storage Mark is detected and provides that on subsequent cycles the Storage Read Mode will not be used. This is shown in FIG. 64*a* where the SMT Off line **136***d*.**12** is negative and in Execute cycles 8 and 9 reading from Storage is avoided. In FIG. 64*c*, Auxiliary Trigger 1 On line **138***i*.**20** and AAM 1 line **64***a*.**05** maintain Turn On Transition Trigger line **64***c*.**06** positive which will later specify Execute cycle 9 to be a Transition cycle.

At R_0 of Execute cycle 8, MASR is set to Memory address 0004 and reading from Memory is accomplished in the same manner as in Execute cycle 1 and at W_0 CR 1 is set to the contents of Memory address 0004 which is CBA8421=0010111. During Execute cycle 8, the lines Memory Read Mode, CR 1 to Adder, Digit Adder Out and Generate C Bit Out are up as indicated in FIG. 64*a*. Auxiliary Trigger 1 is On, Auxiliary Trigger 2 is On, so Zone Adder Out, B bit to T/C, and Turn On Transition Trigger are routed. Note that CR 2 to T/C is not used and, accordingly, the numeric contents of CR1 pass to the Result Register unmodified. Although the Zone Carry trigger was turned On, it was not used directly.

In FIG. 79, the CR 1 to Adder B line **73.08** is positive since the B bit position of CR 1 contains the binary "one" indicating Indirect Addressing. The CR 1 to Adder A line **73.01** is down indicating a binary "zero" in the A bit position of CR 1. In FIG. 64*b*, Auxiliary Trigger 2 On line **138***k*.**11** and AAM 1 line **64***a*.**05** make positive the B bit to T/C line **64***b*.**03**. This signal is passed through FIG. 93*j* to the Zone Adder of FIG. 79 where it makes

positive the CR 2–B line **75.03**. During the Write portion of Execute cycle 8, the Transition trigger, Add trigger and Mode Control trigger are turned On in the usual manner and from W_2 of Execute cycle 8 to W_2 of Execute cycle 9 Transition Trigger On line **136***e*.**21** is positive. In FIG. 64*a*, this line with Add Address to Memory line **23***l*.**02** and E Time line **123.11** bring up Suppress Zone Carry In line **64***a*.**10**. In the Zone Adder of FIG. 79, the Zone Carry In is not provided. As a result of the inputs and the Zone Adder Out signal on **93***b*.**02**, Result A lines **79.02** through **79.05** and Result B lines **79.06** through **79.09** are positive. The Result Register now has positive signals on the B, A, 4, 2 and 1 lines indicating the digit 7 with binary "1" bits in the B and A position. A C bit is furnished from the C Bit Generator and at R_4 the triggers of the Result Register are set to the bit configuration of CBA8421=1110111. Since MAC 1 has not been stepped, MASR contains the address 0004 and during Execute cycle 9 the contents of the Result Register are written into Memory address 0004. As a result, at the end of Execute cycle 9, Memory addresses 0000–0004 contain:

Address	C	B	A	8	4	2	1
0	1	1	1	0	1	1	1
1	0	0	1	0	0	0	1
2	1	1	1	0	1	1	1
3	0	0	1	0	1	1	1
4	1	1	1	0	1	1	1

or

	0	1	0	1
	1	1	1	1
G	1	7	7	7

The G indicates the operation code and has remained unaltered during the Add Address to Memory operation. The Zone bits of the thousands order and the B bit of the units order, taken with the numeric portions of the units, tens, hundreds and thousands orders indicate a Memory address of 51,777. The Zone Bit configuration of the tens and hundreds positions indicate ASU coding of 13. The Indirect Addressing bit indicated by the 1 in the A position of the units order remains uneffected by the operation. During the latter portion of Execute cycle 9 the Add trigger, Mode Control trigger, Transition trigger are turned Off as previously described. In FIG. 64*b*, the AAM 1 line **64***a*.**04**, the Transition line **136***c*.**27** and the Aux. Trigger 2 On line **138***k*.**18** make positive the End E Time line **64***b*.**04** before W_2 of Execute cycle 9. The signal on the End E Time line passes through FIG. 93*r* to the I/E Trigger of FIG. 121 where it conditions a diode gate for the fall of the A_3/R_4–W_2 line **104.10** which switches the trigger from E to I and specifies that the next cycle shall be an Instruction cycle in which the instruction is taken from address 0013 as specified by the Instruction Counter.

It has been illustrated and described how a storage device may be addressed for reading from one address and writing into another during the same cycle and also, for the Data Processing System described herein, a first apparatus was disclosed for use with Memory and a second apparatus was disclosed for use with Storage. However, it is pointed out that various combinations of the structure taught may be employed in the practice of the invention.

The five character parallel read-out system for Memory may be replaced by the single character read-out system of the type used for Storage. This modification requires an Instruction time of five cycles (in the manner shown and described in application "Electronic Multiplier," Serial No. 512,626, filed June 2, 1955, and referred to previously), and so modified, Memory and Storage would then operate in like fashion. More specifically, Memory Read/Write Mode and Storage Read/Write Mode would be identical in operation.

With Memory operating on a single character read-out basis, an Instruction Time, comprising a five stage ring, would be employed to provide four 9 microsecond R/W cycles and a fifth 13 microsecond R/A/W cycle to obtain the Operand. The first order of the Instruction Counter would now contain four triggers (instead of one as described previously) and would be adapted to step minus one. The Minus carriers would be blocked between the first and higher orders. If the IC started at a units order address of 4, the five Instruction cycles would cause it to sit at 9, the proper value for the next instruction. And blocking the carries into the higher orders would cause the higher orders to have the correct value for the next instruction. If the IC started at a units order address of 9, the five I cycles would cause it to hold a 4 in the units order, again proper, and the blocking of carries into the higher orders would cause the address to be low by the amount 10. Here, a correction pulse is entered into the tens order to cause the IC to step plus 10. The PCT cable would now provide single character transmission from and to Input/Output units.

Refer now to the X Switch Core of FIG. 40. When using Storage Read/Write Mode as described in the Example of Add, the following four patterns of events occur during an execution series:

Chart VII

R_{odd} . . . | $R_{even}W_{odd}$ | $R_{odd}W_{even}$ | . . . | . . . W_{odd}
A_{odd} A_{even} . . . A_{odd}

R_{odd} . . . | $R_{even}W_{odd}$ | $R_{odd}W_{even}$ | . . . | . . . W_{even}
A_{odd} A_{even} . . . A_{even}

R_{even} . . . | $R_{odd}W_{even}$ | $R_{even}W_{odd}$ | . . . | . . . W_{odd}
A_{even} A_{odd} . . . A_{odd}

R_{even} . . . | $R_{odd}W_{even}$ | $R_{even}W_{odd}$ | . . . | . . . W_{even}
A_{even} A_{odd} . . . A_{even}

The four cases arise because a series may begin or end with either an odd or an even address. Note that in a succession of Read or a succession of Write portions, an even address follows an odd address and vice versa.

Referring now to the Y Switch Core Matrix of FIG. 39, this 4×4 matrix is duplicated with corresponding cores having their secondaries in *series*. The first of the 4×4 matrices is employed for reading and writing odd addresses and the second of the 4×4 matrices is for reading and writing even addresses. Consider the following sequence:

$Read_{30}$ . . . | $Read_{31}Write_{30}$ | $Read_{32}Write_{31}$ | $Read_{33}Write_{32}$
Add_{30} Add_{31} Add_{32}

30 is an even address. Therefore, the second Y Switch Core Matrix has its 0 switch core and the X Switch Core Matrix of FIG. 40 has its 30 switch core set. Writing is suppressed in the usual manner during the first cycle and the two cores remain set. During the Read portion of the second cycle the 0 switch core of the first Y matrix is set and the 31 core of the X matrix is set. During the Write portion of the second cycle, the 0 core of the second Y matrix is reset and the 30 core of the X matrix is set to write into address 30. At the end of cycle 2, the 0 core of the first Y matrix and the 30 core of the X matrix remain set. During the Read portion of the third cycle, address 32 is read from by setting the 32 core of the second Y matrix and the 0 core of the X matrix. During the Write portion of the third cycle the 0 core of the first Y matrix and the 31 core of the X matrix are reset to write into address 31. At the end of the third cycle, the 32 core of the second Y matrix and the 0 core of the X matrix remain set for writing into address 32 during the Write portion of the fourth cycle. Assuming that an odd address was read from during the first cycle of a given sequence, then the first Y switch core matrix is employed during the first cycle and thereafter the first and second Y matrices alternate to provide reading and writing according to the Chart above.

It will be appreciated that there are no critical addresses

as each of the sequences of Chart VII are accomplished, and the cycle delay introduced by recognition of critical addresses and turning On the Auto Transition trigger is eliminated.

The arrangement described above permits *any* odd address to follow *any* even address, not merely the adjacent even address.

However, according to the principles of this invention, any odd address may follow any other odd address and any even address may follow any even address in a random, although planned, sequence as will be described hereafter. Henceforth, the term random addressing apparatus will be used to refer to the circuits described below.

Consider the two portions of the X Switch Core Matrix of FIG. 40 as the First Odd X Matrix and the First Even Matrix. A matrix identical in construction and having odd and even parts will be a Second Odd Matrix and a Second Even Matrix. For each switch core of the present matrix there is a corresponding switch core in the Second X Matrix and the secondary windings for corresponding switch cores connected in series so that half-select current is provided to the X axis of FIG. 40 from one or the other of the two X switch core matrices on the same drive line. Corresponding cores in the two X switch core matrices are excited by the same Write Drivers of FIGS. 38*b* and *c*, but eight additional Read Drivers, such as the ones of FIG. 35, are provided. Thus, selection of one of the First or Second X Matrix is provided by selection of the corresponding set of Read Drivers.

The present eight read lines are now First 24 Odd lines **35.08** through First 0 Even line **35.01**. Corresponding lines for the Second X Switch Core Matrix are Second 24 Odd through Second 0 Even lines. All that is required is that triggers be employed for which the binary states designate First and Second X Matrices so that operations alternate between the First and Second X Matrices regardless of the addresses involved. Similarly, Y Switch Core Matrices are provided as follows: First Odd Y Matrix and First Even Y Matrix (as described previously) and Second Odd X Matrix and Second Even Y Matrix. The First and Second Odd Y Matrices have secondary windings of corresponding cores connected in series and coupled to drive lines of the Y axis of the Storage Array of FIG. 45; the First and Second Even Y Matrices have secondary windings of corresponding cores connected in series and coupled to the drive lines of the Y axis of the Storage Array of FIG. 45.

With two logically independent addressing circuits for the Storage Array, there need be furnished first and second addresses. In this regard, refer to FIG. 152 wherein there is shown first and second Storage Address Select Registers **152–1** and **152–2** respectively, whose addresses are used to excite the First and Second Switch Core Matrices respectively. The input addresses may come from SAC **152–4** or the Random Storage Address cable **152–6** which receives address information according to a prearranged plan. The setting of SASR I and SASR II is under control of a two-stage ring composed of First Address and Second Address triggers. At the start of the Storage Read/Write Mode operations, the ring will specify First Address and thereafter alternate so that each of the First and Second Addressing circuits are operated in turn. Switching time of these triggers is at W_2 of Execute cycles. If the ring indicates First Address then SASR I is at the address of the cable **152–6** at R_0. If the ring indicates Second Address, then SASR II is set to the address of the cable at R_0.

As stated previously, if Core Memory is to operate in the serial-by-character mode, Core Memory **152–10** comprises seven planes and the capacity of MBR **152–12** is 7 bits. The addressing of Memory is similar to the one described concerning random addressing of Storage. Accordingly, First and Second X Switch Core Matrices and First Odd and Even and Second Odd and Even Y Switch Core Matrices are furnished for Core Memory. Memory Address Select Registers I and II, **152–12** and **152–14** respectively, are alternately selected for addressing Core Memory in any desired sequence of addresses. The Instruction Counter **152–16**, MAC 1 **152–18** and MAC 2 **152–20** are supplied with information from the Memory Address Register **152–22**. However, in the fashion described above, MASR I and MASR II may receive address information from a Random Memory Address Cable **152–24**. Should one of the Data Synchronizer Units signal for a PCT Request cycle, the Input/Output address enters the same MASR as would have been used had there been no PCT Request made. A normal Read/Write Cycle using the I/O address is provided for so that a single switch core in each of the X and Y Switch Core Matrices are switched during the cycle in the normal manner and the First and Second Address ring is suppressed from stepping.

It is not to be assumed that the principles described and illustrated with reference to addressing Storage and applied to Memory are to receive greater emphasis than the principles taught with reference to the Memory Read/Write Mode in Overlap Mode Control Operations. Storage may be construed and arranged for parallel read-out of multiple characters by increasing the number of core planes in multiples of 7 and increasing the capacity of the Storage Buffer Register. Then, the addressing features described and illustrated in Memory Read/Write Mode are fully applicable to use in the Storage Read/Write Mode. Accordingly, use of any combination of circuits employed in this invention is contemplated to satisfy the requirements of increased capacity and/or alteration of machine organization.

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EXPLANATION OF SYMBOLS

A is an AND circuit. —A is a negative AND circuit (+OR circuit). AC is a cascaded AND circuit. AM is a driver. AMD is a switch core read driver. AMP is a switch core write driver or ring circuit driver. AMR is a switch core driver. AMS is a sense amplifier. DG is a negative diode gate. DL is a delay line. GA and GAF are grounded grid amplifiers. GJ is a positive diode gate. I is an inverter. IC is a clock inverter. IF, IJ, IZI, IJK and IK are inverters. IN and INK are neon inverters. IPF is a pulse forming inverter. K is a standard cathode follower. KB is a power cathode follower. KC is a cathode follower clamp. KG is a plate level cathode follower. KJ, Kj, KJO and KMD are cathode followers. $\overset{\infty}{KO}$ is a cathode follower OR. KO is a cathode follower. KR is a cathode follower with a cathode resistor common with another cathode follower. KRA is a reset cathode follower. KS is a resistance gated diode driver. KZ is a power cathode follower. O and $\overset{\infty}{O}$ are OR circuits. OC and OCS are cascaded OR circuits. PKRZ is a peaker. RD is a relay driver. SS is a single short. SSE is a fast recovery single shot. T is a high speed trigger. TB is a Schmitt trigger. TC, TMS and TR are triggers. TS is a slow speed trigger. TT is a tape write trigger. XTAL is a crystal.

While there have been shown and described and pointed out the fundamental novel features of the invention as applied to a preferred embodiment, it will be understood that various omissions and changes in the form and details of the device illustrated and in its operation may be made by those skilled in the art without departing from the spirit of the invention. It is the intention, therefore, to be limited only as indicated by the scope of the following claims.

What is claimed is:

1. In a data processing system operating in cycles, apparatus comprising storage means for storing data manifestations at addressable locations, first addressing means for storing a value indicative of an address in said storage means to be selected for reading and writing, means for altering said value by a chosen amount after said data manifestations have been selected for reading and writing, second addressing means for indicating an address in said storage means to be selected for reading which corresponds to said value altered by said chosen amount, and means responsive to said first and second addressing means in sequence whereby data manifestations are obtained from said storage means at the address indicated by said value during a first cycle, data manifestations are obtained at the address indicated by said value altered by said chosen amount during a second cycle, and data manifestations are stored at the address indicated by said value during said second cycle.

2. In an instruction controlled data processing system operating in cycles, an addressable storage device, addressing means for obtaining data manifestations from and storing data manifestations in said storage device in a predetermined pattern, means for storing instruction manifestations in and obtaining instruction manifestations from said storage device according to a plan, said instruction manifestations comprising a part indicative of a particular operation to be performed and another part indicative of the address of data manifestations to be obtained, means for obtaining said instruction manifestations and decoding the same for controlling said system to perform said particular operation, means for furnishing said address part of the selected intsruction manifestations to said addressing means for obtaining data manifestations from and storing data manifestations in said storage device, and control means cooperating with said addressing means for sequentially obtaining data manifestations from the address specified by said adress part of said instruction manifestations during a first cycle, obtaining data manifestations from the address specified by said pattern during a second cycle, storing data manifestations at the address specified by said address part of said instruction manifestations during said second cycle, and then alternately obtaining data manifestations from and storing data manifestations in addresses according to said pattern during subsequent cycles.

3. In a data handling system, a storage device having a plurality of addressable locations, addressing means for storing signals representative of the addresses of said locations, means responsive to said addressing means for selecting a location of said storage device in accordance with the address signals for reading from and writing into said storage device, an address counter, and means for transferring signals from said address counter to said addressing means in accordance with a count contained in said address counter, said addressing means arranged to store the signals representative of the current address, for reading, and of the preceeding address for writing.

4. In a data processing system, apparatus comprising storage means including bistable devices the states of which represent units of data stored at addressable locations, means providing address representations to said Y and X matrices, first and second Y address matrices operably associated with said storage means and alternately operated to select first and second blocks of addressable locations, and first and second X matrices, each comprising odd and even sub-matrices, operably associated with said storage means and alternately operated to select first and second addressable locations within said blocks of addressable locations selected by said Y address matrices.

5. In a data processing system, a rectangular array of rows and columns of bistable devices, means including first and second Y addressing matrices coupled to said

array and alternately operable to select a particular column of bistable devices, means including first and second X addresing matrices coupled to said storage array and alternately operable to select a particular row of bistable devices, each of said first and second X matrices comprising odd and even sub-matrices for alternate operation therebetween, addressing means for obtaining data manifestations from and storing data manifestations in said array at selected addresses, means supplying address representations to said addressing means, means detecting data manifestations read from said array at addresses selected by said addressing means, and means supplying data to said array for stoarge therein at addresses selected by said addressing means.

6. In a data processing system operating in cycles, apparatus comprising storage means for storing data manifestations at addressable locations, first addressing means for storing a pair of values associated with first and second addresses, second addressing means for storing a pair of values associated with first and second addresses, and means responsive to said first and second addressing means in sequence whereby data manifestations are obtained from said storage means at said first address during a first cycle, data manifestations are obtained from said storage means at said second address during a second cycle, and data manifestations are stored at said first address during said second cycle.

7. In a data processing system, apparatus comprising a buffer register for storing a plurality of units of data in ordered positions; means reading units of data serially therefrom; a utilization device coupled to said register for receiving said units of data serially; a storage device having addressable locations for storing a plurality of units of data and providing said units of data to corresponding positions of said register and for receiving data therefrom; a result register connected to said utilization device for receiving units of data serially therefrom; a switch coupled to said buffer register, said result register, and said storage device; and control means for selecting units of data from said storage device for parallel entry into said buffer register and for controlling said switch to cause the contents of the result register and said buffer register to be returned to said storage means, said result register contents being substituted for said buffer register contents at an address corresponding with the buffer register portion from which said units of data were read.

8. In a data processing system operating in cycles; apparatus comprising means for storing a plurality of units of data; a register coupled to said storage means; a utilization device coupled to said register and to said storing means; and addressing means including a counter, means arranged to alter the contents of said counter in a given direction each cycle by a predetermined amount and means for storing the contents of said counter in each cycle for utilization in the succeeding cycle; said addressing means adapted for reading units of data from said storage means into said register, for reading said units of data serially from said register to said utilization device and thereafter writing units of data from said utilization device into said storage means according to the value stored representing the contents of said counter which were used for reading the previous cycle.

9. In a data processing system, apparatus comprising storage means in which units of data are stored in addressable locations, first addressing means including odd and even sub-matrices for alternately selecting odd and even addresses within a block of addresses, second addressing means including a matrix for selecting a block of addresses, means operably coupling said first and second addressing means to said storage means and controlled by said first and second addressing means for selecting a unit of data according to a selected block of addresses and a selected address within a block of addresses and then selecting another unit of data according to said selected block of addresses and another address within a block of addresses.

10. In a data processing system operating in cycles, apparatus comprising means for storing at addressable locations a plurality of groups of data manifestations subdivided into units, a register coupled to said storage device, a utilization device coupled to said register and to said storage means, addressing means including a counter and means arranged to alter the contents of the counter in a given direction each cycle by a predetermined amount, said addressing means adapted for causing groups of data manifestations to be read from said storage means into said register according to the contents of said counter for causing a first of said units of data to be read from said register into said utilization device according to the contents of said counter and thereafter causing characters from said utilization device to be written into said storage means according to the contents of said counter, and means operably associated with said register, said utilization device and said addressing means for causing individual reading of units of data from selected locations in said register into said utilization device, the selected location differing in each instance from the contents of said counter by said predetermined amount in a given direction.

11. In a data handling system operating in cycles, a storage device having a plurality of addressable locations, addressing means for cyclically storing signals representative of the addresses of said locations, means responsive to said addressing means for selecting a location of said storage device in accordance with the address signals for reading data signals from and writing data signals into said storage device, an address counter selectively operable to advance in a given direction by predetermined increments each cycle after a first cycle, and means for transferring signals from said address counter each cycle to said addressing means in accordance with the contents of said address counter, said addressing means arranged to store the signals representative of the address of a location for writing data signals and arranged for providing signals representative of the initial contents of said counter for reading data signals during a first cycle and thereafter providing signals representative of the contents of said counter adjusted by said predetermined amount for reading data signals.

12. In a data processing system which operates in instruction and execution cycles, each execution cycle comprising a read portion and a write portion, apparatus comprising means storing at addressable locations character representations of values to be processed, means including an arithmetic device for processing said values during a write portion of a cycle and a read portion of the next cycle, means initially providing said values from said storing means to said arithmetic device during the read portion of a first cycle, means thereafter, in over and over sequence, obtaining new values during read portions of successive cycles while said arithmetic device is processing the preceeding values, means holding the same until processing is complete near the end of the read portion of the cycle in which said new values are obtained, means providing said new values to said arithmetic device near the beginning of the write portion of the same cycle, and means storing the results of said processing during the write portion of the last mentioned cycle.

13. In a data processing system arranged to perform various operations on data manifestations in machine cycles, each machine cycle comprising a read and a write portion, apparatus comprising storage means having addressable locations for storing instruction manifestations comprising characters defining said operations to be performed and data manifestations to be operated upon, an instruction interpreter coupled to said storage means for producing an indication of the type of operation defined by the instruction manifestations, first means coupled to said storage means for receiving data manifestations from

said storage means during the read portion of a machine cycle, second means operating on said data manifestations during the write portion of a cycle and the read portion of a succeeding cycle, said first means receiving different data manifestations during the read portion of said succeeding cycle, third means transmitting data manifestations during the write portion of said succeeding cycle while said second means is operating on said different data manifestations, fourth means maintaining the pattern of operations until recognition of a condition imposed by the instruction manifestations or by the absence of data manifestations, fifth means supplying said instruction manifestations to said interpreter, and addressing means for controlling said storage means to read data manifestations and supply the same to said first means during a read portion of a cycle and to receive data manifestations from said first means and store the same during a write portion of a cycle, said reading and writing at locations being accomplished according to a predetermined plan.

14. In a data processing system, apparatus comprising first and second storage means for storing units of data at adressable locations, first and second address select registers for said first storage means, third and fourth address select registers for said second storage means, first selection means controlled by said first and second address select registers for selecting locations in said first storage means for reading units of data therefrom and writing units of data therein, second selection means controlled by said third and fourth address selection registers for selecting locations in said second storage means for reading units of data therefrom and writing units of data therein, means supplying location manifestations to said address select registers, a utilization device operably coupled to said first and second storage means, and program means for selectively making effective said address select registers for reading units of data from said storage means into said utilization device and writing units of data from said utilization device into said storage means.

15. In data processing system including bistable devices arranged in a plurality of planes to form a rectangular storage array having addressable locations, X and Y switching lines, means for applying coincident current to selected ones of said X and Y switching lines for sensing the state of said bistable devices, means inhibiting the change of state of bistable devices in selected planes for setting the states of selected bistable devices, apparatus for reading data manifestations from one location address of said array and for writing data into another location address of said array by selection of two X and two Y switching lines in X and Y pairs comprising first and second Y address matrices, each comprising corresponding settable bistable devices whose changes of state supply read and write currents to a particular one of said Y switching lines of said array, first and second X address matrices, each comprising corresponding settable bistable devices whose changes of state supply read and write currents to a particular one of said X switching lines of said array, first reading means setting a pair of bistable devices, one in said first Y address matrix and one in said first X address matrix, designating a particular address, second reading means setting a pair of bistable devices, one in said second Y address matrix and one in said second X matrix designating another particular address, said first reading means operable in odd cycles and said second reading means operable in even cycles, first writing means for resetting the previously set pair of bistable devices in even cycles, and second writing means for resetting the previously set pair of bistable devices in odd cycles.

16. In an electronic data processing machine operating in instruction cycles and in execution cycles, said execution cycles comprising start, overlap and transition cycles, apparatus comprising, in combination, general storage having discrete addressable locations, intermediate storage having discrete addressable locations, a starting point counter holding the address of a signed value stored in said intermediate storage, an intermediate storage address counter, a general storage address register holding the address of a signed value stored in said general storage, a general storage address counter, a first character register coupled to said general storage, a second character register coupled to said intermediate storage, a true-complement circuit coupled to said character registers, an adder coupled to said true-complement circuit for transmitting manifestations representative of a sum, means initially operable during an instruction cycle causing an execution start cycle to follow said instruction cycle, execution means operable during execution cycles controlled by a manifestation derived from an instruction for producing a particular type of operation upon values in said general storage and intermediate storage, means operative during said instruction cycle for setting said general storage address counter to the contents of said general storage address register and said intermediate storage address counter to the contents of said starting point counter, addressing means responsive to the contents of said general storage address counter and said intermediate storage address counter, respectively, for reading out values stored in the respective location to said character registers durings the read portion of execution, start and overlap cycles, means for normally stepping said general storage address counter and said intermediate address counter and for selectively preventing stepping of said intermediate address counter during transition cycles, means for conditioning said true-complement circuits in accordance with the signs of the values and the kind of operation desired to transfer values representative of true numbers or complement numbers to said adder from said character registers, said addressing means causing the values in said first character register to be stored in said general storage means at the location from which it is obtained during the write portion of said execution start cycle, overlap control means responsive to the quantity of value and the type of operation for causing a series of execution overlap cycles to follow said execution start cycle and controlling the addressing means for writing the sum manifestations from said adder into said intermediate storage device at the location read from the previous cycle during the write portion of each execution overlap cycle, said addressing means causing read out from said general and intermediate storage means to said first character register and to said second character register, respectively, during each execution overlap cycle, means repeating the transfer of values to said character register, means for reading a value from said general storage into said first character register and via said first true-complement circuit to said adder, means for causing said addressing means to write the values in said first character register into said general storage and the sum in said adder into said intermediate storage, means for ascertaining that the last value to be processed in said adder has been read from said intermediate storage into said second character register, and means responsive to said overlap control means for causing an execution transition cycle, said addressing means thereupon during said execution transition cycle writing said sum manifestations from said adder into said intermediate storage means at the location read from the previous cycle.

17. In an electronic data processing machine operating in instruction cycles and execution cycles, said execution cycles comprising start, overlap and transition cycles, each execution cycle having read and write portions, in combination, first storage means having addressable locations, second storage means having addressable locations, a starting point counter holding the address of a signed value stored in said second storage means, a first storage address counter, a storage address register holding the address of a signed value stored in said first storage means, a second storage address counter, a first charac-

ter register coupled to said first storage means, a second character register coupled to said second storage means, a true-complement circuit coupled to said character registers, an adder coupled to said true-complement circuit, means initially operable during an instruction cycle providing an execution start cycle, execution means operable during execution cycles and controlled by a manifestation of an instruction for producing the desired operation upon selected values from said first and second storage means respectively, means operative during an execution start cycle for setting said first storage address counter to the setting of said storage address register and for setting said second storage address counter to the setting of said starting point counter, addressing means controlled by said first and second storage address counters for reading values located at the respective addresses into said first and second character registers respectively, means associated with said addressing means for inhibiting writing back to said second storage device from said second character register during said execution start cycle, recognition means for sensing the extent of the values in each of the storage means, overlap control means responsive to said recognition means and said execution means for initiating execution overlap cycles and controlling the number of such cycles to follow said execution start cycle, means for conditioning said true-complement circuits in accordance with the signs of the values and the execution means to provide true or complement values to said adder during execution, start and overlap cycles, said counters being stepped each execute start and overlap cycle and said execution overlap cycles being repeated until said recognition means indicates the last value is read from said first character register, means operative in response to said recognition and overlap control means to provide an execution transition cycle when the selected value in said storage means is exhausted, means associated with said addressing means effective during said execution transition cycle inhibiting reading said second character register contents into said adder via said true-complement controls, means associated with said addressing means operative during each overlap and transition cycle to write the contents of said adder into a location in said second storage means specified by the address read from in the previous cycle, and means operative during said execution transition cycle to produce an end of execution signal and thereby cause said machine to proceed to an instruction cycle.

18. In an electronic data processing machine operating in instruction, start, overlap and transition cycles, apparatus comprising first storage means having addressable locations, second storage means having addressable locations, means including a counter holding the address of a value stored in said second storage means, means including a counter holding the address of a value stored in said first storage means, a first register coupled to said first storage means, a second register coupled to said second storage means, arithmetic means coupled to said registers, means initially operable during an instruction cycle providing an execution start cycle, execution means operable during start, overlap and transition cycles and controlled by a manifestation of an instruction for producing the desired operation upon selected values from said first and second storage means respectively, addressing means controlled by said means including counters for reading values located at the respective addresses into said first and second registers, respectively, during start and overlap cycles, means associated with said addressing means for inhibiting writing back to said second storage device from said second character register during said start cycle, recognition means for sensing the extent of the value in each of the storage means, overlap control means responsive to said recognition means and said execution means for initiating execution overlap cycles and controlling the number of such cycles to follow said execution start cycles, means including counters responsive to said execution means for conditioning said arithmetic means to process said characters during start, overlap and transition cycles, said means including counters, means for adjusting by a prescribed amount said counters each execute start and overlap cycle in order to address new storage locations, means for repeating said execution overlap cycles until said recognition means indicates the last character is read from said first register, means operative in response to said recognition and overlap control means to provide an execution transition cycle when the selected values in said storage means are exhausted, means associated with said addressing means effective during said execution transition cycle inhibiting reading said second register contents into said arithmetic means, and means associated with said addressing means operative during each overlap and transition cycle to write the contents of said arithmetic means into said second storage means at the address read from in the previous cycle.

19. In an electronic data processing machine operating in instruction, start, overlap and transition cycles, apparatus comprising first storage means having addressable locations, second storage means having addressable locations, first addressing means containing address manifestations of a value stored in said first storage means and adapted to alter said value in a predetermined pattern and read and write from address locations in said first storage means, second addressing means containing the address manifestations of a value stored in said second storage means and adapted to alter said value in a predetermined pattern and read and write from address locations in said second storage means, said first and second addressing means providing reading from addresses during start and overlap cycles and said second addressing means providing writing into addresses read from during the previous cycle during overlap and transition cycles, means including arithmetic circuits coupled to said first and second storage means for receiving values therefrom, means initially operable during an instruction cycle for providing a start cycle, execution means operable during start, overlap and transition cycles and controlled by a manifestation of an instruction for producing the desired operation upon selected values from said first and second storage means, recognition means for sensing the extent of the value selected for processing in each of the storage means, overlap control means responsive to said recognition means and said execution means for initiating overlap cycles and controlling the number of such cycles to follow said start cycle, means responsive to said execution means for conditioning said arithmetic circuits to process said values during start, overlap and transition cycles, and means operative in response to said recognition and overlap control means to provide a transition cycle when the selected values in said storage means are exhausted.

20. In an electronic data processing machine operating in instruction, start, overlap and transition cycles, apparatus comprising first storage means having addressable locations; second storage means having addressable locations; first addressing means containing address manifestations of a value stored in said first storage means and adapted to alter said value in a predetermined pattern and read and write from address locations in said first storage means; second addressing means containing the address manifestation of a value stored in said second storage means, adapted to alter said value in a predetermined pattern, read and write from groups of address locations in said second storage means, each of said groups being represented by a major settable device and each address of said groups being represented by a minor settable device, a major and a minor device when set controlling the selection of address locations; said first addressing means providing reading during start and overlap cycles and said second addressing means providing reading during start and overlap cycles according to the set condition of a one of the major and a one of the minor settable devices and providing writing into ad-

dresses read from the previous cycle during overlap and transition cycles according to the set conditions of the major and minor settable devices used for reading during the previous cycle; means including arithmetic circuits coupled to said first and second storage means for receiving values therefrom; means initially operable during an instruction cycle providing a start cycle; execution means operable during start, overlap and transition cycles and controlled by a manifestation of an instruction for producing the desired operation upon selected values from said first and second storage means, recognition means for sensing the extent of the values selected for processing in each of the storage means and for sensing, in advance, the change from one group of addresses in said second storage means to another; overlap control means responsive to said recognition means and said execution means for initiating overlap cycles and controlling the number of such cycles to follow said start cycle; means responsive to said execution means for conditioning said arithmetic circuits to process said values during start overlap and transition cycles; and means operative in response to said recognition and overlap control means to provide a transition cycle when the selected values in said storage means are exhausted or when changing from one group of addresses to another.

21. In a data processing system operating in machine cycles a plurality of bistable devices arranged into a plurality of planes forming a rectangular storage array, X and Y switching lines, means for sensing the states of said bistable devices by coincident currents applied to selected ones of said X and Y switching lines, means for resetting the states of said bistable devices by inhibiting the change of state of bistable devices in selected planes, apparatus for reading data manifestations from one address of said array and writing data manifestations into another address of said array by selecting one Y and two X switching lines comprising a Y address matrix including settable bistable devices whose changes of state supply read and write currents to a particular one of said Y switching lines of said array, first and second X address matrices, one comprising settable bistable devices whose changes of state supply read and write currents to a particular one of the even of said X switching lines and the other comprising settable bistable devices whose changes of state supply read and write currents to a particular one of the odd of said X switching lines, first reading means operable in odd cycles setting a bistable device in said Y matrix and a bistable device in one of said X matrices, writing means operable in a first cycle resetting the bistable device in said matrix, second reading means operable in even cycles setting the previously-set bistable device of the Y matrix and a bistable device in the other of said X matrices, said writing means operable resetting the bistable device set in the Y matrix and the bistable device in said X matrix set by said first reading means whereby alternately set bistable devices of said X matrix are reset.

22. In a data processing system, apparatus comprising general storage means for storing character manifestations at addressable locations, intermediate storage means for storing character manifestations at addressable locations, reading means for obtaining a pair of said character manifestations, one from said general storage means and one from said intermediate storage means, from locations determined by a plan, arithmetic means coupled to said storage means for processing said character manifestations as they are received from their respective sources and forming a result, said reading means adapted to obtain a different pair of said character manifestations while said previously selected pair of character manifestations is being processed by said arithmetic means, and writing means for selectively storing said result when formed in one or the other of said storage means at a different address from the one last used for obtaining said different pair of character manifestations, additional means for detecting, in advance, the end of processing by said arithmetic means and then providing a signal to end operation, and further means for maintaining said pattern observed by said reading and writing means until said signal is recognized and in response thereto blocking said reading means from obtaining a different pair of character manifestations and storing the last-formed result.

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UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,027,081 March 27, 1962

Oliver D. Evans et al.

It is hereby certified that error appears in the above numbered patent requiring correction and that the said Letters Patent should read as corrected below.

Columns 23 and 24, chart II, under the heading "Remarks" and opposite "St Print", for "Skins" read -- Skips --; column 52, line 14, for "on" read -- one --; column 64, line 33, for "CR 1-1" read -- CR 1-1 --; column 79, line 5, for "crtical" read -- critical --; column 114, line 32, for '"zero"' read -- "zeros" --; column 121, line 47, for "23/.01" read -- 23/.02 --; column 131, line 16, for "bits", second occurrence, read -- bit --; column 137, line 56, strike out "∞" over KO, first occurrence, and insert the same over KO, second occurrence; same column 137, line 63, for "short" read -- shot --; column 138, line 40, for "adress" read -- address --; column 139, line 13, for "stoarge" read -- storage --.

Signed and sealed this 1st day of October 1963.

(SEAL)
Attest:

ERNEST W. SWIDER
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