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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : G02F 1/313, H04Q 3/52 — **A1**

(11) International Publication Number: WO 93/22708

(43) International Publication Date: 11 November 1993 (11.11.93)

(21) International Application Number: PCT/GB93/00923

(22) International Filing Date: 5 May 1993 (05.05.93)

(30) Priority data:
9209662.7 5 May 1992 (05.05.92) GB
92311876.4 31 December 1992 (31.12.92) EP
(34) Countries for which the regional or international application was filed: GB et al.

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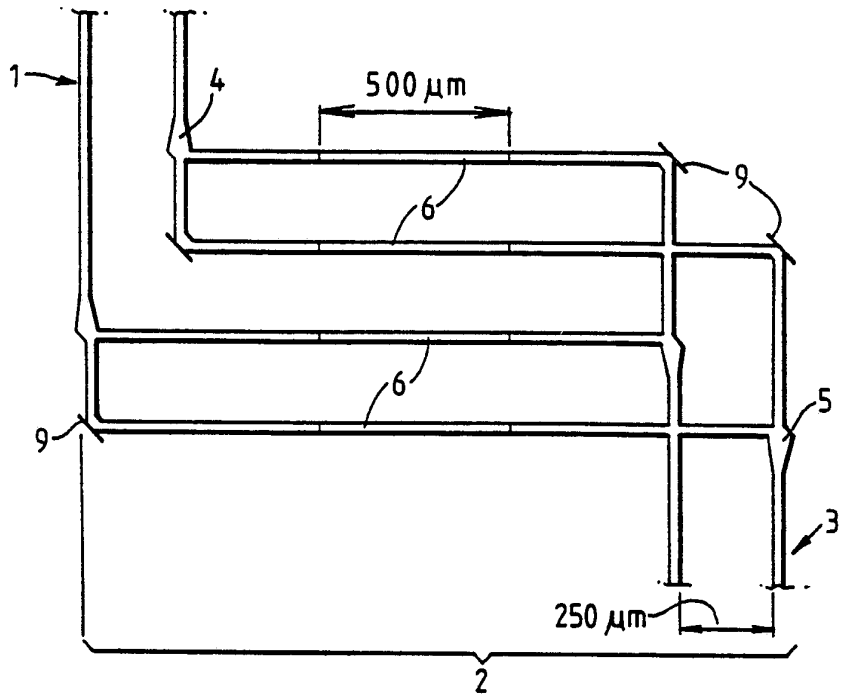
(81) Designated States: AU, CA, GB, JP, KR, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: OPTICAL SWITCHING DEVICE



(57) Abstract

A semiconductor optical switching device comprises a passive optical input stage (1), a matrix stage (2) and a passive optical output stage (3). The matrix stage incorporates active amplifiers (6), the switch as a whole being therefore part passive and part active. Control over the switching configuration is provided by electrical inputs to the amplifiers (6). The matrix stage (2) guides optical signals in a direction transverse to optical signals propagating in the input or output stages (1, 3). With this configuration, fixed change in direction of the optical paths available to optical signals propagating through the device are provided by splitters (4), combiners (5) and total internal reflection mirrors (9).

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OPTICAL SWITCHING DEVICE

The present invention relates to an optical switching device and finds particular application in optical communications systems.

Optical switching is expected to play an important role in future high capacity, for instance broadband, optical telecommunications networks. It is desirable to have all-optical switches in a communications network for several reasons, including the avoidance of a bit rate "bottleneck". Optical switching can offer:

1. Large bandwidth.
2. Avoidance of interfaces with electronics, thereby requiring less equipment than for instance electronic switching.
3. No conversion to electrical form or re-shaping necessary.
4. High switching speeds.
5. Complex modulation schemes, coherent signals or packets of wavelengths can be switched without optical demultiplexing and multiplexing.
6. Avoids discrepancies between optical transmission rates and electronic processing speeds.
7. Potential for an optically transparent network (can accept a wide range of data rates).

The semiconductor laser amplifier gate switch array is an attractive component, offering potential for zero insertion loss, polarisation insensitivity, low wavelength dependence, low crosstalk, high extinction ratio, high switching speed and simple drive conditions. Small size and scope for integration are both important criteria for the practical realisation of optical switches. Switches are known, including a 2x2 switch with waveguided Y-branched input and output, and a 2x2 switch in which the Y-branching is replaced by reactive ion etched (RIE) total internal reflection (TIR) mirrors instead of the waveguided Y-branching.

Known devices of the prior art which have relevance to the present invention are described in the following published documents:

a) "Monolithically Integrated 2x2 InGaAsP/InP Laser Amplifier Gate Switch Arrays" by M. Janson et al, Proceedings of the 17th European Conference on Optical Communications, Post Deadline Papers, pp 28-30,

b) GB Patent Application number 2227854A, in the name STC plc, published 8th August 1990.

The latter is entitled "Integrated Optics Asymmetric Y-Coupler" and provides a description of a fabrication technique for mirrors in optical semiconductor technology.

According to the present invention, there is provided a semiconductor optical switching device comprising passive optical input and output stages and a matrix stage, one or more inputs being selectively couplable to one or more outputs via the matrix stage to provide selective routing for optical signals input to the device, the material of the device in the matrix stage being at least in part active so that said selective routing can be controlled by control inputs to the matrix stage wherein the propagation direction of optical signals in both the input and output stages of the device is substantially the same, and said direction is substantially different from the propagation direction of optical signals in the active part of the matrix.

Thus, by providing that the input and output stages are in a substantially different direction to the active part of the matrix stage, switching devices according to the present invention have an architecture which can be relatively simply adapted to differing number of input and/or output paths, and which is thus scalable.

The matrix stage can thus be set out between the input and output stages so that virtually any number of optical paths can be "picked off" from the input stage and selectively connected to any one of up to a large number of optical paths in the output stage. For instance, the matrix

stage can be provided by optical paths lying generally transverse, for instance, at right angles, to the input and output stages. In the right-angled case, the input and output stages will be offset approximately by the length (in the direction of optical signals propagating in the matrix stage) of the matrix stage, though clearly other configurations might be applicable and advantageous.

Because switching devices according to embodiments of the present invention are part active and part passive, they can provide gain, thereby reducing insertion losses, while only simple drive conditions are required.

Embodiments of the present invention can provide a monolithically integrated amplifier gate switch matrix which provides a small device, compared with like devices of the prior art, and which introduces very low losses in use.

Preferably, changes in direction of propagation of optical signals following a single selected route in a device according to an embodiment of the present invention are provided by mirrors. By this means, the right angled configuration of the matrix stage with respect to the input and output stages referred to above can be provided. By getting away from what seems to be a widespread (optical) approach, in which optical paths are diverted as little as possible so that an incoming path tends to be gently branched and then continues in roughly the same direction, embodiments of the present invention can provide a device which is small, has passive input and output stages (being therefore less subject to faults for example losses and defects, than all-active devices), and is much more readily scalable in that the number of input and output lines are very easily multiplied up. Known devices do not provide this combination of advantages, and cannot provide the easy "scalability" at all.

Embodiments of the present invention will now be described, by way of example only, with reference to the accompanying figures, in which:

Figure 1 shows a plan view of a 2x2 laser amplifier gate switch optical path layout according to an embodiment of the present invention;

Figure 2 shows a schematic diagram of a power splitter and a mirror arrangement for providing changes in propagation direction for optical signals propagating from input to matrix stages in a device according to an embodiment of the present invention;

Figure 3 shows a perspective view of a layer structure providing a passive-active interface for use in a matrix stage of a device according to an embodiment of the present invention;

Figure 4 shows a graph of fibre-to-fibre gain for each of four different optical paths through a 2x2 device according to an embodiment of the present invention, plotted against amplifier injection current supplied to the matrix stage thereof, at 20°C;

Figure 5 shows a perspective view of the arrangement of Figure 2, further incorporating selective amplification stages coupled to said arrangement;

Figure 6 shows a graph of fibre-to-fibre gain in each arm of a 2x2 switch according to an embodiment of the present invention;

Figure 7, parts 1 to 8, shows fabrication steps involved in fabrication of an optical switch array according to an embodiment of the present invention;

Figure 8, parts 1 to 4, shows alternative active/passive structures for use in matrix stages of embodiments of the present invention,

Figure 9 shows a spontaneous emission spectrum for a device according to an embodiment of the present invention, and

Figure 10 is a schematic of a 4x4 switching device according to the present invention.

Referring to Figure 1, a path layout for a switching device according to an embodiment of the present invention

incorporates an input stage 1, a matrix stage 2, and an output stage 3.

The device, shown schematically in Figure 1, consists of 1x2 passive waveguide splitters 4 and combiners 5 integrated with an active section comprising four 500μm long amplifiers 6. The signal is routed by gating the amplifiers 6 on or off to give gain or absorption respectively.

The structure of the splitters 4 is shown more clearly in Figure 2, from which the design principle for the splitters 4 is clear. Each splitter, shown in Figure 2, incorporates a taper 7 to expand the beam horizontally followed by a TIR mirror 8 at 45^0 to the input 1 which reflects half of the light into a perpendicular arm having a passive section 10, with the other half transmitted undeflected to the mirror 9. The mirror 9 reflects all of remaining signal into the next passive section 10.

The dimensions of the device are 1mm x 2mm but could be reduced for instance by shortening passive sections 10 of the path layout.

The separation between the two inputs and the two outputs of the input and output stages 1, 3 of the device shown in Figure 1 is 250μm, this is chosen so that standard telecommunications fibres can be coupled to the input and output stages.

The layer structure and integration scheme is shown in Figure 3. The device operates at 1.55μm, and all layers can be grown by MOVPE.

The amplifier section 6 of the device has the following structure. The device is based on an n-doped InP substrate 50. A guide layer 15, 0.4μm thick, of InGaAsP material having a band gap equivalent wavelength λ_g of 1.1μm, is grown onto the substrate 50, again being n-doped. There is then an active layer 14, comprising 0.18μm of InGaAsP, having a band gap equivalent wavelength λ_g of 1.55μm, undoped, followed by p-doped InGaAsP as a cladding layer 13. This cladding layer 13 has a band gap equivalent wavelength λ_g again 1.1μm and is followed by a second p-doped cladding

layer 12, this time of InP, just under 1.9μm thick, with an uppermost ternary contact layer 11, of p-doped InGaAs.

The passive sections 10 can be formed by etching the InGaAs contact layer 11, p-doped cladding layers 12, 13 and the active layer 14 down to the 0.4μm InGaAsP guide layer 15, and then overgrowing with undoped InP 16.

This gives an active-passive coupling loss of 2dB with a simple fabrication scheme, allowing the high yields necessary for large switch arrays. It also achieves a good interface with very low residual reflectivity which is essential for low gain ripple.

The lateral mode confinement is provided by a ridge-waveguide structure, formed by methane-hydrogen RIE (reactive ion etching). The mirrors 8, 9 are defined by a known technique such as the one described in GB patent application 2227854A, referenced above, with a self-aligned photolithography stage and RIE. P-metallisation is provided as an electrical contact pad (not shown) and channels are etched in the p-metallisation and the InGaAs contact layer 11 between the amplifiers to provide electrical isolation.

A number of devices as described above were antireflection coated and the fibre-to-fibre gain was measured for each device as a function of current for each of the four arms, using lensed fibres for input and output coupling. A fibre-to-fibre loss of 4dB at an injection current of 200mA was achieved for TE input polarisation, shown in Figure 4. The fibre coupling losses account for 8-10dB of the total loss, giving a facet-to-facet gain of typically 5dB. The design should give the same loss in each arm, and the small differences were due to the fabrication process. The gain for TM polarisation was 4dB lower but the polarisation sensitivity could be improved with changes to the layer structure. The optical bandwidth is typically 50-60nm, with less than 1dB gain ripple at 200mA injection current. The passive sections 10 have a loss of 1-2dB/cm and the TIR mirrors 8, 9 have an excess loss of 3-4dB per facet. However, a mirror loss of 2dB has been achieved for passive

mirrors with improved etching techniques. The optical crosstalk between the channels was less than -45dB, most devices showing less than 50dB, with an on-off extinction ratio in excess of 45dB and in most cases greater than 50dB (unmeasurable). The amplifiers have a 200μm separation giving a gain variation due to the thermal interaction of less than 0.2dB.

In summary, the above provides a compact 2x2 laser amplifier gate switch matrix with only 4dB fibre-to-fibre loss, low crosstalk and high extinction ratio. Using TIR mirrors and active-passive integration there is established a technology suitable for fabricating large integrated switch arrays. Zero net fibre-fibre insertion loss is possible with further improvements in both the amplifying and passive sections 6, 10.

The above provides a description of the general structure of a switching device according to an embodiment of the present invention. Referring to Figure 5, the coupling of the input stage 1 to a matrix stage 2 is shown in more detail for a 1x2 switch layout. The structure shown in Figure 5 is substantially self-explanatory, being equivalent to that shown in Figure 3 and discussed above, and the reference numerals used therein indicate features equivalent to those of Figures 1 to 3. It might be noted, however, that the electrical contact pads 51 to drive the amplifiers 6 are shown in place, together with the metallisation 52 to the exposed face of the substrate 50. The metallisation to the amplifier 6 is provided by SiO_2 and Ti/Au and shows the split 53 between the areas of metallisation for adjacent amplifiers 6. There is also indicated an alternative ridge structure 54 for providing lateral confinement in the device, this being a double channel ridge structre 54, in place of the more simple ridge structures of Figure 2.

A further fabrication aspect indicated in Figure 5 is that the vertical sides of the ridge structures are provided by (110) planes in the InP materials while the TIR mirror 9 is provided by a (010) plane of material.

It might be noted that the Figure 5 embodiment is equivalent to that of Figure 2 in that the input 1 is aligned with the matrix stage 2 rather than being transverse thereto. The principles of fabrication are the same however.

Referring to Figure 6, fibre-to-fibre gain results in a 2x2 switch layout confirm the results shown in Figure 4. (The devices providing the results in Figures 4 and 6 were different and it can be seen that the results of Figure 4 showed improvement.)

Referring to Figure 7, a series of fabrication steps for achieving a suitable structure for use in a switch matrix according to an embodiment of the present invention incorporates known fabrication techniques, growth being carried out where relevant by metal-organic vapour phase epitaxy. The steps are indicated respectively in parts 1 to 8.

Referring to Figures 3, 5 and 7, but particularly to Part 1 of Figure 7, first of all the layers from the guide layer 15 through to the contact layer 11 are grown onto an InP substrate 15. In Part 2 of Figure 7, two options are shown for growing in the passive sections 10. In the first of these, SiO_2 55 is put down in a strip 500µm wide to establish the length of the amplifier regions 6. The layers are then etched away in the absence of the SiO_2 55, in the passive regions 10. The second technique shown in Part 2 of Figure 7 uses only thin strips of SiO_2, each 10µm wide to define the ends of the amplifier region 6.

As shown in Part 3 of Figure 7, the layers of the passive waveguiding regions 10 are then grown in at either end of the amplifier region 6. Again, two alternative techniques are shown, these being to remove all the 500µm length of SiO_2 55, thus removing the InP polycrystalline material grown above the active Section 6, or to protect the material of the passive waveguiding regions 10 while the material over the amplifying regions is removed, both InP and SiO_2.

Referring to Part 4 of Figure 7, a continuous layer of SiO_2 56 is then provided over the whole wafer and openings 57 created to define the mirrors 9 and splitters 4. These openings 57 are protected by resist during the stage shown in Part 5 of Figure 7, which is etching of the ridges to provide lateral confinement in the amplifiers 6 and passive waveguides 10. The depth of the ridges can be controlled by timing or by the use of a stop etch layer. The resist material protecting the openings 57 is then removed and photoresist put in place to protect the waveguides during mirror etching below the openings 57. Mirror etching is then carried out through the openings 57. This is followed, as shown in Part 7 of Figure 7 by passivation and etching of contact windows, using SiO_2 as the passivating material 58.

Lastly the p metallisation 51 and the n metallisation 52 is put in place, with thinning as necessary, and the SiO_2 passivation material 58 is removed. The p metallisation might be put down by a known technique such as electron beam deposition of Ti/Pt/Au. The n metallisation might for instance comprise Au on a layer of Ti.

Alternatively, it might be preferred to use sputtered Ti/Au as the p metallisation, rather than the electron beam deposited layer described above.

It might be noted, in the above structure, the amplifier section 6 has a higher ridge structure than the passive waveguiding portions 10, this affecting the onset of higher order modes in known manner.

Referring to Figure 8, various structures might be used to achieve the switch matrix and these are set out in parts 1 to 4, including incorporation of a stop-etch layer 40 to ease fabrication or of a 1.1μm quaternary (Q) guide layer 41. The active/passive transition may be provided by "etched then buried" structure 42, as described with reference to Figure 7, or by a similar structure achieved instead by diffusion of zinc as a dopant into undoped InP, to form the active section 43 as shown in Part 4 of Figure 8.

The approach shown in Part 3 of Figure 8, using the guide layer 41, can provide better coupling efficiency at the active/passive interface, but might introduce growth irregularities.

In Part 4 of Figure 8, it might be noted that the material providing the active layer 14 of the amplifier region 6 will be etched away from the passive regions 10 prior to overgrowth with undoped InP, followed by the zinc diffusion step mentioned above.

(Reference numeral 43 in Figure 8 is equivalent to reference numeral 6 in other Figures of this specification. It should also be noted that the structures shown in side view in the Figures, particularly Figures 7 and 8, are not shown to scale, for instance the substrates 50 in practice being significantly thicker than the ridge depth.)

Referring to Figure 9, measurements of the spontaneous emission spectrum of a switch matrix according to an embodiment of the invention, driven at an amplifying current of 170mA, peaked at just below 1520.1nm.

Referring again to Figure 1, the basic principles of operation of a 2x2 optical switch are that it has two input waveguides 1 and two output waveguides 3. For each input, a signal may be routed to either of the two output arms 3, or broadcast to both outputs 3 simultaneously.

The input and output sections 1, 3 are passive waveguides, separated by a monolithically integrated optical amplifier section. Each input arm 1 is split in two by a 3dB power splitter 4. The resulting four waveguides 10 are then coupled to optical amplifiers 6. Each of these amplifiers 6 may be turned on or off to gate the signal, providing gain when turned on and attenuation when off. This gives a high extinction ratio. The amplifiers 6 are then coupled to passive waveguides 10 and combined passively into the two output guides 3.

Changes in direction of the available optical paths through the switch, in addition to the splitters 4 and

combiners 5, are provided by total internal reflection mirrors 9 to give a compact design.

It should be noted that, as mentioned in the introduction to this patent specification, the general layout of switch matrices according to embodiments of the present invention lends itself to "multiplying up" such that multiple inputs (more than 2) can be selectively coupled to multiple outputs (more than 2) if required, providing a type of optical bus system. This is shown schematically in Figure 10 for a 4x4 switching device. From Figure 4 it can be seen that the architecture of the switching device is particularly suitable for scaling to larger switch arrays, thus each of the input paths in the passive input stage 1 can be easily split into four separate paths by the use of splitters incorporating mirrors, each of these separate paths pass through a common, easily fabricated, amplifying matrix stage 2, and are then easily combined to form four output paths 3 by combiners incorporating mirrors. The whole switching device thus remains compact and easy to fabricate when extended to larger numbers of inputs and outputs.

The number of inputs and number of outputs of a switching device can be significantly different, but in order to maintain full flexibility in switching any input to one or more output, each input path should be split into the number of separate paths corresponding to the number of outputs. The concept of the offset layout is very versatile in this respect. It is not essential of course that the angles involved are 90^0, other angles possibly facilitating other configurations but retaining the offset layout.

CLAIMS

1. A semiconductor optical switching device comprising passive optical input and output stages and a matrix stage, one or more inputs being selectively couplable to one or more outputs via the matrix stage to provide selective routing for optical signals input to the device, the material of the device in the matrix stage being at least in part active so that said selective routing can be controlled by control inputs to the matrix stage wherein the propagation direction of optical signals in both the input and output stages of the device is substantially the same, and said direction is substantially different from the propagation direction of optical signals in the active part of the matrix.

2. A device according to claim 1, wherein changes in propagation direction of optical signals following a selected route in said device are provided at least principally by mirrors.

3. A device according to claim 2, wherein the matrix stage is set generally at right angles to said input and output stages, said input and output stages being offset approximately by the length of said matrix stage, such that an optical signal input to the device propagates in the input stage in a first direction, is deflected through substantially 90^0 at the matrix stage, traverses an active region and subsequently is deflected back to said first direction, on leaving said matrix stage, and consequently propagates in the output stage in said first direction but offset with respect to its path in said input stage.

4. A device according to claim 3 wherein the input stage comprises n input paths, the output stage comprises m output paths, the matrix stage comprises nxm active parts and each input path is split into m separate paths before the matrix stage by m-1 splitters each incorporating a mirror, and each

output path is formed from n separate paths after the matrix stage by n-1 combiners each incorporating a mirror.

5. A device according to any one of the preceding claims, based on the III-V materials system.

6. A device according to claim 5, having an indium phosphide substrate.

Fig.1

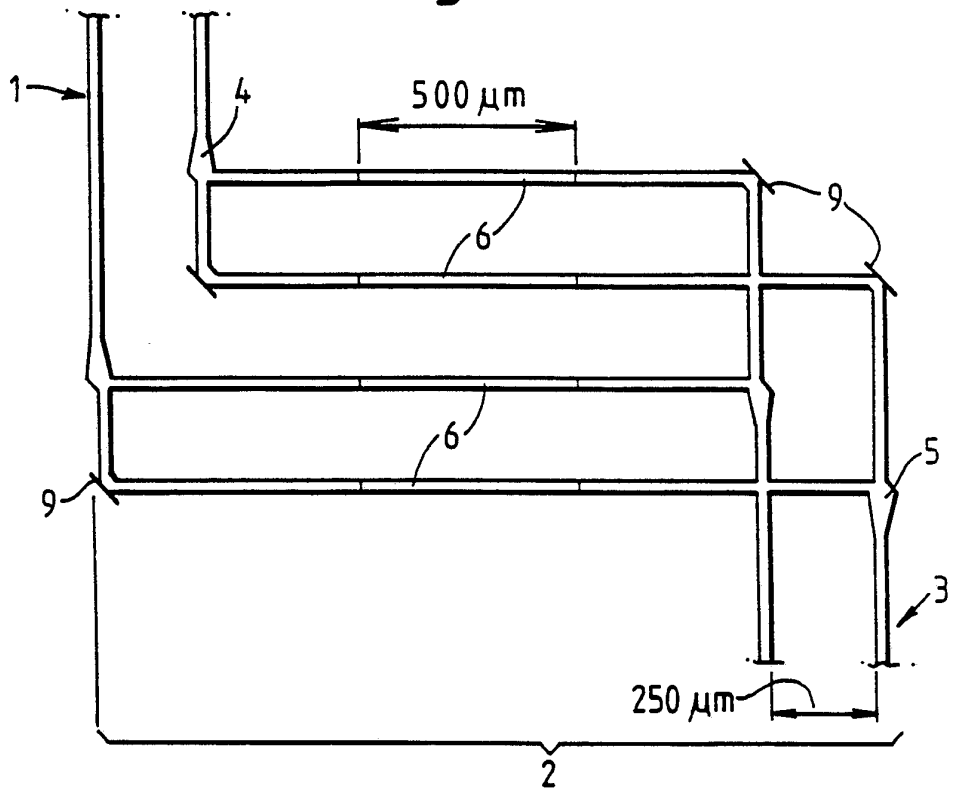


Fig.2

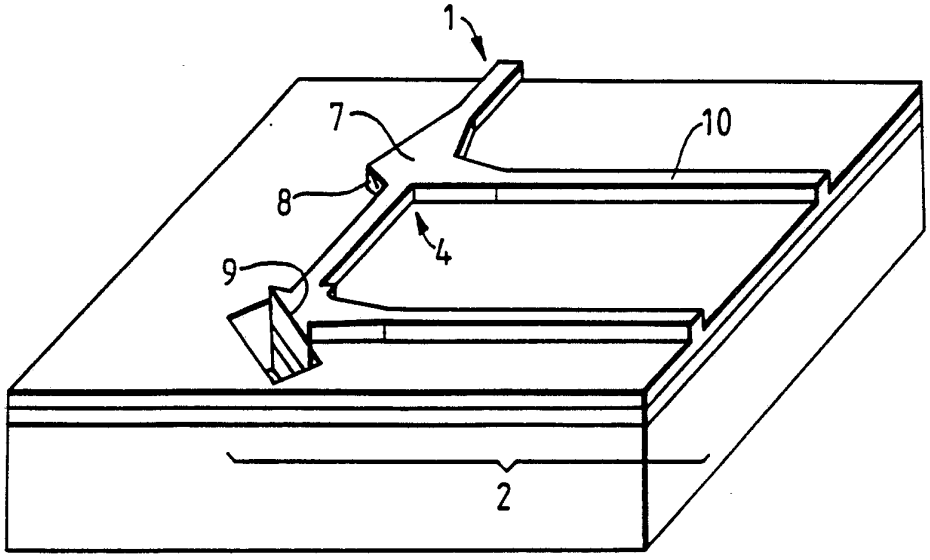


Fig.3

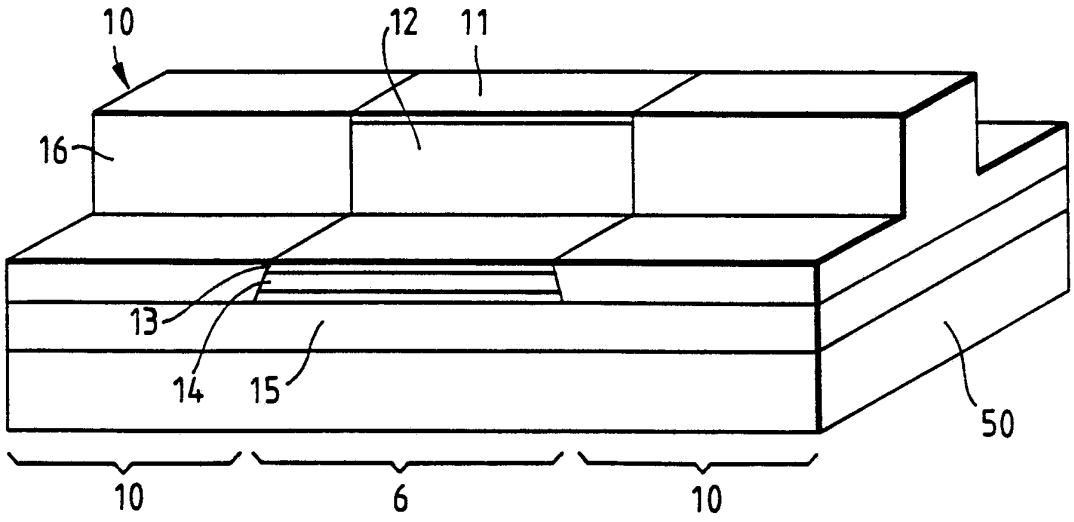

10
12
11
16
13
14
15
50
10
6
10

Fig.4

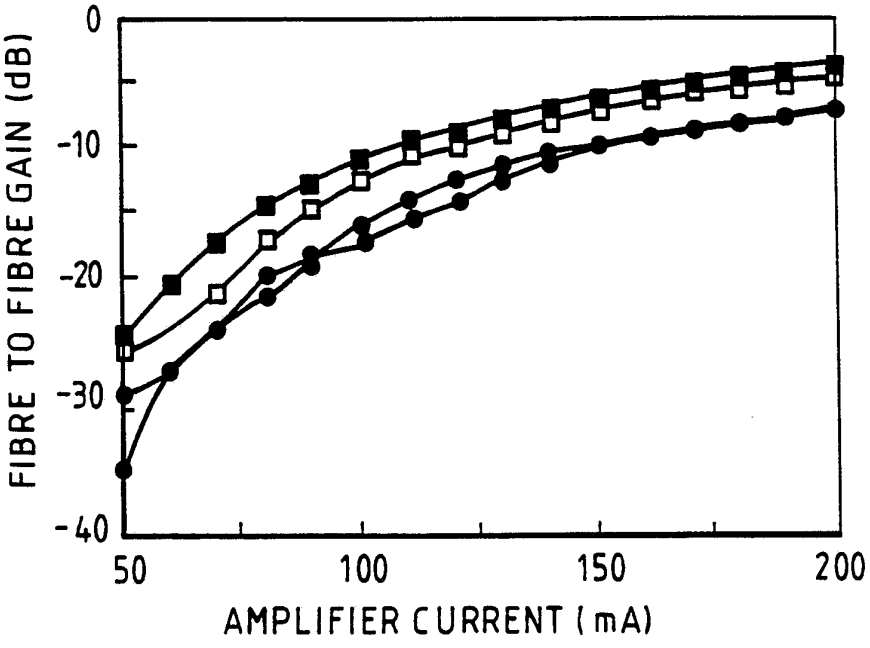

FIBRE TO FIBRE GAIN (dB)
0
-10
-20
-30
-40
50
100
150
200
AMPLIFIER CURRENT (mA)

Fig.5 1×2 OPTICAL SWITCH FABRICATION

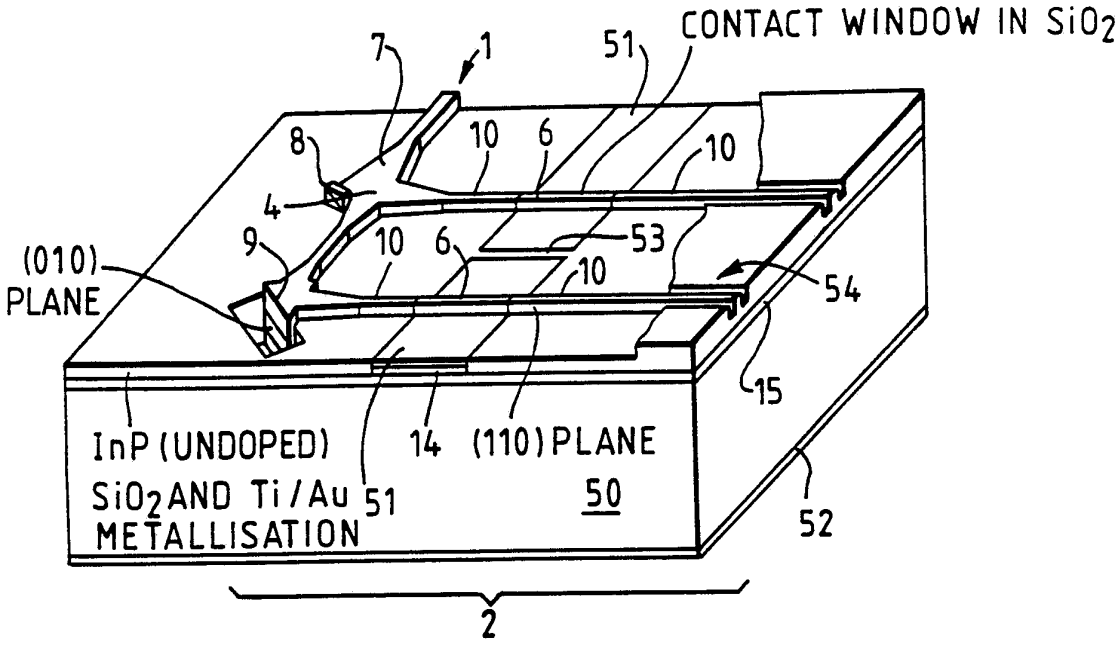


Fig.6

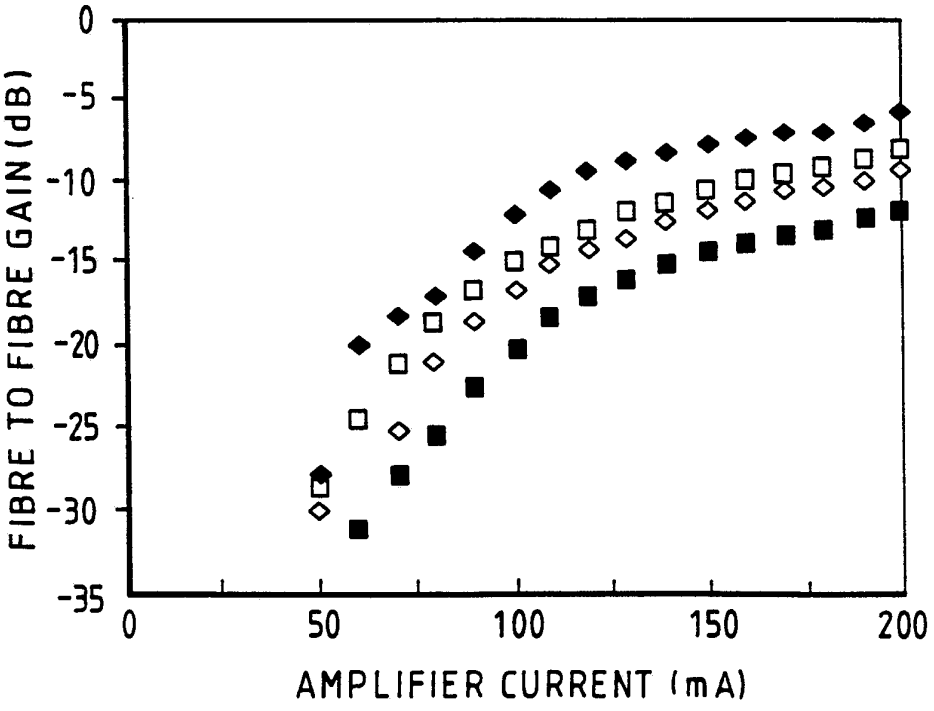


Fig:7

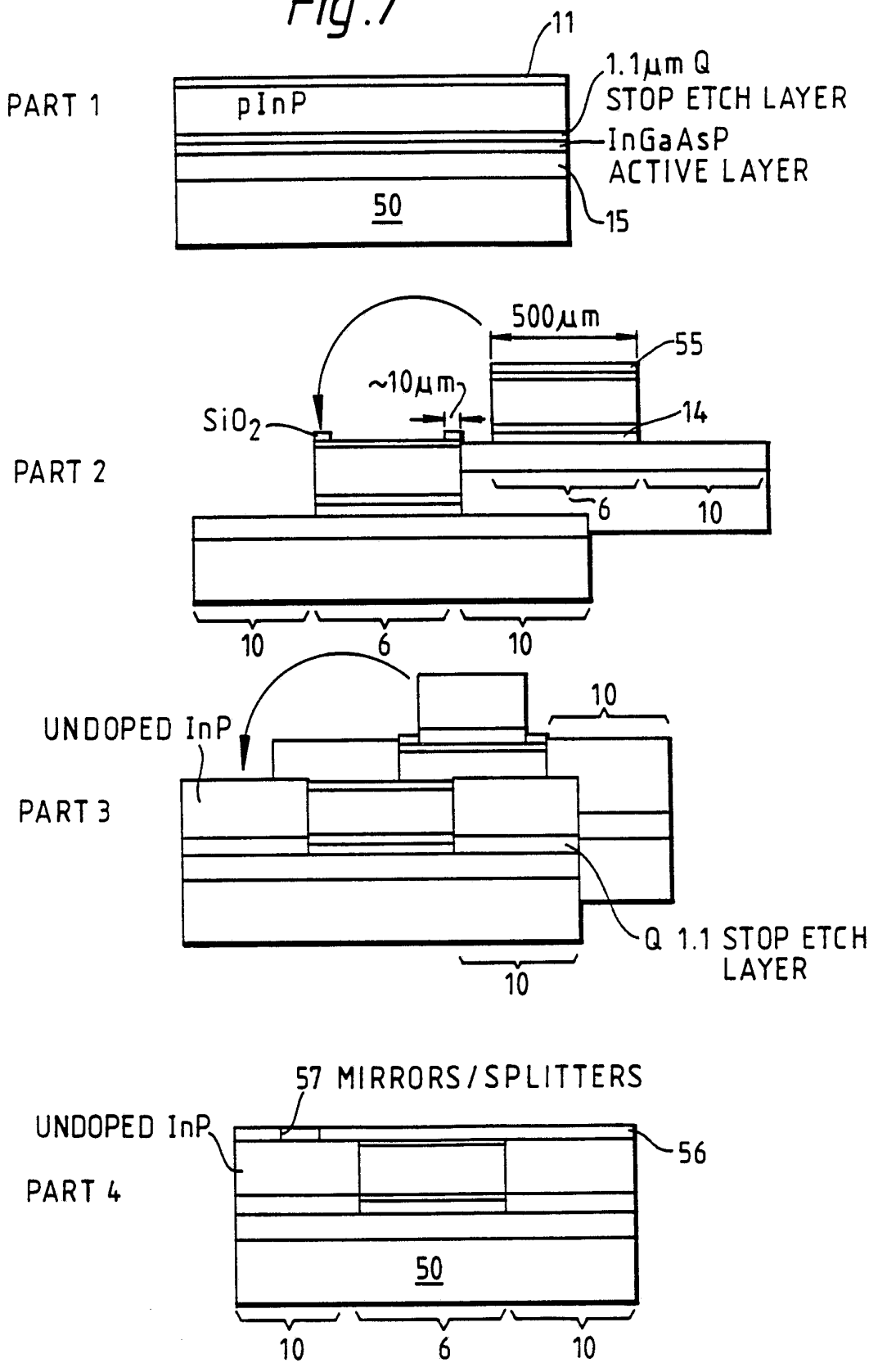

PART 1
pInP
11
1.1μm Q
STOP ETCH LAYER
InGaAsP
ACTIVE LAYER
15
50
PART 2
500μm
55
~10μm
SiO2
14
6
10
10
6
10
PART 3
UNDOPED InP
10
Q 1.1 STOP ETCH
LAYER
10
PART 4
57 MIRRORS/SPLITTERS
UNDOPED InP
56
50
10
6
10

Fig. 7 (CONTD.)

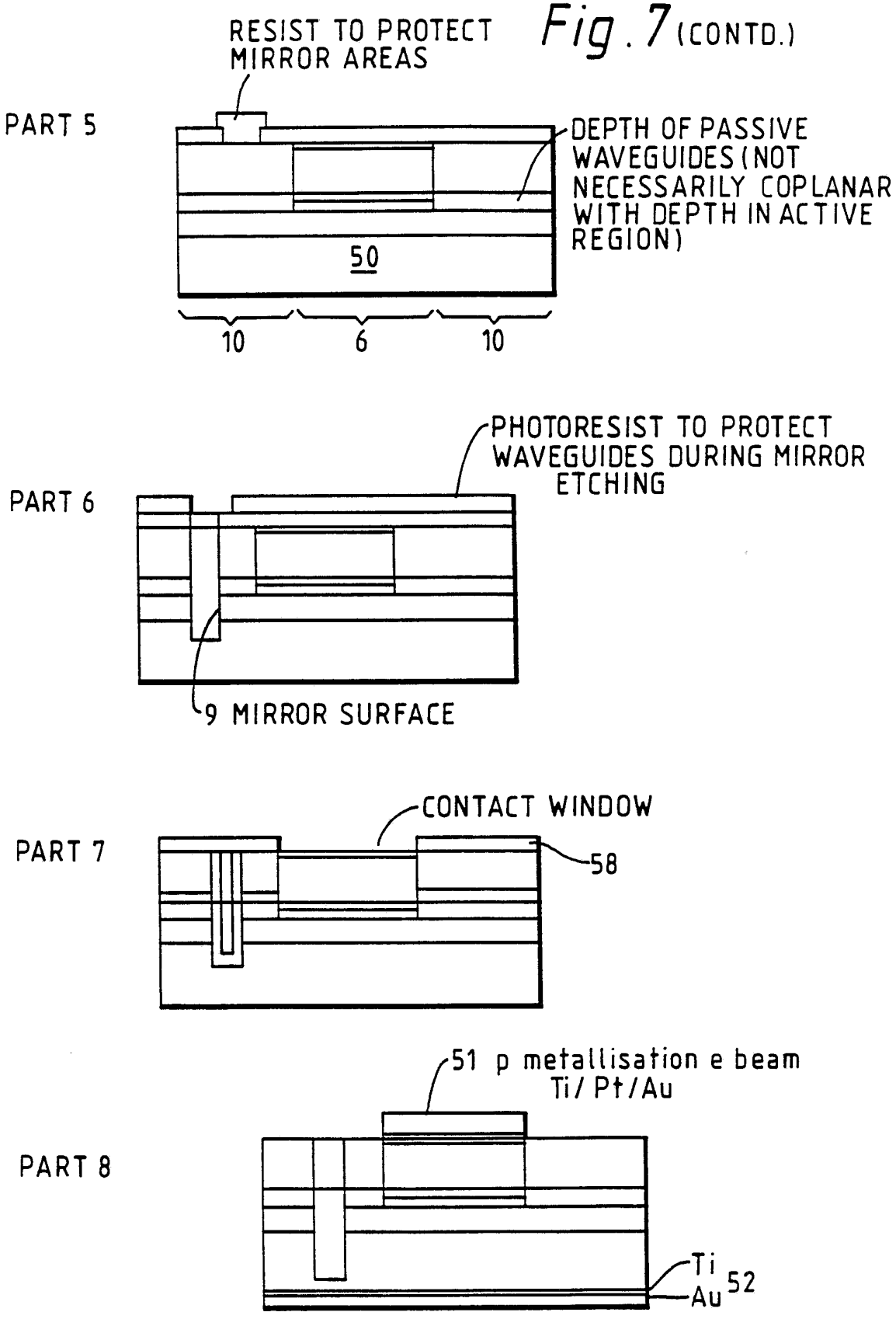

RESIST TO PROTECT MIRROR AREAS
PART 5
DEPTH OF PASSIVE WAVEGUIDES (NOT NECESSARILY COPLANAR WITH DEPTH IN ACTIVE REGION)
50
10
6
10
PHOTORESIST TO PROTECT WAVEGUIDES DURING MIRROR ETCHING
PART 6
9 MIRROR SURFACE
CONTACT WINDOW
PART 7
58
51 p metallisation e beam Ti/ Pt/Au
PART 8
Ti
Au
52

Fig.8

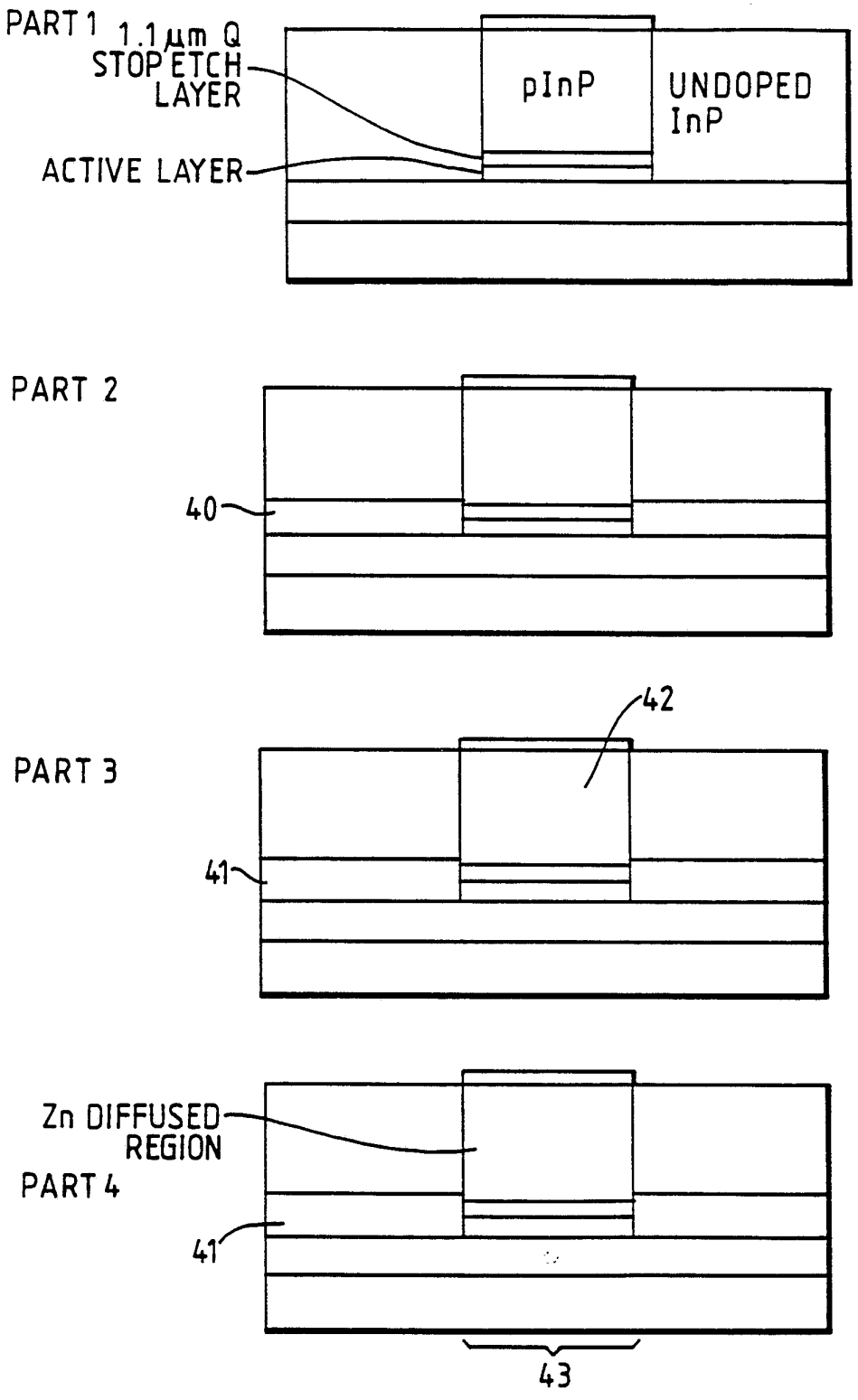
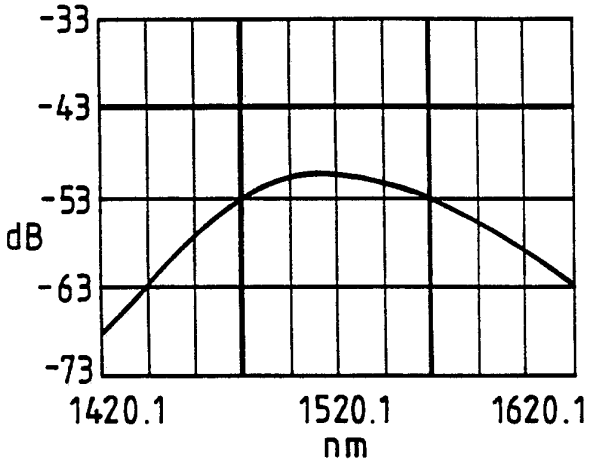

PART 1
1.1μm Q STOP ETCH LAYER
ACTIVE LAYER
pInP
UNDOPED InP
PART 2
40
PART 3
42
41
Zn DIFFUSED REGION
PART 4
41
43

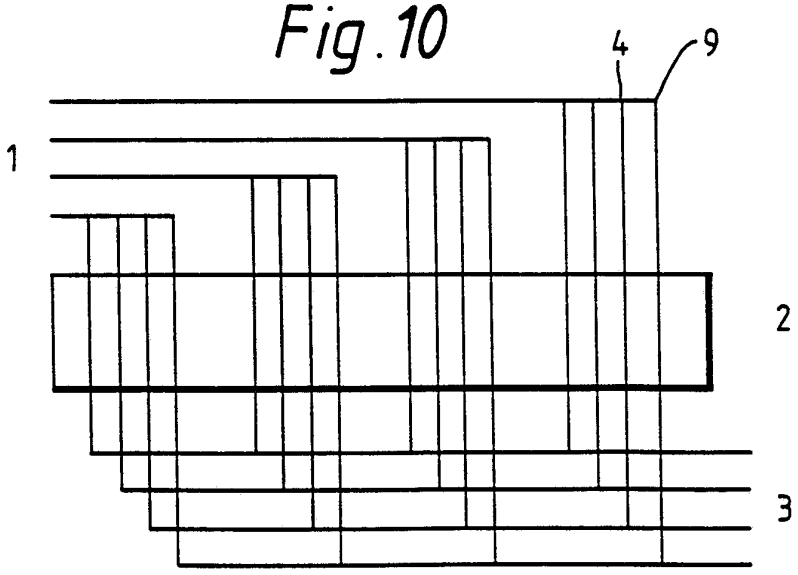
Fig. 9

VERY LOW RIPPLE
80nm BANDWIDTH AT MAXIMUM GAIN
CURRENT



SWP 20nm/	YS 5dB/RES.1nm	AVR 1
WMKR	1559.06 - 1480.10 = 78.96	
LMKR		

Fig. 10



INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 93/00923

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 G02F1/313; H04Q3/52

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	G02F ; H04Q

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
X	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 20, no. 12, May 1978, NEW YORK US pages 5383 - 5384 R.Y. HUNG ET AL. 'Active star connector for optical fibers' see the whole document ---	1-2,5
A	TOPICAL MEETING ON PHOTONIC SWITCHING 1987 SUMMARIES OF PAPERS, PAPER THD1-1 pages 62 - 64 , XP000092377 A. AJISAWA ET AL. 'A Monolithically Integrated Optical Gate 2x2 Matrix Switch Using GaAs/AlGaAs Multiple Quantum Well Structures' see the whole document --- -/--	1-2,5

° Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
27 JULY 1993	-6 AOUT 1993
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	IASEVOLI R.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
P,A	WO,A,9 211 551 (UK SECRETARY FOR DEFENCE) 9 July 1992 see page 22, line 1 - page 24, line 13 see figures 8-9	2-3
A	EP,A,0 380 983 (HITACHI) 8 August 1990 * abstract; column 7, line 23 - line 53 * see claims 17,20-21; figures 1,7-9	1,5-6
A	ELECTRONICS LETTERS. vol. 28, no. 8, April 1992, STEVENAGE GB pages 776 - 778 M. JANSON ET AL. 'Monolithically integrated 2x2 InGaAsP/InP laser amplifier gate switch arrays' see the whole document	1,5-6
A	PATENT ABSTRACTS OF JAPAN vol. 10, no. 266 (P-496)11 September 1986 & JP,A,61 091 623 (NTT) 9 May 1986 see abstract	1,5

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

GB 9300923
SA 73486

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 27/07/93

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
WO-A-9211551	09-07-92	None		
EP-A-0380983	08-08-90	JP-A-	2199430	07-08-90
		CA-A-	2007747	30-07-90
		US-A-	5044745	03-09-91
		US-A-	5146513	08-09-92