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(54) **Title:** TECHNIQUE FOR PROMOTING EFFICIENT INSTRUCTION FUSION

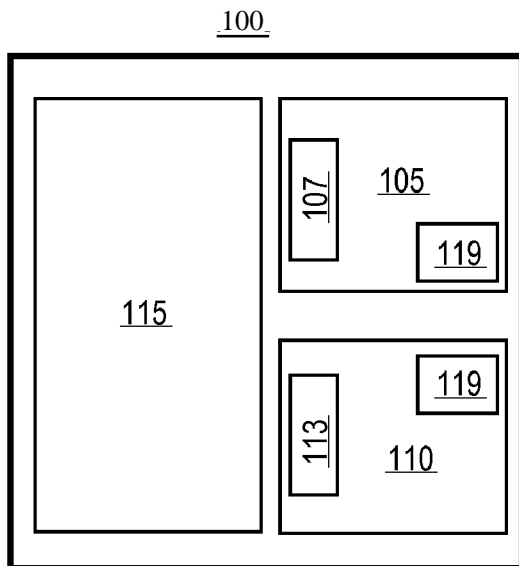


FIG. 1

(57) **Abstract:** A technique to enable efficient instruction fusion within a computer system. In one embodiment, a processor logic delays the processing of a second instruction for a threshold amount of time if a first instruction within an instruction queue is fusible with the second instruction.



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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models applications for Utility Models since 1975, IPC as above

Japanese Utility Models and application for Utility Models since 1975, IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS, IEEExpl, Google, instruction fusion, delay, instruction queue,

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
A	US 2004-0128485 AI (SCOTT R. NELSON) 1 Jul . 2004 See the abstract , claims 1-18 and figures 1-5 .	1-20
A	US 6,889,318 BI (SHANNON A. WICHMAN) 3 May. 2005 See the abstract , claims 1-41 and figures 1-4.	1-20
A	US 2004-139429 AI (RONNY RONEN et al.) 15 Jul . 2004 See the abstract , claims 1-29 and figures 1-5 .	1-20

 Further documents are listed in the continuation of Box C See patent family annex

* Special categories of cited documents

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 06889318 B 1	03.05.2005	None	
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