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(54) **Title:** A VOLTAGE REGULATOR AND A METHOD FOR OPERATING A VOLTAGE REGULATOR

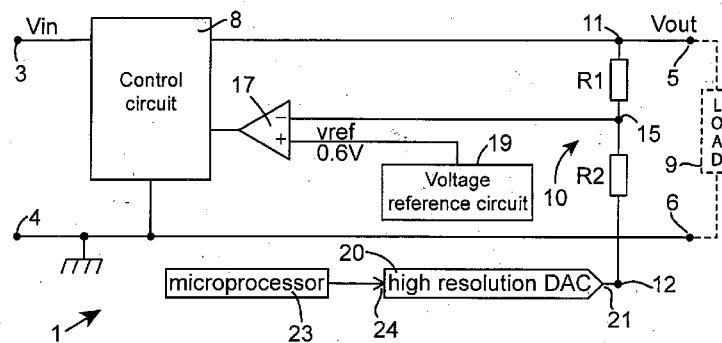


Fig. 1

(57) **Abstract:** A switched mode voltage regulator (1) comprises a resistor-divider circuit (10) comprising first and second resistors (R1,R2) series connected between first and second taps (11,12) for maintaining a regulated output voltage across output terminals (5,6) at a selectable regulated voltage value. The first tap (11) is connected to the positive output terminal (5). The resistors (R1,R2) define an intermediate tap (15), the voltage of which is maintained at the value of a voltage reference, which is produced by a voltage reference circuit (19), by an error amplifier (12) which forms with a control circuit (8) a feedback loop to force the voltage produced across the output terminals (5,6) to the regulated voltage value. A DAC (20) operated under the control of a microprocessor (23) selectively varies the voltage applied to the second tap (12) of the resistor-divider circuit (10) for in turn varying the voltage on the first tap (11) for varying the value of the regulated voltage produced across the output terminals (5,6). The microprocessor (23) may also be programmed to calibrate the voltage regulator (1).



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"A voltage regulator and a method for operating a voltage regulator"

The present invention relates to a voltage regulator and in particular to a voltage regulator for producing a selectively variable regulated DC voltage supply from an input voltage supply. The invention also relates to a method for operating a voltage regulator, and in particular to a method for operating a voltage regulator for producing a selectively variable regulated DC voltage supply from an input voltage supply.

10 Voltage regulators for producing a regulated DC voltage supply from an input voltage supply are known. In general, the input voltage supply is a DC voltage, and may be an unregulated DC voltage supply, or a regulated DC voltage supply. Additionally, the input voltage may be an AC voltage supply, which would be rectified to a DC voltage supply. One type of such voltage regulators is referred to as a switched mode voltage regulator, and another type of such voltage regulators is referred to as a linear mode voltage regulator. A switched mode voltage regulator is disclosed in U.S. Patent Specification No. 5,481,178 of Wilcox, et al, assigned to Linear Technology Corporation.

20 Such switched mode voltage regulators comprise an impedance-divider circuit, which in general is a resistor-divider circuit coupled across a pair of output terminals across which the regulated DC voltage is produced. The resistor-divider circuit comprises first and second resistors connected in series between first and second taps of the resistor-divider circuit. An intermediate tap is defined between the first and second resistors. The first tap is connected to a first one of the output terminals, and the second tap is connected to a second one of the output terminals. Typically, the second output terminal to which the second tap is connected is connected to a common voltage with one of a pair of input terminals to which the input voltage supply is applied. The common voltage typically is ground voltage.

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The intermediate tap of the resistor-divider circuit is coupled to one of the inverting and non-inverting inputs of an error amplifier, and the other of the inverting and non-inverting inputs of the error amplifier is connected to a voltage reference. The error

amplifier forms a feedback loop with suitable control circuitry in the voltage regulator, so that the error amplifier operates to force the voltage on the first output terminal to the regulated voltage value, in order to maintain the voltage on the intermediate tap substantially at the value of the voltage reference. In a switched mode voltage
5 regulator of the type configured to produce a DC regulated voltage of, for example, 5 volts from an unregulated DC voltage which can vary between 10 volts and 20 volts, the intermediate tap of the resistor-divider circuit typically is held at a voltage of approximately 0.6 volts.

10 The value of the regulated voltage produced across the output terminals is determined by the voltage value of the voltage reference, and the ratio of the resistance values of the first and second resistors of the resistor-divider circuit. In a typical switched mode voltage regulator, which is required to produce a regulated DC voltage of up to 5 volts, the voltage reference is of voltage value of 0.6 volts and
15 the first resistor, which is located between the intermediate tap and the first tap, typically is of resistance value of the order of 60.4 Kohms. The resistance value of the second resistor which is located between the intermediate tap and the second tap is selected to produce the regulated voltage of the desired voltage value. If a regulated voltage of a different voltage value is required, it is necessary to replace
20 the second resistor of one resistance value with a resistor of another resistance value. This is inconvenient and cumbersome. Additionally, by virtue of the fact that the regulated voltage is varied by replacing one resistor with another resistor of a different resistance value, the regulated voltage can only be varied in relatively large steps. This is undesirable.

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Typical linear mode voltage regulators are disclosed in U.S. Patent Specification No. 6,377,033 of Hsu, assigned to ASUSTeK Computer Inc. Such linear mode voltage regulators comprise an impedance-divider circuit which is provided by a resistor-
divider circuit connected across the first and second output terminals in a similar
30 manner as the resistor-divider circuit is connected across the first and second output terminals of a switched mode voltage regulator. Current from the input voltage supply is conducted to the first output terminal through a pass element of variable resistance. One of the inverting and non-inverting inputs of an error amplifier is

connected to the intermediate tap defined between the first and second resistors of the resistor-divider circuit, and the other of the inverting and non-inverting inputs of the error amplifier is connected to a voltage reference. The error amplifier forms a feedback loop with the pass element, so that the error amplifier operates to force the
5 voltage on the first output terminal to the regulated voltage value, in order to maintain the voltage on the intermediate tap substantially at the value of the voltage reference.

The regulated voltage produced across the output terminals of a linear mode voltage
10 regulator is a function of the value of the voltage reference, and the ratio of the resistance values of the first and second resistors of the resistor-divider circuit in much the same way as the regulated voltage produced on the output terminals of the switched mode voltage regulator is a function of the value of the voltage reference and the ratio of the resistance values of the first and second resistors of the resistor-
15 divider circuit of the switched mode voltage regulator. Accordingly, in order to vary the value of the regulated voltage produced across the output terminals of a linear voltage regulator, it is necessary to remove and replace the second resistor of one resistance value with a resistor of another resistance value. This is inconvenient and cumbersome, and also as described with reference to a switched mode voltage
20 regulator, only allows the regulated voltage to be varied in relatively large steps.

There is therefore a need for a voltage regulator for producing a regulated DC voltage supply from an input voltage supply, which may be a switched mode voltage regulator or a linear mode voltage regulator, which overcomes the problems of
25 known voltage regulators and which allows the regulated voltage to be selectively varied.

The present invention is directed towards providing such a voltage regulator, and the invention is also directed towards a method for operating a voltage regulator in order
30 to produce a selectively variable regulated DC voltage supply from an input voltage supply.

According to the invention there is provided a voltage regulator for producing a

selectively variable regulated DC voltage supply from an input voltage supply, the voltage regulator comprising first and second output terminals across which the regulated voltage is produced, an impedance-divider circuit comprising a pair of series connected impedance elements between a first tap and a second tap, the series connected impedance elements defining an intermediate tap therebetween, the first tap of the impedance-divider circuit being connected to the first output terminal through a current path, a control circuit co-operable with the impedance-divider circuit and being adapted to force the voltage on the first output terminal to the regulated voltage value in order to maintain the voltage on the intermediate tap of the impedance-divider circuit at a predefined fixed value, and a means for selectively varying the voltage on the second tap of the impedance-divider circuit relative to the voltage on the second output terminal for varying the value of the regulated voltage produced across the first and second output terminals.

In one embodiment of the invention the means for varying the voltage on the second tap of the impedance-divider circuit is adapted to vary the voltage on the second tap between a first voltage value and a second voltage value, the first and second voltage values lying in respective ranges of voltage values between the voltage on the second output terminal and the voltage on the intermediate tap of the impedance-divider circuit. Preferably, the first voltage value is substantially equal to the voltage on the second output terminal. Advantageously, the second voltage value is substantially equal to the voltage on the intermediate tap of the impedance-divider circuit.

In another embodiment of the invention the means for varying the voltage on the second tap of the impedance-divider circuit comprises a variable voltage producing means. Preferably, the variable voltage producing means comprises a high resolution variable voltage producing means.

In another embodiment of the invention the variable voltage producing means comprises a digital-to-analogue converter. Preferably, the digital-to-analogue converter is configured to have a resolution of at least 8 bits. Advantageously, the digital-to-analogue converter is configured to have a resolution in the order of 12

bits.

Preferably, the analogue output voltage produced by the digital-to-analogue converter is applied to the second tap of the impedance-divider circuit.

5 Advantageously, an analogue output of the digital-to-analogue converter is connected to the second tap through a current path.

In an alternative embodiment of the invention the variable voltage producing means comprises a digital potentiometer.

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In one embodiment of the invention a programmable element is provided for controlling the variable voltage producing means to provide selectable voltage values for applying to the second tap of the impedance-divider circuit. Preferably, the programmable element comprises a microprocessor, and the microprocessor is
15 programmed to receive inputs indicative of respective selectable regulated voltage values.

In another embodiment of the invention the microprocessor is responsive to an input indicative of a selectable regulated voltage value inputted thereto to operate the
20 variable voltage producing means to apply a voltage to the second tap of the impedance-divider circuit of a value to produce the selected regulated voltage across the first and second output terminals.

In a further embodiment of the invention a calibration circuit is provided for
25 calibrating the voltage regulator. Preferably, the calibration circuit comprises a means for reading a voltage indicative of the regulated voltage produced across the first and second output terminals, and a means for comparing the read voltage indicative of the regulated voltage produced across the first and second output terminals with an ideal voltage value. Advantageously, a means is provided for
30 deriving a calibration value from the comparison of the read voltage indicative of regulated voltage produced across the first and second output terminals and the ideal voltage value.

In one embodiment of the invention the microprocessor is programmed to read the voltage indicative of the regulated voltage produced across the first and second output terminals and to compare the read voltage indicative of the regulated voltage produced across the first and second output terminals with the ideal voltage.

- 5 Preferably, the microprocessor is programmed to compute the calibration value. Advantageously, the microprocessor is programmed to operate the variable voltage producing means to apply a predefined voltage to the second tap of the impedance-divider circuit to produce a regulated voltage across the first and second output terminals, and to read the voltage indicative of regulated voltage produced across
- 10 the first and second output terminals in response to the predefined voltage applied to the second tap for comparison with the ideal voltage value.

- Ideally, the microprocessor is programmed to operate the variable voltage producing means to apply at least two predefined voltages of different voltage values to the
- 15 second tap of the impedance-divider circuit and to read voltage values indicative of the respective regulated voltages produced across the first and second output terminals in response to the two predefined voltage values applied to the second tap, and to compute respective calibration values from a comparison of the two read voltage values indicative of the regulated voltage produced across the first and
- 20 second output terminals with corresponding respective ideal values.

In one embodiment of the invention each calibration value is stored in a non-volatile memory readable by the microprocessor.

- 25 In another embodiment of the invention each ideal value of the regulated voltage is stored in the microprocessor.

- In a further embodiment of the invention the microprocessor is programmed to operate the variable voltage producing means to apply the voltages to the second
- 30 tap of the impedance-divider circuit corrected with the calibration value to produce the respective regulated voltages across the first and second output terminals of the selected voltage values.

In one embodiment of the invention one of a inverting input and a non-inverting input of an error amplifier is connected through a current path to the intermediate tap of the impedance-divider circuit, and the other of the inverting and the non-inverting inputs of the error amplifier is connected through a current path to a voltage
5 reference, the error amplifier forming with the control circuit a feedback loop to force the voltage on the first output terminal to the regulated voltage value in order to maintain the voltage on the intermediate tap of the impedance-divider circuit at the predefined fixed voltage. Preferably, the predefined fixed voltage is of value substantially equal to the value of the voltage reference.

10

In another embodiment of the invention a pair of input terminals are provided for receiving the input voltage supply.

In a further embodiment of the invention the second output terminal and one of the
15 input terminals are held at a common voltage.

In one aspect of the invention the common voltage is ground voltage.

In another aspect of the invention each impedance element of the impedance-divider
20 circuit comprises an impedance element of substantially fixed impedance value.

In another embodiment of the invention the impedance-divider circuit comprises a resistor-divider circuit.

25 In one aspect of the invention the resistance value of the resistor-divider circuit between the second tap and the intermediate tap is in the range of 8.25 Kohms to 60.4 Kohms when the resistance value of the resistor-divider circuit between the first tap and the intermediate tap is in the order of 60.4 Kohms.

30 In another aspect of the invention the resistor-divider circuit comprises a first resistor connected between the first tap and the intermediate tap, and a second resistor connected between the second tap and the intermediate tap.

In one embodiment of the invention the voltage regulator is adapted for producing selectable regulated DC voltages across the first and second output terminals of values in the range of zero volts to the maximum regulated voltage value of which the voltage regulator is configured to produce.

5

In another embodiment of the invention the voltage regulator is adapted for producing selectable regulated DC voltages across the first and second output terminals of values up to 60 volts.

10 In another embodiment of the invention the voltage regulator is adapted for producing selectable regulated DC voltages across the first and second output terminals of values up to 12 volts.

In a further embodiment of the invention the voltage regulator is adapted for
15 producing selectable regulated DC voltages across the output terminals of values in the range of zero volts to 60 volts.

In one aspect of the invention the voltage regulator is adapted for receiving an unregulated DC voltage supply.

20

In one embodiment of the invention the voltage regulator is configured as a switched mode voltage regulator. In an alternative embodiment of the invention the voltage regulator is configured as a linear mode voltage regulator.

25 In one aspect of the invention the voltage regulator is adapted to be produced as an integrated circuit.

In another aspect of the invention the voltage regulator is adapted to be produced as a module.

30

In a further aspect of the invention the voltage regulator is adapted to be produced from discrete parts.

The invention also provides a method for operating a voltage regulator for producing a selectively variable regulated DC voltage supply from an input voltage supply, the voltage regulator being of the type comprising first and second output terminals across which the regulated voltage is produced, an impedance-divider circuit
5 comprising a pair of series connected impedance elements between a first tap and a second tap, the first and second impedance elements defining an intermediate tap therebetween, the first tap of the impedance-divider circuit being connected to the first output terminal through a current path, and a control circuit co-operable with the impedance-divider circuit and being adapted to force the voltage on the first output
10 terminal to the regulated voltage value in order to maintain the voltage on the intermediate tap of the impedance-divider circuit at a predefined fixed value, the method comprising selectively varying the voltage on the second tap of the impedance-divider circuit relative to the voltage on the second output terminal for varying the value of the regulated voltage produced across the first and second
15 output terminals.

In one aspect of the invention the voltage on the second output tap is varied between a first voltage value and a second voltage value, the first and second voltage values lying in respective ranges of voltage values between the voltage on
20 the second output terminal and the voltage on the intermediate tap of the impedance-divider circuit. Preferably, the first voltage value is substantially equal to the voltage on the second output terminal. Advantageously, the second voltage value is substantially equal to the voltage on the intermediate tap of the impedance-divider circuit.

25

In one embodiment of the invention the voltage on the second tap of the impedance-divider circuit is varied by applying a voltage thereto from a variable voltage producing means.

30 In one aspect of the invention the variable voltage producing means is controlled by a programmable element for producing the variable voltage. Preferably, the programmable element comprises a microprocessor.

In another embodiment of the invention the method further comprises calibrating the voltage regulator.

In one aspect of the invention the voltage regulator is calibrated by comparing a
5 voltage indicative of the regulated voltage produced across the first and second
output terminals with an ideal voltage value and deriving a calibration value from the
comparison. Preferably, a predefined voltage is applied to the second tap of the
impedance-divider circuit, and a voltage indicative of a regulated voltage produced
10 across the first and second output terminals in response to the predefined voltage is
compared with an ideal voltage for producing the calibration value.

In another aspect of the invention each voltage applied to the second tap of the
impedance-divider circuit to produce a selected regulated voltage across the first
and second output terminals is corrected with the calibration value.

15

In another embodiment of the invention respective voltages of different predefined
voltage values are applied to the second tap of the impedance-divider circuit, and
voltages indicative of the corresponding regulated voltages produced across the first
and second output terminals are compared with corresponding ideal voltage values
20 for producing respective calibration values.

In one aspect of the invention the method is adapted for operating a switched mode
voltage regulator for producing the selectively variable DC voltage supply. In an
alternative aspect of the invention the method is adapted for operating a linear mode
25 voltage regulator for producing the selectively variable DC voltage supply.

The advantages of the invention are many. The voltage value of the regulated
output voltage produced across the output terminals of the voltage regulators
according to the invention can be varied without the need for removing and replacing
30 resistors of a resistor-divider circuit or impedance elements of an impedance-divider
circuit. Additionally, the voltage value of the regulated output voltage produced
across the output terminal can be varied between upper and lower limits of a voltage
range, and the voltage range may be as wide as the maximum value at which the

regulated voltage supply can be produced by the voltage regulator and the value of the voltage reference which is applied to the intermediate tap of the impedance-divider circuit. A further advantage of the invention is that the regulated DC output voltage is variable in relatively small increments and decrements within the voltage range. The size of the voltage increments and decrements in which the regulated DC voltage output can be varied is a function of the resolution of the variable voltage producing means. By providing the variable voltage producing means as a high resolution variable voltage producing means, the size of the voltage increments and decrements of the regulated output voltage is relatively small. The provision of a high resolution digital-to-analogue converter for applying the variable voltage on the second tap of the impedance-divider circuit permits the regulated output voltage produced across the output terminals to be varied with a relatively high resolution.

The invention will be more clearly understood from the following description of some preferred embodiments thereof, which are given by way of example only, with reference to the accompanying drawings, in which:

Fig. 1 is a block representation of a voltage regulator according to the invention,

Fig. 2 is a block representation of a voltage regulator according to another embodiment of the invention,

Fig. 3 is a block representation of a voltage regulator according to a further embodiment of the invention, and

Fig. 4 is a block representation of a voltage regulator according to a still further embodiment of the invention.

Referring to the drawings, and initially to Fig. 1, there is illustrated a voltage regulator according to the invention, indicated generally by the reference numeral 1, for producing a regulated DC output voltage supply V_{out} from a DC input voltage supply V_{in} , which may be a regulated or an unregulated DC voltage supply. In this

embodiment of the invention the voltage regulator 1 is a switched mode voltage regulator. The voltage regulator 1 comprises first and second input terminals, namely, a positive input terminal 3 and a ground terminal 4 to which the DC input voltage supply V_{in} is applied. The regulated DC output voltage V_{out} is produced
5 across first and second output terminals, namely, a positive first output terminal 5 and a ground second terminal 6. The input and output ground terminals 4 and 6 are held at a common voltage, which in this embodiment of the invention is ground voltage.

10 A control circuit 8, which will be well known to those skilled in the art of switched mode voltage regulators, controls the voltage regulator 1 to produce the regulated DC voltage supply across the output terminals 5 and 6, which is applied to a load 9 coupled across the first and second output terminals 5 and 6. An impedance-divider circuit, which in this embodiment of the invention is provided by a resistor-divider
15 circuit 10 controls the regulated output voltage across the output terminals 5 and 6 at a selected regulated voltage value. The resistor-divider circuit 10 comprises first and second resistors R1 and R2 which are connected in series between a first tap 11 and a second tap 12. The first and second resistors R1 and R2 are of fixed
20 resistance value. The term "fixed resistance value" when used in connection with the first and second resistors R1 and R2 is intended to mean resistors which are of fixed resistance values to the extent that any change in the resistance values would only occur in the event of a change in temperature of the resistors.

The first tap 11 of the resistor-divider circuit 10 is connected to the first output
25 terminal 5. The first and second resistors R1 and R2 define an intermediate tap 15, which is connected to one of an inverting and non-inverting input of an error amplifier 17. In this embodiment of the invention the intermediate tap 15 is connected to the inverting input of the error amplifier 17. The non-inverting input of the error amplifier 17 is connected to a voltage reference V_{ref} produced by a voltage reference circuit
30 19. The error amplifier 17 forms a feedback loop with the control circuit 8, so that the error amplifier 17 operates to force the voltage on the first output terminal 5 to the desired regulated voltage value, in order to maintain the voltage on the intermediate tap 15 to a fixed voltage value, which in this case is the value of the

voltage reference produced by the voltage reference circuit 19, and the voltage on the intermediate tap 15 is maintained by the error amplifier 17 substantially at the voltage value of the voltage reference.

- 5 A means for selectively varying the voltage on the second tap 12 of the resistor-divider circuit 10 relative to the voltage on the second output terminal 6 for in turn varying the value of the regulated output voltage produced across the first and second output terminals 5 and 6 comprises a variable voltage producing means, namely, a digital-to-analogue converter (DAC) 20. In this embodiment of the
- 10 invention the DAC 20 is a high resolution DAC and comprises a 12-bit DAC. The analogue output 21 of the DAC 20 is connected to the second tap 12 of the resistor-divider circuit 10 for applying selectable analogue voltages thereto. A programmable element for controlling the DAC 20 to apply the selectable output voltages to the second tap 12 in this embodiment of the invention comprises a microprocessor 23.
- 15 The microprocessor 23 is programmed to permit selection of desired regulated output voltages to be produced across the first and second output terminals 5 and 6. An appropriate digital word is written by the microprocessor 23 to the digital input 24 of the DAC 20 to produce a corresponding appropriate analogue output voltage on the analogue output 21 of the DAC 20 for applying to the second tap 12 in order to
- 20 produce the regulated voltage across the output terminals 5 and 6 at the desired regulated voltage value. The resolution with which the regulated voltage produced across the first and second output terminals 5 and 6 may be selectively varied is dependent on the resolution of the DAC 20.
- 25 The value of the voltage reference and the ratio of the resistance values of the first and second resistors R1 and R2 are selected so that when the voltage applied to the second tap 12 of the resistor-divider circuit 10 by the DAC 20 is ground voltage, the value of the regulated voltage produced across the first and second output terminals 5 and 6 is the maximum regulated voltage value to be produced across the output
- 30 terminals for the selected resistor ratio. By increasing the value of the voltage applied by the DAC 20 to the second tap 12 from a first voltage value, which in this case is ground voltage, upwardly to a second voltage value, which in this case is equal to the value of the voltage reference produced by the voltage reference circuit

19, the value of the regulated voltage produced across the first and second output terminals 5 and 6 decreases from the maximum regulated output voltage value produced by the voltage regulator 1 to the value of the voltage reference, which is the minimum selectable regulated output voltage produced by the voltage regulator

5 1.

The operation of the voltage regulator 1 to produce selectable regulated voltage values across the first and second output terminals 5 and 6 within a voltage range from the minimum regulated voltage value equal to the value of the voltage

10 reference V_{ref} to the maximum regulated voltage value can be explained as follows. The regulated output voltage produced across the first and second output terminals 5 and 6 is a function of the ratio of the resistance values of the first and second resistors $R1$ and $R2$, and is also a function of the voltage on the intermediate tap 15 which is forced to the value of the voltage reference V_{ref} produced by the voltage

15 reference circuit 19. Accordingly, the regulated output voltage produced across the first and second output terminals 5 and 6 is given by the following equation (1):

$$V_{out} = V_{ref} + \frac{R1}{R2} (V_{ref} - V_{dac}) \quad (1),$$

where

20 V_{out} is the regulated output voltage produced across the first and second output terminals 5 and 6,

V_{ref} is the value of the voltage reference produced by the voltage reference circuit 19,

25 V_{dac} is the voltage applied to the second tap 12 by the DAC 20 relative to the voltage on the second output terminal 6,

$R1$ is the resistance value of the first resistor $R1$, and

$R2$ is the resistance value of the second resistor $R2$.

When the voltage V_{dac} on the second tap 12 is equal to the first voltage value,

30 namely, ground voltage, in other words, when the voltage on the second tap 12 is equal to the voltage on the second output terminal 6, equation (1) becomes:

$$V_{out} = V_{ref} + \frac{R1}{R2} V_{ref} \quad (2)$$

Thus, when the voltage applied to the second tap 12 by the DAC 20 is ground voltage, the regulated output voltage produced across the first and second output terminals 5 and 6 is at its maximum value.

When the voltage V_{dac} which is applied by the DAC 20 to the second terminal 12 has been increased to the second voltage value, namely, the value of the voltage reference V_{ref} produced by the voltage reference circuit 19, equation (1) becomes:

10

$$V_{out} = V_{ref} \quad (3),$$

which is thus the minimum voltage value of the regulated output voltage which can be produced across the first and second output terminals 5 and 6.

15 Accordingly, by increasing the voltage applied to the second tap 12 by the DAC 20 incrementally from the first voltage value, namely, ground voltage to the second voltage value, namely, the value of the voltage reference V_{ref} , the value of the regulated output voltage produced across the first and second output terminals 5 and 6 is decrementally varied from the maximum value of the regulated output
20 voltage to the minimum value thereof, which is the value of the voltage reference produced by the voltage reference circuit 19. The resolution with which the value of the regulated output voltage produced across the first and second output terminals 5 and 6 can be varied depends on the resolution of the DAC 20.

25 In this embodiment of the invention the maximum value of the regulated output voltage to be produced across the first and second output terminals 5 and 6 is 5 volts and the value of the voltage reference produced by the voltage reference circuit 19 is 0.6 volts. The resistance value of the first resistor $R1$ is 60.4 Kohms, and the resistance value of the second resistor $R2$ is 8.25 Kohms. This, thus, allows the
30 value of the regulated output voltage to be varied between 0.6 volts and 5 volts.

When the resistance values of the first and second resistors $R1$ and $R2$ are equal to

each other, for example, of resistance value of 60.4 Kohms each, the maximum value of the regulated output voltage produced across the first and second output terminals 5 and 6 is twice the value of the voltage reference V_{ref} produced by the voltage reference circuit 19, and is thus 1.2 volts. Accordingly, with the first and second resistors of equal value, the value of the regulated output voltage produced across the first and second output terminals 5 and 6 can be varied between the values of 0.6 volts and 1.2 volts. A resistance value of the second resistor R2 of 30.1 Kohms with the first resistor of 60.4 Kohms and the voltage reference at 0.6 volts produces a maximum regulated output voltage across the first and second output terminals 5 and 6 of 1.8 volts. Accordingly, in this case the value of the regulated voltage produced across the first and second output terminals 5 and 6 can be varied from 0.6 volts to 1.8 volts. A resistance value of the second resistor R2 of 13.3 Kohms with the first resistor being of resistance value of 60.4 Kohms and the voltage reference being at 0.6 volts produces a maximum regulated output voltage across the first and second output terminals 5 and 6 of 3.3 volts, and thus, in this case the value of the regulated voltage produced across the first and second output terminals 5 and 6 can be varied between 0.6 volts and 3.3 volts.

In use, with the microprocessor 23 appropriately programmed, the desired value at which the regulated voltage across the first and second output terminals 5 and 6 is to be produced between the maximum voltage value and the minimum voltage value is appropriately inputted to the microprocessor 23. The microprocessor 23 writes an appropriate digital word to the DAC 20 in order that the analogue voltage applied by the DAC 20 to the second tap 12 is of the appropriate value to produce the regulated output voltage across the first and second output terminals 5 and 6 at the selected desired regulated value. The voltage regulator 1 operates to produce the DC regulated output voltage supply to the load 9 across the first and second output terminals 5 and 6 at the selected desired regulated voltage value. To alter the voltage value at which the regulated voltage supply is produced across the output terminals 5 and 6, the new desired voltage value is inputted to the microprocessor 23, which writes an appropriate digital word to the DAC 20, which in turn applies the appropriate analogue voltage to the second tap 12 in order to produce the regulated voltage supply across the first and second output terminals 5 and 6 at the new

regulated voltage value.

Referring now to Fig. 2, there is illustrated a voltage regulator according to the invention, indicated generally by the reference numeral 30, for producing a regulated DC voltage supply from an input voltage supply, which in this case is also an unregulated DC voltage supply. The voltage regulator 30 is a switched mode voltage regulator and is substantially similar to the switched mode voltage regulator 1 described with reference to Fig. 1, and similar components are identified by the same reference numerals. The main difference between the voltage regulator 30 and the voltage regulator 1 is that the voltage regulator 30 comprises a calibration circuit 31 for carrying out self-calibration of the voltage regulator 30. The calibration circuit 31 comprises a high resolution analogue-to-digital converter 33, an analogue input 34 of which is connected to the first output terminal 5. The analogue-to-digital converter 33 converts the regulated output voltage to a corresponding digital word which is produced on an output 35 of the analogue-to-digital converter 33, and which is indicative of the voltage value of the regulated output voltage produced across the first and second output terminals 5 and 6.

In this embodiment of the invention the microprocessor 23 is also programmed to operate in a calibration mode. In the calibration mode the microprocessor 23 operates the DAC 20 to sequentially apply a series of predefined voltages of respective different voltage values to the second tap 12 of the resistor-divider circuit 10, and to read the corresponding digital words from the digital output 35 of the analogue-to-digital converter 33. The microprocessor 33 compares the values of the digital words read from the digital output 35 of the analogue-to-digital converter 33 with respective corresponding ideal values. Calibration values are then computed by the microprocessor 23 from the differences, if such exist, between the digital words read from the digital output 35 of the analogue-to-digital converter 33 and the corresponding ideal values. The calibration values may be stored as individual calibration values, or the microprocessor 23 may be programmed to prepare a calibration function from the calibration values. The calibration function may be in the form of a suitable calibration equation or a suitable calibration formula. The calibration function may be a linear function or a non-linear function, depending on

the calibration values. A non-volatile memory 37 is provided for storing the computed calibration values and/or the calibration function, and the microprocessor 23 writes the calibration values and/or the calibration function to the non-volatile memory 37. Digital words for producing the predefined voltage values which are applied to the second tap 12 by the DAC 20 when the microprocessor 23 is operating in the calibration mode may be stored in the microprocessor 23, or may be written to the microprocessor 23 from an external source. Additionally, digital words which are indicative of the ideal values with which the digital words which are read from the digital output 35 of the analogue-to-digital converter 33 are to be compared may also be stored in the microprocessor 23, or may be written to the microprocessor 23 from an external source.

The microprocessor 23 is programmed so that on an appropriate calibration instruction being inputted to the microprocessor 23, the microprocessor operates in the calibration mode for calibrating the voltage regulator 30.

In the normal operating mode, the microprocessor 23 is programmed to appropriately apply the calibration values or the calibration function stored in the non-volatile memory 37 to each digital word written to the DAC 20 in order to produce the regulated voltage across the first and second output terminals 5 and 6 of the desired selected voltage value corrected for any errors in the voltage regulator 30.

In use, in the calibration mode, the microprocessor 23 sequentially writes the series of the predefined digital words to the DAC 20, which in turn applies the corresponding predefined voltages between ground voltage and the value of the voltage reference to the second tap 12. The microprocessor 23 reads the corresponding digital words from the digital output 35 of the analogue-to-digital converter 33. The read values of the digital words from the digital output 35 of the analogue-to-digital converter 33 are then compared by the microprocessor 23 with the respective corresponding ideal values, and the calibration values are computed from the difference, if any, in the corresponding values of the read digital words from the analogue-to-digital converter 33 and the corresponding ideal values. A

calibration function may then be prepared from the calibration values. The calibration values and/or the calibration function are then stored in the non-volatile memory 37. The microprocessor 23 is then ready to operate in the normal operating mode to operate the voltage regulator 30 to produce the regulated output voltage
5 across the first and second output terminals 5 and 6 of the desired selected value as already described with reference to the voltage regulator 1 of Fig. 1.

Otherwise, the voltage regulator 30 and its operation is similar to the voltage regulator 1.

10

Referring now to Fig. 3, there is illustrated a voltage regulator according to another embodiment of the invention, indicated generally by the reference numeral 40, for producing a regulated DC voltage supply from an input voltage supply, which in this case is an unregulated DC voltage supply. The voltage regulator 40 in this
15 embodiment of the invention is a linear mode voltage regulator, and the components of the linear mode voltage regulator 40 which are similar to those of the switched mode voltage regulator 1 described with reference to Fig. 1 are identified by the same reference numerals. However, in this embodiment of the invention, being a linear mode voltage regulator, the voltage regulator 40 comprises a control circuit 41
20 within which a pass element 42 is located, and through which the load current passes from the positive first input terminal 3 to the positive first output terminal 5 to the load 9. The control circuit 41 may be of any suitable type which is required by a linear mode voltage regulator, and will be well known to those skilled in the art, and further description should not be required. The pass element 42 may be any
25 suitable pass element. One type of pass element is a field effect transistor.

An impedance-divider circuit, which in this embodiment of the invention is provided by a resistor-divider circuit 10 similar to the resistor-divider circuit 10 of the voltage regulator 1 controls the voltage produced across the first and second output
30 terminals 5 and 6 at the selected regulated voltage value. As with the voltage regulator 1, the first tap 11 of the resistor-divider circuit 10 of the voltage regulator 40 is connected to the first output terminal 5, and the second tap 12 of the resistor-divider circuit 10 is connected to the output 21 of the high resolution DAC 20. The

intermediate tap 15 of the resistor-divider circuit 10 is connected to the inverting input of the error amplifier 17, and the voltage reference is applied to the non-inverting input of the error amplifier 17. The error amplifier 17 forms a feedback loop with the pass element 42, so that the error amplifier 17 operates to force the voltage on the first output terminal 5 to the regulated voltage value, in order to maintain the voltage on the intermediate tap 15 of the resistor-divider circuit 10 substantially at the voltage value of the voltage reference.

In the same manner that the DAC 20 under the control of the microprocessor 23 applies voltage values to the second tap 12 of the resistor-divider circuit 10 of the voltage regulator 1 to vary the voltage value of the regulated output voltage produced across the first and second output terminals 5 and 6 of the voltage regulator 1, the DAC 20 of the linear mode voltage regulator 40 applies voltage values to the second tap 12 of the resistor-divider circuit 10 between the voltage value of the voltage on the second output terminal 6, namely, ground voltage and the value of the voltage reference V_{ref} , in order to vary the regulated output voltage produced across the first and second output terminals 5 and 6 between the maximum value of the regulated voltage value and the minimum value, which in this case is also equal to the value of the voltage reference produced by the voltage reference circuit 19.

Otherwise, the linear mode voltage regulator 40 and its operation is similar to that of the voltage regulator 1, with the exception that the control circuit 41 of the voltage regulator 40 is of a type required by a linear mode voltage regulator, while the control circuit 8 of the voltage regulator 1 is of a type required by a switched mode voltage regulator.

Referring now to Fig. 4, there is illustrated a voltage regulator according to another embodiment of the invention, indicated generally by the reference numeral 50, for producing a regulated DC voltage supply from an unregulated DC voltage supply. The voltage regulator 50 in this embodiment of the invention is a switched mode voltage regulator, and is substantially similar to the voltage regulator 1, and similar components are identified by the same reference numerals. In this embodiment of

the invention the means for selectively varying the voltage on the second tap 12 of the resistor-divider circuit 10 relative to the voltage on the second output terminal 6 for in turn varying the value of the regulated output voltage produced across the first and second output terminals 5 and 6 comprises a digital potentiometer 51. The digital potentiometer 51 is connected between the second tap 12 of the resistor-divider circuit 10 and the second output terminal 6. The resistance of the digital potentiometer 51 is selectively varied by the microprocessor 23 for in turn varying the voltage on the second tap 12 relative to the second output terminal 6.

10 The microprocessor 23 is programmed to vary the resistance of the digital potentiometer 51 for incrementally increasing the resistance produced between the second tap 12 and the output terminal 6 from zero ohms upwardly. When the resistance produced by the digital potentiometer 51 between the second tap 12 and the second output terminal 6 is zero ohms, the voltage on the second tap is ground voltage. As the resistance produced by the digital potentiometer 51 between the second tap 12 and the output terminal 6 is increased incrementally from zero ohms upwardly, the voltage on the second tap 12 relative to the second output terminal 6 is progressively incremented, thereby progressively decrementing the value of the regulated voltage produced across the first and second output terminals 5 and 6.

20

Otherwise, operation of the voltage regulator 50 is similar to that of the voltage regulator 1.

While the voltage regulators 1, 30, 40 and 50 have been described as comprising only the minimum amount of components which are relevant to the invention, it will be readily apparent to those skilled in the art that the voltage regulators 1, 30 and 40 will contain many other components of a type which would commonly be required for a switched mode voltage regulator in the case of the switched mode voltage regulators 1, 30 and 50, and of a type which would be required for a linear mode voltage regulator in the case of the voltage regulator 40.

30

While first and second resistors of specific resistance values have been described, it will be readily apparent to those skilled in the art that the first and second resistors

may be of any other suitable resistance values. Furthermore, it will be appreciated that while the voltage reference produced by the voltage reference circuit has been described as being 0.6 volts, voltage references of other values may be used.

Indeed, the choice of resistance values of the first and second resistors and the
5 choice of the value of the voltage reference are interdependent, and are also dependent on the range of the regulated output voltage to be produced across the output terminals, within which the regulated output voltage is to be selectable. Needless to say, the voltage values to be produced by the DAC 20 for applying to the second tap of the resistor-divider circuit 10 will also be dependent on the
10 resistance values of the first and second resistors, the value of the voltage reference, and the range of regulated output voltage to be produced across the output terminals, within which the regulated output voltage is to be selectable.

It will also be appreciated that the resistance values within which the digital
15 potentiometer must be operable will be dependent on the range of values within which the regulated voltage is to be produced across the first and second output terminals. The resistance values within which the digital potentiometer must be operable will also be dependent on the values of the first and second resistors R1 and R2, and on the voltage reference.

20

It is also envisaged that the linear mode voltage regulator 40 may include a calibration circuit similar to the calibration circuit 31 of the switched mode voltage regulator 30.

25 It is also envisaged that the voltage on the second tap of the resistor-divider circuit of the linear mode voltage regulator may be varied by a digital potentiometer connected between the second tap 12 and the second output terminal 6 as described with reference to the switched mode voltage regulator 50 of Fig. 4.

30 While the resistor-divider circuits have been described as being connected directly to one of the output terminals, and to the output of the DAC 20 or the digital potentiometer as the case may be, it will be appreciated that the connections of the resistor-divider circuits 10 to the one of the output terminals and to the output of the

DAC 20 or the digital potentiometer may not be direct connections, but rather, the resistor-divider circuits 10 may be connected to the one of the output terminals and to the output of the DAC 20 or the digital potentiometer through any suitable current path. Needless to say, any other components in the voltage regulator circuits which
5 have been described as being directly connected together, may be connected where appropriate through any other suitable current paths.

Additionally, while the switched mode voltage regulators 1, 30 and 50 have been described as being voltage regulators operating with a control circuit substantially
10 similar to that disclosed in U.S. Patent Specification No. 5,481,178, it will of course be appreciated that the control circuit of the switched mode voltage regulator may not be similar to the control circuit of the switched mode voltage regulator of U.S. Patent Specification No. 5,481,178 but may be of any other suitable type.

15 While the impedance-divider circuits of the voltage regulators have been described as being resistor-divider circuits, it is envisaged that other impedance-divider circuits besides resistor-divider circuits may be provided. Needless to say, while the resistor-divider circuits have been described as comprising only two resistors, the resistor-divider circuits may include any desired number of resistors. In cases where
20 more than two resistors are provided, the intermediate tap would be provided by a tap defined between two adjacent series connected resistors. Where the resistor-divider circuits are provided with more than two resistors, all the resistors may be connected in series, or alternatively, some of the resistors may be connected in series, and others of the resistors would be connected in parallel with the series
25 connected resistors.

While the means for varying the voltage applied to the second tap of the resistor-divider circuits of the voltage regulators has been described as comprising a variable voltage producing means in the form of a digital-to-analogue converter and in the
30 form of a digital potentiometer which are operated under the control of a microprocessor, any other suitable means for producing a selectable variable voltage, which is relative to or referenced to the voltage on the second output terminal, for applying to the second tap of the resistor-divider circuit may be

provided, and in certain cases, it is envisaged that the means for providing the variable voltage on the second tap of the resistor-divider circuits may be provided by a buffered potentiometer.

5 While the variable voltage producing means for varying the voltage on the second tap of the resistor-divider circuit has been described as being provided by a high resolution digital-to-analogue converter, any suitable digital-to-analogue converter may be used. However, the resolution with which the regulated output voltage is provided across the output terminals is dependent on the resolution of the digital-to-
10 analogue converter, and thus, it is preferable that the digital-to-analogue converter be a relatively high resolution digital-to-analogue converter, for example, a 12-bit digital-to-analogue converter, although reasonable results would be achieved using an 8-bit digital-to-analogue converter.

15 It is also envisaged that the resistors of the resistor-divider circuit may be replaced by digital potentiometers, and in particular, it is envisaged that the second resistor may be replaced by a digital potentiometer.

While the DAC 20 has been described as applying voltages to the second tap of the
20 resistor-divider circuits of the voltage regulators within a range between a first voltage value equal to ground voltage and a second voltage value equal to the value of the voltage reference, it will be appreciated that the voltage range between the first and second voltage values may be any suitable range of voltage values within the range of ground voltage to the value of the voltage reference. For example, the
25 first voltage value may lie in a voltage range between the value of the voltage on the second output terminal and the voltage at which the intermediate tap of the resistor-divider circuit is held, and the second voltage value may lie in a voltage range between the value of the voltage on the second output terminal and the voltage at which the intermediate tap of the resistor-divider circuit is held. However, the first
30 voltage value would be of a value less than the second voltage value.

It will also of course be appreciated that the common voltage at which the second input terminal and the second output terminal are held may be a voltage other than

ground voltage, and in which case, the lowest voltage of the range of voltages which would be applied to the second tap of the resistor-divider circuits of the voltage regulators by the DAC 20 would be the value of the common voltage.

5 It is envisaged that the regulated output voltage produced across the first and second output terminals may float relative to the input voltage applied to the first and second input terminals. In which case, the voltage on the second output terminal would be different to the voltage on the second input terminal. In such cases, the lowest voltage value which would be applied by the DAC 20 or the digital
10 potentiometer to the second tap of the resistor-divider circuit would be the voltage on the second output terminal.

It will of course be appreciated that all voltage values which are applied to the second tap of the resistor-divider circuits of the voltage regulators will be referenced
15 to the voltage on the second output terminal.

While the voltage regulators have been described with the first input and the first output terminals being positive terminals, it will be appreciated that the first input terminal and the first output terminal may be negative terminals, and in which case,
20 the first input terminal and the first output terminal will be at voltage values less than the common voltage value at which the second input and the second output terminals are held. In which case, the rest of the circuitry of the voltage regulators will be appropriately configured as will be well understood by those skilled in the art.

25 While the voltage regulators have been described for producing selectively variable regulated voltage values within specific voltage ranges, it will be appreciated that the voltage regulators according to the invention may be configured to produce selectively variable regulated voltage values within any desired range within which such switched mode voltage regulators and linear mode voltage regulators would be
30 capable of producing. It will also of course be appreciated that the voltage regulators according to the invention may be configured to produce the selectively variable regulated voltages from any input voltage supply, be it an unregulated DC voltage supply or a regulated DC voltage supply. Indeed, it will be readily apparent

to those skilled in the art that the voltage regulators may be configured to produce the selectively variable regulated DC output voltage from an AC voltage supply, and where the input voltage supply is an AC voltage supply, the AC voltage supply would be appropriately rectified to a DC voltage supply. Needless to say, the voltage value
5 and the range of voltage values within which the input voltage supply may vary would be consistent with voltage supplies with which conventional switched mode and linear mode voltage regulators are capable of operating.

It is also envisaged that the second resistor of the voltage regulators according to
10 the invention may be provided in a manner in which it may be replaced with one or more resistors of respective different resistance values. This would permit the voltage range over which the regulated output voltage would be produced to be significantly increased, while at the same time retaining the advantage of the invention whereby the regulated output voltage can be varied in relatively small
15 incremental and decremental steps. The values of the replaceable second resistors would be such that by replacing one second resistor with another, the maximum value of the regulated output voltage produced by the voltage regulator with one resistor would be not less than the minimum value of the regulated output voltage which would be produced by the voltage regulator with the resistor of next value, and
20 so on.

Claims

1. A voltage regulator for producing a selectively variable regulated DC voltage supply from an input voltage supply, the voltage regulator comprising first and second output terminals across which the regulated voltage is produced, an
5 impedance-divider circuit comprising a pair of series connected impedance elements between a first tap and a second tap, the series connected impedance elements defining an intermediate tap therebetween, the first tap of the impedance-divider circuit being connected to the first output terminal through a current path, a control circuit co-operable with the impedance-divider circuit and being adapted to force the
10 voltage on the first output terminal to the regulated voltage value in order to maintain the voltage on the intermediate tap of the impedance-divider circuit at a predefined fixed value, and a means for selectively varying the voltage on the second tap of the impedance-divider circuit relative to the voltage on the second output terminal for varying the value of the regulated voltage produced across the first and second
15 output terminals.
2. A voltage regulator as claimed in Claim 1 in which the means for varying the voltage on the second tap of the impedance-divider circuit is adapted to vary the voltage on the second tap between a first voltage value and a second voltage value,
20 the first and second voltage values lying in respective ranges of voltage values between the voltage on the second output terminal and the voltage on the intermediate tap of the impedance-divider circuit.
3. A voltage regulator as claimed in Claim 2 in which the first voltage value is
25 substantially equal to the voltage on the second output terminal.
4. A voltage regulator as claimed in Claim 2 or 3 in which the second voltage value is substantially equal to the voltage on the intermediate tap of the impedance-
30 divider circuit.
5. A voltage regulator as claimed in any preceding claim in which the means for varying the voltage on the second tap of the impedance-divider circuit comprises a variable voltage producing means.

6. A voltage regulator as claimed in Claim 5 in which the variable voltage producing means comprises a high resolution variable voltage producing means.
- 5 7. A voltage regulator as claimed in Claim 5 or 6 in which the variable voltage producing means comprises a digital-to-analogue converter.
8. A voltage regulator as claimed in Claim 7 in which the digital-to-analogue converter is configured to have a resolution of at least 8 bits.
- 10 9. A voltage regulator as claimed in Claim 7 or 8 in which the digital-to-analogue converter is configured to have a resolution in the order of 12 bits.
- 15 10. A voltage regulator as claimed in any of Claims 7 to 9 in which the analogue output voltage produced by the digital-to-analogue converter is applied to the second tap of the impedance-divider circuit.
- 20 11. A voltage regulator as claimed in any of Claims 7 to 10 in which an analogue output of the digital-to-analogue converter is connected to the second tap through a current path.
12. A voltage regulator as claimed in Claim 5 or 6 in which the variable voltage producing means comprises a digital potentiometer.
- 25 13. A voltage regulator as claimed in any of Claims 5 to 12 in which a programmable element is provided for controlling the variable voltage producing means to provide selectable voltage values for applying to the second tap of the impedance-divider circuit.
- 30 14. A voltage regulator as claimed in Claim 13 in which the programmable element comprises a microprocessor, and the microprocessor is programmed to receive inputs indicative of respective selectable regulated voltage values.

15. A voltage regulator as claimed in Claim 14 in which the microprocessor is responsive to an input indicative of a selectable regulated voltage value inputted thereto to operate the variable voltage producing means to apply a voltage to the
5 second tap of the impedance-divider circuit of a value to produce the selected regulated voltage across the first and second output terminals.
16. A voltage regulator as claimed in Claim 14 or 15 in which a calibration circuit is provided for calibrating the voltage regulator.
- 10 17. A voltage regulator as claimed in Claim 16 in which the calibration circuit comprises a means for reading a voltage indicative of the regulated voltage produced across the first and second output terminals, and a means for comparing the read voltage indicative of the regulated voltage produced across the first and
15 second output terminals with an ideal voltage value.
18. A voltage regulator as claimed in Claim 17 in which a means is provided for deriving a calibration value from the comparison of the read voltage indicative of regulated voltage produced across the first and second output terminals and the
20 ideal voltage value.
19. A voltage regulator as claimed in Claim 17 or 18 in which the microprocessor is programmed to read the voltage indicative of the regulated voltage produced across the first and second output terminals and to compare the read voltage
25 indicative of the regulated voltage produced across the first and second output terminals with the ideal voltage.
20. A voltage regulator as claimed in Claim 19 in which the microprocessor is programmed to compute the calibration value.
- 30 21. A voltage regulator as claimed in Claim 19 or 20 in which the microprocessor is programmed to operate the variable voltage producing means to apply a predefined voltage to the second tap of the impedance-divider circuit to produce a

regulated voltage across the first and second output terminals, and to read the voltage indicative of regulated voltage produced across the first and second output terminals in response to the predefined voltage applied to the second tap for comparison with the ideal voltage value.

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22. A voltage regulator as claimed in any of Claims 19 to 21 in which the microprocessor is programmed to operate the variable voltage producing means to apply at least two predefined voltages of different voltage values to the second tap of the impedance-divider circuit and to read voltage values indicative of the respective regulated voltages produced across the first and second output terminals in response to the two predefined voltage values applied to the second tap, and to compute respective calibration values from a comparison of the two read voltage values indicative of the regulated voltage produced across the first and second output terminals with corresponding respective ideal values.

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23. A voltage regulator as claimed in any of Claims 19 to 22 in which each calibration value is stored in a non-volatile memory readable by the microprocessor.

24. A voltage regulator as claimed in any of Claims 19 to 23 in which each ideal value of the regulated voltage is stored in the microprocessor.

15

25. A voltage regulator as claimed in any of Claims 19 to 24 in which the microprocessor is programmed to operate the variable voltage producing means to apply the voltages to the second tap of the impedance-divider circuit corrected with the calibration value to produce the respective regulated voltages across the first and second output terminals of the selected voltage values.

20

26. A voltage regulator as claimed in any preceding claim in which one of a inverting input and a non-inverting input of an error amplifier is connected through a current path to the intermediate tap of the impedance-divider circuit, and the other of the inverting and the non-inverting inputs of the error amplifier is connected through a current path to a voltage reference, the error amplifier forming with the control circuit a feedback loop to force the voltage on the first output terminal to the

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regulated voltage value in order to maintain the voltage on the intermediate tap of the impedance-divider circuit at the predefined fixed voltage.

27. A voltage regulator as claimed in Claim 26 in which the predefined fixed
5 voltage is of value substantially equal to the value of the voltage reference.

28. A voltage regulator as claimed in any preceding claim in which a pair of input terminals are provided for receiving the input voltage supply.

10 29. A voltage regulator as claimed in Claim 28 in which the second output terminal and one of the input terminals are held at a common voltage.

30. A voltage regulator as claimed in Claim 29 in which the common voltage is ground voltage.
15

31. A voltage regulator as claimed in any preceding claim in which each impedance element of the impedance-divider circuit comprises an impedance element of substantially fixed impedance value.

20 32. A voltage regulator as claimed in any preceding claim in which the impedance-divider circuit comprises a resistor-divider circuit.

33. A voltage regulator as claimed in Claim 32 in which the resistance value of the resistor-divider circuit between the second tap and the intermediate tap is in the
25 range of 8.25 Kohms to 60.4 Kohms when the resistance value of the resistor-divider circuit between the first tap and the intermediate tap is in the order of 60.4 Kohms.

34. A voltage regulator as claimed in Claim 32 or 33 in which the resistor-divider circuit comprises a first resistor connected between the first tap and the intermediate
30 tap, and a second resistor connected between the second tap and the intermediate tap.

35. A voltage regulator as claimed in any preceding claim in which the voltage regulator is adapted for producing selectable regulated DC voltages across the first and second output terminals of values in the range of zero volts to the maximum regulated voltage value of which the voltage regulator is configured to produce.
- 5
36. A voltage regulator as claimed in any preceding claim in which the voltage regulator is adapted for producing selectable regulated DC voltages across the first and second output terminals of values up to 60 volts.
- 10
37. A voltage regulator as claimed in any preceding claim in which the voltage regulator is adapted for producing selectable regulated DC voltages across the first and second output terminals of values up to 12 volts.
38. A voltage regulator as claimed in any preceding claim in which the voltage
15 regulator is adapted for receiving an unregulated DC voltage supply.
39. A voltage regulator as claimed in any preceding claim in which the voltage regulator is configured as a switched mode voltage regulator.
- 20
40. A voltage regulator as claimed in any preceding claim in which the voltage regulator is configured as a linear mode voltage regulator.
41. A voltage regulator as claimed in any preceding claim in which the voltage
25 regulator is adapted to be produced as an integrated circuit.
42. A voltage regulator as claimed in any preceding claim in which the voltage regulator is adapted to be produced as a module.
43. A voltage regulator as claimed in any of Claims 1 to 40 in which the voltage
30 regulator is adapted to be produced from discrete parts.
44. A method for operating a voltage regulator for producing a selectively

variable regulated DC voltage supply from an input voltage supply, the voltage regulator being of the type comprising first and second output terminals across which the regulated voltage is produced, an impedance-divider circuit comprising a pair of series connected impedance elements between a first tap and a second tap, the first and second impedance elements defining an intermediate tap therebetween, the first tap of the impedance-divider circuit being connected to the first output terminal through a current path, and a control circuit co-operable with the impedance-divider circuit and being adapted to force the voltage on the first output terminal to the regulated voltage value in order to maintain the voltage on the intermediate tap of the impedance-divider circuit at a predefined fixed value, the method comprising selectively varying the voltage on the second tap of the impedance-divider circuit relative to the voltage on the second output terminal for varying the value of the regulated voltage produced across the first and second output terminals.

45. A method as claimed in Claim 44 in which the voltage on the second output tap is varied between a first voltage value and a second voltage value, the first and second voltage values lying in respective ranges of voltage values between the voltage on the second output terminal and the voltage on the intermediate tap of the impedance-divider circuit.

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46. A method as claimed in Claim 45 in which the first voltage value is substantially equal to the voltage on the second output terminal.

47. A method as claimed in Claim 45 or 46 in which the second voltage value is substantially equal to the voltage on the intermediate tap of the impedance-divider circuit.

48. A method as claimed in any of Claims 44 to 47 in which the voltage on the second tap of the impedance-divider circuit is varied by applying a voltage thereto from a variable voltage producing means.

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49. A method as claimed in Claim 48 in which the variable voltage producing means comprises a high resolution variable voltage producing means.

50. A method as claimed in Claim 48 or 49 in which the variable voltage producing means comprises a digital-to-analogue converter.

5 51. A method as claimed in Claim 48 or 49 in which the variable voltage producing means comprises a digital potentiometer.

52. A method as claimed in any of Claims 48 to 51 in which the variable voltage producing means is controlled by a programmable element for producing the
10 variable voltage.

53. A method as claimed in Claim 52 in which the programmable element comprises a microprocessor.

15 54. A method as claimed in any of Claims 44 to 53 further comprising calibrating the voltage regulator.

55. A method as claimed in Claim 54 in which the voltage regulator is calibrated by comparing a voltage indicative of the regulated voltage produced across the first
20 and second output terminals with an ideal voltage value and deriving a calibration value from the comparison.

56. A method as claimed in Claim 55 in which a predefined voltage is applied to the second tap of the impedance-divider circuit, and a voltage indicative of a
25 regulated voltage produced across the first and second output terminals in response to the predefined voltage is compared with an ideal voltage for producing the calibration value.

57. A method as claimed in any of Claims 54 to 56 in which each voltage applied
30 to the second tap of the impedance-divider circuit to produce a selected regulated voltage across the first and second output terminals is corrected with the calibration value.

58. A method as claimed in any of Claims 54 to 57 in which respective voltages of different predefined voltage values are applied to the second tap of the impedance-divider circuit, and voltages indicative of the corresponding regulated
5 voltages produced across the first and second output terminals are compared with corresponding ideal voltage values for producing respective calibration values.

59. A method as claimed in any of Claims 54 to 58 in which each calibration value is stored in a non-volatile memory.
10

60. A method as claimed in any of Claims 54 to 59 in which the ideal voltage values are stored in the microprocessor.

61. A method as claimed in any of Claims 44 to 60 in which the method is
15 adapted for operating a switched mode voltage regulator for producing the selectively variable DC voltage supply.

62. A method as claimed in any of Claims 44 to 61 in which the method is
20 adapted for operating a linear mode voltage regulator for producing the selectively variable DC voltage supply.

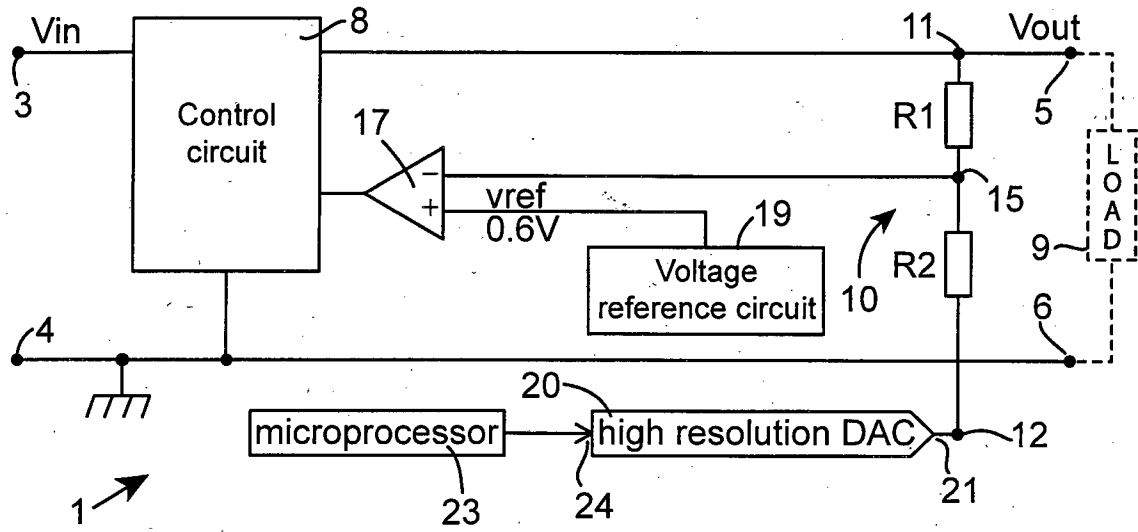


Fig. 1

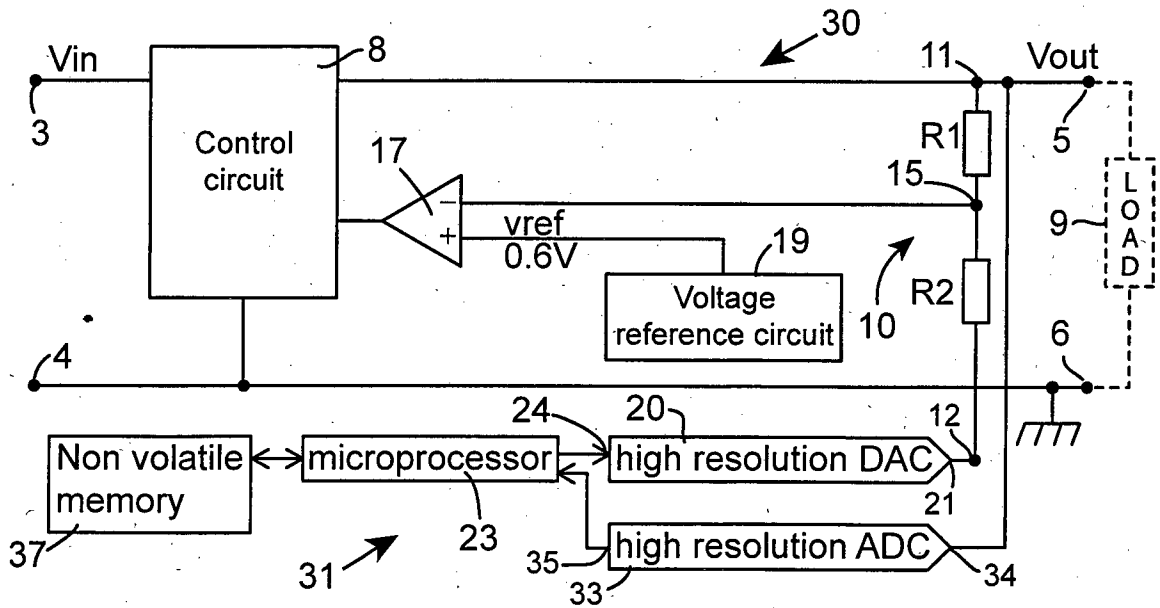


Fig. 2

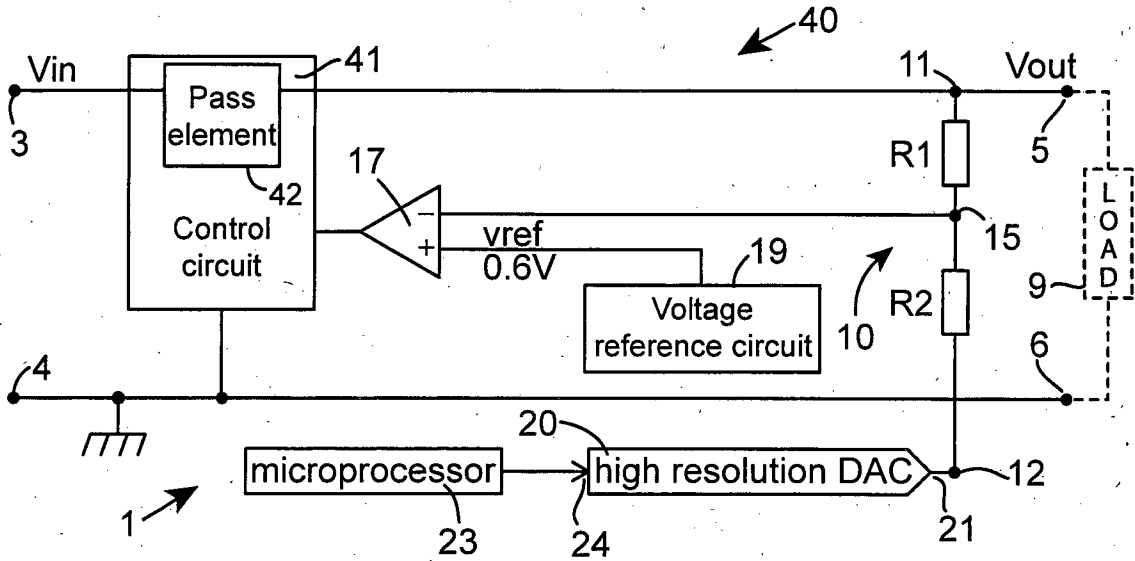


Fig. 3

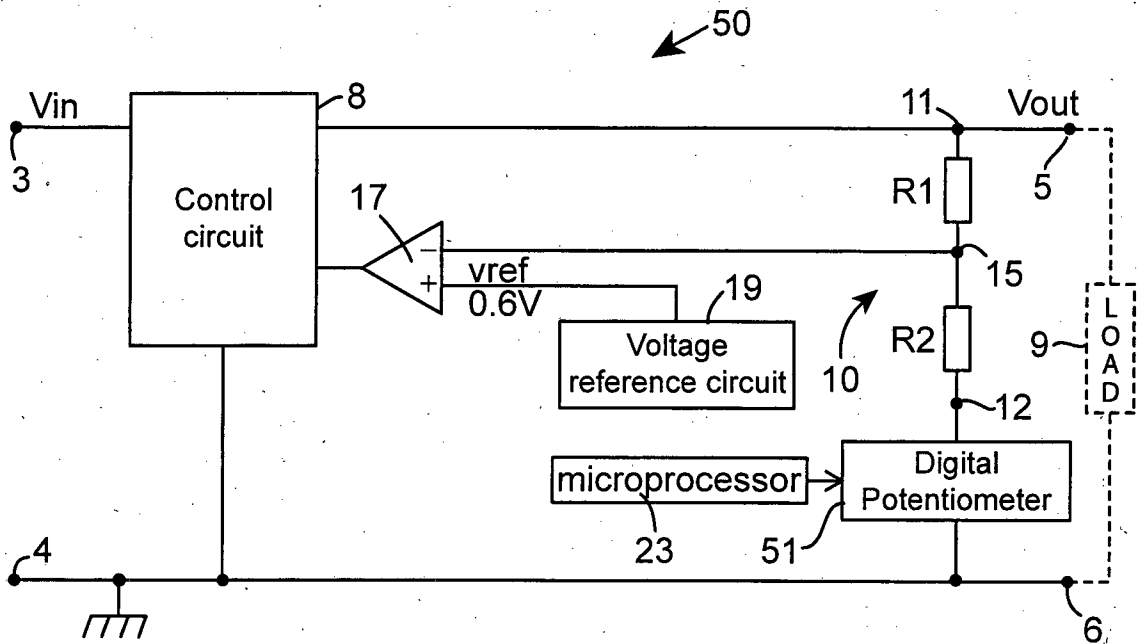


Fig. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/IE2011/000016

A. CLASSIFICATION OF SUBJECT MATTER
INV. G05F1/46
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/057934 A1 (JIA XUAN-CE [CN] ET AL) 15 March 2007 (2007-03-15) figure 3	1-62
A	----- US 7 218 168 B1 (RAHMAN ARIFUR [US]) 15 May 2007 (2007-05-15) the whole document	1-62
A	----- US 6 377 033 B2 (HSU HUI-TE [TW]) 23 April 2002 (2002-04-23) cited in the application the whole document	1-62
A	----- US 5 481 178 A (WILCOX MILTON E [US] ET AL) 2 January 1996 (1996-01-02) cited in the application the whole document	1-62

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

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- "E" earlier document but published on or after the international filing date
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- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

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- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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- "&" document member of the same patent family

Date of the actual completion of the international search 27 May 2011	Date of mailing of the international search report 10/06/2011
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Sundin, Martin
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/IE2011/000016

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