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Peters

[11] **3,777,183**

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[54] **TRANSISTOR CONTROL APPARATUS**

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[52] **U.S. Cl.** ..... **307/268,** 307/237, 315/169 TV

[51] **Int. Cl.** **H03k 5/01**

[58] **Field of Search** ..... 307/237, 261, 263, 307/268, 280; 315/169 R, 169 TV

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Assistant Examiner—R. E. Hart
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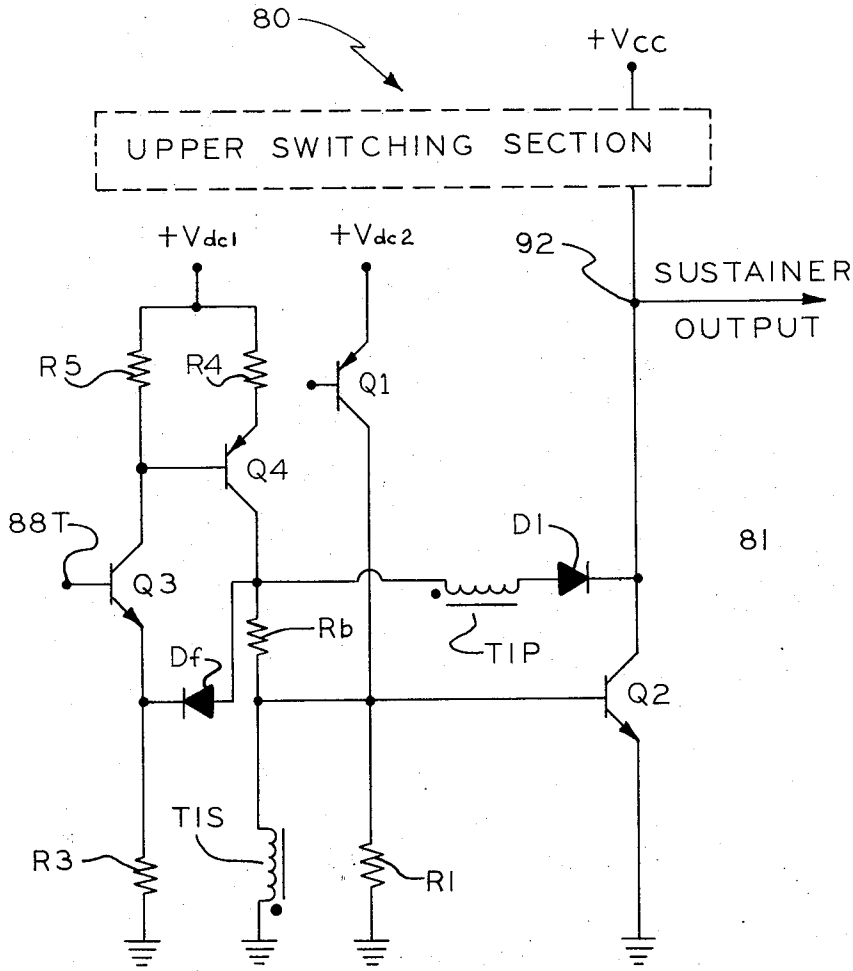
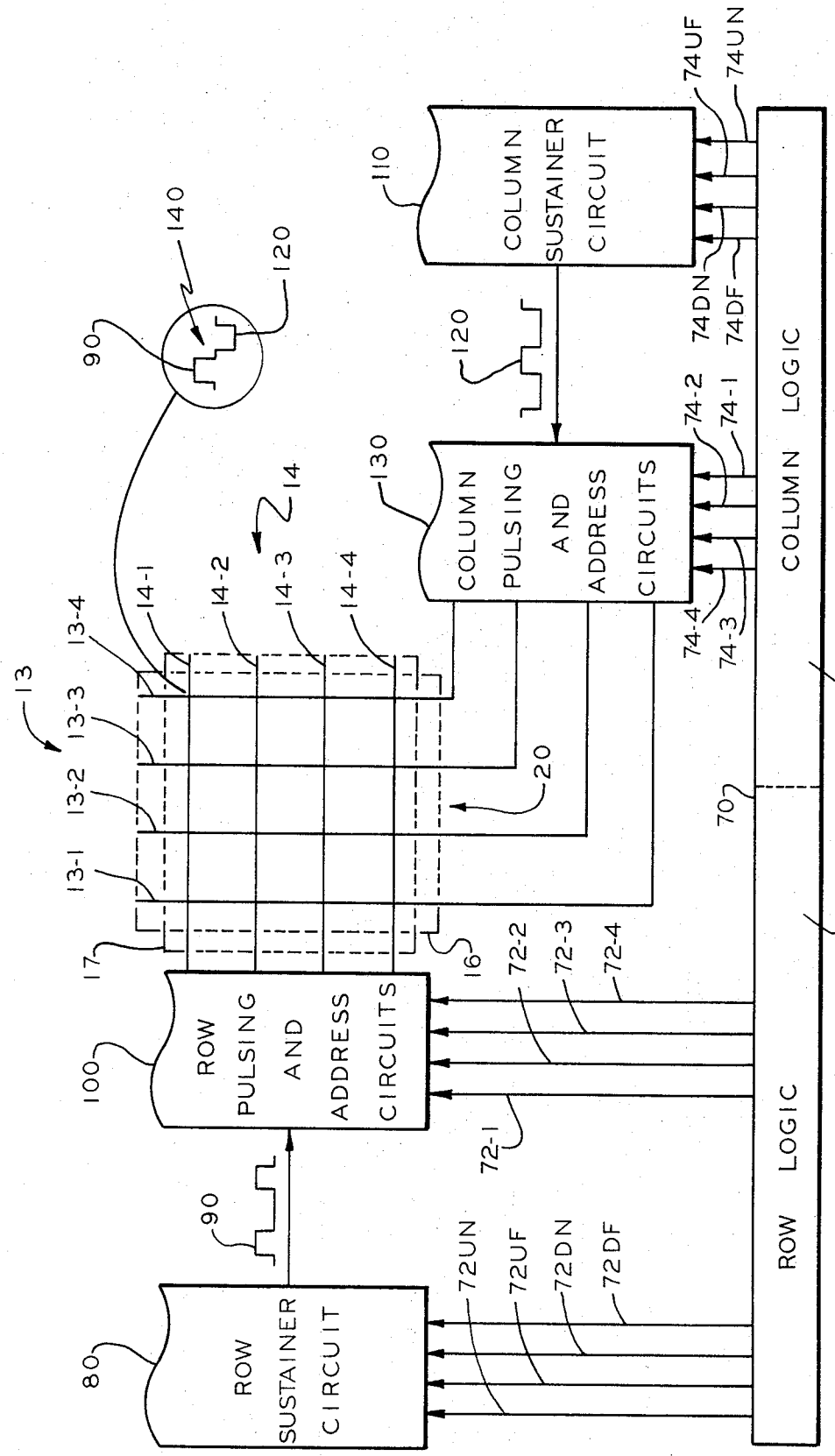
[57] **ABSTRACT**

There is disclosed a system utilizing transistor control apparatus for supplying operating potentials which is particularly useful with load device wherein at least two transversely oriented conductors are dielectrically isolated from a gaseous discharge medium between the conductors. The invention is illustrated in wave form generators, each having at least one output transistor. Novel transformer-diode clamping means are provided which may automatically sense saturation of an output transistor and reverse bias the collector-base junctions of the output transistors, to bring deeply saturated transistors out of saturation and enable them to turn off much more rapidly than was possible heretofore, and to sense the driving current for the primary winding of the transformer to keep the output transistor biased near saturation. The system shown thus produces a more effective wave form having steeper leading and trailing edges, the wave form in the embodiment shown being used as a sustaining voltage for cells in a gas discharge display/memory panel.

10 Claims, 3 Drawing Figures




ROW SUSTAINER CIRCUIT
80
90
ROW PULSING AND ADDRESS CIRCUITS
100
COLUMN SUSTAINER CIRCUIT
110
120
140
90
120
COLUMN PULSING AND ADDRESS CIRCUITS
130
14
14-1
14-2
14-3
14-4
13
13-1
13-2
13-3
13-4
17
16
20
72-1
72-2
72-3
72-4
72UN
72UF
72DN
72DF
ROW LOGIC
72
70
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74-1
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74-4
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74UF
74UN
19

FIG. 1

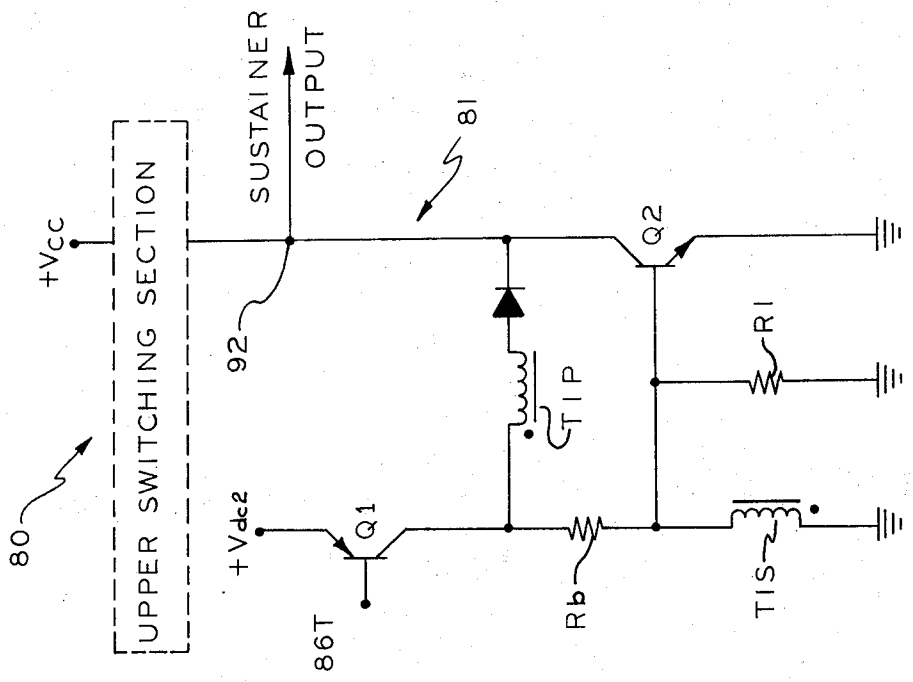
+Vcc
UPPER SWITCHING SECTION
80
SUSTAINER OUTPUT
92
81
Q2
R1
TIP
+Vdc2
Q1
86T
Rb
TIS

FIG. 3

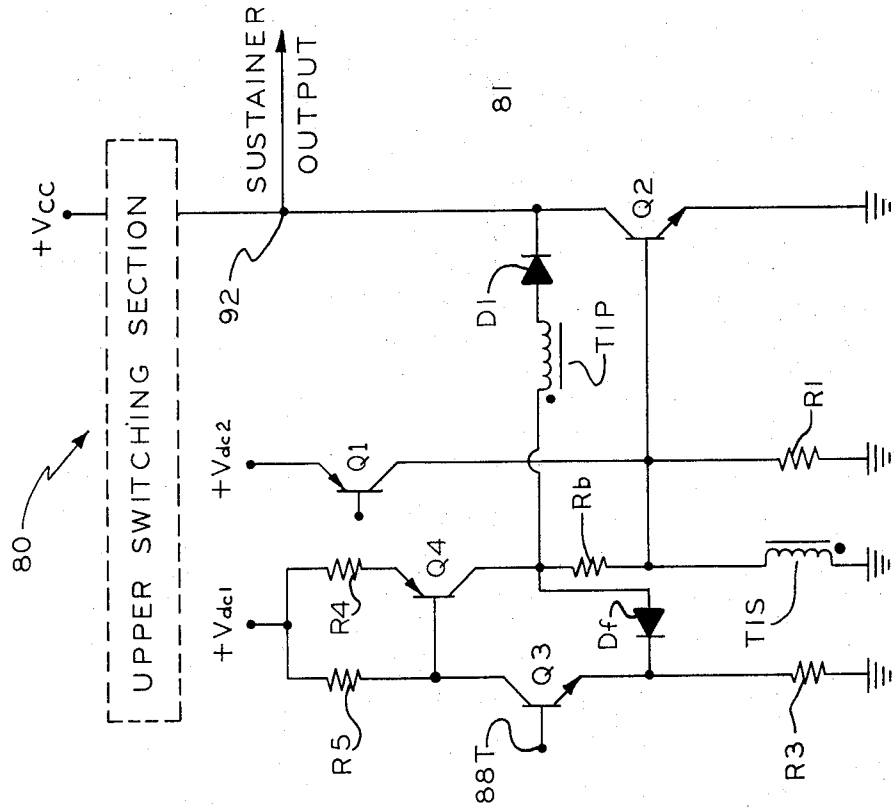
+Vcc
UPPER SWITCHING SECTION
80
SUSTAINER OUTPUT
92
81
Q2
D1
TIP
R1
+Vdc2
Q1
Rb
+Vdc1
R4
Q4
Df
TIS
R5
Q3
88T
R3

FIG. 2

TRANSISTOR CONTROL APPARATUS

BACKGROUND OF THE INVENTION

In the Baker, et al. U.S. Pat. No. 3,499,167, issued Mar. 3, 1970, there is disclosed a multiple discharge display and/or memory panel which may be characterized as being of the pulsing discharge type having a gaseous medium, usually a mixture of two gases at a relatively high gas pressure, in a thin gas chamber of space between opposed dielectric charge storage members which are backed by conductor arrays. The conductor arrays backing each dielectric member are transversely oriented to define or locate a plurality of discrete discharge volumes or sites and constitute a discrete discharge unit. In some cases, the discharge units may be additionally defined by physical structures such as perforated glass plates and the like and in other cases capillary tubes and like structures may be used.

In the above-identified patent application of Baker, et al., physical barriers and isolation members for discrete discharge sites have been eliminated. In such devices charges (electrons and ions) produced upon ionization of the gas at a selected discharge site or conductor crosspoint, when proper operating potentials are applied to selected conductors thereof, are stored upon the surfaces of the dielectric at the selected locations or sites and constitute an electrical field opposing the electrical field which created them. After a firing potential has been applied to initiate a discharge, the electrical field created by the charges stored upon the dielectric members aids in initiating subsequent momentary or pulsing discharges on succeeding half cycles of an applied sustaining potential so that the applied potential, and hence the storage charges indicate the previous discharge condition of a discharge unit or site and can constitute an electrical memory.

In dynamic operation, in addition to the sustaining voltages, writing and erasing pulses may be superimposed on and algebraically added to the sustaining wave forms applied to selected transverse conductor pairs in the conductor arrays to manipulate discharge conditions of discharge sites. Some of the preferred types of circuits for supplying the sustaining potentials, and for generating the manipulating pulses to be added to the sustaining potentials, utilize output transistors which are driven into deep saturation to abruptly switch the wave form from one potential level to another.

Difficulties have been encountered in the past, in that when a transistor is turned "on" and driven into deep saturation, it is difficult to bring the transistor out of saturation and turn it "off" quickly. This makes control of the shape of the trailing edge of the wave form difficult, may interfere with the addition of manipulating pulses, may make a manipulating pulse have an effective width that is too narrow, etc., and is undesirable. Diode clamping circuits have been proposed and are useful in certain applications for bringing transistors out of saturation within the time limits of those previous systems. However, as the switching speeds increase and as the type of wave forms applied as sustaining potentials and as manipulating pulses become more complex, the diode clamping circuit is not suitable for all applications.

Accordingly, it is an object of this invention to provide an improved transformer-diode clamping means, which is particularly useful in providing improved systems for supplying operating potentials to load devices, and even further particularly useful wherein the load devices are of the gas discharge display/memory type.

It is another object of this invention to provide improved voltage wave form generating means which includes at least two sections, each of the sections having an output transistor to connect first and second potential levels to the load device.

It is a further object of this invention to provide improved control apparatus for transistors in which novel transformer-diode clamping circuits may be utilized to automatically sense transistor saturation and to bring the transistor out of saturation and permit the transistor to be turned "off" more quickly, and also to sense the driving current for the primary winding of the transformer to keep the output transistor near saturation.

SUMMARY OF THE INVENTION

The invention is disclosed and described herein in a system for supplying operating potentials to a gas discharge display/memory device of the type described hereinbefore. A wave form generating means is shown which includes at least two sections, a first of the sections being operative to connect a first potential level to the output of the generator, while a second of the sections is operative to connect a second potential level to the output, the output being connected to conductors in the array of the gas discharge device.

Each of the output sections includes at least one output transistor means operating as a switching means between its respective potential level and the output of the wave form generating means. Each of the transistors has a collector, base and emitter electrode and a collector-base junction.

Means are provided for selectively applying turn-on or driving signals to the base electrodes of the output transistor means, the signals being sufficient in magnitude to drive the output transistor into saturation. Means are shown wherein the circuit may be self-sensing in that the circuit may be responsive to the saturation of the transistor for enabling reverse biasing of the collector-base junction.

The reverse bias establishing means for the output transistors includes a transformer having primary and secondary windings, an isolating rectifier means, and means for connecting a reverse bias source to the primary winding of the transformer.

There are different embodiments of the reverse bias establishing means disclosed herein, each useful in a particular application. The reverse bias establishing means may be generically described as having secondary winding means of the transformer means connected in a circuit with the collector-base junction to enable current from secondary winding means to flow through the collector-base junction in a reverse bias direction. The isolating rectifier means may be generically described as connected in a circuit between the collector and base electrodes which includes at least one of the primary and secondary winding means of the transformer means to prevent current flow between the collector and base electrodes through the winding means in response to potential differences between the collector and base electrodes which establish a forward bias on the collector-base junction. The primary winding means of the transformer means may be generically described as connected to receive current from a reverse bias source, which may be derived from the turn-

on or driving source for the transistor, and which will induce a potential on the secondary winding means connected in circuit with the collector-base junction to cause current flow through the collector-base junction in a direction to reverse bias the collector-base junction and discharge the minority carriers from the junction if saturated to enable the transistor to turn "off" quickly.

Specifically, in the embodiments of the transformer-diode clamping means disclosed herein, the primary winding of the transformer is connected at one end via a biasing resistor to the base electrode of the output transistor, and at the other end via the isolating diode to the collector of the output transistor. Means may be provided for connecting one side of the reverse bias source to the junction of the bias resistance and the primary winding. The secondary winding is connected between the base electrode of the output transistor and through a circuit to the other side of the reverse bias source.

In one variation of the embodiments herein, a separate bias source is provided which is connected to the primary winding via switching means including second and third transistors. A feedback rectifier senses the driving current being supplied to the primary winding by sensing the voltage thereacross and feeds back a signal to the output electrode of the second transmitter to control the amount of driving current supplied to the secondary transformer.

In another variation of the transformer-diode circuits disclosed herein, the reverse bias source is derived from the driving current of the turn-on source for the output transistor, the voltage being developed across the bias resistor connecting the secondary winding and the base electrode of the output transistor providing the driving current for the primary winding.

Other objects, features, and advantages will become apparent from the following description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a diagrammatic layout of a system for supplying sustaining voltage for a gaseous discharge display/memory panel;

FIG. 2 is a schematic diagram of a circuit embodying the teachings of this invention for supplying sustaining voltage to the row conductors of the panel; and

FIG. 3 is a schematic diagram of a circuit illustrating further teachings of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The gaseous discharge display/memory device, as fully disclosed in the hereinbefore referenced Baker, et al. U.S. Pat. No. 3,499,167, and indicated generally at **20** in FIG. **1**, utilizes a pair of dielectric films separated by a thin layer of a gaseous discharge medium, the medium producing a copious supply of charges (ions and electrons) which are alternately collectable on the surfaces of the dielectric members at opposed or facing elemental or discrete areas defined by the conductor matrix on non-gas-contacting sides of the dielectric members, each dielectric member presenting a large open surface area and a plurality of pairs of elemental or discrete areas. While the electrically operative structural members such as the dielectric members and the conductor matrixes **13** and **14** are all relatively thin they are formed on and supported by rigid nonconductive support members **16** and **17**, respectively, as diagrammatically shown in FIG. **1**.

Typically, one or both of nonconductive support members **16** and **17** pass light produced by discharge in the elemental gas volumes. Usually, they are transparent glass members and these members essentially define the overall thickness and strength of the panel. For example, the thickness of gas layer **12**, as determined by a spacer is usually under 10 mils and typically about 4 to 6 mils, the dielectric layers (over the conductors at the elemental or discrete areas) are usually between 1 and 2 mils thick; and conductors **13** and **14** about 8,000 angstroms thick. However, support members **16** and **17** are much thicker (particularly in large panels) so as to provide as much ruggedness as may be desired to compensate for stresses in the panel **20**. Support members **16** and **17** also serve as heat sinks for heat generated by discharges and thus minimize the effect of temperature on operation of the device. If it is desired that only the memory function be utilized, then none of the members need be transparent to light.

Except for being nonconductive or good insulators the electrical properties of support members **16** and **17** are not critical. The main function of support members **16** and **17** is to provide mechanical support and strength for the entire panel, particularly with respect to pressure differential acting on the panel and thermal shock. As noted earlier, they should have thermal expansion characteristics substantially matching the thermal expansion characteristics of the dielectric layers. Ordinary ¼ inch commercial grade soda lime plate glasses have been used for this purpose. Other glasses such as low expansion glasses or transparent divitrified glasses can be used provided they can withstand processing and have expansion characteristics substantially matching expansion characteristics of the dielectric coatings. For given pressure differentials and thickness of plates, the stress and deflection of plates may be determined by following standard stress and strain formulas (see R. J. Roark, *Formulas for Stress and Strain*, McGraw-Hill, 1954).

The spacers may be made of the same glass material as dielectric films and may be an integral rib or ribs formed around the outside of the area in which the gas is to be confined and on one of the dielectric members, and fused to the other member to form a bakeable hermetic seal enclosing and confining the ionizable gas volume. However, a separate, outer final hermetic seal may be effected by a high strength devitrified glass sealant, if desired. Tabulation is provided for exhausting the space between the dielectric members and filling that space with the volume of ionizable gas. For large panels small bead-like solder glass spacers may be located between conductor intersections and fused to the dielectric member to aid in withstanding stress on the panel and maintain uniformity of thickness of gas volume.

Conductor arrays **13** and **14** may be formed on support members **16** and **17** by a number of well-known processes, such as photoetching, vacuum deposition, stencil screening, etc. In one embodiment, the center-to-center spacing of conductors in the respective arrays is about 17 mils. Transparent or semitransparent conductive material such as tin oxide, gold or aluminum can be used to form the conductor arrays and should have a resistance less than about 1000 ohms per linear inch of conductor line, usually less than about 50 ohms

per inch. Narrow opaque electrodes may alternately be used so that discharge light passes around the edges of the electrodes to the viewer. It is important to select a conductor material that is not attacked during processing by the dielectric material.

It will be appreciated that conductor arrays **13** and **14** may be wires or filaments of copper, gold, silver or aluminum or any other conductive metal or material. For example, 1 mil wire filaments are commercially available and may be used in the invention. However, formed in situ conductor arrays are preferred since they may be more easily and uniformly placed on and adhered to the support plates **16** and **17.**

The dielectric layer members are formed of an inorganic material and are preferably formed in situ as an adherent film or coating which is not chemically or physically effected during bake-out of the panel. One such material is a solder glass such as Kimble SG–68 manufactured by and commercially available from the assignee of the present invention.

This glass has thermal expansion characteristics substantially matching the thermal expansion characteristics of certain soda-lime glasses, and can be used as the dielectric layer when the support members **16** and **17** are soda-lime glass plates. The dielectric layers must be smooth and have a dielectric strength of about 1,000 volts per mil and be electrically homogeneous on a microscopic scale (e.g., no cracks, bubbles, crystals, dirt, surface films, etc.) In addition, the surfaces of the dielectric layers should be good photoemitters of electrons in a baked out condition. Alternatively, the dielectric layers may be overcoated with materials designed to produce good electron emission, as in U.S. Pat. No. 3,634,719, issued to Roger E. Ernsthausen. Of course, for an optical display at least one of the dielectric layers should pass light generated on discharge and be transparent or translucent and, preferably, both layers are optically transparent.

The preferred spacing between surfaces of the dielectric films is about 4 to 6 mils with conductor arrays **13** and **14** having center-to-center spacing of about 17 mils.

The ends of conductors **14–1 . . . 14–4** and support member **17** extend beyond the enclosed gas volume and are exposed for the purpose of making electrical connection to interface and addressing circuitry indicated generally at **19.** Likewise, the ends of conductors **13–1 . . . 13–4** on support member **16** extend beyond the enclosed gas volume and are exposed for the purpose of making electrical connection to interface and addressing circuitry **19.**

As described in detial in the Baker, et al. U.S. Pat. No. 3,499,167, the entire gas volume can be initially conditioned for subsequent operation at substantially uniform firing potentials by the use of internal or external radiation to supply free electrons throughout the gas medium.

Normal operation of a panel of the type described herein will be described with reference to FIG. **1.** Potentials having the wave forms **90** and **120** as shown in FIG. **1** are supplied from row and column sustainer circuit generators **80, 110** via row and volumn pulsing and addressing circuits **100, 130** to conductor arrays **14, 13** in response to control pulses from row and column sections **72, 74** respectively of the logic control circuit **70.** The resultant or composite potential wave form appearing across each cell is indicated at **140** in FIG. **4** as a periodic wave form of an alternating character. The wave form **140** is derived for the purpose of analysis of the operation of the panel by assuming that the wave forms **90** and **120** are spaced 180° apart or are oppositely phased within the cycles of the periodic composite wave form **140** and that the wave form **120** is subtracted from the wave form **90.**

In the examples set forth in FIG. **1,** the wave form **90** is a square wave with a duration of less than one-half of the cycle defined by the composite wave form **140** and with a magnitude of $+Vcc$. Thus, more than 180° of the cycle of the composite wave form **140** elapses between occurrences. The wave form **120** is a square wave with a duration of less than one-half of the cycle defined by the composite wave form **140,** and with a magnitude of $+Vcc$, since the sustainer **110** may be identical to the sustainer **80.** The logic inputs to the sustainers **80** and **110** are phased 180° apart with respect to the cycle of wave form **140.** Therefore, the positive wave **120** is produced when the positive wave **90** is not being produced. When the positive wave form **120** is subtracted from the positive wave form **90,** the wave form **120** appears to be negative in the composite wave form **140.**

The voltage **90** from sustainer **80** constitutes approximately one-half of the sustaining voltage necessary to operate the panel, the remaining one-half which is necessary being supplied by voltage **120** phased 180° as noted above with respect to the voltage **90.** Thus, one-half of the sustainer potential **140** is applied to each of the row conductors **14** and one-half of the sustainer potential **140** is applied to each of the column conductors **13.** The sustainer circuits **80** and **110** advantageously have a common ground so that the panel **10** floats with respect to ground.

Individual cells or discharge sites located by the crossing of selected conductors or conductor arrays **14, 13** are manipulated by adding unidirectional voltage pulses at the proper time to each of the sustaining voltages on the selected conductors, which, when combined, are sufficient to exceed the firing potential for the selected cells and to initiate a sequence of discharges, one for each half-cycle of the applied composite sustaining potential **140.** By also properly timing such unidirectional voltage pulses and applying them at a different portion in a cycle of the composite sustaining potential **140** to each of the sustaining voltages on the selected conductors, the sequence of discharges may be terminated. Thus, any individual discharge site may be manipulated "ON" or "OFF," by manipulation of the times of occurrences of the unidirectional voltage pulses.

The unidirectional voltage pulses are added to the sustainer voltages **90, 120** on the selected conductors by the row and column pulsing and addrssing circuits **100, 130** in response to logic signals from the logic control circuit **70** via leads **72–1** through **72–4** and **74–1** through **74–4,** respectively, to select the conductor pairs for the individual cells.

It will be noted that between the positive half-cycles **90** and the negative half-cycles **120** of the composite wave form **140** there are provided plateaus at the apparent zero voltage level indicating a brief time interval between the cessation of the generation of one-half cycle of the wave form **140** and the initiation of the other half-cycle of the wave form **140.** These plateaus may be provided to reduce interference between oper-

ation of various circuits for reasons that need not be detailed here.

However, the plateaus provide an opportunity to discuss what happens as the composite sustaining voltage **140** periodically alternates between the opposite polarities derived by subtracting the wave form **120** from the wave form **90.** As the wave form **140** goes from the negative level of the subtracted wave form **120** to the zero level, a cell "displacement" current flow occurs and causes a positive current spike. As the wave form **140** goes from the zero level to its positive level **90,** a second call "displacement" current flow occurs and causes a second positive current spike.

Similarly, as the wave form **140** goes from the positive level **90** to the zero level, a negative "displacement" current spike is produced. As the wave form **140** goes from zero to the negative level of the subtracted wave form **120** a second negative "displacement" current spike occurs.

If separation plateaus are not provided then the spikes would occur at substantially the same time and a single resultant larger "displacement" current spike would occur when the composite wave form **140** reverses polarity.

If the cell in question has been manipulated to an "ON" condition as hereinbefore described, then the cell will discharge when the difference between the wall voltage built up from a previous discharge and the sustainer potential exceeds the firing potential necessary to discharge the cell. There then occurs a cell "discharge" current flow.

It is desirable that the cell not see any appreciable voltage change in the sustainer wave form during the discharge period, since this may interfere with the transfer of wall charge during the discharge, so that subsequent discharges every half-cycle of the sustainer wave form will continue to occur in a manner to maintain the cell "ON" in the condition required.

Row and column sustainer circuits **80, 110** are advantageously constructed using power transistors as output devices. It is desirable to be able to turn the power transistors "ON" and "OFF" as quickly as possible so that the transition slope in the wave form controlled by the power transistors is as steep as possible. To turn a power transistor "On" quickly it is necessary to drive it with a comparatively large current pulse which will drive the transistor into deep saturation. The further the transistor is driven into saturation the smaller the internal resistance will be to the power output circuit it is controlling. If driven sufficiently far into saturation the "displacement" and "discharge" currents may flow freely through the transistor and there will be very little voltage drop across the transistor during the time the cell is discharging. Therefore, the voltage drop across the transistor will be very small during the discharge cycle of the cell, will make very little change as a subtraction to the composite sustainer wave form, and will not appreciably effect the transfer of wall charges during the discharge cycle of a cell.

Difficulties have been encountered, however, in that when the transistor is driven into deep saturation to reduce the wave form alteration resulting from "displacement" and "discharge" current flow to and below a desired level, it takes a longer time to turn the transistor "OFF." This decreases the slope of the wave form being produced and may delay or slow a voltage transition to a point which will interfere with proper panel operation. A power loss can be associated with slow turn-off. In accordance with this invention there is provided circuitry means for quickly turning-off power transistors such that there is minimum excess heating of components.

A diode clamping network has been used in the past to overcome the above-discussed problem. In one embodiment a single diode is connected to conduct in a forward direction from a clamping bias junction to the collector electrode of a power transistor connected to a voltage being controlled. Two diodes in series are connected to conduct in a forward direction from the clamping bias junction to the base electrode of the transistor. The emitter electrode may be connected through a resistor. The emitter electrode may be connected through a resistor to the base electrode.

In operation, the just discussed circuit received a turn-on pulse having a large magnitude to drive the transistor toward deep saturation, changing the configuration of the wave form being controlled and permitting the free flow therethrough of the "displacement" current and "discharge" current, if any, from the panel being controlled. Since the transistor is going toward deep saturation the resistance offered thereby to the "discharge" current results only in a voltage change in the composite sustaining wave form which is below a level which would significantly interfere with the transfer on the wall charges in any cells in the panel which are "ON."

If, in the embodiment of the diode clamping circuit being discussed, the collector electrode is connected to an output voltage source being controlled, when the flow of "displacement" and "discharge" current ceases there is no load on the transistor and if the transistor is still being driven hard, then deep saturation will occur because the collector voltage is lower than the base voltage.

To keep the transistor out of deep saturation the collector voltage is kept just above the base voltage by the diode clamping circuit. The diode between the collector and the clamping bias junction is required to isolate the voltage wave form being controlled from the base of the transistor. If the transistor requires a V voltage drop across the base-emitter junction (and the resistor connecting the base and emitter electrodes) to turn it "on" then the isolating diode means is selected to have a voltage drop in the forward direction in response to current flow through the clamping bias junction which is less than the voltage drop in the forward direction of the serially connected base diode means plus the voltage drop across the base-emitter resistor in response to current flow through the clamping bias junction.

Thus, if the isolating diode and any resistance associated therewith has a voltage drop thereacross which is less than the clamping bias voltage necessary at the clamping bias junction to keep the transistor "on," then the collector voltage is equal to the clamping bias voltage minus the isolating diode voltage drop and is therefore larger than the base voltage. The transistor is kept out of saturation and turns off when the drive pulse is removed and stops conducting relatively quickly.

The clamping bias voltage is preferably applied to the clamping bias junction at the same time that the drive pulse is removed from the base of the transistor.

While the just described diode clamping circuit has worked well in some applications, it is desirable to be

able to turn the power transistor "off" even more quickly in certain applications. It is also desirable to be able to use power transistors which have longer storage times (the length of time a transistor stays in saturation without a driving potential applied) since the longer storage time transistors are less expensive. It is further desirable to be able to saturate the power transistor as much as possible, without interfering with the ability to turn the transistor "off" quickly, to reduce the internal resistance even further than reduced with the diode clamping circuit, so that the voltage drop across the transistor during flow of cell discharge current is as low as possible.

Referring now to FIG. 2 there is illustrated in more detail a schematic diagram of a circuit which may be used as the sustainer wave form generator **80** to produce the wave form **90** as shown in FIG. **1.** As noted hereinbefore, an identical circuit may be used to produce the wave form **120.**

The upper half of the circuits in FIGS. **2** and **3** is not illustrated in detail since one of the embodiments shown herein, or one of my other embodiments of a transformer-diode clamping circuit disclosed in my concurrently filed and copending applications illustrating improvements enabling use of the teachings of this invention in other systems, may be used. For the purpose of avoiding obtaining a copy of the above-referenced applications, in order to understand the operation of this invention, there is included hereinafter a description of the operation of an embodiment which is suitable for use as the upper switching circuit here.

In operation of the upper switching section, a short duration pull-up turn-on pulse is applied to the base of a first switching transistor from the logic control **70** via the lead **74** UN (see FIG. **1**) to turn a first switching transistor "on," thereby also turning a second switching transistor "on" and permitting current flow from a turn-on source through the primary winding of an isolating transformer. A drive pulse is induced on the secondary winding of the isolating transformer causing current flow to turn an output power transistor of the upper switching section "on." The driving pulse induced in the secondary of the isolating transformer is of sufficient magnitude to drive the output power transistor very hard to bring the output terminal **92** to the voltage level +V*cc* as indicated in FIG. **2,** and also leaves the output power transistor of the upper switching section saturated.

Any time after the panel displacement and discharge current flow is, for the most part, over a pull-up turn-off pulse is applied to the base electrode of a third switching transistor via the lead **7** 4UF from the logic circuit **70** (FIG. **1**). This pulse causes the third switching transistor to conduct, which, in turn, causes a fourth switching transistor to conduct and provide a current flow in the primary winding of a transformer of a transformer-diode clamping circuit. Current flow is induced in the secondary winding of the clamping circuit transformer causing a potential to be provided between the collector and the base of the output switching transistor which is higher at the collector than at the base. The minority carriers of the saturated collector-base junction of the output power transistor of the upper switching section are discharged through a diode connected in series with the secondary winding of the clamping transformer. The transformer-diode circuit just described turns the output power transistor "off" very quickly allowing negative panel-address pulses to also be applied quickly to the sustainer wave form **90,** which is a requirement in some addressing circuit schemes or techniques.

The circuit illustrated in FIG. **2** will now be described. When the voltage is to be dropped at the output terminal **92** from the level of the potential +V*cc* to ground or zero as illustrated in FIG. **1,** a short duration pull-down turn-on pulse is applied to the terminal **86**T connected to the base of the transistor **Q1** by suitable means via the lead **7** 4DN from the logic circuit **70.** This turns the transistor Q1 "on" allowing conduction of driving current from a turn-on source +V*dc*2 through its emitter-collector circuit thereby also turning the output transistor Q2 "on." The driving current is sufficiently large to turn the output power transistor Q2 "on" very quickly, deeply saturating the transistor. This quickly reduces the voltage at the terminal **92** to ground level providing the zero output from the sustainer circuit **80** as noted in FIG. **1.**

Any time after panel displacement and discharge current flow through the transistor Q2 is, for the most part, over a pull-down-turn-off pulse may be applied to terminal **88**T connected to the base of the transistor Q3 via the lead **7** 4DF from the logic circuit **70.** The transistor Q3 conducts causing the transistor Q4 to conduct and allow current flow from one side of the reverse bias source +V*dc*1 through the primary winding T1P of the clamping circuit transformer T1 through the isolating rectifier D1 and the collector-emitter circuit of the now saturated transistor Q2. A potential is then induced on and current flow occurs from the secondary winding T1S of the clamping circuit transformer T1 which is connected between the base electrode of the power transistor Q2 and the other side of the reverse bias source. The developed potential on winding T1S also causes current to flow from the primary winding T1P through the isolating diode D1, the saturated collector-base junction of the power transistor Q2, and to the secondary winding T1S of the clamping circuit transformer T1, discharging the minority carriers from the saturated collector-base junction and turning off the power transistor W2 very quickly.

It should be noted that there will be no significant current flow through the secondary winding T1S of the clamping circuit transformer T1 from the driving pulses for the transistor Q2 and no significant current flow through the secondary winding of the transformer T1, if there is a potential on the collector of the transistor Q2 which reverse biases the diodes D1. Such reverse biasing of D1 prevents current flow in the promary winding T1P, reflecting a high impedance to the secondary T1S and preventing any substantial current flow through the secondary from the driving pulses for the output transistor.

The operation of the circuit of FIG. **2** has been described to this point as if the feedback diode D*f* was not connected in the circuit between the primary winding of the transformer T1 and the output emitter of the transistor Q3.

Assume now that the diode D*f* is in the circuit as shown. The operation of the circuit is still the same until the collector-base junction of the transistor Q2 has recovered from saturation and becomes a high impedance to the passage of current from the primary

winding T1P of the transformer T1, indicating that the transistor Q2 is out of saturation.

This higher impedance to current flow from the primary winding will cause the voltage across the primary to increase. A bias current will then flow from the junction of the output collector of Q3 and one end of the primary winding through the resistor Rb which is sufficient to maintain the loading of the transistor Q2 near the saturation level.

The increased voltage across the primary winding of the transformer T1 will also forward bias the feedback diode Df and provide a negative feedback to the output emitter of the transistor Q3. The negative feedback will control the action of the transistor Q4 causing it to conduct only enough to maintain a voltage across the primary winding that will match the input to the transistor Q3, if the input is less than the reverse bias source +V*dc*1. (Such a smaller input signal to Q3 is desirable, since only low voltage level logic circuits need be used as inputs with the inherent advantages attendant therewith.) The circuit utilizing the feedback diode D*f* and bias resistor R*b* thus provides automatic control of drive current to match the load presented by the collector-base junction of the transistor Q2.

If the bias resistor R*b* is omitted from the circuit and the primary winding is not connected to the base of transistor Q2 then the circuit, including the components Q3, Q4, T1P and T1S, serves only to turn the transistor Q2 "off." However, the diode D*f* would still function in the same manner to control the amount of driving current supplied to the primary winding of the transformer T1.

Referring now to FIG. 3, there is illustrated another embodiment of the teachings of this invention which is particularly useful in connecting a load device to ground or zero potential.

When the voltage is to be dropped at the output terminal 92 in FIG. 3 from the level of the potential +Vcc to ground or zero, a short duration pull-down turn-on pulse is applied to the terminal 86T connected to the base of the transistor Q1 by suitable means from the lead 7 4DN from the logic circuit 70. This turns the transistor Q1 "on" allowing conduction through its emitter-collector circuit from the turn-on source +V*dc*2 and application of a driving pulse to the base-emitter circuit of the power transistor Q2 turning it "on" very quickly and deeply saturating the transistor. This reduces the voltage at the terminal 92 to ground level providing the zero output from the sustainer circuit 80.

When the transistor Q2 is deeply saturated and the panel displacement and discharge current flow through the transistor Q2 is over, for the most part, there will be very little voltage drop across the collector-emitter circuit of the transistor Q2, both because the internal resistance has been reduced by the hard driving pulse, and because there is little or no current flow, since terminal 92 is now effectively connected to ground, through the internal resistance to cause a voltage drop. Therefore, when the voltage drop across Q2 falls below the value necessary to reverse bias the diode D1, then the diode D1 becomes forward biased and permits current flow, from the voltage drop across R*b* derived from the drive current, through the primary winding T1P of the clamping circuit transformer T1.

Once current starts to flow through the primary winding T1P of the transformer T1, the voltage induced on the secondary T1S winding of the transformer T1 causes current flow across the saturated collector-base junction of the power transistor Q2 in the reverse direction, thereby discharging the minority carriers from the saturated collector-base junction, enabling the power transistor Q2 to turn "off" very quickly when the drive current is removed from the base thereof.

As is evident by examining FIG. 3, only one source is now required since the reverse bias source may be derived from the turn-on source, or vice versa. Therefore an extra source of supply and/or an extra set of connections to an additional source are not required.

The isolating rectifier D1 is preferably interposed between the primary winding T1P and the collector electrode of Q2, rather than on the other side of the primary winding so as to prevent the charging of inter-electrode capacitance between the primary and secondary (T1P and T1S) of the transformer during output transitions.

It should be noted that logic leads 72DF and 74DF from the logic circuit 70 to the sustainer circuits 80, 110 are not needed for the embodiment illustrated in FIG. 3. There is no need for a pull-down turn-off logic pulse when using the present invention, because of the automatic sensing and acting capabilities of the novel circuit of this invention This circuit thus saves components and required timing logic.

It should also be noted that a mirror image type modification of the circuits illustrated in FIGS. 2 and 3 may be constructed to produce negative pulse outputs 90 and 120, rather than the positive pulses as shown.

It should also be noted that combinations of positive and negative sustainer wave form generator circuits may be used in certain applications.

There have thus been described and disclosed transformer-diode clamping circuits which may be used to turn output power transistors "off" after a very heavy turn-on drive pulse, enabling the power transistors to be turned "off" in a fraction of the normal storage time for such devices. This enables a sustainer performance to meet and match the very fast switching speed and high current requirements of newly developed display/memory panels, as well as prior art panels. The very fast, high voltage, high current switching of the apparatus disclosed herein far outperforms the present prior art devices. The use of the transformer-diode clamps described herein also permits greater flexibility in unique logic address requirements and permits turning transistor Q2 "off" more quickly than other transformer-diode clamping circuits, since the base of the output transistor is directly forced to be negative (in an N-P-N type). The present invention may also be used to take advantage of gaseous mediums which are presently being tested and which exhibit much faster discharge times than past mediums.

What is claimed is:

1. In a system for supplying operating potential to a load device wherein at least two transversely oriented conductors are dielectrically isolated from a gas discharge medium between said conductors, comprising

a. voltage wave form generating means having an output means adapted to be connected to a transverse conductor;

b. said wave form generating means including at least two sections, a first of said sections being operative to connect a first potential level to said output

means while a second of said sections is operative to connect a second potential level to said output means;

c. each of said output sections including at least one output transistor means operating as a switching means between its respective potential level and said output means of said wave form generating means, each said transistor means having collector, base and emitter electrodes and collector-base junction;

d. means for selectively applying turn-on signals to the base electrodes of said output transistor means, said signals being sufficient in magnitude to drive each of said output transistor means into saturation;

e. means for selectively establishing current flow through said collector-base junction of each of said output transistor means to reverse bias said collector-base junction to enable each of said output transistors to turn off quickly;

f. at least one of said reverse bias establishing means including a transformer having primary and secondary windings, isolating rectifier means, and means for connecting one side of a reverse bias source to said primary winding;

g. means for connecting said secondary winding between the base electrode of said output transistor and the other side of said reverse bias source; and

h. means for sensing the voltage across said primary winding to supply biasing current to the base electrode of said output transistor.

2. A system as defined in claim **1** in which said means for connecting a reverse bias source to said primary includes switching means, interposed between the reverse bias source and the primary, which is responsive to turn-off signal to connect said reverse bias source to said primary winding.

3. A system as defined in claim **2** in which said switching means includes

a. second transistor means responsive to turn-off signal to supply driving current to said primary means, and

b. feedback means responsive to the driving current required by said primary for regulating the output of said second transistor means.

4. A system as defined in claim **3** in which said means for sensing said primary winding voltage and supplying current to the base electrode of said first-mentioned transistor means is also responsive to said feedback means, thereby enabling said feedback means to control the driving of said first-mentioned transistor means to maintain the first-mentioned transistor means near saturation as current flow through the collector-emitter circuit thereof varies.

5. A system as defined in claim **1** in which

a. a first switching means is interposed between a turn-on source and said base electrode and is responsive to a turn-on signal to connect said turn-on source to said base electrode, and

b. a second switching means is interposed between said reverse bias source and said primary winding and is responsive to a turn-off signal to connect said reverse bias source to said primary winding.

6. Control apparatus, comprising

a. transistor means having collector, base, and emitter electrodes with collector-base and base-emitter junctions between said electrodes;

b. means for connecting a turn-on source to provide a driving signal to said base electrode having a magnitude sufficient to turn said transistor on and drive said transistor into a saturated condition; and

c. means for selectively establishing current flow through said collector-base junction to reverse bias said junction to enable said transistor to turn off quickly;

d. said reverse bias establishing means including a transformer having primary and secondary windings, an isolating rectifier means, and means for connecting one side of a reverse bias source to said primary winding;

e. said primary winding being connected between said collector and base electrodes of said one output transistor means via said isolating rectifier means, which is connected to prevent current flow in said secondary winding from said collector electrode to said base electrode, so that current flow in said primary winding will induce a voltage on said secondary winding which will reverse bias said collector-base junction;

f. said secondary winding being connected between said base electrode and the other side of said reverse bias source means;

g. and means for connecting the voltage developed across said primary winding to provide a bias current to the base electrode of said transistor means.

7. Apparatus as defined in claim **6** in which said reverse bias source for said primary winding is derived from said driving current for said transistor means.

8. Apparatus as defined in claim **6** in which said means for connecting a reverse bias source to said primary winding includes second and third transistors, said second transistor being responsive to a turn-off signal to enable said third transistor to connect a reverse bias source to supply driving current to said primary winding.

9. Apparatus as defined in claim **8** which further includes feedback means responsive to the driving current supplied to said primary winding for regulating the output of said second transistor means.

10. Apparatus as defined in claim **9** in which the end of said primary winding receiving driving current from said reverse bias source is also connected to said base electrode of said first-mentioned transistor means by said bias current connecting means, thereby enabling said feedback means to maintain said first-mentioned transistor means near saturation as the current flow through the collector-emitter circuit varies and thus also varies the current flow through said secondary winding connected to the collector electrode of said first-mentioned transistor means.

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