LIMITING STRAIN RELAXATION IN III-NITRIDE HETEROSTRUCTURES BY SUBSTRATE AND EPITAXIAL LAYER PATTERNING

Abstract: A method of fabricating a substrate for a semipolar III-nitride device, comprising patterning and forming one or more mesas on a surface of a semipolar III-nitride substrate or epilayer, thereby forming a patterned surface of the semipolar III-nitride substrate or epilayer including each of the mesas with a dimension / along a direction of a threading dislocation glide, wherein the threading dislocation glide results from a III-nitride layer deposited heteroeptaxially and coherently on a non-patterned surface of the substrate or epilayer.
— of inventorship (Rule 4.17(iv))

Published:
— with international search report (Art. 21(3))
— before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments (Rule 48.2(h))
LIMITING STRAIN RELAXATION IN III-NITRIDE HETEROSTRUCTURES BY SUBSTRATE AND EPITAXIAL LAYER PATTERNING

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit under 35 U.S.C. Section 119(e) of co-pending and commonly-assigned U.S. Provisional Application Serial No. 61/406,876 filed on October 26, 2010, by James S. Speck, Anurag Tyagi, Steven P. DenBaars, and Shuji Nakamura, entitled "LIMITING STRAIN RELAXATION IN III-NITRIDE HETEROSTRUCTURES BY SUBSTRATE AND EPITAXIAL LAYER PATTERNING," attorney's docket number 30794.387-US-P1 (2010-804), which application is incorporated by reference herein.


BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates to a method to limit strain relaxation of hetero-epitaxial III-nitride layers grown on III-nitride substrate/epilayers, by patterning said substrate/epilayer.
2. Description of the Related Art.

(Note: This application references a number of different publications as indicated throughout the specification by one or more reference numbers within brackets, e.g., [x]. A list of these different publications ordered according to these reference numbers can be found below in the section entitled "References." Each of these publications is incorporated by reference herein.)

In spite of numerous advantages offered by growth of optoelectronic devices on nonpolar/semipolar III-nitride substrates, misfit dislocation (MD) formation at misfitting heterointerfaces [1, 2] can make it difficult for device manufacturers to fully realize the expected inherent advantages. For semipolar III-nitride based devices, stress relaxation via glide of pre-existing threading dislocations can limit the composition/thickness of strained heteroepitaxial films that can be grown coherently on underlying substrates/films. This can, in turn, limit the device design space e.g. the range of emission wavelength for Light Emitting Diodes (LEDs) / Laser Diodes (LDs).

Additionally, performance for LDs can be affected due to poor optical waveguiding provided by thinner/lower composition waveguiding (typically InGaN) and cladding layers (typically AlGaN). The present invention provides a way to limit the stress-relaxation by the above mentioned glide process, and thus reduces the constraints on device design space, allowing employment of thicker/higher composition strained III-nitride alloy epitaxial layers. The proposed devices can be used as an optical source for various commercial, industrial, or scientific applications. These nonpolar or semipolar nitride LEDs and diode lasers can be expected to find utility in the same applications as c-plane nitride LEDs and diode lasers. These applications include solid-state projection displays, high resolution printers, high density optical data storage systems, next generation DVD players, high efficiency solid-state lighting, optical sensing applications, and medical applications.
SUMMARY OF THE INVENTION

The disclosed invention provides a method to limit strain relaxation of hetero-
epitaxial III-nitride layers grown on III-nitride substrate/epilayers, by patterning said
substrate/epilayer. The present invention further includes growth and fabrication of
devices on patterned III-nitride substrates.

To overcome the limitations in the prior art described above, and to overcome
other limitations that will become apparent upon reading and understanding the
present specification, the present invention describes a semipolar or non-polar III-
nitride device, comprising a semipolar or nonpolar III-nitride substrate or epilayer
having a threading dislocation density of $10^6 \text{cm}^{-2}$ or more; and a heterostructure,
comprising semipolar or nonpolar III-nitride device layers, grown on the substrate or
epilayer, wherein the heterostructure has a misfit dislocation density of $10^4 \text{cm}^{-2}$ or
less.

The semipolar or nonpolar III-nitride substrate or epilayer can comprise one
or more mesas with a dimension $l$ along a direction of a threading dislocation glide,
thereby forming a patterned surface of the semipolar or nonpolar III-nitride substrate
or epilayer, wherein the heterostructure is grown heteroepitaxially and coherently on
the patterned surface.

The dimension $l$ can be between 10 micrometers and 1 millimeter.

At least one of the heterostructure’s layers can have a different III-nitride
composition from the semipolar or nonpolar III-nitride substrate or the epilayer.

A heterointerface between the heterostructure and the patterned surface can
include a misfit dislocation density that is reduced by a factor of at least 10, or at least
1000, as compared to a misfit dislocation density resulting from a semipolar or
nonpolar III-nitride heterostructure grown heteroepitaxially and coherently on a non-
patterned surface of the semipolar or nonpolar III-nitride substrate or epilayer.

One or more of the semipolar or nonpolar III-nitride device layers can be
thicker, and have a higher alloy composition, as compared to (1) semi-polar or
nonpolar III-nitride device layers that are grown on a non-patterned surface of a semi-
polar or nonpolar III-nitride substrate or epilayer, or as compared to (2) semi-polar or nonpolar III-nitride device layers that are grown on a different patterned surface of the semipolar or nonpolar III-nitride substrate.

The device can comprise a device structure for a non-polar or semi-polar III-nitride Light Emitting Diode (LED) or Laser Diode (LD), wherein the device structure includes the heterostructure and one or more active layers emitting light having a peak intensity at one or more wavelengths corresponding to green wavelengths or longer, or a peak intensity at a wavelength of 500 nm or longer.

The active layers can comprise III-nitride Indium containing layers that are sufficiently thick, and have sufficiently high Indium composition, such that the LED or LD emits the light having the wavelengths.

The device structure can comprise waveguiding and/or cladding layers, comprising III-nitride layers that are sufficiently thick, and having a composition, to function as the waveguiding and/or cladding layers for the LD or LED.

The active layers and the waveguiding layers can comprise one or more InGaN quantum wells with GaN barrier layers, and the cladding layers can comprise one or more periods of alternating AlGaN and GaN layers.

One or more of the semi-polar or non-polar III-nitride device layers can have a thickness greater than a (e.g., Matthews Blakeslee) critical thickness for one or more semi-polar or non-polar III-nitride layers deposited on a non-patterned surface of a semipolar or non-polar III-nitride substrate or epilayer.

The present invention further discloses a method of fabricating a substrate for a semipolar or non-polar III-nitride device, comprising patterning and forming one or more mesas on a surface of a semipolar or non-polar III-nitride substrate or epilayer, thereby forming a patterned surface of the semipolar III-nitride substrate or epilayer, wherein each of the mesas has a dimension / along a direction of a threading dislocation glide, wherein the threading dislocation glide results from a III-nitride layer deposited heteroepitaxially and coherently on a non-patterned surface of a semipolar or non-polar III-nitride substrate or epilayer.
A pre-existing threading dislocation density of the III-nitride substrate can be at least $10^5 \text{ cm}^2$ or between $10^5$ and $10^7 \text{ cm}^2$.

**BRIEF DESCRIPTION OF THE DRAWINGS**

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

Fig. 1 is a perspective view schematic illustrating MD formation by TD glide for the exemplary case of a strained heteroepitaxial (Al,In)GaN layer grown on a semipolar (11-22) GaN substrate, taken from [1].

Fig. 2 illustrates a top view (a) and side view (b) of mesas patterned on a substrate or epilayers, according to one or more embodiments of the present invention.

Fig. 3 is a flowchart illustrating a method of fabricating a device, according to one or more embodiments of the present invention.

Fig. 4 is a cross-sectional schematic of device heterostructure layers on a III-nitride substrate or epilayer, according to one or more embodiments of the present invention.

Fig. 5 is a cross-sectional schematic of device heterostructure layers on a non-polar III-nitride substrate or epilayer, according to one or more embodiments of the present invention.

Fig. 6 is a cross-sectional schematic of a device structure grown on the patterned substrate, according to one or more embodiments of the present invention.

**DETAILED DESCRIPTION OF THE INVENTION**

In the following description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.
Overview

State of the art commercial III-nitride devices are based on coherent growth of hetero-epitaxial films on a III-nitride substrate. As mentioned above, this limits the thickness/composition of strained III-nitride films and limits the device design space. Using higher composition strained epilayers leads to the formation of MDs at heterointerfaces, which can degrade device performance [1]. The current invention provides a work-around to the MD formation process by limiting the glide length of pre-existing Threading Dislocations (TDs).

Nomenclature

GaN and its ternary and quaternary compounds incorporating aluminum and indium (AlGaN, InGaN, AlInGaN) are commonly referred to using the terms (Al, Ga, In)N, III-nitride, Group III-nitride, nitride, Al(\(x-y\))GaN where \(0 < x < 1\) and \(0 < y < 1\), or AlInGaN, as used herein. All these terms are intended to be equivalent and broadly construed to include respective nitrides of the single species, Al, Ga, and In, as well as binary, ternary and quaternary compositions of such Group III metal species. Accordingly, these terms comprehend the compounds AIN, GaN, and InN, as well as the ternary compounds AlGaN, GalnN, and AlInN, and the quaternary compound AlGaInN, as species included in such nomenclature. When two or more of the (Ga, Al, In) component species are present, all possible compositions, including stoichiometric proportions as well as "off-stoichiometric" proportions (with respect to the relative mole fractions present of each of the (Ga, Al, In) component species that are present in the composition), can be employed within the broad scope of the invention. Accordingly, it will be appreciated that the discussion of the invention hereinafter in primary reference to GaN materials is applicable to the formation of various other (Al, Ga, In)N material species. Further, (Al, Ga, In)N materials within the scope of the invention may further include minor quantities of dopants and/or other impurity or inclusional materials. Boron (B) may also be included.
The term "Al$_x$Gai$_{1-x}$N-cladding-free" refers to the absence of waveguide cladding layers containing any mole fraction of Al, such as Al$_x$Gai$_{1-x}$/GaN superlattices, bulk Al$_x$Gai$_{1-x}$N, or A1N. Other layers not used for optical guiding may contain some quantity of Al (e.g., less than 10 % Al content). For example, an Al$_x$Gai$_{1-x}$N electron blocking layer may be present.

One approach to eliminating the spontaneous and piezoelectric polarization effects in GaN or III-nitride based optoelectronic devices is to grow the III-nitride devices on nonpolar planes of the crystal. Such planes contain equal numbers of Ga (or group III atoms) and N atoms and are charge-neutral. Furthermore, subsequent nonpolar layers are equivalent to one another so the bulk crystal will not be polarized along the growth direction. Two such families of symmetry-equivalent nonpolar planes in GaN are the \{11-20\} family, known collectively as a-planes, and the \{1-100\} family, known collectively as m-planes. Thus, nonpolar III-nitride is grown along a direction perpendicular to the \(0001\) c-axis of the III-nitride crystal.

Another approach to reducing polarization effects in (Ga,Al,In,B)N devices is to grow the devices on semi-polar planes of the crystal. The term "semi-polar plane" (also referred to as "semipolar plane") can be used to refer to any plane that cannot be classified as c-plane, a-plane, or m-plane. In crystallographic terms, a semi-polar plane may include any plane that has at least two nonzero \(h, i,\) or \(k\) Miller indices and a nonzero \(1M\) Miller index.

Technical Description

For the case of semipolar III-nitride heteroepitaxy, significant stress relaxation can be realized by the glide of pre-existing TDs. Fig. 1 is a perspective view schematic illustrating MD formation by TD glide for the exemplary case of a strained heteroepitaxial (Al,In)GaN layer 100 grown on a semipolar \(\{11-22\}\) GaN substrate 102. The MD line direction corresponds to the intersection of the glide plane 104 (which is \(0001\) for basal plane slip) and the growth plane 106, which for Fig. 1 corresponds to the in-plane m-axis \(1-100\). Also shown is the heterointerface 108.
between the (Al,In)GaN layer 100 and the GaN substrate 102, the non-patterned surface 110 of the substrate 102 upon which layer 100 is deposited, and the (11-22) and (1-1-23) directions.

As a simple estimate, the maximum MD density, $\rho_{\text{MD}}^{\text{max}}$, is given by

$$P_{\text{MD}}^{\text{max}} \approx \frac{1}{2} P_{\text{TD}} / \text{Equation (1)}$$

where $/ \text{is the glide length of the TD and } P_{\text{TD}}$ is the pre-existing TD density.

In the absence of any crossing MDs, or other obstacles to glide, $/ \text{should correspond to the wafer dimensions in the projected glide direction, which for basal slip should correspond to the intersection of the (0001) c-plane 104 and the growth plane 106.}$

Typically, the semipolar GaN substrates 102 are cross-cut from c-plane GaN boules, and the typical wafer dimensions are on the order of 1 cm x 1 cm. Thus, $\rho_{\text{MD}}^{\text{max}} \sim 10^6 \text{ cm}^{-2} \times 1 \text{ cm} = 10^6 \text{ cm}^{-1}$, or the minimum MD spacing is on the order of 100 Angstroms (Å) which corresponds to plastic relaxation of the order of 2% (the relieved misfit strain accompanying plastic relaxation is given by $f_{\text{nu}} f_{\text{nu}} = b_i d_{\text{g}2} \parallel \rho_{\text{MD}}^{\text{MAX}}$, where $b_i, d_{\text{g}2}$.

$\parallel$ is the edge component of the MD Burgers vector that is parallel to the heterointerface 108).

The present invention notes that the MD density, and consequently stress relaxation, has a direct dependence on the run length of the TDs. This enables the present invention to limit stress relaxation by limiting the run/glide length of the TDs.

An expedient way to accomplish this is to pattern "mesas" on the substrate/epilayers. This is illustrated in Figs. 2(a) and 2(b) (again for the exemplary case of (11-22)), wherein mesas 200a, 200b, and 200c are patterned into the surface of the (11-22) GaN substrate 202, to form a patterned surface 204 of the substrate 202. In Fig. 2(a)-(b), $l_1$, $l_2$, and $l_3$ are the mesa dimensions parallel to the TD glide direction (m-axis [1-100], same as MD line direction) for each of the 3 mesas 200a, 200b, and 200c depicted in Figs. 2(a) and 2(b). Also shown are the height $h$ (~0.5 micrometers) of the mesas 200a-200c, a surface area of the substrate 202 having a length $L$ (~ 1 centimeter)
along the direction of the TD glide direction (parallel (||) to the [1-100] m-axis direction which is also shown), and the [-1-123] direction (parallel to the projection of the c-axis).

By using mesa dimensions of \(-10 \ \mu \text{m} \) to \(-1 \ \text{mm} \) in the TD glide direction, the TD glide length and MD density can be reduced by a factor of \(-10^3\) to \(-10\), and consequently, only very little misfit relief can be achieved by TD glide. This enables the present invention to grow strained epitaxial layers with higher alloy composition and/or greater thickness without generating a high density of MDs at the misfitting heterointerfaces (MD density due to pre-existing TDs would be limited to \(\frac{1}{2} \rho_{\text{MD}}^0 l\)), where \(l\) corresponds to the mesa dimension parallel to the glide direction. As mentioned previously, this enables a wider and more flexible design space, which translates into improved performance for devices.

Fig. 3 is a flow chart outlining the steps involved in one embodiment of the present invention.

The present invention starts with a semipolar III-nitride substrate or epilayer (grown on a substrate), as illustrated in Block 300. The pre-existing TD density for the substrate/epilayer would typically be in the \(10^5-10^7 \ \text{cm}^{-2}\) range.

Block 302 represents mesa patterning, wherein the substrate/epilayer is then covered with a suitable mask (either photoresist or dielectric) having the desired mesa pattern, using conventional lithographic techniques. Although the mesa/mask pattern can take an arbitrary shape, the important dimension is the size of the pattern parallel to the glide direction \((l\) in equation 1) since that determines the maximum MD density (due to pre-existing TDs). The present invention is not limited to patterning using photoresist/dielectric masks (other methods may also be used).

Block 304 represents mesa etching, wherein the substrate/epilayer is then etched to a suitable depth (>50 nm, e.g., 0.1-10 \(\mu \text{m}\) are typical etch depths) to form mesa structures, and the mask is subsequently removed (Block 306). The etching can include, but is not limited to, wet or dry etching.
The mesa sidewalls and the field may optionally be covered with a dielectric, and the exposed substrate/epilayer surface may then be subjected to an ex situ or in situ cleaning or preparation, as represented in Block 308, prior to epitaxial re-growth of the device epitaxial structure (Block 310).

Fig. 4 illustrates a III-nitride heterostructure 400 on a substrate or epilayer 402, wherein \( p_{\text{MD}}^{\text{max}} \approx p_{\text{MD}} l \) and strain relaxation \( (\varepsilon_{\text{rel}}) \) in the heterostructure layers is \( \varepsilon_{\text{rel}}^{\text{max}} = p_{\text{MD}} \cdot \text{bedgell} \), and the c-projection direction and the semipolar a- or m- direction are also shown.

Fig. 5 illustrates limiting strain relaxation in non-polar III-nitride heterostructures (comprising heterostructure layers 500) by substrate patterning of a non-polar substrate 502 or epilayer. Also shown are MDs, the c-direction 504 of the III-nitride, the growth direction 506 of the heterostructure layers 500, and the m- or a- direction 508 of the III-nitride. An \( l = 1 \) cm wide wafer or substrate 502 with \( 10^6 \) cm\(^{-2} \) TDs, leads to \( 10^6 \) MDs/cm\(^2\) using the relation \( p_{\text{MD}}^{\text{max}} \approx p_{\text{MD}} l \). If \( l \) is reduced to 100 micrometers or \( 10^{-2} \) cm, the MD density can be reduced to \( 10^4 \) MDs/cm\(^2\).

**Device Embodiments**

Fig. 1(a)-(b), Fig. 2(a)-(b), Fig. 5, and Fig. 6, illustrate various device embodiments.

Fig. 5 illustrates a semipolar or nonpolar III-nitride substrate 502 or epilayer having a threading dislocation density of \( 10^6 \) cm\(^{-2} \) or more; and one or more semipolar or nonpolar III-nitride layers 500a, 500b, such as device layers (or a heterostructure 500, comprising semipolar or nonpolar III-nitride layers or device layers 500a, 500b), grown (e.g., coherently and/or heteroepitaxially) on the semipolar or nonpolar III-nitride substrate 502 or epilayer, wherein the heterostructure 500 or layers 500a, 500b have a misfit dislocation density of \( 10^4 \) cm\(^{-2} \) or less.

The substrate 502, 202 can be bulk III-nitride or a film of III-nitride. The substrate can comprise an initial semi-polar III-nitride (e.g., template) layer or
epilayer 502, 202 grown on a substrate (e.g., heteroepitaxially on a foreign substrate, such as sapphire, spinel, or silicon carbide).

Fig. 2(a), Fig. 2(b), and Fig. 5 illustrate the semipolar or nonpolar III-nitride substrate 202, 502 or epilayer can comprise one or more mesas 200a with a dimension / along a direction of a threading dislocation glide, thereby forming a patterned surface 204 of the semipolar or nonpolar III-nitride substrate or epilayer 502, 202 (the surface 204 of the substrate comprises the mesas 200a-c). The heterostructure 500 or layers 500a-b are grown heteroepitaxially and/or coherently on the patterned surface 204.

The threading dislocation glide typically results from a nonpolar or semipolar III-nitride layer 100 of the heterostructure deposited heteroepitaxially and coherently on a non-patterned surface 110 of a nonpolar or semipolar III-nitride substrate 102 or epilayer (see Fig. 1). The use of the patterned surface 204 can reduce or eliminate the amount of threading dislocation glide.

The dimension / can be, but is not limited to, between 10 micrometers and 1 millimeter. The mesas 200a can have a variety of shapes, including, but not limited to, square or rectangular shapes (as viewed from the top).

At least one of the layers 500a-b can have a different III-nitride composition from the nonpolar or semipolar III-nitride substrate 502 or the epilayer.

A heterointerface 510 between the heterostructure 500, or layers 500a-b, and the patterned surface 204 can include a misfit dislocation (MD) density that is reduced by a factor of at least 10, or at least 1000, as compared to a misfit dislocation density resulting from a semipolar or nonpolar III-nitride heterostructure 100 grown heteroepitaxially and/or coherently on a non-patterned surface 110 of the nonpolar or semipolar III-nitride substrate or epilayer 102.

Fig. 6 illustrates a device structure 600 comprising device layers that can be deposited on the patterned surface 204, wherein the device structure 600 or device layers are for a non-polar or semi-polar III-nitride Light Emitting Diode (LED) or Laser Diode (LD) emitting light. The device structure 600 includes the heterostructure
500, or layers 500a-b, or one or more active layers 602 emitting light having a peak intensity at one or more wavelengths corresponding to green wavelengths or longer (e.g., yellow or red light), or a peak intensity at a wavelength of 500 nm or longer. The layers 500a-b of the heterostructure 500 can be the active layers 602.

The present invention is not limited to devices emitting at particular wavelengths, and the devices can emit at other wavelengths. The device can be a blue, yellow, or red light emitting device, for example.

The active layer 602 can comprise one or more non-polar or semi-polar III-nitride layers comprising Indium. The nonpolar or semipolar III-nitride device layer 500a-b or active layer 602 can be sufficiently thick, and have sufficiently high Indium composition, such that the light emitting device emits the light having the desired wavelengths. The light emitting active layer(s) 602 can include InGaN layers, e.g., one or more InGaN quantum wells with GaN barriers. The InGaN quantum wells can have an Indium composition of at least 7%, at least 10%, at least 16%, or at least 30%, and a thickness greater than 4 nanometers (e.g., 5 nm), at least 5 nm, or at least 8 nm, for example. However, the quantum well thickness may also be less than 4 nm, although it is typically above 2 nm thickness.

The semipolar or nonpolar III-nitride device layers of the semi-polar or non-polar light emitting device structure 600 can further include n-type waveguiding layers 604a and p-type waveguiding layers 604b and/or n-type cladding layers 606a and p-type cladding 606b layers that are sufficiently thick, and have a composition, to function as waveguiding/cladding layers for the light emitted by the active layers 602 of the LD or LED. The waveguiding layers 604a-b can comprise an indium composition of at least 7%, or at least 30%, for example.

The waveguiding layers 604a, 604b can comprise one or more InGaN quantum wells with GaN barrier layers, and the cladding layers 606a, 606b can comprise one or more periods of alternating AlGaN and GaN layers, for example. The device structure can be AlGaN cladding layer free.
The device structure 600 can further comprise an AlGaN blocking layer 608 and a GaN layer 610. While Fig. 6 illustrates a Laser Diode structure, the structure can be modified as necessary to form a Light Emitting Diode structure.

One or more of the III-nitride semi-polar or non-polar device layers 500a-b can be heterostructures, or layers that are lattice mismatched with, and/or have a different composition from, another of the semi-polar or non-polar III-nitride device layers or the substrate. For example, the device layers can be (Al,In)GaN layers on a GaN substrate. For example, the device layers can be InGaN layer(s) and an AlGaN layer(s), wherein the heterointerface is between the InGaN layer and the AlGaN layer, the InGaN layer and a GaN layer, or an AlGaN layer and a GaN layer.

One or more of the semi-polar or semipolar III-nitride device layers 500a, 500b can have a thickness equal to or greater than their critical thickness on a non-patterned surface 110 of the nonpolar or semipolar III-nitride substrate 102.

The equilibrium critical thickness corresponds to the case when it is energetically favorable to form one misfit dislocation at the layer/substrate interface.

Experimental, or kinetic critical thickness, is always somewhat or significantly larger than the equilibrium critical thickness. However, regardless of whether the critical thickness is the equilibrium or kinetic critical thickness, the critical thickness corresponds to the thickness where a layer transforms from fully coherent to partially relaxed.

Another example of the critical thickness is the Matthews Blakeslee critical thickness [4].

For example, a total thickness 612 of all the active layers 600 (e.g., multi-quantum-well stack thickness) can be equal to, or greater than, the critical thickness for the active layer on a non-patterned surface 110. A total thickness 614 of the n-type or p-type waveguiding layers 604a, 604b can be equal to, or greater than, the critical thickness for the waveguiding layers 604a, 604b on the non-patterned surface 110. A total thickness 616 of the n-type or p-type cladding layers 606a, 606b can be
equal to, or greater than, the critical thickness for the cladding layers 606a, 606b on the non-patterned surface 110.

However, using the patterned surface 204, the layers 602, 604a, 604b, and 606b, 606a can be coherently grown. For a layer X grown on a layer Y, for the case of coherent growth, the in-plane lattice constant(s) of X are constrained to be the same as the underlying layer Y. If X is fully relaxed, then the lattice constants of X assume their natural (i.e. in the absence of any strain) value. If X is neither coherent nor fully relaxed with respect to Y, then it is considered to be partially relaxed. In some cases, the substrate might have some residual strain.

Device structures using this method can be different because of the possibility of a wider available device design space (e.g., defect-free coherent structures with higher composition/thicker alloy layers).

One or more of the device layers 500a-b can have a thickness and/or composition that is high enough such that a film, comprising all, or one or more of, the device layers 500a-b, has a thickness near or greater than the film's critical thickness for relaxation on a non-patterned substrate.

One or more of the semipolar or nonpolar III-nitride device layers 500a, 500b can be thicker, and have a higher alloy composition (e.g., more Al, In, and/or B, or non-gallium element), as compared to semi-polar or nonpolar III-nitride device layers that are grown on an a non-patterned, or different patterned surface, of a semi-polar or nonpolar III-nitride substrate or epilayer.

Accordingly, one or more embodiments of the present invention illustrate a method to limit strain relaxation of hetero-epitaxial III-nitride layers 500 grown on a III-nitride substrate or epilayer, comprising patterning the substrate or epilayer; and growing the III-nitride layers 500 on the patterned substrate 202.

Embodiments of the present invention include growing, processing, and/or contacting the device layers 500a, 500b on the patterned surface 204 to fabricate any electronic or optoelectronic device, including, but not limited to, an LED, a transistor, a solar cell, or a LD.
Possible Modifications

The substrate/epilayer can be grown using alternative techniques e.g., Hydride Vapor Phase Epitaxy (HVPE)/ Molecular Beam Epitaxy (MBE)/ Chemical Vapor Deposition (CVD)/ Metal Organic Vapor Deposition (MOCVD) / ammonothermal techniques etc. The process flow for patterning etched mesas can be different - e.g., positive/negative photoresist, various dielectric masks (SiO₂, silicon nitride, etc.) can be employed for the etching (e.g., dry/wet etching).

Various etch chemistry and/or cleaning procedures can alternatively be employed. The device epitaxial re-growth can be performed using a variety/combination of growth techniques - e.g., HVPE, MBE, CVD, MOCVD, or ammonothermal growth, etc. Additionally, if MDs are formed by pyramidal/prismatic slip, then the line direction of the MDs would change accordingly; so the mesa dimensions would have to be modified accordingly. In all cases, $l$ (in Equation 1) corresponds to the TD run length in the glide direction, and is the dimension of consequence.

Advantages and Improvements

The present invention is applicable to electronic and optoelectronic devices grown on III-nitride substrates (e.g., LEDs, LDs, solar cells, High Electron Mobility Transistors (HEMTs) etc.)

The invention provides a way to limit stress-relaxation in semipolar III-nitride heteroepitaxy, thus providing an extended device design space incorporating thicker/higher composition alloy epilayers. For LEDs or LDs, an expanded emission wavelength, e.g. green, yellow and red LEDs and LDs can be realized. Significantly improved optical waveguiding can be achieved for LDs by using thicker/higher composition waveguiding and cladding layers.

State of the art semipolar III-nitride devices are grown on as received GaN substrates (typically grown by HVPE with TD density $\sim 10^6 \text{ cm}^{-2}$). As discussed
above, this implies there are enough pre-existing TDs to relieve a misfit stress of -2%. Alternatively, looking at Equation 1, MD density can also be limited by reducing TD density. In fact, GaN substrates grown by the ammonothermal method with TD density of $5 \times 10^4 \text{ cm}^{-2}$ have been reported [3]. However, such substrates are not easily available and the TD density strongly depends on the growth techniques and growth conditions. HVPE grown GaN substrates which are commercially available have typical TD density of $\sim 10^6 \text{ cm}^{-2}$. In contrast, the present invention can be applied to substrates/epilayers with varying degrees of TD density and is thus not limited by pre-existing TD density. Thus, the present invention has fewer constraints and is widely applicable.

References

The following references are incorporated by reference herein.


Conclusion

This concludes the description of the preferred embodiment of the present invention. The foregoing description of one or more embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.
WHAT IS CLAIMED IS:

1. A semipolar or non-polar III-nitride device, comprising:
   a semipolar or nonpolar III-nitride substrate or epilayer having a threading dislocation density of $10^6 \text{ cm}^2$ or more; and
   a heterostructure, comprising semipolar or nonpolar III-nitride device layers, grown on the semipolar or nonpolar III-nitride substrate or epilayer, wherein the heterostructure has a misfit dislocation density of $10^4 \text{ cm}^2$ or less.

2. The device of claim 1, wherein:
   the semipolar or nonpolar III-nitride substrate or epilayer comprises one or more mesas with a dimension $l$ along a direction of a threading dislocation glide, thereby forming a patterned surface of the semipolar or nonpolar III-nitride substrate or epilayer, and
   the heterostructure is grown heteroepitaxially and coherently on the patterned surface.

3. The device of claim 2, wherein $l$ is between 10 micrometers and 1 millimeter.

4. The device of claim 2, wherein at least one of the heterostructure’s layers has a different III-nitride composition from the semipolar or nonpolar III-nitride substrate or the epilayer.

5. The device of claim 2, wherein a heterointerface between the heterostructure and the patterned surface includes a misfit dislocation density that is reduced by a factor of at least 10 as compared to a misfit dislocation density resulting from a semipolar or nonpolar III-nitride heterostructure grown heteroepitaxially and
coherently on a non-patterned surface of the semipolar or nonpolar III-nitride substrate or epilayer.

6. The device of claim 2, wherein a heterointerface between the heterostructure and the patterned surface includes a misfit dislocation density that is reduced by a factor of at least 1000 as compared to a misfit dislocation density resulting from a semipolar or nonpolar III-nitride heterostructure grown heteroepitaxially and coherently on a non-patterned surface of the semipolar or nonpolar III-nitride substrate or epilayer.

7. The device of claim 1, wherein one or more of the semipolar or nonpolar III-nitride device layers are thicker, and have a higher alloy composition, as compared to:
   - semi-polar or nonpolar III-nitride device layers that are grown on a non-patterned surface of semi-polar or nonpolar III-nitride substrate or epilayer, or
   - semi-polar or nonpolar III-nitride device layers that are grown on a different patterned surface of the semipolar or nonpolar III-nitride substrate.

8. The device of claim 1, further comprising a device structure on the patterned surface, wherein:
   - The device structure is for a non-polar or semi-polar III-nitride Light Emitting Diode (LED) or Laser Diode (LD), and
   - the device structure includes the heterostructure and one or more active layers emitting light having a peak intensity at one or more wavelengths corresponding to green wavelengths or longer, or a peak intensity at a wavelength of 500 nm or longer.

9. The device of claim 8, wherein the active layers comprise III-nitride Indium containing layers that are sufficiently thick, and have sufficiently high Indium composition, such that the LED or LD emits the light having the wavelengths.
10. The device of claim 9, wherein:
the device structure comprises waveguiding layers, comprising III-nitride
layers that are sufficiently thick, and have a composition, to function as the
waveguiding layers for the LD or LED, or
the device structure comprises waveguiding and cladding layers, comprising
III-nitride layers that are sufficiently thick, and have a composition, to function as
waveguiding and cladding layers for the LD or LED.

11. The device of claim 11, wherein the active layers and the waveguiding
layers comprise one or more InGaN quantum wells with GaN barrier layers, and the
cladding layers comprise one or more periods of alternating AlGaN and GaN layers.

12. The device of claim 1, wherein:
one or more of the semi-polar or non-polar III-nitride device layers have a
thickness and composition that is high enough such that a film, comprising the semi-
polar or non-polar III-nitride device layers, has a thickness near or greater than the
film's critical thickness for relaxation, and
the critical thickness is for one or more semi-polar or non-polar III-nitride
device layers deposited on a non-patterned surface of a semi-polar or non-polar III-
nitride substrate or epilayer.

13. A method of fabricating a substrate for a semipolar or non-polar III-
nitride device, comprising:
patterning and forming one or more mesas on a surface of a semipolar or non-
polar III-nitride substrate or epilayer, thereby forming a patterned surface of the
semipolar or non-polar III-nitride substrate or epilayer, wherein:
each of the mesas has a dimension / along a direction of a threading
dislocation glide, wherein the threading dislocation glide results from a semi-polar or
non-polar III-nitride layer deposited heteroepitaxially and coherently on a non-patterned surface of a semi-polar or non-polar III-nitride substrate or epilayer.

14. The method of claim 13, wherein a pre-existing threading dislocation density of the non-polar or semi-polar III-nitride substrate is at least $10^5$ cm$^{-2}$, or between $10^5$ and $10^7$ cm$^{-2}$.

15. The method of claim 13, wherein $l$ is between 10 $\mu$m and 1 mm.

16. The method of claim 13, further comprising growing a heterostructure, comprising semi-polar or non-polar III-nitride device layers, coherently on the patterned surface, wherein at least one of the semi-polar or non-polar III-nitride layers has a different III-nitride composition from the nonpolar or semipolar III-nitride substrate or epilayer.

17. The method of claim 16, wherein a heterointerface between the heterostructure and the patterned surface includes a misfit dislocation density that is reduced by a factor of at least 10 as compared to a misfit dislocation density resulting from a semipolar or nonpolar III-nitride heterostructure grown heteroepitaxially and coherently on a non-patterned surface of the semipolar or nonpolar III-nitride substrate or epilayer.

18. The method of claim 16, wherein a heterointerface between the heterostructure and the patterned surface includes a misfit dislocation density that is reduced by a factor of at least 1000 as compared to a misfit dislocation density resulting from a semipolar or nonpolar III-nitride heterostructure grown heteroepitaxially and coherently on a non-patterned surface of the semipolar or nonpolar III-nitride substrate or epilayer.
19. The method of claim 16, wherein one or more of the semipolar or nonpolar III-nitride device layers are thicker, and have a higher alloy composition, as compared to:

semi-polar or nonpolar III-nitride device layers that are grown on an on-axis surface of semi-polar or nonpolar III-nitride substrate or epilayer, or

semi-polar or nonpolar III-nitride device layers that are grown on a different vicinal surface of the semipolar or nonpolar III-nitride substrate.

20. The method of claim 16, further comprising growing a device structure, comprising nonpolar or semipolar III-nitride layers for a non-polar or semipolar III-nitride Light Emitting Diode (LED) or Laser Diode (LD), on the patterned surface, wherein:

the device structure includes the heterostructure and one or more active layers emitting light having a peak intensity at one or more wavelengths corresponding to green wavelengths or longer, or a peak intensity at a wavelength of 500 nm or longer.

21. The method of claim 20, wherein the active layers comprise III-nitride Indium containing layers that are sufficiently thick, and have sufficiently high Indium composition, such that the LED or LD emits the light having the wavelengths.

22. The method of claim 21, wherein:

the device structure comprises waveguiding layers, comprising III-nitride layers that are sufficiently thick, and have a composition, to function as the waveguiding layers for the LD or LED, or

the device structure comprises waveguiding and cladding layers, comprising III-nitride layers that are sufficiently thick, and have a composition, to function as waveguiding and cladding layers for the LD or LED.
23. The method of claim 22, wherein the active layers and the waveguiding layers comprise one or more InGaN quantum wells with GaN barrier layers, and the cladding layers comprise one or more periods of alternating AlGaN and GaN layers.

24. The method of claim 13, wherein one or more of the semi-polar or non-polar III-nitride device layers have a thickness and composition that is high enough such that a film, comprising the semi-polar or non-polar III-nitride device layers, has a thickness near or greater than the film's critical thickness for relaxation, and the critical thickness is for one or more semi-polar or non-polar III-nitride device layers deposited on a non-patterned surface of a semi-polar or non-polar III-nitride substrate or epilayer.

25. A substrate for a semipolar III-nitride device, comprising:

one or more mesas on a surface of a semipolar III-nitride substrate or epilayer, forming a patterned surface of the semipolar III-nitride substrate or epilayer, wherein:

each of the mesas includes a dimension / along a direction of a threading dislocation glide.
Fig. 1
(a) **TOP VIEW**

- $l_1$, $l_2$, $l_3$
- 200a, 200b, 200c
- Patterned mesa
- $\{1\bar{1}22\}$ GaN Substrate 202
- II projection of c-axis

L ~ 1 cm

- $l_1$, $l_2$, $l_3$
- 200a, 200b, 200c
- $\{1\bar{1}22\}$ GaN Substrate 202
- h ~ 0.5 µm

(b) **SIDE VIEW**

Fig. 2
Semipolar III-nitride substrate/epilayer

Mesa patterning using photoresist/dielectric mask

Wet/dry etching of mesa structure(s)

Removal of mask

(Optional) Surface cleaning/preparation

Epitaxial re-growth of device structure

Fig. 3
Fig. 4
Fig. 5
Fig. 6
**INTERNATIONAL SEARCH REPORT**

**A. CLASSIFICATION OF SUBJECT MATTER**

<table>
<thead>
<tr>
<th>IPC(8)</th>
<th>USPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>H01S 5/00</td>
<td>372/44.01</td>
</tr>
</tbody>
</table>

According to International Patent Classification (IPC) or to both national classification and IPC.

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

<table>
<thead>
<tr>
<th>IPC(8)</th>
<th>USPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>H01S 5/00</td>
<td>372/44.01</td>
</tr>
</tbody>
</table>

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWest (US Pat, PgPub, EPO, JPO), GoogleScholar (PL, NPL), FreePatentsOnline (US Pat, PgPub, EPO, JPO, WIPO, NPL); search terms: misfit, thread, dislocation, density, epitlayer, Group III, Ga, In, N, nitride, semi-polar, non-polar, mesa, glide, vicinal, surface, layer, device, active, waveguide, barrier.

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>WO2011/0041657 A1 (YOSHIZUMI et al.) 15 April 2010 (15.04.2010), para [0004]-[0010], [0040]-[0042], [0051]-[0054], [0059], [0073], [0077], [0079], [0081], [0088]-[0097], [0119]</td>
<td>1, 7, 12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2-6, 8-11, 13-25</td>
</tr>
<tr>
<td>Y</td>
<td>US 2003/0213964 A1 (FLYNN et al.) 20 November 2003 (20.11.2003), Figs. 42-44; para [0007], [0022], [0028], [0050], [0064], [0157], [0168], [0205]-[0209], [0254], [0260], [0262], [0271], [0287], [0296]-[0303], [0311], [0326], [0337], [0341], [0380]-[0385], [0389], [0398], [0407]-[0414]</td>
<td>2-6, 8-11, 13-25</td>
</tr>
</tbody>
</table>

Further documents are listed in the continuation of Box C.

- Special categories of cited documents:
  - "A" document defining the general state of the art which is not considered to be of particular relevance
  - "E" earlier application or patent but published on or after the international filing date
  - "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
  - "O" document referring to an oral disclosure, use, exhibition or other means
  - "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "Z" document member of the same patent family

Date of the actual completion of the international search: 20 February 2012 (20.02.2012)

Date of mailing of the international search report: 08 March 2012

Name and mailing address of the ISA/US:

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
Facsimile No. 571-273-3201

Authorized officer: Lee W. Young
PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774