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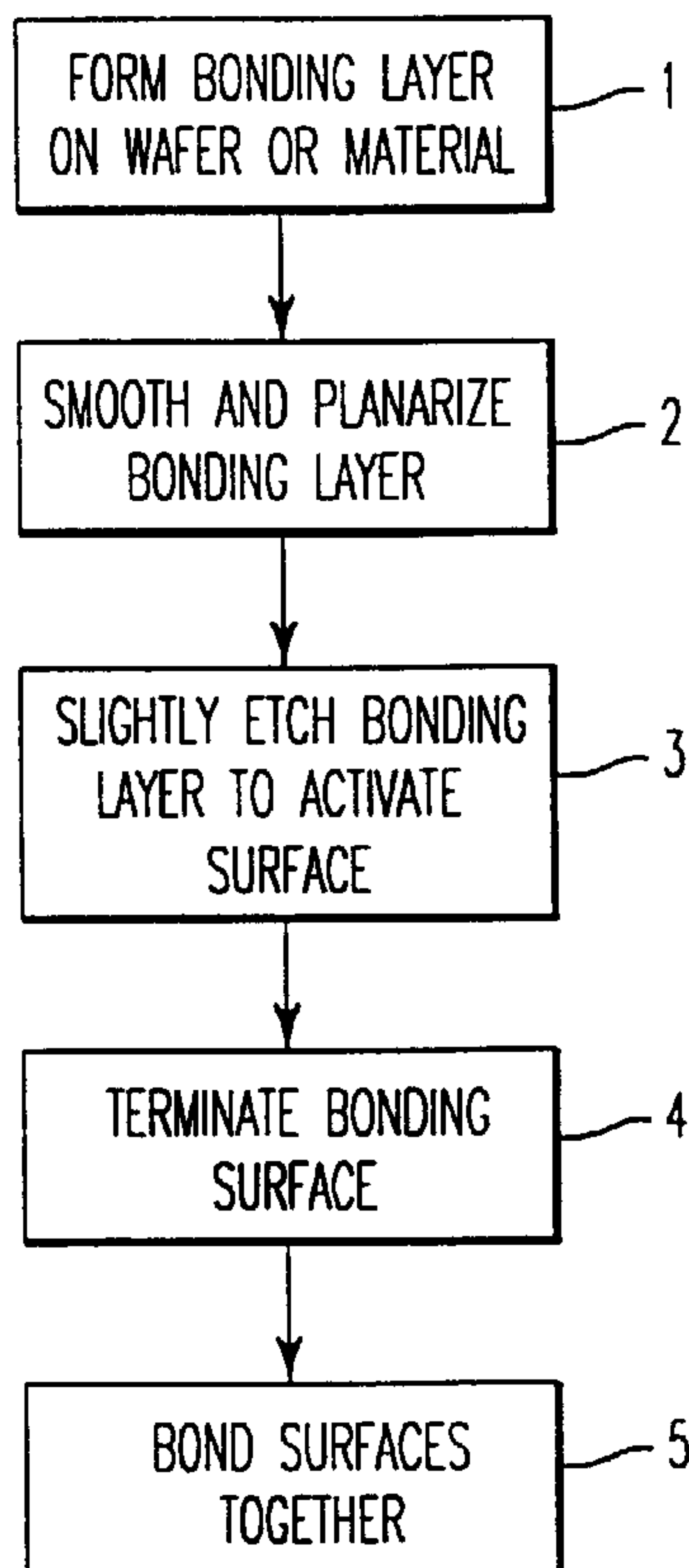

(57) Abrégé/Abstract:
A method for bonding at low or room temperature includes steps of surface cleaning and activation by cleaning or etching. The method may also include removing by-products of interface polymerization to prevent a reverse polymerization reaction to allow room temperature chemical bonding of materials such as silicon, silicon nitride and SiO_2. The surfaces to be bonded are

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(57) **Abrégé(suite)/Abstract(continued)**:
polished to a high degree of smoothness and planarity (2). VSE may use reactive ion etching or wet etching to slightly etch the surfaces being bonded (3). The surface roughness and planarity are not degraded and may be enhanced by the VSE process. The etched surfaces may be rinsed in solutions such as ammonium hydroxide or ammonium fluoride to promote the formation of desired bonding species on the surfaces (4).

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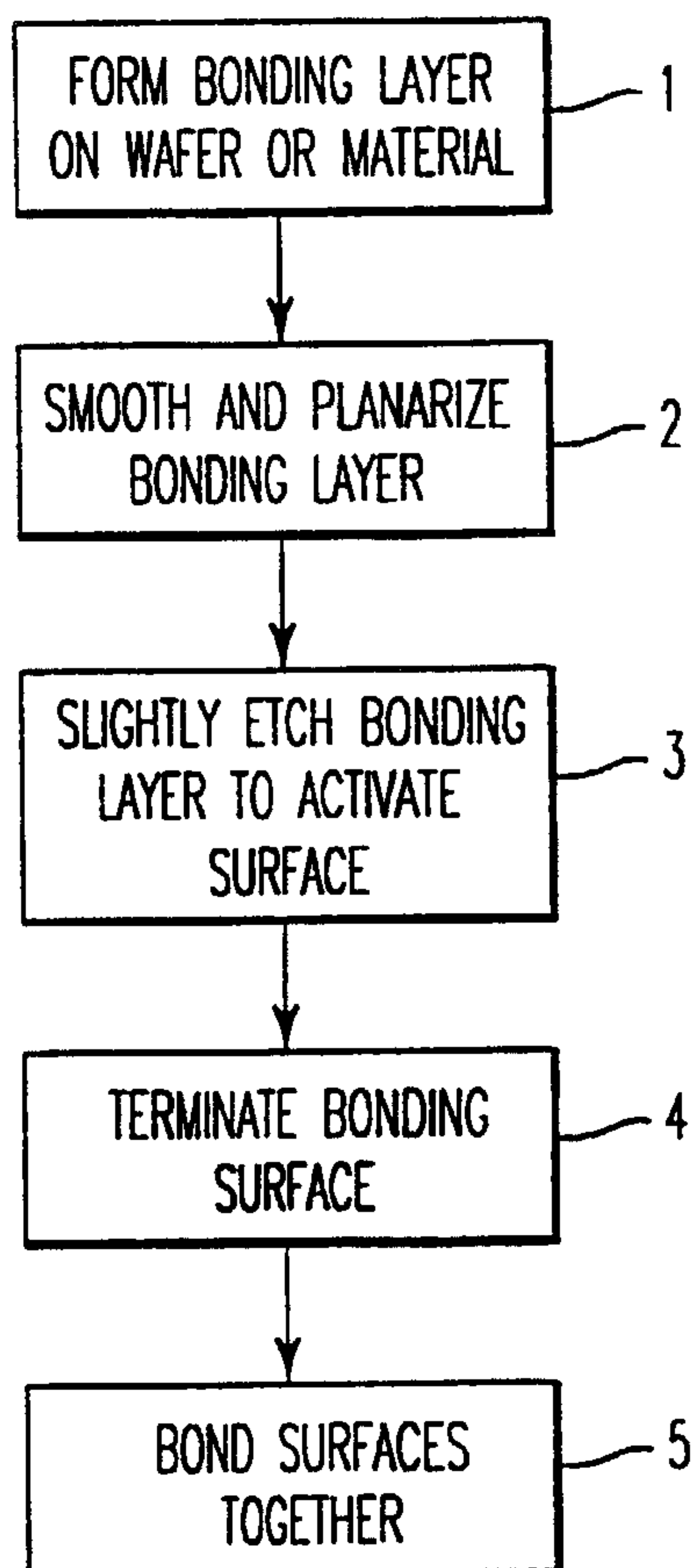
(54) Title: METHOD FOR LOW TEMPERATURE BONDING AND BONDED STRUCTURE



(57) Abstract: A method for bonding at low or room temperature includes steps of surface cleaning and activation by cleaning or etching. The method may also include removing by-products of interface polymerization to prevent a reverse polymerization reaction to allow room temperature chemical bonding of materials such as silicon, silicon nitride and SiO_2. The surfaces to be bonded are polished to a high degree of smoothness and planarity (2). VSE may use reactive ion etching or wet etching to slighthly etch the surfaces being bonded (3). The surface roughness and planarity are not degraded and may be enhanced by the VSE process. The etched surfaces may be rinsed in solutions such as ammonium hydroxide or ammonium fluoride to promote the formation of desired bonding species on the surfaces (4).

WO 01/61743 A1

Method For Low Temperature Bonding And Bonded Structure

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to bonding of materials at room temperature and, in particular, to bonding of processed semiconductor materials, such as integrated circuit or device substrates, having activated surfaces to achieve high bonding strength adequate for subsequent fabrication and/or a desired application.

2. Background of the Invention

Direct room temperature bonding generally produces weak van der Waals or hydrogen bonding. Annealing is typically required to convert the weak bond to a stronger chemical bond such as a covalent bond. Other wafer bonding techniques including anodic and fusion typically require the application of voltage, pressure and/or annealing at elevated temperature to achieve a sufficient bond strength for subsequent fabrication and/or the desired application. The need to apply voltage, pressure or heat has significantly limited wafer bonding applications because these parameters can damage the materials being wafer bonded, give rise to internal stress and introduce undesirable changes in the devices or materials being bonded. Achieving a strong bond at low temperatures is also critical for bonding of thermally mismatched or thermally sensitive wafers including processed device wafers.

Ultra high vacuum (UHV) bonding is one of the approaches to achieve a low or room temperature strong bond. However, the bonding wafers still have to be pre-annealed at high temperatures, for instance >600° C for silicon and 500° C for GaAs, before cooling down to low or room temperature for bonding. Furthermore, the UHV approach does not generally work on commonly used materials, for example, in SiO_2. It is further also expensive and inefficient.

Adhesive layers can also be used to bond device wafers to a variety of substrates and to transfer device layers at low temperatures. However, thermal and chemical instability, interface bubbles, stress and the inhomogeneous nature of adhesive layers prevent its wide application. It is thus highly desirable to achieve a strong bond at room temperature by bonding wafers in ambient without any adhesive, external pressure or applied electric field.

Low vacuum bonding has been explored as a more convenient alternative to UHV bonding but a bonding energy comparable to the bulk silicon fracture energy using bonded

bare silicon wafer pairs has only be achieved after annealing at ~150° C. For oxide covered silicon wafer pairs annealing at ~300° C is required to obtain a high bond energy. It has not been possible to obtain high bonding energies in bonded material using low vacuum bonding at room temperature.

A gas plasma treatment prior to bonding in ambient is known to enhance the bonding energy of bonded silicon pairs at low or room temperature. See, for example, G.L. Sun, Q.-Y. Tong, et al., J. de Physique, 49(C4), 79 (1988); G.G. Goetz, Proc.of 1st Intl. Symp. on Semicond. Wafer Bonding: Science, Technol. and Applications, The Electrochem. Soc., 92-7, 65 (1992); S. Farrens et al., J. Electroch. Soc., 142,3950 (1995) and Amirffeiz et al, Abstracts of 5th Intl. Symp. on Semi. Wafer Bonding: Science, Tech. and Appl., The Electrochemical Society, 99-2, Abstract No. 963 (1999). Although these treatments have increased the bond energy obtainable at low or room temperature, they have only been demonstrated with planar silicon wafers or with silicon wafers using a plasma process that results in oxide being grown on the wafers during the plasma process. Moreover, these treatments have only been used to increase the bond energy by charging or damaging the surface. Furthermore, these treatments have not been used or shown to be applicable to deposited dielectrics or other materials.

Obtaining low or room temperature bonding with a method that is not only applicable to planar silicon and grown oxide surfaces but further to deposited materials and non-planar surfaces with planarized deposited materials will allow generic materials, including processed semiconductor wafers, to be bonded with minimal damage for manufacturing purposes. Such a method based on etching and chemical bonding is described herein.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a method for bonding materials at low or room temperature.

It is another object of the invention to bond materials by cleaning and activating the bonding surfaces to promote chemical bond formation at about room temperature.

It is a further object of the invention to provide a bonding method to bond any solid state material such as processed device or integrated circuit wafers or thermally sensitive or mis-matched materials at or about room temperature.

It is further object of the invention to provide a bonding method to bond processed

device or integrated circuit wafers of different types of devices or different technologies, and transfer a layer of devices or circuits at or about room temperature.

It is another object of the invention to enable a direct wafer bonding method that does not require annealing to achieve a required bond strength.

It is a further object of the invention to provide a method whereby diverse materials including those with non-planar surfaces and deposited materials can be planarized and bonded.

These and other objects are achieved by a method of bonding having steps of forming first and second bonding surfaces, etching the first and second bonding surfaces, and bonding together at room temperature the first and second bonding surfaces after said etching step. The etching may include etching the first and second bonding surfaces such that respective surface roughnesses of the first and second bonding surfaces after said etching are substantially the same as respective surface roughnesses before said etching. The surface roughness may be in a range of 0.1 to 3.0 nm.

The bonding surfaces may be the surface of a deposited insulating material, such as silicon oxide, silicon nitride or a dielectric polymer. The bonding surface may also be the surface of a silicon wafer. Silicon wafers, using either the surface of the wafer or a deposited material on the wafer, may be bonded together. The wafers may have devices or integrated circuits formed therein. The devices and circuits in the wafers bonded together may be interconnected. The wafers may have a non-planar surface or an irregular surface topology upon which a material is deposited to form the bonding surfaces.

Forming at least one of the bonding surfaces may include depositing a polishable material on a non-planar surface. Depositing said polishable material may include depositing one of silicon oxide, silicon nitride or a dielectric polymer. The bonding surfaces may be polished using a method such as chemical-mechanical polishing. The surfaces may also be etched prior to the polishing.

The etching step may also include activating the first and second bonding surfaces and forming selected bonding groups on the first and second bonding surfaces. Bonding groups may also be formed capable of forming chemical bonds at approximately room temperature, and chemical bonds may be formed between the bonding surfaces allowing bonded groups to diffuse or dissociate away from an interface of the bonding surfaces. The chemical bonds can

increase the bonding strength between the bonding surfaces by diffusing or dissociating away said bonding groups.

After said etching step, the bonding surfaces may be immersed in a solution to form bonding surfaces terminated with desired species. The species may comprise at least one of a silanol group, an NH_2 group, a fluorine group and an HF group. Also, a monolayer of one of a desired atom and a desired molecule may be formed on the bonding surface. Terminating the surface may include rinsing said bonding materials in an ammonia-based solution after said slightly etching. The ammonia-based solution may be ammonium hydroxide or ammonium fluoride.

The method may also include exposing the bonding surfaces to one of an oxygen, argon, NH_3 and CF_4 RIE plasma process. Silicon dioxide may be deposited as to form the bonding surfaces, and etched using the RIE process.

The etching process may create a defective or damaged zone proximate to the bonding surfaces. The defective or damaged zone can facilitate the removal of bonding by-products through diffusion or dissociation.

The method may also include steps of forming first and second bonding surfaces, etching the bonding surfaces, terminating the bonding surfaces with a species allowing formation of chemical bonds at about room temperature, and bonding the bonding surfaces at about room temperature, or may include steps of forming the bonding surfaces each having a surface roughness in a range of 0.1 to 3 nm, removing material from the bonding surfaces while maintaining said surface roughness, and directly bonding the bonding surfaces at room temperature with a bonding strength of at least 500 mJ/m^2, at least 1000 mJ/m^2, or at least 2000 mJ/m^2.

The objects of the invention may also be achieved by a bonded device having a first material having a first etched bonding surface, and a second material having a second etched bonding surface directly bonded to the first bonding surface at room temperature having a bonding strength of at least 500 to 2000 mJ/m^2. The bonding surfaces may be being activated and terminated with a desired bonding species, and the desired species may include a monolayer of one of a desired atom and a desired molecule on said bonding surface or at least one of a silanol group, an NH_2 group, a fluorine group and an HF group. The bonding surfaces may each have a defective region located proximate to said first and second bonding

surfaces, respectively.

The first material may include a surface of a first semiconductor wafer having devices formed therein, and the second material may include a surface of a second semiconductor wafer having devices formed therein. Devices in the wafers may be interconnected, and the wafers may be of different technologies. The wafers may also have an integrated circuit formed therein, and devices or circuits in the wafers may be interconnected.

One of said first and second wafers may be a device region after removing a substantial portion of a substrate of said one of said first and second wafers. The wafers may have an irregular surface topology.

The first material may include a first wafer containing electrical devices and having a first non-planar surface, and the first bonding surface may include a polished and etched deposited oxide layer on said first non-planar surface. The second material may include a second wafer containing electrical devices and having a second non-planar surface, and the second bonding surface may include a polished, planarized and slightly etched deposited oxide layer on the second non-planar surface.

The first material may include a first wafer containing electrical devices and having a first surface with irregular topology, and the first bonding surface may include a polished, planarized and slightly etched deposited oxide layer on the first surface. The second material may include a second wafer containing electrical devices and having a second surface with irregular topology, and the second bonding surface may include a polished, planarized and slightly etched deposited oxide layer on the second surface.

The bonded device according to the invention may also include a first material having a first etched and activated bonding surface terminated with a first desired bonding species, and a second material having a second etched and activated bonding surface terminated with a second desired bonding species bonded to the first bonding surface at room temperature.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention and many of the attendant advantages thereof are readily obtained as the same become better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

FIG. 1 is a flow chart of the method according to the invention;

FIG. 2 is a flow chart of an example of the method according to the invention;

FIGS. 3A-3E are diagrams illustrating a first embodiment of a method according to the invention;

FIG. 4 is a diagram illustrating bonding according to the invention using silicon oxide;

FIG. 5 is a diagram illustrating bonding according to the invention using silicon;

FIGS. 6A and 6B are graphs of room temperature bonding energy versus storage time;

FIG. 7 is a diagram of a bonding fixture used in the invention; nd

FIG. 8 is a fluorine concentration profile by SIMS (Secondary Ion Mass Spectroscopy) near the bonding interface of deposited oxide covered silicon wafers that were very slight etched by diluted HF before bonding.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIGS. 1 and 3A-3E, a first embodiment of the method according to the invention will be described. Wafer 30, preferably a processed semiconductor device wafer and more preferably a processed silicon device wafer, contains a device layer 31 with processed devices. Device layer 31 may contain a number of layers and include surface regions of wafer 30. The surface topography of layer 31 is typically nonplanar. Layer 31 may also represent a processed integrated circuit containing any number of layers such as active devices, interconnection, insulation, etc.

The integrated circuit may be fully processed, or partially processed where the remaining processing is performed after the bonding process. The processing after the bonding may include full or partial substrate removal or via formation between the bonded wafers for interconnection.

On layer 31 a bonding layer 32 is formed (step 1, FIG. 1). Bonding layer 32 may be any solid state material or mixed materials which can be deposited or formed at low temperatures and can be polished to a sufficiently smooth surface. Layer 32 may be an insulator, such as SiO_2, silicon nitride, amorphous silicon formed using chemical vapor deposition (CVD) or plasma-enhanced CVD (PECVD), sputtering or by evaporation. Other materials such as polymers, semiconductors or sintered materials may also be used. Layer 32

should have thickness greater than the surface topography of layer 31.

The surface 33 of layer 32 is planarized and smoothed, as shown in step 2 of FIG. 1 and in FIG. 3B. It is noted that the roughness/planarity of surface 33 is exaggerated in FIG. 3A for illustrative purposes. This step may be accomplished using chemical-mechanical polishing. Surface 33 is preferably polished to a roughness of about no more than about 3 nm and preferably no more than about 0.1 nm and be substantially planar. The surface roughness values are typically given as root-mean square (RMS) values. Also, the surface roughness may be given as mean values which are nearly the same as the RMS values. After polishing surface 33 is cleaned and dried to remove any residue from the polishing step. Polished surface 33 is preferably then rinsed with a solution.

The bonding surface may also be etched prior to polishing to improve the planarity and/or surface roughness. The etching can be effective to remove high spots on the bonding surface by selective etching of the high spots using, for example, standard photolithographic techniques. For example, a layer of silicon nitride can be embedded within a silicon dioxide bonding layer 32 that can serve as an etch stop when using a solution containing HF. The etch stop material may be used to improve uniformity, reproducibility, and manufacturability.

FIG. 3B illustrates layer 32 having upper surface 34 after the polishing/planarization and cleaning steps. Surface 34 then undergoes an activation process (step 3, FIG. 1). This activation process is an etching process and preferably a very slight etch (VSE) process. The term VSE means that the root-mean-square micro-roughness (RMS) of the very slightly etched surface remains at approximately the unetched value, typically < 0.5 nm and preferably in the range of 0.1 nm to 3 nm. The optimum amount of material removed depends upon the material and the method used for removal. Typical amounts removed vary from Angstroms to a few nanometers. It is also possible to remove more material. VSE also includes the breaking of bonds on the treated surfaces and can occur without significant removal of material. The VSE is distinct from simple modification of the surface by, for example, charging the surface with electronic charge or damaging the surface layer. In a first example of the method according to the invention, the VSE process consists of a gas or mixed gas (such as oxygen, argon, nitrogen, CF_4, NH_3) plasma process at a specified power level for a specified time (FIG. 3C) . The power and duration of the plasma process will vary depending upon the materials used to obtain the desired bond energy. Examples are given

below, but in general, the power and duration will be determined empirically.

The plasma process may be conducted in different modes. Both reactive ion etch (RIE) and plasma modes may be used, as well as an inductively-coupled plasma mode (ICP). Sputtering may also be used. Data and examples are given below in both the RIE and plasma modes.

The VSE process etches the surface very slightly via physical sputtering and/or chemical reaction and preferably is controlled to not degrade the surface roughness of the bonding surfaces. The surface roughness may even be improved depending upon the VSE and materials etched. Almost any gas or gas mixture that will not etch surface 34 excessively can be used for the room temperature bonding method according to the invention.

The VSE serves to clean the surface and break bonds of the oxide on the wafer surface. The VSE process can thus enhance the surface activation significantly. A desired bonding species can be used to terminated on surface 34 during the VSE by proper design of the VSE. Alternatively, a post-VSE treatment that activates and terminates the surface with a desired terminating species during the post-VSE process may be used.

The desired species further preferably forms a temporary bond to the surface 34 atomic layer, effectively terminating the atomic layer, until a subsequent time that this surface can be brought together with a surface terminated by the same or another bonding species 36 as shown in FIG. 3D. Desired species on the surfaces will further preferably react with each other when they are in sufficiently close proximity allowing chemical bonding between surfaces 34 and 36 at low or room temperature that is enhanced by diffusion or dissociation and diffusion of the reacted desired species away from the bonding interface.

The post-VSE process preferably consists of immersion in a solution containing a selected chemical to generate surface reactions that result in terminating the bonding surface 34 with desired species. The immersion is preferably performed immediately after the VSE process. The post-VSE process may be performed in the same apparatus in which the VSE process is conducted. This is done most readily if both VSE and post-VSE processes are either dry, i.e, plasma, RIE, ICP, sputtering, etc, or wet, i.e., solution immersion. A desired species preferably consists of a monolayer or a few monolayers of atoms or molecules.

The post-VSE process may also consist of a plasma, RIE, or other dry process whereby appropriate gas chemistries are introduced to result in termination of the surface

with the desired species. The post-VSE process may also be a second VSE process. The termination process may also include a cleaning process where surface contaminants are removed without VSE. In this case, a post-cleaning process similar to the post-VSE processes described above then results in a desired surface termination.

The post-VSE or post-cleaning process may or may not be needed to terminate surfaces with desired species if the activated surface bonds by the cleaning or VSE process are subsequently sufficiently weakly surface reconstructed and can remain sufficiently clean before bonding such that subsequent bonding with a similar surface can form a chemical bond.

The wafers are optionally rinsed then dried. Two wafers are bonded by aligning them (if necessary) and bringing them together to form a bonding interface. As shown in FIG. 3D, a second wafer 35 has been processed in the manner shown in FIG. 3C to prepare bonding surface 36. The two wafers are brought together by, for example, commercially available wafer bonding equipment (not shown) to initiate bonding interface 37 (FIG. 3E).

A spontaneous bond then typically occurs at some location in the bonding interface and propagates across the wafer. As the initial bond begins to propagate, a chemical reaction such as polymerization that results in chemical bonds takes place between species used to terminate surfaces 34 and 36 when the surfaces are in sufficient proximity. The bonding energy is defined as the specific surface energy of one of the separated surfaces at the bonding interface that is partially debonded by inserting a wedge. The by-products of the reaction then diffuse away from the bonding interface to the wafer edge or are absorbed by the wafers, typically in the surrounding materials. The by-products may also be converted to other by-products that diffuse away or are absorbed by the wafers. The amount of covalent and/or ionic bonding may be increased by removal of converted species resulting in further increase in bond strength.

FIGS. 4A-4E show surface conditions and the bonding propagation to form covalent bonds in a the case of a planar Si wafer covered with silicon oxide. On Si wafer 40 an SiO_2 layer 41 is formed, which has been polished and planarized. Surface 42 of layer 41 is subjected to the VSE process to produce an activated surface (FIG. 4A). On a second wafer 44 a second SiO_2 layer 45 is formed, and surface 46 is subjected to a VSE process to activate surface 46 (FIG. 4B). Desired species are terminated on surface 46 and are shown as lines 43

in FIG. 4C. Either or both of a VSE and post-VSE processes are used to properly terminate surface 46. While not shown, surface 42 may also be terminated using a post-VSE process. Wafer 44 is brought together with wafer 40 (FIG. 4D) and bonds 46 begin to form. the bonding propagates and by-products are removed (indicated as arrows 47) and chemical bonds (such as covalent) are formed, as shown in FIG. 4E.

The bonding immediately after the RIE process may use a special bonding fixture allowing immediate in situ bonding of the etched wafers. A diagram of the fixture is shown in FIG. 7. In plasma chamber 75 are two wafers to be bonded 70 disposed on RF electrodes 76 and 77. A plasma is formed in zone 79 by the application of RF power to the electrodes via moveable vacuum RF power feedthrough 74 and by the introduction of an appropriate gas or gas mixture through gas feedthrough 73. Element 71 is a vacuum feedthrough for mechanical actuator (not shown) to retract retractable spacer 72. Chamber 75 is pumped down to a desired vacuum level via pumps (not shown) and chamber inlet 78. In the case where a post-VSE process or post cleaning process is also a dry process, as discussed above, the VSE and post-VSE or post-cleaning may be conducted in chamber 75.

After the plasma treatment to conduct the VSE process, the mechanical spacers 72 are retracted by the mechanical actuator and the wafers 70 are moved into contact with to begin the bonding process. The bonded wafers are then moved from the chamber into ambient or into another vacuum chamber (not shown) and stored for a desired period to allow the bonding to propagate by a wafer handling system (not shown).

The materials of the bonding layers preferably have an open structure so that the by-products of the polymerization reaction can be easily removed. The bonding species on the opposing bonding surfaces must be able to react at room temperature to form a strong or chemical bond. The bond energy is sufficiently high to virtually eliminate slippage between wafers after subsequent heat treatments associated with a subsequent processing or operation when wafers have different thermal expansion coefficients. Lack of slippage is manifest by a lack of wafer bowing upon inspection after the subsequent processing or operation.

In order to achieve the high bonding energies, it is preferable for at least one of the wafers to be as thin as possible because a thin wafer allows compliance to accommodate a lack of perfect surface planarization and smoothness. Thinning to thickness of about 10 mils to 10 microns is effective.

The bonded wafers are preferably stored at ambient or at low or room temperature after bonding to allow removal of species or converted species for a specified period of time depending upon the materials and species used. Twenty four hours is usually preferable. The storage time is dependent upon the type of plasma process used. Chemical bonds may be obtained more quickly, in a matter of minutes, when certain plasma processes such as an Ar plasma are used. For example, 585 mJ/m^2 bonds were obtained in immediately after bonding and over 800 mJ/m2 were observed after 8 hours for deposited oxides etched by an Ar plasma followed by NH_4OH dip.

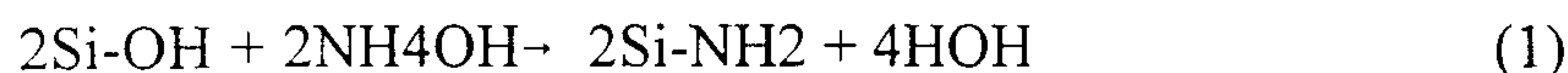
Annealing the bonded wafers during bonding may increase the bonding strength. The annealing temperature should be below 200° C and may be typically in the range of 75-100° C. Storing the bonded wafers under vacuum may facilitate the removal of residual gasses from the bonding surfaces, but is not always necessary.

All of the processes above may be carried out at or near room temperature. The wafers are bonded with sufficient strength to allow subsequent processing operations (lapping, polishing, substrate removal, chemical etching, lithography, masking, etc.). Bonding energies of approximately 500-2000 mJ/m^2 or more can be achieved (see FIG. 6A).

At this point (FIG. 3E) it is possible to remove a part or all of the substrate of wafer 35 by, for instance, lapping and etch back. The layer of devices of wafer 35 is thus transferred onto wafer 30. The devices from the two layers may be interconnected. Additional device or circuit layers may be bonded and interconnected to form a multilayer structure. Different types of wafers, devices or circuits may be bonded, as well as different technologies (i.e. CMOS and bipolar or III-V HBT and Si CMOS). Other elements or materials such as thermal spreaders, surrogate substrates, antennas, wiring layers, a pre-formed multi-layer interconnects, etc. may be bonded to produce different types of circuits or systems, as desired.

In an example, shown in FIG.2, PECVD SiO_2 is deposited on a Si wafer containing devices. Surface 34, after the plasma (such as argon, oxygen or CF_4) treatment, is mainly terminated by Si-OH groups due to the availability of moisture in the plasma system and in air. After the plasma treatment, the wafers are immediately immersed in solution such as ammonium hydroxide (NH_4OH), NH_4F or HF for a period such as between 10 and 120 seconds. After immersing the wafers in the NH_4OH solution, many Si-OH groups are

replaced by Si-NH2 groups according to the following substitution reaction:



$$2Si\text{-}OH + 2NH4OH \rightarrow 2Si\text{-}NH2 + 4HOH \quad (1)$$

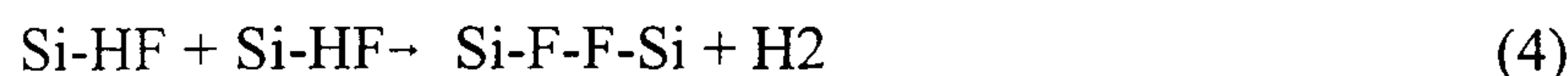
Alternatively, many Si-F groups are terminating on the PECVD SiO_2 surface after an NH_4F or HF immersion.

The hydrogen bonded Si-NH2:Si-OH groups or Si-NH2:Si-NH2 groups across the bonding surfaces can polymerize at room temperature in forming Si-O-Si or Si-N-N-Si (or Si-N-Si) covalent bonds:

$$Si\text{-}NH2 + Si\text{-}OH \rightarrow Si\text{-}O\text{-}Si + NH3 \quad (2)$$

$$Si\text{-}NH2 + Si\text{-}NH2 \rightarrow Si\text{-}N\text{-}N\text{-}Si + 2H2 \quad (3)$$

Alternatively, the HF or NH_4F dipped oxide surfaces are terminated by Si-F groups in addition to Si-OH groups. Since HF or NH_4F solution etches silicon oxide strongly, their concentrations must be controlled to an adequately low level, and the immersion time must be sufficiently short. This is an example of a post-VSE process being a second VSE process. The covalent bonds across the bonding interface are formed due to the polymerization reaction between hydrogen bonded Si-HF or Si-OH groups:



$$Si\text{-}HF + Si\text{-}HF \rightarrow Si\text{-}F\text{-}F\text{-}Si + H2 \quad (4)$$

$$Si\text{-}F + Si\text{-}OH \rightarrow Si\text{-}O\text{-}Si + HF \quad (5)$$

FIG. 8 shows the fluorine concentration profile of bonded thermal oxide covered silicon wafers that were dipped in 0.05% HF before room temperature bonding. A fluorine concentration peak is clearly seen at the bonding interface. This provides evidence of the chemical process described above where the desired species are located at the bonding interface.

Since reaction (2) is reversible only at relatively high temperatures of ~500° C, the formed siloxane bonds should not be attacked by NH_3 at lower temperatures. It is known that H_2 molecules are small and diffuse about 50 times quicker than water molecules in oxide. The existence of a damaged layer near the surface of an adequate thickness i.e. a few nm, will facilitate the diffusion or dissolution of NH_3, and HF and hydrogen in reactions (2), (3), (4) and/or (5) in this layer and enhancement of the chemical bond. The three reactions result in a higher bonding energy of SiO_2/SiO_2 bonded pairs at room temperature after a period of storage time to allow NH_3 or H_2 to diffuse away.

In the example of FIG. 2, the plasma treatment may create a damaged or defective

area in the oxide layer near the bonding surface. The zone extends for a few monolayers. The damaged or defective area aids in the removal of bonding by-products. Efficient removal of the bonding by-products improves the bonding strength since the by-products can interfere with the bonding process by preventing high-strength bond from forming..

Many different surfaces of materials may be smoothed and/or planarized, followed by a cleaning process, to prepare for bonding according to the invention. These materials can be room temperature bonded by mating surfaces with sufficient planarity, surface smoothness, and passivation that includes cleaning, and/or VSE, activation and termination. Amorphous and sintered materials, non-planar integrated circuits, and silicon wafers are examples of such materials. Single crystalline semiconductor or insulating surfaces, such as SiO_2 or Si surfaces, can also be provided with the desired surface roughness, planarity and cleanliness. Keeping the surfaces in high or ultra-high vacuum simplifies obtaining surfaces sufficiently free of contamination and atomic reconstruction to achieve the strong bonding according to the invention. Other semiconductor or insulator materials such as InP, GaAs, SiC, sapphire, etc., may also be used. Also, since PECVD SiO_2 may be deposited on many types of materials at low temperatures, many different combinations of materials may be bonded according to the invention at room temperature. Other materials may also be deposited as long as appropriate processes and chemical reactions are available for the VSE, surface activation, and termination.

For example, the method may also be used with silicon nitride as the bonding material. Silicon nitride may be bonded to silicon nitride, or to silicon dioxide and silicon. Silicon oxide may also be bonded to silicon. Other types of dielectric materials may be bonded together including aluminum nitride and diamond-like carbon.

The method may be applied to planar wafers having no devices or circuits and one wafer with devices and circuits. The planar wafer may be coated with a bonding layer, such as PECVD oxide or amorphous silicon, and then processed as described above to bond the two wafers. The planar wafer may not need to be coated with a bonding layer if it has sufficient smoothness and planarity and the proper bonding material.

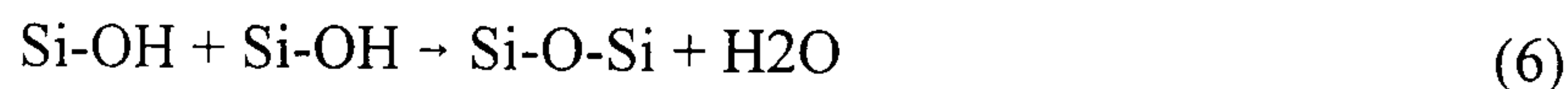
As can be appreciated, the bonding process may be repeated with any number of wafers, materials or functional elements. For example, two device or IC wafers may be joined, followed by removing one of the exposed substrates to transfer a layer or more of

devices, or just the active regions of an IC.

The bonding according to the invention may be applied to joining different types of materials. For example, a silicon wafer can be bonded to another silicon wafer, or bond to an oxidized silicon wafer. The bare silicon wafer and the oxide covered wafer are immersed in HF, NH_4F and/or NH_4OH and bonded after drying. The time for the immersion should be less than about twenty minutes for the silicon wafer covered with the thin oxide since the NH_4OH solution etches silicon oxide. Since HF and NH_4F etches oxides strongly, very diluted solutions, preferably in 0.01-0.2% range should be used for dipping of the silicon wafers.

After drying the silicon wafer and the oxide-covered wafer are bonded in ambient at room temperature. Reactions (2), (3), (4) and/or (5) take place at the bonding interface between the two wafers. The plasma-treated wafers may also be immersed in deionized water instead of the NH_4OH solution.

The silicon bonding may be conducted with a bare silicon wafer, i.e. having a native oxide or a silicon wafer having an oxide layer formed on its surface as described above. During the oxygen plasma treatment, the native oxide which if formed on the bare silicon wafer is sputter etched, and the oxide layer formed on the silicon surface is etched. The final surface is an activated (native or formed) oxide. When rinsed in deionized water, the activated oxide surface is mainly terminated with Si-OH groups. Since oxide growth in oxygen plasma has been found to have less water than in normal native oxide layers, the water from the original bonding bridge and generated by the following polymerization reaction (6) can be absorbed into the plasma oxide readily.



$$\text{Si-OH} + \text{Si-OH} \rightarrow \text{Si-O-Si} + \text{H2O} \qquad (6)$$

FIGS. 5A-5E illustrate bonding two silicon wafers. Wafers 50 and 52 have respective surfaces 51 and 53 with native oxides (not shown) subjected to a VSE process. Surface 53 is in FIG. 5C is shown terminated with a desired species 54. The two wafers are brought together and bonds 55 begin to form (FIG. 5D). The bonding propagates and bonding by-products, in this case H_2 gas, are removed. The by-products being removed are shown as arrows 56 in FIG. 5E.

In addition to removal of the water from the bonding interface by dissolving into the plasma activated oxide of the oxidized silicon wafer, the water can also diffuse through the

thin oxide layer on the bare silicon wafer to react with silicon. As the silicon surface underneath the oxide has a damaged or defective zone, extending for a few monolayers, the water molecules that diffuse through the oxide layer and reach the damaged or defective zone can be converted to hydrogen at room temperature and be removed readily:

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \qquad (7)$$

The reverse reaction of (6) is thus avoided and the room temperature bonding energy increases enormously due to the formation of covalent Si-O-Si bonds.

If a relatively thick (~5 nm) oxide layer is formed, it will take a long period of time for the water molecules to diffuse through this thick layer. On the other hand, if after the plasma treatment a thin oxide layer is left or a too narrow defective zone is formed, water that can reach the silicon surface may not react sufficiently with the silicon and convert to hydrogen. In both cases the bonding energy enhancement will be limited. The preferred oxygen plasma treatment thus leaves a minimum plasma oxide thickness (e.g., about 0.1-1.0 nm) and a reasonably thick defective zone (e.g., about 0.1-0.3 nm) on the silicon surface.

In a second embodiment, the VSE process uses wet chemicals. For example, an InP wafer having a deposited silicon oxide layer, as in the first embodiment, and a device layer are bonded to a AlN substrate having a deposited oxide layer. After smoothing and planarizing the InP wafer bonding surface and the AlN wafer bonding surface, both wafers are cleaned in an standard RCA cleaning solution. The wafers are very slightly etched using a dilute HF aqueous solution with an HF concentration preferably in the range of 0.01 to 0.2%. About a few tenths of a nm is removed and the surface smoothness is not degraded as determined by AFM (atomic force microscope) measurements. Without deionized water rinse, the wafers are spin dried and bonded in ambient air at room temperature. The resulting bonding energy has been measured to reach ~700 mJ/m^2 after storage in air. After annealing this bonded pair at 75°C the bonding energy of 1500 mJ/m^2 was obtained., The bonding energy has been measured to reach silicon bulk fracture energy (about 2500 mJ/m^2) after annealing at 100°C. If the wafers are rinsed with deionized water after the HF dip, the bonding energy at 100°C is reduced to 200 mJ/m^2 , that is about one tenth of that obtained without the rinse. This illustrates the preference of F to OH as a terminating species.

In a third embodiment the VSE process consists of 0.1% HF etching followed by 5 min dip in 0.02% HN_4F solution of thermally oxidized silicon wafers at room temperature

after a standard cleaning process. Without rinsing in deionized water, the wafers are bonded after spin drying at room temperature. The bonding energy of the bonded pairs reaches ~1700 mJ/m^2 after 100°C annealing. If the wafers are rinsed in de-ionized water after the HF etching before bonding, the bonding energy of bonded pairs is only 400 mJ/m^2, again illustrating the preference of F to OH as a terminating species.

Dilute NH_4F is used in the VSE process to etch silicon oxide covered wafers in a fourth embodiment. The concentration of the NH_4F should be below 0.02% to obtain the desired bonding. The bonding energy of ~600 mJ/m^2 can be achieved at room temperature after storage.

A fifth embodiment of the invention is used to bond Si surfaces having a native oxide of about 1 nm in thickness. In the fifth embodiment, after cleaning the Si surface by a standard RCA1 cleaning process, a VSE process using 5 min etching in 70% HNO_3 + diluted HF (preferably 0.01 to 0.02%) is performed. Wafers are pulled out of the solution vertically with a basically hydrophobic surface. Without rinsing in water, the wafers were bonded at room temperature in air. In this process covalent bonding occurs at room temperature with measured bonding energies typically about 600 mJ/m^2. This bonding energy is significantly increased to 1300 mJ/m^2 after annealing at 75°C and reaches the fracture energy of bulk silicon (about 2500 mJ/m^2) at a temperature of 100° C.

Instead of 70% HNO_3, diluted HNO_3 with water can be used in the solution to achieve similar results. According to AMF measurements and high resolution transmission electron microscopy measurement results, the silicon is etched in the dilute HNO_3 VSE process at a rate of 0.1-0.15 nm/min and a new thick oxide 2.5-3.5 nm in thickness is formed.

As further embodiments, the VSE process may consist of a dry etch that has chemical and/or physical components. For a bare Si surface, chemical etching may result from SF_4/H_2 gas mixture while physical etching may result from Ar etch. For a silicon oxide surface, chemical etching may use CF_4 while physical etching may use oxygen or argon gas. It is also possible to use a thermally stable polymer material for the bonding materials and bond two polymer surfaces together. Examples are polyimides or spin-on materials.

The mechanisms governing the increased bond energy at low or room temperature are similar. A very slight etching (VSE) of the bonding wafers by plasma to clean and activate the surfaces, and improve removal of by-products of interface polymerization to prevent the

undesirable reverse reaction and rinse in appropriate solution to terminate the surface with desired species to facilitate room temperature covalent bonding. The oxide covered wafer bonding case is similar except that a different surface termination is preferred. In bare silicon wafer bonding, the highly reactive surface layers of oxide and silicon to allow water adsorption and conversion to hydrogen should be formed. The highly reactive layers can be a plasma thin oxide layer and a damaged silicon surface layer. The oxide on the silicon wafer will also have some damage. Not only O_2 plasma but also plasma of other gases (such as Ar, CF_4) are adequate. Because during and after VSE the silicon surface is readily to react with moisture to form an oxide layer, and the underlying damaged silicon layer is created by VSE. Since the VSE and by-products removal methods are rather general in nature, this approach can be implemented by many means and apply to many materials.

EXAMPLE 1

In a first example, three inch <100>, 1-10 ohm-cm, boron doped silicon wafers were used. PECVD oxide was deposited on some of the silicon wafers. For comparison, thermal oxidized silicon wafers were also studied. The PECVD oxide thickness was 0.5 μm and 0.3 μm on the front side and the back side of the wafers, respectively. Oxide is deposited on both sides of the wafer to minimize wafer bow during polishing and improve planarization. A soft polish was performed to remove about 30 nm of the oxide and to smooth the front oxide surface originally having a root mean square of the micro-roughness (RMS) of ~0.56 nm to a final ~0.18 nm. A modified RCA1 solution was used to clean the wafer surfaces followed by spin-drying.

Two wafers were loaded into the plasma system, both wafers are placed on the RF electrode and treated in plasma in RIE mode. For comparison, some wafers were treated in plasma mode in which the wafers were put on the grounded electrode. An oxygen plasma was used with a nominal flow rate of 16 scc/m. The RF power was 20-400 W (typically 80 W) at 13.56 MHz and the vacuum level was 100 mTorr. The oxide covered wafers were treated in plasma for times between 15 seconds to 5 minutes. The plasma treated silicon wafers were then dipped in an appropriate solution or rinse with de-ionized water followed by spin-drying and room temperature bonding in air. Some of the plasma treated wafers were also directly bonded in air without rinse or dipping.

The bonding energy was measured by inserting a wedge into the interface to measure the crack length according to the equation:

$$\gamma = \frac{3t_b^2 E_1 t_{w1}^3 E_2 t_{tw2}^3}{16L^4 \left(E_1 t_{w1}^3 + E_2 t_{w2}^3 \right)}$$

E and tw are the Young's modulus and thickness for wafers one and two and tb is the thickness of a wedge inserted between the two wafers that results in a wafer separation of length L from the edge of the wafers.

The room temperature bonding energy as a function of storage time of bonded plasma treated oxide covered silicon wafers is shown in FIG. 6A. This figure shows measured room temperature bonding energy versus storage time for 4 different cases as shown. The results can be summarized as follows: (1) for dipped and bonded RIE plasma treated oxide wafers, the room temperature bonding energy increases with storage time and reaches a stable value after ~20 h in air or at low vacuum; (2) RIE mode results in higher bonding energies than plasma mode; (3) too short a plasma exposure time or too low a plasma power provides a small or negligible increase in bond energy; (4) NH_4OH dip after plasma treatment shows a much higher increase in bonding energy than water rinse; (5) direct bonding in air after plasma treatment without dipping or rinse shows an almost constant bonding energy with time. The bonding energy of the directly bonded wafer pairs immediately after room temperature bonding is slightly higher than the de-ionized water rinsed or NH_4OH dipped wafer pairs.

FIG. 6B shows room temperature bonding of Si and AlN wafers with PECVD oxide deposited layers. After about 100 h of storage time a bonding energy of over 2000 mJ/m^2 were observed.

Comparing different bonding materials, the bonding energy as a function of storage time of O_2 plasma treated thermally oxidized silicon wafer pairs is similar to wafers with PECVD oxide, although the values of the room temperature bonding energy are somewhat lower.

After ~24 h storage in air at room temperature, the bonding energy as high as ~1000 mJ/m2 was reached in the RIE mode plasma treated and NH_4OH dipped PECVD oxide

covered wafer pairs. Since the maximum bonding energy of a van der Waals bonded silicon oxide covered wafer pairs is about 200 mJ/m2, a large portion of the bonding energy is attributed to the formation of covalent bonds at the bonding interface at room temperature according to the above equation.

EXAMPLES 2-3

The above process was applied to bond processed InP wafers (600 μm thick) to AlN wafers (380 μm thick), or to bond processed Si (380 μm thick) and InP (600 μm thick) wafers, as second and third examples. The processed InP device wafers are covered with PECVD oxide and planarized and smoothed by chemical-mechanical polishing CMP. A PECVD oxide layer is also deposited on the AlN wafers and is planarized and smoothed to improve the RMS surface roughness. The processed Si and processed InP wafers are deposited with PECVD oxide and planarized and smoothed using CMP. After VSE similar to the example 1 bonding at room temperature, the bonded wafers are left in ambient air at room temperature.

After 24 hours storage at room temperature, bonding energy of 1000 mJ/m2 and 1100 mJ/m2 were achieved for the InP/Si and InP/AlN bonded pairs, respectively. For processed Si (380 μm thick) /oxide covered AlN (280 μm thick) wafer pairs, the bonding energy at room temperature as high as 2500 mJ/m2 has been achieved. These room temperature bonded plasma treated wafer pairs have sufficient bonding strength to sustain subsequent substrate lapping and etching and other typical semiconductor fabrication processes before or after substrate removal.

The InP substrate in the room temperature bonded InP/AlN pairs was lapped with 1900# Al2O3 powder from initial 600 μm thick to ~50 μm thick followed by etching in an HCl/H3PO4 solution to leave about a 2.0 μm thick InP device layer on the AlN or Si wafer. The water and etching solution did not penetrate into the bonding interface.

Surfaces are sputter etched by energetic particles such as radicals, ions, photons and electrons in the plasma or RIE mode. For example, the O_2 plasma under conditions that bring about the desired VSE is sputter-etching about 2 Å /min of PECVD oxide as measured by a reflectance spectrometry. For thermal oxide the sputter etching rate is about 0.5 Å/min. The thickness of oxide before and after plasma treatment was measured by a reflectance

spectrometry and averaged from 98 measured points on each wafer. The etching by O_2 plasma has not only cleaned the surface by oxidation and sputtering but also broken bonds of the oxide on the wafer surfaces.

However, the surface roughness of plasma treated oxide surfaces must not be degraded by the etching process. AFM measurements show that compared with the initial surface roughness, the RMS of the O_2 plasma treated oxide wafers was ~2 Å and did not change noticeably. On the other hand, if the etching is not sufficiently strong, the bonding energy enhancement effect is also small. Keeping other conditions unchanged when the O_2 plasma treatment was performed with plasma mode rather than RIE mode, the etching of oxide surfaces is negligible and the oxide thickness does not change. The final room temperature bonding energy is only 385 mJ/m2 compared to 1000 mJ/m2 of RIE treated wafers (see FIG. 6A).

Other gas plasma has shown a similar effect. CF_4/O_2 RIE was used to remove ~4 nm of PECVD oxide from the wafer surfaces prior to bonding. The bonding energy of room temperature bonded PECVD oxide covered silicon wafers was also enhanced significantly in this manner and exceeds 1000 mJ/m2 after sufficient storage time (see also FIG. 6A).

An argon plasma has also been used for the VSE with a nominal flow rate of 16 scc/m. The RF power was typically 60 W at 13.56 MHz and the vacuum level was 100 mTorr. The oxide covered silicon wafers were treated in plasma in RIE mode for times between 30 seconds to 2 minutes. The plasma treated silicon wafers were then dipped in an NH_4OH solution followed by spin-drying and room temperature bonding in air. The bonding energy reached ~800 mJ/m^2 at room temperature after only 8 h storage in air.

Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.

Claims:

1. A bonding method, comprising:

forming first and second bonding surfaces;

etching said first and second bonding surfaces; and

bonding together at room temperature said first and second bonding surfaces after said etching step.

2. A method as recited in claim 1, wherein said etching step comprises:

etching said first and second bonding surfaces such that respective surface roughnesses of said first and second bonding surfaces after said etching are substantially the same as respective surface roughnesses before said etching.

3. A method as recited in claim 2, comprising:

forming said first and second bonding surfaces to have a surface roughness in a range of 0.1 to 3.0 nm.

4. A method as recited in claim 1, wherein said etching step comprises:

activating said first and second bonding surfaces and forming selected bonding groups on said first and second bonding surfaces.

5. A method as recited in claim 4, comprising:

forming bonding groups capable of forming chemical bonds at approximately room temperature.

6. A method as recited in claim 1, comprising:

forming chemical bonds between said bonding surfaces allowing bonded groups to diffuse or dissociate away from an interface of said first and second bonding surfaces.

7. A method as recited in claim 6, comprising:

increasing bonding strength between said first and second bonding surfaces by diffusing or dissociating away said bonding groups.

8. A method as recited in claim 1, wherein said etching step comprises:

forming a monolayer of one of a desired atom and a desired molecule on said bonding surface.

9. A method as recited in claim 8, wherein said etching step comprises:

forming a few monolayers of one of a desired atom and a desired molecule on said bonding surface.

10. A method as recited in claim 1, comprising:

after said etching step, immersing said first and second bonding surfaces in a solution to form bonding surfaces terminated with desired species.

11. A method as recited in claim 10, wherein said species comprise at least one of a silanol group, an NH_2 group, a fluorine group and an HF group.

12. A method as recited in claim 10, wherein said etching step comprises:

forming a monolayer of one of a desired atom and a desired molecule on said bonding surface.

13. A method as recited in claim 1, wherein said etching comprises:

exposing said first and second bonding surfaces to a plasma.

14. A method as recited in claim 1, comprising:

exposing said first and second bonding surfaces to one of an oxygen, argon, NH_3 and CF_4 plasma process.

15. A method as recited in claim 14, comprising:

conducting said plasma process in one of RIE mode, ICP mode, plasma mode and sputtering mode.

16. A method as recited in claim 1, comprising:

polishing respective first and second bonding surfaces to respective desired surface roughnesses and planarity; and

etching said first and second bonding surfaces after said polishing to activate said first and second bonding surfaces.

17. A method as recited in claim 16, wherein:

forming at least one of said first and second bonding surfaces comprises depositing a polishable material on a non-planar surface.

18. A method as recited in claim 17, wherein depositing said polishable material comprises depositing one of silicon oxide, silicon nitride or a dielectric polymer.

19. A method as recited in claim 1, wherein said etching step comprises:

increasing available bonding energy of bonding pairs on said first and second bonding surfaces at approximately room temperature.

20. A method as recited in claim 19, comprising:

obtaining a bond of at least 500 mJ/m^2.

21. A method as recited in claim 19, comprising:

obtaining a bond of at least 1000 mJ/m^2.

22. A method as recited in claim 19, comprising:

obtaining a bond of at least 2000 mJ/m^2.

23. A method as recited in claim 1, comprising:

forming a bond of at least 500 mJ/m^2.

24. A method as recited in claim 1, comprising:

obtaining a bond of at least 1000 mJ/m^2.

25. A method as recited in claim 1, comprising:

obtaining a bond of at least 2000 mJ/m^2.

26. A method as recited in claim 1, comprising:

forming chemical bonds between said bonding surfaces.

27. A method as recited in claim 26, comprising:

forming chemical bonds between said bonding surfaces in one of ambient and vacuum.

28. A method as recited in claim 26, comprising:

forming chemical bonds between said bonding surfaces in one of low and ultra high and vacuum.

29. A method as recited in claim 1, comprising:

forming a bond of sufficient energy to virtually eliminate wafer bowing during subsequent processing of said bonded bonding surfaces.

30. A method as recited in claim 29, comprising:

forming a bond of sufficient energy to virtually eliminate wafer bowing during subsequent thermal cycling of said bonded bonding surfaces.

31. A method as recited in claim 1, wherein said etching step comprises:

increasing available bonding energy of bonding pairs on said first and second bonding surfaces at approximately room temperature; and

propagating said bonding at room temperature.

32. A method as recited in claim 31, comprising:

propagating chemical bonding at room temperature.

33. A method as recited in claim 1, comprising:

depositing silicon dioxide as first and second bonding materials having said first and second bonding surfaces; and

etching said first and second bonding surfaces using an oxygen plasma.

34. A method as recited in claim 33, comprising:

rinsing said bonding materials in an ammonia-based solution after said etching.

35. A method as recited in claim 34, comprising:

rinsing said bonding materials in ammonium hydroxide after said etching.

36. A method as recited in claim 34, comprising:

rinsing said bonding materials in ammonium fluoride after said etching.

37. A method as recited in claim 1, comprising:

etching said first and second bonding surfaces under vacuum; and

bonding said first and second bonding surfaces without breaking said vacuum.

38. A method as recited in claim 1, comprising:

depositing a bonding material on each of first and second surfaces to obtain said first and second bonding surfaces.

39. A method as recited in claim 38, comprising:

depositing one of silicon dioxide and silicon nitride as said bonding material.

40. A method as recited in claim 1, comprising:

depositing silicon dioxide as said bonding material;

etching said silicon dioxide using one of oxygen, CF_4, and Ar plasma RIE; and

rinsing said silicon dioxide in an ammonia-based solution after said etching.

41. A method as recited in claim 1, comprising:

etching said first and second bonding materials using a wet etch process.

42. A method as recited in claim 42, comprising:

immersing said first and second bonding surfaces into a solution after said etching.

43. A method as recited in claim 1, comprising:

depositing silicon dioxide as said bonding material;

etching said silicon dioxide using one of diluted HF and diluted NH_4F.

44. A method as recited in claim 43, comprising:

rinsing said silicon dioxide in an ammonia-based solution after said etching.

45. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces as silicon; and

etching said bonding surfaces using a solution of HNO_3 and diluted HF.

46. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces as silicon each having a native oxide layer; and

activating said native oxide layer using said etching step.

47. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces each as silicon having a native oxide layer; and

exposing said first and second bonding surfaces to an oxygen plasma to etch said native oxide layers.

48. A method as recited in claim 47,

creating a defective zone in said silicon during plasma etching.

49. A method as recited in claim 1, comprising:

etching said first and second bonding materials using a plasma RIE process;

forming a region having defects proximate to said bonding surface; and

removing bonding by-products using said region.

50. A method as recited in claim 1, wherein said etching comprises:

activating said first and second bonding surfaces; and

creating a region under said first and second bonding surfaces for removing bonding by-products.

51. A method as recited in claim 1, comprising:

creating a region proximate to said first and second bonding surfaces for at least one of removal and conversion of bonding by-products to a species capable of being absorbed by or diffusing away from said bonding surfaces.

52. A method as recited in claim 1, comprising:

forming said first bonding surface by depositing an oxide layer on a first semiconductor wafer;

forming said second bonding surface by depositing an oxide layer on a second semiconductor wafer; and

bonding said first and second semiconductor wafers.

53. A method as recited in claim 1, comprising:

forming said first bonding surface as a deposited oxide layer on a first semiconductor wafer, said first wafer comprising a first substrate and a first active region;

forming said second bonding surface as a deposited oxide layer on a second semiconductor wafer, said second wafer comprising a second substrate and a second active region;

bonding said first and second semiconductor wafers; and

removing at least a substantial portion of one of said first and second substrates after said bonding.

54. A method as recited in claim 1, comprising:

forming said first bonding surface as a deposited oxide layer on a semiconductor wafer, said wafer comprising a substrate and an active region;

forming said second bonding surface as a surrogate substrate;

bonding said wafer and said surrogate substrate; and

removing at least a substantial portion of said first substrate after said bonding.

55. A method as recited in claim 1, wherein said bonding comprises:

maintaining contact between said first and second bonding surfaces for a specified period to produce bonding polymerization and allow removal of by-products.

56. A method as recited in claim 55, comprising:

maintaining said contact between said first and second bonding surfaces for a period less than about 20 hours.

57. A method as recited in claim 1, wherein said bonding comprises:

maintaining said first and second bonding surfaces for a specified period in ambient to remove bonding by-products.

58. A method as recited in claim 1, comprising:

etching said first and second bonding surfaces using a bonding fixture under vacuum;

bonding said first and second bonding surfaces using said fixture to bring together said first and second bonding surfaces while maintaining said vacuum.

59. A method as recited in claim 1, comprising:

forming a first oxide layer on a first wafer containing electrical devices; and

polishing said first oxide layer to form said first bonding surface.

60. A method as recited in claim 59, comprising:

forming a second oxide layer on a second wafer containing electrical devices; and

polishing said second oxide layer to form said second bonding surface.

61. A method as recited in claim 60, comprising:

forming said first oxide layer on said first wafer containing electrical devices of a first technology; and

forming said second oxide layer on said second wafer containing electrical devices of a second technology different from said first technology.

62. A method as recited in claim 60, comprising:

interconnecting said first and second devices.

63. A method as recited in claim 60, comprising:

forming said first bonding surface on a surface of a one of a thermal spreader, surrogate substrate, antenna, wiring layer, and pre-formed multi-layer interconnect.

64. A method as recited in claim 60, comprising:

forming said second bonding surface on a surface of a one of a thermal spreader, surrogate substrate, antenna, wiring layer, and pre-formed multi-layer interconnect.

65. A method as recited in claim 1, comprising:

forming said first bonding surface on a first wafer containing a first integrated circuit.

66. A method as recited in claim 65, comprising:

forming said second bonding surface on a second wafer containing a second integrated circuit.

67. A method as recited in claim 66, comprising:

forming said first bonding surface on said first wafer containing said first integrated circuit of a first technology; and

forming said second bonding surface on said second wafer containing said second integrated circuit of a second technology different from said first technology.

68. A method as recited in claim 66, comprising:

interconnecting said first and second integrated circuits.

69. A method as recited in claim 1, comprising:

said first and second bonding surfaces being substantially planar.

70. A method as recited in claim 1, wherein:

forming said first and second bonding surfaces comprises depositing a dielectric material.

71. A method as recited in claim 70, comprising:

polishing said dielectric material to a desired planarity and surface roughness.

72. A method as recited in claim 70, comprising:

depositing said dielectric material on a non-planar surface.

73. A method as recited in claim 72, wherein:

said polishing comprises chemical-mechanical polishing.

74. A method as recited in claim 1, comprising:

forming said first and second bonding surfaces to be non-planar; and

polishing said first and second bonding surfaces to a desired planarity and surface roughness

75. A method as recited in claim 74, wherein:

said polishing comprises chemical-mechanical polishing.

76. A method as recited in claim 1, where said etching comprises:

activating said bonding surfaces; and

terminating said bonding surfaces with a desired species.

77. A method as recited in claim 1, wherein said etching comprises:

a first etching step to activate said bonding surfaces; and

a second etching step to terminate said bonding surfaces with a desired species.

78. A method as recited in claim 1, comprising:

obtaining etched bonding surfaces using said etching step; and

exposing said bonding surfaces to a gaseous chemical environment to terminate said etched bonding surfaces with a desired species.

79. A method as recited in claim 1, comprising:

forming a first oxide layer on a first wafer containing electrical devices and having a non-planar surface; and

forming a second oxide layer on a second wafer containing electrical devices; and

polishing said first and second oxide layers to form said first and second bonding surfaces, respectively.

80. A method as recited in claim 79, comprising:

forming said second oxide layer on said second wafer having a non-planar surface.

81. A method as recited in claim 1, comprising:

forming a first oxide layer on a first wafer containing electrical devices and having an irregular surface topology; and

forming a second oxide layer on a second wafer containing electrical devices; and

polishing said first and second oxide layers to form said first and second bonding surfaces, respectively.

82. A method as recited in claim 81, comprising:

forming said second oxide layer on said second wafer having an irregular surface topology.

83. A bonding method, comprising:

forming first and second bonding surfaces each having a surface roughness in a range of 0.1 to 3 nm;

removing material from said first and second bonding surfaces while maintaining said surface roughness; and

directly bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 500 mJ/m^2.

84. A method as recited in claim 83, comprising:

directly bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 1000 mJ/m^2.

85. A method as recited in claim 83, comprising:

directly bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 2000 mJ/m^2.

86. A method as recited in claim 83, comprising:

activating said first and second bonding surfaces and forming selected bonding groups on said first and second bonding surfaces.

87. A method as recited in claim 83, comprising:

polishing respective first and second bonding surfaces to said surface roughness; and

etching said first and second bonding surfaces after said polishing to activate said first and second bonding surfaces.

88. A method as recited in claim 83, comprising:

converting bonding by-products to a species capable of being absorbed by or diffusing away from said bonding surfaces during said bonding step.

89. A method as recited in claim 83, comprising:

etching said first and second bonding surfaces using a plasma RIE process;

forming a subsurface layer having defects; and

removing bonding by-products using said subsurface layer.

90. A method as recited in claim 83, comprising:

forming said first bonding surface as a surface of a first semiconductor wafer having devices formed therein; and

forming said second bonding surface as a surface of a second semiconductor wafer having devices formed therein.

91. A method as recited in claim 90, comprising:

removing a substantial portion of said one of said first and second wafers.

92. A method as recited in claim 90, comprising:

interconnecting devices in said first and second wafers.

93. A method as recited in claim 83, comprising:

forming a first insulating layer on a first wafer containing electrical devices;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices; and

polishing said second oxide layer to form said second bonding surface.

94. A method as recited in claim 83, comprising:

forming a first insulating layer on a first wafer containing electrical devices and having an irregular surface topology;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices and having an irregular surface topology; and

polishing said second oxide layer to form said second bonding surface.

95. A bonding method, comprising:

forming first and second bonding surfaces;

etching said first and second bonding surfaces;

terminating said first and second bonding surfaces with a species allowing formation of chemical bonds at about room temperature; and

bonding said first and second bonding surfaces at about room temperature.

96. A method as recited in claim 95, comprising:

bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 500 mJ/m^2.

97. A method as recited in claim 95, comprising:

bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 1000 mJ/m^2.

98. A method as recited in claim 95, comprising:

bonding said first and second bonding surfaces at room temperature with a bonding strength of at least 2000 mJ/m^2.

99. A method as recited in claim 95, comprising:

activating said first and second bonding surfaces prior to said bonding step.

100. A method as recited in claim 95, comprising:

polishing said first and second bonding surfaces; and

etching said first and second bonding surfaces after said polishing to activate said first and second bonding surfaces.

101. A method as recited in claim 95, comprising:

converting bonding by-products to a species capable of being absorbed by or diffusing away from said bonding surfaces during said bonding step.

102. A method as recited in claim 95, comprising:

forming said first bonding surface as a surface of a first semiconductor wafer having devices formed therein; and

forming said second bonding surface as a surface of a second semiconductor wafer having devices formed therein.

103. A method as recited in claim 102, wherein one of said first and second wafers comprises a substrate, said method comprising:

removing a substantial portion of said one of said first and second wafers.

104. A method as recited in claim 102, comprising:

interconnecting devices in said first and second wafers.

105. A method as recited in claim 95, comprising:

forming a first insulating layer on a first wafer containing electrical devices;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices; and

polishing said second oxide layer to form said second bonding surface.

106. A method as recited in claim 95, comprising:

forming a first insulating layer on a first wafer containing electrical devices and having an irregular surface topology;

polishing said first insulating layer to form said first bonding surface;

forming a second insulating layer on a second wafer containing electrical devices and having an irregular surface topology; and

polishing said second oxide layer to form said second bonding surface.

107. A bonded device, comprising:

a first material having a first etched bonding surface; and

a second material having a second etched bonding surface directly bonded to said first bonding surface at room temperature having a bonding strength of at least 500 to 2000 mJ/m^2.

108. A device as recited in claim 107, comprising:

said first and second bonding surfaces being activated and terminated with a desired bonding species.

109. A device as recited in claim 108, wherein said desired species comprise:

a monolayer of one of a desired atom and a desired molecule on said bonding surface.

110. A device as recited in claim 108, wherein said desired species comprise at least one of a silanol group, an NH_2 group, a fluorine group and an HF group.

111. A device as recited in claim 107, comprising:

said first and second bonding surfaces each having a defective region located proximate to said first and second bonding surfaces, respectively.

112. A device as recited in claim 107, wherein:

said first material comprises a surface of a first semiconductor wafer having devices formed therein; and

said second material comprises a surface of a second semiconductor wafer having devices formed therein.

113. A device as recited in claim 112, wherein one of said first and second wafers comprises a device region after removing a substantial portion of a substrate of said one of said first and second wafers.

114. A device as recited in claim 112, comprising:

devices in said first and second wafers being interconnected.

115. A device as recited in claim 112, comprising:

said first and second wafers being different technologies.

116. A device as recited in claim 107, wherein:

one of said first and second wafers comprises an integrated circuit.

117. A device as recited in claim 116, comprising:

devices in said first and second wafers being interconnected.

118. A device as recited in claim 116, comprising:

said first and second wafers having an irregular surface topology.

119. A device as recited in claim 107, wherein:

said first material comprises a first wafer containing electrical devices and having a first non-planar surface; and

said first bonding surface comprises a polished and etched deposited oxide layer on said first non-planar surface.

120. A device as recited in claim 119, wherein:

said second material comprises a second wafer containing electrical devices and having a second non-planar surface; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second non-planar surface.

121. A method as recited in claim 107, wherein:

said first material comprises a first wafer containing electrical devices and having a first surface with irregular topology; and

said first bonding surface comprises a polished, planarized and etched deposited oxide layer on said first surface.

122. A method as recited in claim 121, comprising:

said second material comprises a second wafer containing electrical devices and having a second surface with irregular topology; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second surface.

123. A bonded device, comprising:

a first material having a first etched and activated bonding surface terminated with a first desired bonding species; and

a second material having a second etched and activated bonding surface terminated with a second desired bonding species bonded to said first bonding surface at room temperature.

124. A device as recited in claim 123, wherein said species comprise at least one of a silanol group, an NH_2 group, a fluorine group and an HF group.

125. A device as recited in claim 123, comprising:

said first and second bonding surfaces each having a defective region located proximate to said surfaces.

126. A device as recited in claim 123, wherein said desired species comprises:

a monolayer of one of a desired atom and a desired molecule on said bonding surface.

127. A device as recited in claim 123, comprising:

said second bonding surface bonded to said first bonding surface at room temperature having a bonding strength of at least 500 to 2000 mJ/m^2.

128. A device as recited in claim 123, wherein:

said first bonding surface comprises a surface of a first semiconductor wafer having devices formed therein; and

said second bonding surface comprises a surface of a second semiconductor wafer having devices formed therein.

129. A device as recited in claim 128, wherein one of said first and second wafers comprises a device region after removing a substantial portion of a substrate of said one of said first and second wafers.

130. A device as recited in claim 123, comprising:

devices in said first and second wafers being interconnected.

131. A device as recited in claim 123, comprising:

said first and second wafers being different technologies.

132. A device as recited in claim 123, wherein:

one of said first and second wafers comprises an integrated circuit.

133. A device as recited in claim 123, comprising:

devices in said first and second wafers being interconnected.

134. A device as recited in claim 123, wherein:

said first material comprises a first wafer containing electrical devices and having a first non-planar surface; and

said first bonding surface comprises a polished and etched deposited oxide layer on said first non-planar surface.

135. A device as recited in claim 134, wherein:

said second material comprises a second wafer containing electrical devices and having a second non-planar surface; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second non-planar surface.

136. A method as recited in claim 123, wherein:

said first material comprises a first wafer containing electrical devices and having a first surface with irregular topology; and

said first bonding surface comprises a polished, planarized and etched deposited oxide layer on said first surface.

137. A method as recited in claim 123. wherein:

said second material comprises a second wafer containing electrical devices and having a second surface with irregular topology; and

said second bonding surface comprises a polished, planarized and etched deposited oxide layer on said second surface.

138. A method as recited in claim 1, wherein said first and second bonding surfaces are respective surfaces of first and second substrates, the method comprising:

removing a substantial portion of one of said first and second substrates.

139. A method as recited in claim 138, comprising:

annealing said bonded substrates after said removing step.

140. A method as recited in claim 138, wherein said first and second substrates have

first and second electrical devices, the method comprising:

interconnecting said first and second devices after said removing step.

141. A method as recited in claim 91, comprising:

annealing said bonded substrates after said removing step.

142. A method as recited in claim 91, comprising:

interconnecting devices in said first and second semiconductor wafers after said removing step.

143. A method as recited in claim 103, comprising:

annealing said bonded substrates after said removing step.

144. A device as recited in claim 113, wherein:

said device region comprises an annealed device region.

145. A device as recited in claim 129, wherein;

said first and second materials comprise respective first and second substrates; and

one of said first and second substrates comprises a substrate region obtained by removing a substantial portion of a substrate of said one of said first and second substrate.

146. A device as recited in claim 145, wherein:

said substrate region comprises an annealed substrate region.

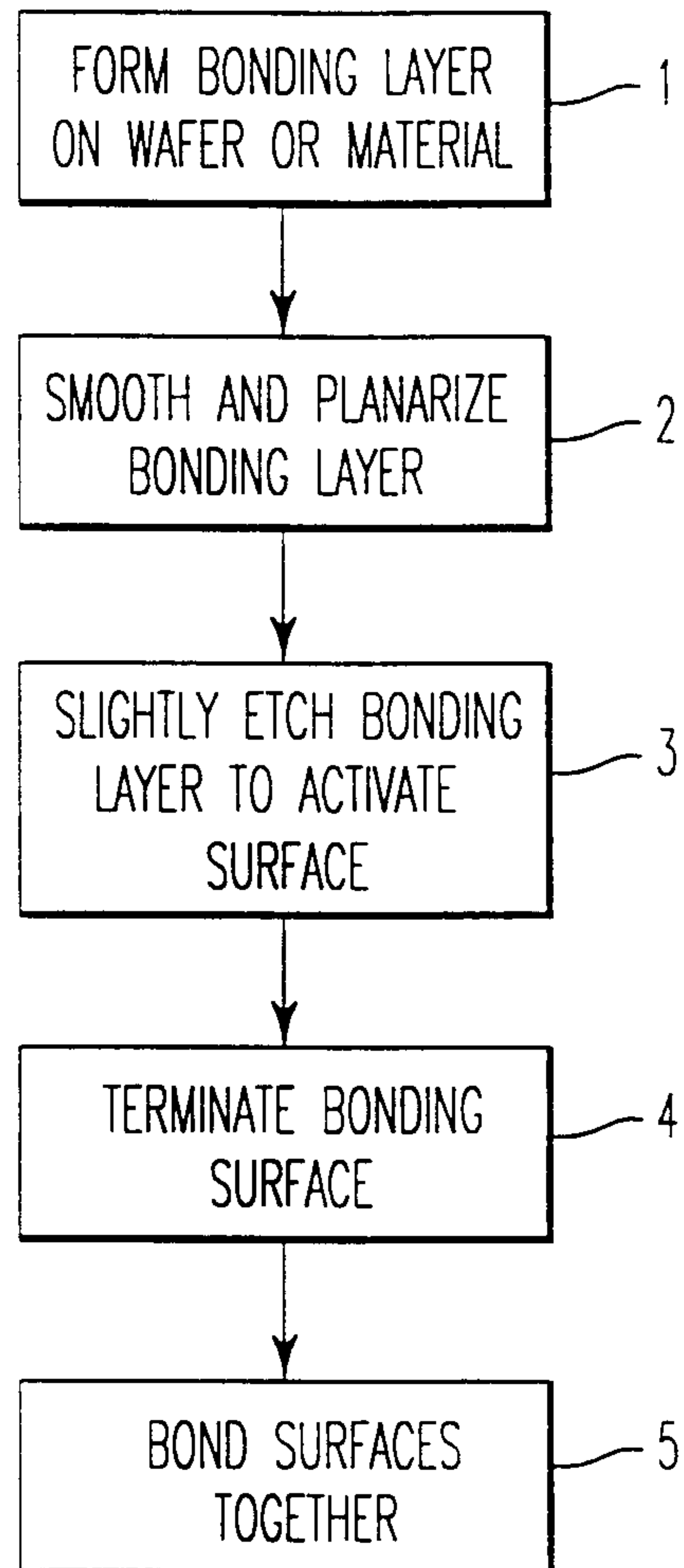


FIG. 1

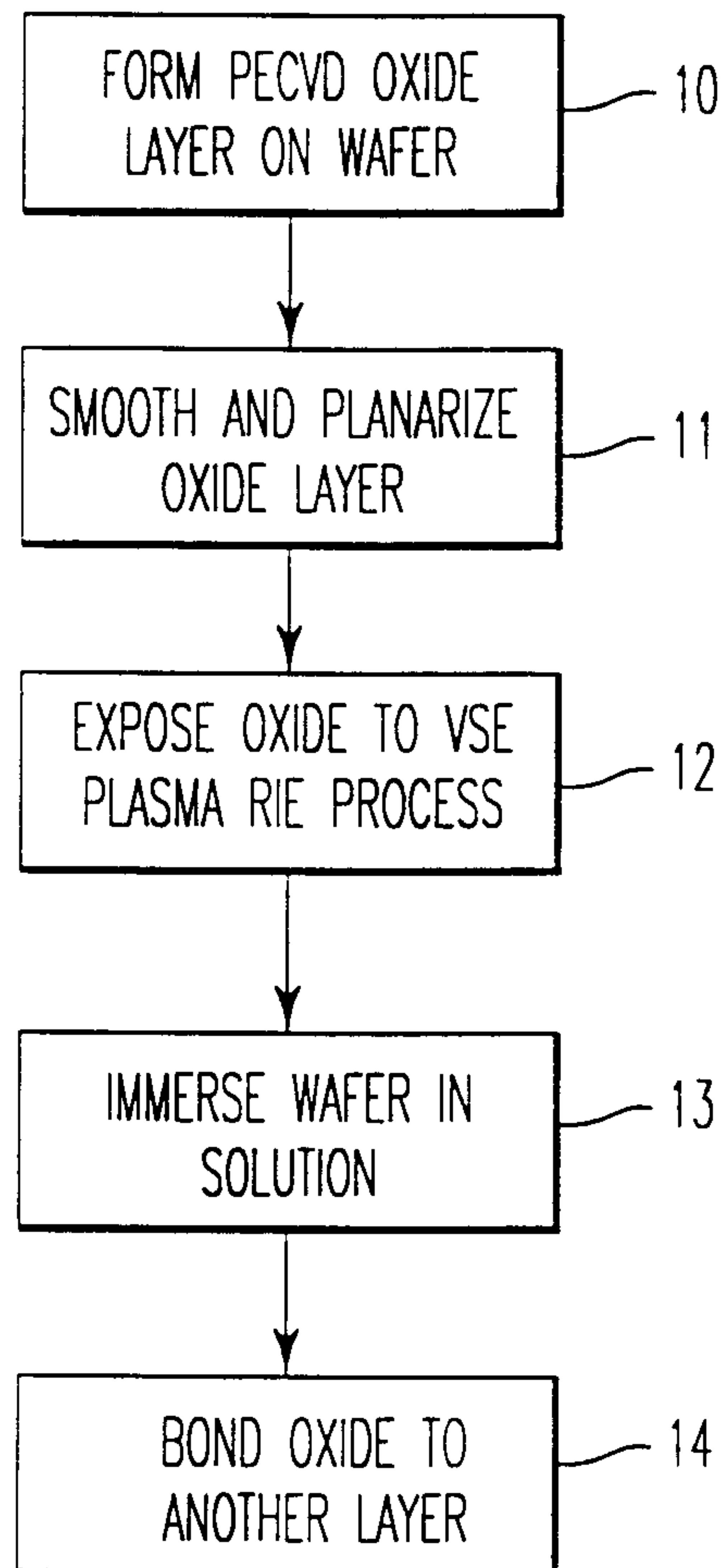


FIG. 2

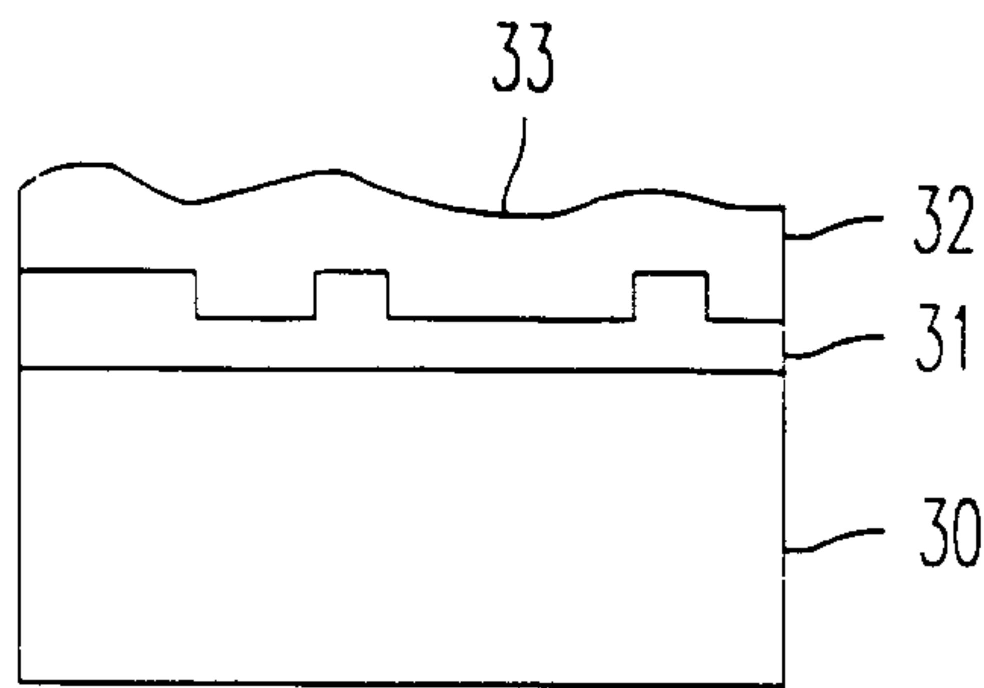


FIG. 3A

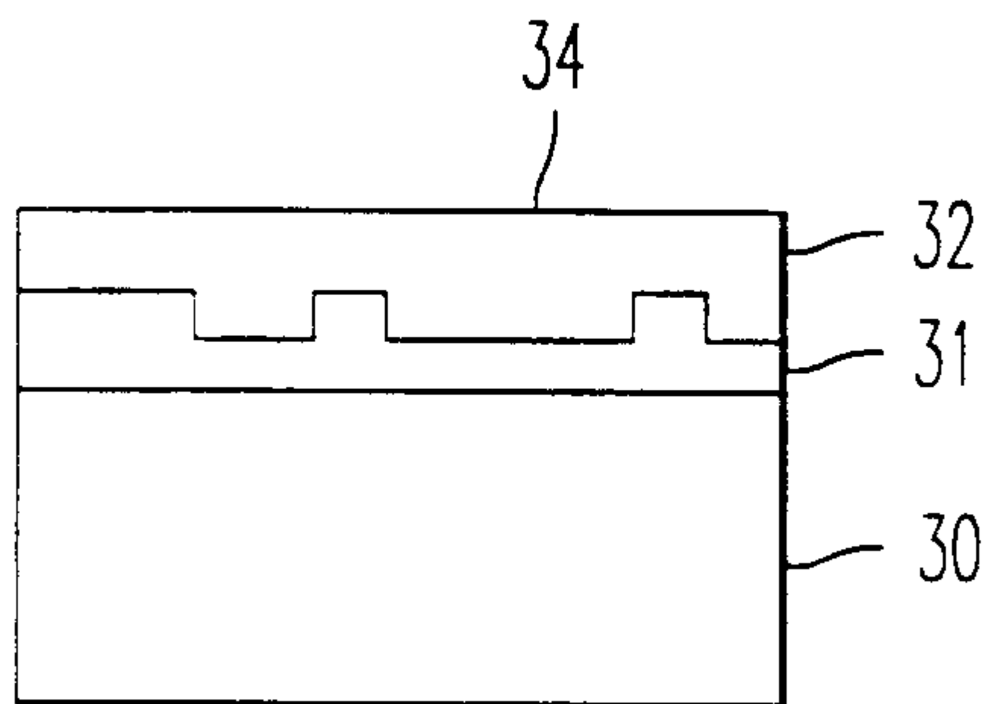
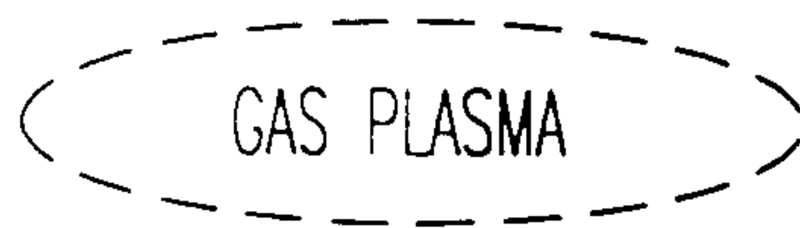


FIG. 3B



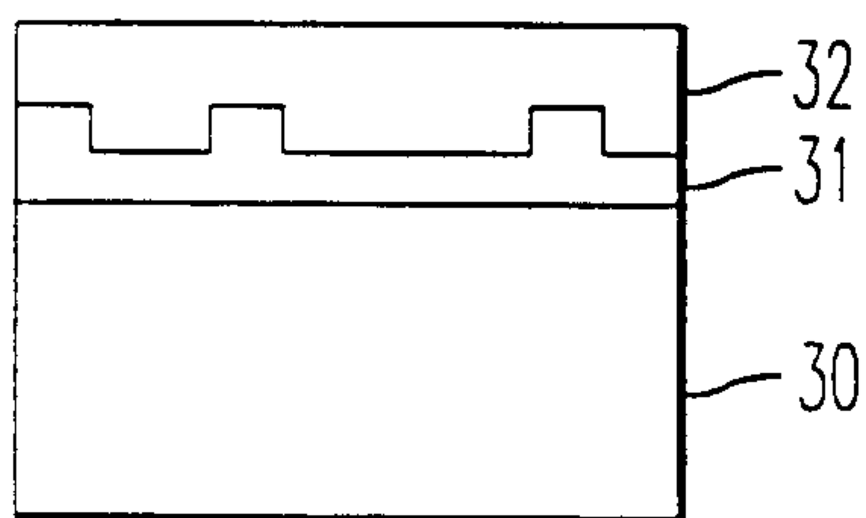


FIG. 3C

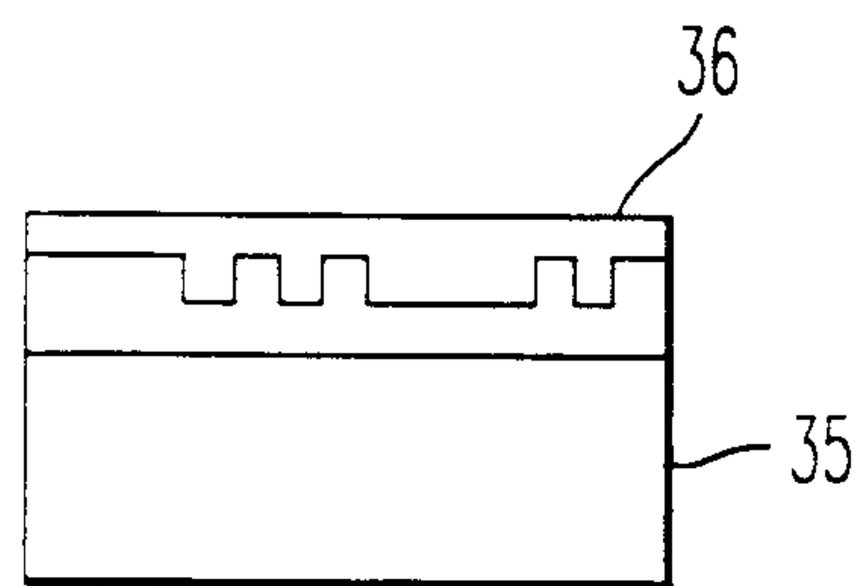


FIG. 3D

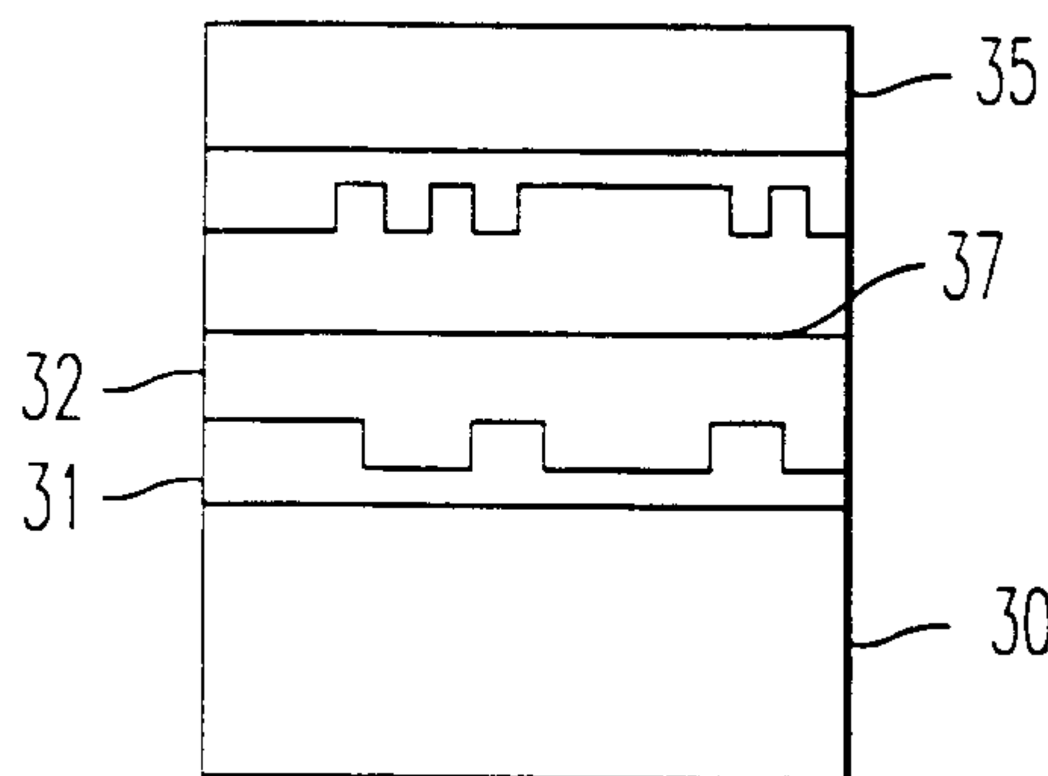


FIG. 3E

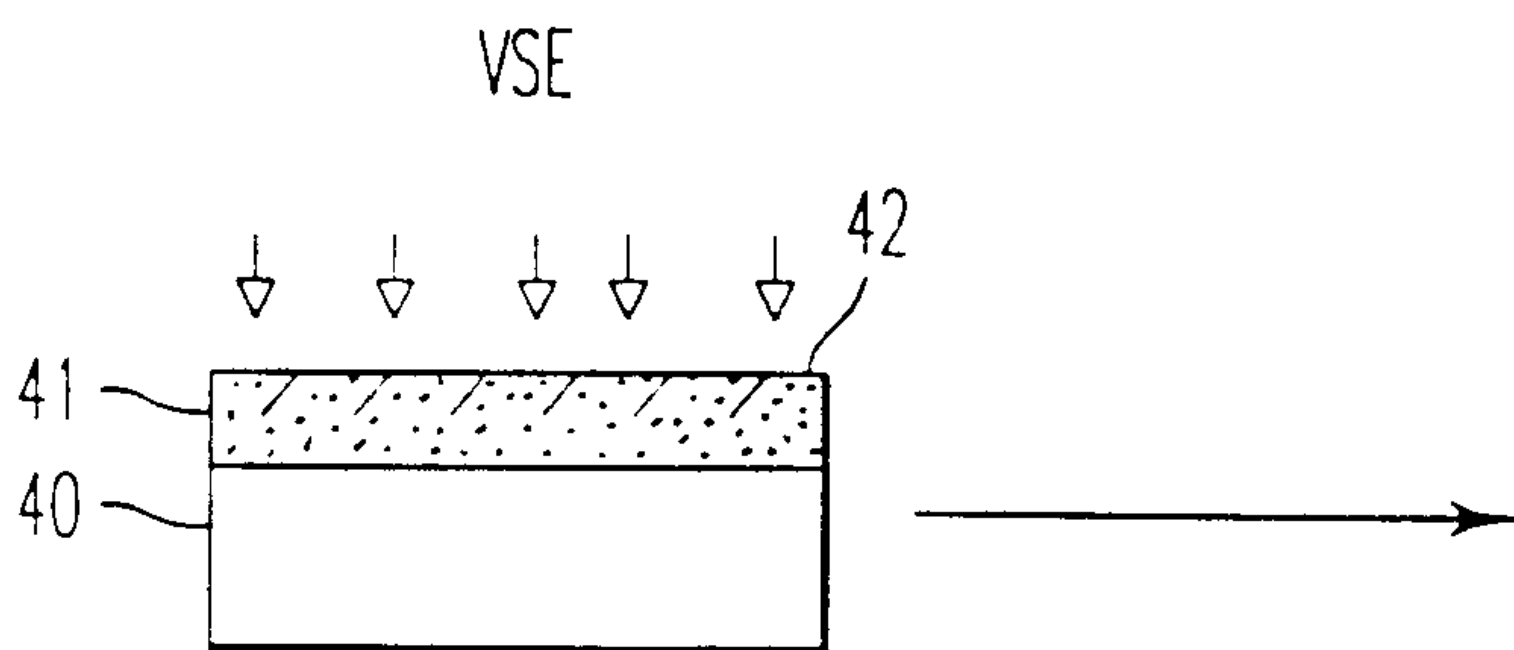


FIG. 4A

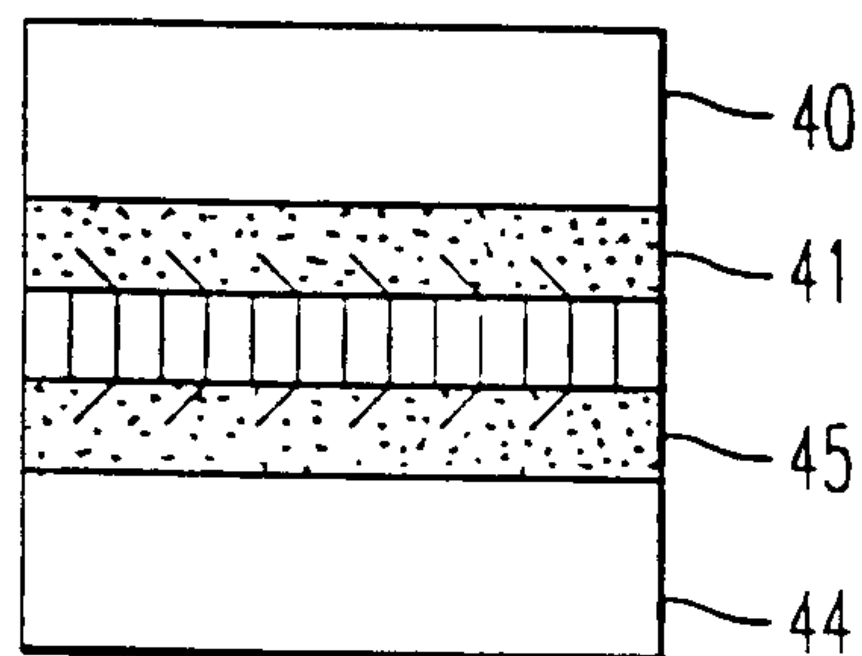


FIG. 4D

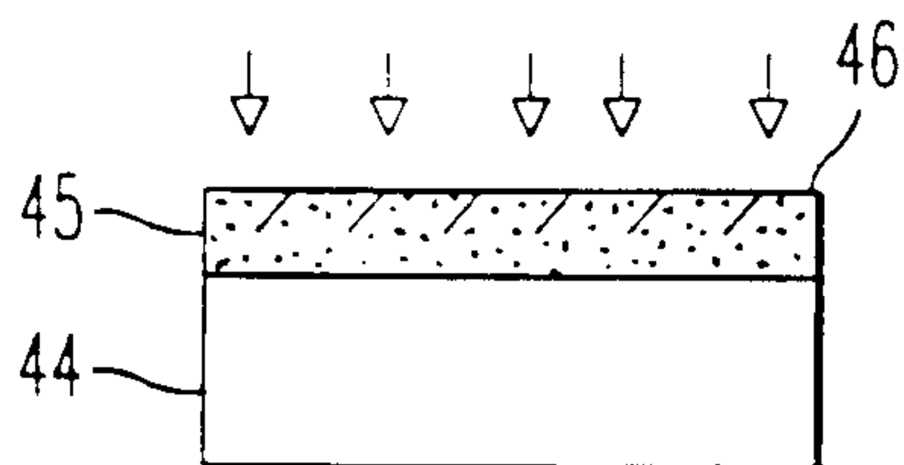


FIG. 4B

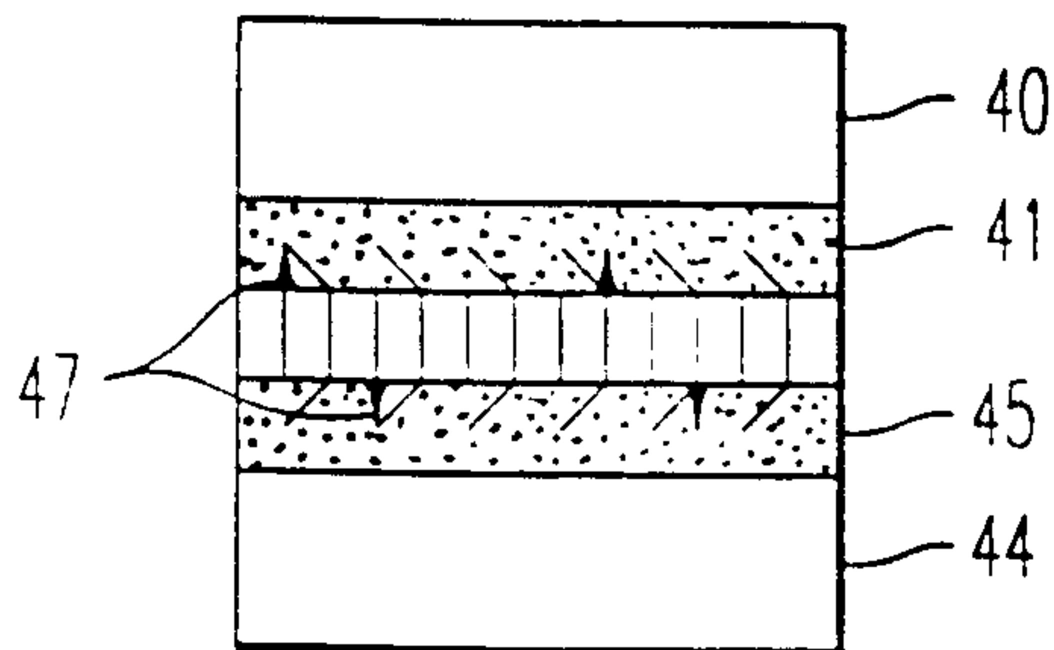


FIG. 4E

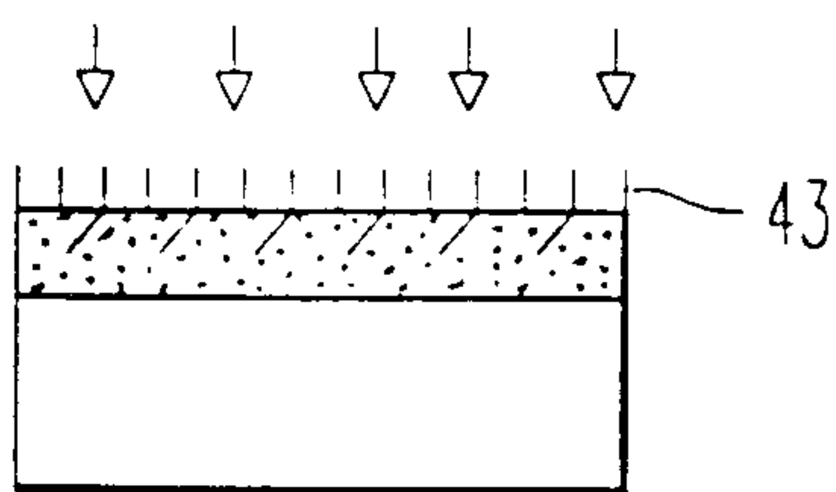


FIG. 4C

VSE

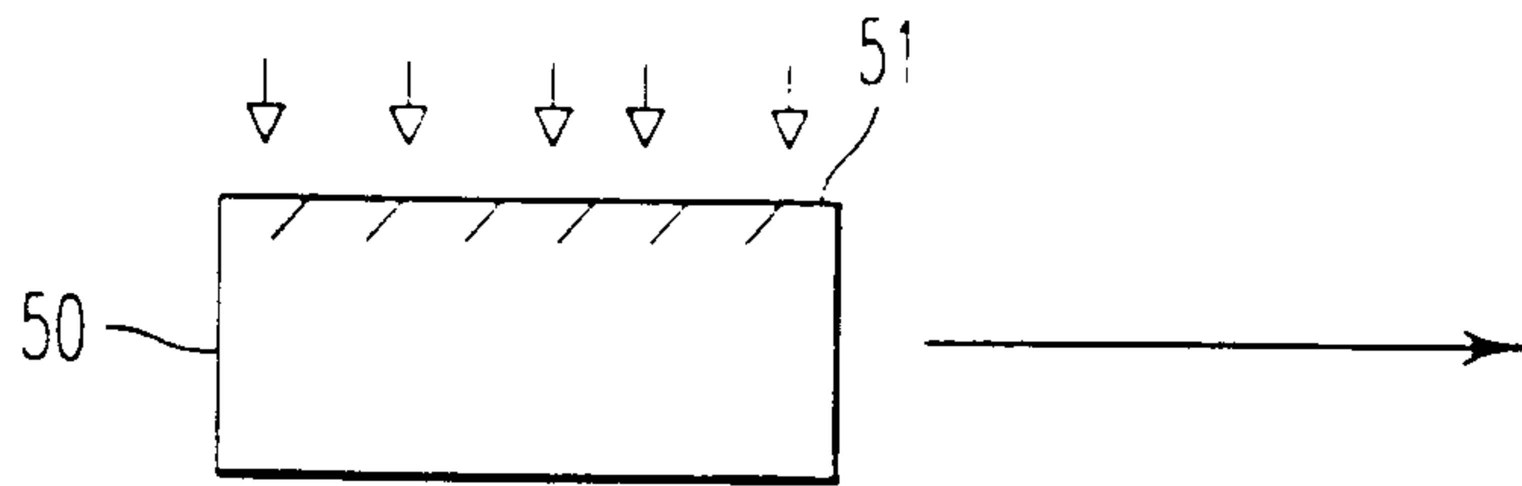


FIG. 5A

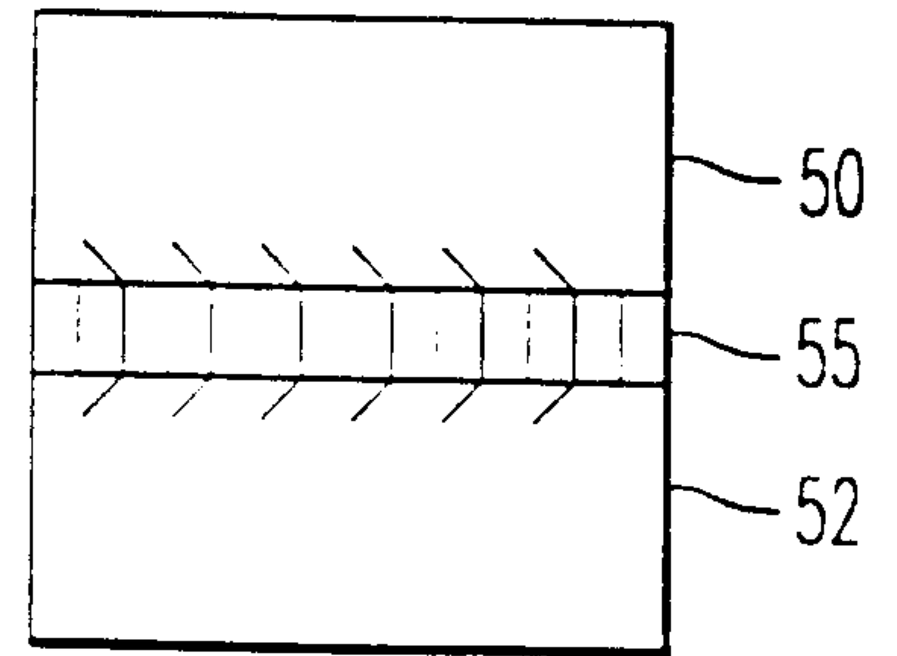


FIG. 5D

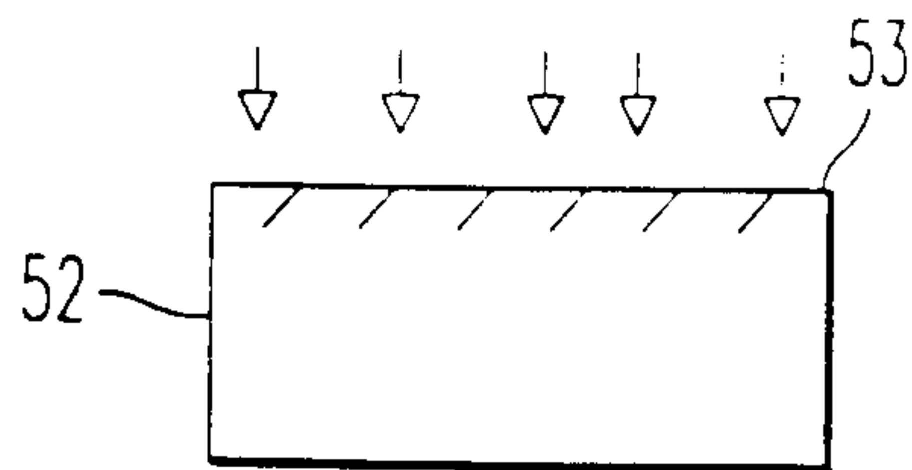


FIG. 5B

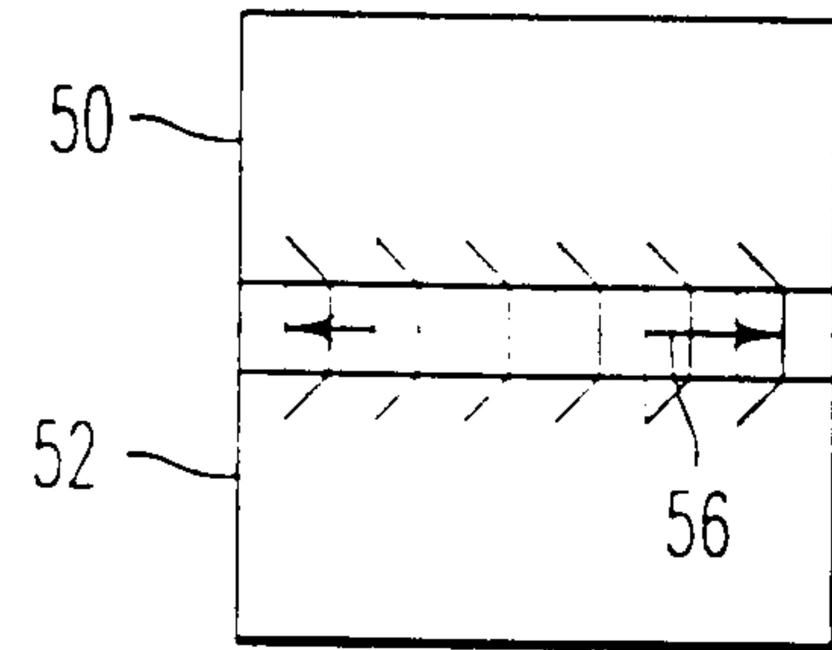


FIG. 5E

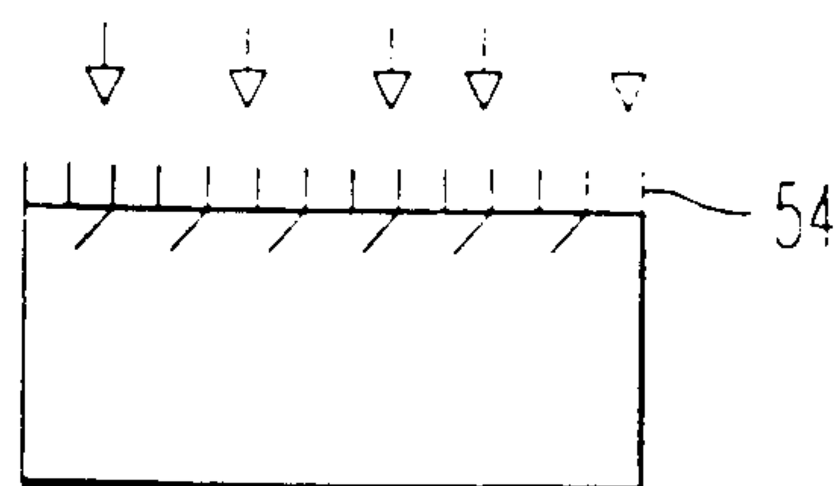


FIG. 5C

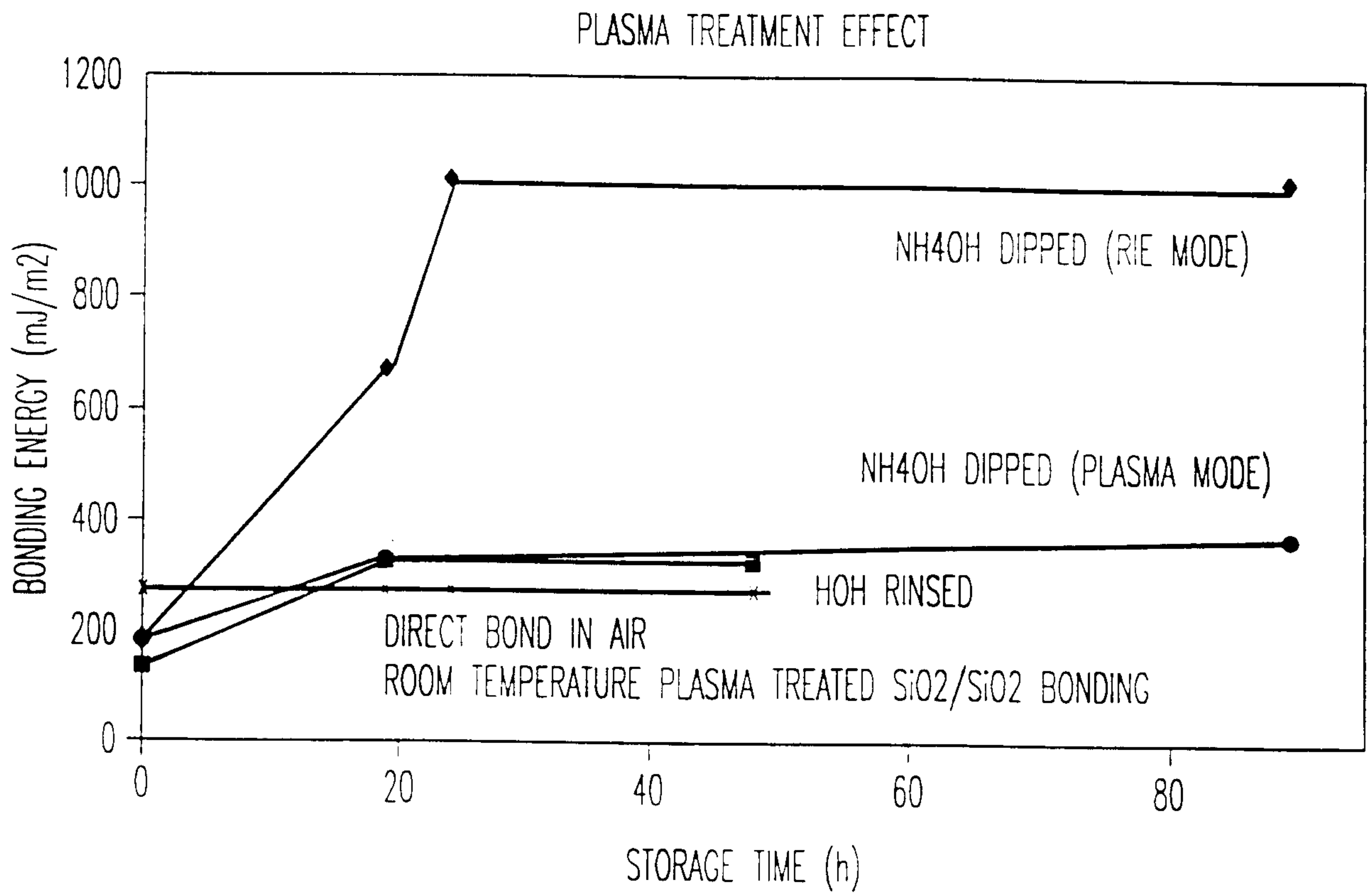


FIG. 6A

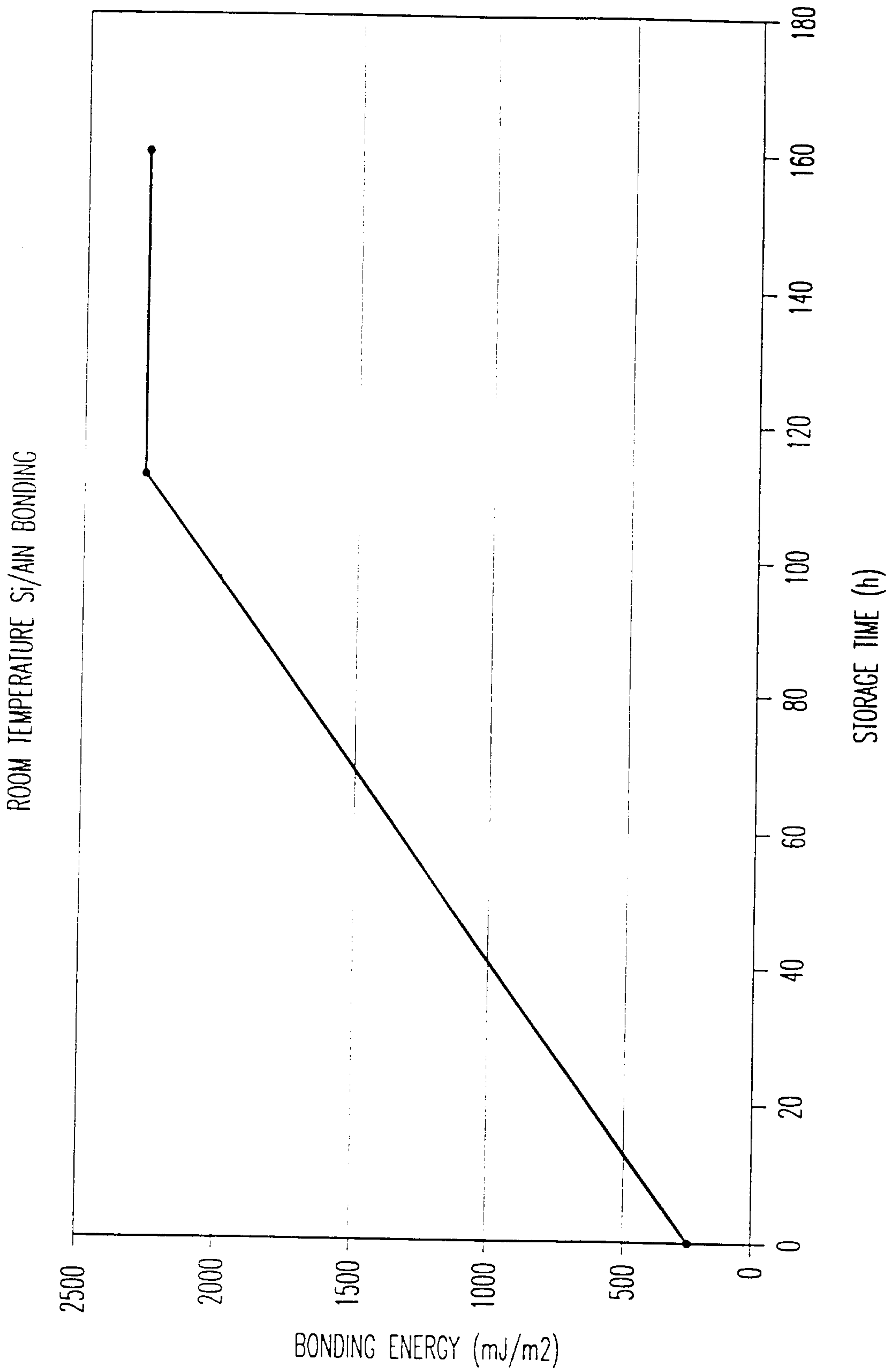


FIG. 6B

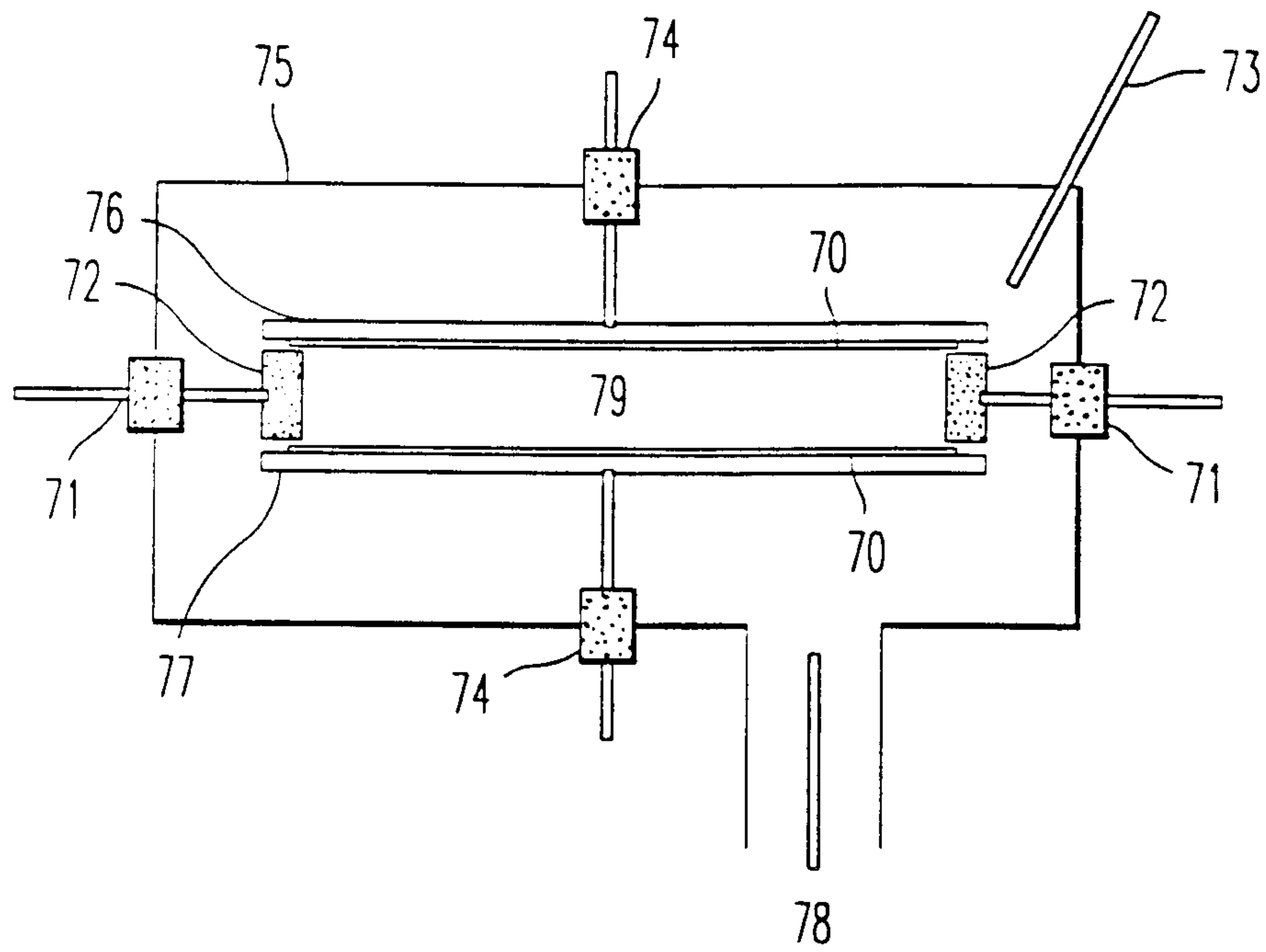


FIG. 7

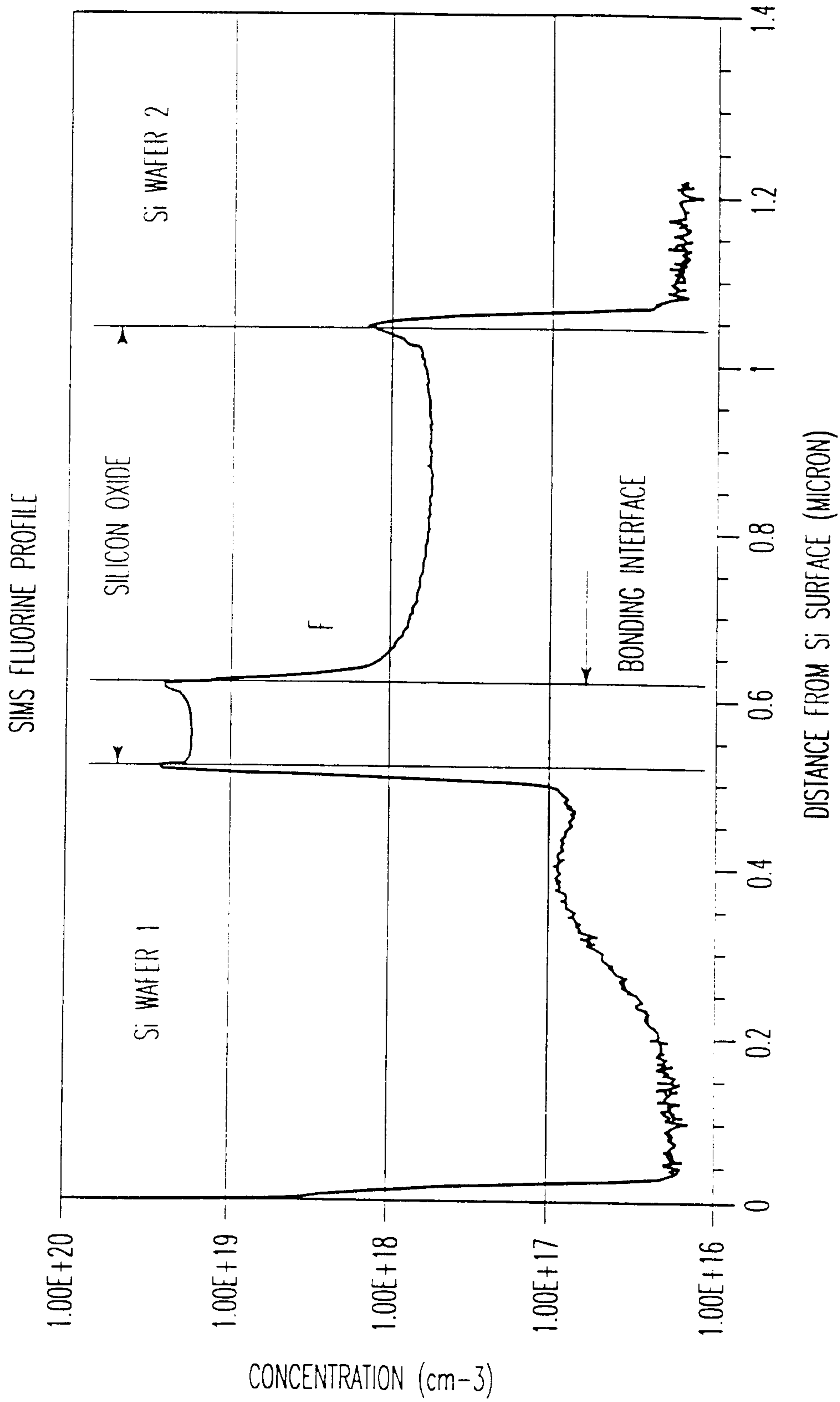
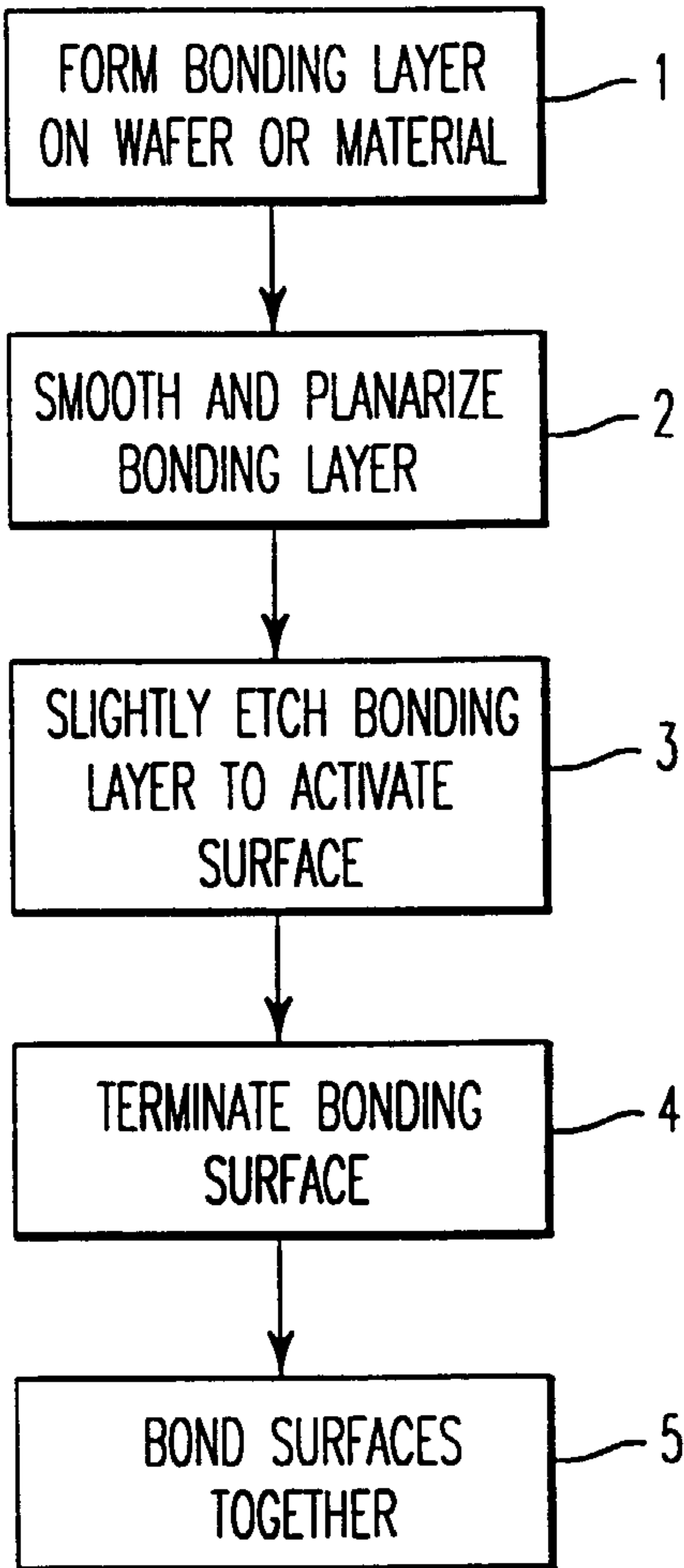


FIG. 8


FORM BONDING LAYER ON WAFER OR MATERIAL
1
SMOOTH AND PLANARIZE BONDING LAYER
2
SLIGHTLY ETCH BONDING LAYER TO ACTIVATE SURFACE
3
TERMINATE BONDING SURFACE
4
BOND SURFACES TOGETHER
5