

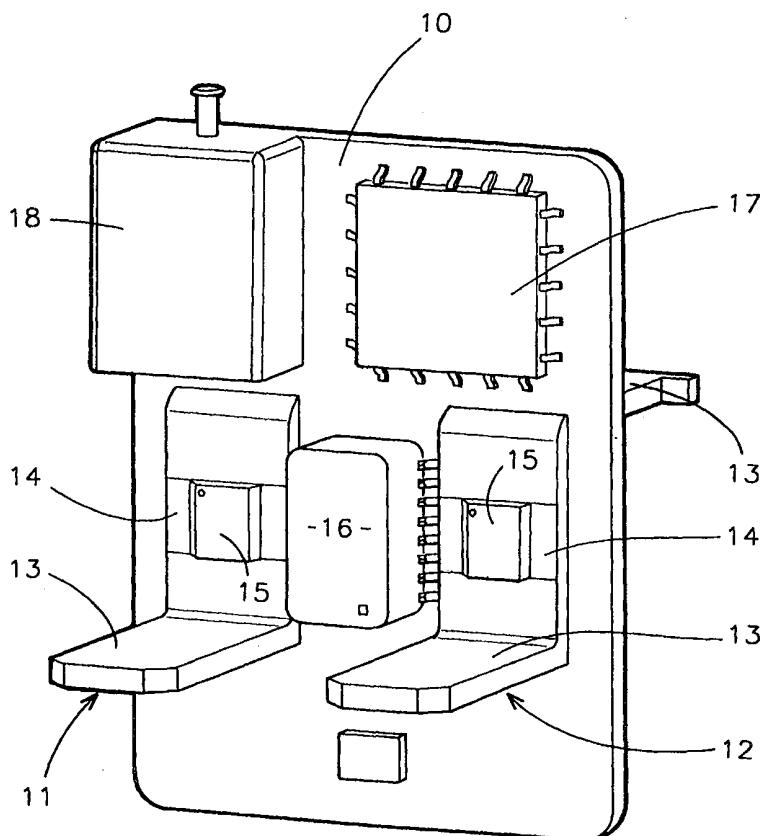


INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G01R 19/00	A1	(11) International Publication Number: WO 00/00834 (43) International Publication Date: 6 January 2000 (06.01.00)
(21) International Application Number: PCT/GB99/02060 (22) International Filing Date: 30 June 1999 (30.06.99) (30) Priority Data: 9813982.7 30 June 1998 (30.06.98) GB (71) Applicant (for all designated States except US): MEM LIMITED [GB/GB]; Turkey Shore, Holyhead, Anglesey, Gwynedd LL65 2DH (GB). (72) Inventors; and (75) Inventors/Applicants (for US only): SKERRITT, Robert, Charles [GB/GB]; 2 Charleston Close, Penrhyn Bay, Conwy LL30 3HX (GB). CROSIER, Mark, David [GB/GB]; 4 Sunrise Terrace, Gors Avenue, Holyhead, Isle of Anglesey LL65 1PD (GB). MURRAY, Martin, Anthony [GB/GB]; 47 Penrhos Road, Bangor LL57 2AX (GB). REEDER, Brian, Martin [GB/GB]; 'Samona', Lon Cre Crist, Trearddur Bay, Isle of Anglesey LL65 2AZ (GB). (74) Agents: CARPENTER, David et al.; Marks & Clerk, Alpha Tower, Suffolk Street Queensway, Birmingham B1 1TT (GB).		(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i>

(54) Title: RESIDUAL CURRENT DETECTION DEVICE**(57) Abstract**

A residual current detection device comprising a plurality of resistive shunts for connection in respective ones of a plurality of lines through which current can flow to and from a load, and detector means sensitive to the voltage developed across each of the shunts to detect any imbalance between the currents flowing through the shunts.



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Residual Current Detection Device

This invention relates to a residual current correction device for use in a circuit breaker.

Conventionally, residual current is detected utilising a current transformer having primary windings through which, in the case of a single phase device, load current flows in opposite directions so that if the return current is different from the outwardly flowing current because of current leakage an output current signal is induced in a secondary winding of the transformer. In the case of a multi-phase device, primary windings of the transformer are connected in all of the phase lines and the neutral line. In normal situations, when there is no current leakage, the net current induced in the secondary winding is zero and therefore no output is detected.

Sophisticated materials have been developed for the core of the current transformer, which enable considerable accuracy to be obtained when the currents flowing in the primary windings are substantially sinusoidal. However, switch mode power supplies are often used for computers and other equipment and there is an increasing tendency for such equipment to cause dc offsets in the currents. Such developments have made detectors utilising current transformers less reliable and prone to false tripping or failure to detect a dc current leakage.

This is a particular problem in the case of directly actuated electro-mechanical devices, where the current transformer secondary winding actually drives an actuator. The situation is not much improved, when including an electronic detection and amplification means connected to the secondary winding, as there are still problems with high frequency

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transients and dc offsets. A very small dc current level can cause the core to saturate thereby seriously impairing the ability of the detector to detect current leakage.

It is an object of the present invention to provide a residual current detection device in which the above mentioned problems are substantially overcome in a simple and efficacious manner.

In accordance with the invention there is provided a residual current detection device comprising a plurality of resistive shunts for connection in respective ones of a plurality of lines through which current can flow to and from a load, and detector means sensitive to the voltage developed across each of the shunts to detect any imbalance between the currents flowing through the shunts.

Preferably, the detector means comprises an analog to digital converter for each shunt and a processor for receiving the digital signals from the converters and determining whether a current imbalance exists.

Each shunt preferably takes the form of a composite strip having conductive portions at its ends and a resistive portion interconnecting the conductive portions. Such composite strips can be mass produced inexpensively to very high tolerances which makes them extremely suitable for this purpose.

The analog to digital converter for each shunt may include a delta-sigma modulator, which generates a high frequency single digital data stream which is converted by decimation filtering to a multibit digital data stream at a lower frequency.

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The analog to digital converter for each shunt is preferably connected to the processor through an isolation barrier so that the converter can float at the voltage level of the shunt which it serves. The decimation filtering may be effected entirely in the converter, entirely in the processor or split between the converter and the processor.

In the accompanying drawings:

Figure 1 is a diagrammatic perspective view of an example of the invention as applied to a single phase device,

Figure 2 is a block diagram of an another example of the invention as applied to a three phase device,

Figure 3 is a perspective view showing one of the current sensing devices,

Figure 4 is a sectional view of the current sensing device of Figure 3,

Figure 5 is an elevation of the device of Figure 3,

Figure 6 is a block diagram of a simple form of the electronic circuit of a single current sensor device,

Figure 7 is a block diagram of an alternative form of the electronic circuit, and

Figure 8 is a block diagram of yet another form of the electronic circuit.

In the device shown in Figure 1, a substrate 10 supports two composite conductor strips 11, 12. Each of these includes end portions 13 of copper

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and an intermediate portion 14 of a resistive material such as manganin. The strips are formed by slicing up a sandwich formed by electron beam welding the copper portions to opposite sides of the manganin portion. The shunts formed by the resistive portions manufactured by this method can have a nominal resistance of $0.2\text{m}\Omega$ to a tolerance of less than 5%. If the two shunts 14 used on one device are pressed from adjacent portions of the sandwich stock, they are matched to within 2%. Calibration of the shunts built into a unit at two different temperatures can virtually eliminate shunt errors.

In the example shown in Figure 1, there is a separate signal pre-processing ASIC 15 mounted on each of the shunts 14 and connected to the copper end portions 13 of the associated conductor strips. The two ASICs 15 are connected to via an isolation transformer array 16 to a main processor 17. The ASICs 15 operate to convert the two voltages across the shunts into a digital signal stream which is communicated to the processor 17 via the isolation transformer array. The main processor is programmed to provide a drive signal to a trip actuator 18.

The actual preferred structural configuration of the sensors is shown in Figures 3 to 5. These show leads 40 connecting two analog input terminals of the ASIC to the two copper end portions. Other leads connect other terminals of the ASIC 15 to a lead frame by means of which all other external connections are made. Figure 5 shows in dotted lines a block 42 of encapsulation material and Figure 4 shows an electrically insulative adhesive layer 41 by means of which the ASIC is attached to the intermediate portion 14 of the composite strip 14, 15.

Figure 2 shows in rather more electrical detail a three phase device. In this case there are four shunts 14, one in each phase line and a fourth in

the neutral line. The ASICs 15 of Figure 1 are shown as four separate blocks 20, 21, 22, and 23, and there is a power supply unit 24 which draws power from the phase lines on the mains side of the shunts 14 and provides controlled voltages to the processor 17. Power is supplied to the four blocks 20 to 23 via isolation barriers 25 which make up the array 16.

Each block of the ASIC includes an analog to digital converter in the form of a delta-sigma modulator which provides a high frequency one bit digital data stream. A multiplexer may be included in each converter so that the converter can provide to the processor, through the respective isolation barrier, signals representing both current in the associated shunt and the voltage at one end of it. The processor uses these signals to monitor the current in each shunt and to operate the actuator 18 if an imbalance occurs.

It will be noted that the voltage sensing connections to the ASICs are made via resistor chains connected between each phase line and the neutral. Each such resistor chain comprises an outer pair of precision resistors of relatively low ohmic value and an intermediate resistor of relatively high ohmic value. These resistor chains allow the RCD to be provided with an independent reference. If the neutral ADC is taken as the selected system reference, then the operating software of the main processor can use the multiple signals derived from the several resistor chains to calibrate each phase against the neutral reference.

The CPU is programmed to carry out the necessary calculations to determine the existence of an imbalance and can determine the true RMS value of the residual current, which conventional devices fail to do correctly particularly in the case of non-sinusoidal current waveforms. The CPU may be programmed to enable it to determine from the data it receives whether a particular event is, in fact, an unacceptable leakage

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more reliably than conventional devices. For example, the CPU can take into account the historic performance of the unit when setting the leakage current threshold and may ignore events which have a recognisable "signature". In this way improved tolerance to nuisance tripping can be obtained

Decimation filtering of the high frequency one bit data stream is required to reduce each data stream to a multi-bit digital signal at a predetermined sample frequency. By way of example, each current signal may be a 23-bit signal at a sample rate of 64 times the mains frequency, but lower resolution at lower sample rates can be employed when non-linear, rather than linear conversion is acceptable. The decimation filtering is typically a function of the processor, filtering of the four data streams being executed simultaneously so that sample values are derived for all four shunts simultaneously. A circuit employing such an arrangement is shown in Figure 6.

In an alternative embodiment as shown in Figure 7, one or more stages of the decimation filtration may be executed by hardware included within the ASIC. Multi-bit digital words are transmitted serially across the isolation barriers instead of a one-bit signal stream. The filtration stages may be split between the ASIC and the processor.

Where current and voltage are both to be monitored as in the system shown in Figure 2, the circuit 15 may be as shown in Figure 8 with separate modulations and filtering components for the two signal streams and a common serial interface. Alternatively separate serial interfaces may be employed.

The arrangements described enable very accurate detection of current

imbalance to be effected even in the presence of switching transients and DC offsets. The problems which arise from potential saturation of the current transformer core are avoided completely.

Since the CPU receives actual line current and voltage data from each of the blocks 20 to 23, it can be programmed to perform other calculations, such as current limit and power consumption. Thus an RCD device constructed as described above can also provide the functions of a conventional circuit breaker and/or those of a power consumption meter without any additional sensing or analog-to-digital components being required.

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CLAIMS

1. A residual current detection device comprising a plurality of resistive shunts for connection in respective ones of a plurality of lines through which current can flow to and from a load, and detector means sensitive to the voltage developed across each of the shunts to detect any imbalance between the currents flowing through the shunts.
2. A device as claimed in Claim 1, in which the detector means comprises an analog to digital converter for each shunt and a processor for receiving the digital signals from the converters and determining whether a current imbalance exists.
3. A device as claimed in Claim 1 or Claim 2, in which each shunt takes the form of a composite strip having conductive portions at its ends and a resist portion interconnecting the conductive portions.
4. A device as claimed in Claim 2 or Claim 3, in which the analog to digital converter for each shunt includes a delta-sigma modulator which produces a high frequency single digital data stream which is converted by decimation filtering into a multi-bit digital data stream at a lower frequency.
5. A device as claimed in Claim 2, 3 or 4, in which each converter is in the form of an integrated circuit mounted on a corresponding one of the resistive shunts.
6. A device as claimed in Claim 5, in which each integrated circuit has analog input terminals connected by lead wires to the two copper end portions of the corresponding one of the resistive shunts.

7. A device as claimed in Claim 6, in which the integrated circuit also has a terminal connected to a voltage reference source and includes a second converter for providing a digital signal stream dependent on the voltage on one of the copper end portions of the associated one of the shunts.

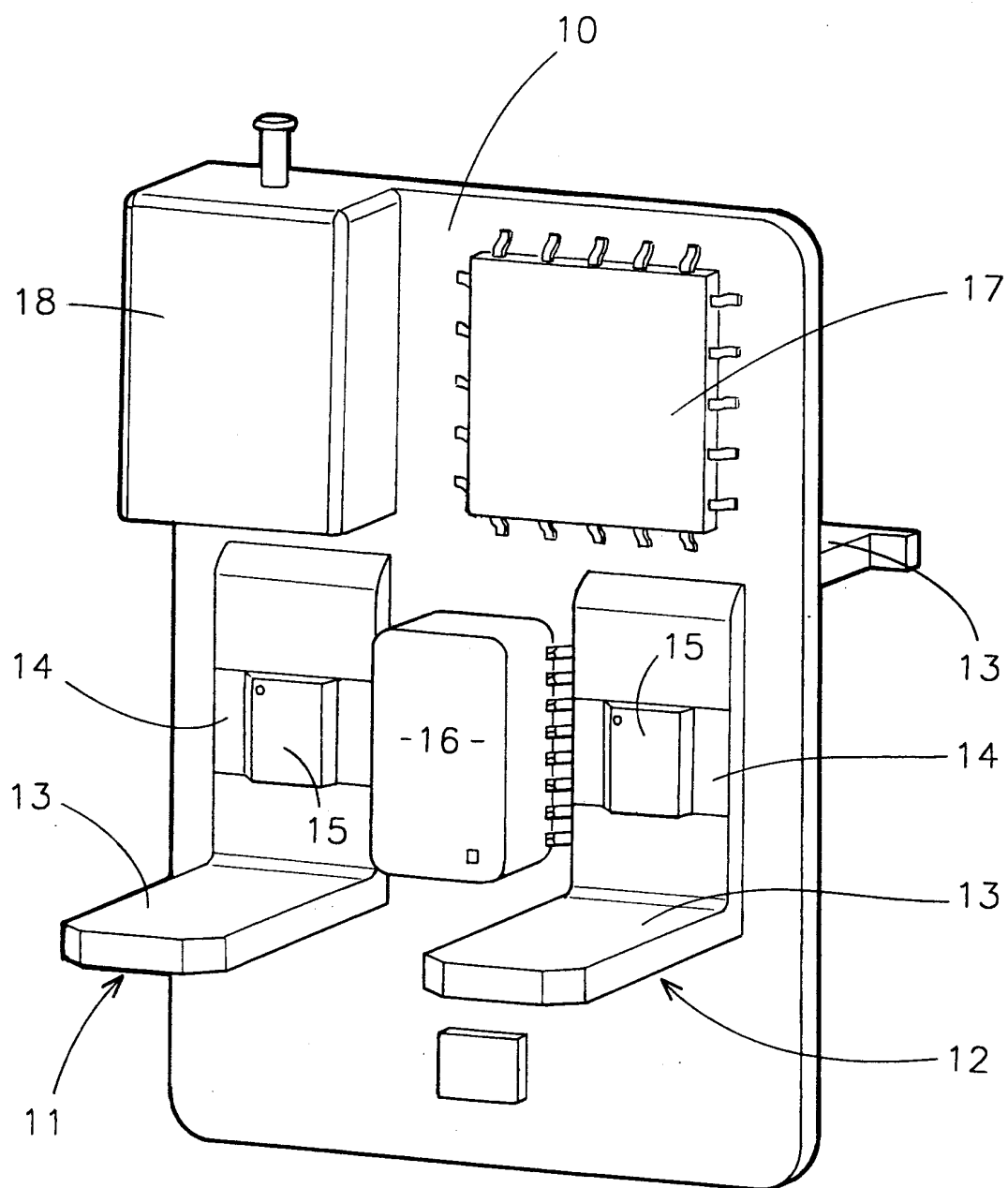
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FIG 1

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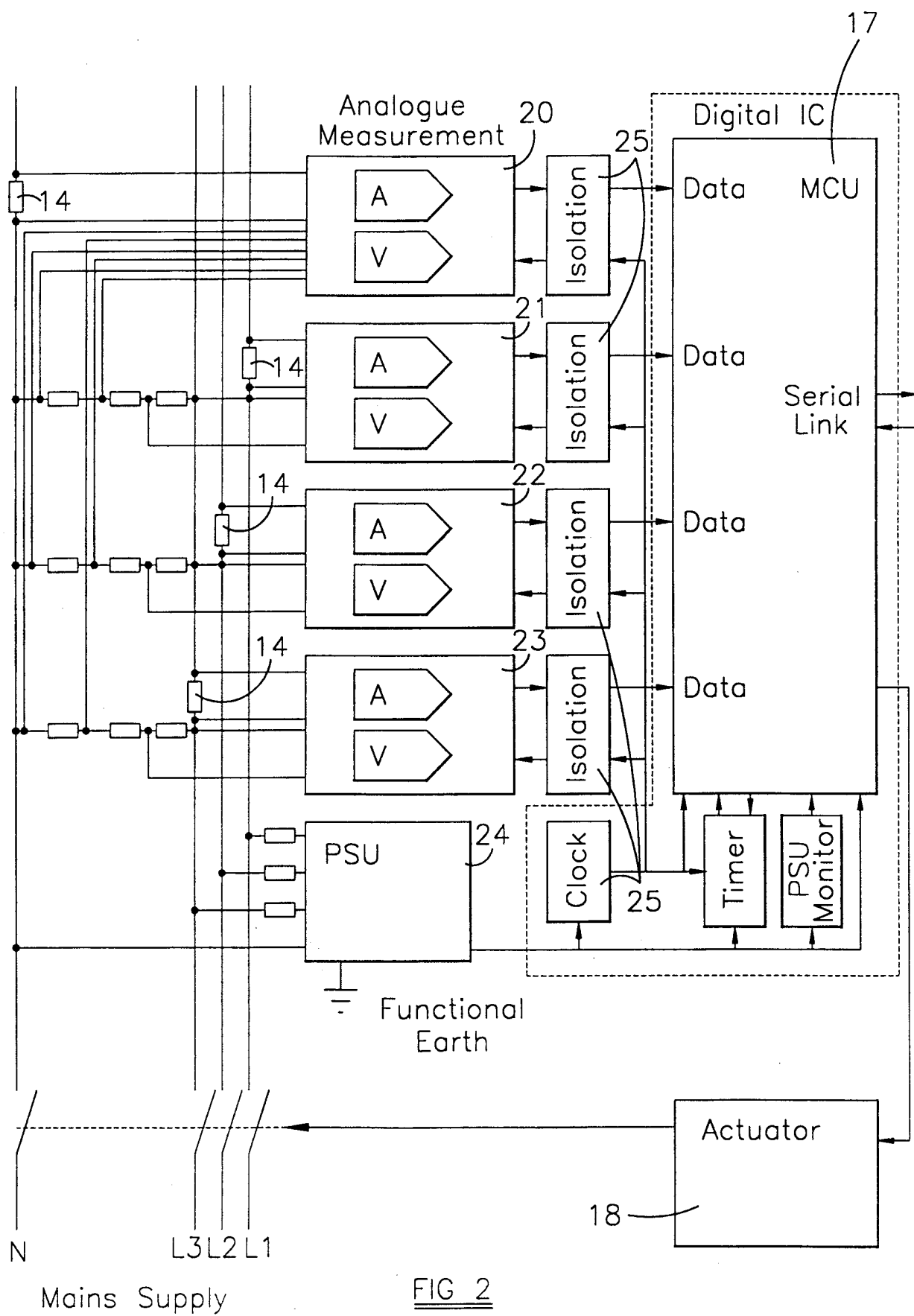


FIG 2

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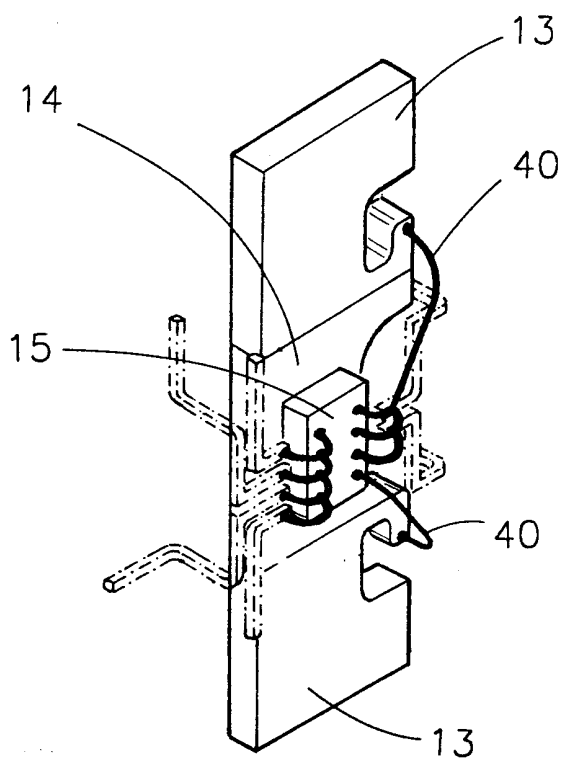


FIG 3

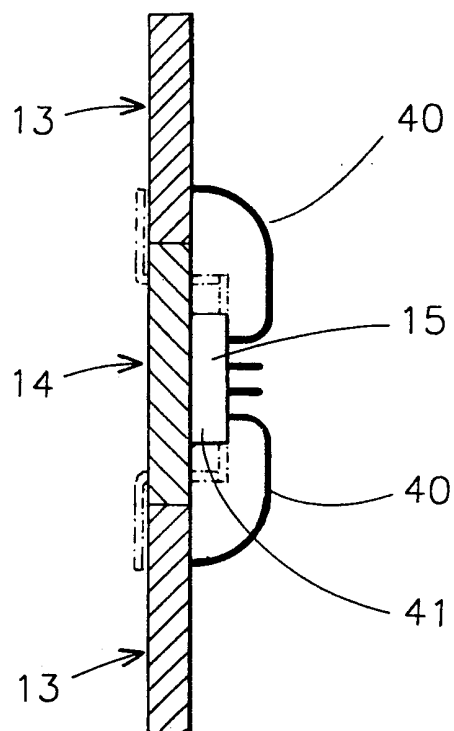


FIG 4

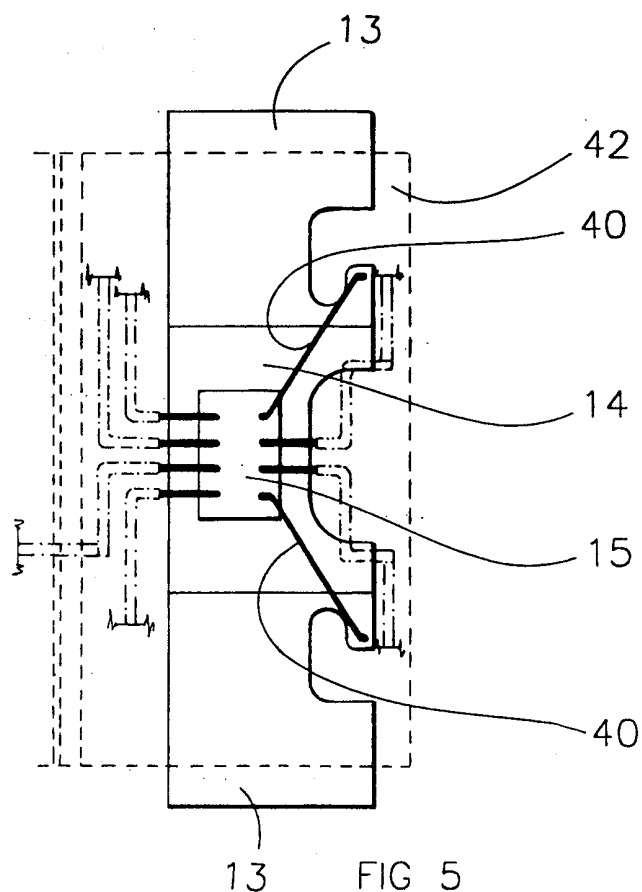
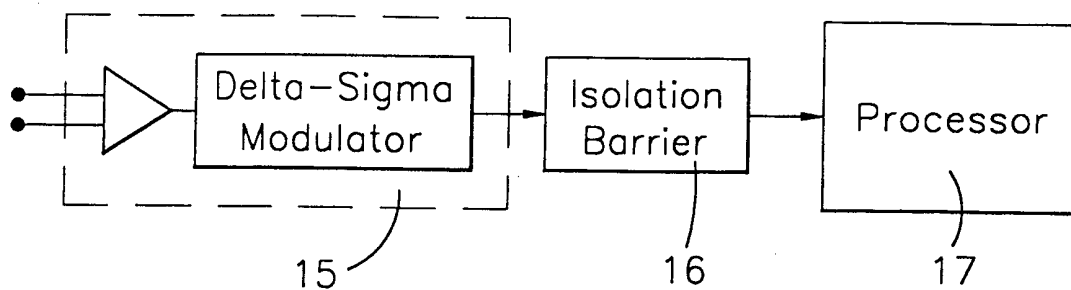
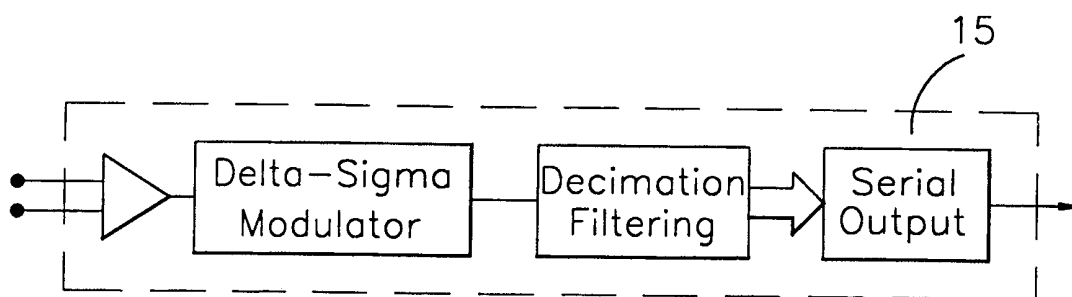
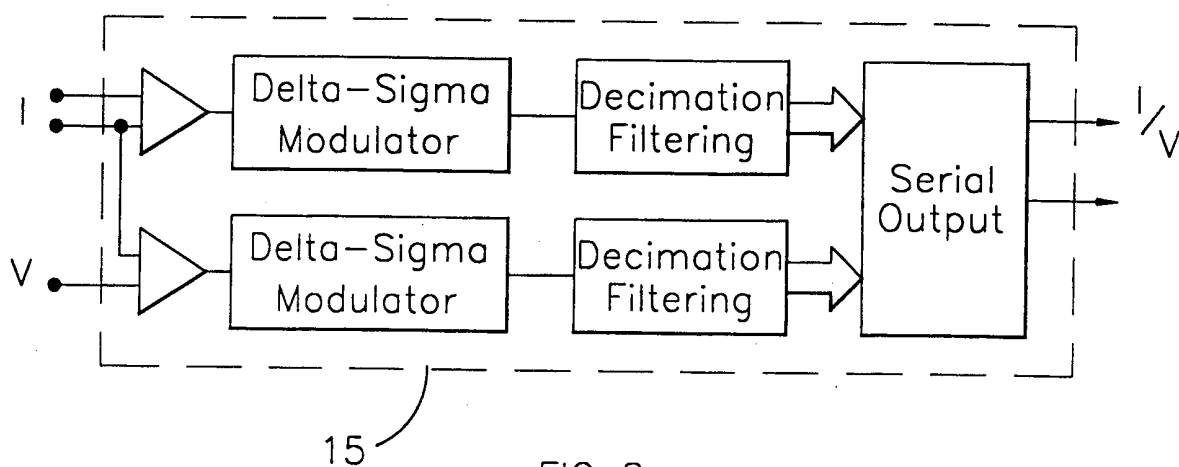


FIG 5

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FIG 6FIG 7FIG 8

INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 99/02060

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01R19/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 38 15 824 A (SPECHER & SCHUH) 19 January 1989 (1989-01-19)	1
Y	column 3, line 12 - line 23	2,3
A	column 3, line 60 - column 4, line 36; figure 2	4
Y	US 5 701 253 A (MAYELL ET AL.) 23 December 1997 (1997-12-23) abstract; figures 1-3	2
Y	EP 0 612 081 A (SAGEM) 31 August 1994 (1994-08-31) abstract; figures 1,2	3

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Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE 3815824 A	19-01-1989	CH 672959 A	15-01-1990
US 5701253 A	23-12-1997	NONE	
EP 612081 A	24-08-1994	FR 2701590 A	19-08-1994
		DE 69400014 D	12-10-1995
		DE 69400014 T	02-05-1996
		ES 2079988 T	16-01-1996
		JP 6294821 A	21-10-1994
		ZA 9400994 A	14-02-1995