ADAPTIVE ERASE OF A STORAGE DEVICE

Abstract: The various implementations described herein include systems, methods and/or devices used to enable adaptive erasure in a storage device. The method includes performing a plurality of memory operations including read operations and respective erase operations on portions of one or more non-volatile memory devices specified by the read operations and respective erase operations, where the respective erase operations are performed using a first set of erase parameters that has been established as a current set of erase parameters prior to performing the respective erase operations. The method includes, in accordance with each erase operation at least a subset of the respective erase operations, updating one or more erase statistics that correspond to performance of multiple erase operations. The method includes, in accordance with a comparison of the erase statistics with an erasure performance threshold, establishing a second set of erase parameters as the current set of erase parameters.
ADAPTIVE ERASE OF A STORAGE DEVICE

TECHNICAL FIELD

[0001] The disclosed embodiments relate generally to memory systems, and in particular, to adaptive erasure in memory devices.

BACKGROUND

[0002] Semiconductor memory devices, including flash memory, typically utilize memory cells to store data as an electrical value, such as an electrical charge or voltage. A flash memory cell, for example, includes a single transistor with a floating gate that is used to store a charge representative of a data value. Flash memory is a non-volatile data storage device that can be electrically erased and reprogrammed. More generally, non-volatile memory (e.g., flash memory, as well as other types of non-volatile memory implemented using any of a variety of technologies) retains stored information even when not powered, as opposed to volatile memory, which requires power to maintain the stored information.

[0003] Writing data to some types of non-volatile memory, including flash memory requires erasing one or more portions of the memory before writing the data to those portions of the memory. Typically, erasing the one or more portions of the memory is accomplished by applying a voltage to the one or more portions of the memory to be erased. As memory goes through repeated cycles of writes and erasures, it gets worn by the application of repeated, high voltage erase operations.

SUMMARY

[0004] Various implementations of systems, methods and devices within the scope of the appended claims each have several aspects, no single one of which is solely responsible for the attributes described herein. Without limiting the scope of the appended claims, after considering this disclosure, and particularly after considering the section entitled "Detailed Description" one will understand how the aspects of various implementations are used to enable adaptive erasure in memory devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] So that the present disclosure can be understood in greater detail, a more particular description may be had by reference to the features of various implementations,
some of which are illustrated in the appended drawings. The appended drawings, however, merely illustrate the more pertinent features of the present disclosure and are therefore not to be considered limiting, for the description may admit to other effective features.

[0006] Figure 1A is a block diagram illustrating an implementation of a data storage system, in accordance with some embodiments.

[0007] Figure 1B is a block diagram illustrating an implementation of a data storage system, in accordance with some embodiments.

[0008] Figure 2 is a block diagram illustrating an implementation of a non-volatile memory controller, in accordance with some embodiments.

[0009] Figures 3A-3F illustrate a flowchart representation of a method of adaptively erasing data in a storage device, in accordance with some embodiments.

[0010] In accordance with common practice the various features illustrated in the drawings may not be drawn to scale. Accordingly, the dimensions of the various features may be arbitrarily expanded or reduced for clarity. In addition, some of the drawings may not depict all of the components of a given system, method or device. Finally, like reference numerals may be used to denote like features throughout the specification and figures.

DETAILED DESCRIPTION

[0011] The various implementations described herein include systems, methods and/or devices used to enable adaptive erasure in memory devices. Some implementations include systems, methods and/or devices to perform an adaptive erase operation to preserve memory life. In some embodiments, the systems, methods, and/or devices perform the adaptive erase operation to maintain a consistent latency associated with erase operations.

[0012] More specifically, some implementations include a method of adaptively erasing data in a storage device. In some implementations, the storage device comprises one or more non-volatile memory devices. In some implementations, the method includes performing a plurality of memory operations including read operations and respective erase operations on portions of the one or more non-volatile memory devices specified by the read operations and respective erase operations. The respective erase operations are performed using a first set of erase parameters that has been established as a current set of erase parameters prior to performing the respective erase operations. The method also includes, in accordance with each erase operation of at least a subset of the respective erase operations,
updating one or more erase statistics that correspond to performance of multiple erase operations. The method further includes, in accordance with a comparison of the erase statistics with an erasure performance threshold, establishing a second set of erase parameters as the current set of erase parameters.

[0013] In some embodiments, the one or more erase statistics include erase operation duration statistics with respect to durations for the multiple erase operations.

[0014] In some embodiments, the method further includes, for each erase operation of the respective erase operations, updating the one or more erase statistics.

[0015] In some embodiments, updating the one or more erase statistics that correspond to the performance of the multiple erase operations includes updating at least one of the one or more erase statistics in accordance with how many erase operations, of the multiple erase operations, have durations that exceed a predefined duration threshold.

[0016] In some embodiments, updating the one or more erase statistics that correspond to the performance of the multiple erase operations includes identifying erase operations, of the multiple erase operations, whose durations exceed a predefined duration threshold, and updating at least one of the one or more erase statistics in accordance with the identified erase operations.

[0017] In some embodiments, the first set of erase parameters includes an initial pulse voltage and an incremental pulse voltage.

[0018] In some embodiments, the method includes, in accordance with a determination that one or more erase statistics corresponds to a rate or count of successful erase operations that equals or exceeds an erasure success threshold, establishing the second set of erase parameters as the current set of erase parameters by decreasing one or both of: an initial pulse voltage and an incremental pulse voltage of the current set of erase parameters.

In some embodiments, successful erase operations include erase operations having erase durations less than a first duration threshold.

[0019] In some embodiments, the method includes, in accordance with a determination that one or more erase statistics corresponds to a rate or count of unsuccessful erase operations that equals or exceeds an erasure failure threshold, establishing the second set of erase parameters as the current set of erase parameters by increasing one or both of: an initial pulse voltage and an incremental pulse voltage of the current set of erase parameters.
In some embodiments, unsuccessful erase operations include erase operations having erase durations greater than a second duration threshold.

[0020] In some embodiments, each erase operation of the respective erase operations includes applying a first voltage pulse to one or more portions of the one or more non-volatile memory devices in accordance with the current set of erase parameters, and in accordance with a determination that the one or more portions of the one or more non-volatile memory devices have not been successfully erased, applying one or more subsequent voltage pulses in accordance with the current set of erase parameters until predefined criteria have been met. The predefined criteria includes that the one or more portions of the one or more non-volatile memory devices have been successfully erased.

[0021] In some embodiments, each erase operation of the respective erase operations includes applying a set of voltage pulses to one or more portions of the one or more non-volatile memory devices in accordance with the current set of erase parameters, and in accordance with a determination that the one or more portions of the one or more non-volatile memory devices have not been successfully erased, applying one or more subsequent sets of voltage pulses to the one or more portions of the one or more non-volatile memory devices until second predefined criteria have been met. The second predefined criteria includes that the one or more portions of the one or more non-volatile memory devices have been successfully erased.

[0022] In some embodiments, the method further includes receiving one or more host read commands to read data from one or more memory blocks on the storage device, and prior to applying the one or more subsequent sets of voltage pulses to the one or more portions of the one or more non-volatile memory devices, processing at least a subset of the one or more host read commands to read data from the one or more memory blocks on the storage device.

[0023] In some embodiments, the method further includes identifying one or more portions of the one or more non-volatile memory devices that fail to satisfy a predefined erasure performance requirement when one or more erase operations are performed using the first set of erase parameters. In some embodiments, the method includes, subsequent to identifying the one or more portions of the one or more non-volatile memory devices, forgoing erase operations on the one or more portions of the one or more non-volatile memory devices using the first set of erase parameters. In some embodiments, the method
includes, subsequent to establishing the second set of erase parameters as the current set of erase parameters, performing an erase operation on at least a subset of the identified one or more portions of the one or more non-volatile memory devices using the second set of erase parameters.

[0024] In some embodiments, the method is performed by a non-volatile memory controller of the storage device and the one or more erase statistics correspond to performance of multiple erase operations on portions of one or more non-volatile memory devices coupled to the non-volatile memory controller.

[0025] In some embodiments, the storage device includes a plurality of non-volatile memory controllers, each coupled to a distinct set of one or more non-volatile memory devices in the storage device, and the method is performed independently by each non-volatile memory controller of the plurality of non-volatile memory controllers of the storage device.

[0026] In some embodiments, the one or more non-volatile memory devices include one or more flash memory devices.

[0027] In some embodiments, multiple sets of erase parameters, including the first set of erase parameters and the second set of erase parameters, are stored in non-volatile memory of the storage device.

[0028] In some embodiments, the storage device includes a dual in-line memory module (DIMM) device.

[0029] In some embodiments, a plurality of controllers on the storage device include at least one non-volatile memory controller and at least one other memory controller other than the at least one non-volatile memory controller.

[0030] In some embodiments, one of the plurality of controllers on the storage device maps double data rate (DDR) interface commands to serial advance technology attachment (SATA) interface commands.

[0031] In another aspect, any of the methods described above are performed by a storage device including (1) an interface for coupling the storage device to a host system, (2) one or more controllers, each of the one or more controllers configured to: (A) perform a plurality of memory operations including read operations and respective erase operations on portions of the one or more non-volatile memory devices specified by the read operations and
respective erase operations, where the respective erase operations are performed using a first set of erase parameters that has been established as a current set of erase parameters prior to performing the respective erase operations, (B) in accordance with each erase operation of at least a subset of the respective erase operations, update one or more erase statistics that correspond to performance of multiple erase operations, and (C) in accordance with a comparison of the erase statistics with an erasure performance threshold, establish a second set of erase parameters as the current set of erase parameters.

[0032] In some embodiments, the storage device is configured to perform any of the methods described above.

[0033] In yet another aspect, any of the methods described above are performed by a storage device. In some embodiments, the device includes (A) a storage controller, including (1) means for performing a plurality of memory operations including read operations and respective erase operations on portions of the one or more non-volatile memory devices specified by the read operations and respective erase operations, where the respective erase operations are performed using a first set of erase parameters that has been established as a current set of erase parameters prior to performing the respective erase operations; (2) means, enabled in accordance with each erase operation of at least a subset of the respective erase operations, for updating one or more erase statistics that correspond to performance of multiple erase operations; and (3) means, enabled in accordance with a comparison of the erase statistics with an erasure performance threshold, for establishing a second set of erase parameters as the current set of erase parameters.

[0034] In yet another aspect, a non-transitory computer readable storage medium, stores one or more programs for execution by one or more processors of a storage device having one or more controllers, the one or more programs including instructions for performing any of the methods described above.

[0035] In some embodiments, the non-transitory computer readable storage medium includes a non-transitory computer readable storage medium for each controller of a plurality of controllers of the storage device, each having the one or more programs including instructions for performing any of the methods described above.

[0036] Numerous details are described herein in order to provide a thorough understanding of the example implementations illustrated in the accompanying drawings. However, some embodiments may be practiced without many of the specific details, and the
scope of the claims is only limited by those features and aspects specifically recited in the
claims. Furthermore, well-known methods, components, and circuits have not been
described in exhaustive detail so as not to unnecessarily obscure more pertinent aspects of the
implementations described herein.

[0037] Figure 1A is a block diagram illustrating an implementation of a data storage
system 100, in accordance with some embodiments. While some example features are
illustrated, various other features have not been illustrated for the sake of brevity and so as
not to obscure more pertinent aspects of the example implementations disclosed herein. To
that end, as a non-limiting example, data storage system 100 includes storage device 120,
which includes host interface 122, intermediate modules 125, one or more non-volatile
memory controllers (e.g., non-volatile memory controller(s) 130), and non-volatile memory
(e.g., one or more non-volatile memory device(s) 140, 142), and is used in conjunction with
computer system 110. In some implementations, storage device 120 includes a single non-
volatile memory device while in other implementations storage device 120 includes a
plurality of non-volatile memory devices. In some implementations, non-volatile memory
devices 140, 142 include NAND-type flash memory or NOR-type flash memory. Further, in
some implementations, non-volatile memory controller 130 is a solid-state drive (SSD)
controller. However, one or more other types of storage media may be included in
accordance with aspects of a wide variety of implementations.

[0038] Computer system 110 is coupled to storage device 120 through data
connections 101. However, in some implementations computer system 110 includes storage
device 120 as a component and/or sub-system. Computer system 110 may be any suitable
computer device, such as a personal computer, a workstation, a computer server, or any other
computing device. Computer system 110 is sometimes called a host or host system. In some
implementations, computer system 110 includes one or more processors, one or more types
of memory, optionally includes a display and/or other user interface components such as a
keyboard, a touch screen display, a mouse, a track-pad, a digital camera and/or any number
of supplemental devices to add functionality. Further, in some implementations, computer
system 110 sends one or more host commands (e.g., read commands and/or write commands)
on control line 111 to storage device 120. In some implementations, computer system 110 is
a server system, such as a server system in a data center, and does not have a display and
other user interface components.
In some implementations, storage device 120 includes non-volatile memory devices 140, 142 (e.g., non-volatile memory devices 140-1 through 140-n and non-volatile memory devices 142-1 through 142-k) and non-volatile memory controllers 130 (e.g., non-volatile memory controllers 130-1 through 130-m). In some implementations, each non-volatile memory controller of non-volatile memory controllers 130 include one or more processing units (also sometimes called CPUs or processors or microprocessors or microcontrollers) configured to execute instructions in one or more programs (e.g., in non-volatile memory controllers 130). In some implementations, the one or more processors are shared by one or more components within, and in some cases, beyond the function of non-volatile memory controllers 130. In some implementations, each non-volatile memory controller of non-volatile memory controllers 130 includes adaptive erase circuitry 150. Non-volatile memory devices 140, 142 are coupled to non-volatile memory controllers 130 through connections that typically convey commands in addition to data, and optionally convey metadata, error correction information and/or other information in addition to data values to be stored in non-volatile memory devices 140, 142 and data values read from non-volatile memory devices 140, 142. For example, non-volatile memory devices 140, 142 can be configured for enterprise storage suitable for applications such as cloud computing, or for caching data stored (or to be stored) in secondary storage, such as hard disk drives. Additionally and/or alternatively, flash memory can also be configured for relatively smaller-scale applications such as personal flash drives or hard-disk replacements for personal, laptop and tablet computers. Although flash memory devices and flash controllers are used as an example here, storage device 120 may include any other non-volatile memory device(s) and corresponding non-volatile memory controller(s).

In some implementations, intermediate modules 125 include one or more processing units (also sometimes called CPUs or processors or microprocessors or microcontrollers) configured to execute instructions in one or more programs. Intermediate modules 125 are coupled to host interface 122, and non-volatile memory controllers 130 in order to coordinate operations performed by these components, for example supervising and controlling functions such as power up, power down, data hardening, charging energy storage device(s), data logging, communicating between modules on the storage device and other aspects of managing functions on storage device 120.

Figure 1B is a block diagram illustrating an implementation of a data storage system 100, in accordance with some embodiments. While some exemplary features are
illustrated, various other features have not been illustrated for the sake of brevity and so as not to obscure more pertinent aspects of the example implementations disclosed herein. To that end, as a non-limiting example, data storage system 100 includes storage device 120, which includes host interface 122, serial presence detect (SPD) device 124, data hardening circuitry 126, memory controller 128, one or more non-volatile memory controllers (e.g., non-volatile memory controller(s) 130), and non-volatile memory (e.g., one or more non-volatile memory device(s) 140, 142), and is used in conjunction with computer system 110. Storage device 120 may include various additional features that have not been illustrated for the sake of brevity and so as not to obscure more pertinent features of the example implementations disclosed herein, and a different arrangement of features may be possible. Host interface 122 provides an interface to computer system 110 through data connections 101.

[0042] In some implementations, data hardening circuitry 126 is used to transfer data from volatile memory to non-volatile memory during a power failure condition, and includes one or more processing units (also sometimes called CPUs or processors or microprocessors or microcontrollers) configured to execute instructions in one or more programs (e.g., in data hardening circuitry 126). In some implementations, the one or more processors are shared by one or more components within, and in some cases, beyond the function of data hardening circuitry 126. Data hardening circuitry 126 is coupled to host interface 122, SPD device 124, memory controller 128, and non-volatile memory controllers 130 in order to coordinate the operation of these components, including supervising and controlling functions such as power up, power down, data hardening, charging energy storage device(s), data logging, and other aspects of managing functions on storage device 120.

[0043] Memory controller 128 is coupled to host interface 122, data hardening circuitry 126, and non-volatile memory controllers 130. In some implementations, during a write operation, memory controller 128 receives data from computer system 110 through host interface 122 and during a read operation, memory controller 128 sends data to computer system 110 through host interface 122. Further, host interface 122 provides additional data, signals, voltages, and/or other information needed for communication between memory controller 128 and computer system 110. In some embodiments, memory controller 128 and host interface 122 use a defined interface standard for communication, such as double data rate type three synchronous dynamic random access memory (DDR3). In some embodiments, memory controller 128 and non-volatile memory controllers 130 use a defined
interface standard for communication, such as serial advance technology attachment (SATA). In some other implementations, the device interface used by memory controller 128 to communicate with non-volatile memory controllers 130 is SAS (serial attached SCSI), or other storage interface. In some implementations, memory controller 128 includes one or more processing units (also sometimes called CPUs or processors or microprocessors or microcontrollers) configured to execute instructions in one or more programs (e.g., in memory controller 128). In some implementations, the one or more processors are shared by one or more components within, and in some cases, beyond the function of memory controller 128.

[0044] SPD device 124 is coupled to host interface 122 and data hardening circuitry 126. Serial presence detect (SPD) refers to a standardized way to automatically access information about a computer memory module (e.g., storage device 120). For example, if the memory module has a failure, the failure can be communicated with a host system (e.g., computer system 110) through SPD device 124.

[0045] Figure 2 is a block diagram illustrating an implementation of a non-volatile memory controller 130-1, in accordance with some embodiments. Non-volatile memory controller 130-1 typically includes one or more processors (also sometimes called CPUs or processing units or microprocessors or microcontrollers) 202 for executing modules, programs and/or instructions stored in memory 206 and thereby performing processing operations, memory 206, and one or more communication buses 208 for interconnecting these components. Communication buses 208 optionally include circuitry (sometimes called a chipset) that interconnects and controls communications between system components. In some implementations, non-volatile memory controller 130-1 also includes adaptive erase circuitry 150-1. In some embodiments, adaptive erase circuitry 150-1 performs erase operations based on one or more sets of erase parameters (e.g., current set of erase parameters 226). In some embodiments, non-volatile memory controller 130-1 is coupled to memory controller 128, data hardening circuitry 126 (if present), and non-volatile memory devices 140 (e.g., non-volatile memory devices 140-1 through 140-n) by communication buses 208. Memory 206 includes high-speed random access memory, such as DRAM, SRAM, DDR RAM or other random access solid state memory devices, and may include non-volatile memory, such as one or more magnetic disk storage devices, optical disk storage devices, flash memory devices, or other non-volatile solid state storage devices. Memory 206 optionally includes one or more storage devices remotely located from processor(s) 202.
Memory 206, or alternately the non-volatile memory device(s) within memory 206, comprises a non-transitory computer readable storage medium. In some embodiments, memory 206, or the computer readable storage medium of memory 206 stores the following programs, modules, and data structures, or a subset thereof:

- an interface module 210 that is used for communicating with other components, such as memory controller 128, data hardening circuitry 126, and non-volatile memory devices 140;
- a reset module 212 that is used for resetting non-volatile memory controller 130-1;
- one or more read and write modules 214 used for reading from and writing to non-volatile memory devices 140;
- an erase module 216 that is used for erasing portions of memory on non-volatile memory devices 140;
- adaptive erase data 218 that is used for performing adaptive erase operations on non-volatile memory devices 140; and
- volatile data 228 including volatile data associated with non-volatile memory controller 130-1.

[0046] In some embodiments, the erase module 216 includes an erase statistics update module 230 that includes instructions for updating one or more erase statistics 224 (described below) based on erase operations, and/or an erase parameter update module 232 that includes instructions for conditionally modifying one or more current sets of erase parameters 226.

[0047] In some embodiments, the adaptive erase data 218 includes erase parameter sets 220-1 to 220-L. In some embodiments, each erase parameter set includes an initial pulse voltage and an incremental pulse voltage (e.g., an initial pulse voltage of 1.8 V, and an incremental pulse voltage of 0.1 V). In some embodiments, the sets of erase parameters are on a scale of increasing initial pulse voltage (e.g., the initial pulse voltage of erase parameter set 1 is less than the initial pulse voltage of erase parameter set L). In some embodiments, one or both of the initial pulse voltage and the incremental pulse voltage increase from one erase parameter set to a subsequent erase parameter set (e.g., an initial pulse voltage of a first set of erase parameters is less than an initial pulse voltage of a second set of erase parameters, and/or an incremental pulse voltage of the first set of erase parameters is less than an incremental pulse voltage of the second set of erase parameters). In some embodiments, the
erase parameter set includes more than one incremental pulse voltage (e.g., a first incremental pulse voltage of 0.1 V for the first five erase pulses, then a second incremental pulse voltage of 0.2 V for all remaining erase pulses).

[0048] In some embodiments, the adaptive erase data 218 includes memory portion data subsets 222-1 to 222-M. These memory portion data subsets 222 store adaptive erase information pertaining to distinct memory portions of non-volatile memory devices 140. In some embodiments, one memory portion data subset (e.g., subset 222-1) corresponds to one non-volatile memory device (e.g., non-volatile memory device 140-1). In some embodiments, one memory portion of non-volatile memory devices 140, corresponds to a subset of memory on a non-volatile memory device (e.g., non-volatile memory device 140-1). In some embodiments, one or more of non-volatile memory devices 140, respectively comprise a single integrated circuit die (i.e., chip or microchip). In some embodiments, one or more of non-volatile memory devices 140 respectively include a plurality of integrated circuit dies.

[0049] In some embodiments, the memory portion subsets 222 include data elements pertaining to erase statistics 224 and the current set of erase parameters 226 for the respective memory portion. For example, memory portion data subset 222-1 includes erase statistics 224-1 for the first memory portion, and information regarding the current set of erase parameters 226-1 being applied in an adaptive erase function to the first memory portion. As erase operations are performed on the respective memory portions, the corresponding erase statistics are updated. In some embodiments, the erase statistics 224 include information regarding the proportion of the corresponding memory portions that have successfully or unsuccessfully been erased. For example, if erase operations are performed on the first memory portion using the current set of erase parameters 226-1, and 90% of the erase operations are successful (e.g., meet predefined success criteria), the erase statistics 224-1 would be updated to reflect this information. In some embodiments, erase operations are considered to be successful if the erase operations are completed within a predefined amount of time or within a predefined number of erase pulses. Thus, in such embodiments, if an erase operation does result in erasure of the memory portion (e.g., one or more blocks), but takes longer than the predefined amount of time, the erase operation would be considered to be unsuccessful for purposes of at least one of the erase statistics. In some embodiments, the erase statistics are used to make a comparison to an erasure performance threshold (e.g., proportion of erase success, average duration of time to erase, etc.), for determining if the current set of erase parameters needs to be updated. Alternatively, the erase statistics 224
include information regarding a number of memory units (e.g., blocks, etc.) that have successfully or unsuccessfully been erased.

[0050] In some embodiments, the current set of erase parameters 226 for each memory portion data subset 222 includes a reference to one of the set of erase parameters 220-1 to 220-L. In some embodiments, the current set of erase parameters 226 for each memory portion data subset 222, includes a copy of the parameter values of one of the sets of erase parameters 220-1 to 220-L.

[0051] In some embodiments, memory portion data subsets 222 may store a subset of the data structures identified above. Furthermore, memory portion data subsets 222 may store additional data structures not described above.

[0052] In some embodiments, the adaptive erase data 218 may include a subset of the data structures identified above. Furthermore, the adaptive erase data 218 may store additional modules and data structures not described above.

[0053] Each of the above identified elements may be stored in one or more of the previously mentioned memory devices, and corresponds to a set of instructions for performing a function described above. The above identified modules or programs (i.e., sets of instructions) need not be implemented as separate software programs, procedures or modules, and thus various subsets of these modules may be combined or otherwise re-arranged in various embodiments. In some embodiments, memory 206 may store a subset of the modules and data structures identified above. Furthermore, memory 206 may store additional modules and data structures not described above. In some embodiments, the programs, modules, and data structures stored in memory 206, or the computer readable storage medium of memory 206, provide instructions for implementing respective operations in the methods described below with reference to Figures 3A-3F.

[0054] Although Figure 2 shows a non-volatile memory controller 130-1, Figure 2 is intended more as a functional description of the various features which may be present in a non-volatile memory controller than as a structural schematic of the embodiments described herein. In practice, and as recognized by those of ordinary skill in the art, items shown separately could be combined and some items could be separated. Further, although Figure 2 shows a non-volatile memory controller 130-1, the description of Figure 2 similarly applies to other non-volatile memory controllers (e.g., non-volatile memory controllers 130-2 through 130-m) in storage device 120 (Figure 1).
Figures 3A-3F illustrate a flowchart representation of a method 300 of adaptively erasing data in a storage device, in accordance with some embodiments. In some embodiments, the storage device includes one or more non-volatile memory devices. The method includes, performing (302) a plurality of memory operations including read operations and respective erase operations on portions of the one or more non-volatile memory devices specified by the read operations and respective erase operations. The respective erase operations are performed using a first set of erase parameters that has been established as a current set of erase parameters prior to performing the respective erase operations. In some embodiments, at least one portion of the portions of one or more non-volatile memory devices corresponds to the non-volatile memory of one or more integrated circuit die. In some embodiments, at least one portion of the portions of one or more non-volatile memory devices is smaller than the non-volatile memory of an integrated circuit die. In some embodiments, the portions of the one or more non-volatile memory devices are configured to store host data (e.g., user data corresponding to files, documents photos), as well as metadata. In some embodiments, the portions of the one or more non-volatile memory devices store the host data and the metadata.

In some embodiments, the first set of erase parameters includes (304) an initial pulse voltage and an incremental pulse voltage. For example, the first set of erase parameters may include an initial pulse voltage of 1.8 V and an incremental pulse voltage of 0.1 V. The exemplary initial pulse voltage of 1.8 V and an incremental pulse voltage of 0.1 V correspond to application of an initial erase pulse of 1.8 V, a subsequent voltage pulse of 1.9 V, a subsequent voltage pulse of 2.0 V, etc. to one or more portions of non-volatile memory. In some embodiments, the sets of erase parameters include sequentially increasing initial pulse voltages (e.g., a first set has a 1.8 V initial pulse voltage and a second set has a 1.9 V initial pulse voltage, etc.). In some embodiments, the sets of erase parameters include sequentially increasing incremental pulse voltages (e.g., a first set has 0.1 V incremental pulse voltage, and a second set has 0.2 V incremental pulse voltage, etc.). In some embodiments, one or both of the initial pulse voltage and the incremental pulse voltage increase from one set of erase parameters to a subsequent set of erase parameters. In some embodiments, the set of erase parameters includes more than one incremental pulse voltage (e.g., a first incremental pulse voltage of 0.1 V for first five pulses, then a second incremental pulse voltage of 0.2 V for all of the remaining pulses). In some embodiments, any and all sets of erase parameters
have an initial pulse voltage and one or more incremental pulse voltages. In some
embodiments, the incremental pulse voltage is 0 V.

[0057] In some embodiments, each erase operation of the respective erase operations
includes, applying (306) a first voltage pulse to one or more portions of the one or more non-
volatile memory devices in accordance with the current set of erase parameters (e.g., a first
voltage pulse of 1.8 V); and, in accordance with a determination that the one or more portions
of the one or more non-volatile memory devices have not been successfully erased, applying
(308) one or more subsequent voltage pulses in accordance with the current set of erase
parameters until predefined criteria have been met. The predefined criteria includes that the
one or more portions of the one or more non-volatile memory devices have been successfully
erased. For example, after applying an initial pulse voltage of 1.8 V to one or more portions
of the one or more non-volatile memory devices, in accordance with a determination that the
one or more portions of the one or more non-volatile memory devices have not been
successfully erased, five subsequent voltage pulses may applied to the one or more portions
of the one or more non-volatile memory devices before the one or more portions of the one or
more non-volatile memory devices are determined to be successfully erased.

[0058] In some embodiments, the one or more non-volatile memory devices include
(310) one or more flash memory devices.

[0059] In some embodiments, each erase operation of the respective erase operations
includes, applying (312, Figure 3B) a set of voltage pulses to one or more portions of the one
or more non-volatile memory devices in accordance with the current set of erase parameters;
and, in accordance with a determination that the one or more portions of the one or more non-
volatile memory devices have not been successfully erased, applying (314) one or more
subsequent sets of voltage pulses to the one or more portions of the one or more non-volatile
memory devices until second predefined criteria have been met. The second predefined
criteria includes that the one or more portions of the one or more non-volatile memory
devices have been successfully erased. Optionally, the second predefined criteria include a
maximum number of sets of voltage pulses to erase the one or more portions of the one or
more non-volatile memory devices. Thus, optionally, the second predefined criteria are
satisfied when the maximum number of sets of voltage pulses have been applied, regardless
of whether the one or more portions of the one or more non-volatile memory devices have
been successfully erased. In some embodiments, the one or more subsequent sets of voltage pulses are applied in accordance with the current set of erase parameters.

[0060] In some embodiments, the method further includes, receiving (316) one or more host read commands to read data from one or more memory blocks on the storage device; and, prior to applying the one or more subsequent sets of voltage pulses to the one or more portions of the one or more non-volatile memory devices, processing (318) at least a subset of the one or more host read commands to read data from the one or more memory blocks on the storage device. For example, host read commands are sent to a controller for reading data from one or more non-volatile memory devices. In this example, an erase operation is being performed by the controller on a first non-volatile memory device while one or more of the host read commands request reading data from the same first non-volatile memory device. In this example, after applying a first set of voltage pulses (e.g., ten voltage pulses) to the first non-volatile memory device, that device has not been successfully erased. In this example, one or more of the host read commands are processed before a second set of voltage pulses is applied to the first non-volatile memory device, to try to erase the device again. In a further example, all host read commands pending (e.g., already received) at the conclusion of applying the first set of voltage pulses are processed before a second set of voltage pulses is applied to the first non-volatile memory device. In some embodiments, receiving the one or more host read commands to read data from one or more memory blocks on the storage device includes receiving the one or more host read commands while performing one or more erase operations of the respective erase operations.

[0061] The method further includes, in accordance with each erase operation of at least a subset of the respective erase operations, updating (320, Figure 3C) one or more erase statistics that correspond to performance of multiple erase operations. In some embodiments, as erase operations are performed on one or more portions of the one or more non-volatile memory devices, erase statistics that correspond to the one or more portions of the one or more non-volatile memory devices are updated. In some embodiments, the erase statistics include information regarding a fraction of the one or more portions of the one or more non-volatile memory devices (or a number of memory units, such as blocks, within each portion of the one or more portions of the one or more non-volatile memory devices) that have successfully or unsuccessfully been erased. For example, when an adaptive erase operation was performed on a first memory portion using a current set of erase parameters, and resulted in 90% of the first memory portion (or a number of memory units that correspond to 90% of
memory units in the first memory portion) being successfully erased, the erase statistics would be updated to reflect this information. In some embodiments, the updated erase statistics include a reference to the set of erase parameters used during a last erase operation on the first memory portion.

[0062] In some embodiments, the one or more erase statistics include (322) erase operation duration statistics with respect to durations for the multiple erase operations. For example, when an erase operation required seven voltage pulses to successfully erase a portion of the one or more non-volatile memory devices, the erase operation duration statistics include the number of pulses (e.g., seven) applied to successfully erase the portion of the one or more non-volatile memory devices, or a unit of time (e.g., seconds, milliseconds, etc.) that corresponds to the number of pulses applied to successfully erase the portion of the one or more non-volatile memory devices. In some embodiments, the erase operation duration statistics are rounded up or down to predefined values (e.g., seconds, milliseconds, sets of ten pulses) and recorded as a rounded value. In some embodiments, the one or more erase statistics include an average duration for the multiple erase operations.

[0063] In some embodiments, the one or more erase statistics include erase success statistics, the erase success statistics indicating whether the portions of the one or more non-volatile memory devices have successfully completed one or more erase operations within a target erase duration. In some embodiments, the one or more erase statistics include erase success statistics, the erase success statistics indicating whether the portions of the one or more non-volatile memory devices have not successfully completed one or more erase operations within a target erase duration. In some embodiments, a portion of the one or more non-volatile memory devices is deemed to have successfully completed an erase operation in accordance with a determination that the portion of the one or more non-volatile memory devices is in a condition for receiving and storing data.

[0064] In some embodiments, the method includes, for each erase operation of the respective erase operations, updating (324) the one or more erase statistics. For example, in some embodiments, subsequent to a first erase operation performed on a first memory portion and a second erase operation performed on a second memory portion, one or more erase statistics corresponding to the first memory portion and one or more erase statistics corresponding to the second memory portion are updated.
In some embodiments, updating the one or more erase statistics that correspond to the performance of the multiple erase operations includes updating (326) at least one of the one or more erase statistics in accordance with how many erase operations, of the multiple erase operations, have a duration that exceeds a predefined duration threshold. For example, the storage device updates erase statistics to indicate that a particular number of erase operations (e.g., 137 out of 5000) performed on a first portion of the one or more non-volatile memory devices have taken more than a predefined duration threshold, such as eight voltage pulses or 3 milliseconds, to successfully erase the first portion. In some embodiments, determining how many erase operations, of the multiple erase operations, have durations that exceed a predefined duration threshold includes identifying the current set of erase parameters used for the multiple erase operations (e.g., 137 erase operations have taken more than 3 ms to successfully erase the first portion, using the fifth set of erase parameters).

In some embodiments, updating the one or more erase statistics that correspond to the performance of the multiple erase operations includes (328) identifying erase operations, of the multiple erase operations, whose durations exceed a predefined duration threshold, and updating at least one of the one or more erase statistics in accordance with the identified erase operations. For example, the storage device identifies that a specific number of erase operations (e.g., 137 of 5000) performed on a first portion of the one or more non-volatile memory devices have taken more than a predefined duration threshold, such as eight voltage pulses or 3 milliseconds, to successfully erase the first portion, and updates erase statistics to indicate the number of erase operations (e.g., 137) that have taken more than the predefined duration threshold for a successful erasure.

The method further includes, in accordance with a comparison of the erase statistics with an erasure performance threshold, establishing (330, Figure 3D) a second set of erase parameters as the current set of erase parameters. For example, in some embodiments, in accordance with a determination that the erase statistics do not satisfy the erasure performance threshold, the storage device modifies the current set of erase parameters. In some embodiments, in accordance with a determination that the erase statistics satisfy the erasure performance threshold, the storage device forgoes modifying the current set of erase parameters (e.g., the storage device continues to use the current set of erase parameters for erase operations until the erase statistics no longer satisfy the erasure performance threshold).
In some embodiments, the method includes, in accordance with a
determination that one or more erase statistics correspond to a rate or count of successful
erase operations that equals or exceeds an erasure success threshold, establishing (332) the
second set of erase parameters as the current set of erase parameters by decreasing one or
both of an initial pulse voltage and an incremental pulse voltage of the current set of erase
parameters. In some embodiments, successful erase operations include erase operations
having erase durations less than a first duration threshold. For example, in some
embodiments, in accordance with a determination that the erase statistics for the first portion
of the one or more non-volatile memory devices indicate a 99.9% rate of erase success using
the current set of erase parameters and the erase success threshold is 99%, the current set of
erase parameters is updated to be another set of erase parameters that includes a lower initial
pulse voltage and/or a lower incremental pulse voltage. In some embodiments, successful
erase operations include erase operations that have completed successfully within a target
erase duration.

In some embodiments, the method further includes, in accordance with a
determination that one or more erase statistics corresponds to a rate or count of unsuccessful
erase operations that equals or exceeds an erasure failure threshold, establishing (334) the
second set of erase parameters as the current set of erase parameters by increasing one or both
of an initial pulse voltage and an incremental pulse voltage of the current set of erase
parameters. In some embodiments, unsuccessful erase operations include erase operations
having erase durations greater than a second duration threshold. For example, if the erase
statistics for the first portion of the one or more non-volatile memory devices indicate a 5% rate
of erase failure using the current set of erase parameters, and the erase failure threshold is
1%, the current set of erase parameters is updated to be another set of erase parameters that
includes a higher initial pulse voltage and/or a higher incremental pulse voltage. In some
embodiments, unsuccessful erase operations include erase operations that have not completed
successfully within a target erase duration.

In some embodiments, successful erase operations include erase operations
having erase durations less than a first duration threshold, and the method includes, in
accordance with a determination that one or more erase statistics corresponds to a rate or
count of successful erase operations that does not meet an erasure success threshold,
establishing the second set of erase parameters as the current set of erase parameters by
increasing one or both of an initial pulse voltage and an incremental pulse voltage of the
current set of erase parameters. For example, if the erase statistics for the first portion of the one or more non-volatile memory devices indicate a 95% rate of erase success using the current set of erase parameters, and the erase success threshold is 99%, the current set of erase parameters is updated to be another set of erase parameters that utilizes a higher initial pulse voltage and/or a higher incremental pulse voltage.

[0071] In some embodiments, the method includes, identifying (336, Figure 3E) one or more portions of the one or more non-volatile memory devices that fail to satisfy a predefined erasure performance requirement when one or more erase operations are performed using the first set of erase parameters; subsequent to identifying the one or more portions of the one or more non-volatile memory devices, forgoing (338) erase operations on the one or more portions of the one or more non-volatile memory devices using the first set of erase parameters; and, subsequent to establishing the second set of erase parameters as the current set of erase parameters, performing (340) an erase operation on at least a subset of the identified one or more portions of the one or more non-volatile memory devices using the second set of erase parameters. For example, a first portion of a non-volatile memory device that failed to be erased after repeated erase operations using the first set of erase parameters is identified. In this same example, the identified portion does not have any more erase operations performed on it using the first set of erase operations. In this example, the first portion is set aside to be erased with the second set of erase parameters.

[0072] Alternatively, in some embodiments, the method includes, subsequent to establishing the second set of erase parameters as the current set of erase parameters, performing an erase operation on at least a subset of the identified one or more portions of the one or more non-volatile memory devices using a third set of erase parameters. The third set of erase parameters is distinct from the first set of erase parameters or the second set of erase parameters. Continuing from the previous example, if the identified portion is determined to require a set of erase parameters that include a higher initial pulse voltage and/or incremental pulse voltage than found in the second set of erase parameters, the identified portion is set aside to be erased with a third set of erase parameters.

[0073] In some embodiments, the method is performed (342, Figure 3F) by a non-volatile memory controller (e.g., NVM controller 130-1, Figure 1A) of the storage device (e.g., storage device 120, Figure 1A) and the one or more erase statistics correspond to performance of multiple erase operations on portions of one or more non-volatile memory
devices coupled to the non-volatile memory controller (e.g., non-volatile memory devices 140, Figure 1A).

[0074] In some embodiments, the storage device (e.g., storage device 120, Figure 1A) includes (344) a plurality of non-volatile memory controllers (e.g., NVM controllers 130-1 and 130-2, Figure 1A), each coupled to a distinct set of one or more non-volatile memory devices (e.g., non-volatile memory devices 140, 142, Figure 1A) in the storage device, and the method is performed independently by each non-volatile memory controller of the plurality of non-volatile memory controllers of the storage device. For example, in some embodiments, NVM controller 130-1 and NVM controller 130-2, shown in Figure 1A, perform the above-described method independent of each other.

[0075] In some embodiments, multiple sets of erase parameters, including the first set of erase parameters and the second set of erase parameters, are stored (346) in non-volatile memory of the storage device (e.g., erase parameter set 220-1 through 220-L in memory 206, Figure 2).

[0076] In some implementations, with respect to any of the methods described above, a non-volatile memory corresponds to a single flash memory device, while in other implementations, the non-volatile memory includes a plurality of flash memory devices.

[0077] In some implementations, with respect to any of the methods described above, a storage device includes (1) an interface for coupling the storage device to a host system, (2) one or more controllers, each of the one or more controllers configured to perform or control performance of any of the methods described above.

[0078] It will be understood that, although the terms "first," "second," etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first contact could be termed a second contact, and, similarly, a second contact could be termed a first contact, which changing the meaning of the description, so long as all occurrences of the "first contact" are renamed consistently and all occurrences of the second contact are renamed consistently. The first contact and the second contact are both contacts, but they are not the same contact.

[0079] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the claims. As used in the description of the embodiments and the appended claims, the singular forms "a", "an" and "the" are
intended to include the plural forms as well, unless the context clearly indicates otherwise. It will also be understood that the term "and/or" as used herein refers to and encompasses any and all possible combinations of one or more of the associated listed items. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0080] As used herein, the term "if" may be construed to mean "when" or "upon" or "in response to determining" or "in accordance with a determination" or "in response to detecting," that a stated condition precedent is true, depending on the context. Similarly, the phrase "if it is determined [that a stated condition precedent is true]" or "if [a stated condition precedent is true]" or "when [a stated condition precedent is true]" may be construed to mean "upon determining" or "in response to determining" or "in accordance with a determination" or "upon detecting" or "in response to detecting" that the stated condition precedent is true, depending on the context.

[0081] The foregoing description, for purpose of explanation, has been described with reference to specific implementations. However, the illustrative discussions above are not intended to be exhaustive or to limit the claims to the precise forms disclosed. Many modifications and variations are possible in view of the above teachings. The implementations were chosen and described in order to best explain principles of operation and practical applications, to thereby enable others skilled in the art.
What is claimed is:

1. A method of erasing data in a storage device, the storage device having one or more non-volatile memory devices, the method comprising:
   performing a plurality of memory operations including read operations and respective erase operations on portions of the one or more non-volatile memory devices specified by the read operations and respective erase operations, wherein the respective erase operations are performed using a first set of erase parameters that has been established as a current set of erase parameters prior to performing the respective erase operations;
   in accordance with each erase operation of at least a subset of the respective erase operations, updating one or more erase statistics that correspond to performance of multiple erase operations; and,
   in accordance with a comparison of the erase statistics with an erasure performance threshold, establishing a second set of erase parameters as the current set of erase parameters.

2. The method of claim 1, wherein the one or more erase statistics include erase operation duration statistics with respect to durations for the multiple erase operations.

3. The method of any one of claims 1-2, including, for each erase operation of the respective erase operations, updating the one or more erase statistics.

4. The method of any one of claims 1-3, wherein updating the one or more erase statistics that correspond to the performance of the multiple erase operations includes updating at least one of the one or more erase statistics in accordance with how many erase operations, of the multiple erase operations, have durations that exceed a predefined duration threshold.

5. The method of any one of claims 1-4, wherein updating the one or more erase statistics that correspond to the performance of the multiple erase operations includes identifying erase operations, of the multiple erase operations, whose durations exceed a predefined duration threshold, and updating at least one of the one or more erase statistics in accordance with the identified erase operations.

6. The method of any one of claims 1-5, wherein the first set of erase parameters includes an initial pulse voltage and an incremental pulse voltage.
7. The method of any one of claims 1-6, including, in accordance with a determination that one or more erase statistics corresponds to a rate or count of successful erase operations that equals or exceeds an erasure success threshold, establishing the second set of erase parameters as the current set of erase parameters by decreasing one or both of: an initial pulse voltage and an incremental pulse voltage of the current set of erase parameters.

8. The method of any one of claims 1-6, including, in accordance with a determination that one or more erase statistics corresponds to a rate or count of unsuccessful erase operations that equals or exceeds an erasure failure threshold, establishing the second set of erase parameters as the current set of erase parameters by increasing one or both of: an initial pulse voltage and an incremental pulse voltage of the current set of erase parameters.

9. The method of any one of claims 1-8, wherein each erase operation of the respective erase operations includes:

   applying a first voltage pulse to one or more portions of the one or more non-volatile memory devices in accordance with the current set of erase parameters; and,

   in accordance with a determination that the one or more portions of the one or more non-volatile memory devices have not been successfully erased, applying one or more subsequent voltage pulses in accordance with the current set of erase parameters until predefined criteria have been met, the predefined criteria including that the one or more portions of the one or more non-volatile memory devices have been successfully erased.

10. The method of any one of claims 1-9, wherein each erase operation of the respective erase operations includes:

    applying a set of voltage pulses to one or more portions of the one or more non-volatile memory devices in accordance with the current set of erase parameters; and,

    in accordance with a determination that the one or more portions of the one or more non-volatile memory devices have not been successfully erased, applying one or more subsequent sets of voltage pulses to the one or more portions of the one or more non-volatile memory devices until second predefined criteria have been met, the second predefined criteria including that the one or more portions of the one or more non-volatile memory devices have been successfully erased.

11. The method of claim 10, further comprising:
receiving one or more host read commands to read data from one or more memory blocks on the storage device; and,
prior to applying the one or more subsequent sets of voltage pulses to the one or more portions of the one or more non-volatile memory devices, processing at least a subset of the one or more host read commands to read data from the one or more memory blocks on the storage device.

12. The method of any one of claims 1-11, further comprising:
identifying one or more portions of the one or more non-volatile memory devices that fail to satisfy a predefined erasure performance requirement when one or more erase operations are performed using the first set of erase parameters;
subsequent to identifying the one or more portions of the one or more non-volatile memory devices, forgoing erase operations on the one or more portions of the one or more non-volatile memory devices using the first set of erase parameters; and,
subsequent to establishing the second set of erase parameters as the current set of erase parameters, performing an erase operation on at least a subset of the identified one or more portions of the one or more non-volatile memory devices using the second set of erase parameters.

13. The method of any one of claims 1-12, wherein the method is performed by a non-volatile memory controller of the storage device and the one or more erase statistics correspond to performance of multiple erase operations on portions of one or more non-volatile memory devices coupled to the non-volatile memory controller.

14. The method of any one of claims 1-12, wherein the storage device comprises a plurality of non-volatile memory controllers, each coupled to a distinct set of one or more non-volatile memory devices in the storage device, and the method is performed independently by each non-volatile memory controller of the plurality of non-volatile memory controllers of the storage device.

15. The method of any one of claims 1-14, wherein the one or more non-volatile memory devices comprise one or more flash memory devices.
16. The method of any one of claims 1-15, wherein multiple sets of erase parameters, including the first set of erase parameters and the second set of erase parameters, are stored in non-volatile memory of the storage device.

17. A storage device, having one or more non-volatile memory devices, comprising:
an interface for coupling the storage device to a host system; and
one or more controllers, each of the one or more controllers configured to:
perform a plurality of memory operations including read operations and respective erase operations on portions of the one or more non-volatile memory devices specified by the read operations and respective erase operations, wherein the respective erase operations are performed using a first set of erase parameters that has been established as a current set of erase parameters prior to performing the respective erase operations;
in accordance with each erase operation of at least a subset of the respective erase operations, update one or more erase statistics that correspond to performance of multiple erase operations; and,
in accordance with a comparison of the erase statistics with an erasure performance threshold, establish a second set of erase parameters as the current set of erase parameters.

18. The storage device of claim 17, wherein the one or more erase statistics include erase operation duration statistics with respect to durations for the multiple erase operations.

19. The storage device of any one of claims 17-18, wherein the adaptive erase circuitry is further configured to, for each erase operation of the respective erase operations, update the one or more erase statistics.

20. The storage device of any one of claims 17-19, wherein updating the one or more erase statistics that correspond to the performance of the multiple erase operations includes updating at least one of the one or more erase statistics in accordance with how many erase operations, of the multiple erase operations, have durations that exceed a predefined duration threshold.

21. The storage device of any one of claims 17-20, wherein updating the one or more erase statistics that correspond to the performance of the multiple erase operations includes identifying erase operations, of the multiple erase operations, whose durations exceed a
predefined duration threshold, and updating at least one of the one or more erase statistics in accordance with the identified erase operations.

22. The storage device of any one of claims 17-21, wherein the first set of erase parameters includes an initial pulse voltage and an incremental pulse voltage.

23. The storage device of any one of claims 17-22, wherein the adaptive erase circuitry is further configured to:

   in accordance with a determination that one or more erase statistics corresponds to a rate or count of successful erase operations that equals or exceeds an erasure success threshold, establish the second set of erase parameters as the current set of erase parameters by decreasing one or both of: an initial pulse voltage and an incremental pulse voltage of the current set of erase parameters, wherein successful erase operations comprise erase operations having erase durations less than a first duration threshold.

24. The storage device of any one of claims 17-23, wherein the adaptive erase circuitry is further configured to:

   in accordance with a determination that one or more erase statistics corresponds to a rate or count of unsuccessful erase operations that equals or exceeds an erasure failure threshold, establish the second set of erase parameters as the current set of erase parameters by increasing one or both of: an initial pulse voltage and an incremental pulse voltage of the current set of erase parameters, wherein unsuccessful erase operations comprise erase operations having erase durations greater than a second duration threshold.

25. The storage device of any one of claims 17-24, wherein each erase operation of the respective erase operations includes:

   applying a first voltage pulse to one or more portions of the one or more non-volatile memory devices in accordance with the current set of erase parameters; and,

   in accordance with a determination that the one or more portions of the one or more non-volatile memory devices have not been successfully erased, applying one or more subsequent voltage pulses in accordance with the current set of erase parameters until predefined criteria have been met, the predefined criteria including that the one or more portions of the one or more non-volatile memory devices have been successfully erased.
26. The storage device of any one of claims 17-25, wherein each erase operation of the respective erase operations includes:

applying a set of voltage pulses to one or more portions of the one or more non-volatile memory devices in accordance with the current set of erase parameters; and,

in accordance with a determination that the one or more portions of the one or more non-volatile memory devices have not been successfully erased, applying one or more subsequent sets of voltage pulses to the one or more portions of the one or more non-volatile memory devices until second predefined criteria have been met, the second predefined criteria including that the one or more portions of the one or more non-volatile memory devices have been successfully erased.

27. The storage device of claim 26, wherein the adaptive erase circuitry is further configured to:

receive one or more host read commands to read data from one or more memory blocks on the storage device; and,

prior to applying the one or more subsequent sets of voltage pulses to the one or more portions of the one or more non-volatile memory devices, process at least a subset of the one or more host read commands to read data from the one or more memory blocks on the storage device.

28. The storage device of any one of claims 17-27, wherein the adaptive erase circuitry is further configured to:

identify one or more portions of the one or more non-volatile memory devices that fail to satisfy a predefined erasure performance requirement when one or more erase operations are performed using the first set of erase parameters;

subsequent to identifying the one or more portions of the one or more non-volatile memory devices, forgo erase operations on the one or more portions of the one or more non-volatile memory devices using the first set of erase parameters; and,

subsequent to establishing the second set of erase parameters as the current set of erase parameters, perform an erase operation on at least a subset of the identified one or more portions of the one or more non-volatile memory devices using the second set of erase parameters.

29. The storage device of any one of claims 17-28, wherein the one or more controllers comprise a non-volatile memory controller of the storage device, and the one or more erase
statistics correspond to performance of multiple erase operations on portions of one or more non-volatile memory devices coupled to the non-volatile memory controller.

30. The storage device of any one of claims 17-29, including a plurality of non-volatile memory controllers, each coupled to a distinct set of one or more non-volatile memory devices in the storage device, wherein each non-volatile memory controller of the plurality of non-volatile memory controllers of the storage device is configured to independently perform operations, including performing a plurality of memory operations; in accordance with each erase operation of at least a subset of the respective erase operations, updating one or more erase statistics that correspond to performance of multiple erase operations; and, in accordance with a comparison of the erase statistics with an erasure performance threshold, establishing a second set of erase parameters as the current set of erase parameters.

31. The storage device of any one of claims 17-30, wherein the one or more non-volatile memory devices comprise one or more flash memory devices.

32. The storage device of any one of claims 17-31, wherein multiple sets of erase parameters, including the first set of erase parameters and the second set of erase parameters, are stored in non-volatile memory of the storage device.

33. The storage device of any one of claims 17-31, wherein each of the one or more controllers is further configured to, for each erase operation of the respective erase operations, update the one or more erase statistics.

34. A non-transitory computer readable storage medium, storing one or more programs for execution by one or more processors of a storage device having one or more controllers, the one or more programs including instructions for performing the method of any one of claims 1-16.

35. The non-transitory computer readable storage medium of claim 34, wherein the storage device has a plurality of controllers, and the non-transitory computer readable storage medium includes a non-transitory computer readable storage medium for each controller of the plurality of controllers, each having one or more programs including instructions for performing the method of any one of claims 1-16.

36. A storage device, comprising:
a storage controller, including:

means for performing a plurality of memory operations including read operations and respective erase operations on portions of the one or more non-volatile memory devices specified by the read operations and respective erase operations, wherein the respective erase operations are performed using a first set of erase parameters that has been established as a current set of erase parameters prior to performing the respective erase operations;

means, enabled in accordance with each erase operation of at least a subset of the respective erase operations, for updating one or more erase statistics that correspond to performance of multiple erase operations; and

means, enabled in accordance with a comparison of the erase statistics with an erasure performance threshold, for establishing a second set of erase parameters as the current set of erase parameters.

37. The storage device of claim 36, wherein the storage controller includes means configured to operate in accordance with the method of any one of claims 2-16.
Perform a plurality of memory operations including read operations and respective erase operations on portions of one or more non-volatile memory devices specified by the read operations and respective erase operations. The respective erase operations are performed using a first set of erase parameters that has been established as a current set of erase parameters prior to performing the respective erase operations.

The first set of erase parameters includes an initial pulse voltage and an incremental pulse voltage.

Each erase operation of the respective erase operations includes:

Applying a first voltage pulse to one or more portions of the one or more non-volatile memory devices in accordance with the current set of erase parameters.

In accordance with a determination that the one or more portions of the one or more non-volatile memory devices have not been successfully erased, applying one or more subsequent voltage pulses in accordance with the current set of erase parameters until predefined criteria have been met, the predefined criteria including that the one or more portions of the one or more non-volatile memory devices have been successfully erased.

The one or more non-volatile memory devices include one or more flash memory devices.
Perform a plurality of memory operations including read operations and respective erase operations on portions of one or more non-volatile memory devices specified by the read operations and respective erase operations. The respective erase operations are performed using a first set of erase parameters that has been established as a current set of erase parameters prior to performing the respective erase operations.

Each erase operation of the respective erase operations includes:

- Applying a set of voltage pulses to one or more portions of the one or more non-volatile memory devices in accordance with the current set of erase parameters.

In accordance with a determination that the one or more portions of the one or more non-volatile memory devices have not been successfully erased, applying one or more subsequent sets of voltage pulses to the one or more portions of the one or more non-volatile memory devices until second predefined criteria have been met, the second predefined criteria including that the one or more portions of the one or more non-volatile memory devices have been successfully erased.

Receive one or more host read commands to read data from one or more memory blocks on the storage device.

Prior to applying the one or more subsequent sets of voltage pulses to the one or more portions of the one or more non-volatile memory devices, process at least a subset of the one or more host read commands to read data from the one or more memory blocks on the storage device.
In accordance with each erase operation of at least a subset of the respective erase operations, update one or more erase statistics that correspond to performance of multiple erase operations.

The one or more erase statistics include erase operation duration statistics with respect to durations for the multiple erase operations.

For each erase operation of the respective erase operations, update the one or more erase statistics.

Updating the one or more erase statistics that correspond to the performance of the multiple erase operations includes updating at least one of the one or more erase statistics in accordance with how many erase operations, of the multiple erase operations, have a duration that exceeds a predefined duration threshold.

Updating the one or more erase statistics that correspond to the performance of the multiple erase operations includes identifying erase operations, of the multiple erase operations, whose duration exceeds a predefined duration threshold, and updating at least one of the one or more erase statistics in accordance with the identified erase operations.

Figure 3C
In accordance with a comparison of the erase statistics with an erasure performance threshold, establish a second set of erase parameters as the current set of erase parameters.

In accordance with a determination that one or more erase statistics corresponds to a rate or count of successful erase operations that equals or exceeds an erasure success threshold, establish the second set of erase parameters as the current set of erase parameters by decreasing one or both of: an initial pulse voltage and an incremental pulse voltage of the current set of erase parameters.

In accordance with a determination that one or more erase statistics corresponds to a rate or count of unsuccessful erase operations that equals or exceeds an erasure failure threshold, establish the second set of erase parameters as the current set of erase parameters by increasing one or both of: an initial pulse voltage and an incremental pulse voltage of the current set of erase parameters.
D

Identify one or more portions of the one or more non-volatile memory devices that fail to satisfy a predefined erasure performance requirement when one or more erase operations are performed using the first set of erase parameters

Subsequent to identifying the one or more portions of the one or more non-volatile memory devices, forgo erase operations on the one or more portions of the one or more non-volatile memory devices using the first set of erase parameters

Subsequent to establishing the second set of erase parameters as the current set of erase parameters, perform an erase operation on at least a subset of the identified one or more portions of the one or more non-volatile memory devices using the second set of erase parameters

Figure 3E
The method is performed by a non-volatile memory controller of the storage device and the one or more erase statistics correspond to performance of multiple erase operations on portions of one or more non-volatile memory devices coupled to the non-volatile memory controller.

The storage device includes a plurality of non-volatile memory controllers, each coupled to a distinct set of one or more non-volatile memory devices in the storage device, and the method is performed independently by each non-volatile memory controller of the plurality of non-volatile memory controllers of the storage device.

Multiple sets of erase parameters, including the first set of erase parameters and the second set of erase parameters, are stored in non-volatile memory of the storage device.

Figure 3F
According to International Patent Classification (IPC) or to both national classification and IPC:

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C16/34 G11C16/14 G11C11/56

ADD.

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols):

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched:

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used):

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<td>US 2012/239858 AI (MELI K-MARTI ROSIAN ASHOT [US]) 20 September 2012 (2012-09-20)</td>
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<td>A</td>
<td>paragraph [0046] - paragraph [0062] ; figures 5-9 ; paragraph [0037] - paragraph [0041] ; figures 3, 4</td>
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<td>A</td>
<td>paragraph [0027] - paragraph [0048] ; figures 1, 2 ; paragraph [0052] - paragraph [0087] ; figures 3B-7</td>
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Further documents are listed in the continuation of Box C. See patent family annex.

Date of the actual completion of the international search: 12 February 2015

Date of mailing of the international search report: 18/02/2015

Name and mailing address of the ISA:

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
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Authorized officer:

Bal aguer Lopez, J
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<td>US 2009/310422 Al (EDAHIRO TOSHIAKI [JP]) ET AL 17 December 2009 (2009-12-17)</td>
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