

Feb. 2, 1971

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3,560,939

DIGITAL CHANNEL SELECTION APPARATUS

Filed July 5, 1968

3 Sheets-Sheet 1

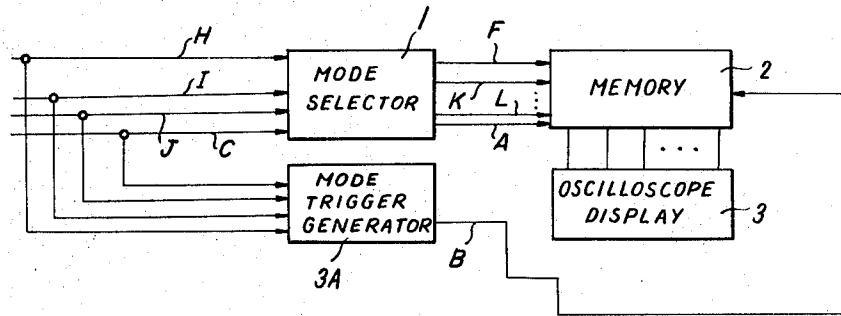


Fig. 1

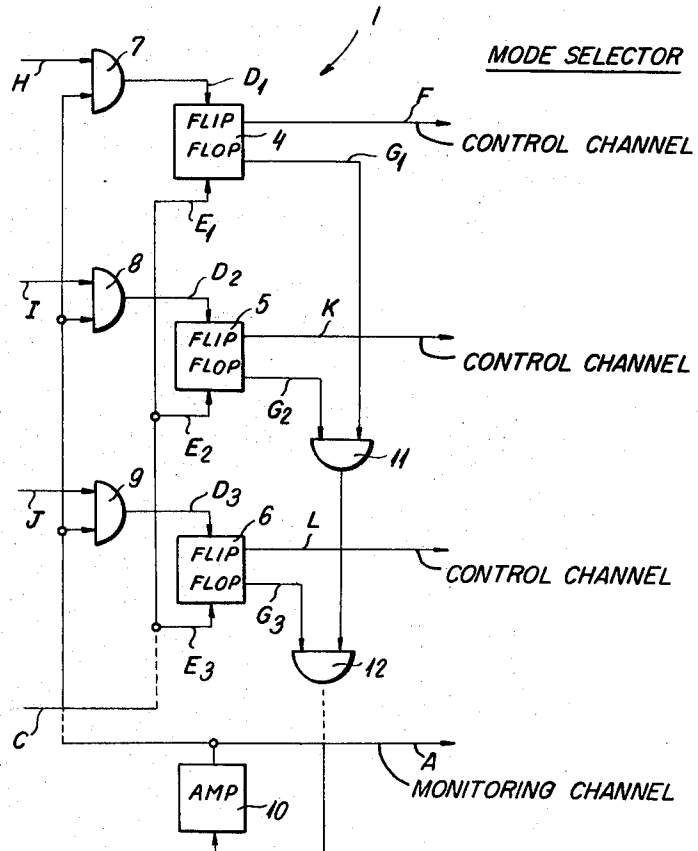


Fig. 2

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3 Sheets-Sheet 2

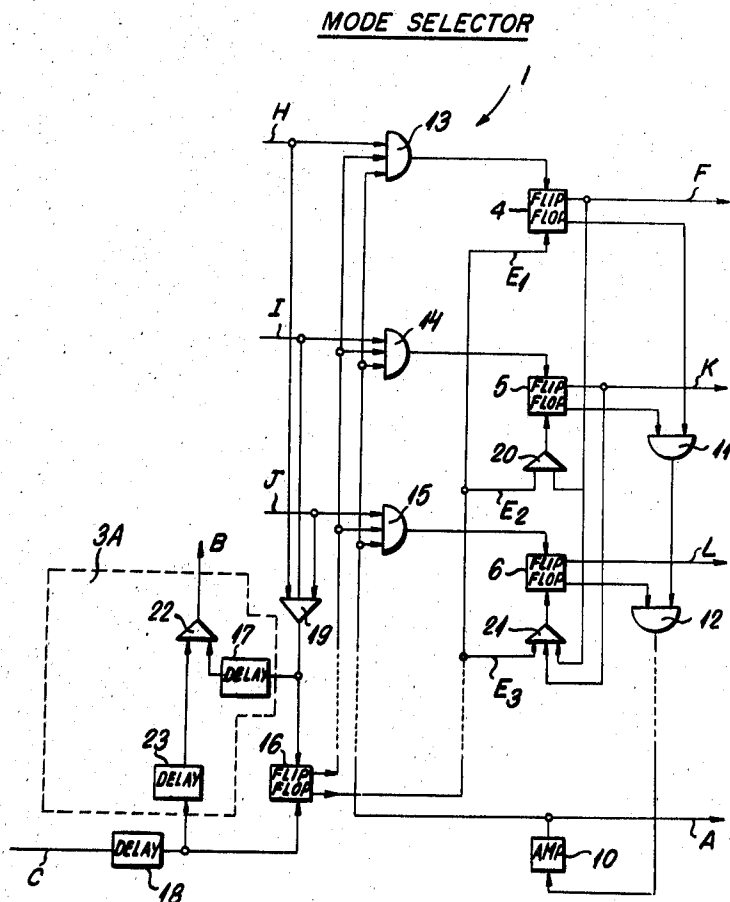


Fig. 3

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RELAY EMBODIMENT OF FIG. 3

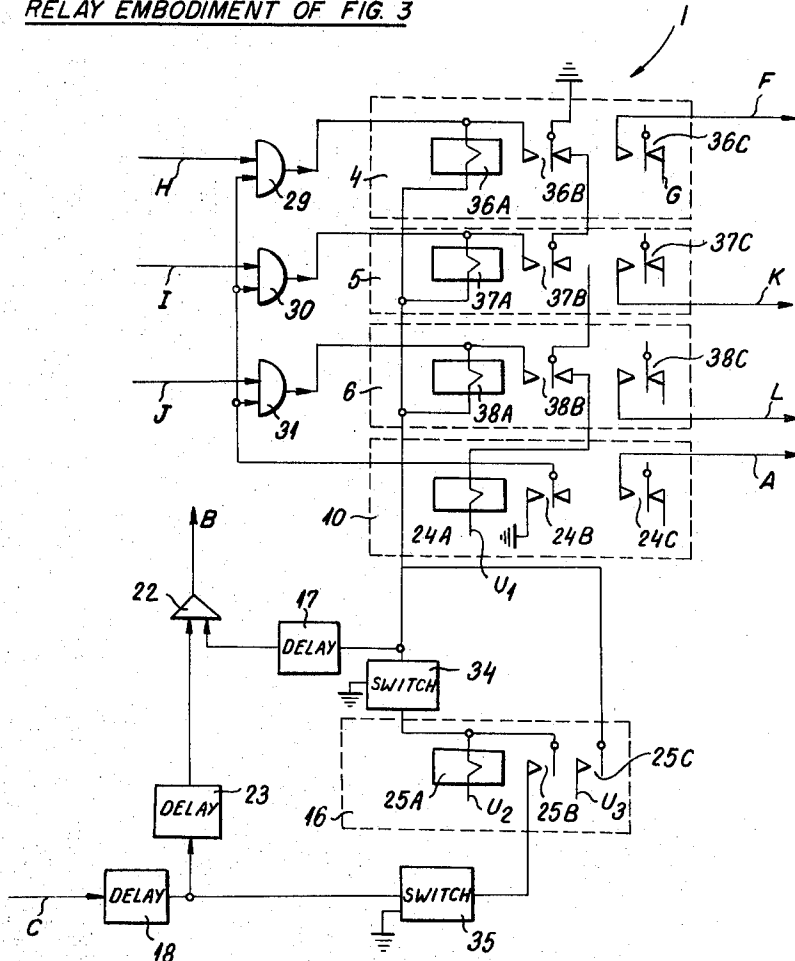


Fig. 4

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DIGITAL CHANNEL SELECTION APPARATUS
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Continuation-in-part of application Ser. No. 541,731, Apr. 11, 1966. This application July 5, 1968, Ser. No. 743,272

Int. Cl. G06f 9/00; H03k 17/00
U.S. Cl. 340—172.5

4 Claims

ABSTRACT OF THE DISCLOSURE

A selection circuit for exciting one of M digital channels (including one monitoring channel and M-1 operating channels) automatically excites the monitoring channel upon the de-excitation of any of the operating channels. Each selected operating channel is energized, and the monitoring channel deenergized, by an associated unique one of M-1 switching pulses. The de-excitation of an operating channel and the simultaneous energizing of the monitoring channel is accomplished by the application of a stop pulse to the last-mentioned operating channel.

RELATED APPLICATIONS

The present case is a continuation-in-part of applicant's copending application Ser. No. 541,731, filed Apr. 11, 1966, now abandoned.

BACKGROUND OF THE INVENTION

In many situations, digital memories are designed to perform a plurality of operations (e.g., arithmetic manipulations, clearing, etc.) in a prescribed time sequence upon the application of discrete commands thereto. The commands are applied over associated unique control channels chosen by a suitable selection circuit. In particular, if the "clearing" mode is desired, such mode is selected by energizing the associated control channel, which conditions the memory in a well-known manner for subsequent operation in this mode. The actual operation of the memory in the clearing mode is commenced a predetermined time after its selection by a suitable trigger pulse applied to the memory.

It is often advantageous, before the selection of each of the various sequential operating modes of the memory, to be able to visually monitor the performance of the memory in carrying out the preceding operating mode to be sure that cumulative errors do not build up in the memory.

Accordingly, the selection circuit may be adapted to energize, in addition to the M control channels, a monitoring channel, which when energized, conditions the memory operation in a "display" mode. When this "display" mode is selected, the application of the subsequent trigger pulse to the memory causes the latter to output the portion of its contents resulting from the preceding mode in analog form to an oscilloscope or the like for evaluation. Such switch-over between the monitoring and the operating modes is now done manually or by employing separate switching circuits.

The problem treated by the instant invention is that of providing, as an integral portion of the above-described selection circuitry, improved means for (a) selecting the monitoring channel automatically upon the termination of each operating mode and for (b) terminating the monitoring mode automatically upon receipt of a command for energizing the next selected control channel in the operation sequence.

SUMMARY OF THE INVENTION

A solution of this problem is provided by a selection circuit constructed in accordance with the invention. A

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plurality of first bistable devices equal in number to the operating channels are individually and selectively set into their first, or operating states by start pulses applied through associated AND gates. The establishment of the first state in the selected first device energizes the corresponding operating channel. The first devices are interconnected to energize the monitoring channel when and only when all the first devices are in their second or reset states.

Once the first state is established, all of the AND gates are disabled until the application of the next stop pulse to the selector circuit to terminate the then-occurring operating mode. At this time, the corresponding first device (which is then in its first or operating state) is switched to its reset state, thereby energizing the monitoring channel. After a prescribed interval in the monitoring mode, the next start pulse may be applied to the first device associated with the newly selected operating channel through its enabled AND gate to switch such first device into its first state and energize its operating channel. The switching of this first device out of its reset state deenergizes the monitoring channel.

With this arrangement, the monitoring channel is automatically energized in the intervals between the stop pulse of one operating mode and the start pulse of the next operating mode.

BRIEF DESCRIPTION OF THE DRAWING

The nature of the invention and its advantages will appear more fully from the following detailed description taken in conjunction with the appended drawing, in which:

FIG. 1 is a block diagram of a mode selection circuit for energizing a selected one of a plurality of operating and monitoring channels together with additional means for triggering operating in the selected mode;

FIG. 2 is a block and schematic diagram of one form of mode selection circuit in accordance with the invention;

FIG. 3 is a block and schematic diagram of another form of mode selection circuit in accordance with the invention, together with one form of mode trigger generator for use therewith; and

FIG. 4 is a block and schematic diagram of a relay-type embodiment of the arrangement of FIG. 3.

DETAILED DESCRIPTION

Referring now in more detail to the drawing, FIG. 1 shows in block form a circuit 1 for selecting the mode of operation of a conventional digital memory 2. It will be assumed that the memory can be employed in either an operating mode (e.g., arithmetic manipulations, clearing, etc.) or a monitoring mode (e.g., oscilloscopic display). The selection of an operating mode is accomplished by exciting an associated one of a plurality of control channels, three of which (designated F, K, and L) are shown. The selection of the monitoring mode is accomplished by exciting a monitoring channel A.

As indicated below, each of the control channels F, K, and L may be energized at separate times by means of momentary switching pulses from a suitable central controller (not shown) via corresponding input lines H, I, and J. (The switching pulses will hereafter sometimes be referred to as start pulses.)

The operating mode corresponding to the selected one of the control channels F, K, and L remains energized for a period starting with the application of a start pulse to the corresponding input line H, I or J and terminating with the application of a momentary stop pulse from the above-mentioned controller (not shown) to the mode selector 1 over a line C. The monitoring channel A is

activated for the purpose of selecting a visual display mode after the termination of each operating mode.

During the occurrence of the monitoring mode, the portion of the contents of the memory 2, resulting from the operation in the preceding mode is converted to analog form in a conventional manner and applied to an oscilloscope display 3. As will be described below, the selection of the monitoring channel A is effected, in accordance with the invention, upon each occurrence of a stop pulse on the line C. The termination of the monitoring mode is triggered by the application of the next start pulse on one of the lines H, I, and J; i.e. by the energizing of the control channel F, K, or L associated therewith.

A trigger pulse generated by a generator 3A is applied to the memory 2 over a channel B for commencing memory operation in the mode selected by the then excited one of the channels F, K, L, and A. For example, if a mode corresponding to the channel F is selected by applying a start pulse to the line H, the memory does not start operation in that mode until the trigger generator 3A applies an excitation pulse to the memory over the line B. In like manner, when the mode corresponding to the excitation of the monitoring channel A is selected by the occurrence of a stop pulse on the line C, the monitoring mode does not commence until a corresponding trigger pulse is applied to the memory over the line B.

It will be understood that the trigger pulses on the line B will be delayed with respect to the immediately preceding ones of (1) the start pulses on the lines H, I, and J, and (2) the stop pulse on the line C.

A schematic diagram of one form of selection circuit 1 of FIG. 1 is shown in FIG. 2. The input lines H, I and J are respectively coupled to the like first inputs of a plurality of AND gates 7, 8, and 9. The outputs of the AND gates 7, 8, and 9 are respectively coupled, via lines D1, D2 and D3 to corresponding first inputs of a plurality of first bistable circuits 4, 5 and 6 (illustratively flip-flops). Each of the flip-flops 4, 5, and 6 manifest first and second alternately establishable stable states. The first state, which is established upon the excitation of the inputs connected to the associated ones of the lines D1, D2, and D3, enables like first outputs of the flip-flops. The first outputs of the flip-flops 4, 5, and 6 are respectively coupled to the control channels F, K, and L. Thus, if the AND gates 7, 8, and 9 are enabled as described below, the presence of a start pulse on one of the incoming lines H, I, and J will be routed through the corresponding one of the AND gates 7, 8, and 9 to establish the first state on the corresponding one of the flip-flops 4, 5, and 6 and to thereby excite the corresponding control channel F, K, or L.

The stop pulses on the line C are applied via lines E1, E2, and E3 to like second inputs of the flip-flops 4, 5, and 6. The presence of the stop pulse at each of the inputs E1, E2, and E3 switches the corresponding flip-flop to its second state, which is manifested by the enabling of a second output thereof coupled to an associated one of a plurality of channels G1, G2, and G3. The channels G1, and G2 are respectively applied to the inputs of an AND gate 11. The channel G3 and the output of the AND gate 11 are respectively applied to the inputs of an AND gate 12. With this arrangement, the gate 12 will manifest an output only when signals simultaneously appear on all of the channels G1, G2, and G3, i.e. when all of the flip-flops 4, 5, and 6 are in their second or reset states.

The output of the AND gate 12 is coupled to the input of an amplifier 10. The output of the amplifier 10 is coupled in parallel to the monitoring channel A and to like second inputs of the AND gates 7, 8, and 9.

In an illustrative operation of the arrangement of FIG. 2, the input lines H, I and J are isolated from the corresponding flip-flop 4, 5, and 6 during each operating mode, i.e., during the energizing of one of the operating channels F, K, and L. In other words, once a start pulse on one of the lines H, I, and J, triggers the associated

flip-flop into its first or operating state, no output appears on the corresponding channel G1, G2, or G3 and no output appears on the AND gate 12. Thus, the second inputs of the AND gates 7, 8, 9, are deenergized. However, as soon as a stop pulse is applied to the lines E1, E2, and E3 to terminate the operating mode, the flip-flop associated with the operated channel F, K, or L is switched back into its reset state so that an output appears on each of the channels G1, G2, and G3. The resulting output of the AND gate 12 energizes the monitoring channel A and simultaneously enables the gates 7, 8, and 9. Thus, at the termination of the monitoring interval, a start pulse may be applied over a selected one of the lines H, I, and J to switch the corresponding flip-flop 4, 5, or 6 to its first state and energize the channel F, K, or L, thereby selecting a new operating mode.

It will be understood from the preceding discussion that only one of the lines H, I, and J will be energized at any given time, and that the particular ones of the flip-flops 4, 5, and 6 corresponding to the unenergized lines will be in their reset states.

An alternative form of the arrangement of FIG. 2 is shown in FIG. 3. Corresponding elements in FIGS. 2 and 3 have been given corresponding reference numerals. The AND gates 13, 14, and 15 of FIG. 3 correspond to the AND gates 7, 8, and 9 of FIG. 2 except that the gates 13, 14, and 15 (FIG. 3) are additionally provided with like third inputs. In addition, the stop pulses on the line C are coupled to the lines E1, E2, and E3 via one input of a second bistable device 16 (illustratively a flip-flop). The other input of the flip-flop 16 is coupled to the output of an OR gate 19, whose inputs are respectively coupled to the input lines H, I, and J. One output of the flip-flop 16 is coupled to the third inputs of the AND gates 13, 14, and 15, and is enabled each time a switching pulse appears on one of the input lines H, I, and J. The other output of the flip-flop 16 is coupled to the lines E1, E2, and E3, and is enabled each time a stop pulse (which may be retarded by a suitable delay circuit 18) is applied to the line C.

In order to insure that only one of the flip-flops 4, 5, and 6 is switched into its first state despite the accidental appearance of a switching pulse on more than one of the lines H, I, and J, the arrangement of FIG. 3 employs a pair of OR gates 20 and 21 whose outputs are coupled to the second inputs of the flip-flops 5 and 6, respectively. A first input of the OR gate 20 is coupled to the line E2. A second input of the OR gate 20 is coupled to the control channel F. A first input of the OR gate 21 is coupled to the line E3, while an additional pair of inputs thereof are respectively coupled to the control channels F and K. In this way, if the flip-flop 4 is in its first state, the second or reset input of the flip-flops 5 and 6 will always be excited to prevent the switching of the flip-flops 5 and 6 out of their reset states. In like manner, if either of the flip-flop 4 or 5 is switched into its first state, the second input of the flip-flop 6 will be excited to prevent the switching of the flip-flop 6 out of its reset state.

FIG. 3 further illustrates one embodiment of the mode trigger generator 3A. The input lines H, I, and J are coupled to one input of an OR gate 22 through the OR gate 19 and a delay network 17. In addition, the input line C is coupled to the other input of the OR gate 22 through the delay network 18 and an additional delay network 23. The output of the OR gate 22 is the line B, which triggers the commencement of the then-selected mode in the memory 2 (FIG. 1). The delay lines 17 and 23 (FIG. 3) respectively establish the required retardation between the selection of the modes represented by the enabling of the channels F, K, L, and A, and the subsequent triggering of operation of the memory in the selected modes.

A relay-type embodiment of the mode selection circuit 1 of FIG. 3 is shown in FIG. 4. It will be assumed for purposes of discussion that the control channel F is initially energized. Accordingly, the bistable device 4 associated

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with the selected channel F will have been placed in its first state by the prior application thereto of a start pulse on the line H through an AND gate 29, which may be analogous to the gate 13 of FIG. 3. The bistable devices 5 and 6 (FIG. 4) respectively associated with the non-selected control channels K and L are initially in the second or reset states, and will remain so until an associated one of the start pulses on the line I or J is applied thereto through one of gates 30 and 31. The latter may be analogous to the gates 14 and 15 of FIG. 3.

The bistable circuit 16 which by analogy to FIG. 3 is also in its first state when the control channel F is energized, includes a relay 25 (FIG. 4) having a coil 25A and a pair of ganged, normally open contacts 25B and 25C. The first state of the circuit 16 is represented by the operated condition of the relay 25 i.e., the energized condition of its coil 25A. Initially therefore the contacts 25B and 25C are closed, although it will be observed that such contacts, as well as all other relay contacts in FIG. 4, are shown unoperated for purposes of clarity. The coil 25A is locked up in its energized condition from a source U2 to ground through the closed contacts 25B and a conventional controllable switch 35, which normally provides a short circuit to ground except when a stop pulse is applied thereto over the line C via the delay circuit 18.

The bistable circuit 4 is represented by a relay 36 having a coil 36A and two pairs of transfer contacts 36B and 36C. The first condition of the relay 36 is manifested by the energized condition of the coil 36A, so that the associated transfer contacts 36B and 36C will be initially in their left hand position as viewed in FIG. 4. The initial selection of the control channel F is represented by the left hand position of the contacts 36C.

The unoperated bistable devices 5 and 6 are represented by initially unoperated relays 37 and 38 respectively having coils 37A and 38A and two sets of transfer contacts 37B-37C and 38B-38C. The contacts 37C and 38C, being unoperated, are in their right hand position, which is representative of the non-selection of the associated control channels K and L.

During the period of selection of the control channel F, the coil 36A is locked up in its energized condition from a source U3 to ground through the operated contacts 25C and the left-hand position of the operated contacts 36B.

In order to terminate the energizing of the control channel F and to energize the monitoring channel A a momentary stop pulse is applied over the line C. The stop pulse is applied through the delay element 18 to decouple the switch 35 from ground, thereby breaking the lock-up path of the relay 25. The coil 25A is therefore deenergized and releases the contacts 25B and 25C, which switches the bistable device 16 represented by the relay 25 into its second or reset state. The release of the contacts 25C opens the lock-up path of the coil 36A, which releases the contacts 36B and 36C. The resulting movement of the contacts 36C to their right-hand position deenergizes the control channel F. At the same time the movement of the contacts 36B to their right-hand position completes a serial energizing path from a source U1 to ground for a coil 24A of a relay 24 through the right-hand positions of the contacts 36B, 37B, and 38B. The relay 24 represents the amplifier 10 of FIG. 3.

The operation of the contacts 24B conditions the gates 29, 30, and 31 for operation by grounding one input thereof so that a selected one of the gates may be subsequently opened by the application thereto of a start pulse over one of the lines H, I, and J. At the same time, the operation of the contacts 24C energizes the monitoring channel A to start the monitoring interval.

In order to subsequently terminate the monitoring interval on the channel A and to energize the next selected one of the control channels (illustratively K), the gate 30 is opened by applying a start pulse over the input line I to the gate 30. A conventional controllable switch 34, which may be identical to the switch 35, is now grounded through

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the coil 37A, the open gate 30, and the operated contact 24B. In response, the switch 34 completes an energizing path from the source U2 to ground for the coil 25A of the relay 25. The contacts 25B and 25C are thereupon operated. In the absence of the stop pulse on the line C, therefore, a lockup path is again established between the source U3 and ground for the coil 25A through the operated contact 25B and the switch 35, which again provides a short circuit to ground. Thus, the bistable device 16 represented by the relay 25 is again placed in its first state. At this point, an energized path for the coil 37A associated with the now-selected control channel K is momentarily established from the source U3 to ground through the operated contacts 25C the open gate 30 and the operated contacts 24B. The resulting movement of the contact 37B locks up the coil 37A from the source U3 to ground through the operated contacts 25C and 37B thereby establishing the first state of the bistable device represented by the relay 37. The corresponding movement of the contacts 37C to their left-hand position energizes the channel K to start the next control mode.

The movement of the contacts 37B to their left-hand position also breaks the energizing path for the coil 24A, thereby causing the release of the contacts 24B and 24C. The movement of the contacts 24C to their right-hand position disables the channel A and terminates the monitoring mode. It will be understood that the energizing of the control channel K and the deenergizing of the monitoring channel A may be substantially coincident.

In an analogous manner similar sequences of relay operations may be subsequently employed to (1) disable the control channel K; (2) simultaneously re-enable the monitoring channel A; (3) disable the monitoring channel A after a selected interval; (4) enable the next control channel L in response to a switching pulse J on the line 102; and so forth. In this way, the monitoring channel A is automatically energized over the entire interval between the disabling of one selected control channel and the enabling of the next selected control channel.

In the foregoing, the invention has been described in connection with preferred arrangements thereof. Many modifications will now occur to those skilled in the art. It is, accordingly, desired, that the scope of the appended claims not be limited to the specific disclosure herein contained.

What is claimed is:

1. For use in combination with N first digital control channels that are energizable over separate mutually spaced periods framed by start and stop pulses, apparatus for automatically energizing a second digital monitoring channel in the intervals between stop signal of one period and the start signal of the succeeding period, which comprises:

N first coincidence gating means;

N first bistable devices each having alternately establishable first and second states, the establishing of the first state enabling a first output of the first device and the establishing of the second state enabling a second output thereof;

means individually coupling the outputs of the first gating means to the first devices for establishing the first state when the associated first gating means is operated;

a second coincidence gating means;

means for individually coupling the first outputs of the first devices to the first channels;

means for coupling the second outputs of the first devices to the inputs of the second gating means to operate the second gating means when all of the first devices are in their second states;

first means coupling the output of the second gating means to the second channel for energizing the second channel when the second gating means are operated;

second means coupling the output of the second gat-

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ing means to one input of each of the first gating means for conditioning the first gating means; means for individually coupling the start pulses to the other inputs of the conditioned first gating means to operate the associated one of the conditioned first gating means; and means coupling the stop pulses to each of the first devices for establishing the reset states thereof.

2. Apparatus as defined in claim 1, in which the first gating means is provided with an additional input, and the means for establishing the reset states comprises, in combination, a second bistable device having alternately establishable third and fourth states, the establishing of the third state enabling a first output of the second device and the establishing of the fourth state enabling a second output of the second device; means individually coupling the start pulses to the second device for establishing the third state; means individually coupling the stop pulses to the second device to establish the fourth state; means for coupling the first output of the second device to the additional input of the first gating means; and means for coupling the second output of the second device to each of the first devices to establish the reset states therein.

3. Apparatus as defined in claim 2, in which the means for coupling the second output of the second device comprises, in combination (N-1), first OR gates having out-

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puts individually coupled to the first devices to establish the first states, and first inputs coupled to the second output of the second device; and means for selectively coupling the first outputs of the first devices to second inputs of the first OR gates for preventing the simultaneous establishment of the first state in more than one of the first devices.

4. Apparatus as defined in claim 1, further comprising means for generating triggering pulses in timed relation to the occurrence of each of the start and stop pulses, the generating means comprising, in combination, a second OR gate, the trigger pulses selectively appearing on the output of the second OR gate; first delay means for coupling the start pulses to a first input of the second OR gate; and second delay means for coupling the stop pulses to a second input of the second OR gate.

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