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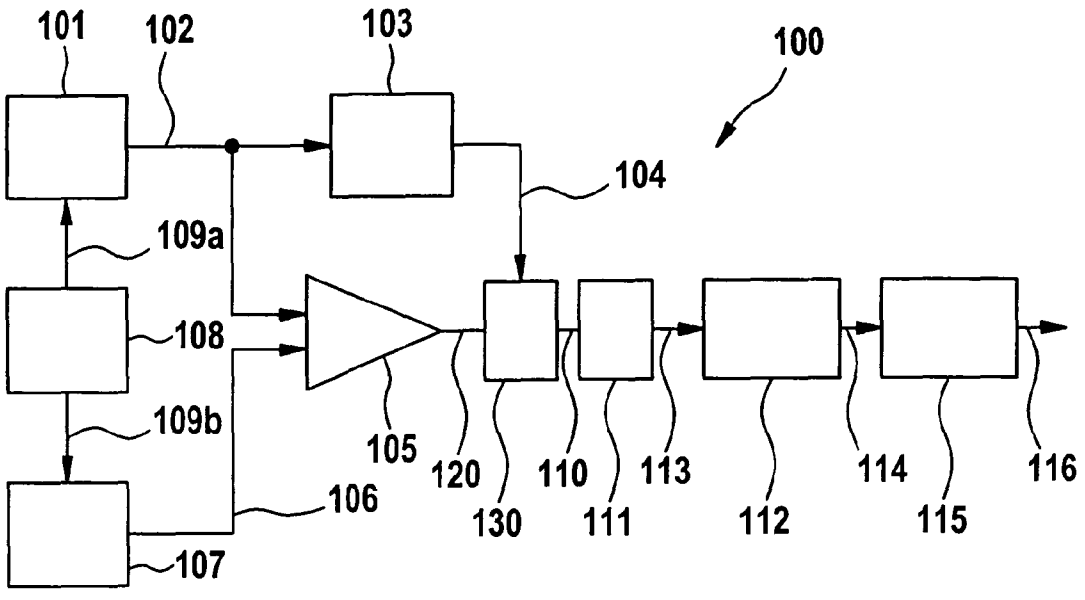
(54) **Title:** CONVERTING NON-EQUIDISTANT SIGNALS INTO EQUIDISTANT SIGNALS



(57) **Abstract:** A signal processing device (100), preferably an undersampling ADC using coherent sampling, is presented for processing a signal (102) , the signal processing device (100) comprising a comparator unit (105) for comparing the signal (102) with a reference signal (106), a generation unit (105, 130) for generating digital result signals (110) indicative of the result of the comparing, an evaluation unit (112) for determining transition times of the digital result signals (110), and an output signal calculation unit (115) adapted for calculating essentially uniformly spaced output signals (116).

WO 2008/022653 A1

DESCRIPTION

CONVERTING NON-EQUIDISTANT SIGNALS INTO EQUIDISTANT SIGNALS

BACKGROUND ART

[0001] The present invention relates to signal processing.

[0002] US 6,462,693 B1 by the same applicant Agilent Technologies discloses converting an analog signal into a quantity of digital signal representations. The method comprises the step of comparing an amplitude value in the analog signal to a quantity of reference amplitude values to determine whether the analog value is greater than or less than a reference value. The method further comprises the step of producing a logic level in a digital signal corresponding to the determination in the step of comparing. The method essentially converts the analog signal to a time representation and then converts the time representation to a digital representation. The apparatus comprises a quantity of comparators each connected to receive the analog signal, separately to receive a different one of the reference values, and to produce the digital signal. The analog signal is reconstructed from the digital representation.

[0003] US 6,429,799 B1 by the same applicant Agilent Technologies discloses converting an analog signal into a digital representation. The method comprises the steps of generating a quantity of time-varying reference signals, comparing an amplitude of the analog signal to an amplitude of each of the reference signals to determine whether the analog signal amplitude is greater than, less than or equal to reference signal amplitudes, and producing a timestamp each time the analog signal and reference signal amplitudes are equal. The apparatus comprises a reference signal generator and a quantity of comparators, each of the comparators being connected to receive the analog signal, separately to receive a different one of the reference signals, and to produce a digital signal. The analog signal may be reconstructed from the digital representation.

[0004] US 2004/0070529 A1 by the same applicant Agilent Technologies discloses

preconditioning an analog signal and converting the preconditioned signal into a digital representation. The method comprises preconditioning the analog signal, generating a quantity of reference signals, comparing an amplitude of the preconditioned signal to an amplitude of the reference signals to determine whether the preconditioned signal amplitude is greater than, less than or equal to reference signal amplitudes, and producing a timestamp at a time that the preconditioned signal and reference signal amplitudes are equal. The apparatus comprises a preconditioner, a reference signal generator and a quantity of comparators. A comparator of the quantity of comparators receives the preconditioned signal from the preconditioner, separately receives a reference signal, and produces a digital signal. The preconditioned signal or the analog signal may be reconstructed from the digital representation.

[0005] S. Sunter, "An Automated, Complete, Structural Test Solution for SERDES", IEEE International Test Conference, 2004, pp. 95-104, discloses jitter test of Gigahertz serialization and deserialization (SERDES) which has become a dominant inter-chip and interboard data transmission technique. Signal integrity is the primary factor determining its bit error rate, typically less than 10^{-12}, so the primary production test challenges are testing picosecond jitter and the signal eye opening. Off-chip jitter and rise/fall time measurements are limited by hardware complexity, access, bandwidth, and noise. Published on-chip measurement techniques are limited by delay line jitter. This paper presents a new jitter test technique that has been demonstrated on an FPGA to achieve less than 1 ps RMS self-jitter, and a new signal eye test that has unlimited bandwidth; neither test uses high speed circuitry. The all-digital technique uses the receiver itself to demodulate the signal jitter to a low-speed bit stream that is analyzed by a single-clock domain, synthesizable circuit. This is combined with logic BIST and 1149.6 boundary scan to completely test an IC.

[0006] However, there is still a need for efficient signal processing.

DISCLOSURE

[0007] It is an object of the invention to enable efficient signal processing. The object is solved by the independent claims. Further embodiments are shown by the dependent claims.

[0008] According to an exemplary embodiment of the present invention, a signal processing device for processing a signal is provided, the signal processing device comprising a comparator unit for comparing the signal with a reference signal, a generation unit for generating digital result signals indicative of the result of the comparing, an evaluation unit for determining transition times of the digital result signals, and an output signal calculation unit adapted for calculating essentially uniformly spaced output signals (based on the, for instance non-equidistant, digital result signals).

[0009] According to another exemplary embodiment, a measurement apparatus is provided, the measurement apparatus comprising a signal processing device having the above-mentioned features for processing a (for instance repetitive) signal related to a measurement carried out by the measurement apparatus.

[0010] According to still another exemplary embodiment, a signal processing method of processing a signal is provided, the method comprising comparing the signal with a reference signal, generating digital result signals indicative of the result of the comparing, determining transition times of the digital result signals, and calculating essentially uniformly spaced output signals (for instance based on the digital result signals).

[0011] According to yet another exemplary embodiment, a computer-readable medium is provided, in which a computer program of processing a signal is stored, which computer program, when being executed by a processor, is adapted to control or carry out the above-mentioned method.

[0012] According to a further exemplary embodiment, a program element of processing a signal is provided, which program element, when being executed by a processor, is adapted to control or carry out the above-mentioned method.

[0013] Embodiments of the invention can be partly or entirely embodied or supported by one or more suitable software programs, which can be stored on or otherwise provided by any kind of data carrier, and which might be executed in or by any suitable data processing unit. Software programs or routines can be preferably applied for processing a signal. The signal processing according to an embodiment of

the invention can be performed by a computer program, i.e. by software, or by using one or more special electronic optimization circuits, i.e. in hardware, or in hybrid form, i.e. using software components and hardware components.

[0014] According to an exemplary embodiment, non-equidistant signals obtained with any signal processing scheme may be manipulated to thereby generate signals being essentially equidistant (for example in the time domain). Thus, a uniform signal reconstruction scheme may be provided allowing to provide output signals in a format which is in some sort "standardized" (with respect to a time sequence of the signals) and therefore suitable for many post-processing schemes.

[0015] According to an exemplary embodiment, a signal having some kind of periodicity (so as to be repeated several times) is processed by undersampling. In this context, the term "undersampling" may denote a sampling scheme in which a signal is sampled with a sample rate that is less than twice the single bandwidth. After having determined several points in time at which the sampling shall be carried out, for instance essentially equidistant points of time, the repetitive signal is compared with a compare or reference signal at these points in time. The result of this comparison may be that the repetitive signal is larger than the reference signal, is smaller than the reference signal or is equal to the reference signal. Thus, some kind of digital result signal may be generated indicative of a result of this comparison. Information about the repetitive signal may be "encoded" in the points of time at which a transition of this digital result signal form "0" to "1", or vice versa, occurs. In other words, an information about the signal to be processed may be included in points of time at which a transition of the logical value of the result of the comparison occurs. The analog signal may be reconstructed from the digital representation.

[0016] It may be advantageous to perform so-called "coherent sampling", that is to say to ensure a defined time correlation between the operation of the individual components of the signal processing device, particularly of the unit generating the reference signal and the determining signal. Such a coherence may be obtained, for instance, by providing a common clock signal for such components, or by strictly linking or coupling the timing of such components, for instance using frequency locking or the like.

[0017] More particularly, undersampling of an analog signal using coherent digital automatic test equipment (ATE) channels may be performed.

[0018] For testing electronic devices, in particular integrated electronic circuits providing digital electronic output signals, a test or stimulus signal may be fed to an input of the device under test (DUT), and the response signal from the device under test may be evaluated by an automatic test equipment, for instance by comparison with expected data. Such an automatic test equipment may have included a particular test functionality, that is to say test functions or routines which the test equipment may carry out. The test functionality may be incorporated in a test equipment in the form of executable software code. When test signals, which may be repetitive signals, are transmitted within such an electronic test device, it may also happen that signals are converted between analog and digital format. In order to perform such a conversion, the undersampling feature according to an exemplary embodiment may be implemented. Benefit may be taken from the fact that such stimulus signals and/or response signals may have a certain periodicity, that is to say may be repetitive signals.

[0019] Exemplary embodiments may transform results of such a data processing into a "standard" ADC (analog-to-digital converter) result format. For instance, after having undersampled the repetitive signal a plurality of times with different points of time within the periodicity of the repetitive signal, it may be advantageous to resort the data points so as to get interpolations between data points with each new iteration of the repetitive signal. However, by performing such a resorting, the equidistant character of the signals may be influenced, so that the output signals may be non-equidistantly. Embodiments of the invention may take such non-equidistant signals and post-process them so as to derive an essentially equidistant sequence of output signals, for instance essentially equidistant in time or in frequency.

[0020] Particularly, embodiments of the invention may be implemented within an Analog-to-Digital Converter (ADC) in which an analog signal shall be digitized. In other words, an analog waveform may be converted to a digital signal. In this context, a repetitive signal may be undersampled. In this context, the term "analog" may denote a signal having a continuous level (for instance a modulated radio frequency signal). The

term "digital" may particularly denote a signal having discrete levels (for instance a logical value "1" or "0").

[0021] An exemplary field of application of embodiments of the invention is "automatic test equipment", i.e. the digitalization of analog test signals in the context of testing a device under test (DUT). Since such a test may be repeatable, thus the concept of undersampling a repetitive signal may be applied.

[0022] The term "coherent sampling" may be particularly understood as to be as sub-form of "undersampling". "Undersampling" may denote that the sampling is performed in a slower manner or with a slower sample rate than necessary to capture all required information without repetition. In the context of "coherent sampling", a defined ratio between the sample period and the repetition time of the signal may be ensured or adjusted. When performing such an undersampling, preferably using coherent sampling, the information to be derived is encoded in the transition times of the digital compare signal. The signal is analyzed a plurality of times, for instance three times. For each iteration, new intermediate measurement points are obtained which successively refine the measurement. "Digital undersampling" may be carried out with the goal to measure the transition times or timestamps with increased accuracy. For such a coherent measurement of transition times, the repetitive signal is sampled a plurality of times, and a fractional frequency ratio between signal frequency and sample rate may be selected. Taking this measure, intermediate sample points may be generated, thereby increasing accuracy of the determined transition times. Accuracy may particularly be increased by repeating the waveform a large number of times, and by selecting a sufficiently high sample rate.

[0023] According to an exemplary embodiment, an analog-to-digital converter implementing coherent sampling for measuring transition times for reconstructing an analog waveform may be provided. Particularly, such an ADC may be implemented advantageously within a measurement device, like a test device for testing a device under test (DUT).

[0024] A control clock unit may provide a clock signal which can be used globally by the signal processing device, thereby enabling coherent time stamping. Coherent sampling may increase accuracy of the sampling at the determined points of time.

[0025] Therefore, according to an exemplary embodiment, undersampling (or some kind of digitization) of repetitive analog signals, including modulated RF signals, may be performed. Such signals may particularly have a frequency range between 100 MHz and 10 GHz. As a modulation scheme, amplitude modulation, frequency modulation or face modulation may be used, for instance.

[0026] Such an undersampling may be embedded in the field of automatic test equipment (ATE), where mixed signal/RF tests are performed and where signals can be made repetitive. Thus, any technical field in which repetitive signals occur may be a potential field of application of exemplary embodiments. In many cases, test criteria assume access uniformly the space samples, like from a conventional ADC, or assume access to the signal spectrum.

[0027] The term "digital" may denote two levels, independent of time. The term "analog" may denote that the levels are continuous, independent of time. Analog signals may include modulated RF signals. The term "coherent" may denote an N/M frequency or period ratio, wherein N may be the number of sample points and M may be the number of repetitions of the signal to be sampled, and wherein N and M are coprime.

[0028] According to an exemplary embodiment, a signal processing device may be provided in which a repetitive analog signal is evaluated. For such an analog signal, a comparison to a known level or to known levels or to any other waveform may be performed. The result of such a comparison may be a digital signal. The digital compare signal may then be coherently sampled so as to obtain digital samples. Next, precise transition times may be determined of compare signals from digital samples. Samples may be constructed using the transition times plus the levels of the known waveform at the transition times.

[0029] Optionally, it is possible to compare the repetitive signal to one static level, multiple static levels, sine waves, other dynamic waveforms, or preconditioned signals. It is possible to use a digital ATE channel as coherent sampler. Furthermore, jitter may be selectively added to the signal to improve resolution/accuracy. When detecting transitions, the "first" signal after the transition may be determined, the "last" signal before the transition may be determined, a "mid" time between the last and the first

point may be determined, or a "count" may be performed in an interval between measurement points before and after a transition.

[0030] According to another exemplary embodiment, an analog signal may be processed by the signal processing device. The analog signal may be compared to known levels. Afterwards, transition times of the compare signal may be determined. Samples may be constructed. These samples may be transformed into a usual "ADC" format. In this context, an interpolation may be performed, NUFFT (Non-Uniform Fast Fourier Transformation) may be performed, and/or a Non-Uniform Discrete Fourier Transformation (NUDFT) may be performed. In the context of the NUDFT, it is possible to perform a direct down conversion of (modulated) RF signals. It is also possible to perform an offset correction by including DC term in NUDFT. Spur suppression may be enabled by including known spur frequencies in NUDFT. Furthermore, noise suppression may be carried out. It is possible to use equally spaced frequencies in a single contiguous frequency range, like in a conventional FFT.

[0031] According to an exemplary embodiment, an RF receiver using digital ATE channel may be provided. In this context, a (modulated) narrowband (RF) signal may be used. It may be compared to one (or more) static level(s). A digital ATE channel may be used for coherent sampling. Accurate crossing times may be determined. A narrowband spectrum may be reconstructed (NUDFT). The result may be down-converted by simple frequency shifting.

[0032] Next, further exemplary embodiments of the invention will be explained.

[0033] In the following, further exemplary embodiments of the signal processing device will be explained. However, these embodiments also apply for the measurement apparatus, for the method, for the program element and for the computer-readable medium.

[0034] The signal processing device may be adapted for processing a repetitive analog signal. Such an analog signal may represent any continuous value. The term repetitive may have the meaning that the signal has some kind of periodicity and is repeated a plurality of times.

[0035] Furthermore, the signal processing device may be adapted for processing a repetitive modulated radio frequency (RF) signal. Particularly, such a signal processing may be performed in the context of an RF receiver.

[0036] The signal processing device may be adapted as an Analog-to-Digital Converter (ADC) for converting a repetitive analog signal into a digital signal. Implementing the coherent sampling in such a conversion may allow to perform the conversion with high precision. Recalculating the result signal so as to obtain equidistantly spaced result signals may simplify the post-processing of such a converted signal.

[0037] The determining unit may be adapted for determining different points of time for each of a plurality of repetitions. When different periods of such a repeated signal are compared based on different repetitions, the sampled points of subsequent periods may be shifted with respect to one another. By taking this measure, intermediate points of the sampling may be obtained so as to refine the analysis.

[0038] The determining unit may be adapted for determining different points of time for each of a plurality of repetitions so as to obtain essentially uniformly spaced time data. By selecting the ratio between sampled points and number of transitions to be a non-integer value, this uniform spaced time feature may be combined with an efficient way of obtaining intermediate points for each repetition of the signal.

[0039] The reference signal may be one of the group consisting of a single signal being constant in time, a plurality of signals each being constant in time, a signal varying in time in accordance with a predefined waveform, and a sine signal. However, any other waveforms are possible, for instance any trigonometric function, a saw tooth function, a step function, etc.

[0040] The evaluation unit may be adapted for determining the transition times taking into account the signal at points of time related to different ones of a plurality of repetitions. Thus, different repetition sample signals may be combined to increase accuracy, particularly to obtain intermediate signals between two data points. This may refine the data format conversion.

[0041] The number of points of times may be larger than the number of repetitions. The ratio between the number of points of time and the number of repetitions may be a non-integer value. The latter measure may ensure that additional repetitions provide additional information about the signal.

[0042] Advantageously, the signal processing device may comprise a sorting unit adapted for sorting the digital result signals related to different repetitions in accordance with a chronology of the corresponding points of time within the periodicity of the repetitive signal. By resorting or reordering the signals after undersampling, the number of points in the environment of a transition of the digital result signal may be refined.

[0043] The generation unit may be adapted for generating a digital result signal having a first logical value (for instance "1") in case that the respective repetitive signal is larger than the reference signal, and may be adapted for generating a digital result signal having a second logical value (for instance "0") in case that the respective repetitive signal is smaller than the reference signal. Therefore, the transition time may be calculated as a point of time at which a transition from the first logical value to the second logical value occurs. For this purpose, the evaluation unit may determine the transition times based on an analysis of the last point of time in a sequence in which the digital result signal has the first logical value. Alternatively, a first point of time may be determined as the time of transition in a sequence in which the digital result signal has the second logical value. It is also possible to calculate an average time between this last point of time of the first logical value and the first point of time of the second logical value.

[0044] Alternatively, it is possible to further refine the accuracy of estimating the transition time by performing a statistical analysis of a transition interval. For instance, due to effects like jitter, noise or other signal distortions, it may happen that around a transition time, a sequence of alternating values of the first logical value and the second logical value may occur. In such a scenario, it may be more reasonable to statistically analyze the data points in this region and calculate a (most) probable transition time. This may include interpolation, statistically averaging, fitting a mathematical probability function to the determined digital values (some kind of

thermometer code), for instance a cumulative probability density function, etc.

[0045] The evaluation unit may be adapted to determine the transition times according to an operation mode which is selected in accordance with a degree of presence of signal jitter or signal noise. When signal jitter/noise is large, it is relatively likely that signal distortions occur and that the transition interval comprises some distorted measurement points. When signal jitter is small, the numerically more easy solution may be preferred, namely to use the last time of the first logical value or the first point of time of the second logical value, or an average thereof, as an actual transition time.

[0046] The signal processing device may comprise an output signal calculation unit adapted for calculating essentially uniformly spaced output signals. By the reordering, the equidistance may be achieved. However, it may be desirable for post-processing of the signals, that the signals are essentially uniformly spaced, particularly uniformly spaced in time or uniformly spaced in frequency.

[0047] In order to obtain such a uniformly spaced signal, the output signal calculation unit may be adapted for determining the essentially uniformly spaced output signals by using a Sinc interpolation (that is to say a mathematical function being formed by the ratio of the sine of the argument and the argument, wherein the argument may be the time), a polynomial interpolation (for example a Lagrange interpolation, a spline interpolation, or a linear interpolation). It is also possible to implement a fractional delay filter.

[0048] The output signal calculation unit may be adapted for calculating the output signal by performing at least one of the group consisting of a Fast Fourier Transformation (FFT), a Non-Uniform Fast Fourier Transformation (NUFFT), a Non-Uniform Fast Fourier Transformation (NUFFT) with Fast Multipole Method (FMM), and a Non-Uniform Discrete Fourier Transformation (NUDFT). Particularly, the signal processing device may be adapted for processing the repetitive signal using coherent sampling. Coherent sampling may denote that the time properties of the sampling are well-established.

[0049] Coherent sampling may be enabled by implementing a clock generating unit

adapted for generating a common clock signal for a plurality of components of the signal processing device. For instance, such a clock generating unit may supply a common clock signal to a device under test, to a reference signal generator for generating the reference signal and to a unit for evaluating or processing the compare signal. Thus, the clock generating unit may generate a common clock signal for a part of or for all components of the signal processing device.

[0050] Alternatively, a plurality of clock generating units may be provided, each adapted for generating an individual clock signal for an assigned component of the signal processing device, wherein the plurality of clock generating units may be frequency-locked. For instance, three frequency-locked generators with the same output frequencies may be provided to generate individual clock signals for the device under test, a reference signal generator and a unit for evaluating the compare signal.

[0051] Further alternatively, three independent clock generators with sufficient precision to ensure the desired output frequencies may be implemented.

[0052] The signal processing device may further comprise a jitter adding unit adapted to selectively add jitter to the repetitive signal and/or to the compare signal and/or to the coherent sample clock. By taking this measure, the signal may be smeared out in a defined manner which may increase accuracy of the signal conversion.

[0053] The signal processing device may comprise an automatic test equipment unit (ATE) providing an environment for the DUT so that the DUT is a source for providing the repetitive signal, like an Agilent 93000 test apparatus. Thus, the signal processing device may particularly be implemented as an ADC of an such an ATE for testing a device under test, for instance a chip for a mobile phone. Such an automatic test equipment may provide an environment for the DUT so that the DUT is the source for providing the repetitive signal, and may be implemented for testing a device under test.

[0054] In the following, further exemplary embodiments of the measurement apparatus will be explained. However, these embodiments also apply to the signal processing device, to the method, to the program element and to the computer-

readable medium.

[0055] A signal generation unit of the measurement apparatus may be adapted to generate, as the repetitive signal or as a basis for a repetitive signal, a stimulus signal to be applied to a device under test for testing the device under test. It is also possible that the DUT generates a repetitive signal based on a (repetitive or non-repetitive) stimulus signal of the measurement apparatus. Such a stimulus signal may be any signal pattern which is applied to pins of a DUT, for instance a chip to be tested, and a response signal can be detected at other pins of the DUT. By comparing such response signals with expected signals, it may be determined whether the device under test is acceptable or has to be rejected. When applying test sequences to such a device under test, the signals are usually repeated a plurality of times. Thus, a signal processing device according to an exemplary embodiment may be advantageously implemented in such a measurement apparatus, particularly in the context of an ADC used for such a measurement apparatus.

[0056] The measurement apparatus may further be adapted to receive, as the repetitive signal, a response signal from a device under test in response to applying a stimulus signal to the device under test for testing the device under test. In such a scenario, the device under test may generate the repetitive signal which may then be evaluated by a signal processor of the measurement apparatus.

[0057] More particularly, the measurement apparatus may comprise at least one of the group consisting of an Analog-to-Digital Converter (ADC), a sensor device (for instance for sensing a parameter of a DUT), a test device for testing a device under test or a substance (for instance an apparatus of the Agilent 93000 series), a device for chemical, biological and/or pharmaceutical analysis, a fluid separation system adapted for separating compounds of a fluid, a capillary electrophoresis device, a liquid chromatography device, a gas chromatography device, an electronic measurement device, and a mass spectroscopy device. More generally, embodiments may be employed in many fields of electronics and measurement applications, for instance in life science regime, or in any field of analog or digital electronics in which accurate signal conversion or signal processing may be an issue, particularly when a repetitive signal is used.

BRIEF DESCRIPTION OF DRAWINGS

[0058] Other objects and many of the attendant advantages of embodiments of the present invention will be readily appreciated and become better understood by reference to the following more detailed description of embodiments in connection with the accompanied drawings. Features that are substantially or functionally equal or similar will be referred to by the same reference signs.

[0059] Fig. 1 shows a signal processing device according to an exemplary embodiment of the invention.

[0060] Fig. 2 shows diagrams in the context of coherent time stamping.

[0061] Fig. 3 illustrates a signal processing device according to an exemplary embodiment.

[0062] Fig. 4 shows diagrams illustrating the function of a signal processing device in the presence of jitter.

[0063] Fig. 5 shows diagrams illustrating an operation mode of a data processing device in the presence of jitter.

[0064] Fig. 6 shows diagrams during an operation of a signal processing device for analog waveform reconstruction according to an exemplary embodiment.

[0065] Fig. 7 illustrates a data processing device according to an exemplary embodiment of the invention.

[0066] Fig. 8 illustrates uniform interpolation in the context of a signal processing device according to an exemplary embodiment.

[0067] Fig. 9 shows a measurement apparatus according to an exemplary embodiment.

[0068] The illustration in the drawing is schematically.

[0069] In the following, referring to **Fig. 1**, a signal processing device 100 according to an exemplary embodiment of the invention will be explained.

[0070] A repetitive signal source 101 is adapted to generate a periodic repetitive signal 102. The repetitive signal 102 is a periodic signal which is repeated several times. This repetitive signal 102 is used in the context of investigating a device under test. The repetitive signal 102 is supplied to an input of a determining unit 103. The determining unit 103 is adapted for determining a number of points of times for undersampling the repetitive signal 102. These points of times at which the repetitive signal 102 is sampled may be supplied in the form of a control signal 104 to a flip flop 130 located at an output of a comparator unit 105 at which output a comparator signal 120 may be provided indicative of a result of the comparison. A first signal input of the comparator unit 105 is supplied with the repetitive signal 102. A second signal input of the comparator unit 105 is supplied with a reference signal 106 which is generated by a reference signal generator unit 107. As can be taken from Fig. 1, a clock generating unit 108 generates clock signals 109a, 109b which are supplied to the repetitive signal source 101 and the reference signal generator 107, respectively. In this context, it may be ensured that the reference signal source 101 and the reference signal generator 107 are synchronized so as to enable coherent sampling.

[0071] The comparator unit 105 is adapted for comparing the repetitive signal 102 with the reference signal 106. A result of this comparison is provided at an output of the comparator unit 105 coupled to an input of the flip flop 130. The flip flop 130 is supplied with the compare signal 120 provided at the output of the comparator unit 105 and generates, taking into account the control signal 104 indicative of a number of specific compare times, a digital result signal 110. The digital result signal 110 is supplied to a re-sorting unit 111 which is adapted for re-sorting the digital result signals 110 related to different repetitions of the repetitive signal 102 in accordance with a chronology of the corresponding points of time defined by the time control signal 104 within the periodicity of the repetitive signal 102 (see Fig. 2). After having reordered the components of the signal 110, it is supplied to an evaluation unit 112 for determining transition times of the digital result signal 110. The transition times are assumed to include the information to be derived by the signal processing of the system 100.

[0072] The evaluation unit 112 evaluates, based on the sorted signals 113, transition time signals 114 which are supplied to an output signal generation unit 115.

The output signal calculation unit 115 calculates output signals 116 which are essentially uniformly spaced in time and which are supplied at an output of the signal processing device 100.

[0073] The repetitive signal 102 is a repetitive analog signal, more particularly a repetitive modulated radio frequency signal. The signal processing device 100 is adapted for analog-to-digital-signal-conversion, so as to provide a digital signal 116 indicative of the analog waveform of the signal 102.

[0074] As will be explained below in more detail referring to Fig. 2, the determining unit 103 determines different points of time for each of the plurality of repetitions of the signal 102 at which the comparison is performed by the comparator unit 105. Therefore, the signals generated by the determining unit 103 are essentially uniformly spaced in time. The reference signal 106 is a constant signal in the embodiment of Fig. 1. The digital result signal 110 may have a logical value of "1" in case that, at a particular point of time, the repetitive signal is larger or equal than the reference signal 106. In the alternative case that the repetitive signal is smaller than the reference signal 106, the logical value of the digital result signal 110 is "0".

[0075] The output signal calculation unit 115 may perform an interpolation so as to derive the output signal 116 to be essentially uniformly spaced in time. For this purpose, a plurality of signal transformation algorithms may be applied by the output signal generation unit 115.

[0076] The clock generation unit 108 generates a first clock signal 109a for the repetitive signal source 101 and a second clock signal 109b for the reference signal generator 107. As an alternative to the provision of two separate clock signals 109a, 109b, it is also possible that the clock generation unit 108 generates a common clock signal for the repetitive signal source 101 and for the reference signal generator 107.

[0077] Therefore, the embodiment of Fig. 1 enables a measurement of transition times for analog waveform reconstruction. This will be further clarified on the basis of the diagrams 200 and diagram 250 shown in **Fig. 2**.

[0078] Along an abscissa 201 of the diagram 200, the time is plotted. Along an

ordinate 202 of the diagram 200, a signal value is plotted. A first graph shows the repetitive analog signal 102. A second graph shows the constant reference signal 106. Points of time 203 of the step function-like compare signal 120 is further shown in Fig. 2.

[0079] A modified time axis 210 (time modulo 1/M=1/3) is shown along an abscissa 210 of the diagram 250. Along an ordinate 211 of the diagram 250, a signal value is plotted. The resorted data points 203 are shown in diagram 250 as well. Furthermore, the compare signal 120 is shown. Beyond this, transition times 251 can be derived from in the diagram 250 of Fig. 2.

[0080] According to the nomenclature of Fig. 2, R=0.7 is the value of the reference signal 106, N=32 is the number of data points 203. M=3 is the number of repetitions of the repetitive signal 102. Thus, according to Fig. 2, the signal 102 to be sampled has a sine-like shape, but can have any alternative shape, particularly periodic shape. Advantageously, N and M may be coprime or relatively prime.

[0081] According to the described embodiment, the transition times 251 of the repetitive digital compare signal 120 may be evaluated or estimated accurately through coherent digital sampling using a digital ATE channel.

[0082] The time interval between two measurement moments 203 may be denoted as T_S, and the time duration of a period of the repetitive signal 102 may be denoted as T_R. Preferably, the equation $N \times T_S = M \times T_R$ holds, wherein N is coprime M, and K x N samples are taken. Samples may then be re-ordered according to the sorting scheme $i_{sort} = \text{mod}\ (i \times M, N)$. The transition time 251 is between the time of the last sample before the transition and the time of the first sample after transition.

[0083] With the coherent sampling scheme of the embodiments of Fig. 1 and Fig. 2, arbitrary fine time resolution (T_S / N) may be obtained particularly when N is sufficiently large. An essentially linear time measurement may be made possible (assuming a constant frequency sample clock for T_S).

[0084] Level accuracy of samples may only be determined by the accuracy of transition time measurements, not for instance by the number of static compare levels.

[0085] In the following, a coherency feature according to an exemplary embodiment of the invention will be explained based on the signal processing device 300 shown in Fig. 3.

[0086] Fig. 3 shows a device under test 301. The device under test 301 generates a signal under test s(t) (wherein t is the time) which is supplied to a first signal input of a comparator 302. A reference signal r(t) is supplied to a second signal input of the comparator 302 and is been generated by a reference signal generator 303. At an output of the comparator 302, a compare signal c(t) is provided which is supplied to a flip-flop 304. The output of the flip-flop 304 is coupled to an input of a memory 305. An output of the memory 305 is coupled to an input of a transition time algorithm unit 306 for determining the desired transition time(s).

[0087] Furthermore, the data processing device 300 comprises a common clock generator unit 307 which generates a common clock for different components of the system 300. The clock generator unit 307 is coupled to a divider DN unit 308 for supplying a clock signal to the flip-flop 304. Further, the clock generator unit 307 is coupled to a divider Dref 309 generating a clock signal to be supplied to the reference signal generator 303. Moreover, the clock generator 307 is coupled to a divider DM 310 which is, in turn, coupled to the device under test 301 so as to generate a clock signal for the device under test 301.

[0088] According to the embodiment of **Fig. 3**, coherency may be ensured for instance through the common clock reference. The signal under test repeats after the time T_R (controlled by the divider DM 308). The dynamic reference signal has a period T_{Ref} and is controlled by the divider Dref unit 309. A static compare level requires no clock. Furthermore, a digital sample period T_S may be implemented controlled by the divider unit DN 310.

[0089] Alternatively to the embodiment of Fig. 3, there can be three individual frequency-locked clock generators with the same output frequencies. Or, three independent clock generators may be provided with enough precision to ensure the desired output frequencies.

[0090] It should be noted that blocks 304 to 306 of the system 300 may be

substituted by any desired time to digital converter unit. The conversion from non-equidistant samples into equidistant samples may be performed with any signal processing scheme, more particularly may be applied to any digitalization of a signal with time stamps. In order words, the generation of equidistant samples from non-equidistant samples is not restricted to repetitive signals.

[0091] **Fig. 4** shows diagrams 400, 430, 450 illustrating the situation of Fig. 2 in the context of the measurement of transition times of imperfect signals, that is to say of signals which are disturbed by noise and/or jitter.

[0092] In the presence of noise or jitter, a better estimate of the time stamp can be obtained by looking at all samples in the vicinity of the transition and choosing an appropriate "average" transition point. That is to say, jitter may allow interpolation between samples. It is also possible to add jitter artificially if not noisy enough (for instance some small PRBS signal to sample clock, or connect a noisy diode to comparator input). The plot in Fig. 4 includes a level of noise of 0.02 rms.

[0093] In the following, referring to **Fig. 5**, measuring transition times of imperfect signals, that is to say signals in the presence of noise or jitter, will be explained in more detail.

[0094] Fig. 5 again shows a diagram 500 which is similar to the diagram 400 of Fig. 4 and shows a diagram 550 which is similar to the diagram 450 of Fig. 4.

[0095] One easy way of determining a transition time without averaging is to take the first "1". In the scenario of Fig. 5, the measurement point 203 #12 is then selected to be the transition time, so that t=12/256. The total number of samples is 256. Alternatively, the last "0" can be selected, which would result in the estimation of the transition time at measurement point 203 #22.

[0096] Alternatively, it is possible to implement some averaging: For example, the middle between the first "1" and the last "0" can be taken. This would result in a transition time t=(22+12)/2/256=17/256.

[0097] Alternatively, even more averaging can be involved, which results in a still quite easy calculation scheme and proper results. According to such an embodiment,

the values "0" may be counted. This may result in a transition time t=16/256.

[0098] An even better estimate of the transition time, but involving more computation, involves searching the time "T" that minimizes the sum of deviations (E_1 or E_2). S samples around the transitions, i=1,…,S, each with sample time t_i, data value d_i ("0" or "1").

[0099] The following equation describes the situation for rising transition:

[00100]
$$E_1 = \sum_{t=1, d_i=1, t_i<T}^{S} (T - t_i) + \sum_{t=1, d_i=0, T \geq t_i}^{S} (t_i - T)$$

$$E_2 = \sum_{t=1, d_i=1, t_i<T}^{S} (T - t_i)^2 + \sum_{t=1, d_i=0, T \geq t_i}^{S} (t_i - T)^2$$

[00101] In the following, referring to **Fig. 6**, analog waveform reconstruction will be explained in more detail.

[00102] A first diagram 600 shows the time dependence of the signals s(t), r(t) and c(t) in accordance with Fig. 3 for a first resolution value of 0.005. A second diagram 650 shows the time dependence of these signals s(t), r(t) and c(t) for a second resolution value of 0.0001.

[00103] Accurate transition times T_k are determined as described above. Sampled levels are given by known reference waveforms at times T_k, $V_k=r(T_k)$, or just known static levels. Samples may be (time, value) pairs (T_k, V_k).

[00104] Circles in diagram 600, 650 show the "measured" samples (T_k, V_k) for a resolution of 0.005 (diagram 600) and 0.0001 (diagram 650).

[00105] In the following, referring to **Fig. 7**, a signal processing device 700 according to an exemplary embodiment of the invention will be explained.

[00106] The left hand side of Fig. 7 essentially equals to Fig. 3, so that only the additional components will be explained in the following.

[00107] The signal processing device 700 comprises a uniform interpolation unit 701, a Fast Fourier Transformation unit 702, a Non-Uniform Fast Fourier Transformation

unit 703, an Inverse Fast Fourier Transformation unit 704, a Non-Uniform Discrete Fourier Transformation unit 705, a down conversion unit (frequency shift) 706 and an Inverse Fast Fourier Transformation unit 707.

[00108] An output of the transition time algorithm unit 306 is supplied to a first output 708 as a non-uniform time sample signal. Furthermore, the output of the transition time algorithm unit 306 is supplied to an input of the uniform interpolation unit 701. An output of the uniform interpolation unit 701 supplies a uniform time sample signal 709. Furthermore, the output of the uniform interpolation unit 701 is coupled to an input of the FFT unit 702, wherein an output of the FFT unit 702 provides a uniform spectrum signal 710.

[00109] Beyond this, the output of the transition time algorithm unit 306 is supplied to an input of the NUFFT unit 703. At an output of the NUFFT unit 703, a uniform spectrum signal 711 is provided. Furthermore, the output of the NUFFT unit 703 is coupled to an input of the Inverse FFT unit 704. At an output of the Inverse FFT unit 704, uniform time samples 712 are provided. Moreover, the output signals of the transition time algorithm unit 306 are supplied to the Non-Uniform DFT unit 705. At an output of the Non-Uniform DFT unit 705, a signal 713 is provided which is indicative of a spectrum at selected user-defined frequencies. Furthermore, the output of the Non-Uniform DFT unit 705 is coupled to an input of the down conversion unit 706. At an output of the down conversion unit 706, a baseband spectrum signal 714 is provided. Furthermore, the output of the down conversion unit 706 is coupled to an input of the Inverse FFT unit 707. At an output of the Inverse FFT unit 707, a uniform baseband sample time signal 715 is provided. In a practical application, usually only a few of the outputs are foreseen, for instance one or two.

[00110] The processing according to the embodiment of Fig. 7 allows a transformation of the transition times into usual ADC sample format.

[00111] For some applications, non-uniform samples (T_i, V_i) are fine, for instance for eye diagram. However, many applications require data representation with uniformly spaced time samples or spectrum at uniformly spaced frequencies.

[00112] In order to achieve this solution, it is possible to use uniform interpolation to

transform non-uniformly spaced time samples into samples with uniform time spacing (as common in the art of conventional ADCs). For this purpose, standard FFT can be applied.

[00113] It is also possible to use NUFFT (Non-Uniform Fast Fourier Transformation) to calculate a spectrum at uniformly spaced frequencies from non-uniformly spaced time samples. Preferably, NUFFT may be used in combination with FMM (Fast Multipole Method) for fast computation time. Time samples can be calculated using standard inverse FFT.

[00114] It is also possible to use Non-Uniform DFT (Non-Uniform Discrete Fourier Transformation, not so "fast") to transform to non-uniformly spaced time samples into a spectrum at selected user-defined frequencies. This may be useful for narrowband (for instance RF) signals.

[00115] **Fig. 8** shows a first diagram 800 and a second diagram 850 which are similar to the diagrams of Fig. 6.

[00116] Fig. 8 illustrates uniform interpolation. It is possible to use reconstruction algorithms to obtain uniformly spaced time data. For this purpose, a Sinc(t) interpolation is possible, a polynomial interpolation (Lagrange interpolation, spline interpolation, linear interpolation) is possible, and/or fractional delay filters may be implemented. The diagram 850 illustrates by the circles non-uniform samples from transition times of a compare signal. The dotted line shows the true DUT waveform. The stars in diagram 850 show the result of a uniform interpolation using spline interpolation, for instance MATLAB interp1(..., 'spline').

[00117] In the following, the NUFFT feature will be explained in more detail.

[00118] For this purpose, the nomenclature will be defined in the following:

[00119]

$$x_i \in R, i = 1 \ldots N, \text{ time samples}$$
$$f_k = (k-1) \cdot f_0 \in R, k = 1 \ldots N, \text{ frequency points}$$
$$X_k = X(f_k) \in C, \text{ spectrum}$$
$$x_i = x(t_i) = \sum_{k=1}^{N} X_k e^{j2\pi(k-1)f_0 t_i}$$
$$\mathbf{W} = (w_{ik}) = (e^{j2\pi(k-1)f_0 t_i}), \text{ Non-uniform Fourier matrix}$$
$$w_{ik} = (w_i)^{k-1}, w_i = e^{j2\pi f_0 t_i}$$
$$W = \begin{pmatrix} 1 & w_1 & w_1^2 & \cdots & w_1^{N-1} \\ 1 & w_2 & w_2^2 & \cdots & w_2^{N-1} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & w_N & w_N^2 & \cdots & w_N^{N-1} \end{pmatrix}, \text{ Vandermonde Matrix}$$
$$\begin{pmatrix} x_1 \\ \vdots \\ x_N \end{pmatrix} = \begin{pmatrix} w_{11} & \cdots & w_{1N} \\ \vdots & \ddots & \vdots \\ w_{N1} & \cdots & w_{NN} \end{pmatrix} \begin{pmatrix} X_1 \\ \vdots \\ X_N \end{pmatrix}$$
$$\mathbf{x} = \mathbf{W} \cdot \mathbf{X}$$
$$\mathbf{X} = \mathbf{W}^{-1} \cdot \mathbf{x}, \text{ Non-uniform FFT}$$

[00120] It is possible to use NUFFT to calculate spectrum at uniformly spaced frequencies from non-uniformly spaced time samples. Uniform frequency spacing may make the Fourier matrix a Vandermonde Matrix (which is always invertible for different x_i, wherein columns are powers of a column vector) which allows to speed up the transform compared to arbitrary frequencies.

[00121] In the following, NUDFT for narrowband signals (RF) will be explained in more detail.

[00122] For this purpose, the nomenclature will be defined in the following:

$x_i \in R, i = 1..N$, time samples

$f_k \in R, k = 1..P$, frequencies of interest

$X_k = X(f_k) \in C$, spectrum at frequencies of interest

$$x_i = x(t_i) = \sum_{k=1}^{P} X_k e^{j2\pi f_k t_i}$$

$\mathbf{W} = (w_{ik}) = (e^{j2\pi f_k t_i})$, Non - uniform Fourier matrix

$$\begin{pmatrix} x_1 \\ \vdots \\ x_N \end{pmatrix} = \begin{pmatrix} w_{11} & \cdots & w_{1P} \\ \vdots & \ddots & \vdots \\ w_{N1} & \cdots & w_{NP} \end{pmatrix} \begin{pmatrix} X_1 \\ \vdots \\ X_p \end{pmatrix}$$

$\mathbf{x} = \mathbf{W} \cdot \mathbf{X}$

$\mathbf{X} = \mathbf{W}^+ \cdot \mathbf{x}$, Non - uniform DFT

$\mathbf{W}^+ = (\mathbf{W}'\mathbf{W})^{-1}\mathbf{W}'$, Definition of pseudo inverse

$\mathbf{W}' = (w_{ki})$, Definition of transpose

[00123]

[00124] It is possible to calculate the spectrum only for P frequencies f_k in a (narrow) frequency range of interest $[f_L,f_H]$ to avoid calculation for millions of frequencies from DC to RF.

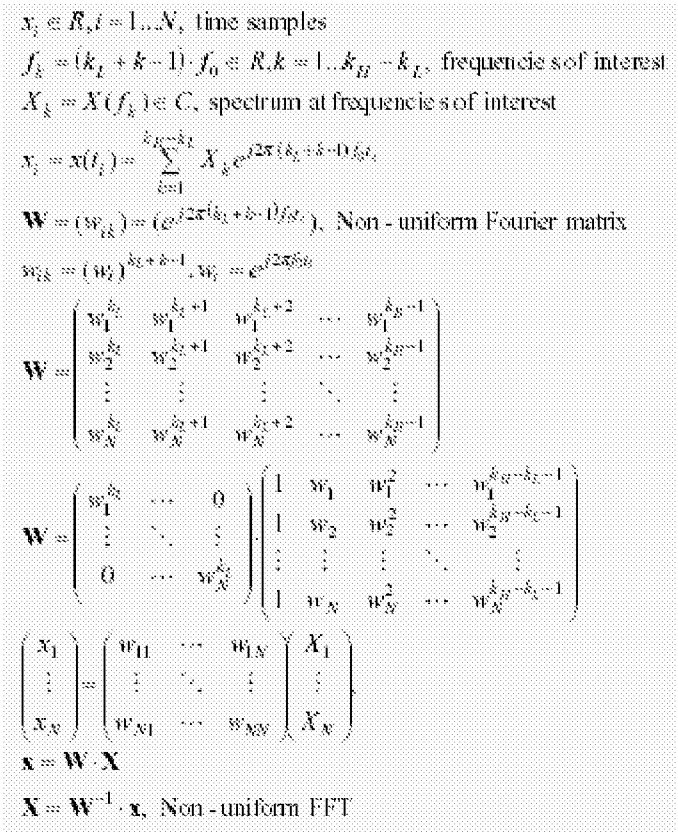
[00125] Optionally, it is possible to include DC (f=0) in NUDFT to tolerate offset errors.

[00126] Optionally, it is possible to include known spur frequencies to avoid noise aliasing into the frequencies of interest.

[00127] It is also possible to perform down conversion into a base band directly in the frequency domain by a simple frequency shift. No hardware down conversion is needed in this scenario.

[00128] When N > B, often N >> P, averaging may improve the estimate of X. W may become rectangular. Spectrum X may be calculated using Moore-Penrose Pseudo-Inverse W^+.

[00129] Next, another scenario will be described:

[00130] 

$x_i \in R, i = 1..N$, time samples

$f_k = (k_L + k - 1) \cdot f_0 \in R, k = 1..k_H - k_L$, frequencies of interest

$X_k = X(f_k) \in C$, spectrum at frequencies of interest

$$x_i = x(t_i) = \sum_{k=1}^{k_H - k_L} X_k e^{j2\pi(k_L + k - 1)f_0 t_i}$$

$\mathbf{W} = (w_{ik}) = (e^{j2\pi(k_L + k - 1)t_i})$, Non-uniform Fourier matrix

$w_{ik} = (w_i)^{k_L + k - 1}, w_i = e^{j2\pi f_0 t_i}$

$$\mathbf{W} = \begin{pmatrix} w_1^{k_L} & w_1^{k_L+1} & w_1^{k_L+2} & \cdots & w_1^{k_H-1} \\ w_2^{k_L} & w_2^{k_L+1} & w_2^{k_L+2} & \cdots & w_2^{k_H-1} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ w_N^{k_L} & w_N^{k_L+1} & w_N^{k_L+2} & \cdots & w_N^{k_H-1} \end{pmatrix}$$

$$\mathbf{W} = \begin{pmatrix} w_1^{k_L} & \cdots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \cdots & w_N^{k_L} \end{pmatrix} \cdot \begin{pmatrix} 1 & w_1 & w_1^2 & \cdots & w_1^{k_H-k_L-1} \\ 1 & w_2 & w_2^2 & \cdots & w_2^{k_H-k_L-1} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & w_N & w_N^2 & \cdots & w_N^{k_H-k_L-1} \end{pmatrix}$$

$$\begin{pmatrix} x_1 \\ \vdots \\ x_N \end{pmatrix} = \begin{pmatrix} w_{11} & \cdots & w_{1N} \\ \vdots & \ddots & \vdots \\ w_{N1} & \cdots & w_{NN} \end{pmatrix} \begin{pmatrix} X_1 \\ \vdots \\ X_N \end{pmatrix}$$

$\mathbf{x} = \mathbf{W} \cdot \mathbf{X}$

$\mathbf{X} = \mathbf{W}^{-1} \cdot \mathbf{x}$, Non-uniform FFT

[00131] When frequencies are chosen to be equally spaced within a single contiguous frequency range of interest (typical for RF signals), the Fourier matrix is a product of a Vandermonde Matrix and a diagonal matrix which may simplify inversion.

[00132] **Fig. 9** shows a measurement apparatus 900 according to an exemplary embodiment of the invention.

[00133] The measurement apparatus 900 comprises a control computer (like a workstation, a PC or a laptop) 901 which controls the entire test of the measurement apparatus. A test control unit 902 generates and/or receives from DUTs 903, 904 signals, including a repetitive signal 102 related to the measurement carried out by the measurement apparatus 900. Within the test control unit 902 or apart therefrom, a signal processing device 100 having the features as described in Fig. 1 is implemented. The test control unit 902 comprises a plurality of pins 905 which are connected to the devices under test 903, 904 (for instance memories, chips for mobile phones, etc.).

[00134] During the test, stimulus signals are supplied to the DUTs 903, 904 so as to perform a specific test pattern, and response signals are evaluated by the test control

unit 902 and by the control computer 901.

[00135] It should be noted that the term "comprising" does not exclude other elements or features and the "a" or "an" does not exclude a plurality. Also elements described in association with different embodiments may be combined. It should also be noted that reference signs in the claims shall not be construed as limiting the scope of the claims.

CLAIMS

1. A signal processing device (100) for processing a signal (102), the signal processing device (100) comprising

a comparator unit (105) for comparing the signal (102) with a reference signal (106),

a generation unit (105, 130) for generating digital result signals (110) indicative of the result of the comparing,

an evaluation unit (112) for determining transition times of the digital result signals (110),

an output signal calculation unit (115) adapted for calculating essentially uniformly spaced output signals (116).

2. The signal processing device (100) of claim 1,

adapted for processing a repetitive signal (102).

3. The signal processing device (100) of claim 1 or any one of the above claims,

comprising a determining unit (103) for determining a number of points of time for undersampling the signal (102).

4. The signal processing device (100) of claim 3,

wherein the comparator unit (105) is adapted for comparing, at the number of points of time, the signal (102) with the reference signal (106),

5. The signal processing device (100) of claim 1 or any one of the above claims,

wherein the output signal calculation unit (115) is adapted for calculating essentially uniformly spaced output signals (116) based on non-uniformly spaced digital result signals (110).

6. The signal processing device (100) of claim 1 or any one of the above claims,

adapted for processing an analog signal (102).

7. The signal processing device (100) of claim 1 or any one of the above claims,

adapted for processing a modulated radio frequency signal (102).

8. The signal processing device (100) of claim 1 or any one of the above claims,

adapted as an analog-to-digital converter for converting an analog signal (102) into a digital signal (116).

9. The signal processing device (100) of claim 3 or any one of the above claims,

wherein the determining unit (103) is adapted for determining points of time differing for at least a part of a plurality of repetitions.

10. The signal processing device (100) of claim 3 or any one of the above claims,

wherein the determining unit (103) is adapted for determining points of time differing for at least a part of a plurality of repetitions so as to refine accuracy of signal processing with each additional repetition.

11. The signal processing device (100) of claim 1 or any one of the above claims,

wherein the reference signal (106) is one of the group consisting of a single signal being constant in time, a plurality of signals each being constant in time, a signal varying in time in accordance with a predefined waveform, and a sine signal.

12. The signal processing device (100) of claim 1 or any one of the above claims,

wherein the evaluation unit (112) is adapted for determining the transition times (114) taking into account the signal at points of time related to different ones of a plurality of repetitions.

13. The signal processing device (100) of claim 3 or any one of the above claims,

wherein the number of points of time is larger than a number of repetitions.

14. The signal processing device (100) of claim 3 or any one of the above claims,

comprising a re-sorting unit (111) adapted for re-sorting the digital result signals (110) related to different repetitions in accordance with a chronology of the corresponding points of time within a periodicity of the repetitive signal (102).

15. The signal processing device (100) of claim 1 or any one of the above claims,

wherein the generation unit (105, 130) is adapted for generating a digital result signal (110) having a first logical value in case that the respective signal (102) is larger than the reference signal (106), and is adapted for generating a digital result signal (110) having a second logical value in case that the respective signal (102) is smaller than the reference signal (106).

16. The signal processing device (100) of claim 15,

wherein the evaluation unit (112) is adapted for determining the transition times (114) based on an analysis of at least one of the group consisting of a last point of time in a sequence in which the digital result signal (110) has the first logical value, and a first point of time in a sequence in which the digital result signal (110) has the second logical value.

17. The signal processing device (100) of claim 15,

wherein the evaluation unit (112) is adapted for determining the transition times (114) based on a statistical analysis of a plurality of points of time forming an interval comprising digital result signals (110) having the first logical value and comprising digital result signals (110) having the second logical value.

18. The signal processing device (100) of claim 15,

wherein the evaluation unit (112) is adapted for determining the transition times (114) based on fitting a mathematical probability function, particularly a cumulative probability density function, to a plurality of points of time forming an interval comprising digital result signals (110) having the first logical value and comprising digital result signals (110) having the second logical value and determining the transition times (114) from a result of the fit.

19. The signal processing device (100) of claim 1 or any one of the above claims,

wherein the evaluation unit (112) is adapted to determine the transition times (114) in accordance with a degree of presence of at least one of the group consisting of signal jitter and signal noise.

20. The signal processing device (100) of claim 1 or any one of the above claims,

wherein the output signal calculation unit (115) is adapted for determining the essentially uniformly spaced output signals (116) by using at least one of the group consisting of a Sinc interpolation, a polynomial interpolation, a Lagrange interpolation, a spline interpolation, a linear interpolation, and a fractional delay filter.

21. The signal processing device (100) of claim 1 or any one of the above claims,

wherein the output signal calculation unit (115) is adapted for calculating the output signals (116) essentially uniformly spaced in time or essentially uniformly spaced in frequency.

22. The signal processing device (100) of claim 1 or any one of the above claims,

wherein the output signal calculation unit (115) is adapted for calculating the output signal (116) by performing at least one of the group consisting of a Fast Fourier Transformation, a Non-Uniform Fast Fourier Transformation, a Non-Uniform Fast Fourier Transformation with Fast Multipole Method, and a Non-Uniform Discrete Fourier Transformation.

23. The signal processing device (100) of claim 2 or any one of the above claims,

adapted for processing the repetitive signal (102) using coherent sampling.

24. The signal processing device (100) of claim 1 or any one of the above claims,

comprising a clock generating unit (108) adapted for generating a common clock signal for a plurality of components (101, 107) of the signal processing device (100).

25. The signal processing device (100) of claim 1 or any one of the above claims,

comprising a plurality of clock generating units (108), each adapted for generating an individual clock signal (109a, 109b) for an assigned component (101, 107) of the signal processing device (100), wherein the plurality of clock generating units (108) are frequency-locked to one another.

26. The signal processing device (100) of claim 1 or any one of the above claims,

comprising a jitter adding unit adapted to selectively add jitter to the signal (102).

27. The signal processing device (100) of claim 1 or any one of the above claims,

comprising an automatic test equipment unit as a source for providing the signal (102).

28. The signal processing device (100) of claim 1 or any one of the above claims,

adapted as an automatic test equipment for testing a device under test.

29. A measurement apparatus (900), comprising

a signal processing device (100) of claim 1 or any one of the above claims for processing a signal (102) related to a measurement carried out by the measurement apparatus (900).

30. The measurement apparatus (900) of claim 29,

adapted to generate, as the signal (102), a stimulus signal to be applied to a device under test (903, 904) for testing the device under test (903, 904).

31. The measurement apparatus (900) of claim 29 or any one of the above claims,

adapted to receive, as the signal (102), a response signal from a device under test (903, 904) in response to applying a stimulus signal to the device under test (903, 904) for testing the device under test (903, 904).

32. The measurement apparatus (900) of claim 29 or any one of the above claims,

comprising at least one of an analog-to-digital converter, a sensor device, a test device for testing a device under test or a substance, a device for chemical, biological and/or pharmaceutical analysis, a fluid separation system adapted for separating compounds of a fluid, a capillary electrophoresis device, a liquid chromatography device, a gas chromatography device, an electronic measurement device, and a mass spectroscopy device.

33. A signal processing method of processing a signal (102), the method comprising

comparing the signal (102) with a reference signal (106),

generating digital result signals (110) indicative of the result of the comparing,

determining transition times of the digital result signals (110),

calculating essentially uniformly spaced output signals (116).

34. A computer-readable medium, in which a computer program of signal processing is stored, which computer program, when being executed by a processor (100), is adapted to control or carry out a method of processing a signal (102), the method comprising

comparing the signal (102) with a reference signal (106),

generating digital result signals (110) indicative of the result of the comparing,

determining transition times of the digital result signals (110),

calculating essentially uniformly spaced output signals (116).

35. A program element of signal processing, which program element, when being executed by a processor (100), is adapted to control or carry out a method of processing a signal (102), the method comprising

comparing the signal (102) with a reference signal (106),

generating digital result signals (110) indicative of the result of the comparing,

determining transition times of the digital result signals (110),

calculating essentially uniformly spaced output signals (116).

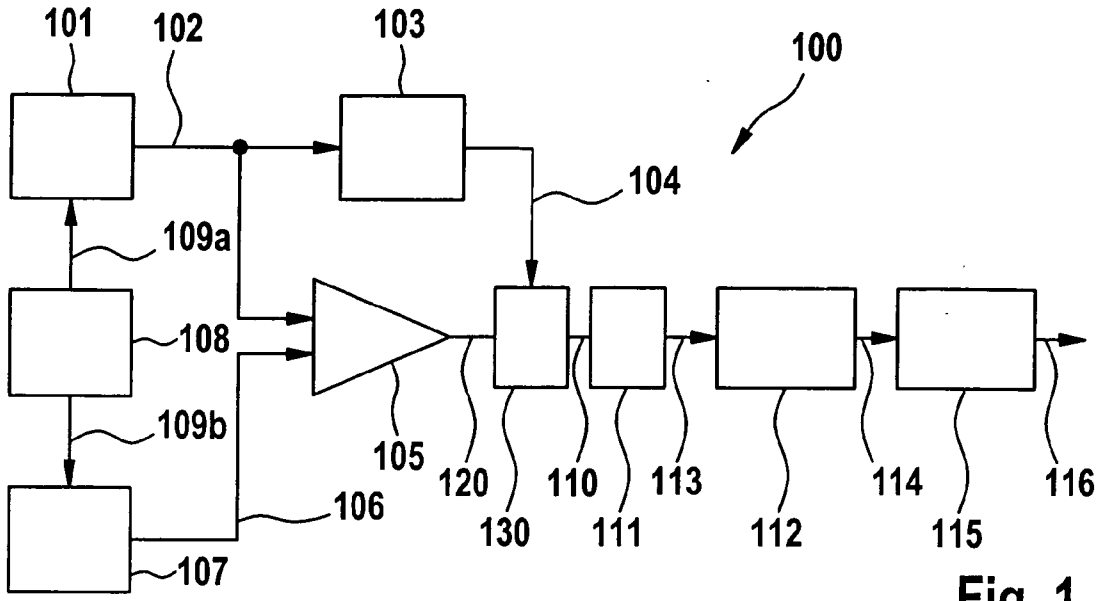
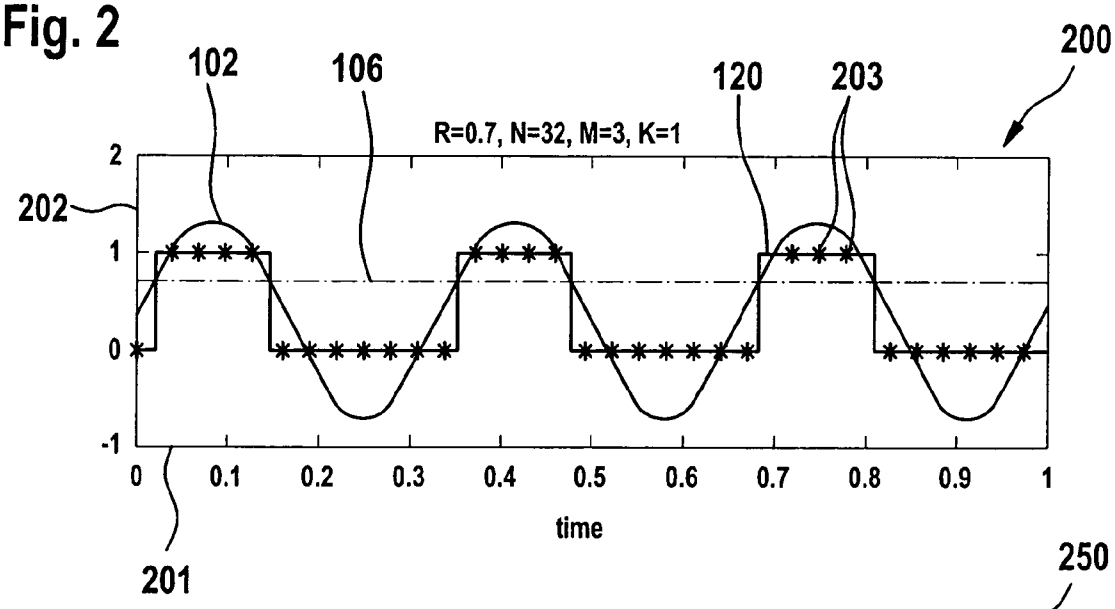
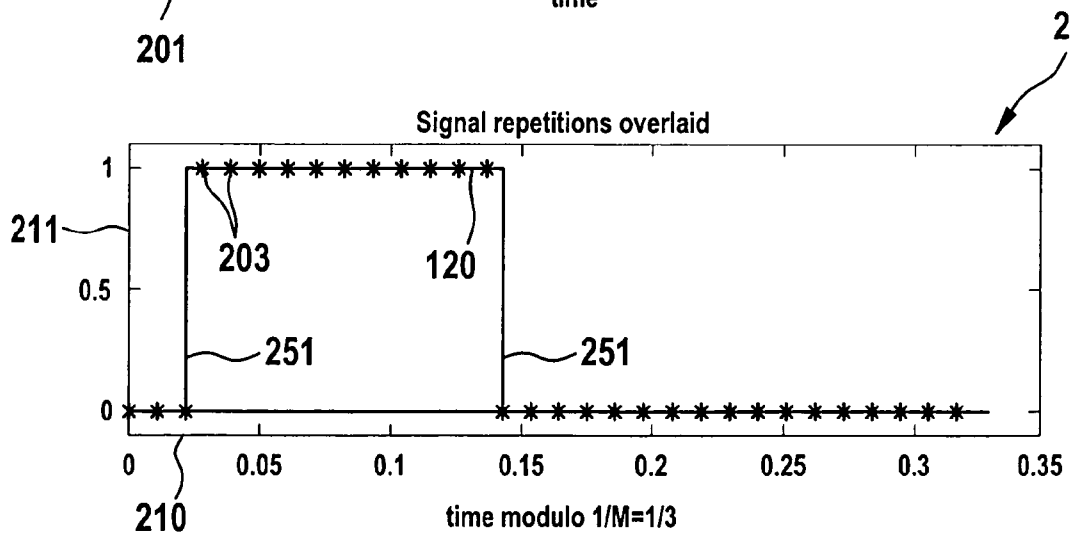

101
102
103
100
104
109a
108
109b
105
120
130
110
111
113
112
114
115
116
106
107

Fig. 1

Fig. 2


200
102
106
120
203
R=0.7, N=32, M=3, K=1
202
2
1
0
-1
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
time
201


250
Signal repetitions overlaid
211
1
0.5
0
203
120
251
251
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
time modulo 1/M=1/3
210

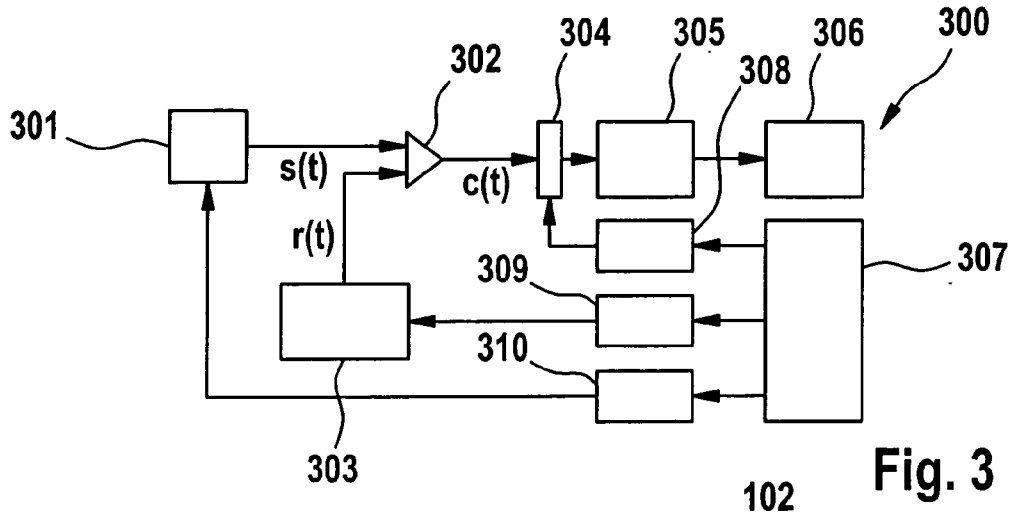

301
302
304
305
306
300
308
s(t)
c(t)
r(t)
309
307
310
303

Fig. 3

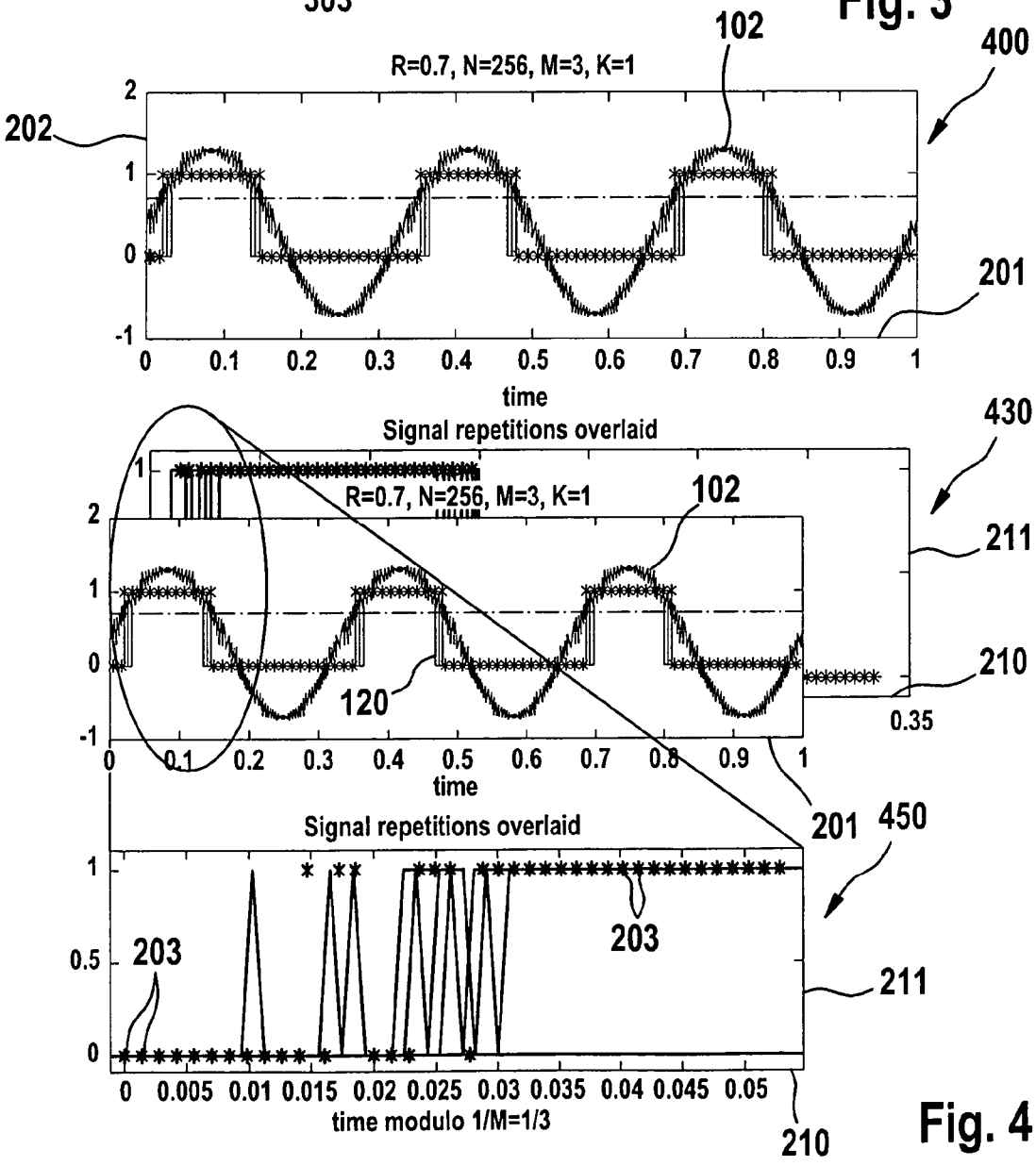

102
400
R=0.7, N=256, M=3, K=1
202
201
time
Signal repetitions overlaid
430
R=0.7, N=256, M=3, K=1
102
211
210
120
0.35
time
201
450
Signal repetitions overlaid
203
203
211
time modulo 1/M=1/3
210

Fig. 4

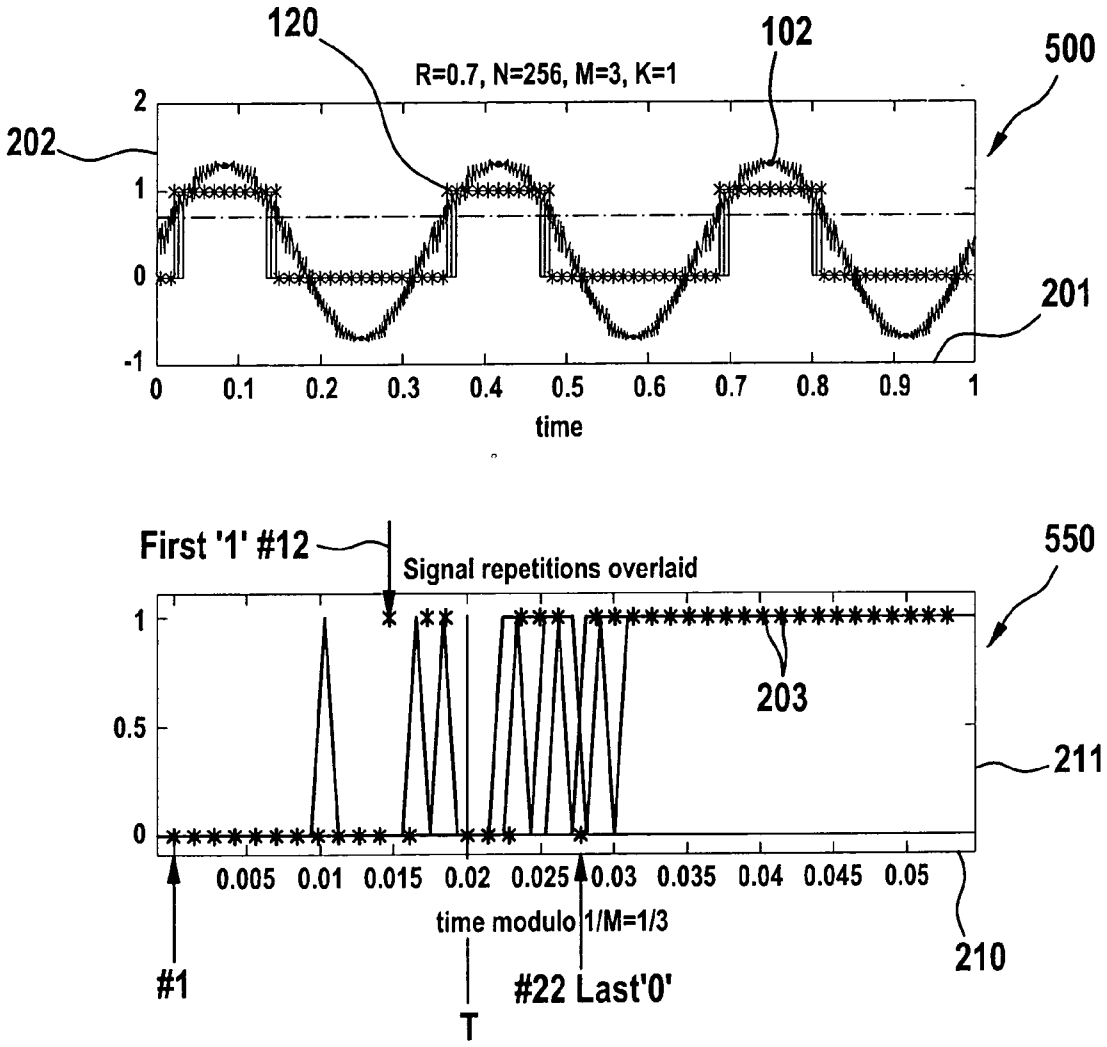

120
102
500
R=0.7, N=256, M=3, K=1
202
201
2
1
0
-1
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1
time
First '1' #12
Signal repetitions overlaid
550
203
211
1
0.5
0
0.005 0.01 0.015 0.02 0.025 0.03 0.035 0.04 0.045 0.05
time modulo 1/M=1/3
210
#1
#22 Last'0'
T

Fig. 5

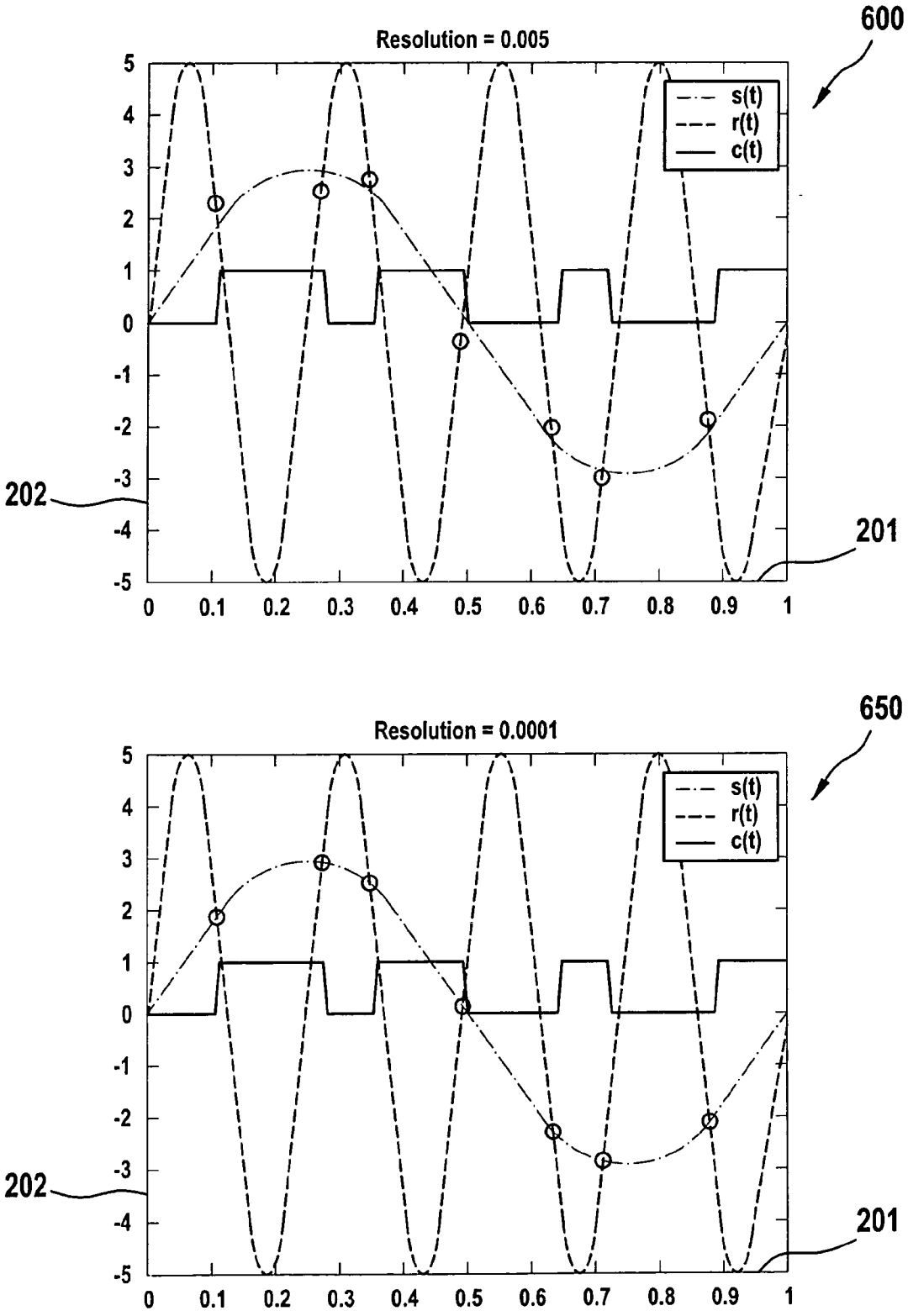

600
Resolution = 0.005
s(t)
r(t)
c(t)
202
201
650
Resolution = 0.0001
s(t)
r(t)
c(t)
202
201

Fig. 6

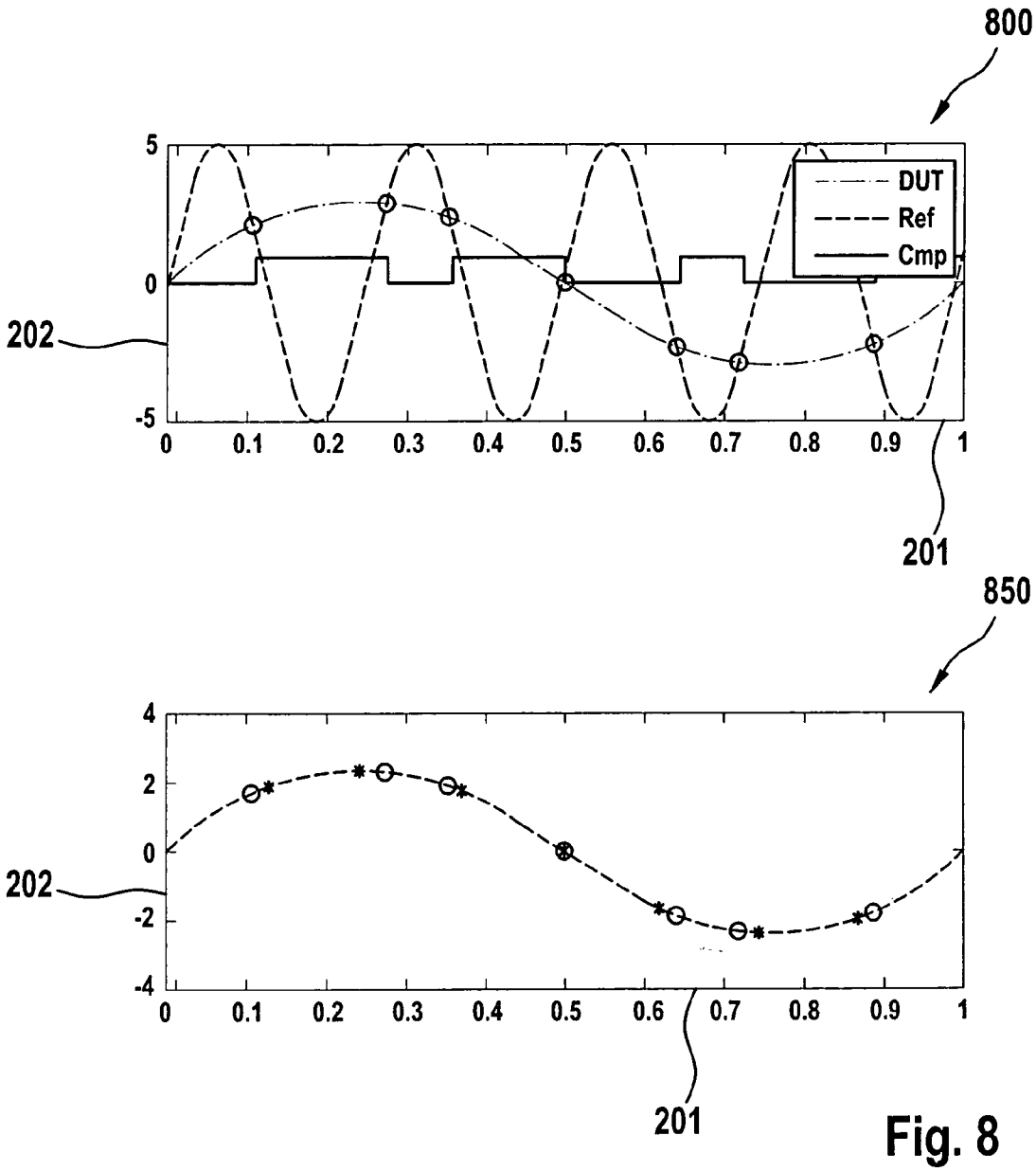

800
5
0
-5
202
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
DUT
Ref
Cmp
201
850
4
2
0
-2
-4
202
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
201

Fig. 8

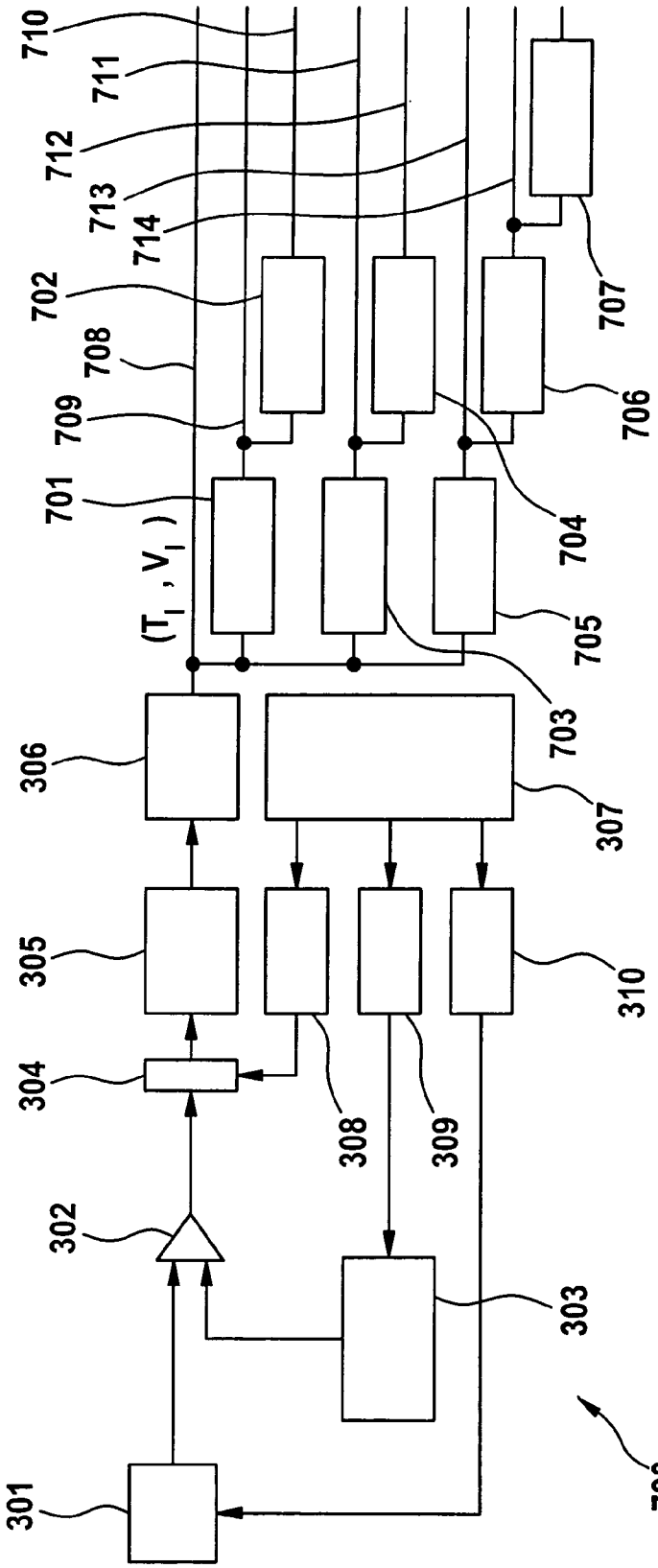

710
711
712
713
714
702
708
709
701
(T_I, V_I)
306
305
304
302
301
303
307
308
309
310
703
704
705
706
707
700

Fig. 7

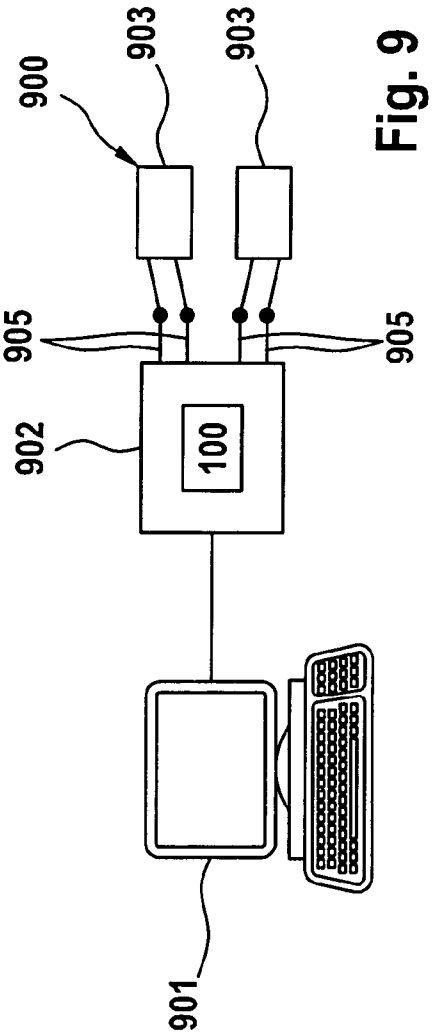

900
903
903
905
905
902
100
901

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/065616

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/12 G01R13/02 G01R31/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 661 836 B1 (DALAL WAJIH [US] ET AL) 9 December 2003 (2003-12-09) column 5, line 5 - column 8, line 6; figure 3	1-35
X	US 6 346 907 B1 (DACY SUSAN M [US] ET AL) 12 February 2002 (2002-02-12) abstract; figure 1	1,29, 33-35
A	US 2005/219107 A1 (GUIDRY DAVID W [US]) 6 October 2005 (2005-10-06) abstract; figure 3	1-35

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 April 2007	27/04/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gerdes, Rolf

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/065616

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	BURNS M ET AL: "A DSP-based technique for high-speed A/D conversion to generate coherently sampled sequences" IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 52, no. 3, June 2003 (2003-06), pages 950-958, XP011098650 ISSN: 0018-9456 abstract; figure 2	1-35
A	MAXIM /DALLAS: "Coherent sampling vs. window sampling" MAXIM APPLICATION NOTE 1040, 29 March 2002 (2002-03-29), pages 1-6, XP002429380 Retrieved from the Internet: URL:http://www.maxim-ic.com/appnotes.cfm/appnote_number/1040/> [retrieved on 2007-04-16] abstract; figure 1	1-35
A	US 2005/206545 A1 (KOBAYASHI HARUO [JP] ET AL) 22 September 2005 (2005-09-22) abstract; figure 2	1-35

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2006/065616

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 6346907 B1	12-02-2002	JP 3522598 B2	26-04-2004
		JP 2000078012 A	14-03-2000
US 2005219107 A1	06-10-2005	NONE	
US 2005206545 A1	22-09-2005	JP 2005249690 A	15-09-2005