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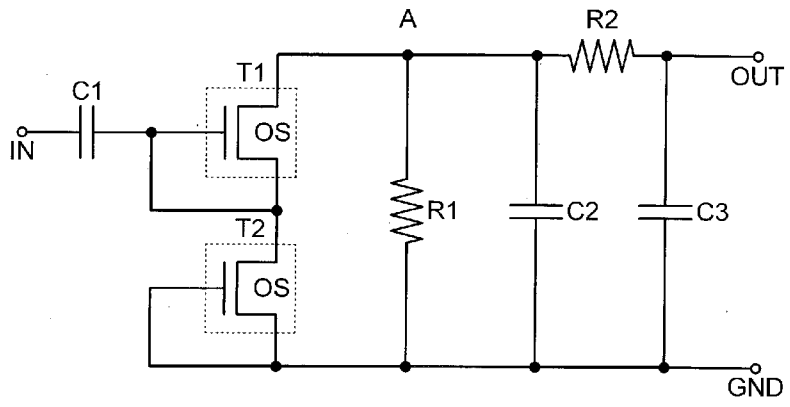
(54) **Title**: DEMODULATION CIRCUIT AND RFID TAG INCLUDING THE DEMODULATION CIRCUIT

FIG. 1A



(57) **Abstract**: An object is to provide a demodulation circuit having a sufficient demodulation ability. Another object is to provide an RFID tag which uses a demodulation circuit having a sufficient demodulation ability. A material which enables a reverse current to be small enough, for example, an oxide semiconductor material, which is a wide bandgap semiconductor, is used in part of a transistor included in a demodulation circuit. By using the semiconductor material which enables a reverse current of a transistor to be small enough, a sufficient demodulation ability can be secured even when an electromagnetic wave having a high amplitude is received.

WO 2011/102190 A1

DESCRIPTION

DEMODULATION CIRCUIT AND RFID TAG INCLUDING THE DEMODULATION CIRCUIT

TECHNICAL FIELD

[0001]

The invention disclosed herein relates to a demodulation circuit and an RFID tag that utilizes the demodulation circuit.

BACKGROUND ART

[0002]

Recently, semiconductor devices that are capable of transmitting and receiving data without contact have been actively developed. Such semiconductor devices are particularly called RFID (radio frequency identification) tags, ID tags, IC tags, IC chips, RF tags, wireless tags, electronic tags, wireless chips, transponders, and the like.

[0003]

The data transfer between the RFID tag and a communication device is generally carried out in such a manner that a device on the transmission side (e.g., the communication device) transmits a modulated carrier wave, and the device on the reception side (e.g., the RFID tag) demodulates the modulated carrier wave.

[0004]

As one of the methods for modulating a carrier wave, there is an amplitude modulation method (an amplitude shift keying (ASK) modulation method). An ASK modulation method is a method in which a difference in amplitude of a carrier wave is generated and this amplitude difference is used as a modulation signal in transmitting data.

[0005]

In order to extract data from the modulated carrier wave, the RFID tag is provided with a demodulation circuit. As an example of the demodulation circuit, there is a device that uses a rectifying function of a transistor whose gate terminal and drain terminal (or source terminal) are connected to each other (e.g., see Patent

Document 1).

[Reference]

[Patent Document]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2008-182687

DISCLOSURE OF INVENTION

[0007]

By the way, energy of electromagnetic waves is inversely proportional to the square of the distance between a point on which the electromagnetic waves are radiated and an observation point. That is, as the distance between a communication device and an RFID tag becomes longer, the energy of electromagnetic waves that the RFID tag receives becomes lower; on the contrary, as the distance between the communication device and the RFID tag becomes shorter, the energy of electromagnetic waves that the RFID tag receives becomes higher.

[0008]

As described above, the energy of electromagnetic waves that the RFID tag receives becomes higher when the distance between the communication device and the RFID tag is shorter. Therefore, in the case where the distance between the communication device and the RFID tag is short, an advantage in terms of supplied electric power can be gained generally. However, for example in an RFID tag provided with the demodulation circuit disclosed in Patent Document 1 which utilizes a rectifying function of a transistor whose gate terminal and drain terminal (or source terminal) are connected to each other, a reverse current is generated in the transistor when electromagnetic waves with large amplitude are received, so that a sufficient rectifying function cannot be obtained. In other words, it is difficult to perform sufficient demodulation.

[0009]

In consideration of the above-described problem, an object of an embodiment of the invention disclosed herein is to provide a demodulation circuit having a sufficient demodulation ability. Further, another object is to provide an RFID tag provided with a demodulation circuit having a sufficient demodulation ability.

[0010]

In the invention disclosed herein, a material which enables a reverse current to be small enough, for example an oxide semiconductor material, which is a wide bandgap semiconductor, is used in a transistor in a demodulation circuit, whose gate terminal and drain terminal (or source terminal) are connected to each other. By using a semiconductor material which enables a reverse current of a transistor whose gate terminal and drain terminal (or source terminal) are connected to each other to be small enough, even in the case where electromagnetic waves with large amplitude are received, a sufficient demodulation ability can be secured.

[0011]

Specifically, the following structures can be employed, for example.

[0012]

An embodiment of the present invention is a demodulation circuit which includes a first transistor, a second transistor, a first capacitor, a second capacitor, a third capacitor, a first resistor, and a second resistor. In addition, a gate terminal of the first transistor, a drain terminal (or a source terminal) of the first transistor, a source terminal (or a drain terminal) of the second transistor, and one terminal of the first capacitor are electrically connected to each other; a gate terminal of the second transistor, a drain terminal (or a source terminal) of the second transistor, one terminal of the second capacitor, one terminal of the third capacitor, and one terminal of the first resistor are electrically connected to each other; a source terminal (or a drain terminal) of the first transistor, the other terminal of the second capacitor, the other terminal of the first resistor, and one terminal of the second resistor are electrically connected to each other; the other terminal of the third capacitor and the other terminal of the second resistor are electrically connected to each other; and a channel formation region of the first transistor and a channel formation region of the second transistor include an oxide semiconductor.

[0013]

In the above-described demodulation circuit, a reference potential may be supplied to a node which is electrically connected to the gate terminal of the second transistor, the drain terminal (or the source terminal) of the second transistor, the one terminal of the second capacitor, the one terminal of the third capacitor, and the one

terminal of the first resistor.

[0014]

Another embodiment of the present invention is a demodulation circuit which includes a first transistor, a second transistor, a first capacitor, a second capacitor, a third capacitor, a first resistor, and a second resistor. In addition, a gate terminal of the second transistor, a drain terminal (or a source terminal) of the second transistor, a source terminal (or a drain terminal) of the first transistor, and one terminal of the first capacitor are electrically connected to each other; a source terminal (or a drain terminal) of the second transistor, one terminal of the second capacitor, one terminal of the third capacitor, and one terminal of the first resistor are electrically connected to each other; a gate terminal of the first transistor, a drain terminal (or a source terminal) of the first transistor, the other terminal of the second capacitor, the other terminal of the first resistor, and one terminal of the second resistor are electrically connected to each other; the other terminal of the third capacitor and the other terminal of the second resistor are electrically connected to each other; and a channel formation region of the first transistor and a channel formation region of the second transistor include an oxide semiconductor.

[0015]

In the above-described demodulation circuit, a reference potential may be supplied to a node which is electrically connected to the source terminal (or the drain terminal) of the second transistor, the one terminal of the second capacitor, the one terminal of the third capacitor, and the one terminal of the first resistor.

[0016]

By using any of the embodiments of the demodulation circuit, an RFID tag having excellent characteristics can be obtained.

[0017]

Note that although the transistor may be formed using an oxide semiconductor in the above embodiments, the invention disclosed herein is not limited thereto. A material which can realize reverse current characteristics equivalent to those of the oxide semiconductor, such as a wide bandgap material (more specifically, a semiconductor material with an energy gap Eg of larger than 3 eV) like silicon carbide, may be used.

[0018]

Note that in this specification and the like, the term such as "over" or "below" does not necessarily mean that a component is placed "directly on" or "directly under" another component. For example, the expression "a gate electrode over a gate insulating layer" can mean the case where there is an additional component between the gate insulating layer and the gate electrode. Moreover, the terms such as "over" and "below" are only used for convenience of description, and the positions of components may be reversed upside down, unless otherwise specified.

[0019]

In addition, in this specification and the like, the term such as "electrode" or "wiring" does not limit the function of the component. For example, an "electrode" can be used as part of "wiring", and vice versa. Further, the term "electrode" or "wiring" can also mean a combination of a plurality of "electrodes" and "wirings" formed in an integrated manner.

[0020]

Functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flow is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be used to denote the drain and the source, respectively, in this specification.

[0021]

Note that in this specification and the like, the term "electrically connected" includes the case where components are connected through an "object having any electric function." There is no particular limitation on the "object having any electric function" as long as electric signals can be transmitted and received between components that are connected through the object.

[0022]

Examples of the "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions as well as an electrode and a wiring.

[0023]

By using an oxide semiconductor in a transistor whose gate terminal and drain

terminal (or source terminal) are connected to each other, a reverse current can be made small enough. Therefore, using this transistor, an ability of a demodulation circuit can be improved sufficiently. Accordingly, even when the distance between a communication device and an RFID tag is short, favorable data transmission and reception can be carried out.

[0024]

In this manner, by using a transistor including an oxide semiconductor (in a broad sense, a transistor in which a reverse current can be small enough) in part of a demodulation circuit, the demodulation circuit can have excellent characteristics. Further, with the use of the demodulation circuit, an RFID tag having excellent characteristics can be realized.

BRIEF DESCRIPTION OF DRAWINGS

[0025]

In the accompanying drawings:

FIGS. 1A and 1B are circuit diagrams of semiconductor devices;

FIGS. 2A to 2C show operation of a semiconductor device;

FIGS. 3A to 3C show operation of a semiconductor device;

FIG. 4 illustrates an example of the structure of an RFID tag;

FIGS. 5A to 5D illustrate examples of the structure of a transistor; and

FIGS. 6A to 6E illustrate an example of a manufacturing method of a transistor.

BEST MODE FOR CARRYING OUT THE INVENTION

[0026]

Hereinafter, embodiments of the present invention will be described with reference to the drawings. Note that the present invention is not limited to the following description and it will be easily understood by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention should not be construed as being limited to the description in the following embodiments.

[0027]

Note that the position, the size, the range, or the like of each structure

illustrated in drawings and the like is not accurately represented in some cases for easy understanding. Therefore, the invention disclosed herein is not necessarily limited to such position, size, range, and the like disclosed in the drawings and the like.

[0028]

In this specification and the like, ordinal numbers such as "first", "second", and "third" are used in order to avoid confusion among components, and the terms do not limit the components numerically.

[0029]

(Embodiment 1)

In this embodiment, a circuit configuration and the like of a semiconductor device according to an embodiment of the invention disclosed herein will be described with reference to FIGS. 1A and 1B, FIGS. 2A to 2C, and FIGS. 3A to 3C. Note that in circuit diagrams, "OS" may be written beside a transistor in order to indicate that the transistor includes an oxide semiconductor.

[0030]

<Circuit Configuration>

First, circuit configurations and functions of components of a semiconductor device of an embodiment of the invention disclosed herein will be described with reference to FIGS. 1A and 1B.

[0031]

FIG. 1A shows an example of a demodulation circuit of the invention disclosed herein. The demodulation circuit includes a first transistor T1, a second transistor T2, a first capacitor C1, a second capacitor C2, a third capacitor C3, a first resistor R1, and a second resistor R2.

[0032]

Here, a gate terminal of the first transistor T1, a drain terminal (or a source terminal) of the first transistor T1, a source terminal (or a drain terminal) of the second transistor T2, and one terminal of the first capacitor C1 are electrically connected to each other. In addition, a gate terminal of the second transistor T2, a drain terminal (or a source terminal) of the second transistor T2, one terminal of the second capacitor C2, one terminal of the third capacitor C3, and one terminal of the first resistor R1 are electrically connected to each other. Further, a source terminal (or a drain terminal) of

the first transistor T1, the other terminal of the second capacitor C2, the other terminal of the first resistor R1, and one terminal of the second resistor R2 are electrically connected to each other. Furthermore, the other terminal of the third capacitor C3 and the other terminal of the second resistor R2 are electrically connected to each other. Note that the other terminal of the first capacitor C1 functions as an input terminal IN, and a node which is electrically connected to the other terminal of the third capacitor C3 and the other terminal of the second resistor R2 functions as an output terminal OUT.

[0033]

In the demodulation circuit shown in FIG. 1A, normally, a reference potential V_{GND} is supplied to a node GND which is electrically connected to the gate terminal of the second transistor T2, the drain terminal (or the source terminal) of the second transistor T2, the one terminal of the second capacitor C2, the one terminal of the third capacitor C3, and the one terminal of the first resistor R1.

[0034]

In the demodulation circuit shown in FIG. 1A, a channel formation region of the first transistor T1 and a channel formation region of the second transistor T2 are formed using a material which enables a reverse current to be small enough, for example, an oxide semiconductor. Thus, even in a situation where a high reverse voltage is applied between the source terminal and the drain terminal of the transistor, a sufficient rectifying function can be obtained. That is, a demodulation circuit having a sufficient demodulation ability can be realized.

[0035]

FIG. 1B shows another example of the demodulation circuit of the invention disclosed herein. Components of the demodulation circuit are similar to those of the demodulation circuit shown in FIG. 1A. That is, the demodulation circuit in FIG. 1B includes the first transistor T1, the second transistor T2, the first capacitor C1, the second capacitor C2, the third capacitor C3, the first resistor R1, and the second resistor R2.

[0036]

Note that the demodulation circuit shown in FIG. 1B is different from that of FIG. 1A in the connection relation of components.

[0037]

Specifically, the gate terminal of the second transistor T2, the drain terminal (or the source terminal) of the second transistor T2, the source terminal (or the drain terminal) of the first transistor T1, and the one terminal of the first capacitor C1 are electrically connected to each other. In addition, the source terminal (or the drain terminal) of the second transistor T2, the one terminal of the second capacitor C2, the one terminal of the third capacitor C3, and the one terminal of the first transistor R1 are electrically connected to each other. Further, the gate terminal of the first transistor T1, the drain terminal (or the source terminal) of the first transistor T1, the other terminal of the second capacitor C2, the other terminal of the first resistor R1, and the one terminal of the second resistor R2 are electrically connected to each other. Note that the other terminal of the first capacitor functions as an input terminal IN, and the node which is electrically connected to the other terminal of the third capacitor C3 and the other terminal of the second resistor R2 functions as an output terminal OUT.

[0038]

In the demodulation circuit shown in FIG. 1B, normally, a reference potential V_{GND} is supplied to the node GND which is electrically connected to the source terminal (or the drain terminal) of the second transistor T2, the one terminal of the second capacitor C2, the one terminal of the third capacitor C3, and the one terminal of the first resistor R1.

[0039]

In the demodulation circuit shown in FIG. 1B, a channel formation region of the first transistor T1 and a channel formation region of the second transistor T2 are formed using a material which enables a reverse current to be small enough, for example, an oxide semiconductor. Thus, even in a situation where a high reverse voltage is applied between the source terminal and the drain terminal of the transistor, a sufficient rectifying function can be obtained. That is, a demodulation circuit having a sufficient demodulation ability can be realized.

[0040]

In the demodulation circuits shown in FIGS. 1A and 1B, the first capacitor C1 has a function of compensating the center (reference line) of a wave amplitude. The second capacitor C2 has a function of smoothing a waveform. Further, the first resistor R1 has a function of keeping a current flowing through a point A constant.

[0041]

The resistance value of the first resistor R1 is determined on the basis of the capacitance of the second capacitor C2. If the resistance value of the first resistor R1 is too small, the amplitude of a signal obtained via a carrier wave becomes small. In contrast, if the resistance value of the first resistor R1 is too large, a breakdown phenomenon of the second transistor T2 is caused and the second transistor T2 does not operate normally.

[0042]

Further, the second resistor R2 and the third capacitor C3 function as a low-pass filter that removes a high-frequency component.

[0043]

<Features of Demodulation Circuit>

Next, features of the demodulation circuits shown in FIGS. 1A and 1B will be described with reference to FIGS. 2A to 2C and FIGS. 3A to 3C.

[0044]

First, a demodulated signal obtained with a conventional demodulation circuit will be described with reference to FIGS. 2A to 2C. FIG. 2A shows a carrier wave that is input to a demodulation circuit. The potential difference Vpp between a maximum potential and a minimum potential of the carrier wave is 2V (that is, the amplitude is V), and the carrier wave is modulated by 2ΔV.

[0045]

After demodulation of the carrier wave in "an ideal condition", a signal which can be expressed by an envelope in which a potential difference Vpp′ between a maximum potential and a minimum potential is 2V′ and a modulation amount is 2ΔV′ is obtained. Here, "an ideal condition" means such a condition where a reverse current is not generated in a transistor having a rectifying function in a demodulation circuit, in other words, such a condition where a potential on the input side and a potential on the output side of a transistor have a linear relation and a sufficient rectifying function can be obtained.

[0046]

In the above-described "ideal condition", the relations between an input

potential difference VIN (a potential difference between a maximum potential and a minimum potential of a carrier wave) of a demodulation circuit and an output potential difference VOUT of the demodulation circuit are expressed by a line A and a line B in FIG. 2C. Here, the line A shows a relation between the input potential difference VIN of a demodulation circuit and the output potential difference VOUT of the demodulation circuit in the case where modulation is not performed. The line B shows a relation between the input potential difference VIN of the demodulation circuit and the output potential difference VOUT of the demodulation circuit in the case where modulation is performed. That is, a difference between the VOUT when the VIN is Vpp in the line A and the VOUT when the VIN is Vpp in the line B corresponds to a potential difference (2ΔV′) in a modulated portion of the output signal.

[0047]

Various circuits are connected to the output teminal OUT side of the demodulation circuit, and various operations are carried out with the use of signals which are output in the above-described manner. Therefore, the output signal needs to have a sufficient and constant ratio of the potential difference in a modulated portion with respect to the potential difference Vpp′ between the maximum potential and the minimum potential.

[0048]

However, in a conventional demodulation circuit, when the input potential difference VIN is large, a large reverse current is generated in the transistor having a rectifying function, so that the rectifying function becomes weaker. As a result, the output from the demodulation circuit with respect to the input to the demodulation circuit is not linear, and a signal having a sufficient and constant strength ratio cannot be output. In other words, the output signal does not correspond to the envelope of the input (see FIGS. 2A and 2B).

[0049]

The relations between the input potential difference VIN and the output potential difference VOUT of the conventional demodulation circuit are expressed by a line C and a line D in FIG. 2C. From FIG. 2C, it can be understood that as compared to the signal potential difference Vpp′ and the potential difference 2ΔV′ in a modulated

portion in an ideal condition, a conventional demodulation circuit has a smaller signal potential difference of Vpp'' and a smaller potential difference in a modulated portion of $2\Delta V''$. In addition, since the input potential difference VIN and the output potential difference VOUT are not linear, in the output signal, the ratio of the potential difference in a modulated portion with respect to the potential difference between a maximum potential and a minimum potential varies depending on the input potential difference VIN.

[0050]

On the other hand, in a demodulation circuit of an embodiment of the invention disclosed herein, a transistor having a rectifying function includes a material which enables a reverse current to be small enough, for example, an oxide semiconductor. Accordingly, the phenomenon of a rectifying function becoming weaker due to generation of a reverse current can be suppressed, and saturation of the output from the demodulation circuit can be prevented. In other words, the output from the demodulation circuit corresponding to the input to the demodulation circuit can be linear and a condition sufficiently close to the "ideal condition" can be made (see FIGS. 3A and 3B).

[0051]

Rectifying characteristics of a transistor whose gate terminal and drain terminal (or source terminal) are connected to each other is shown in FIG. 3C. In the drawing, a broken line 101 shows rectifying characteristics of a conventional transistor (e.g., a transistor including silicon), and a solid line 103 shows rectifying characteristics of a transistor including a material which enables a reverse current to be small enough, (e.g., a transistor including an oxide semiconductor). From FIG. 3C, it is found that both the conventional transistor and the transistor including a material which enables a reverse current to be small enough have favorable characteristics when being applied with a forward voltage. When a reverse voltage is applied, the characteristics of the conventional transistor are degraded; in contrast, the characteristics of the transistor including a material which enables a reverse current to be small enough are favorable. Using a transistor in which a reverse current is not generated even when a high reverse voltage is applied, a demodulation circuit having a sufficient demodulation ability can

be realized.

[0052]

(Embodiment 2)

In this embodiment, an RFID tag which is an example to which the demodulation circuit described in the above embodiment is applied will be described with reference to FIG. 4.

[0053]

The RFID tag of this embodiment includes a memory circuit storing necessary data and exchanges data with the outside using contactless means such as wireless communication. Having these features, the RFID tag can be used for an individual authentication system in which an object is identified by reading individual information of the object, or the like. Note that the RFID tag is required to have extremely high reliability in order to be used for this purpose.

[0054]

A configuration of the RFID tag will be described with reference to FIG. 4. FIG. 4 is a block diagram showing a configuration of an RFID tag.

[0055]

As shown in FIG. 4, an RFID tag 300 includes an antenna 304 which receives a radio signal 303 that is transmitted from an antenna 302 connected to a communication device 301 (also referred to as an interrogator, a reader/writer, or the like). The RFID tag 300 includes a rectifier circuit 305, a constant voltage circuit 306, a demodulation circuit 307, a modulation circuit 308, a logic circuit 309, a memory circuit 310, and a ROM 311. In a manner similar to that of the above embodiment, the demodulation circuit 307 includes a material which enables a reverse current to be small enough, for example, an oxide semiconductor, in part of a transistor. Note that data transmission methods are roughly classified into the following three methods: an electromagnetic coupling method in which a pair of coils is provided so as to face each other and communicates with each other by mutual induction, an electromagnetic induction method in which communication is performed using an induction field, and a radio wave method in which communication is performed using a radio wave. Any of these methods can be used in the RFID tag 300 of this embodiment.

[0056]

Next, the structure of each circuit will be described. The antenna 304 exchanges the radio signal 303 with the antenna 302 which is connected to the communication device 301. The rectifier circuit 305 generates an input potential by rectification, for example, half-wave voltage doubler rectification of an input alternating signal generated by reception of a radio signal at the antenna 304 and smoothing of the rectified signal with a capacitor provided in a later stage in the rectifier circuit 305. Note that a limiter circuit may be provided on an input side or an output side of the rectifier circuit 305. The limiter circuit controls electric power so that electric power which is higher than or equal to certain electric power is not input to a circuit in a later stage if the amplitude of the input alternating signal is high and an internal generation voltage is high.

[0057]

The constant voltage circuit 306 generates a stable power supply voltage from an input potential and supplies it to each circuit. Note that the constant voltage circuit 306 may include a reset signal generation circuit. The reset signal generation circuit is a circuit which generates a reset signal of the logic circuit 309 by utilizing rise of the stable power supply voltage.

[0058]

The demodulation circuit 307 demodulates the input alternating signal by envelope detection and generates the demodulated signal. The demodulation circuit described in the above embodiment can be applied to the demodulation circuit 307. Further, the modulation circuit 308 performs modulation in accordance with data to be output from the antenna 304.

[0059]

The logic circuit 309 analyzes and processes the demodulated signal. The memory circuit 310 holds the input data and includes a row decoder, a column decoder, a memory region, and the like. Further, the ROM 311 stores an identification number (ID) or the like and outputs it in accordance with processing.

[0060]

Note that any of the above-described circuits may be omitted as appropriate.

[0061]

In this embodiment, the demodulation circuit described in the above

embodiment is mounted on the RFID tag 300. Therefore, even in a situation where the distance between the RFID tag 300 and the communication device 301 is short and the intensity of an input signal is high, a sufficient demodulation ability can be achieved. As a result, errors at the time of transmitting or receiving data can be reduced. That is, the RFID tag 300 can have high reliability of data transmission and reception.

[0062]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0063]

(Embodiment 3)

In this embodiment, examples of a transistor which can be applied to the demodulation circuit described in the above embodiment will be described with reference to FIGS. 5A to 5D. There is no particular limitation on the structure of the transistor; for example, a staggered type or a planar type having a top-gate structure or a bottom-gate structure can be employed as appropriate. Further, the transistor may have any of a single gate structure including one channel formation region, a double gate structure including two channel formation regions, or a triple gate structure including three channel formation regions. Alternatively, the transistor may have a dual gate structure including two gate electrode layers positioned over and below a channel region with a gate insulating layer provided therebetween.

[0064]

FIGS. 5A to 5D each illustrate an example of a cross-sectional structure of a transistor. Transistors illustrated in FIGS. 5A to 5D are transistors including an oxide semiconductor as a semiconductor. An advantage of using an oxide semiconductor is that high mobility and a low off-state current can be obtained with an easy and low-temperature process.

[0065]

A transistor 410 illustrated in FIG. 5A is an example of bottom-gate transistors, and is also referred to as an inverted staggered transistor.

[0066]

The transistor 410 includes, over a substrate 400 having an insulating surface, a

gate electrode layer 401, a gate insulating layer 402, an oxide semiconductor layer 403, a source electrode layer 405a, and a drain electrode layer 405b. Further, an insulating layer 407 being in contact with the oxide semiconductor layer 403 is provided so as to cover the transistor 410. Further, a protective insulating layer 409 is formed over the insulating layer 407.

[0067]

A transistor 420 illustrated in FIG. 5B is an example of bottom-gate transistors called channel-protective (channel-stop) transistors and is also called an inverted staggered transistor.

[0068]

The transistor 420 includes, over the substrate 400 having an insulating surface, the gate electrode layer 401, the gate insulating layer 402, the oxide semiconductor layer 403, an insulating layer 427 which functions as a channel protective layer, the source electrode layer 405a, and the drain electrode layer 405b. Further, the protective insulating layer 409 is formed so as to cover the transistor 420.

[0069]

A transistor 430 illustrated in FIG. 5C is an example of bottom-gate transistors. The transistor 430 includes, over the substrate 400 having an insulating surface, the gate electrode layer 401, the gate insulating layer 402, the source electrode layer 405a, the drain electrode layer 405b, and the oxide semiconductor layer 403. Further, the insulating layer 407 being in contact with the oxide semiconductor layer 403 is provided so as to cover the transistor 430. The protective insulating layer 409 is further formed over the insulating layer 407.

[0070]

In the transistor 430, the gate insulating layer 402 is provided over and in contact with the substrate 400 and the gate electrode layer 401; the source electrode layer 405a and the drain electrode layer 405b are provided over and in contact with the gate insulating layer 402. In addition, the oxide semiconductor layer 403 is provided over the gate insulating layer 402, the source electrode layer 405a, and the drain electrode layer 405b.

[0071]

A transistor 440 illustrated in FIG. 5D is an example of top-gate transistors.

The transistor 440 includes, over the substrate 400 having an insulating surface, an insulating layer 437, the oxide semiconductor layer 403, the source electrode layer 405a, the drain electrode layer 405b, the gate insulating layer 402, and the gate electrode layer 401. A wiring layer 436a and a wiring layer 436b are provided in contact with the source electrode layer 405a and the drain electrode layer 405b, respectively.

[0072]

In this embodiment, as described above, the oxide semiconductor layer 403 is used as a semiconductor layer. As examples of an oxide semiconductor used for the oxide semiconductor layer 403, there are an In-Sn-Ga-Zn-O-based oxide semiconductor which is a four-component metal oxide; an In-Ga-Zn-O-based oxide semiconductor, an In-Sn-Zn-O-based oxide semiconductor, an In-Al-Zn-O-based oxide semiconductor, a Sn-Ga-Zn-O-based oxide semiconductor, an Al-Ga-Zn-O-based oxide semiconductor, and a Sn-Al-Zn-O-based oxide semiconductor which are three-component metal oxides; an In-Zn-O-based oxide semiconductor, a Sn-Zn-O-based oxide semiconductor, an Al-Zn-O-based oxide semiconductor, a Zn-Mg-O-based oxide semiconductor, a Sn-Mg-O-based oxide semiconductor, and an In-Mg-O-based oxide semiconductor which are two-component metal oxides; and an In-O-based oxide semiconductor, a Sn-O-based oxide semiconductor, and a Zn-O-based oxide semiconductor. Further, SiO_2 may be added to the above-described oxide semiconductor. Here, for example, an In-Ga-Zn-O-based oxide semiconductor is an oxide including at least In, Ga, and Zn, and there is no particular limitation on the composition ratio thereof. Further, the In-Ga-Zn-O-based oxide semiconductor may include an element other than In, Ga, and Zn.

[0073]

For the oxide semiconductor layer 403, an oxide semiconductor represented by the chemical formula, $InMO_3(ZnO)_m$ ($m > 0$) can be used. Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, M may be Ga, Ga and Al, Ga and Mn, Ga and Co, or the like.

[0074]

In the transistor 410, the transistor 420, the transistor 430, and the transistor 440 which include the oxide semiconductor layer 403, a reverse current can be made small enough. By using such transistor, a demodulation circuit having a sufficient

demodulation ability can be realized.

[0075]

There is no particular limitation on the substrate that can be used as the substrate 400 having an insulating surface. For example, a glass substrate, a quartz substrate, or the like which is used in a liquid crystal display device or the like can be used. Alternatively, a substrate in which an insulating layer is formed over a silicon wafer, or the like may be used.

[0076]

In the bottom-gate transistors 410, 420, and 430, an insulating layer serving as a base may be provided between the substrate and the gate electrode layer. The insulating layer has a function of preventing diffusion of an impurity element from the substrate, and can be formed of one or more of a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

[0077]

The gate electrode layer 401 can be formed using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material which includes any of these metal materials as a main component. The gate electrode layer 401 may have either a single-layer structure or a stacked structure.

[0078]

The gate insulating layer 402 can be formed of one or more of a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, an aluminum nitride oxide film, and a hafnium oxide film by a plasma CVD method, a sputtering method, or the like. For example, a gate insulating layer (e.g., with a total thickness of 200 nm) can be formed in such a manner that a silicon nitride film (SiN_y ($y > 0$)) with a thickness of 50 nm to 200 nm is formed as a first gate insulating layer by a plasma CVD method and a silicon oxide film (SiO_x ($x > 0$)) with a thickness of 5 nm to 300 nm is stacked over the first gate insulating layer by a sputtering method as a second gate insulating layer.

[0079]

The source electrode layer 405a and the drain electrode layer 405b can be formed using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material which includes any of these metal materials as a main component. For example, the source electrode layer 405a and the drain electrode layer 405b can have a stacked structure of a layer of metal such as aluminum, copper, or the like and a layer of high-melting-point metal such as titanium, molybdenum, or tungsten. An aluminum material including an element which prevents generation of hillocks or whiskers (e.g., silicon, neodymium, or scandium) may be used for higher heat resistance.

[0080]

Alternatively, the conductive film to be the source electrode layer 405a and the drain electrode layer 405b (including a wiring layer formed in the same layer as the source and drain electrode layers) may be a conductive metal oxide film. As a conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), indium oxide-tin oxide alloy (In_2O_3-SnO_2, which is abbreviated as ITO in some cases), indium oxide-zinc oxide alloy (In_2O_3-ZnO), any of these metal oxide materials in which silicon oxide is contained, or the like can be used.

[0081]

A material similar to that of the source electrode layer 405a and the drain electrode layer 405b can be used for the wiring layer 436a and the wiring layer 436b which are in contact with the source electrode layer 405a and the drain electrode layer 405b, respectively.

[0082]

As the insulating layers 407, 427, and 437, an inorganic insulating film typified by a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, and an aluminum oxynitride film, can be used.

[0083]

As the protective insulating layer 409, an inorganic insulating film such as a silicon nitride film, an aluminum nitride film, a silicon nitride oxide film, or an aluminum nitride oxide film can be used.

[0084]

In addition, a planarization insulating film may be formed over the protective

insulating layer 409 in order to reduce surface unevenness due to the transistor. As the planarization insulating film, an organic material such as polyimide, acrylic, or benzocyclobutene can be used. Other than such organic materials, it is also possible to use a low-dielectric constant material (a low-k material) or the like. Note that the planarization insulating film may be formed by stacking a plurality of insulating films formed of these materials.

[0085]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0086]

(Embodiment 4)

In this embodiment, an example of a transistor including an oxide semiconductor layer and an example of a manufacturing method thereof will be described in detail with reference to FIGS. 6A to 6E.

[0087]

FIGS. 6A to 6E are cross-sectional views illustrating a manufacturing process of a transistor. A transistor 510 illustrated here is an inverted staggered transistor similar to the transistor 410 illustrated in FIG. 5A.

[0088]

An oxide semiconductor used for a semiconductor layer of this embodiment is an i-type (intrinsic) oxide semiconductor or a substantially i-type (intrinsic) oxide semiconductor. The i-type (intrinsic) oxide semiconductor or substantially i-type (intrinsic) oxide semiconductor is obtained in such a manner that hydrogen, which is an n-type impurity, is removed from an oxide semiconductor, and the oxide semiconductor is purified so as to contain as few impurities that are other than main components of the oxide semiconductor as possible.

[0089]

Note that the purified oxide semiconductor includes extremely few carriers, and the carrier concentration is lower than 1×10^{14} /cm^3, preferably lower than 1×10^{12} /cm^3, further preferably lower than 1×10^{11} /cm^3. Such few carriers enable a current in

an off state (off-state current) to be small enough.

[0090]

Specifically, in the transistor including the above-described oxide semiconductor layer, the off-state current density per channel width of 1 μm at room temperature (25 °C) can be 100 zA/μm (1×10^{-19} A/μm) or lower, or further 10 zA/μm (1×10^{-20} A/μm) or lower under conditions where the channel length L of the transistor is 10 μm and the source-drain voltage is 3 V.

[0091]

The transistor 510 including the purified oxide semiconductor layer hardly has temperature dependence of an on-state current and also has an extremely small off-state current.

[0092]

A process for manufacturing the transistor 510 over a substrate 505 will be described with reference to FIGS. 6A to 6E.

[0093]

First, a conductive film is formed over the substrate 505 having an insulating surface, and then a gate electrode layer 511 is formed through a first photolithography process. Note that a resist mask used in the photolithography process may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask; thus, manufacturing cost can be reduced.

[0094]

As the substrate 505 having an insulating surface, a substrate similar to the substrate 400 described in the above embodiment can be used. In this embodiment, a glass substrate is used as the substrate 505.

[0095]

An insulating layer serving as a base may be provided between the substrate 505 and the gate electrode layer 511. The insulating layer has a function of preventing diffusion of an impurity element from the substrate 505, and can be formed of one or more films selected from a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, a silicon oxynitride film, and the like.

[0096]

The gate electrode layer 511 can be formed using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material which includes any of these metal materials as a main component. The gate electrode layer 511 can have a single-layer structure or a stacked structure.

[0097]

Next, a gate insulating layer 507 is formed over the gate electrode layer 511. The gate insulating layer 507 can be formed by a plasma CVD method, a sputtering method, or the like. The gate insulating layer 507 can be formed of one or more films selected from a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a silicon nitride oxide film, an aluminum oxide film, an aluminum nitride film, an aluminum oxynitride film, an aluminum nitride oxide film, a hafnium oxide film, and the like.

[0098]

Further, in order that hydrogen, a hydroxyl group, and moisture are contained as little as possible in the gate insulating layer 507 and an oxide semiconductor film 530, it is preferable to preheat the substrate 505 over which the gate electrode layer 511 is formed or the substrate 505 over which the gate electrode layer 511 and the gate insulating layer 507 are formed, in a preheating chamber of a sputtering apparatus as pretreatment for the formation of the oxide semiconductor film 530, so that impurities such as hydrogen and moisture adsorbed on the substrate 505 are eliminated. As an evacuation unit, a cryopump is preferably provided in the preheating chamber. This preheating step may be performed on the substrate 505 over which layers up to and including a source electrode layer 515a and a drain electrode layer 515b are formed. Note that this preheating treatment can be omitted.

[0099]

Next, over the gate insulating layer 507, the oxide semiconductor film 530 with a thickness of greater than or equal to 2 nm and less than or equal to 200 nm, preferably greater than or equal to 5 nm and less than or equal to 30 nm is formed (see FIG. 6A).

[0100]

For the oxide semiconductor film 530, any of the four-component metal oxide, the three-component metal oxides, the two-component metal oxides, an In-O-based

oxide semiconductor, a Sn-O-based oxide semiconductor, a Zn-O-based oxide semiconductor, and the like, which are described in the above embodiment, can be used.

[0101]

As a target for forming the oxide semiconductor film 530 by a sputtering method, it is particularly preferable to use a target having a composition ratio of In:Ga:Zn = 1:x:y (x is 0 or more and y is more than or equal to 0.5 and less than or equal to 5). For example, a target having a composition ratio of In:Ga:Zn = 1:1:1 [atomic ratio] (x = 1, y = 1) (that is, In_2O_3:Ga_2O_3:ZnO = 1:1:2 [molar ratio]) can be used. Alternatively, a target having a composition ratio of In:Ga:Zn = 1:1:0.5 [atomic ratio] (x = 1, y = 0.5), a target having a composition ratio of In:Ga:Zn = 1:1:2 [atomic ratio] (x = 1, y = 2), or a target having a composition ratio of In:Ga:Zn = 1:0:1 [atomic ratio] (x = 0, y = 1) can be used.

[0102]

In this embodiment, an oxide semiconductor layer having an amorphous structure is formed by a sputtering method using an In-Ga-Zn-O-based metal oxide target.

[0103]

The relative density of a metal oxide in the metal oxide target is greater than or equal to 80 %, preferably greater than or equal to 95 %, and further preferably greater than or equal to 99.9 %. The use of a metal oxide target having high relative density makes it possible to form an oxide semiconductor layer with a dense structure.

[0104]

The atmosphere in which the oxide semiconductor film 530 is formed is preferably a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere containing a rare gas (typically, argon) and oxygen. Specifically, it is preferable to use, for example, an atmosphere of a high-purity gas from which an impurity such as hydrogen, water, a hydroxyl group, or hydride is removed so that the concentration of the impurity is 1 ppm or lower (preferably the concentration is 10 ppb or lower).

[0105]

In the formation of the oxide semiconductor film 530, for example, a process

object may be held in a treatment chamber that is kept under reduced pressure and the process object may be heated so that the temperature of the process object is higher than or equal to 100 °C and lower than 550 °C, preferably higher than or equal to 200 °C and lower than or equal to 400 °C. Alternatively, the temperature of the process object in the formation of the oxide semiconductor film 530 may be room temperature (25 °C ± 10 °C). Then, a sputtering gas from which hydrogen, water, or the like is removed is introduced while moisture in the treatment chamber is removed, and the aforementioned target is used, whereby the oxide semiconductor film 530 is formed. In forming the oxide semiconductor film 530 while heating the process object, impurities in the oxide semiconductor layer can be reduced. Further, damage due to sputtering can be reduced. In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, a titanium sublimation pump, or the like can be used. Alternatively, a turbo pump provided with a cold trap may be used. By evacuation with the cryopump or the like, hydrogen, water, and the like can be removed from the treatment chamber, whereby the impurity concentration in the oxide semiconductor film 530 can be reduced.

[0106]

The oxide semiconductor film 530 can be formed under the following conditions, for example: the distance between the process object and the target is 170 mm, the pressure is 0.4 Pa, the direct-current (DC) power is 0.5 kW, and the atmosphere is an oxygen (oxygen: 100 %) atmosphere, an argon (argon: 100 %) atmosphere, or a mixed atmosphere including oxygen and argon. Note that a pulsed direct-current (DC) power source is preferably used because dust (such as powder substances formed at the time of film formation) can be reduced and the film thickness can be uniform. The thickness of the oxide semiconductor film 530 is greater than or equal to 1 nm and less than or equal to 50 nm, preferably greater than or equal to 1 nm and less than or equal to 30 nm, and further preferably greater than or equal to 1 nm and less than or equal to 10 nm. With the oxide semiconductor film 530 having such a thickness, a short-channel effect due to miniaturization can be suppressed. Note that the appropriate thickness differs depending on the oxide semiconductor material to be used, the intended use of the semiconductor device, and the like; therefore, the thickness may be determined in

accordance with the material, the intended use, and the like.

[0107]

Note that before the oxide semiconductor film 530 is formed by a sputtering method, a substance attached to a surface where the oxide semiconductor film 530 is to be formed (e.g., a surface of the gate insulating layer 507) is preferably removed by reverse sputtering in which an argon gas is introduced to generate plasma. Here, the reverse sputtering is a method in which ions collide with a process surface so that the surface is modified, in contrast to normal sputtering in which ions collide with a sputtering target. As an example of a method for making ions collide with a process surface, there is a method in which high-frequency voltage is applied to the process surface in an argon atmosphere so that plasma is generated in the vicinity of the process object. Note that an atmosphere of nitrogen, helium, oxygen, or the like may be used instead of an argon atmosphere.

[0108]

Next, the oxide semiconductor film 530 is processed into an island-shaped oxide semiconductor layer through a second photolithography process. Note that a resist mask used in the photolithography process may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask; thus, manufacturing cost can be reduced.

[0109]

In the case where a contact hole is formed in the gate insulating layer 507, a step of forming the contact hole can be performed at the same time as processing of the oxide semiconductor film 530.

[0110]

As the etching of the oxide semiconductor film 530, either wet etching or dry etching or both of them may be employed. As an etchant used for wet etching of the oxide semiconductor film 530, a solution obtained by mixing phosphoric acid, acetic acid, and nitric acid, an ammonia peroxide mixture (31 wt% hydrogen peroxide water : 28 wt% ammonia water : water = 5:2:2), or the like can be used. An etchant such as ITO07N (produced by KANTO CHEMICAL CO., INC.) may also be used.

[0111]

Then, heat treatment (first heat treatment) is performed on the oxide semiconductor layer, so that an oxide semiconductor layer 531 is formed (see FIG. 6B). By the first heat treatment, excessive hydrogen (including water and a hydroxyl group) in the oxide semiconductor layer is removed and a structure of the oxide semiconductor layer is improved, so that defect level in energy gap can be reduced. The temperature of the first heat treatment is, for example, higher than or equal to 300 °C and lower than 550 °C, or higher than or equal to 400 °C and lower than or equal to 500 °C.

[0112]

The heat treatment can be performed in such a way that, for example, a process object is introduced into an electric furnace in which a resistance heating element or the like is used and heated at 450 °C under a nitrogen atmosphere for an hour. During the heat treatment, the oxide semiconductor layer is not exposed to the air, in order to prevent entry of water and hydrogen.

[0113]

The heat treatment apparatus is not limited to an electric furnace; the heat treatment apparatus can be an apparatus that heats a process object using thermal radiation or thermal conduction from a medium such as a heated gas or the like. For example, an RTA (rapid thermal annealing) apparatus such as a GRTA (gas rapid thermal annealing) apparatus or an LRTA (lamp rapid thermal annealing) apparatus can be used. An LRTA apparatus is an apparatus for heating a process object using radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with a process object by heat treatment, such as nitrogen or a rare gas such as argon is used.

[0114]

For example, as the first heat treatment, GRTA treatment may be performed in the following manner. The process object is put in an inert gas atmosphere that has been heated, heated for several minutes, and then taken out of the inert gas atmosphere. The GRTA treatment enables high-temperature heat treatment in a short time.

Moreover, in the GRTA treatment, even conditions of the temperature that exceeds the upper temperature limit of the process object can be employed. Note that the gas may be switched from the inert gas to a gas including oxygen during the process. This is because defect levels in the energy gap due to oxygen deficiency can be reduced by performing the first heat treatment in an atmosphere including oxygen.

[0115]

Note that as the inert gas atmosphere, an atmosphere that contains nitrogen or a rare gas (e.g., helium, neon, or argon) as its main component and does not contain water, hydrogen, or the like is preferably used. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is set to 6 N (99.9999 %) or more, preferably 7 N (99.99999 %) or more (i.e., the impurity concentration is 1 ppm or less, preferably 0.1 ppm or less).

[0116]

In any case, when impurities are reduced by the first heat treatment to form the oxide semiconductor layer that is an i-type (intrinsic) or substantially i-type semiconductor layer, a transistor with extremely excellent characteristics can be realized.

[0117]

The above heat treatment (first heat treatment) has an effect of removing hydrogen, water, and the like and thus can be referred to as dehydration treatment, dehydrogenation treatment, or the like. The dehydration treatment or the dehydrogenation treatment can be performed after the formation of the oxide semiconductor film 530 and before the oxide semiconductor film 530 is processed into the island-shaped oxide semiconductor layer. Such dehydration treatment or dehydrogenation treatment may be conducted once or plural times.

[0118]

The first heat treatment can be performed at any of the following timings other than the above timing: after formation of a source electrode layer and a drain electrode layer, after formation of an insulating layer over the source electrode layer and the drain electrode layer, and the like.

[0119]

Next, a conductive film to be a source electrode layer and a drain electrode

layer (including a wiring formed from the same film as the source electrode layer and the drain electrode layer) is formed over the gate insulating layer 507 and the oxide semiconductor layer 531. The conductive film used to form the source electrode layer and the drain electrode layer can be formed using any of the materials described in the above embodiment.

[0120]

A resist mask is formed over the conductive film in a third photolithography process, and the source electrode layer 515a and the drain electrode layer 515b are formed by selective etching, and then, the resist mask is removed (see FIG. 6C).

[0121]

Light exposure at the time of formation of the resist mask in the third photolithography process may be performed using ultraviolet light, KrF laser light, or ArF laser light. Note that the channel length (L) of the transistor is determined by the distance between the source electrode layer and the drain electrode layer. Therefore, in light exposure for forming a mask which is used for forming a transistor with a channel length (L) of less than 25 nm, it is preferable to use extreme ultraviolet light whose wavelength is as short as several nanometers to several tens of nanometers. In light exposure using extreme ultraviolet light, resolution is high and depth of focus is large. For these reasons, the channel length (L) of the transistor completed later can be greater than or equal to 10 nm and less than or equal to 1000 nm (1 μm), and the circuit can operate at high speed. Moreover, power consumption of the semiconductor device can be reduced by miniaturization.

[0122]

In order to reduce the number of photomasks and the number of photolithography processes, the etching step may be performed using a resist mask formed with a multi-tone mask. Since a resist mask formed with a multi-tone mask includes regions of plural thicknesses and can be further changed in shape by performing etching, the resist mask can be used in a plurality of etching steps to provide different patterns. Therefore, a resist mask corresponding to at least two kinds of different patterns can be formed with one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography processes can also be reduced, whereby simplification of the process

can be realized.

[0123]

Note that it is preferable that etching conditions be optimized so as not to etch and divide the oxide semiconductor layer 531 when the conductive film is etched. However, it is difficult to obtain etching conditions in which only the conductive film is etched and the oxide semiconductor layer 531 is not etched at all. In some cases, part of the oxide semiconductor layer 531 is etched when the conductive film is etched, whereby the oxide semiconductor layer 531 having a groove portion (a recessed portion) is formed.

[0124]

Either wet etching or dry etching may be used for the etching of the conductive film. Note that dry etching is preferably used in terms of microfabrication of the element. An etching gas and an etchant can be selected as appropriate in accordance with a material of a layer to be etched. In this embodiment, a titanium film is used as the conductive film and an In-Ga-Zn-O based material is used for the oxide semiconductor layer 531; accordingly, in the case of employing wet etching, an ammonia hydrogen peroxide solution (a mixture of ammonia, water, and a hydrogen peroxide solution) is used as an etchant.

[0125]

Next, plasma treatment using a gas such as N_2O, N_2, or Ar is preferably performed, so that water, hydrogen, or the like attached to a surface of an exposed portion of the oxide semiconductor layer may be removed. In the case of performing the plasma treatment, an insulating layer 516 serving as a protective insulating film is formed without being exposed to the air.

[0126]

The insulating layer 516 is preferably formed to a thickness of at least 1 nm by a method by which an impurity such as water or hydrogen is not introduced into the insulating layer 516, such as a sputtering method. When hydrogen is contained in the insulating layer 516, entry of the hydrogen to the oxide semiconductor layer, or extraction of oxygen in the oxide semiconductor layer by the hydrogen is caused, thereby causing the backchannel of the oxide semiconductor layer to have lower resistance (to have an n-type conductivity), so that a parasitic channel may be formed.

As the insulating layer 516, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, or the like is preferably used.

[0127]

In this embodiment, a silicon oxide film is formed to a thickness of 200 nm by a sputtering method as the insulating layer 516. The substrate temperature in deposition may be higher than or equal to room temperature (25 °C) and lower than or equal to 300 °C, and is 100 °C in this embodiment. The silicon oxide film can be deposited by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere containing a rare gas and oxygen. As a target, a silicon oxide target or a silicon target may be used.

[0128]

In order to remove residual moisture in the deposition chamber for the insulating layer 516 in a manner similar to that of the deposition of the oxide semiconductor film 530, an entrapment vacuum pump (such as a cryopump) is preferably used. When the insulating layer 516 is deposited in the deposition chamber which is evacuated using a cryopump, the impurity concentration in the insulating layer 516 can be reduced. A turbo pump provided with a cold trap may be used as an evacuation unit for removing moisture remaining in the deposition chamber used for forming the insulating layer 516.

[0129]

A sputtering gas used for depositing the insulating layer 516 is preferably a high-purity gas from which an impurity such as hydrogen or water is removed.

[0130]

Next, second heat treatment is performed in an inert gas atmosphere or an oxygen gas atmosphere. The second heat treatment is performed at a temperature higher than or equal to 200 °C and lower than or equal to 450 °C, preferably higher than or equal to 250 °C and lower than or equal to 350 °C. For example, the heat treatment may be performed at 250 °C for 1 hour in a nitrogen atmosphere. The second heat treatment can reduce variation in electric characteristics of the transistor. By supply of oxygen from the insulating layer 516 to the oxide semiconductor layer 531, an oxygen deficiency in the oxide semiconductor layer 531 is compensated, whereby an i-type

(intrinsic) or substantially i-type oxide semiconductor layer can be formed.

[0131]

In this embodiment, the second heat treatment is performed after the formation of the insulating layer 516; however, the timing of the second heat treatment is not limited thereto. For example, the first heat treatment may be followed by the second heat treatment, or the first heat treatment may also serve as the second heat treatment.

[0132]

In the above-described manner, through the first heat treatment and the second heat treatment, the oxide semiconductor layer 531 is purified so as not to contain an impurity other than main components of the oxide semiconductor layer, whereby the oxide semiconductor layer 531 can become an i-type (intrinsic) oxide semiconductor layer.

[0133]

Through the above-described process, the transistor 510 is formed (see FIG. 6D).

[0134]

It is preferable to further form a protective insulating layer 506 over the insulating layer 516 (see FIG. 6E). The protective insulating layer 506 prevents entry of hydrogen, water, and the like from the outside. As the protective insulating layer 506, a silicon nitride film, an aluminum nitride film, or the like can be used, for example. The formation method of the protective insulating layer 506 is not particularly limited; however, an RF sputtering method is suitable because of its high productivity.

[0135]

After the formation of the protective insulating layer 506, heat treatment may be further performed at a temperature of 100 °C to 200 °C inclusive for 1 hour to 30 hours inclusive in the air.

[0136]

With the use of the transistor which includes a purified oxide semiconductor layer and is manufactured in accordance with this embodiment, a reverse current can be made small enough. Therefore, in the case of using this transistor in a demodulation circuit, the demodulation circuit can have a sufficient demodulation ability.

[0137]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

5

This application is based on Japanese Patent Application serial no. 2010-034858 filed with Japan Patent Office on February 19, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A demodulation circuit comprising:

a first transistor comprising a channel formation region including an oxide semiconductor;

a second transistor comprising a channel formation region including an oxide semiconductor;

a first capacitor;

a second capacitor;

a third capacitor;

a first resistor; and

a second resistor,

wherein a gate terminal of the first transistor, a drain terminal of the first transistor, a source terminal of the second transistor, and one terminal of the first capacitor are electrically connected to each other,

wherein a gate terminal of the second transistor, a drain terminal of the second transistor, one terminal of the second capacitor, one terminal of the third capacitor, and one terminal of the first resistor are electrically connected to each other,

wherein a source terminal of the first transistor, the other terminal of the second capacitor, the other terminal of the first resistor, and one terminal of the second resistor are electrically connected to each other, and

wherein the other terminal of the third capacitor and the other terminal of the second resistor are electrically connected to each other.

2. The demodulation circuit according to claim 1,

wherein a reference potential is supplied to a node which is electrically connected to the gate terminal of the second transistor, the drain terminal of the second transistor, the one terminal of the second capacitor, the one terminal of the third capacitor, and the one terminal of the first resistor.

3. An RFID tag comprising the demodulation circuit according to claim 1.

4. A demodulation circuit comprising:

a first transistor comprising a channel formation region including an oxide semiconductor;

a second transistor comprising a channel formation region including an oxide semiconductor;

a first capacitor;

a second capacitor;

a third capacitor;

a first resistor; and

a second resistor,

wherein a gate terminal of the second transistor, a drain terminal of the second transistor, a source terminal of the first transistor, and one terminal of the first capacitor are electrically connected to each other,

wherein a source terminal of the second transistor, one terminal of the second capacitor, one terminal of the third capacitor, and one terminal of the first resistor are electrically connected to each other,

wherein a gate terminal of the first transistor, a drain terminal of the first transistor, the other terminal of the second capacitor, the other terminal of the first resistor, and one terminal of the second resistor are electrically connected to each other, and

wherein the other terminal of the third capacitor and the other terminal of the second resistor are electrically connected to each other.

5. The demodulation circuit according to claim 4,

wherein a reference potential is supplied to a node which is electrically connected to the source terminal of the second transistor, the one terminal of the second capacitor, the one terminal of the third capacitor, and the one terminal of the first resistor.

6. An RFID tag comprising the demodulation circuit according to claim 4.

7. A demodulation circuit comprising:

a first transistor comprising a semiconductor material with an energy gap of

larger than 3 eV;

a second transistor comprising a semiconductor material with an energy gap of larger than 3 eV;

a first capacitor;

a second capacitor;

a third capacitor;

a first resistor; and

a second resistor,

wherein a gate terminal of the first transistor, a drain terminal of the first transistor, a source terminal of the second transistor, and one terminal of the first capacitor are electrically connected to each other,

wherein a gate terminal of the second transistor, a drain terminal of the second transistor, one terminal of the second capacitor, one terminal of the third capacitor, and one terminal of the first resistor are electrically connected to each other,

wherein a source terminal of the first transistor, the other terminal of the second capacitor, the other terminal of the first resistor, and one terminal of the second resistor are electrically connected to each other, and

wherein the other terminal of the third capacitor and the other terminal of the second resistor are electrically connected to each other.

8. The demodulation circuit according to claim 7,

wherein a reference potential is supplied to a node which is electrically connected to the gate terminal of the second transistor, the drain terminal of the second transistor, the one terminal of the second capacitor, the one terminal of the third capacitor, and the one terminal of the first resistor.

9. An RFID tag comprising the demodulation circuit according to claim 7.

10. A demodulation circuit comprising:

a first transistor comprising a semiconductor material with an energy gap of larger than 3 eV;

a second transistor comprising a semiconductor material with an energy gap of

larger than 3 eV;

a first capacitor;

a second capacitor;

a third capacitor;

a first resistor; and

a second resistor,

wherein a gate terminal of the second transistor, a drain terminal of the second transistor, a source terminal of the first transistor, and one terminal of the first capacitor are electrically connected to each other,

wherein a source terminal of the second transistor, one terminal of the second capacitor, one terminal of the third capacitor, and one terminal of the first resistor are electrically connected to each other,

wherein a gate terminal of the first transistor, a drain terminal of the first transistor, the other terminal of the second capacitor, the other terminal of the first resistor, and one terminal of the second resistor are electrically connected to each other, and

wherein the other terminal of the third capacitor and the other terminal of the second resistor are electrically connected to each other.

11. The demodulation circuit according to claim 10,

wherein a reference potential is supplied to a node which is electrically connected to the source terminal of the second transistor, the one terminal of the second capacitor, the one terminal of the third capacitor, and the one terminal of the first resistor.

12. An RFID tag comprising the demodulation circuit according to claim 10.

FIG. 1A

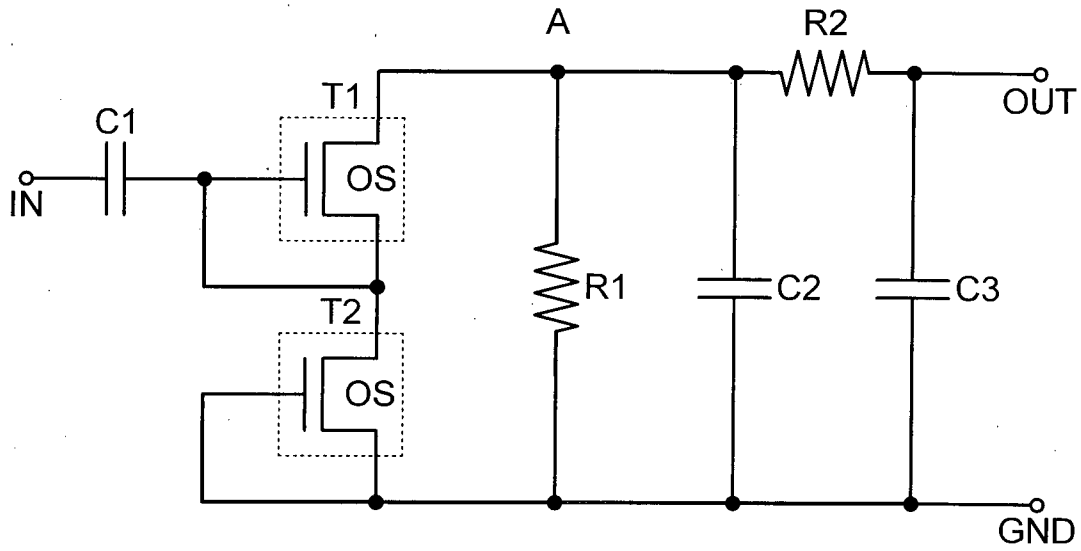

A
R2
T1
C1
OUT
IN
OS
R1
C2
C3
T2
OS
GND

FIG. 1B

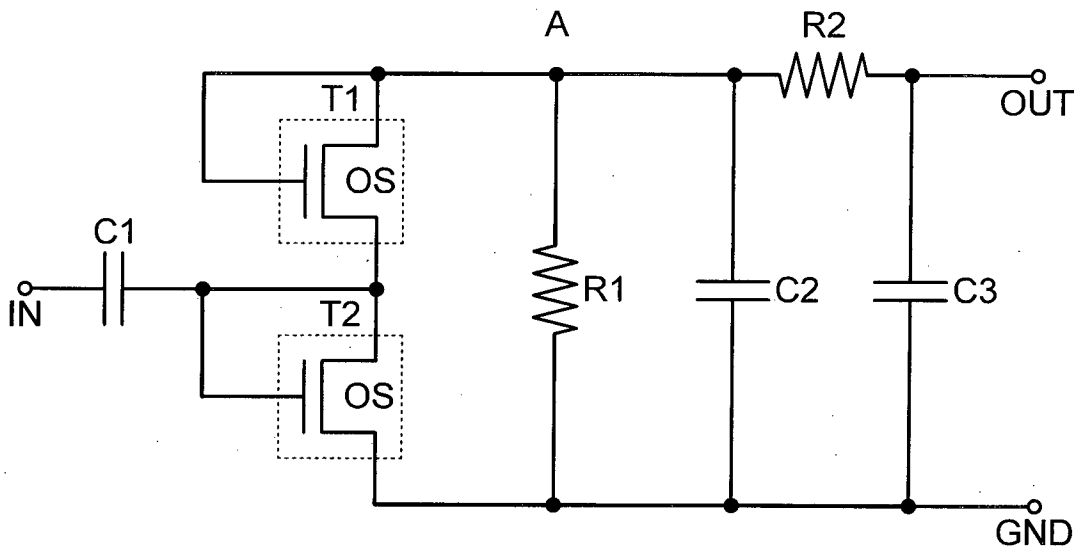

A
R2
T1
OUT
OS
C1
R1
C2
C3
IN
T2
OS
GND

FIG. 2A

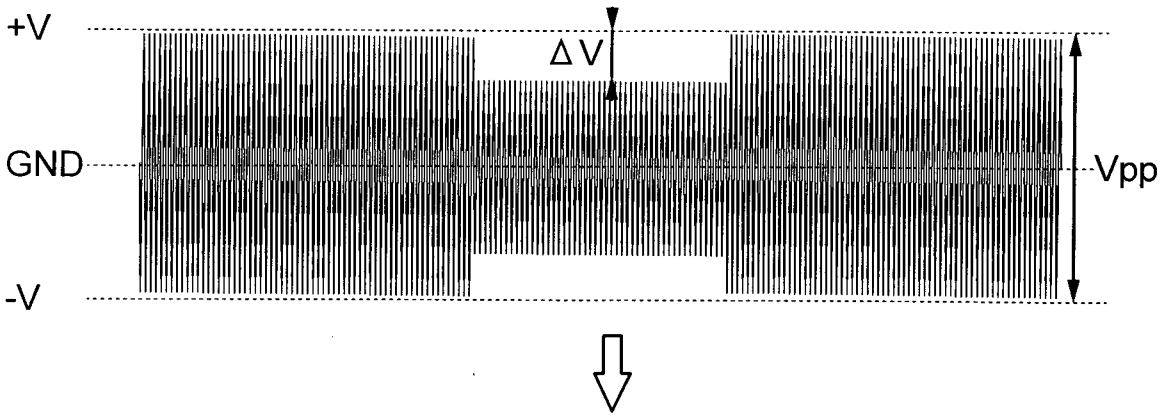


FIG. 2B

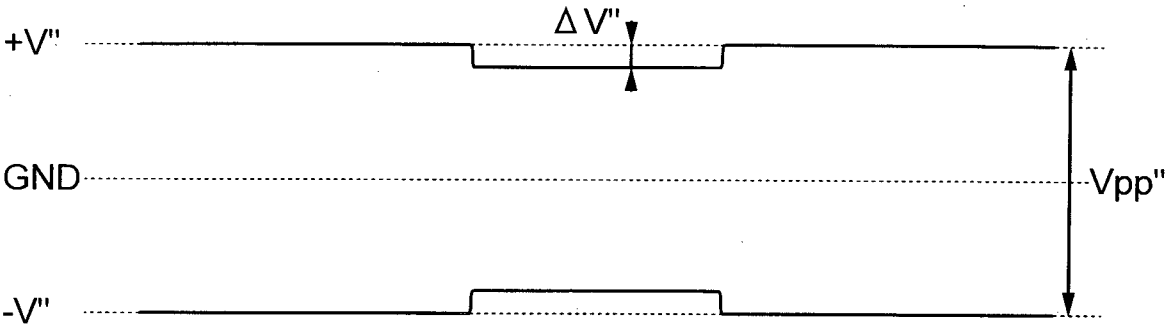


FIG. 2C

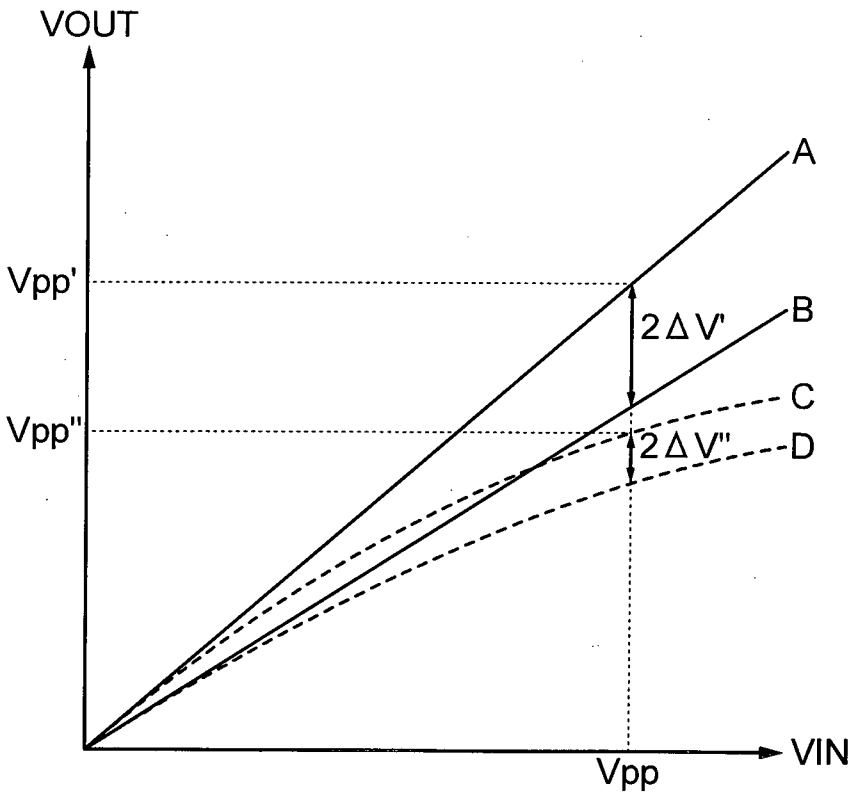


FIG. 3A

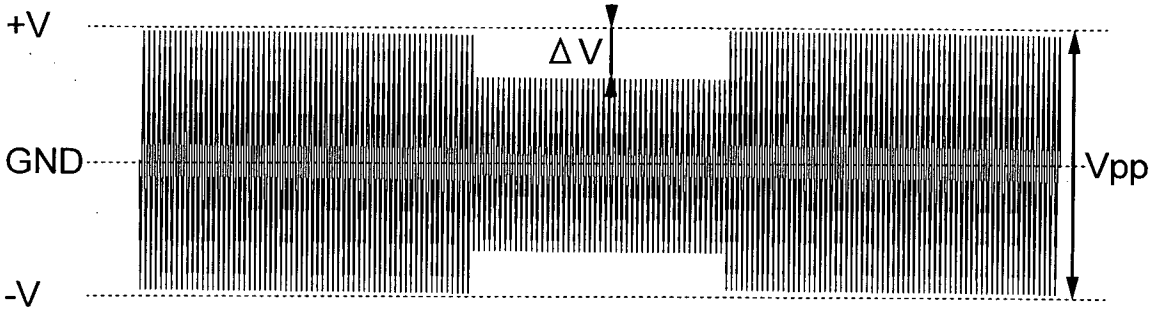


FIG. 3B

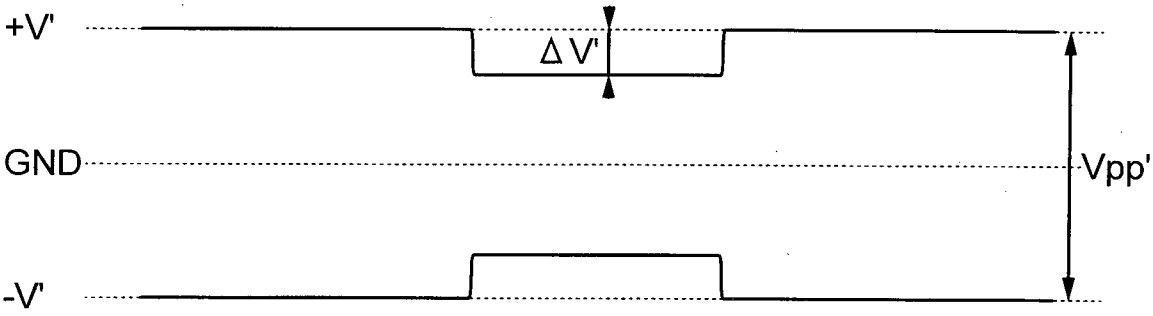
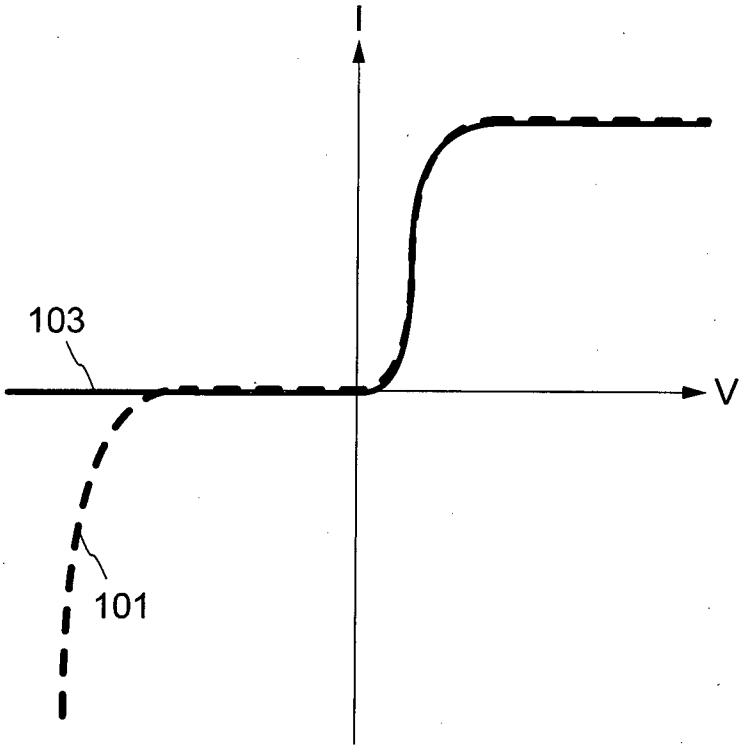


FIG. 3C



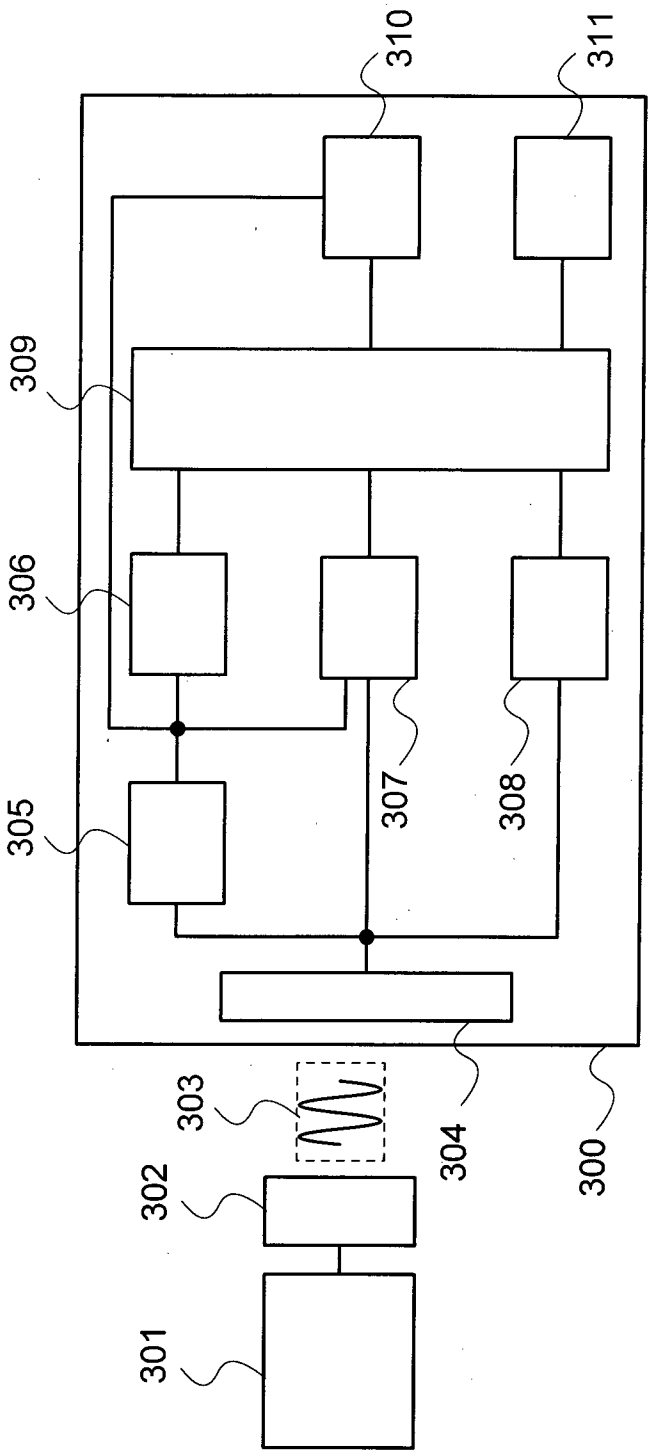


FIG. 4

FIG. 5A

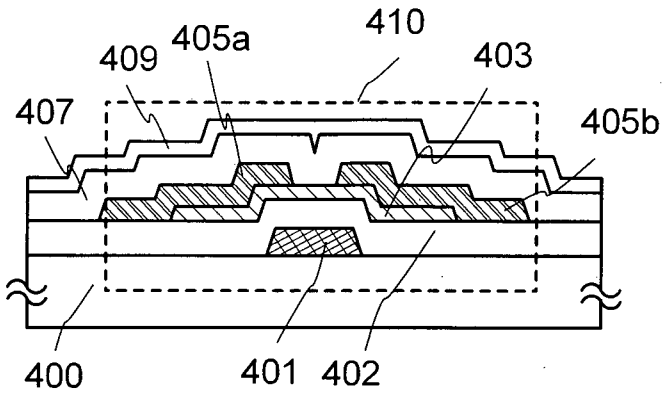


FIG. 5B

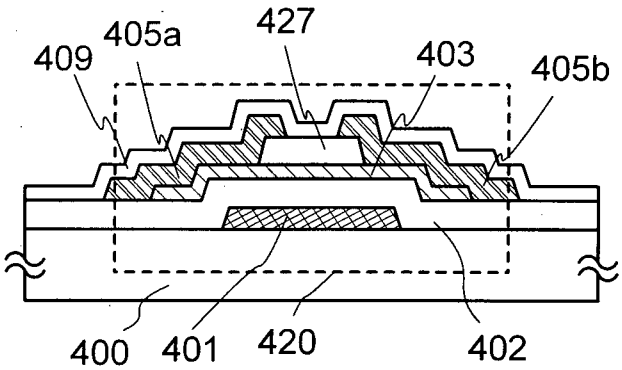


FIG. 5C

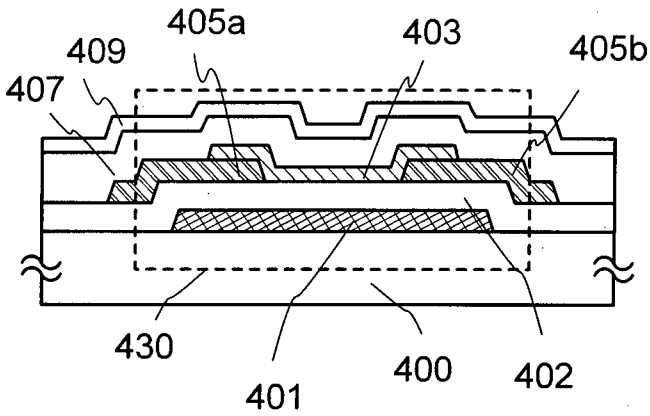


FIG. 5D

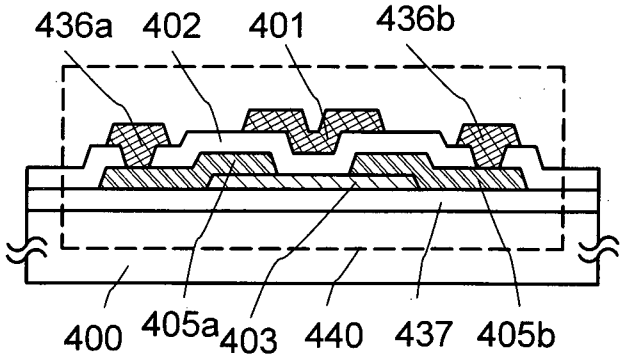


FIG. 6A

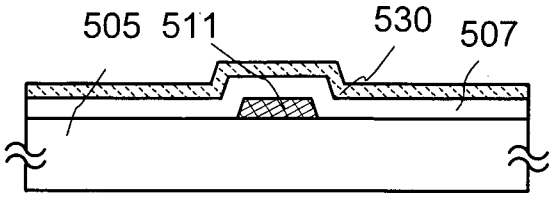


FIG. 6B

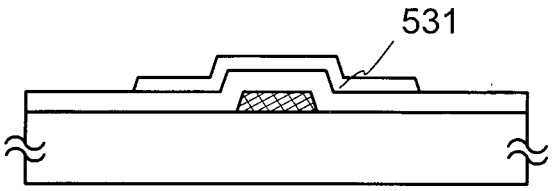


FIG. 6C

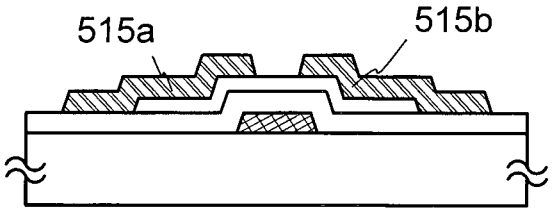


FIG. 6D

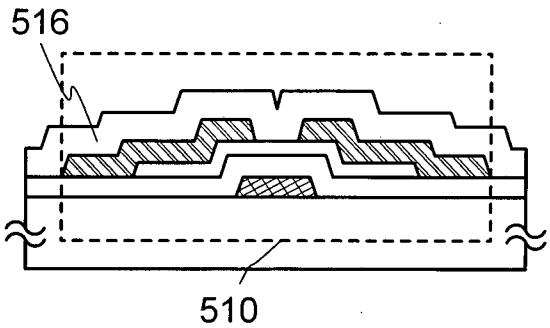
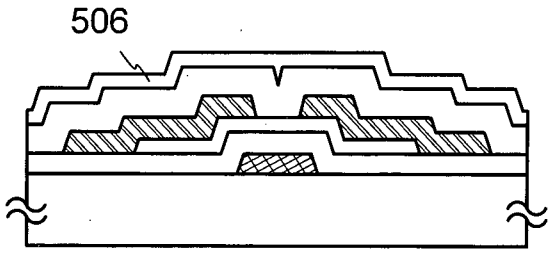


FIG. 6E



EXPLANATION OF REFERENCE

T1: first transistor, T2: second transistor, C1: first capacitor, C2: second capacitor, C3: third capacitor, R1: first resistor, R2: second resistor, 101: broken line, 103: solid line, 300: RFID tag, 301: communication device, 302: antenna, 303: radio signal, 304: antenna, 305: rectifier circuit, 306: constant voltage circuit, 307: demodulation circuit, 308: modulation circuit, 309: logic circuit, 310: memory circuit, 311: ROM, 400: substrate, 401: gate electrode layer, 402: gate insulating layer, 403: oxide semiconductor layer, 405a: source electrode layer, 405b: drain electrode layer, 407: insulating layer, 409: protective insulating layer, 410: transistor, 420: transistor, 427: insulating layer, 430: transistor, 436a: wiring layer, 436b: wiring layer, 437: insulating layer, 440: transistor, 505: substrate, 506: protective insulating layer, 507: gate insulating layer, 510: transistor, 511: gate electrode layer, 515a: source electrode layer, 515b: drain electrode layer, 516: insulating layer, 530: oxide semiconductor film, and 531: oxide semiconductor layer.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/051380

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H04L27/06(2006.01)i, G06K19/07(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H04L27/06, G06K19/07

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

IEEE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2001-266102 A (STMicroelectronics NV) 2001.09.28, figure 1, paragraphs [0001]to[0002], paragraphs [0006]to[0007] & EP 903689 A1 & FR 2768880 A	1-12
Y	JP 8-162257 A (Sumitomo Sitix Corporation) 1996.06.21, figure 1, paragraphs [0014] (No Family)	1-12
Y	JP 2007-220818 A (Kochi Industrial Promotion Center) 2007.08.30, figure 1, paragraphs [0029], claim 1 (No Family)	1-12
A	JP 10-13312 A (SONY CORPORATION) 1998.01.16, figure 2 & US 6126077 A & CN 1175043 A & CN 1495667 A	1-12

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20.04.2011	10.05.2011

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/051380

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2006-295319 A (Denso Corporation) 2006.10.26, abstract (No Family)	1-12
A	JP 11-215026 A (Toshiba Corporation) 1999.08.06, abstract (No Family)	1-12
A	JP 2009-302652 A (Toshiba Corporation) 2009.12.24, figure 2 & US 2009/0302935 A1 & CN 101605114 A	1-12
A	JP 2006-34085 A (Toshiba Corporation) 2006.02.02, abstract & US 2005/0282505 A1 & EP 1607900 A2 & DE 602005009284 D & CN 1722595 A	1-12
A	JP 2008-4791 A (SONY CORPORATION) 2008.01.10, claim 1 (No Family)	1-12