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(71) Applicant *(for all designated States except US)*: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, New York 10504 (US).

(71) Applicant *(for MG only)*: **IBM UNITED KINGDOM LIMITED** [GB/GB]; PO Box 41, Portsmouth Hampshire PO6 3AU (GB).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **MANDELMAN, Jack, Allan** [US/US]; 11 Claremont Drive, Flat Rock, North Carolina 28731 (US). **CHENG, Kangguo** [CN/US]; 35B Hudson View Drive, Beacon, New York 12508 (US). **HSU, Louis, Lu-Chen** [US/US]; 7 Crosby Court, Fishkill, New York 12524 (US). **YANG, Haining** [CN/US]; 36 Robinson Lane, Wappingers Falls, New York 12590 (US).

(74) Agent: **BURT, Roger, James**; IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Winchester Hampshire SO21 2JN (GB).

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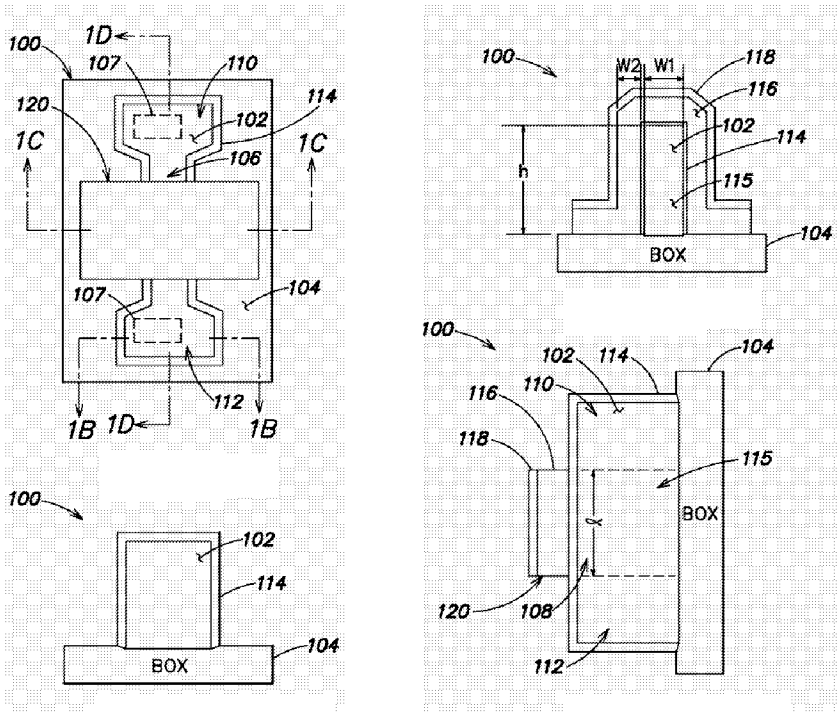


(57) Abstract: A method of manufacturing a finFET including the steps of (1) providing a substrate; and (2) forming at least one source/drain diffusion region of the finFET on the substrate. Each source/drain diffusion region includes (a) an interior region of unsilicided silicon; and (b) silicide formed on a top surface and sidewalls of the region of unsilicided silicon.

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# REDUCED-RESISTANCE FINFETS AND METHODS OF MANUFACTURING THE SAME

## FIELD OF THE INVENTION

The present invention relates generally to semiconductor device manufacturing, and more particularly to reduced-resistance finFETs and methods of manufacturing the same.

## BACKGROUND

A finFET is a transistor that includes a narrow fin (e.g., of silicon) with gate conductors either on two opposing sidewalls of the fin, or on two opposing sidewalls and the top surface of the fin. An overall resistance of the finFET is strongly determined by the area of an interface between a silicide layer and silicon in the source/drain regions of the finFET. Conventional finFETs may include a silicide formed on portions of a top surface of silicon in a source/drain region of the finFETs. However, such finFETs exhibit a high resistance, which is undesirable, because of the small area available at the top surface of the fin. Consequently, improved finFETs and methods of manufacturing the same are desired.

## SUMMARY OF THE INVENTION

In a first aspect of the invention, a first method of manufacturing a finFET is provided. The first method includes the steps of (1) providing a substrate; and (2) forming at least one source/drain diffusion region of the finFET on the substrate. Each source/drain diffusion region includes (a) an interior region of unsilicided silicon; and (b) silicide formed on a top surface and sidewalls of the region of unsilicided silicon.

In a second aspect of the invention, a first apparatus is provided. The first apparatus is a finFET that includes at least one source/drain diffusion region formed on a substrate. Each source/drain diffusion region includes (1) an interior region of unsilicided silicon; and (2) silicide formed on a top surface and sidewalls of the region of unsilicided silicon.

In a third aspect of the invention, a first system is provided. The first system is a substrate that includes a finFET having at least one source/drain diffusion region formed on the substrate. Each source/drain diffusion region includes (1) an interior region of unsilicided silicon; and (2) silicide formed on a top surface and

sidewalls of the region of unsilicided silicon. Numerous other aspects are provided in accordance with these and other aspects of the invention.

Other features and aspects of the present invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE FIGURES

FIGS. 1A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of a substrate following a step of a method of manufacturing a finFET in which a body region having source/drain diffusion regions and a gate region are formed in accordance with an embodiment of the present invention.

FIGS. 2A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which spacers are formed adjacent the body region and gate region in accordance with an embodiment of the present invention.

FIGS. 3A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which one or more portions of the spacers are removed from the substrate in accordance with an embodiment of the present invention.

FIGS. 4A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which porous silicon is formed in the source/drain diffusion regions in accordance with an embodiment of the present invention.

FIGS. 5A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which the substrate undergoes a second implant in accordance with an embodiment of the present invention.

FIGS. 6A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which the substrate undergoes a third implant in accordance with an embodiment of the present invention.

FIGS. 7A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which silicide is formed on the substrate in accordance with an embodiment of the present invention.

FIGS. 8A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which back-end-of-line (BEOL) processing is performed in accordance with an embodiment of the present invention.

FIG. 9 illustrates a process flow of the method of manufacturing the finFET in accordance with an embodiment of the present invention.

FIG. 10 illustrates sub-steps of a step in the process flow in which porous silicon is formed in source/drain diffusion regions in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

The present invention provides an improved fin MOSFET (FinFET) and methods of manufacturing the same. More specifically, the present invention provides a finFET with silicide formed on a top surface of and sidewalls of silicon in at least one source/drain diffusion region of the finFET and methods of manufacturing the same. In this manner, the source/drain diffusion region includes an interior unsilicided region (e.g., silicon) nearly surrounded by silicide. Therefore, an area of an interface of the silicide and silicon in the finFET source/drain diffusion region is increased compared to conventional finFETs. Consequently, a resistance of the finFET manufactured in accordance with an embodiment of the present invention may be reduced compared to conventional finFETs.

To form the silicide around portions of silicon in the source/drain diffusion region as described above, portions of silicon in the source/drain diffusion region may be converted to porous silicon. Thereafter, a layer of metal may be deposited on the substrate. Silicidation may be employed to cause the metal to react with silicon of the substrate such that silicide is formed around portions of silicon in the source/drain diffusion region as described above. In this manner, the present invention provides an improved finFET and methods of manufacturing the same.

FIGS. 1A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of a substrate following a step of a method of manufacturing a

finFET in which a body region having source/drain diffusion regions and a gate region are formed in accordance with an embodiment of the present invention. With reference to FIGS. 1A-D, a substrate 100 may be provided. The substrate 100 may include a silicon-on-insulator (SOI) layer. Alternatively, the substrate 100 may include a bulk substrate layer. Although a method of manufacturing a finFET with a reduced source-drain resistance is described below with reference to an SOI substrate, the present invention includes methods of manufacturing a finFET with a reduced source-drain resistance on a bulk substrate. Such methods may employ different isolation techniques.

The substrate 100 may include a layer of silicon 102 (e.g., single crystal silicon) formed on a layer of oxide (e.g., buried oxide) 104. RIE or another suitable method may be employed to remove portions of the silicon layer 102 such that a body region 106 may be formed. The body region 106 may include at least one source/drain diffusion region and define a gate channel region 108. Further, the body region 106 may include one or more source/drain contact regions 107. For example, the body region 106 may include a first source/drain diffusion region 110 and a second source/drain diffusion region 112. Chemical vapor deposition (CVD) or another suitable method may be employed to form a layer of dielectric material 114 and/or another suitable material around the body region 106. As shown, the body region 106 may be a "dog bone"-shaped silicon island (although the body region may have a different shape). In this manner, the body region 106 may provide an increased contact area and/or an area within the source/drain diffusion region 110, 112 normal to the direction of the current density. The source-drain current density is predominantly determined by the majority carrier flux. The majority carrier flux refers to charge carriers (electrons or holes) normal to the interface between the source/drain diffusion and the silicide. In an NFET the source/drain diffusions are heavily N-type doped and the majority carrier flux comprises electrons. In a PFET the source/drain diffusions are heavily P-type doped and the majority carriers are holes. A portion 115 of the body region 106 between the first and second source/drain diffusion regions 110-112 may serve as a silicon fin of the finFET being manufactured. The fin may have a height h of about 50 nm to about 500 nm and a width w1 of about 5 nm to about 100 nm (although a larger or smaller and/or different height range may be employed). In this manner, the fin may be design to be narrow enough to enable fully-depleted body operation which may result in volume inversion, high carrier mobility and/or increased control of electric potential in the body region 106.

Consequently, the finFET being manufactured may provide an "on"/"off" current ratio that is superior to a planar MOSFET.

CVD or another suitable method may be employed to deposit a layer of polysilicon material 116 or another suitable material on the substrate 100, and a layer of nitride 118 or another suitable material thereon. RIE or another suitable method may be employed to remove portions of the polysilicon material layer 116 and nitride layer 118 such that the polysilicon material layer 116 and nitride layer 118 are formed on a portion of the body region 106 between source/drain diffusion regions 110-112 thereof. The polysilicon material layer 116 and dielectric layer 114 may serve as a gate 120 (e.g., gate region or stack) of finFET being manufactured. More specifically, the polysilicon material layer 116 may serve as a gate conductor layer. Further, the nitride layer 118 may serve as a gate capping layer. Consequently, the gate 120 may be formed around multiple (e.g., three) sides of the body region 106. For example, a three-sided gate 120 may be formed on portions of opposing approximately vertical sidewalls and a portion of a top surface of the body region 106. The gate 120 may have a length l of about 18 nm to about 130 nm (although a larger or smaller and/or different length range may be employed). The length l of the gate 120 may determine the length of a channel formed in the finFET.

FIGS. 1A-8D are not drawn to scale. For example, for illustrative purposes a width w1 of the fin and a width w2 of the gate conductor layer are intentionally enlarged. However, in an actual finFET device both the width w1, w2 of the gate conductor and the fin are significantly narrower than that shown in these drawings.

FIGS. 2A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which spacers are formed adjacent the body region and gate region in accordance with an embodiment of the present invention. With reference to FIGS. 2A-D, CVD or another suitable method may be employed to form a layer of silicon nitride or another suitable material on the substrate 100. RIE or another suitable method may be employed to remove portions of the silicon nitride layer such that spacers 200 are formed adjacent sidewalls of the body region 106 and the gate 120. The spacers 200 may be about 10 nm to about 100 nm wide (although a larger or smaller and/or different width range may be employed). During RIE to form the spacers 200, portions of the dielectric material layer 114 may be removed. For example, portions of the dielectric material layer 114 on a

top surface of source/drain diffusion regions 110-112 of the body region 106 may be removed.

The spacers 200 may serve as sacrificial or temporary spacers employed to protect portions of the gate conductor layer 116 during subsequent processing. In this manner, a spacer width may be employed such that subsequently-formed silicide may be prevented from penetrating into a junction of the finFET as described below. Penetration of the silicide into the junction regions of the source/drain diffusion regions may result in severe leakage currents and must be avoided.

FIGS. 3A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which one or more portions of the spacers are removed from the substrate in accordance with an embodiment of the present invention. With reference to FIGS. 3A-D, a spin-on technique or another suitable method may be employed to deposit a photoresist layer or another suitable material layer on the substrate 100. The photoresist layer may be patterned with a mask such that portions of the photoresist layer may be removed during a subsequent process (e.g., developing). In this manner a trim mask 300 may be formed. Although the trim mask 300 described above comprises photoresist, in some embodiments, the trim mask may comprise a hard mask material. Dotted boxes 302, 304 illustrate portions of the substrate 100 that may be exposed by the trim mask 300 during subsequent processing. For example, the trim mask 300 may be employed during RIE or another suitable method to remove portions of the spacers 200 and/or the dielectric material layer 114 adjacent source/drain diffusion regions 110-112 of the body region 106. In this manner, a larger area of the source/ drain diffusion regions 110-112 (e.g., including sidewalls thereof) may be exposed during subsequent processing, thereby improving contact to the source/drain diffusion regions thereof.

FIGS. 4A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which porous silicon 400 is formed in the source/drain diffusion regions 110-112 in accordance with an embodiment of the present invention. With reference to FIGS. 4A-D, impurity atoms (e.g., dopant) may be introduced into exposed portions of the substrate 100. For example, exposed portions of the substrate 100, such as source/drain diffusion regions 110-112, may be doped to form a p+ impurity species layer (which is later converted to porous silicon 400), such as boron or the like. The p+ doped layer may have a peak concentration of

about 5 x $10^{17}$ $cm^{-3}$ to about 1 x $10^{21}$ $cm^{-3}$ (although a larger or smaller and/or different concentration range may be employed). The thickness of the p+ doped layer preferably ranges from 5 nm to 100 nm (although a larger or smaller thickness may be employed). The P+ doped layer is preferably formed by plasma immersion implantation. Alternatively, solid source doping, gas phase doping, or angled ion implantation processes, or combinations thereof, may be employed to form the p+ doped layer. In some embodiments, a thin layer of CVD nitride or another suitable material may be employed as a mask to block doping of portions of the substrate 100.

An anodization process may be employed to convert the doped (e.g., p+ doped) silicon to porous silicon. For example, contactless anodization such as that described in "A technique to form a porous silicon layer with no backside contact by alternating current electrochemical process," A. El-Bahar, Y. Nemirovsky, *Applied Physics Letters, v* 77, n 2, Jul 10, 2000, p 208-210 may be employed to form porous silicon in an SOI layer, which is electrically insulated from a contacted substrate. During such anodization, an AC voltage excitation may be applied to the substrate 100, with the insulated silicon layer 102 being capacitively coupled to the substrate 100. A reaction that forms the porous silicon 400 in the source/drain diffusion regions 110-112 may occur while an AC anode, which may be positive relative to the cathode, is excited. A fluoride-containing acidic electrolyte solution or the like may be employed for etching (e.g., anodic etching) during anodization. In this manner, a contactless anodization method (e.g., a method which may not require direct electrical contact with the substrate 100) may be employed to form porous silicon 400 as described above. In some embodiments, an excitation frequency of between about 500 Hz and about 10 kHz, an RMS current density of about_5 $mA/cm^2$ to about 200$mA/cm^2$, and silicon regions having a p+ doping concentration of greater than about $10^{19}/cm^3$ may be may be employed to form the porous silicon 400 (although a larger or smaller and/or different range may be employed for the excitation frequency, current density and/or doping concentration). In this manner, pores (e.g., canals) having a diameter of about 1 nm to about 100 nm may be formed. A density of such pores ranges from about $10^9$ pores/$cm^2$ to about $10^{15}$ pores/$cm^2$. However, a larger or smaller and/or different diameter and/or density range may be employed. Consequently, pores of the porous silicon 400 may occupy about 30% to about 80% of an overall volume of the silicon 400 (although the pores may occupy a larger or smaller and/or different percentage range of the overall volume).

A stripper bath or another suitable method may be employed to remove the trim mask 300 from the substrate 100. Further, the substrate

100 may undergo annealing to remove excess dopant from the porous silicon 400. For example, the substrate 100 may undergo a hydrogen-ambient bake after the porous silicon 400 is formed such that some or all of the p+ dopant remaining in the source/drain diffusion regions 110-112 may be removed. During the hydrogen-ambient bake, the substrate 100 may be subjected to a temperature of about 850 °C to about 1100 °C for about 10 seconds to about 30 minutes (although a larger or smaller and/or different temperature range and/or time period may be employed).

FIGS. 5A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which the substrate undergoes a second implant in accordance with an embodiment of the present invention. With reference to FIGS. 5A-D, RIE or another suitable method may be employed to remove portions (e.g., remaining portions) of the spacers 200. Additionally, isotropic etching or another suitable method may be employed to remove exposed portions of the nitride layer 118 and/or the dielectric layer 114 from the substrate 100. In this manner, portions of the spacers 200 and/or the nitride layer 118 remaining while the porous silicon 400 is formed served to protect the gate 120 (e.g., polysilicon material layer 116 and dielectric layer 114) while forming the porous silicon 400. Further, the spacers 200 served to position an edge (e.g., sidewall) of the porous silicon 400 a predetermined distance d (e.g., based on the width of the spacers 200) from the gate 120. In this manner, a leakage current between such regions may be reduced and/or prevented. For example, a spiking through of a source/drain metal into a gate channel of the finFET may be reduced and/or eliminated. Consequently, the width of the spacer 200 may be employed such that subsequently-formed silicide may be prevented from penetrating into a gate-source/drain junction.

The substrate 100 may be subjected to angled ion implantations (Ldd I/I), such that lightly-doped source/drain diffusion (LDD) regions are formed within the N-channel and P-channel finFETs. For example, in accordance with standard MOSFET technology, a concentration of about 1 x $10^{18}$ $cm^{-3}$ to about 5 x $10^{19}$ $cm^{-3}$ may be employed for the LDD regions (although a larger or smaller and/or different concentration range may be employed). Standardly practiced LDD dopants such as arsenic, phosphorus or antimony N-type dopant species may be used for the N-channel finFETs, and boron or indium P-type species for the P-channel finFETs. In this manner, the substrate 100 may be lightly doped. More specifically, a region 500 of relatively low doping close to the gate 120 may be formed in the source/drain diffusion regions 110, 112.

FIGS. 6A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which the substrate undergoes a third implant in accordance with an embodiment of the present invention. With reference to FIGS. 6A-D, CVD or another suitable method followed by RIE or another suitable method may be employed to form spacers 600 (e.g., permanent spacers) on sidewalls of the gate 120 and sidewalls of the body region 106 including the source/drain diffusion regions 110, 112. The width of the spacers 600 may be less than the previously-formed spacers 200. For example, the spacers 600 may be about 5 nm to about 50 nm wide (although a larger or smaller and/or different width range may be employed).

The substrate 100 may be subjected to implantation, such as a source/drain ion implant (S/D I/I) or the like, such that junctions (e.g., of the source/drain diffusion regions 110, 112) of the finFET being manufactured may be formed. For example, a concentration of about 1 x $10^{9}$ $cm^{-3}$ to about 5x$10^{20}$ $cm^{-3}$ of dopant may be introduced into the substrate 100 (although a larger or smaller and/or different concentration range and/or dopant type may be employed). In this, manner, the substrate 100 may be heavily doped with impurity atoms. For example, an angled source-drain ion implant S/D I/I may be performed through the porous silicon 400 to form a doped (e.g., heavily doped silicon) region underneath the porous silicon 400. Further, a gate conductor work function of the finFET being manufactured may be based on such doping. In this manner, a gate 120 has a work function which generally matches (e.g., is approximately equal to) the work function of the adjacent source-drain diffusions.

The second implant (e.g., light doping of the source/drain diffusion regions 110, 112) and the third implant (e.g., heavy doping of the source/drain diffusion regions 110, 112) are performed after porous silicon 400 is formed in the source/drain diffusion regions 110, 112. Therefore, dopants inserted into the substrate 100 during the second and third implants may penetrate through the porous layer 400 and form a junction. It should be noted the spacers 200 may cause the porous silicon 400 to be formed a predetermined distance (e.g., based on a width of the spacer 200) from a source-drain junction near the gate 120. Such distance may prevent silicide subsequently formed in the porous silicon 400 from encroaching (e.g., laterally) on such junction.

Implantation of impurity atoms through the porous silicon 400 during the third implant enables formation of heavy source-drain doping much deeper than the porous silicon 400 after the substrate 100 undergoes annealing. As described below, the porous silicon 400 may eventually be

converted to a highly-conductive metallic silicide. Such silicide should not encroach (e.g., penetrate or spike through) the junctions. To reduce and/or eliminate such penetration (e.g., lateral penetration), spacer 200 is wider than the spacer 600, which may be employed to separate the lightly-doped and heavily-doped implants of the source/drain diffusion regions 110, 112. In this manner, substantially thick silicide subsequently may be formed inside the porous silicon 400 upon the source/drain diffusion regions 110, 112 but away from the edge of gate 120 so that a series resistance can be significantly reduced. However, closer to the gate 120 (e.g., along the edges of the polysilicon material layer 116 serving as the gate conductor) only a very shallow surface layer of the source/drain diffusion regions 110, 112 subsequently may be converted into silicide. Therefore, neither lateral nor vertical metal spiking will occur using the present method.

Thereafter, the substrate 100 may undergo annealing or another suitable process. For example, following the light and heavy doping of the source/drain diffusion regions 110, 112 (among other regions), the substrate 100 may be subjected to a dopant activation anneal, such as a rapid thermal anneal (RTA) or spike anneal at a temperature between about 950 °C and about 1150 °C for about 5 seconds to about 30 seconds (although a larger or smaller and/or different temperature and/or time period range may be employed). Further, a different type of annealing may be employed.

FIGS. 7A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which silicide is formed on the substrate in accordance with an embodiment of the present invention. With reference to FIGS. 7A-D, CVD or another suitable method may be employed to form a layer of metal, such as tungsten, cobalt, titanium, nickel and/or the like, on the substrate 100.

Thereafter, the substrate 100 undergoes silicidation. Silicidation of different regions of the substrate 100 may lower series resistance and enable better current drivability of the finFET. During silicidation, the metal may react with different portions of silicon on the substrate 100 such that silicide forms therein. For example, the porous silicon 400 may be silicided. More specifically, metal may be soaked into pores of the porous silicon 400. Silicidation may proceed more rapidly through the porous silicon 400 than through remaining portions of silicon in the source/drain diffusion regions 110, 112 and on remaining portions of the substrate 100. Consequently, a time period for

silicidation of the porous silicon 400 and/or remaining portions of the finFET may be reduced.

Further, a depth of a silicide layer 700 formed on the substrate 100 may be precisely controlled. More specifically, silicon in the entire source/drain diffusion regions 110, 112 may not be converted to silicide. Consequently, the present method may form an interior unsilicided silicon region 702 (e.g., an unsilicied silicon "core") within the source/drain diffusion regions 110, 112. Thus, an area of an interface 704 of the silicide layer 700 and unsilicided silicon region 702 is increased compared to a transistor having silicide formed only on a top surface of source/drain diffusion regions of the transistor and compared to a transistor having silicide formed in the entire source/drain diffusion region of the transistor. A resistance (e.g., a source-drain resistance) of a finFET may be based on (e.g., inversely proportional to) the area of such interface. Consequently, the unsilicided silicon "core" 702 formed by the present invention may reduce a series resistance of the finFET being manufactured. Further, the finFET may employ the unsilicided silicon "core" 702 to avoid reducing an area normal to the direction of the current density crossing the silicide/unsilicided silicon interface in source/drain diffusion regions 110, 112 of the finFET.

Process parameters employed while forming the porous silicon 400 may determine thicknesses of respective portions of the porous silicon 400. A thickness of the subsequently-formed silicide may be based on the porous silicon layer thickness. Therefore, the present invention may be employed to form a silicide layer 700 (as described above) portions of which may be thinner than a conventional silicide layer. In this manner, the present invention may be employed in finFETs with shallow junctions.

The silicide layer 700 formed in a source/drain diffusion region 110, 112 may have a first portion 706 having a thickness t1 of about 1 nm to about 5 nm (although a larger or smaller and/or different thickness range may be employed). Such portion 706 may serve as a contact (e.g., a thin contact) to the LDD silicon. Additionally, the silicide layer 700 formed in the source/drain diffusion region 110, 112 may have a second portion 708 having a thickness t2 of about 5 nm to about 100 nm (although a larger or smaller and/or different thickness range may be employed). Such portion 708 may serve as a contact (e.g., a thicker contact) to a top surface of silicon in the source/drain diffusion region 110, 112. Further, the silicide layer 700 formed in the source/drain diffusion region 110, 112 may have a third portion 710 having a width w1 of about 5 nm to about 100 nm (although a larger or smaller and/or different width range may be employed). Such portion 710 may serve as a

contact to sidewalls of silicon in the source/drain diffusion region 110, 112. Consequently, the silicide layer 700 may form or define a region of silicon in the interior of the source/drain diffusion region 110, 112 (e.g., the unsilicided silicon "core" 702). Although a specific shape is described above for the silicide layer 700 in the source/drain diffusion regions 110, 112, the silicide layer 700 in the source/drain diffusion regions 110, 112 may have any shape adapted to increase an area of the interface 704 of the silicide layer 700 and silicon in the source/drain diffusion region 110, 112 of the finFET being manufactured. The silicide may have a resistivity of about 10 micro-ohm-cm to about 100 micro-ohm-cm (although a larger or smaller and/or different resistivity range may be employed).

Thereafter, RIE or another suitable method may be employed to remove unreacted metal from the substrate 100. Such RIE may be selective to silicide.

FIGS. 8A-D are block diagrams of respective top, first cross-sectional front, second cross-sectional front and cross-sectional side views of the substrate following a step of the method of manufacturing a finFET in which back-end-of-line (BEOL) processing is performed in accordance with an embodiment of the present invention. With reference to FIGS. 8A-D, CVD or another suitable method may be employed to deposit an insulator layer 800, such as a planarizing glass (e.g., undoped TEOS, phosphosilicate glass (PSG), borosilicate glass (BSG), borophosphosilicate glass (BPSG) and/or the like) on a top surface of the substrate 100. Thereafter, the insulator layer 800 may be planarized. In some embodiments, the insulator may be reflowed to planarize the insulator layer 800. Alternatively, chemical mechanical polishing (CMP) or another suitable method may be employed to planarize the insulator layer 800. RIE or another suitable method may be employed to form one or more vias or contact openings 802 on the substrate 100. CVD or another suitable method followed by RIE, CMP or another suitable method may be employed to fill such vias 802 with a conductor, such as tungsten or another suitable material, thereby forming studs 804. Additionally, one or more levels of wiring and/or interlevel dielectric may be formed on the substrate 100. In this manner, an improved finFET 806 may be formed. The finFET 806 has a reduced source-drain resistance compared to conventional transistors. The finFET 806 includes at least one source/drain diffusion region 110, 112 having silicide (e.g., a low-resistivity silicide) formed on a top surface of and on sidewalls of silicon (e.g., heavily-doped unsilicided silicon) in the source/drain diffusion regions 110, 112. For example, a source/drain diffusion region 110, 112 of the finFET 806 may include a

silicide layer 700 having a thin silicide region (e.g., the first portion 706) located in the vicinity of a gate channel region 808 of the finFET 806, a thicker silicide region (e.g., the second portion 708) located in a distance away from the gate channel region 808, sidewall silicide regions (e.g., the third portion 710) which may be coupled to and/or included in outer edges of the source/drain diffusion region 110, 112 and an unsilicided silicon region 702 in the interior of the source/drain diffusion region 110, 112.

FIG. 9 illustrates a process flow 900 of the method of manufacturing the finFET in accordance with an embodiment of the present invention. With reference to FIG. 9, during the method of manufacturing the finFET 806, in step 902, the gate region 120 may be protected (e.g., by the trim mask 300) and the source/drain diffusion regions 110, 112 may be exposed (e.g., by the trim mask 300) while the porous silicon 400 is formed in portions of the source/drain diffusion regions 110, 112. In this manner, pores may be prevented from forming in the gate conductor material layer 116, and the gate dielectric 114 is protected from damage due to the etching action of the electrolyte used to form pores in the exposed silicon. Consequently, subsequent doping and/or silicidation of the gate region 120 may be controlled. Therefore, the gate region 120 may not be doped more than desired, thereby avoiding a problem of removing a dopant, such as boron, from grain boundaries of the gate conductor material. Further, a larger portion (depth) than that desired of the gate region 120 may not be silicided, which would adversely affect a work function at an edge of the gate region 120 (e.g., for a short channel device) and threshold voltage of the finFET 806.

In step 904, porosity (e.g., porous silicon 400) may be formed in selected areas of the source/drain diffusion regions 110, 112. Details of step 904 are described below with reference to FIG. 10. After the porous silicon 400 is formed, implant and annealing process steps may be employed to form the source/drain diffusion regions 110, 112 of the finFET 806. For example, in step 906, dopant may be implanted into the substrate 100. For example, the LDD I/I and the S/D I/I may be employed to dope the gate region 120 and form junctions in the source/drain diffusion regions 110, 112. In step 908, silicidation may be employed to form the silicide layer 700 on the substrate 100 (e.g., on the gate region 120 and on the porous silicon 400 of the source/drain diffusion regions 110, 112). The silicide layer 700 may be formed inside the porous silicon 400 as well as at exposed surfaces of single-crystal silicon and polysilicon on the substrate 100. Thereafter, step 910 may be performed. In step 910, BEOL processing may continue. For example, the insulator layer 800, vias or

contact openings 802, studs 804, interlevel dielectrics, wiring levels and/or the like may be formed such that contact may be made to the finFET 806. In this manner, the low source-drain resistance finFET 806 may be formed.

FIG. 10 illustrates sub-steps 1000 of a step in the process flow 900 in which porous silicon is formed in source/drain diffusion regions in accordance with an embodiment of the present invention. With reference to FIG. 10, to perform step 904, in step 1002, dummy spacers such as the sacrificial or temporary spacers 200 may be formed on the substrate 100. The temporary spacers 200 may be formed adjacent the gate region 120 and body region 106 of the substrate 100. In step 1004, portions of the temporary spacers 200 adjacent source/drain diffusion regions 110, 112 of the body region 106 may be removed using isotropic etching or the like. Such portions may be exposed during etching by the trim mask 300. Trimming away portions of the spacers 200 around the outer edges of the source/drain diffusion regions 110, 112 allows such areas to be completely converted to porous silicon 400. In step 1006, dopant (e.g., p+ dopant such as boron and/or the like) may be introduced into exposed portions of the substrate 100. Plasma immersion implantation, ion implantation (e.g., angled), gas phase doping, a solid source doping technique or conventional gaseous source diffusion process may be employed to dope the exposed portions of the substrate 100. In this manner, the source/drain diffusion regions 110, 112 may be doped after porous silicon 400 is formed.

Thereafter, in step 1008, the substrate 100 may undergo anodization such that pores form inside the p+ doped regions of the source/drain diffusion regions 110, 112. In step 1010, remaining portions of the temporary spacers 200 may be stripped from the substrate 100. RIE or another suitable method may be employed. Further, in step 1012, the substrate 100 may undergo annealing to remove excessive dopant therefrom. For example, the substrate 100 may be subjected to a hydrogen bake (e.g., a low temperature bake in a hydrogen ambient) such that excess p+ dopant inserted in the substrate 100 during step 1006 may be removed (e.g., depleted by the bake). Through use of the present method, a finFET 806 with a unique and robust source-drain contacting scheme may be formed.

Conventional methods and apparatus for semiconductor device manufacturing pose problems. For example, when scaling CMOS technology below the 45nm node, processes associated with the formation of a gate electrode, including the gate stack and dielectric, the channel and the source/drain regions all have to be significantly modified from earlier technology generations. Effective mitigation of short channel effects

requires ever shallower junction depths. Additionally, SOI film thickness and finFET fin width also must be reduced for short channel scalability. Unless raised source/drain structures are implemented, a thinner silicide is required to cope with the shallower junctions and thinner materials. Silicidation of source-drain diffusions is required to lower series resistance for better current drivability. However, consumption of silicon under silicide leads to increased contact resistance due to dopant depletion effects. Increased source-drain doping concentration may be employed to attempt to resolve this problem. However, high doping concentration may not easily be obtained due to limitations of solid solubility and electrical activation. Furthermore, a significant fraction of the source-drain series resistance is due to the interface between the silicide layer and the silicon. This leads to sharply increased series resistance when silicide is formed completely through the source-drain silicon because a channel current is forced to flow through a small cross-sectional area dictated by the thickness of the SOI film or by the width of the FinFET fin.

Therefore, a portion of the silicon normal to the surface of the source-drain diffusion should remain unsilicided. However, it is a great challenge to reduce contact resistance between a thin silicide layer and shallow source/drain. The problem is further complicated when contacting the source-drain diffusions of conventional finFETs because sidewalls of the source-drain regions of such finFETs are covered by the spacers as a consequence of the gate processing. Therefore, silicidation of such finFET source-drain diffusions is limited to the horizontally oriented surfaces, and not the sidewalls. This results in greatly compromised source-drain resistance and degraded performance of the conventional device.

The present methods and apparatus may provide advantages over conventional finFETs and avoid the disadvantages of conventional finFETs described above. For example, by forming the sacrificial spacer 200 before forming the porous silicon 400, the subsequently-formed silicide layer 700 may be prevented from encroaching on metallurgical junctions. In this manner, the finFET 806 may avoid the high leakage currents of conventional finFETs by maintaining a low-junction leakage current. Further, a gate electrode of the finFET 806 may be protected while forming porous silicon 400 in the source/drain diffusion region 110, 112 so the finFET gate 120 has a preferred work-function.

In a conventional finFET, a source and drain region may contribute a high series resistance to the finFET. As the aspect ratio (fin height/width) of the body of such conventional finFET increases, a

contact resistance problem increases. More specifically, because the sidewalls of the source/drain diffusion regions of such finFETs are often blocked by spacer material associated with gate formation, doping and silicidation occurs only on portions of a top surface of the source/drain diffusion regions. Further, a contact region on a top surface of the source/drain diffusion area is narrow, resulting in high contact resistance.

In contrast, by converting at least a portion of silicon in the source/drain diffusion regions 110, 112 into porous silicon 400, subsequently-formed silicide of the present invention may have a larger contact surface area than the planar surface area of the source/drain diffusion region 110, 112. Further, an interior of the source/drain diffusion region may remain unsilicided to increase an area of a silicide/non-silicide interface. More specifically, the silicide layer 700 may form on four sides (e.g., on three sidewalls and a top surface) of the source/drain diffusion region 110, 112 thereby reducing a contact resistance to the finFET 806. For the above reasons, compared to conventional transistors, the finFET 806 has a reduced source-drain series resistance.

Further, a source/drain ion implant is performed on the substrate 100 after forming the porous silicon 400 so that after drive-in of dopant a junction is always formed beneath the layer of porous silicon 400. Thereafter, the entire region of porous silicon 400 may be converted to silicide. Because the silicide forms mainly inside the region of porous silicon 400, dopant depletion problems are reduced and/or eliminated.

The foregoing description discloses only exemplary embodiments of the invention. Modifications of the above disclosed apparatus and methods which fall within the scope of the invention will be readily apparent to those of ordinary skill in the art. For instance, although the second implant described above is an LDD I/I, alternatively or additionally, the substrate 100 may be subjected to a halo implants or the like. For example, a concentration of about 5 x $10^{17}$ $cm^{-3}$ to about 5x$10^{18}$ $cm^{-3}$ may be employed of dopant polarity opposite of the source-drain doping polarity may be implanted into the substrate 100 (although a larger or smaller and/or different concentration range and/or dopant type may be employed). The halo implant may be employed to adjust a threshold voltage of the finFET 806 being manufactured.

## CLAIMS

1. A method of manufacturing a finFET, comprising:
providing a substrate; and
forming at least one source/drain diffusion region of the finFET on the substrate;
wherein each source/drain diffusion region includes:
an interior region of unsilicided silicon; and
silicide formed on a top surface and sidewalls of the region of unsilicided silicon.

2. The method of claim 1 wherein forming at least one source/drain diffusion region of the finFET on the substrate includes increasing a surface area of a silicon-silicide interface in the source/drain diffusion region.

3. The method of claim 1 wherein forming at least one source/drain diffusion region on the substrate includes:
forming a region of silicon on the substrate; and
converting one or more portions of the silicon in the region to porous silicon.

4. The method of claim 3 wherein converting one or more portions of the silicon in the region to porous silicon includes employing a contactless anodization process to convert one or more portions of the silicon in the region to porous silicon.

5. The method of claim 4 wherein converting one or more portions of the silicon in the region to porous silicon further includes removing portions of a previously-implanted dopant from the substrate using annealing.

6. The method of claim 4 further comprising employing a spacer to separate the porous silicon from a gate region of the finFET by a predetermined distance.

7. The method of claim 3 wherein forming at least one source/drain diffusion region on the substrate further includes:
depositing a layer of metal on the substrate; and
causing the metal to react with at least the porous silicon such that silicide is formed on a top surface and sidewalls of the region of silicon.

8. The method of claim 1 further comprising forming a gate having a predetermined work function on the substrate.

9. A finFET, comprising:
at least one source/drain diffusion region formed on a substrate;
wherein each source/drain diffusion region includes:
an interior region of unsilicided silicon; and
silicide formed on a top surface and sidewalls of the region of unsilicided silicon.

10. The finFET of claim 9 wherein each source/drain diffusion region further includes a silicon-silicide interface having an increased surface area.

11. The finFET of claim 9 wherein a distance between the silicide formed on the top surface and sidewalls of the region of unsilicided silicon and a gate region of the finFET is based on a spacer width.

12. The finFET of claim 11 wherein the spacer is about 10 nm to about 100 nm wide.

13. The finFET of claim 9 further comprising a gate;
wherein a work function of the gate is substantially equal to the work function of the source-drain diffusions.

14. The finFET of claim 9 wherein the silicide has a resistivity of about 10 micro-ohm-cm to about 100 micro-ohm-cm.

15. A substrate, comprising a finFET as claimed in any one of claims 9 to 14.

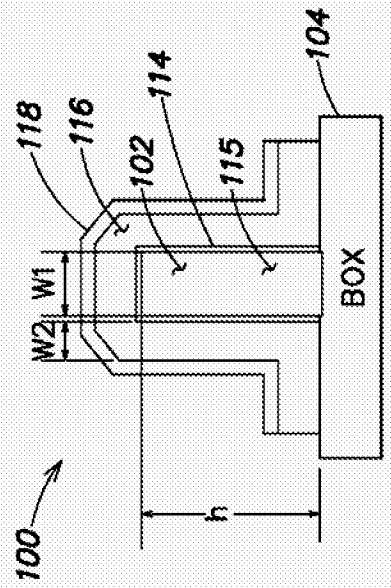


FIG. 1C

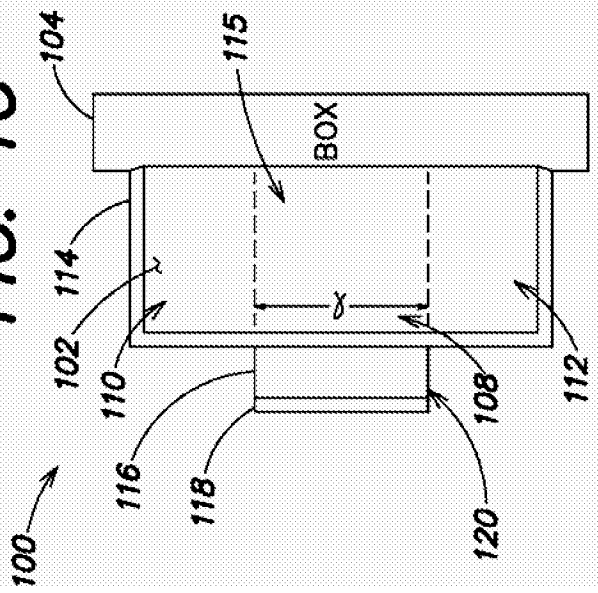


FIG. 1D

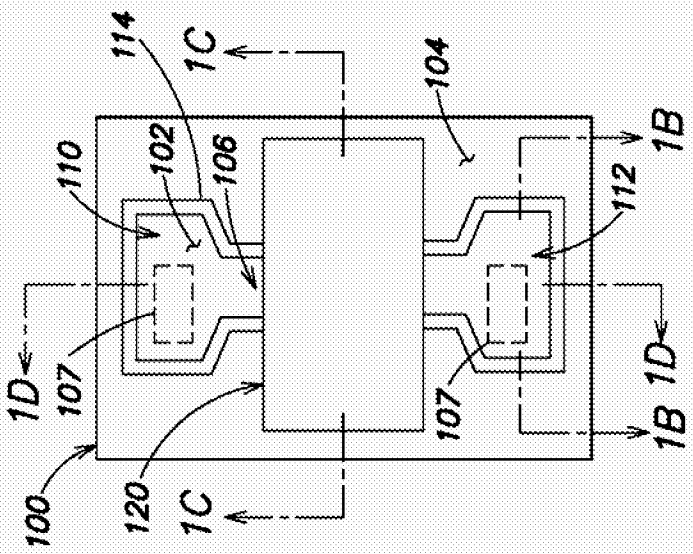


FIG. 1A

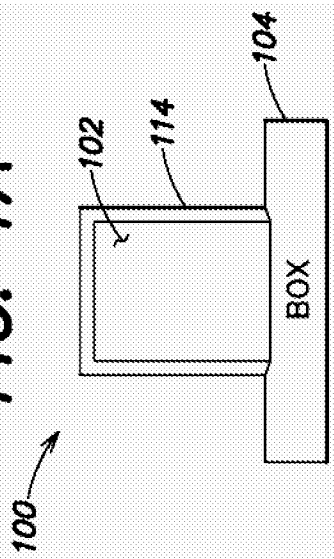


FIG. 1B

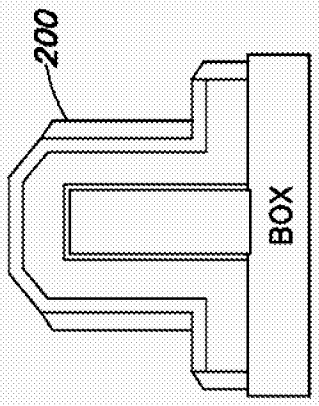


FIG. 2C

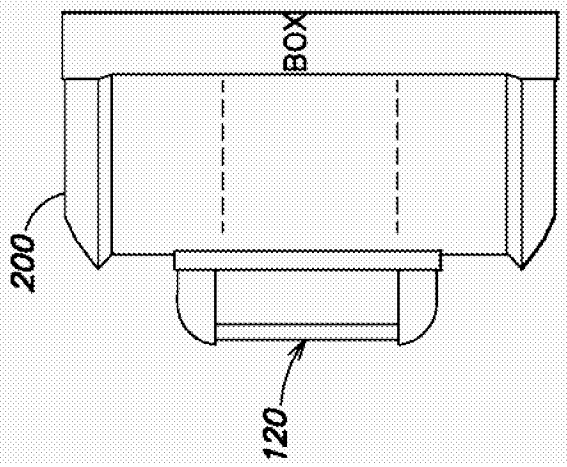


FIG. 2D

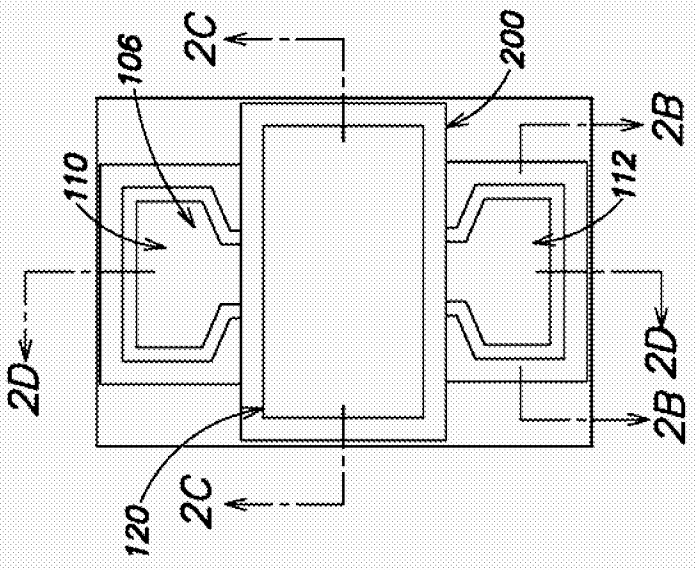


FIG. 2A

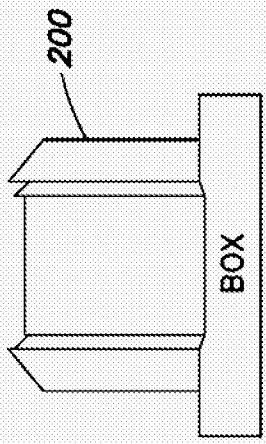


FIG. 2B

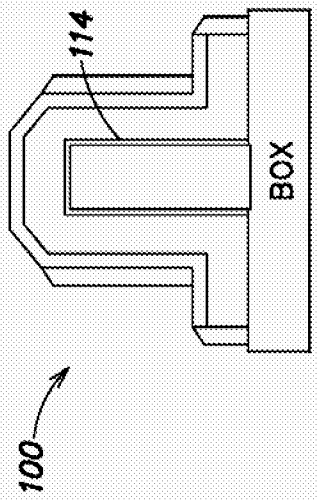


FIG. 3C

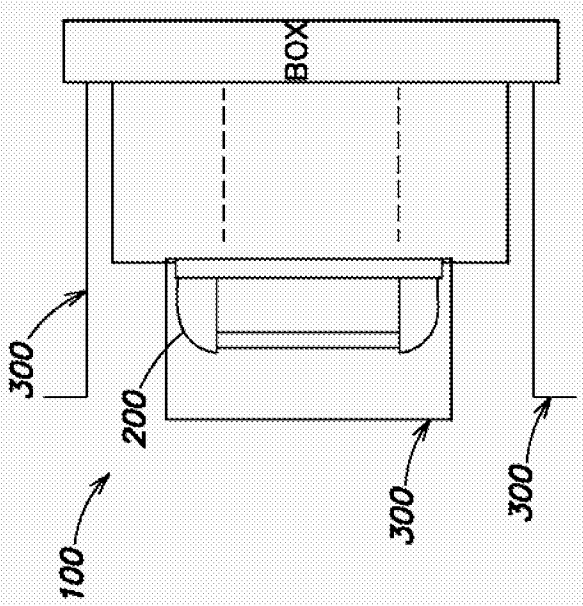


FIG. 3D

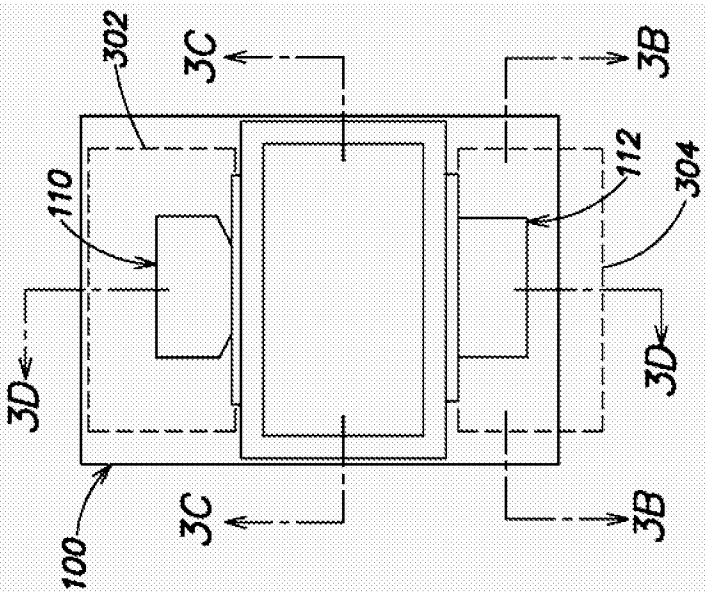


FIG. 3A

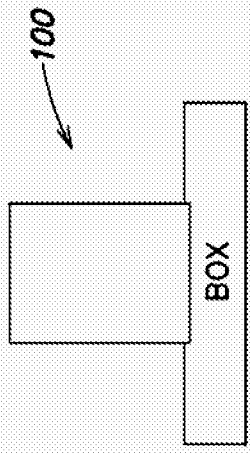


FIG. 3B

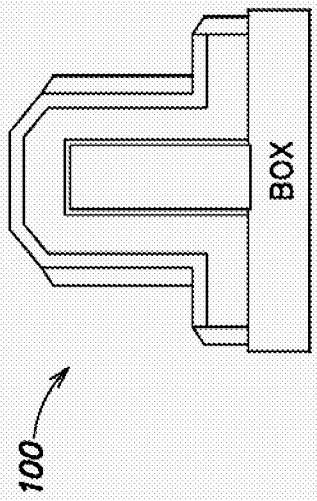


FIG. 4C

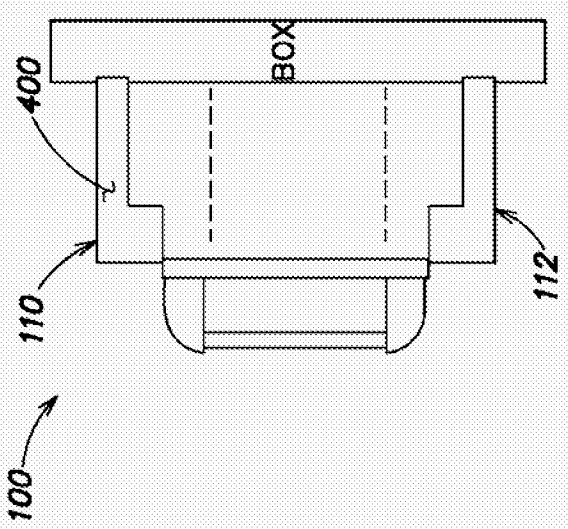


FIG. 4D

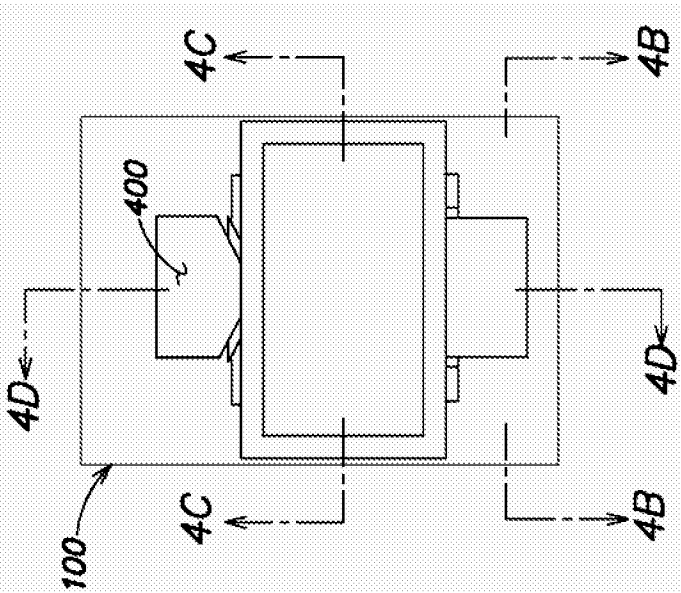


FIG. 4A

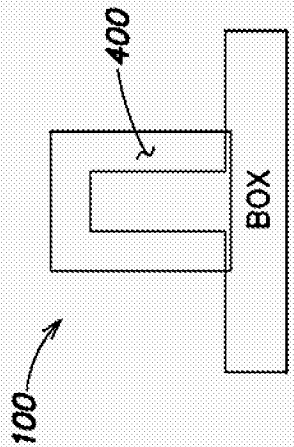


FIG. 4B

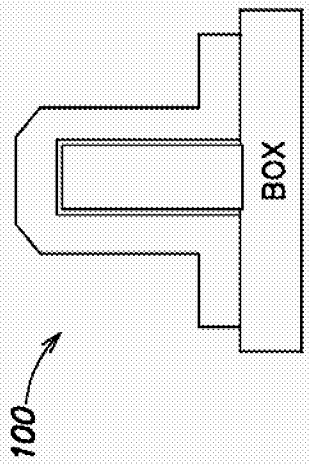


FIG. 5C

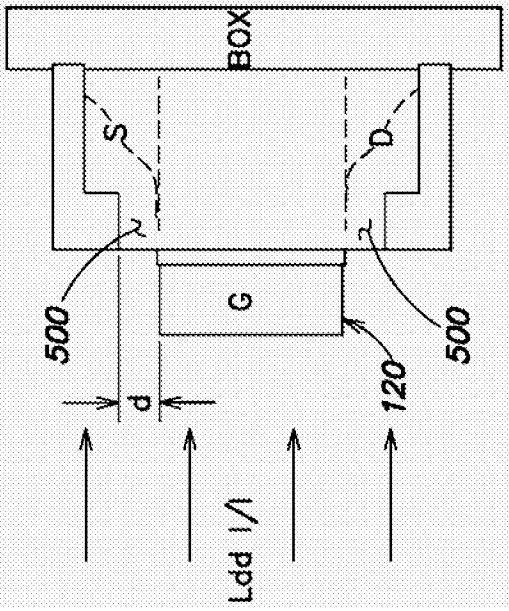


FIG. 5D

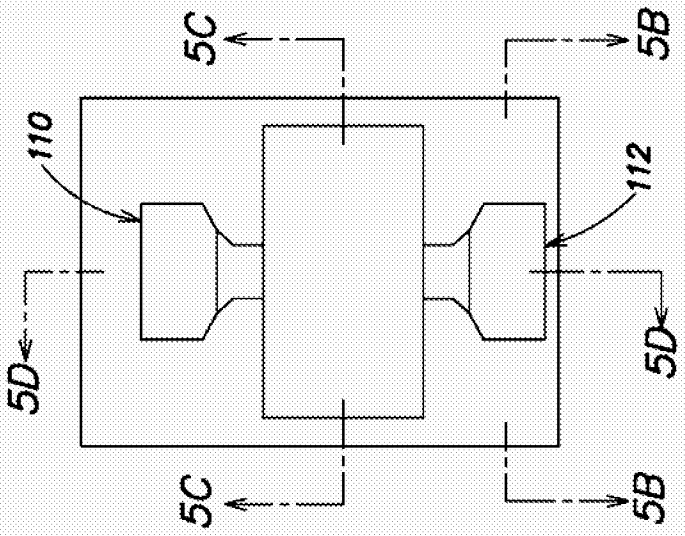


FIG. 5A

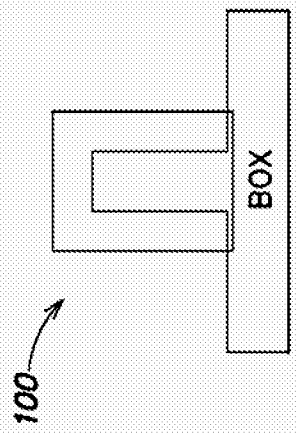


FIG. 5B

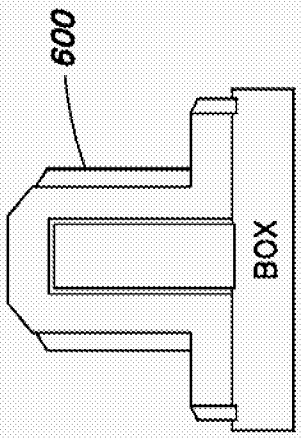


FIG. 6C

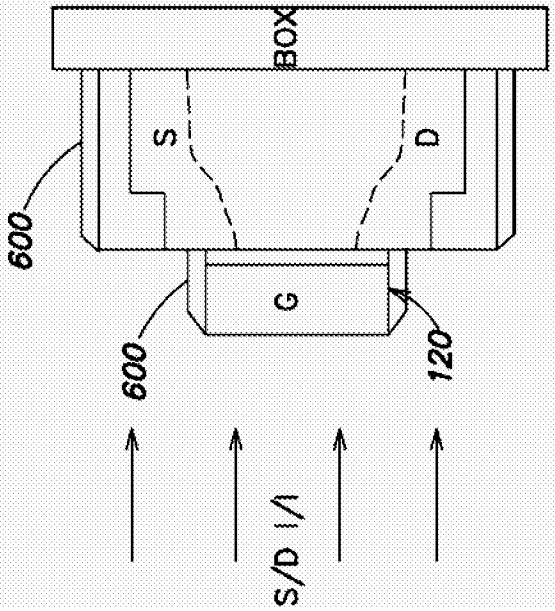


FIG. 6D

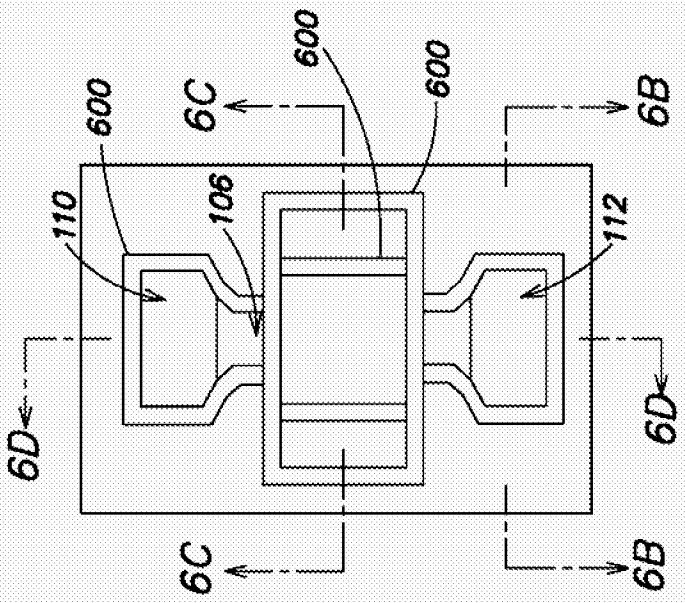


FIG. 6A

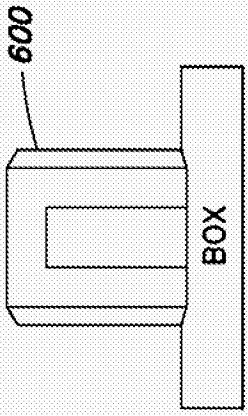


FIG. 6B

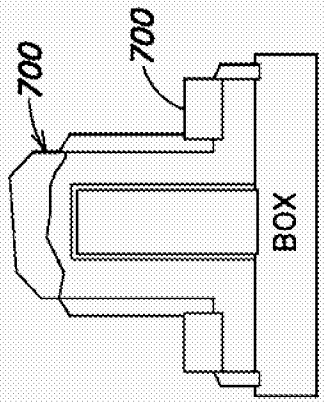


FIG. 7C

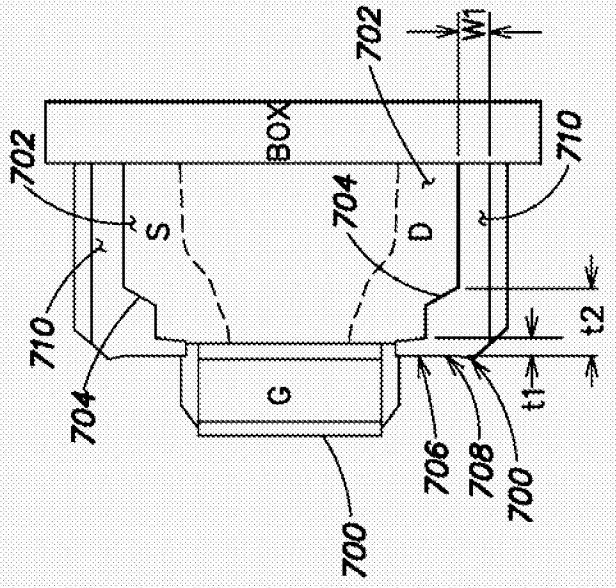


FIG. 7D

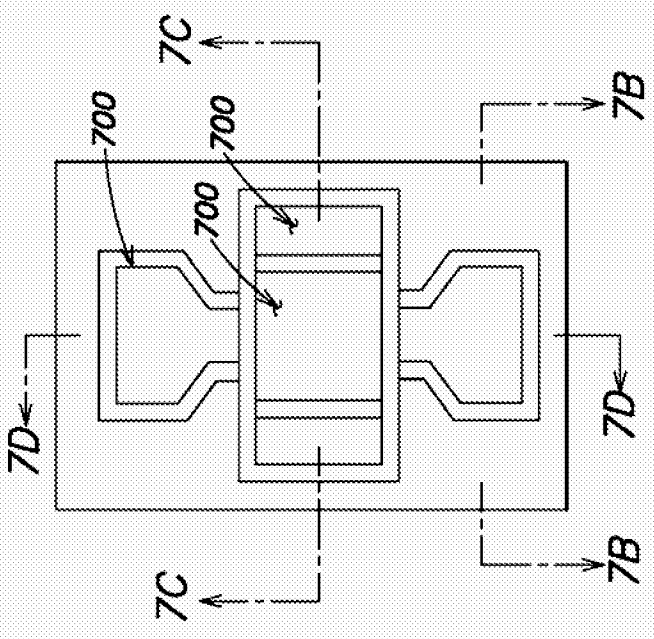


FIG. 7A

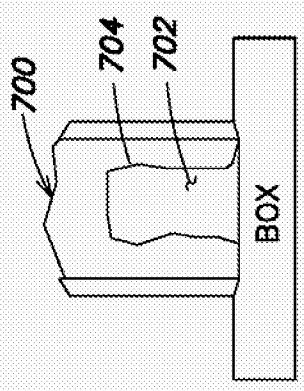


FIG. 7B

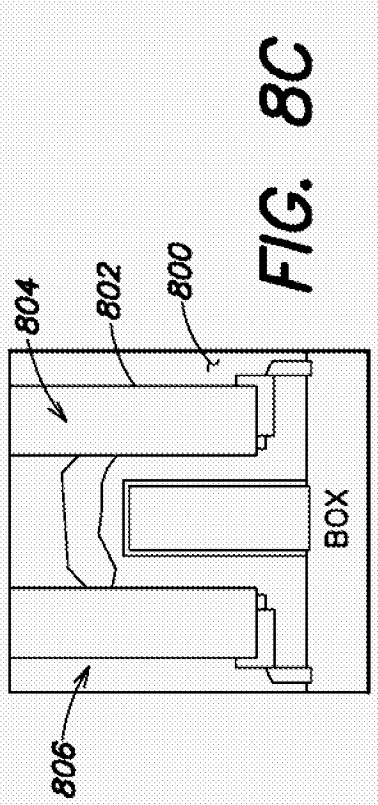


FIG. 8C

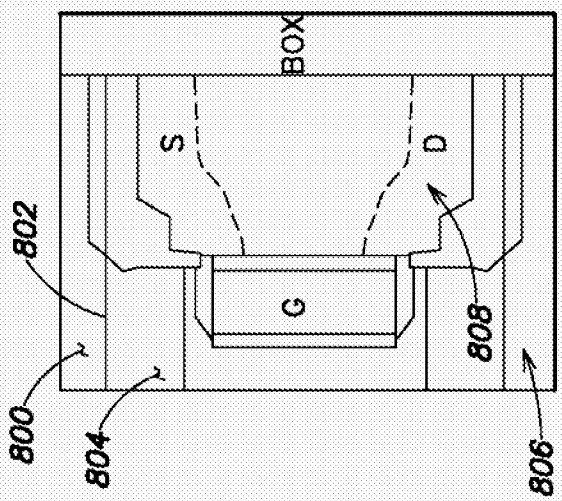


FIG. 8D

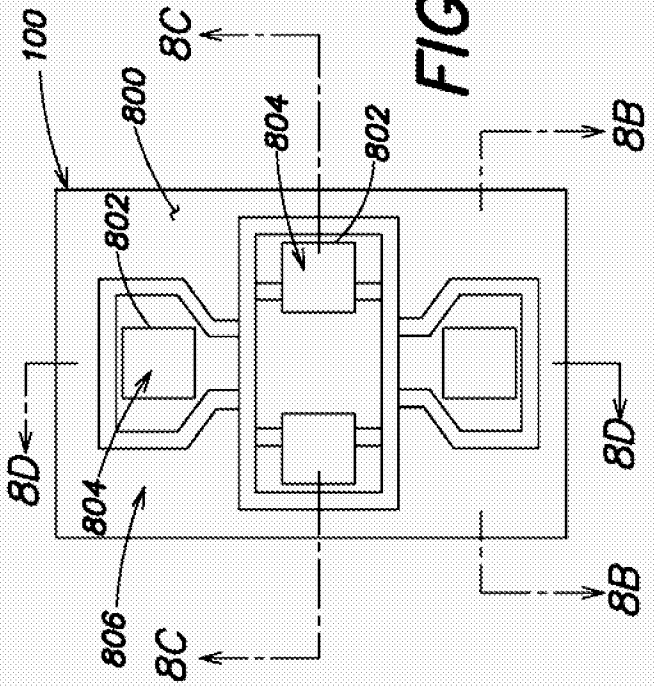


FIG. 8A

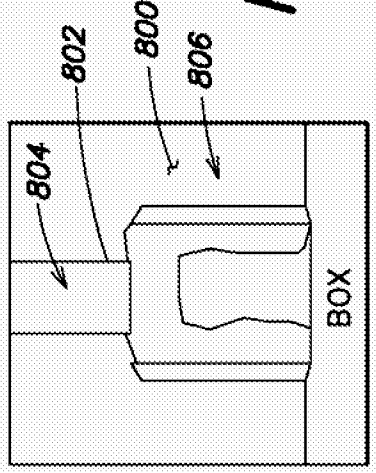


FIG. 8B

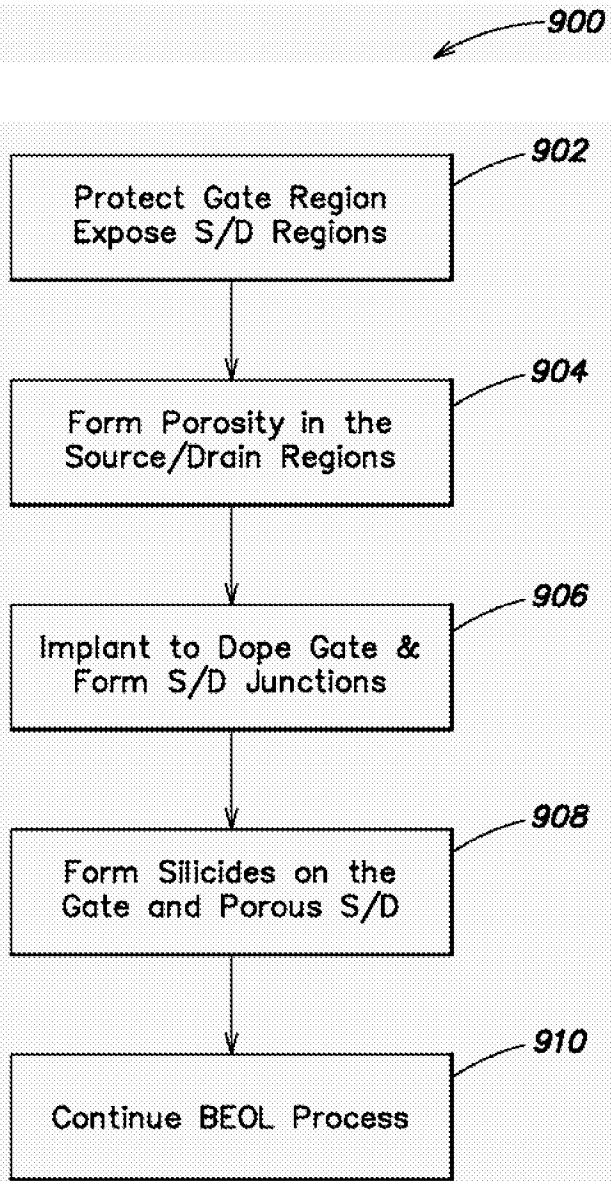
900
902
Protect Gate Region
Expose S/D Regions
904
Form Porosity in the
Source/Drain Regions
906
Implant to Dope Gate &
Form S/D Junctions
908
Form Silicides on the
Gate and Porous S/D
910
Continue BEOL Process

FIG. 9

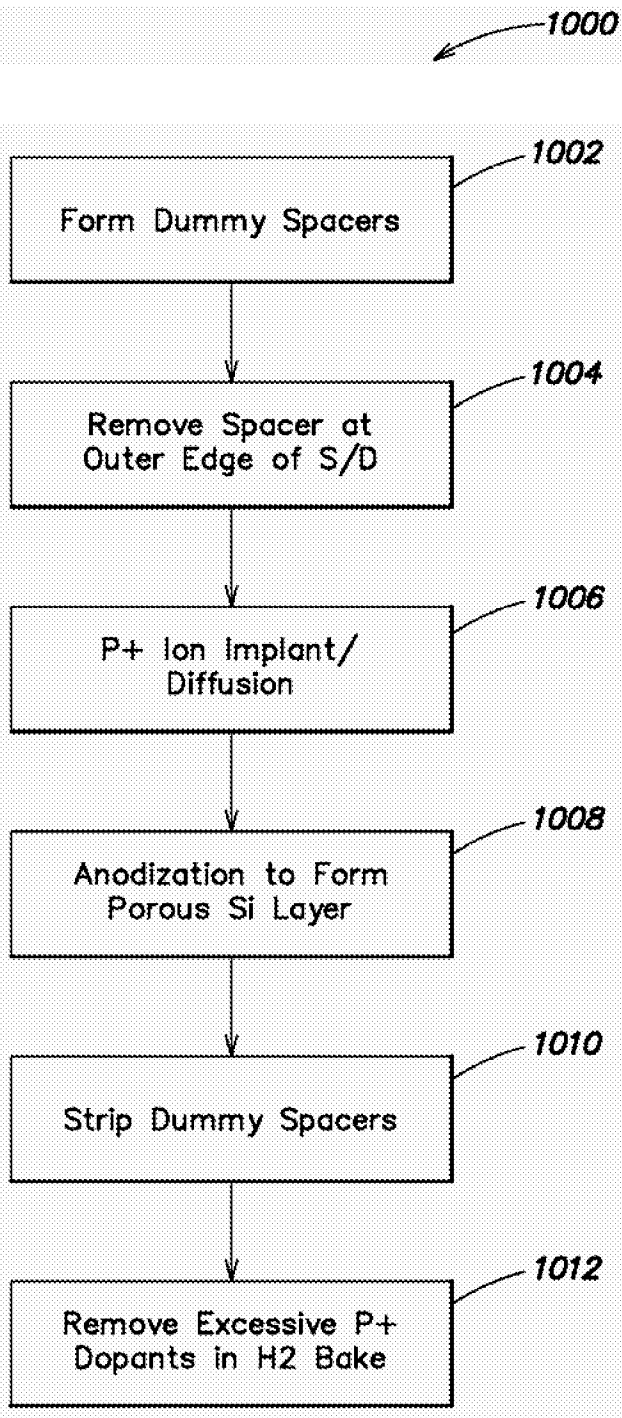
1000
1002
Form Dummy Spacers
1004
Remove Spacer at Outer Edge of S/D
1006
P+ Ion Implant/ Diffusion
1008
Anodization to Form Porous Si Layer
1010
Strip Dummy Spacers
1012
Remove Excessive P+ Dopants in H2 Bake

FIG. 10

# INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/069339

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/786 H01L21/336 H01L29/45 H01L21/285 H01L21/8234

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 2004/036126 A1 (CHAU ROBERT S [US] ET AL) 26 February 2004 (2004-02-26)<br>paragraph [0029]; figure 4A | 1,2, 8-12,14, 15 |
| Y | | 13 |
| X | US 2004/099885 A1 (YEO YEE-CHIA [TW] ET AL) 27 May 2004 (2004-05-27)<br>paragraph [0062] | 1,2, 9-12,14, 15 |
| A | US 6 255 214 B1 (WIECZOREK KARSTEN [DE] ET AL) 3 July 2001 (2001-07-03)<br>column 4, line 15 - line 34 | 1-7 |
| A | WO 00/17914 A2 (ULTRATECH STEPPER INC [US]) 30 March 2000 (2000-03-30)<br>page 5, line 11 - line 13 | 1-7 |

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 18 April 2007 | 24/04/2007 |

| Name and mailing address of the ISA/ | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL – 2280 HV Rijswijk<br>Tel. (+31–70) 340–2040, Tx. 31 651 epo nl,<br>Fax: (+31–70) 340–3016 | Hoffmann, Niels |

# INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/069339

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
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| A | RAMOS A R ET AL: "Synthesis of cobalt silicide on porous silicon by high dose ion implantation" NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION - B: BEAM INTERACTIONS WITH MATERIALS AND ATOMS, ELSEVIER, AMSTERDAM, NL, vol. 178, no. 1-4, May 2001 (2001-05), pages 283-286, XP004242579 ISSN: 0168-583X the whole document | 1-7 |
| A | RAMOS A R ET AL: "Ion beam synthesis of chromium silicide on porous silicon" NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION - B: BEAM INTERACTIONS WITH MATERIALS AND ATOMS, ELSEVIER, AMSTERDAM, NL, vol. 161-163, March 2000 (2000-03), pages 926-930, XP004192356 ISSN: 0168-583X the whole document | 1-7 |
| Y | US 2005/173768 A1 (LEE CHOONG-HO [KR] ET AL) 11 August 2005 (2005-08-11) paragraphs [0026] - [0028] paragraphs [0041], [0042] | 13 |
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| A | LIFSHITZ NADIA: "Dependence of the Work-Function Difference Between the Polysilicon Gate and Silicon Substrate on the Doping Level in Polysilicon" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, vol. ED-32, no. 3, March 1985 (1985-03), pages 617-621, XP002411227 ISSN: 0018-9383 the whole document | 1,8,9, 13,15 |
| A | US 2005/272235 A1 (WU CHII-MING [TW] ET AL) 8 December 2005 (2005-12-08) paragraphs [0013], [0022] | 1,8,9, 13,15 |
| A | US 2005/258477 A1 (SAITO TOMOHIRO [JP]) 24 November 2005 (2005-11-24) the whole document | 1,8,9, 13,15 |
| A | US 2005/255643 A1 (AHN YOUNG-JOON [KR] ET AL) 17 November 2005 (2005-11-17) paragraph [0034] | 1,8,9, 13,15 |

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2006/069339

## Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

## Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

**Remark on Protest**

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

**FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210**

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1 (in part), 2-7, 9 (in part), 10, 11, 12, 14, 15 (in part)

   Method of forming silicide by forming porous oxide on source/drain regions and FinFET having a silicided source/drain.

   ---

2. claims: 1 (in part), 8, 9 (in part), 13, 15 (in part)

   Method of forming gate electrode with having a predetermined work function and FinFET having gate electrode with predetermined work function.

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# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2006/069339

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
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