A driving method of a light emitting device, in which when an N-type driving TFT is connected to an anode of a light emitting element or a P-type driving TFT is connected to a cathode thereof, the driving TFT operates in a saturation region and an image can be displayed with a desired gray scale level depending on a video signal. In addition, a light emitting device adopting the driving method is provided. According to the invention, when a potential having image data is supplied to a gate of a driving TFT depending on a video signal, a reverse bias voltage is applied to the driving TFT and a light emitting element which are connected in series with each other. Meanwhile, when a pixel displays an image depending on the video signal, a forward bias voltage is applied to the driving TFT and the light emitting element.
FIG. 1A WRITING PERIOD (DURING APPLICATION OF REVERSE BIAS)

FIG. 1B DISPLAY PERIOD (DURING APPLICATION OF FORWARD BIAS)
FIG. 1C
FIG. 3A

FIRST LINE
SECOND LINE

K-TH LINE

LAST LINE

F: FRAME PERIOD

FIG. 3B

G1

G2

Gy

V1

V2

Vx

Vdd

Vdd

Vss
FIG. 5A

SCAN LINE DRIVER CIRCUIT 406
SIGNAL LINE DRIVER CIRCUIT 405

FIG. 5B

SHIFT REGISTER 410

Video signal
INVERTER 411
TRANSMISSION GATE 412

FIG. 5C

SP
CLK

INVERTER 416
NOR

INVERTER 417

SHIFT REGISTER 415

PULSE WIDTH CONTROL SIGNAL
FIG. 7A

FIRST LINE
SECOND LINE
K-TH LINE
LAST LINE

F: FRAME PERIOD

FIG. 7B

FIRST LINE
SECOND LINE
K-TH LINE
LAST LINE

F: FRAME PERIOD

FIG. 7C

FIRST LINE
SECOND LINE
K-TH LINE
LAST LINE

F: FRAME PERIOD
DRIVING METHOD OF LIGHT EMITTING DEVICE AND LIGHT EMITTING DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application Ser. No. 10/902,811, filed Aug. 2, 2004, now allowed, which claims the benefit of a foreign priority application filed in Japan as Serial No. 2003-289569 on Aug. 8, 2003, both of which are incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The invention relates to a driving method of a light emitting device comprising a plurality of pixels each of which includes a light emitting element and a means for supplying a current to the light emitting element. The invention further relates to a light emitting device.

[0004] 2. Description of the Related Art

[0005] Emitting light by itself, a light emitting element has a high visibility. Further, since it requires no backlight, a display device using the light emitting element can be easily reduced in thickness and the viewing angle thereof is not restricted. Therefore, the light emitting device using a light emitting element, which attracts attention as an alternative display device to a CRT or an LCD, has been developed for practical use. The light emitting device can be classified into a passive matrix device and an active matrix device. In the active matrix device, a current supply to a light emitting element can be maintained to some extent after a video signal input. Thus, the active matrix device can be flexibly applied to a large panel with high definition and it is expected to become the mainstream in the future. Specifically, each manufacturer offers a different pixel configuration of the active matrix light emitting device, and adopts various technical measures. Though, in general, each pixel comprises at least a light emitting element, a transistor for controlling a video signal input to the pixel, and a transistor for supplying a current to the light emitting element.

[0006] For a transistor provided in each pixel of a light emitting device, a thin film transistor (TFT) whose active layer is formed of a thin semiconductor film is mainly employed. Among the TFTs, a TFT using an amorphous semiconductor or a semi-amorphous semiconductor (microcrystalline semiconductor) has the advantage that the cost and the yield can be improved as compared with a TFT using a polycrystalline semiconductor because of fewer manufacturing steps. In addition, such a TFT requires no crystallization step after forming a semiconductor film, therefore, it can be used for forming a large panel with relative ease.

[0007] A problem in practical use of a light emitting device is luminance decay of a light emitting element with the degradation of an electro luminescent material. A degradation level of an electro luminescent material depends on the amount of light emitting time and the amount of current flowing. Accordingly, when the gray level differs in each pixel depending on a displayed image, the degradation level of a light emitting element differs in each pixel as well, leading to variations in luminance. In order to suppress such luminance decay, in the following Patent Document 1, a transistor for controlling a current supplied to a light emitting element operates in a saturation region, and a drain current is thus kept constant when the transistor is ON regardless of the degradation of an electro luminescent layer.

[0008] Patent Document 1


SUMMARY OF THE INVENTION

[0010] Explained hereinafter is a problem in using in a pixel a TFT formed of an amorphous semiconductor or a semi-amorphous semiconductor and operating a transistor for supplying a current to a light emitting element in a saturation region.

[0011] A semi-amorphous semiconductor is a film including a semiconductor which has an intermediate structure between amorphous and crystalline (including single crystalline and polycrystalline) structures. The semi-amorphous semiconductor has a third state which is stable in free energy, and it is a kind of a crystalline semiconductor which has a short range order and a lattice distortion. This semiconductor has a grain size of 0.5 to 20 nm and can be dispersed in a non-single crystalline semiconductor. Further, the semiconductor is mixed with at least 1 atom % of hydrogen or halogen as the neutralizing agent for dangling bond. Such a semiconductor is called herein a semi-amorphous semiconductor (SAS) for convenience. When a noble gas element such as helium, argon, krypton, or neon is mixed into an SAS, the lattice distortion is increased and the stability is thus enhanced, leading to an excellent SAS. Such SAS semiconductor is disclosed in U.S. Pat. No. 4,409,134, for example.

[0012] In the case where a TFT formed of an amorphous semiconductor or a semi-amorphous semiconductor is actually used as a transistor (driving TFT) for supplying a current to a light emitting element, an N-type TFT is employed because it has a certain mobility. The light emitting element comprises an anode, a cathode, and an electro luminescent layer provided between the anode and the cathode. In general, the anode is connected to a source or a drain of the transistor for supplying a current to the light emitting element.

[0013] FIG. 19A shows a connection of a P-type driving TFT and a light emitting element. Note that a potential Vdd> a potential Vss is satisfied. As shown in FIG. 19A, a P-type driving TFT 10 is connected in series with a light emitting element 11. In the P-type TFT, an electrode with a higher potential serves as a source (S) whereas an electrode with a lower potential serves as a drain (D). Therefore, the Vdd is supplied to a source of the P-type driving TFT 10, a drain thereof is connected to an anode of the light emitting element 11, and the Vss is supplied to a cathode of the light emitting element 11.

[0014] When a potential is supplied to a gate (G) of the driving TFT 10 in accordance with a video signal inputted to a pixel, a potential difference (gate voltage) Vgs is generated between the gate and the source of the driving TFT 10 and a drain current thereof corresponding to the Vgs is supplied to the light emitting element 11. In the case of FIG. 19A, since a fixed potential Vdd is supplied to the source of the driving TFT 10, the gate voltage Vgs is determined only by a potential supplied to the gate thereof.

[0015] A connection of an N-type driving TFT and a light emitting element is shown in FIG. 19B. As shown in FIG. 19B, an N-type driving TFT 20 is connected in series with a light emitting element 21. As for the N-type TFT, an electrode with a lower potential serves as a source (S) whereas an electrode with a higher potential serves as a drain (D). Therefore, the Vdd is supplied to a drain of the N-type driving TFT.
20, a source thereof is connected to an anode of the light emitting element 21, and the Vss is supplied to a cathode of the light emitting element 21.  

[0016] When a potential is supplied to a gate (G) of the driving TFT 20 in accordance with a video signal inputted to a pixel, a potential difference (gate voltage) Vgs is generated between the gate and the source of the driving TFT 20 and a drain current thereof corresponding to the Vgs is supplied to the light emitting element 21. In the case of the connection shown in FIG. 19D, however, differently from the connection shown in FIG. 19A, a potential supplied to the source of the driving TFT 20 is not fixed and determined by a source-drain voltage (drain voltage) Vds of the driving TFT 20 and an anode-cathode voltage Ve1 of the light emitting element 21. Accordingly, the gate voltage Vgs cannot be determined only by a potential supplied to the gate, and a drain current of the driving TFT 20 cannot be kept constant even when inputting to a pixel a video signal having the same image data, leading to variations in luminance of the light emitting element 21.  

[0017] In particular, the drain voltage Vds of the driving TFT 20 which operates in a saturation region is higher than that of the driving TFT 20 which operates in a linear region. Therefore, it becomes difficult to fix a source potential when a potential is supplied to the gate of the driving TFT 20 depending on a video signal, and thus a pixel cannot display an image with a desired gray scale level.  

[0018] It is to be noted that the aforementioned problem may occur when using a P-type driving TFT as well as an N-type driving TFT. In the case of a pixel where a drain of a P-type driving TFT is connected to a cathode of a light emitting element, it is difficult to fix a source potential when a potential is supplied to a gate of the P-type driving TFT in accordance with a video signal. Thus, the pixel cannot display a desired gray scale level.  

[0019] In view of the foregoing, the invention provides a driving method of a light emitting device, in which a driving TFT operates in a saturation region and an image can be displayed with a desired gray scale level depending on a video signal when an N-type driving TFT is connected to an anode of a light emitting element or a P-type driving TFT is connected to a cathode of the light emitting element. The invention further provides a light emitting device using the driving method.  

[0020] The general idea of the inventor is that a gate voltage of a driving TFT will be able to be written without fail depending on a video signal having image data by utilizing nonlinearity of a light emitting element. According to the invention, when a potential having image data is supplied to a gate of a driving TFT depending on a video signal, a reverse bias voltage is applied to the drain to a light emitting element which are connected in series with each other. Meanwhile, a forward bias voltage is applied to the driving TFT and the light emitting element when a pixel displays an image in accordance with the video signal.  

[0021] A driving method of the invention is described in more detail with reference to FIGS. 1A and 1B. FIG. 1A shows a connection of an N-type driving TFT and a light emitting element and a relation between potentials supplied to each element during a period in which a video signal is inputted to a pixel (writing period). In the writing period, a reverse bias voltage is applied to a driving TFT 100 and a light emitting element 101 which are connected in series with each other. Specifically, a potential Vss is supplied to a source of the driving TFT 100, a drain thereof is connected to an anode of the light emitting element 101, and a potential Vdd higher than the Vss is supplied to a cathode of the light emitting element 101.  

[0022] It is to be noted that a TFT comprises three electrodes: a gate, a source and a drain. One of the two electrodes (first electrode and second electrode) other than the gate corresponds to either the source or the drain depending on a supplied potential level. In the case of an N-type TFT, an electrode with a lower potential corresponds to the source whereas an electrode with a higher potential corresponds to the drain. In this specification, an electrode which is closer to an anode of a light emitting element is referred to as a first electrode.  

[0023] Since the light emitting element 101 is a nonlinear element, an anode-cathode voltage Ve1 of thereof is much higher relative to a drain voltage Vds of the driving TFT 100. Accordingly, a potential at a connection node (node A) of the driving TFT 100 and the light emitting element 101 is approximately equal to the Vss. That is, a potential at the node A is considered to be substantially fixed. Note that the node A in the writing period corresponds to a connection point of the anode of the light emitting element 101 and the drain of the driving TFT 100.  

[0024] When a potential Vg is supplied to the gate of the driving TFT 100 depending on a video signal at this time, a potential difference between the Vss and the Vg is held in a capacitor 102.  

[0025] FIG. 1B shows a connection of the N-type driving TFT and the light emitting element and a relation between potentials supplied to each element during a period in which a pixel displays an image (display period). In the display period, a forward bias voltage is applied to the driving TFT 100 and the light emitting element 101 which are connected in series with each other. Specifically, the Vdd is supplied to the drain of the driving TFT 100, the source thereof is connected to the anode of the light emitting element 101, and the Vss is supplied to the cathode of the light emitting element 101.  

[0026] At this time, the node A corresponds to a connection point of the source of the driving TFT 100 and the anode of the light emitting element 101. Accordingly, a potential difference between the Vss and the Vg, which is held in the capacitor 102 corresponds to a gate voltage Vgs of the driving TFT 100, and a drain current corresponding to the gate voltage Vgs is supplied to the light emitting element 101. Thus, according to the invention, the gate voltage Vgs of the driving TFT 100 is determined only by the Vg supplied to the gate thereof because the Vss is fixed.  

[0027] Note that in the invention, the driving TFT is not limited to an N-type TFT, and a P-type TFT may be employed as well. Though, in the case of using a P-type driving TFT, the driving TFT is connected to a cathode of a light emitting element.  

[0028] According to the invention, a semi-amorphous semiconductor has only to be used for a channel forming region. In addition, not all the channel forming region necessarily includes the semi-amorphous semiconductor along the thickness thereof, and the semi-amorphous semiconductor has only to be included in a part of the channel forming region.  

[0029] In this specification, a light emitting element includes an element whose luminance is controlled by current or voltage. More specifically, it includes an OLED (Organic
Light Emitting Diode), an MIM electron source element (electron emissive element) used for an FED (Field Emission Display), and the like.

[0030] A light emitting device includes a panel having a light emitting element sealed therein, and a module having an IC and the like including a controller which are mounted on the panel. In addition, the invention relates to an element substrate which corresponds to one mode before completing the light emitting element in manufacturing steps of the light emitting device, and the element substrate comprises a plurality of pixels each having a means for supplying a current to the light emitting element. The element substrate specifically corresponds to any aspect such as the one including only a pixel electrode of the light emitting element and the one after forming a conductive layer serving as a pixel electrode and before patterning it to form the pixel electrode.

[0031] An OLED (Organic Light Emitting Diode), which is one of the light emitting elements, comprises an anode layer, a cathode layer, and a layer including an electro luminescent material (hereinafter referred to as an electro luminescent layer) which generates the electro luminescence when an electric field is applied. The electro luminescent layer is provided between the anode and the cathode and formed of one or more layers. Specifically, the electro luminescent layer includes a hole injection layer, a hole transporting layer, a light emitting layer, an electron injection layer, an electron transporting layer, and the like. An inorganic compound may be included in the electro luminescent layer. The luminescence in the electro luminescent layer includes luminescence that is generated when an excited singlet state returns to a ground state (fluorescence) and luminescence that is generated when an excited triplet state returns to a ground state (phosphorescence).

[0032] According to the aforementioned configuration of the invention, an N-type driving TFT can operate in a saturation region and an image can be displayed with a desired gray scale level in accordance with a video signal. Further, since the driving TFT operates in a saturation region, a drain current does not vary depending on a drain voltage Vds and is determined only by a gate voltage Vgs. Therefore, the drain current can be maintained relatively constant even when the Vds is lowered without increasing the Vgs in accordance with the degradation of a light emitting element. Thus, it is possible to suppress luminance decay and variations in luminance of the light emitting element due to the degradation of an electro luminescent material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] FIGS. 1A and 1B are diagrams each showing a connection of a driving TFT and a light emitting element and a relation between potentials supplied to each element.

[0034] FIG. 2 is a circuit diagram of a pixel portion.

[0035] FIGS. 3A and 3B are diagrams each showing a driving method of the light emitting device of the invention.

[0036] FIG. 4 is a circuit diagram of a pixel portion.

[0037] FIGS. 5A to 5C are diagrams each showing a configuration of the light emitting device of the invention.

[0038] FIGS. 6A to 6E are circuit diagrams of a pixel.

[0039] FIGS. 7A to 7C are diagrams each showing a driving method of the light emitting device of the invention.

[0040] FIGS. 8A to 8D are schematic diagrams of an element substrate used for the light emitting device of the invention.

[0041] FIGS. 9A and 9B are cross sectional views of a driving circuit and a pixel portion.

[0042] FIG. 10A is a circuit diagram of a pixel and FIG. 10B is a cross sectional view of the same.

[0043] FIGS. 11A to 11C are diagrams each showing a manufacturing method of the light emitting device.

[0044] FIGS. 12A to 12C are diagrams each showing a manufacturing method of the light emitting device.

[0045] FIGS. 13A and 13B are diagrams each showing a manufacturing method of the light emitting device.

[0046] FIG. 14 is a top plan view of a pixel.

[0047] FIGS. 15A to 15C are cross sectional views of a pixel.

[0048] FIGS. 16A and 16B are diagrams each showing an example of a shift register.

[0049] FIG. 17A is a top plan view of the light emitting device of the invention and FIG. 17B is a cross sectional view of the same.

[0050] FIGS. 18A to 18C are views each showing an electronic apparatus using the light emitting device of the invention.

[0051] FIGS. 19A and 19B are diagrams each showing a connection of a driving TFT and a light emitting element.

[0052] FIGS. 20A and 20B are diagrams each showing a driving method of the light emitting device of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Embodiment Mode

[0053] FIG. 2 shows a configuration of a pixel portion of a light emitting device which displays an image by using the driving method of the invention. As shown in FIG. 2, a plurality of pixels are arranged in matrix in the pixel portion, and various signals and potentials are supplied to each of the pixels via signal lines S1 to Sx, scan lines G1 to Gx and power supply lines V1 to Vx.

[0054] Each of the pixels comprises a light emitting element 201, a TFT (a switching TFT) 202 for controlling a video signal input to the pixel 200, a driving TFT 203 for controlling a current supply to the light emitting element 201. Although the pixel 200 shown in FIG. 2 further comprises a capacitor 204 separately from the driving TFT 203, the invention is not limited to this configuration. The capacitor 204 is not necessarily formed separately from the driving TFT 203, and a capacitance (gate capacitance) between a gate electrode and an active layer of the driving TFT 203 may be employed as the capacitor 204 instead. An N-type TFT is used for both the switching TFT 202 and the driving TFT 203.

[0055] A gate of the switching TFT 202 is connected to a scan line Gx (j=1 to y). Either a source or a drain of the switching TFT 202 is connected to a signal line Si (i=1 to x) and the other thereof is connected to a gate of the driving TFT 203. Either a source or a drain of the driving TFT 203 is connected to a power supply line Vi (i=1 to x) and the other thereof is connected to an anode of the light emitting element 201. One of two electrodes of the capacitor 204 is connected to the gate of the driving TFT 203 and the other is connected to the anode of the light emitting element 201.

[0056] It is to be noted that the pixel configuration shown in FIG. 2 is just an example of the light emitting device to which the driving method of the invention can be applied, and the light emitting device capable of adopting the driving method of the invention is not limited to the configuration shown in FIG. 2.
A driving method of the pixel portion shown in FIG. 2 is described next. The driving method of the invention can be divided into a writing period, a reverse bias period and a display period. FIG. 3A shows an example of timing of a writing period T_{a}, a reverse bias period T_r and a display period T_d.

First, when the reverse bias period T_r starts, a reverse bias voltage is applied to the driving TFT 203 and the light emitting element 201 which are connected in series with each other. Specifically, a potential V_{ss} is supplied to the power supply lines V_{1} to V_{x} and a potential V_{dd} higher than the V_{ss} is supplied to a cathode of the light emitting element 201.

Then, the writing period T_{a} starts. Note that according to the driving method of the invention, the writing period T_{a} is included in the reverse bias period T_r. When the writing period T_{a} starts, the scan lines G_{1} to G_{y} are sequentially selected, and the switching TFT 202 of each pixel 200 is turned ON. Then, as a video signal is supplied to the signal lines S_{1} to S_{x}, a video signal potential V_{g} is supplied to the gate of the driving TFT 203 via the switching TFT 202.

Since the light emitting element 201 is a nonlinear element, a voltage V_{el} between the anode and the cathode of the light emitting element 201 becomes much higher than a drain voltage V_{ds} of the driving TFT 203 when the reverse bias voltage is applied. Accordingly, a potential of the anode of the light emitting element 201 becomes approximately equal to the V_{ss} supplied to the power supply lines V_{1} to V_{x}, and a potential difference between the V_{ss} and the video signal potential V_{g} is accumulated and held in the capacitor 204.

When the writing period T_{a} is completed and the switching TFT 202 is turned OFF, the reverse bias period T_r is completed and then, the display period T_d starts.

In the display period T_d, a forward bias voltage is applied to the driving TFT 203 and the light emitting element 201 which are connected in series with each other. Specifically, a potential V_{dd} higher than the V_{dd} is supplied to the power supply lines V_{1} to V_{x}, and the V_{dd} is supplied to the cathode of the light emitting element 201.

Although the same potential is supplied to the cathode in both the reverse bias period T_r and the display period T_d in this embodiment mode, the invention is not limited to this. It is only necessary that a reverse bias voltage is applied to the light emitting element 201 in the reverse bias period T_r and a forward bias voltage is applied to the light emitting element 201 in the display period T_d, when the driving TFT 203 is ON.

When a forward bias voltage is applied, the source of the driving TFT 203 is connected to the anode of the light emitting element 201 since the driving TFT 203 is an N-type transistor. Therefore, the potential difference between the V_{ss} and the video signal potential V_{g} is held in the capacitor 204 and becomes equal to the gate voltage V_{gs} of the driving TFT 203. As a result, the driving TFT 203 supplies to the light emitting element 201 a drain current corresponding to the gate voltage V_{gs}.

FIG. 3B shows a timing chart of the scan lines G_{1} to G_{y} and the power supply lines V_{1} to V_{x} in each period. When it is supposed that pixels of one row have a scan line in common, the writing period T_{a} appears in sequence in each row. Each writing period T_{a} is included in the reverse bias period T_r. It is to be noted that the writing period T_{a} and the reverse bias period T_r can be overlapped with each other completely. However, by setting the reverse bias period T_r longer than the writing period T_{a}, it is possible to prevent noise and the like due to fluctuation of the potential of the power supply lines V_{1} to V_{x}.

Note that in the invention, the driving TFT 203 is not limited to an N-type transistor and a P-type transistor may also be employed. In the case of a P-type driving TFT, the driving TFT is connected to the cathode of the light emitting element.

In FIG. 3A, an example of timing of the writing period, the reverse bias period and the display period is shown in the case of using an analog video signal, however, a digital video signal may be used in the invention as well. For example, in the case where time gray scale display is achieved by the use of a digital video signal, the writing period T_{a}, the reverse bias period T_r and the display period T_d may be provided for each bit of the digital signal as shown in FIG. 7A.

Although an amorphous semiconductor or a semi-amorphous semiconductor is used for TFTs in a pixel portion in this embodiment mode, the invention is not limited to this. The driving method of the invention can also be applied to a light emitting device using a polycrystalline semiconductor for TFTs in a pixel portion.

Embodiment 1

Described in this embodiment is an example of the light emitting device, in which the power supply lines are arranged parallel to the scan lines in the pixel portion shown in FIG. 2 and one scan line driver circuit controls both the scan lines and the power supply lines.

FIG. 4 shows a configuration of a pixel portion 401 in a light emitting device according to this embodiment. In FIG. 4, a pixel 400 comprises a light emitting element 405, a switching TFT 402, a driving TFT 403, and a capacitor 404 as the pixel portion shown in FIG. 2. The connection of each element is the same as that of the pixel 200 shown in FIG. 2. However, the power supply lines V_{1} to V_{y} are arranged parallel to the scan lines G_{1} to G_{y} in this embodiment.

A driving method of the pixel portion shown in FIG. 4 is described next. The driving method of the invention can be divided into a writing period T_{a}, a reverse bias period T_r and a display period T_d. FIG. 20A shows an example of timing of the writing period T_{a}, the reverse bias period T_r and the display period T_d. The total period from the beginning until the end of the reverse bias period T_r in all pixels is denoted by T_w.

First, when the reverse bias period T_r starts, a potential V_{dd} higher than a potential V_{ss} is supplied to a cathode of the light emitting element 405, and the V_{ss} is supplied to the power supply lines V_{1} to V_{y} in sequence. Accordingly, a reverse bias voltage is sequentially applied to the driving TFT 403 and the light emitting element 405, which are connected in series with each other, for pixels in each row.

Then, the writing period T_{a} starts. Note that in the driving method of the invention, the writing period T_{a} is included in the reverse bias period T_r for each row. When the writing period T_{a} starts, the scan lines G_{1} to G_{y} are sequentially selected, and the switching TFT 402 in each pixel is turned ON. Then, when a video signal is supplied to the signal lines S_{1} to S_{x}, a video signal potential V_{g} is supplied to a gate of the driving TFT 403 via the switching TFT 402.

Since the light emitting element 405 is a nonlinear element, an anode-cathode voltage V_{el} of the light emitting element 405 becomes much higher than a drain voltage V_{ds} of the driving TFT 403 when the reverse bias voltage is applied.
Accordingly, a potential of the anode of the light emitting element 405 is approximately equal to the Vss supplied to the power supply lines V1 to Vv, and a potential difference between the Vss and the video signal potential Vg is accumulated and held in the capacitor 404.

[0075] When the writing period Ta is completed and the switching TFT 402 is turned OFF, the reverse bias period Tr is completed and then, the display period Td starts.

[0076] In the display period Td, a forward bias voltage is sequentially applied to the driving TFT 403 and the light emitting element 405 which are connected in series with each other. Specifically, the Vdd is supplied to the cathode of the light emitting element 405, and a potential Vdd higher than the Vdd is supplied to the power supply lines V1 to Vv.

[0077] In the light emitting device shown in Fig. 4, the same potential is supplied to the cathode in both the reverse bias period Tr and the display period Td.

[0078] When a forward bias voltage is applied, a source of the driving TFT 403 is connected to the anode of the light emitting element 405 since the driving TFT 403 is an N-type transistor. Therefore, the potential difference between the Vss and the video signal potential Vg, which is held in the capacitor 404 becomes equal to the gate voltage Vgs of the driving TFT 403. As a result, the driving TFT 403 supplies the light emitting element 405 a drain current corresponding to the gate voltage Vgs.

[0079] FIG. 20B shows a timing chart of the scan lines G1 to Gv and the power supply lines V1 to Vv in each period. When it is supposed that pixels of one row have a scan line in common, the writing period Ta appears in sequence in each row. Each writing period Ta is included in the corresponding reverse bias period Tr. It is to be noted that the writing period Ta and the reverse bias period Tr can be overlapped with each other completely. However, by setting the reverse bias period Tr longer than the writing period Ta, it is possible to prevent noise and the like due to fluctuation of the potential of the power supply lines V1 to Vv.

[0080] Differently from the pixel shown in Fig. 2, timing of the reverse bias period Tr can be set for each row in the pixel shown in Fig. 4. Therefore, the proportion that the display period Td occupies on each frame period can be increased, and thus, the operating frequency of the driver circuit can be suppressed.

[0081] In Fig. 20A, an example of timing of the writing period, the reverse bias period and the display period is shown in the case of using an analog video signal, however, a digital video signal may be used in the invention as well. For example, in the case where time gray scale display is achieved by the use of a digital video signal, the writing period Ta, the reverse bias period Tr and the display period Td may be provided for each bit of the digital signal as shown in Fig. 7B.

[0082] FIG. 5A shows a configuration of a light emitting device which comprises the pixel portion 401 shown in FIG. 4 and driver circuits. In FIG. 5A, reference numeral 405 denotes a signal line driver circuit for supplying a video signal to the signal lines S1 to Sx, and 406 denotes a scan line driver circuit for controlling potentials of the scan lines G1 to Gv and the power supply lines V1 to Vv.

[0083] FIG. 5B shows a part of the signal line driver circuit 405. The signal line driver circuit 405 comprises a shift register 410, an inverter 411 for inverting a signal outputted from the shift register 410, and a transmission gate which samples a video signal in synchronism with the signal outputted from the shift register 410 and the inverted signal outputted from the inverter 411 and supplies the video signal to the signal lines S1 to Sx.

[0084] FIG. 5C shows a part of the scan line driver circuit 406. The scan line driver circuit 406 comprises a shift register 415, inverters 416 and 417 for inverting a signal outputted from the shift register 415, and a NOR circuit which controls a pulse width of an inverted signal outputted from the inverter 416 depending on a pulse width control signal and supplies the inverted signal to the scan lines G1 to Gv. A signal outputted from the inverter 417 is supplied to the power supply lines V1 to Vv.

[0085] According to the aforementioned configuration, the scan lines G1 to Gv and the power supply lines V1 to Vy can be controlled by a single scan line driver circuit 406.

Embodiment 2

[0086] Described in this embodiment is a pixel configuration of a light emitting device capable of adopting the driving method of the invention.

[0087] A pixel shown in FIG. 6A comprises a light emitting element 601, a switching TFT 602, a driving TFT 603, an erasing TFT 604 for forcibly stopping light emission of the light emitting element 601, and a capacitor 605. A gate of the switching TFT 602 is connected to a first scan line Gaj (j = 1 to y), either a source or a drain thereof is connected to a signal line Si (i = 1 to x), and the other thereof is connected to a gate of the driving TFT 603. Either a source or a drain of the driving TFT 603 is connected to a power supply line Vj (j = 1 to y) and the other thereof is connected to an anode of a light emitting element 601. A gate of the erasing TFT 604 is connected to a second scan line Gbj (j = 1 to y), either a source or a drain thereof is connected to the gate of the driving TFT 603, and the other thereof is connected to the anode of the light emitting element 601. One of two electrodes of the capacitor 605 is connected to the anode of the light emitting element 601 and the other thereof is connected to the gate of the driving TFT 603.

[0088] The erasing TFT 604 is OFF in a writing period Ta. Then, the erasing TFT 604 is turned ON when a forward bias voltage is applied to the driving TFT 603 and the light emitting element 601 which are connected in series with each other. As a result, a gate voltage Vgs of the driving TFT 603 can be made equal to 0, the driving TFT 603 is turned OFF, and light emission of the light emitting element 601 is forcibly stopped. Thus, a display period is completed.

[0089] A pixel shown in FIG. 6B comprises a light emitting element 611, a switching TFT 612, a driving TFT 613, an erasing TFT 614 for forcibly stopping light emission of the light emitting element 611, and a capacitor 615. A gate of the switching TFT 612 is connected to the first scan line Gaj (j = 1 to y), either a source or a drain thereof is connected to the signal line Si (i = 1 to x), and the other thereof is connected to a gate of the driving TFT 613. The driving TFT 613 and the erasing TFT 614 are connected in series with each other between the power supply line Vj (j = 1 to y) and the light emitting element 611. Specifically, either a source or a drain of the driving TFT 613 is connected to an anode of the light emitting element 611, and either a source or a drain of the erasing TFT 614 is connected to the power supply line Vj. A gate of the erasing TFT 614 is connected to the second scan line Gbj (j = 1 to y). One of two electrodes of the capacitor 615
is connected to the anode of the light emitting element 611 and the other thereof is connected to the gate of the driving TFT 613.

[0090] It is to be noted that although the erasing TFT 614 is provided between the driving TFT 613 and the power supply line Vj in FIG. 63, the invention is not limited to this arrangement of the erasing TFT 614. For example, the erasing TFT 614 may be provided between the light emitting element 611 and the driving TFT 613. In that case, specifically, either the source or the drain of the driving TFT 614 is connected to the power supply line Vj, and either the source or the drain of the erasing TFT 614 is connected to the anode of the light emitting element 611. Then, one of the two electrodes of the capacitor 615 is connected to the gate of the driving TFT 613, and the other thereof is connected to either the source or the drain of the driving TFT 613, which is not connected to the power supply line Vj.

[0091] The erasing TFT 614 is ON in a reverse bias period Tr and a display period Td. Then, the erasing TFT 614 is turned OFF when a forward bias voltage is applied to the driving TFT 613, the erasing TFT 614 and the light emitting element 611, which are connected in series with each other. As a result, light emission of the light emitting element 611 is forcibly stopped and the display period Td can be completed.

[0092] FIG. 7C shows timing of the writing period Ta, the reverse bias period Tr, the display period Td, and an erasing period Te which appears by forcibly stopping light emission of the light emitting element, in the case where time gray scale display is achieved in the pixels shown in FIGS. 6A and 6B by the use of a digital video signal. As shown in FIG. 7C, the erasing period Te allows the display period Tr to be forcibly completed from the first row in which the writing period Ta is completed, before completing the writing period Ta in all the rows. Accordingly, gray scale levels can be increased without reducing the writing period, leading to suppressed operating frequency of the driver circuit.

[0093] Note that in the case of the pixel shown in FIG. 6A, the erasing TFT 604 may be ON all the time in the erasing period Te, or it may be turned ON at the beginning of the erasing period Te and may be OFF in the rest of the period. On the other hand, in the case of the pixel shown in FIG. 6B, the erasing TFT 604 is ON all the time in the erasing period Te.

[0094] FIG. 6C shows a pixel configuration in which a diode connected TFT is added between an anode of a light emitting element and a power supply line in the pixel shown in FIG. 2. A pixel shown in FIG. 6C comprises a light emitting element 621, a switching TFT 622, a driving TFT 623, a capacitor 624, and a rectifying TFT 625. A gate of the switching TFT 622 is connected to the scan line Gj (j=1 to y), either a source or a drain thereof is connected to the signal line Si (i=1 to x), and the other thereof is connected to a gate of the driving TFT 623. Either a source or a drain of the driving TFT 623 is connected to the power supply line Vj (i=1 to x) and the other thereof is connected to an anode of the light emitting element 621. A gate of the rectifying TFT 625 is connected to the anode of the light emitting element 621, either a source or a drain thereof is connected to the power supply line Vj, and the other is connected to the anode of the light emitting element 621.

[0095] In a reverse bias period, the source of the rectifying TFT 625 is connected to the power supply line Vj, and the gate and the drain thereof are connected to each other. Accordingly, the rectifying TFT 625 is turned ON and a forward bias current is supplied, thus, a potential of the anode of the light emitting element 621 becomes closer to that of the power supply line Vj. Meanwhile, in a display period, the drain of the rectifying TFT 625 is connected to the power supply line Vj, and the gate and the source thereof are connected to each other. Therefore, a reverse bias voltage is applied to the rectifying TFT 625, and the rectifying TFT 625 is thus turned OFF. According to such a configuration, in the pixel shown in FIG. 6C, a potential of the anode of the light emitting element 621 can be made close to that of the power supply line Vj sooner even when a drain current of the driving TFT 623 is low, in the case where an image is displayed with low level gray scale by the use of an analog video signal.

[0096] FIG. 6D shows a pixel configuration in which a diode connected TFT is added between an anode of a light emitting element and a power supply line in the pixel shown in FIG. 6A. A pixel shown in FIG. 6D comprises a light emitting element 631, a switching TFT 632, a driving TFT 633, a capacitor 634, an erasing TFT 635, and a rectifying TFT 636. A gate of the switching TFT 632 is connected to the first scan line Gaj (j=1 to y), either a source or a drain thereof is connected to the signal line Si (i=1 to x), and the other thereof is connected to a gate of the driving TFT 633. Either a source or a drain of the driving TFT 633 is connected to the power supply line Vj (j=1 to y) and the other thereof is connected to an anode of the light emitting element 631. A gate of the erasing TFT 635 is connected to the second scan line Gbj (j=1 to y), either a source or a drain thereof is connected to the gate of the driving TFT 633, and the other thereof is connected to the anode of the light emitting element 631. A gate of the rectifying TFT 636 is connected to the anode of the light emitting element 631, either a source or a drain thereof is connected to the power supply line Vj, and the other thereof is connected to the anode of the light emitting element 631.

[0097] FIG. 6E shows a pixel configuration in which a diode connected TFT is added between an anode of a light emitting element and a power supply line in the pixel shown in FIG. 6B. A pixel shown in FIG. 6E comprises a light emitting element 641, a switching TFT 642, a driving TFT 643, a capacitor 644, an erasing TFT 645, and a rectifying TFT 646. A gate of the switching TFT 642 is connected to the first scan line Gaj (j=1 to y), either a source or a drain thereof is connected to the signal line Si (i=1 to x), and the other thereof is connected to a gate of the driving TFT 643. The driving TFT 643 and the erasing TFT 645 are connected in series with each other. Either a source or a drain of the driving TFT 643 is connected to the power supply line Vj, and either a source or a drain thereof is connected to an anode of the light emitting element 641. A gate of the rectifying TFT 646 is connected to the anode of the light emitting element 641, either a source or a drain thereof is connected to the power supply line Vj, and the other thereof is connected to the anode of the light emitting element 641.

[0098] Although the erasing TFT 645 is provided between the driving TFT 643 and the power supply line Vj in FIG. 6E, the invention is not limited to this arrangement of the erasing TFT 645. For example, it may be provided between the light emitting element 641 and the driving TFT 643. In this case, specifically, either the source or the drain of the driving TFT 643 is connected to the power supply line Vj, and either the source or the drain of the erasing TFT 645 is connected to the anode of the light emitting element 641. Further, one of two electrodes of the capacitor 644 is connected to the gate of the driving TFT 643, and the other thereof is connected to either
the source or the drain of the driving TFT 643, which is not connected to the power supply line Vj.

[0099] The pixel configuration of the light emitting device of the invention is not limited to the ones shown in this embodiment.

**Embodiment 3**

[0100] In the case of using TFTs formed of a semi-amorphous semiconductor (semi-amorphous TFTs) for the light emitting device of the invention, a driver circuit can be integrally formed on the same substrate as a pixel portion. Meanwhile, in the case of using TFTs formed of an amorphous semiconductor (amorphous TFTs), a driver circuit formed on another substrate may be mounted on the same substrate as a pixel portion.

[0101] FIG. 8A shows an example of an element substrate in which a pixel portion 6012 is formed on a substrate 6011 and connected to a signal line driver circuit 6013 formed separately. The pixel portion 6012 and scan line driver circuits 6014 are formed by using semi-amorphous TFTs. The signal line driver circuit 6013 is formed of transistors which exhibit a higher mobility than the semi-amorphous TFTs. As a result, it is possible to stabilize the operation of the signal line driver circuit which is required to operate at a higher frequency than the scan line driver circuit. It is to be noted that the signal line driver circuit 6013 may be formed of transistors using a single crystalline semiconductor, TFTs using a polycrystalline semiconductor, or transistors using an SOI. Power supply potentials, various signals and the like are supplied to each of the pixel portion 6012, the signal line driver circuit 6013, and the scan line driver circuits 6014 via an FPC 6015.

[0102] Note that the signal line driver circuit and the scan line driver circuits may be integrally formed on the same substrate as the pixel portion.

[0103] Further, in the case of forming a driver circuit separately, a substrate on which the driver circuit is formed is not necessarily attached on a substrate on which a pixel portion is formed, and may be attached on an FPC, for example. FIG. 8B shows an example of an element substrate in which a pixel portion 6022 and a scan line driver circuit 6024 are formed on a substrate 6021 and connected to a signal line driver circuit 6023 formed separately. The pixel portion 6022 and scan line driver circuits 6024 are formed by using semi-amorphous TFTs. The signal line driver circuit 6023 is connected to the pixel portion 6022 via an FPC 6025. Power supply potentials, various signals and the like are supplied to each of the pixel portion 6022, the signal line driver circuit 6023, and the scan line driver circuit 6024 via the FPC 6025.

[0104] Alternatively, only a part of a signal line driver circuit or a part of a scan line driver circuit may be formed on the same substrate as a pixel portion by using semi-amorphous TFTs, and the rest thereof may be formed separately and connected to the pixel portion electrically. FIG. 8C shows an example of an element substrate in which an analog switch 6033a of a signal line driver circuit is formed on the same substrate 6031 as a pixel portion 6032 and scan line driver circuits 6034, and a shift register 6033b of the signal line driver circuit is formed separately on another substrate and attached on the substrate 6031. The pixel portion 6032 and the scan line driver circuits 6034 are formed of semi-amorphous TFTs. Power supply potentials and various signals and the like are supplied to each of the pixel portion 6032, the signal line driver circuit, and the scan line driver circuits 6034 via an FPC 6035.

[0105] As shown in FIGS. 8A to 8C, according to the invention, apart or the whole of a driver circuit of the light emitting device can be formed on the same substrate as a pixel portion by using semi-amorphous TFTs.

[0106] Moreover, both a signal line driver circuit and a scan line driver circuit may be formed separately and mounted on a substrate on which a pixel portion is formed. FIG. 8D shows an example of an element substrate in which a chip 6043 includes a signal line driver circuit and chips 6044 each including a scan line driver circuit are attached on a substrate 6041 on which a pixel portion 6042 is formed. The pixel portion 6042 is formed of semi-amorphous TFTs or amorphous TFTs. Power supply potentials and various signals are supplied to each of the pixel portion 6042, the chip 6043 including a signal line driver circuit, and the chips 6044 each including a scan line driver circuit via an FPC 6045.

[0107] A connecting method of a separately formed substrate is not exclusively limited, and a known method such as COG, wire bonding, and TAB may be used. In addition, a connecting point is not limited to the ones shown in FIGS. 8A to 8D as far as electrical connection is possible. Further, a controller, a CPU, a memory and the like may be formed separately to be connected.

[0108] The signal line driver circuit used in the invention is not limited to the one including a shift register and an analog switch only. It may comprise other circuits such as a buffer, a level shifter, and a source follower as well as the shift register and the analog switch. The shift register and the analog switch are not necessarily provided. For example, a circuit such as a decoder for selecting a signal line can be used instead of the shift register and a latch or the like can be used instead of the analog switch.

[0109] A mounting method of a chip is not exclusively limited, and a known method such as COG, wire bonding, and TAB may be employed. In addition, a mounting point is not limited to the ones shown in FIGS. 8A to 8D as far as electrical connection is possible. Although the signal line driver circuit and the scan line driver circuit are each formed in a chip in FIGS. 8A to 8D, a controller, a CPU, a memory and the like may be formed in a chip to be mounted. Further, not the whole scan line driver circuit is necessarily formed in a chip, and only a part of the scan line driver circuit may be formed in a chip.

[0110] According to this embodiment, an integrated circuit such as a driver circuit is separately formed in a chip and mounted. As a result, the yield can be improved as compared with in the case of integrally forming all the circuits on the same substrate as a pixel portion, and optimization of process can be easily achieved in accordance with characteristics of each circuit.

**Embodiment 4**

[0111] Described next is a structure of a TFT formed of a semi-amorphous semiconductor, which is used in the light emitting device of the invention. FIG. 9A shows a cross sectional structure of a TFT used for a driver circuit and a TFT used for a pixel portion. Reference numeral 501 corresponds to a cross sectional view of a TFT used for a driver circuit, 502 corresponds to a cross sectional view of a TFT used for a pixel portion, and 503 corresponds to a cross sectional view of a
light emitting element to which the TFT 502 supplies a current. The TFTs 501 and 502 are inverted staggered (bottom gate) TFTs.

The TFT 501 of the driver circuit comprises a gate electrode 510 formed on a substrate 500, a gate insulating layer 511 formed so as to cover the gate electrode 510, and a first semiconductor layer 512 which is formed of a semi-amorphous semiconductor film and overlapped with the gate electrode 510 with the gate insulating layer 511 interposed therebetween. The TFT 501 further comprises a pair of second semiconductor layers 513 each of which functions as either a source region or a drain region, and third semiconductor layers 514 formed between the first semiconductor layer 512 and the second semiconductor layers 513.

Although the gate insulating layer 511 is formed of two insulating layers in FIG. 9A, the invention is not limited to this. The gate insulating layer 511 may be formed of a single insulating layer or three or more insulating layers.

The second semiconductor layers 513 are formed of an amorphous semiconductor film or a semi-amorphous semiconductor film, and added with an impurity which imparts one conductivity. The pair of second semiconductor layers 513 are opposed to each other with a channel forming region of the first semiconductor layer 512 interposed therebetween.

The third semiconductor layers 514 are formed of an amorphous semiconductor film or a semi-amorphous semiconductor film, and has the same conductivity as the second semiconductor layers 513 and a lower conductivity than the second semiconductor layers 513. Since the third semiconductor layers 514 function as LDD regions, they grade the electric field concentrated at ends of the second semiconductor layers 513 which function as drain regions, leading to prevention of a hot carrier effect. The third semiconductor layers 514 are not necessarily provided, however, a high voltage TFT can be achieved as well as an improved reliability by providing the third semiconductor layers 514.

In the case where the TFT 501 is an N-type transistor, an N-type conductivity can be obtained when forming the third semiconductor layers 514 without adding an impurity which imparts an N-type conductivity. Therefore, in the case of using an N-type transistor for the TFT 501, an impurity which imparts an N-type conductivity is not necessarily added to the third semiconductor layers 514. However, an impurity which imparts a P-type conductivity is added to the first semiconductor layer 512 for forming a channel region, so that the conductivity is as close to I-type as possible.

Wirings 515 are formed so as to cover the pair of third semiconductor layers 514.

The TFT 502 of the pixel portion comprises a gate electrode 520 formed on the substrate 500, the gate insulating layer 511 formed so as to cover the gate electrode 520, and a first semiconductor layer 522 which is formed of a semi-amorphous semiconductor film and overlapped with the gate electrode 520 with the gate insulating layer 511 interposed therebetween. The TFT 502 further comprises a pair of second semiconductor layers 523 each of which functions as either a source region or a drain region, and third semiconductor layers 524 formed between the first semiconductor layer 522 and the second semiconductor layers 523.

The second semiconductor layers 523 are formed of an amorphous semiconductor film or a semi-amorphous semiconductor film, and an impurity which imparts one conductivity is added thereto. The pair of second semiconductor layers 523 are opposed to each other with a channel forming region of the first semiconductor layer 522 interposed therebetween.

The third semiconductor layers 524 are formed of an amorphous semiconductor film or a semi-amorphous semiconductor film, and has the same conductivity as the second semiconductor layers 523 and a lower conductivity than the second semiconductor layers 523. Since the third semiconductor layers 524 function as LDD regions, they grade the electric field concentrated at ends of the second semiconductor layers 523 which function as drain regions, leading to prevention of a hot carrier effect. The third semiconductor layers 524 are not necessarily provided, however, a high voltage TFT can be achieved as well as an improved reliability by providing the third semiconductor layers 524. In the case where the TFT 502 is an N-type transistor, an N-type conductivity can be obtained when forming the third semiconductor layers 524 without adding an impurity which imparts an N-type conductivity. Therefore, in the case of using an N-type transistor for the TFT 502, an impurity which imparts an N-type conductivity is not necessarily added to the third semiconductor layers 524. However, an impurity which imparts a P-type conductivity is added to the first semiconductor layer 522 for forming a channel region, so that the conductivity is as close to I-type as possible.

Wirings 525 are formed so as to cover the pair of third semiconductor layers 524.

A first passivation layer 540 and a second passivation layer 541 are formed of insulating films so as to cover the TFTs 501 and 502 and the wirings 515 and 525. The number of passivation layers for covering the TFTs 501 and 502 is not limited to two, and a single layer or three or more layers may be used. For example, the first passivation layer 540 may be formed of silicon nitride and the second passivation layer 541 may be formed of silicon oxide. The passivation layers formed of silicon nitride or silicon oxide can prevent the TFTs 501 and 502 from degrading due to moisture and oxygen.

Either of the wirings 525 is connected to an anode 530 of the light emitting element 503. An electro luminescent layer 531 is formed on the anode 530, and a cathode 532 is formed on the electro luminescent layer 531.

When the first semiconductor layers 512 and 522 each including a channel forming region are formed by using a semi-amorphous semiconductor, a TFT which exhibits a higher mobility than a TFT using an amorphous semiconductor can be achieved. As a result, the driver circuit and the pixel portion can be integrally formed on the same substrate.

Described next is a structure of a TFT included in the light emitting device of the invention, which is different from the one shown in FIG. 9A. FIG. 9B shows a cross sectional structure of a TFT used for a driver circuit and a TFT used for a pixel portion. Reference numeral 301 corresponds to a cross sectional view of a TFT used for a driver circuit, 302 corresponds to a cross sectional view of a TFT used for a pixel portion, and 303 corresponds to a cross sectional view of a light emitting element 303 to which the TFT 302 supplies a current.

The TFT 301 of the driver circuit and the TFT 302 of the pixel portion comprise gate electrodes 310 and 320 formed on a substrate 300, a gate insulating layer 311 formed so as to cover the gate electrodes 310 and 320, and first semiconductor layers 312 and 322 which are formed of a semi-amorphous semiconductor film and overlapped with the gate electrodes 310 and 320 with the gate insulating layer 311.
interposed therebetween, respectively. Channel protective layers 330 and 331 formed of insulating films are formed so as to cover channel forming regions of the first semiconductor layers 312 and 322, respectively. The channel protective layers 330 and 331 are provided in order to prevent the channel forming regions of the first semiconductor layers 312 and 322 from being etched during manufacturing steps of the TFTs 301 and 302, respectively. The TFTs 301 and 302 further comprise pairs of second semiconductor layers 313 and 323 each of which functions as either a source region or a drain region, and third semiconductor layers 314 and 324 formed between the first semiconductor layers 312 and 322 and the second semiconductor layers 313 and 323, respectively.

Although the gate insulating layer 311 is formed of two insulating layers in FIG. 9B, the invention is not limited to this. The gate insulating layer 311 may be formed of a single insulating layer or three or more insulating layers. The second semiconductor layers 313 and 323 are formed of an amorphous semiconductor film or a semi-amorphous semiconductor film, and an impurity which imparts one conductivity is added thereto. The pairs of second semiconductor layers 313 and 323 are opposed to each other with channel forming regions of the first semiconductor layers 312 and 322 interposed therebetween.

The third semiconductor layers 314 and 324 are formed of an amorphous semiconductor film or a semi-amorphous semiconductor film, and have the same conductivity as the second semiconductor layers 313 and 323 and a lower conductivity than the second semiconductor layers 313 and 323. Since the third semiconductor layers 314 and 324 function as LDD regions, they grade the electric field concentrated at ends of the second semiconductor layers 313 and 323 which function as drain regions, leading to prevention of a hot carrier effect. The third semiconductor layers 314 and 324 are not necessarily provided, however, a high voltage TFT can be achieved as well as an improved reliability by providing the third semiconductor layers 314 and 324. In the case where the TFTs 301 and 302 are N-type transistors, an N-type conductivity can be obtained when forming the third semiconductor layers 314 and 324 without adding an impurity which imparts an N-type conductivity. Therefore, in the case of using N-type transistors for the TFTs 301 and 302, an impurity which imparts an N-type conductivity is not necessarily added to the third semiconductor layers 314 and 324. However, an impurity which imparts a P-type conductivity is added to the first semiconductor layers 312 and 322 for forming channel regions, so that the conductivity is as close to L-type as possible.

Wiring layers 315 and 325 are formed so as to cover the pairs of third semiconductor layers 314 and 324.

A first passivation layer 340 and a second passivation layer 341 are formed of insulating films so as to cover the TFTs 301 and 302 and the wiring layers 315 and 325. The number of passivation layers for covering the TFTs 301 and 302 is not limited to two, and a single layer or three or more layers may be used. For example, the first passivation layer 340 may be formed of silicon nitride and the second passivation layer 341 may be formed of silicon oxide. The passivation layers formed of silicon nitride or silicon oxide can prevent the TFTs 301 and 302 from degrading due to moisture and oxygen.

Either of the wiring layers 325 is connected to an anode 350 of the light emitting element 303. An electro luminescent layer 351 is formed on the anode 350, and a cathode 352 is formed on the electroluminescent layer 351.

When the first semiconductor layers 312 and 322 each including a channel forming region are formed by using a semi-amorphous semiconductor, a TFT which exhibits a higher mobility than a TFT using an amorphous semiconductor can be achieved. As a result, the driver circuit and the pixel portion can be integrally formed on the same substrate.

Described in this embodiment is the case where the driver circuit and the pixel portion of the light emitting device are integrally formed on the same substrate by using TFTs including a semi-amorphous semiconductor, though the invention is not limited to this. After a pixel portion is formed of TFTs using a semi-amorphous semiconductor, a driver circuit formed separately may be attached on a substrate on which the pixel portion is formed. Further, the first semiconductor layer including a channel may be formed of an amorphous semiconductor. In this case, however, a pixel portion is formed of TFTs using an amorphous semiconductor, and then a driver circuit formed separately is attached on a substrate on which the pixel portion is formed.

Embodiment 5

Described next is a pixel configuration included in the light emitting device of the invention. FIG. 10A shows an example of a circuit diagram of a pixel, and FIG. 10B shows an example of a cross sectional structure of the pixel corresponding to FIG. 10A.

In FIGS. 10A and 10B, reference numeral 221 denotes a switching TFT for controlling a video signal input to the pixel, and 222 denotes a driving TFT for controlling a current supply to a light emitting element 223. Specifically, a drain current is controlled by a video signal inputted to the pixel via the switching TFT 221, and the drain current is supplied to the light emitting element 223. Reference numeral 224 denotes a capacitor for holding a gate voltage of the driving TFT 222 when the switching TFT 221 is OFF, and the capacitor 224 is not necessarily provided.

More specifically, a gate electrode of the switching TFT 221 is connected to a scan line Cj (j=1 to y), either a source region or a drain region thereof is connected to a signal line Si (i=1 to x), and the other thereof is connected to a gate electrode of the driving TFT 222. Either a source region or a drain region of the driving TFT 222 is connected to a power supply line Vi (i=1 to x) and the other thereof is connected to an anode 225 of the light emitting element 223. One of two electrodes of the capacitor 224 is connected to the gate electrode of the driving TFT 222 and the other thereof is connected to the anode 225 of the light emitting element 223.

In FIGS. 10A and 10B, the switching TFT 221 adopts a multi-gate structure in which a plurality of TFTs, which are connected in series and gate electrodes thereof are connected to each other, have a first semiconductor layer in common. By adopting the multi-gate structure, OFF current of the switching TFT 221 can be reduced. Although the switching TFT 221 has a structure in which two TFTs are connected in series with each other in FIGS. 10A and 10B, the invention can be applied to a multi-gate structure in which three or more TFTs are connected in series with each other and gate electrodes thereof are connected to each other. Further, the switching TFT 221 does not necessarily have a multi-gate structure, and a TFT of a single gate structure including a single gate electrode and channel forming region may also be employed.
Embodiment 6

[0138] A manufacturing method of the light emitting device of the invention is next described in more detail.

[0139] For a substrate 710, a plastic material can be used as well as glass, quartz and the like. Alternatively, an insulating layer may be formed on a metal material such as stainless steel and aluminum in order to obtain the substrate 710. A conductive layer for forming a gate electrode and a gate wiring (scan line) is formed on the substrate 710. For the conductive layer, a metal material such as chrome, molybdenum, titanium, tantalum, tungsten, and aluminum, or an alloy of these materials is used. The conductive layer can be formed by sputtering or vacuum vapor deposition.

[0140] The conductive layer is etched to form gate electrodes 712 and 713. The gate electrodes 712 and 713 preferably have tapered ends so that a first semiconductor layer and a wiring layer are formed thereon. In the case where the conductive layer is formed of an aluminum-based material, a surface thereof is preferably insulated by anodization and the like after the etching step. Although not shown, a wiring layer connected to the gate electrodes can be formed at the same time in this step.

[0141] Subsequently, a first insulating layer 714 and a second insulating layer 715 are formed over the gate electrodes 712 and 713 in order to form gate insulating layers. In this case, it is preferable that the first insulating layer 714 is formed of a silicon oxide film whereas the second insulating layer 715 is formed of a silicon nitride film. These insulating layers can be formed by glow discharge decomposition or sputtering. In particular, in order to form an insulating layer having a high density and a small gate leakage current at a low deposition temperature, a reactive gas mixed with a noble gas element such as argon may be added into the insulating layer.

[0142] A first semiconductor layer 716 is formed over the first insulating layer 714 and the second insulating layer 715. The first semiconductor layer 716 is formed of a semi-amorphous semiconductor (SAS).

[0143] The SAS can be obtained by glow discharge decomposition of a silicon gas. Typically, SiH₄ is used as a silicon gas, though SiH₂, SiH₂Cl₂, SiHCl₃, SiCl₄, SiF₄, or the like may be used as well. The formation of the SAS can be facilitated by using the silicon gas which is diluted by adding a single or a plurality of noble gas elements selected from among hydrogen, hydrogen and helium, argon, krypton, and neon. The silicon gas is preferably diluted with a dilution rate of 10 to 1000. It is needless to say that the reactive production of the film by glow discharge decomposition is performed under reduced pressure, but the pressure may be in the range of about 0.1 to 133 Pa. The power for generating the glow discharge is in the range of 1 to 120 MHz, and more preferably, an RF power in the range of 13 to 60 MHz may be supplied. The substrate is preferably heated at a temperature of 300°C or less, and more preferably, 100 to 200°C.

[0144] The silicon gas may also be mixed with a carbon gas such as CH₄ and C₂H₆, or a germanium gas such as GeH₄ and GeF₄ to set the energy bandwidth in the range of 1.5 to 2.4 eV, or 0.9 to 1.1 eV.

[0145] When an impurity element for controlling valence electrons is not added to the SAS intentionally, the SAS exhibits a small N-type conductivity. This is because oxygen is easily mixed into a semiconductor layer since the glow discharge is performed at a higher power than in the case of forming an amorphous semiconductor.

[0146] When an impurity element which imparts a P-type conductivity is added to the first semiconductor layer including a channel forming region at the same time as or after the deposition, a threshold voltage can be controlled. Typically, boron is used for an impurity element which imparts a P-type conductivity. An impurity gas such as B₂H₆ and BF₃ may be mixed into the silicon gas at a rate of 1 to 1000 ppm. It is preferable that the concentration of boron is 1x10¹⁴ to 6x10¹⁵ atoms/cm².

[0147] Subsequently, a second semiconductor layer 717 and a third semiconductor layer 718 are formed (FIG. 11A). The second semiconductor layer 717 is formed without intentionally adding an impurity element for controlling valence electrons, and is preferably formed of an SAS as the first semiconductor layer 716. The second semiconductor layer 717 is disposed between the first semiconductor layer 716 and a third semiconductor layer 718 having one conductivity and forming a source and a drain, and thereby it functions as a buffer layer. Therefore, the second semiconductor layer 717 is not necessarily provided when the third semiconductor layer 718 has the same conductivity as the first semiconductor layer 716 having a small N-type conductivity. In the case where an impurity element which imparts a P-type conductivity is added to the third semiconductor layer 718 with the intention of controlling a threshold voltage, the second semiconductor layer 717 functions to gradually change the concentration of impurities, leading to a good joint formation. That is, the second semiconductor layer 717 is capable of serving as a lightly doped impurity region (LDI region) formed between a channel forming region and a source or a drain region in a TFT to be obtained.

[0148] The third semiconductor layer 718 having one conductivity may be added with phosphorous as a typical impurity element when forming an N-channel TFT. Specifically, an impurity gas such as PH₃ may be mixed into the silicon gas. The third semiconductor layer 718 having one conductivity can be formed of an SAS or an amorphous semiconductor as long as valence electrons can be controlled.

[0149] As set forth above, the forming steps from the first insulating layer 714 to the third semiconductor layer 718 having one conductivity can be sequentially performed without exposing them to the atmosphere. Accordingly, each layer can be formed while not contaminating each surface thereof with atmospheric elements or impurity elements existing in the atmosphere, leading to reduced variations in characteristics of TFTs.

[0150] Next, masks 719 are formed by using a photo resist. Then, the first semiconductor layer 716, the second semiconductor layer 717, and the third semiconductor layer 718 having one conductivity are etched to be patterned like islands (FIG. 11B).

[0151] A second conductive layer 720 is formed thereafter to form a wiring connected to the source and the drain. The second conductive layer 720 is formed of aluminum or an aluminum-based conductive material. Alternatively, the second conductive layer 720 may have a laminated structure in which a layer having contact with the semiconductor layer is formed of titanium, tantalum, molybdenum, tungsten, copper, or nitrides of these elements. For example, it is possible that the first layer is formed of Ta and the second layer is formed of W, the first layer is formed of TaN and the second layer is formed of Al, the first layer is formed of TaN and the second layer is formed of Cu, or the first layer is formed of Ti, the second layer is formed of Al, and the third layer is formed
of Ti. Either the first layer or the second layer may be formed of an AgPdCu alloy. Further, W, an alloy of Al and Si (Al—Si), and TiN may be sequentially laminated as well. Tungsten nitride may be used instead of W, an alloy of Al and Ti (Al—Ti) may be substituted for the alloy of Al and Si (Al—Si), or Ti may be used instead of TiN. Aluminum may be added with 0.5 to 5 atom % of an element such as titanium, silicon, scandium, neodymium, and copper in order to improve the heat resistance (FIG. 11C).

[0152] Subsequently, a mask 721 is formed. The mask 721 is patterned to form wirings connected to the source and the drain, and is also used as an etching mask for forming a channel forming region by removing the third semiconductor layer 718 having one conductivity. The conductive layer formed of aluminum or aluminum-based material may be etched by the use of chloride gas such as BCl₃ and Cl₂. This etching process provides wirings 723 to 726. The channel forming region is formed by etching by the use of fluoride gas such as SF₆, NF₃, and CF₄. In this case, it is not possible to have etch selectivity relative to first semiconductor layers 716a and 716b which are to be used as base layers, therefore, processing time has to be adjusted appropriately. In this manner, a channel etched TFT can be obtained (FIG. 12A).

[0153] Next, a third insulating layer 727 for protecting the channel forming region is formed of a silicon nitride film. The silicon nitride film can be formed by sputtering or glow discharge decomposition, and is required to have a high density in order to block out pollutants in the atmosphere such as organic materials, metals, and moisture. By using the silicon nitride film for the third insulating layer 727, the concentration of oxygen in the first semiconductor layer 716 can be lowered to 5×10¹⁷ atoms/cm³ or less, more preferably 1×10¹⁹ atoms/cm³ or less. When the silicon nitride film is formed by RF sputtering using silicon as a target, the use of a sputtering gas in which a noble gas element such as argon is mixed with nitrogen promotes the higher density of the silicon nitride film. On the other hand, when the silicon nitride film is formed by glow discharge decomposition, the silicon nitride film is obtained by diluting a silicon gas by 100 to 500 times with a noble gas element such as argon. Thus, the silicon nitride film is capable of having a high density at a low temperature of 100°C or less. Further, a fourth insulating layer 728 formed of a silicon oxide film may be laminated on the third insulating layer 727 as needed. The third insulating layer 727 and the fourth insulating layer 728 correspond to passivation layers.

[0154] A planarizing layer 729 is formed on the third insulating layer 727 and/or the fourth insulating layer 728. The planarizing layer 729 is preferably formed of an organic resin such as acrylic, polyimide, and polyamide, or a silicone-based insulating film having a Si—O bond and a Si—CFx bond. As these materials are hydrous, a sixth insulating layer 730 is preferably formed as a barrier film for preventing moisture absorption and release. The aforementioned silicon nitride film may be employed for the sixth insulating layer 730 (FIG. 12B).

[0155] A wiring 732 is formed after a contact hole is formed through the sixth insulating layer 730, the planarizing layer 729, the third insulating layer 727, and the fourth insulating layer 728 (FIG. 12C).

[0156] The channel etched TFT formed in this manner, whose channel forming region is formed of an SAS, has a field effect mobility of 2 to 10 cm²/V·sec.

[0157] Next, an anode 731 is formed on the sixth insulating layer 730 so as to be in contact with the wiring 732. For the anode 731, a transparent conductive film in which indium oxide is mixed with zinc oxide (ZnO) of 2 to 20% may be used as well as ITO, IZO, or ITSO. Alternatively, a titanium nitride film or a titanium film may also be used for the anode 731. In this case, after forming a transparent conductive film, a titanium nitride film or a titanium film is formed so as to be thin enough to transmit light (preferably, about 5 to 30 nm). In FIG. 13A, ITO is used for the anode 731. The anode 731 may be polished by CMP or by cleaning with porous body of polyvinyl alcohols so that the surface thereof is made flat. Further, the surface of the anode 731 may be processed with oxygen plasma or exposed to ultraviolet radiation after the polishing by CMP.

[0158] As shown in FIG. 13A, a bank 733 is formed over the sixth insulating layer 730 by using an organic resin film, an inorganic resin film or a siloxane-based material. Note that siloxane is a material which has a backbone structure formed by bonding of silicon (Si) and oxygen (O), and comprises at least hydrogen in its constituent. In addition, siloxane may also comprise one or more elements selected from fluoride, alkyl group, and aromatic hydrocarbon in its constituent. The bank 733 includes an opening portion at which the anode 731 is exposed. Then, as shown in FIG. 13B, an electro luminescent layer 734 is formed so as to be in contact with the anode 731 in the opening portion of the bank 733. The electro luminescent layer 734 may be formed of a single layer or a plurality of layers. In the case where the electro luminescent layer 734 has a laminated structure, a hole injection layer, a hole transporting layer, an electron transporting layer, and an electron injection layer are laminated in this order on the anode 731.

[0159] Subsequently, a cathode 735 is formed so as to cover the electro luminescent layer 734. The cathode 735 can be formed of a known material having a low work function, such as Ca, Al, CaF, MgAg, and AlLi. The anode 731, the electro luminescent layer 734 and the cathode 735 are overlapped with each other in the opening portion of the bank 733 to form a light emitting element 736.

[0160] Actually, when the light emitting device is completed up to the steps shown in FIGS. 13A and 13B, it is preferably sealed with a protective film (laminate film, ultraviolet curable resin film or the like) or a cover material which has high airtightness and less degasification, in order not to expose it to the atmosphere.

[0161] An element substrate in which both a pixel portion and a driver circuit are made up of the same type of TFTs can be formed by using five masks: a gate electrode forming mask, a semiconductor region forming mask, a wiring forming mask, a contact hole forming mask, and an anode forming mask.

[0162] Although the driver circuit and the pixel portion of the light emitting device are formed on the same substrate by using TFTs including a semi-amorphous semiconductor in this embodiment, the invention is not limited to this. The pixel portion may be formed of TFT using an amorphous semiconductor, and a driver circuit separately formed may be attached on a substrate on which the pixel portion is formed.

[0163] FIGS. 11A to 11C, FIGS. 12A to 12C, and FIGS. 13A and 13B show the manufacturing method of a TFT having the structure shown in FIG. 9A, though a TFT having the structure shown in FIG. 9B can be manufactured similarly. However, the TFT shown in FIG. 9B is different from that shown in FIGS. 11A to 11C, FIGS. 12A to 12C, and FIG. 13A and 13B in that the channel protective layers 330 and 331
are formed over the first semiconductor layers 312 and 322 including an SAS so as to be overlapped with the gate electrodes 310 and 320, respectively.

[0164] In FIGS. 12A and 12B, after forming a contact hole in the third insulating layer (first passivation layer) and the fourth insulating layer (second passivation layer), an anode and a bank are formed. The bank may be formed of an organic resin such as acrylic, polyimide, and polyamide, or a siloxane-based insulating film having a Si—O bond and a Si—CHx bond. In particular, an opening portion is preferably formed on the anode by using a photosensitive material so that side walls of the opening portion have a continuous curvature.

Embodiment 7

[0165] Described in this embodiment is an example of a top plan view of the pixel shown in FIGS. 10A and 10B.

[0166] FIG. 14 is a top plan view of a pixel of this embodiment. Si, Vi, and Gj correspond to a signal line, a power supply line, and a scan line respectively. In this embodiment, the signal line Si and the power supply line Vi are formed of the same conductive layer. The scan line Gj and a wiring 250 are also formed of the same conductive layer. A part of the scan line Gj functions as a gate electrode of the switching TFT 221. A part of the wiring 250 functions as a gate electrode of the driving TFT 222 and another part thereof functions as a first electrode of the capacitor 224. A part 251 of an active layer of the driving TFT 222, which is on a side of an anode 225, functions as a second electrode of the capacitor 224. The capacitor 224 is formed of the part 251 of the active layer at the anode 225 side, a part of the wiring 250, and a gate insulating layer (not shown). Reference numeral 225 denotes the anode, and light is emitted in an overlapping area (light emitting area) of the anode 225, an electro luminescent layer and a cathode (both not shown).

[0167] It is needless to say that the top plan view shown in this embodiment is just an example and the invention is not limited to this

Embodiment 8

[0168] An N-type transistor is used for a semi-amorphous TFT or an amorphous TFT used in the light emitting device of the invention. Described in this embodiment is a cross sectional structure of a pixel taking an N-type driving TFT as an example.

[0169] FIG. 15A is a cross sectional view of a pixel in which an N-type driving transistor 7001 is used and light from a light emitting element 7002 is emitted in the direction of a cathode 7003. In FIG. 15A, an electro luminescent layer 7004 and the cathode 7003 are laminated in this order on an anode 7005 which is electrically connected to the driving TFT 7001. The anode 7005 is preferably formed of a material which transmits light with difficulty, and for example, titanium nitride or titanium can be employed. The electro luminescent layer 7004 may be formed of either a single layer or a plurality of layers. The cathode 7003 may be formed of a known material as long as it is a conductive film having a low work function. For example, Ca, Al, CaF, MgAg, AlLi or the like is desirably used, however, it is formed so as to be thin enough to transmit light (preferably, about 5 to 30 nm). Al having a thickness of 20 nm may be utilized as the cathode 7003, for instance. Then, a transparent conductive layer 7007 is formed so as to cover the cathode 7003. For the transparent conductive layer 7007, a transparent conductive film in which indium oxide is mixed with zinc oxide (ZnO) of 2 to 20% may be used as well as ITO, IZO, or ITSO.

[0170] An overlapping area of the cathode 7003, the electro luminescent layer 7004 and the anode 7005 corresponds to a light emitting element 7002. In the case of the pixel shown in FIG. 15A, light from the light emitting element 7002 is emitted in the direction of the cathode 7003 as shown by an outline arrow.

[0171] FIG. 15B is a cross sectional view of a pixel in which an N-type driving transistor 7011 is used and light from a light emitting element 7012 is emitted in the direction of a cathode 7013. In FIG. 15A, an electro luminescent layer 7014 and the cathode 7013 are laminated in this order on an anode 7015 which is electrically connected to the driving TFT 7011. The anode 7015 is formed of a transparent conductive film which transmits light, and for example, a transparent conductive film in which indium oxide is mixed with zinc oxide (ZnO) of 2 to 20% may be used as well as ITO, IZO, or ITO. The electro luminescent layer 7014 may be formed of either a single layer or a plurality of layers as in FIG. 15A. The cathode 7013 may be formed of a known material as long as it is a conductive film which has a low work function as in FIG. 15A, and reflects light.

[0172] An overlapping area of the anode 7015, the electro luminescent layer 7014, and the cathode 7013 corresponds to a light emitting element 7012. In the case of the pixel shown in FIG. 15B, light from the light emitting element 7012 is emitted in the direction of the anode 7015 as shown by an outline arrow.

[0173] FIG. 15C is a cross sectional view of a pixel in which an N-type driving TFT 7021 is used and light from a light emitting element 7022 is emitted in both the directions of an anode 7025 and a cathode 7023. In FIG. 15C, an electro luminescent layer 7024 and the cathode 7023 are laminated in this order on the anode 7025 which is electrically connected to the driving TFT 7021. The anode 7025 can be formed of a transparent conductive film which transmits light as in FIG. 15B, and the electro luminescent layer 7024 may be formed of either a single layer or a plurality of layers as in FIG. 15A. The cathode 7023 may be formed of a known material as long as it is a conductive film having a low work function, however, it is formed so as to be thin enough to transmit light. For example, Al having a thickness of 20 nm can be used as the cathode 7023.

[0174] An overlapping area of the cathode 7023, the electro luminescent layer 7024, and the anode 7025 corresponds to a light emitting element 7022. In the case of the pixel shown in FIG. 15C, light from the light emitting element 7022 is emitted in both the directions of the anode 7025 and the cathode 7023 as shown by an outline arrow.

[0175] Although the driving TFT is electrically connected to the light emitting element in this embodiment, other TFTs may be connected in series between the driving TFT and the light emitting element.

[0176] Note that in all the pixels shown in FIGS. 15A to 15C, a protective layer may be formed so as to cover the light emitting element. The protective layer is formed of a film which transmits a substance such as moisture and oxygen with difficulty as compared with other insulating films in order to prevent such a substance from being absorbed in the light emitting element and accelerating deterioration of the light emitting element. Typically, for example, a DLC film, a silicon nitride film, a silicon oxide film formed by RF sput-
tering are desirably used. It is also possible to use for the protective layer a laminated layer of a layer which transmits the moisture, the oxygen and the like with difficulty and a layer which transmits the moisture, the oxygen and the like with ease.

[0177] In order to obtain light from the cathode side in FIGS. 15B and 15C, ITO which is added with Li to lower the work function may be used instead of reducing the film thickness of the cathode.

[0178] The light emitting device of the invention is not limited to the structures shown in FIGS. 15A to 15C, and various changes based on the scope of the invention are possible.

Embodiment 9

[0179] Described in this embodiment is an example of a shift register using TFTs all of which has the same conductivity. A configuration of a shift register of this embodiment is shown in FIG. 16A. The shift register shown in FIG. 16A operates in accordance with a first clock signal CLK, a second clock signal CLKb, and a start pulse signal SP. Reference numeral 1401 denotes a pulse output circuit, and a specific configuration thereof is shown in FIG. 16B.

[0180] The pulse output circuit 1401 comprises TFTs 801 to 806 and a capacitor 807. A gate of the TFT 801 is connected to a node 2, a source thereof is connected to a gate of the TFT 805, and a drain thereof is supplied with a potential Vdd. A gate of the TFT 802 is connected to a gate of the TFT 806, a drain thereof is connected to the gate of the TFT 805, and a drain thereof is supplied with a potential Vss. A gate of the TFT 803 is connected to a node 3, a source thereof is connected to the gate of the TFT 806, and a drain thereof is supplied with the Vdd. A gate of the TFT 804 is connected to the node 2, a drain thereof is connected to the gate of the TFT 805, and a source thereof is supplied with the Vss. A gate of the TFT 805 is connected to one electrode of the capacitor 807, a drain thereof is connected to the node 1, and a source thereof is connected to the other electrode of the capacitor 807 and a node 4. A gate of the TFT 806 is connected to one electrode of the capacitor 807, a drain thereof is connected to the node 4, and a source thereof is supplied with the Vss. It is further assumed for simplicity that the Vss is equal to 0.

[0181] When the SP reaches H level, the TFT 801 is turned ON, and thus, a gate potential of the TFT 805 starts to rise. At the last, the TFT 801 is turned OFF and brought into a floating state when the gate potential of the TFT 805 becomes equal to Vdd−Vth (Vth is a threshold voltage of the TFTs 801 to 806). On the other hand, when the SP reaches H level, the TFT 804 is turned ON. As a result, gate potentials of the TFTs 802 and 806 drop to the Vss and the TFTs 802 and 806 are turned OFF. A gate potential of the TFT 803 is L level at this time and the TFT 803 is OFF.

[0182] Then, the SP becomes L level, the TFTs 801 and 804 are turned OFF, and thus the gate potential of the TFT 805 is maintained equal to Vdd−Vth. In the case where a gate-source voltage of the TFT 805 is higher than the threshold voltage Vth, the TFT 805 is turned ON.

[0183] Subsequently, when the CLK supplied to the node 1 is changed from L level to H level, the node 4, namely a source voltage of the TFT 805 starts to rise since the TFT 805 is ON. The gate and the source of the TFT 805 are capacitively coupled due to the capacitor 807, therefore, the gate potential of the TFT 805 which is in a floating state starts to rise again as the potential of the node 4 is increased. At the last, the gate potential of the TFT 805 becomes higher than Vdd−Vth, and the potential of the node 4 becomes equal to the Vdd. The aforementioned operation is performed similarly in the subsequent stages of the pulse output circuit 1401, and a pulse is outputted in sequence.

Embodiment 10

[0185] In this embodiment, an exterior of a panel which is one mode of the light emitting device of the invention is described with reference to FIGS. 17A and 17B. FIG. 17A is a top plan view of a panel in which a TFT and a light emitting element are formed on a first substrate and sealed with a sealing member interposed between the first substrate and a second substrate. FIG. 17B is a cross sectional view taken by cutting along a line A-A' of FIG. 17A.

[0186] Sealing members 4005 are provided so as to surround a pixel portion 4002 and a scan line driver circuit 4004 which are formed on a first substrate 4001. A second substrate 4006 is formed over the pixel portion 4002 and the scan line driver circuit 4004. Accordingly, the pixel portion 4002 and the scan line driver circuit 4004 as well as a filling member 4007 are sealed with the first substrate 4001, the sealing members 4005, and the second substrate 4006. In an area on the first substrate 4001, which is different from the area surrounded by the sealing members 4005, a signal line driver circuit 4003 is formed on another substrate by using a polycrystalline semiconductor is mounted. In this embodiment, a signal line driver circuit formed of TFTs using a polycrystalline semiconductor is mounted on the first substrate 4001, however, a signal line driver circuit may be formed of a single crystalline semiconductor and mounted on the first substrate 4001. In FIG. 17B, a TFT 4009 formed of a polycrystalline semiconductor is shown as an example of a TFT included in the signal line driver circuit 4003.

[0187] The pixel portion 4002 and the scan line driver circuit 4004 formed on the first substrate 4001 comprise a plurality of TFTs, and a TFT 4010 included in the pixel portion 4002 is shown as an example in FIG. 17B. Note that, it is assumed in this embodiment that the TFT 4010 is a driving TFT. The TFT 4010 corresponds to a TFT using a semiconductor.

[0188] Reference numeral 4011 corresponds to a light emitting element, and a pixel electrode of the light emitting element 4011 is electrically connected to a drain of the TFT 4010 via a wiring 4017. In this embodiment, a counter electrode of the light emitting element 4011 and a transparent conductive layer 4012 are electrically connected to each other. The structure of the light emitting element 4011 is not limited to the one shown in this embodiment. It may be changed arbitrarily depending on the direction of light emitted from the light emitting element 4011 and the conductivity of the TFT 4010.

[0189] Although not shown in the cross sectional view of FIG. 17B, various signals and potentials are supplied from a connecting terminal 4016 from the signal line driver circuit 4003 formed separately and the scan line driver circuit 4004 or the pixel portion 4002 via lead wirings 4014 and 4015.

[0190] In this embodiment, the connecting terminal 4016 is formed of the same conductive layer as the pixel electrode of the light emitting element 4011. The lead wiring 4014 is
formed of the same conductive layer as the wiring 4017. Further, the lead wiring 4015 is formed of the same conductive layer as a gate electrode of the TFT 4010.

0191 The connecting terminal 4016 is electrically connected to a terminal of an FPC 4018 via an anisotropic conductive layer 4019.

0192 For the first substrate 4001 and the second substrate 4006, glass, metal (typically, stainless), ceramics, or plastic may be employed. As a plastic material, an FRP (Fiberglass-Reinforced Plastic) board, a PVF (Polyvinyl Fluoride) film, a mylar film, a polyester film, or an acrylic resin film may be used. Alternatively, an aluminum foil sandwiched between PVF films or mylar films may also be employed.

0193 However, for the substrate which is in the direction to which light from the light emitting element is emitted, a light transmitting material is used such as a glass board, a plastic board, a polyester film, and an acryl film.

0194 For the filling member 4007, an ultraviolet curable resin or a heat-curable resin may be used as well as an inert gas such as nitrogen and argon. These resins include PCV (Polyvinyl Chloride), acryl, polyimide, epoxy resin, silicon resin, PVB (Polyvinyl Butyral), and EVA (Ethylene Vinyl Acetate). In this embodiment, nitrogen is used as the filling member 4007.

0195 Although the signal line driver circuit 4003 is formed separately and mounted on the first substrate 4001 in Fig. 17, the invention is not limited to this configuration. The scan line driver circuit may be formed separately and mounted, or only a part of the signal line driver circuit or a part of the scan line driver circuit may be formed separately and mounted.

0196 In this embodiment mode, the driver circuit and the pixel portion of the light emitting device are formed on the same substrate by using TFTs including a semi-amorphous semiconductor. However, the invention is not limited to this configuration. The pixel portion may be formed by using TFTs including an amorphous semiconductor and the driver circuit formed separately may be mounted on a substrate on which the pixel portion is formed.

0197 This embodiment can be implemented in combination with the configurations described in other embodiments.

Embodiment 11

0198 A light emitting device using a light emitting element emits light by itself, therefore, it has a high visibility in bright light and a wide viewing angle as compared with a liquid crystal display. Accordingly, it can be applied to display portions of various electronic apparatuses.

0199 The light emitting device of the invention can be applied to various electronic apparatuses such as a video camera, a digital camera, a goggle type display (a head mounted display), a navigation system, an audio reproducing device (an in-car audio system, a component stereo, or the like), a notebook personal computer, a game player, a portable information terminal (a mobile computer, a mobile phone, a portable game player, an electronic book, or the like), and an image reproducing device provided with a recording medium (specifically, a device which is capable of reproducing a recording medium such as DVD (Digital Versatile Disk) and which includes a display for displaying the reproduced image). In particular, the light emitting device of the invention is desirable for a portable electronic apparatus whose screen is often seen from an oblique direction and which requires a wide viewing angle. Further, according to the invention, a crystallization step after forming a semiconductor layer is not needed and thus a large panel can be formed with relative ease. Therefore, the light emitting device of the invention is so useful in forming electronic apparatuses which use a large panel having a size of 10 to 50 inches. Specific examples of such electronic apparatuses are shown in FIGS. 18A to 18C.

0200 FIG. 18A shows a display device which includes a housing 2001, a supporting base 2002, a display portion 2003, speaker portions 2004, a video input terminal 2005 and the like. The light emitting device of the invention can be applied to the display portion 2003 to complete the display device of the invention. Since the light emitting device emits light by itself and requires no backlight, the display portion thereof can be made thinner than a liquid crystal display. It is to be noted that the light emitting display device includes all the information display devices such as one used for personal computer, TV broadcast receiving, or advertisement display.

0201 FIG. 18B shows a notebook personal computer which includes a main body 2201, a housing 2202, a display portion 2203, a keyboard 2204, an external connecting port 2205, a pointing mouse 2206 and the like. The light emitting device of the invention can be applied to the display portion 2203 to complete the notebook personal computer of the invention.

0202 FIG. 18C shows a portable image reproducing device provided with a recording medium (specifically, a DVD reproducing device), which includes a main body 2401, a housing 2402, a display portion A 2403, a display portion B 2404, a recording medium (DVD and the like) reading portion 2405, an operating key 2406, a speaker portion 2407 and the like. The display portion A 2403 mainly displays image data whereas the display portion B 2404 mainly displays character data. It is to be noted that the image reproducing device provided with a recording medium includes a home video game player and the like. The light emitting device of the invention can be applied to the display portion A 2403 and the display portion B 2404 to complete the image reproducing device of the invention.

0203 Since light emitting parts consume power in a light emitting device, data is desirably displayed so that the light emitting parts occupy as small an area as possible. Accordingly, in the case where the light emitting device is used for a display portion which mainly displays character data, such as the display of a mobile phone or an audio reproducing device, it is preferably driven so that the character data emits light by using non-light emitting parts as background.

0204 As set forth above, the application range of the invention is so wide that it can be applied to electronic apparatuses of all fields. The electronic apparatuses shown in this embodiment may include the light emitting device having any one of configurations described in Embodiments 1 to 10.

0205 This application is based on Japanese Patent Application serial no. 2003-289569 filed in Japan Patent Office on 8, Aug. 2003, the contents of which are hereby incorporated by reference.

0206 Although the present invention has been fully described by way of Embodiment Modes and Embodiments with reference to the accompanying drawings, it is to be understood that various changes and modifications will be apparent to those skilled in the art. Therefore, unless such changes and modifications depart from the scope of the present invention hereinafter defined, they should be constructed as being included therein.
1. (canceled)
2. A light emitting device comprising:
a scan line;
a first signal line;
a second signal line;
a power supply line;
a first transistor;
a second transistor;
a third transistor;
a fourth transistor;
a first capacitor;
a second capacitor;
a first light emitting element; and
a second light emitting element,
wherein a gate of the first transistor is connected to the scan line,
wherein one of a source and a drain of the first transistor is connected to the first signal line,
wherein the other of the source and the drain of the first transistor is directly connected to a gate of the second transistor,
wherein one of a source and a drain of the second transistor is connected to the first light emitting element,
wherein the other of the source and the drain of the second transistor is directly connected to the power supply line,
wherein a first electrode of the first capacitor is connected to the gate of the second transistor,
wherein a second electrode of the first capacitor is connected to the one of the source and the drain of the second transistor,
wherein a gate of the third transistor is connected to the scan line,
wherein one of a source and a drain of the third transistor is connected to the second signal line,
wherein the other of the source and the drain of the third transistor is directly connected to a gate of the fourth transistor,
wherein one of a source and a drain of the fourth transistor is connected to the second light emitting element,
wherein the other of the source and the drain of the fourth transistor is directly connected to the power supply line,
wherein a first electrode of the second capacitor is connected to the gate of the fourth transistor, and
wherein a second electrode of the second capacitor is connected to the one of the source and the drain of the fourth transistor.
3. The light emitting device according to claim 2, wherein the power supply line is supplied with a pulse signal.
4. The light emitting device according to claim 2, wherein the power supply line is functionally connected to an inverter.
5. An electronic apparatus comprising the light emitting device according to claim 2 and a housing.
6. A light emitting device comprising:
a first line;
a second line;
a third line;
a fourth line;
a first transistor;
a second transistor;
a third transistor;
a fourth transistor;
a first capacitor;
a second capacitor;
a first light emitting element; and
a second light emitting element,
wherein a gate of the first transistor is connected to the first line,
wherein one of a source and a drain of the first transistor is connected to the second line,
wherein the other of the source and the drain of the first transistor is directly connected to a gate of the second transistor,
wherein one of a source and a drain of the second transistor is connected to the first light emitting element,
wherein the other of the source and the drain of the second transistor is directly connected to the fourth line,
wherein a first electrode of the first capacitor is connected to the gate of the second transistor,
wherein a second electrode of the first capacitor is connected to the one of the source and the drain of the second transistor,
wherein a gate of the third transistor is connected to the first line,
wherein one of a source and a drain of the third transistor is connected to the third line,
wherein the other of the source and the drain of the third transistor is directly connected to a gate of the fourth transistor,
wherein one of a source and a drain of the fourth transistor is connected to the second light emitting element,
wherein the other of the source and the drain of the fourth transistor is directly connected to the fourth line,
wherein a first electrode of the second capacitor is connected to the gate of the fourth transistor, and
wherein a second electrode of the second capacitor is connected to the one of the source and the drain of the fourth transistor.
7. The light emitting device according to claim 6, wherein the fourth line is supplied with a pulse signal.
8. The light emitting device according to claim 6, wherein the fourth line is functionally connected to an inverter.
9. An electronic apparatus comprising the light emitting device according to claim 6 and a housing.
10. A light emitting device comprising:
a first line;
a second line;
a third line;
a fourth line;
a fifth line;
a sixth line;
a first transistor;
a second transistor;
a third transistor;
a fourth transistor;
a fifth transistor;
a sixth transistor;
a first capacitor;
a second capacitor;
a third capacitor;
a first light emitting element;
a second light emitting element; and
a third light emitting element,
wherein a gate of the first transistor is connected to the first line,
wherein one of a source and a drain of the first transistor is connected to the second line,
wherein the other of the source and the drain of the first transistor is directly connected to a gate of the second transistor,
wherein one of a source and a drain of the second transistor is connected to the first light emitting element,
wherein the other of the source and the drain of the second transistor is directly connected to the fourth line,
wherein a first electrode of the first capacitor is connected to the gate of the second transistor,
wherein a second electrode of the first capacitor is connected to the one of the source and the drain of the second transistor,
wherein a gate of the third transistor is connected to the first line,
wherein one of a source and a drain of the third transistor is connected to the third line,
wherein the other of the source and the drain of the third transistor is directly connected to a gate of the fourth transistor,
wherein one of a source and a drain of the fourth transistor is connected to the second light emitting element,
wherein the other of the source and the drain of the fourth transistor is directly connected to the fourth line,
wherein a first electrode of the second capacitor is connected to the gate of the fourth transistor,
wherein a second electrode of the second capacitor is connected to the one of the source and the drain of the fourth transistor,
wherein a gate of the fifth transistor is connected to the fifth line,
wherein one of a source and a drain of the fifth transistor is connected to the second line,
wherein the other of the source and the drain of the fifth transistor is directly connected to a gate of the sixth transistor,
wherein one of a source and a drain of the sixth transistor is connected to the third light emitting element,
wherein the other of the source and the drain of the sixth transistor is directly connected to the sixth line,
wherein a first electrode of the third capacitor is connected to the gate of the sixth transistor, and
wherein a second electrode of the third capacitor is connected to the one of the source and the drain of the sixth transistor.

11. The light emitting device according to claim 10, wherein the fourth line is not directly connected to the sixth line.

12. The light emitting device according to claim 10, wherein the fourth line is supplied with a first pulse signal, and
wherein the sixth line is supplied with a second pulse signal.

13. The light emitting device according to claim 10, wherein the fourth line is functionally connected to an inverter.

14. An electronic apparatus comprising the light emitting device according to claim 10 and a housing.