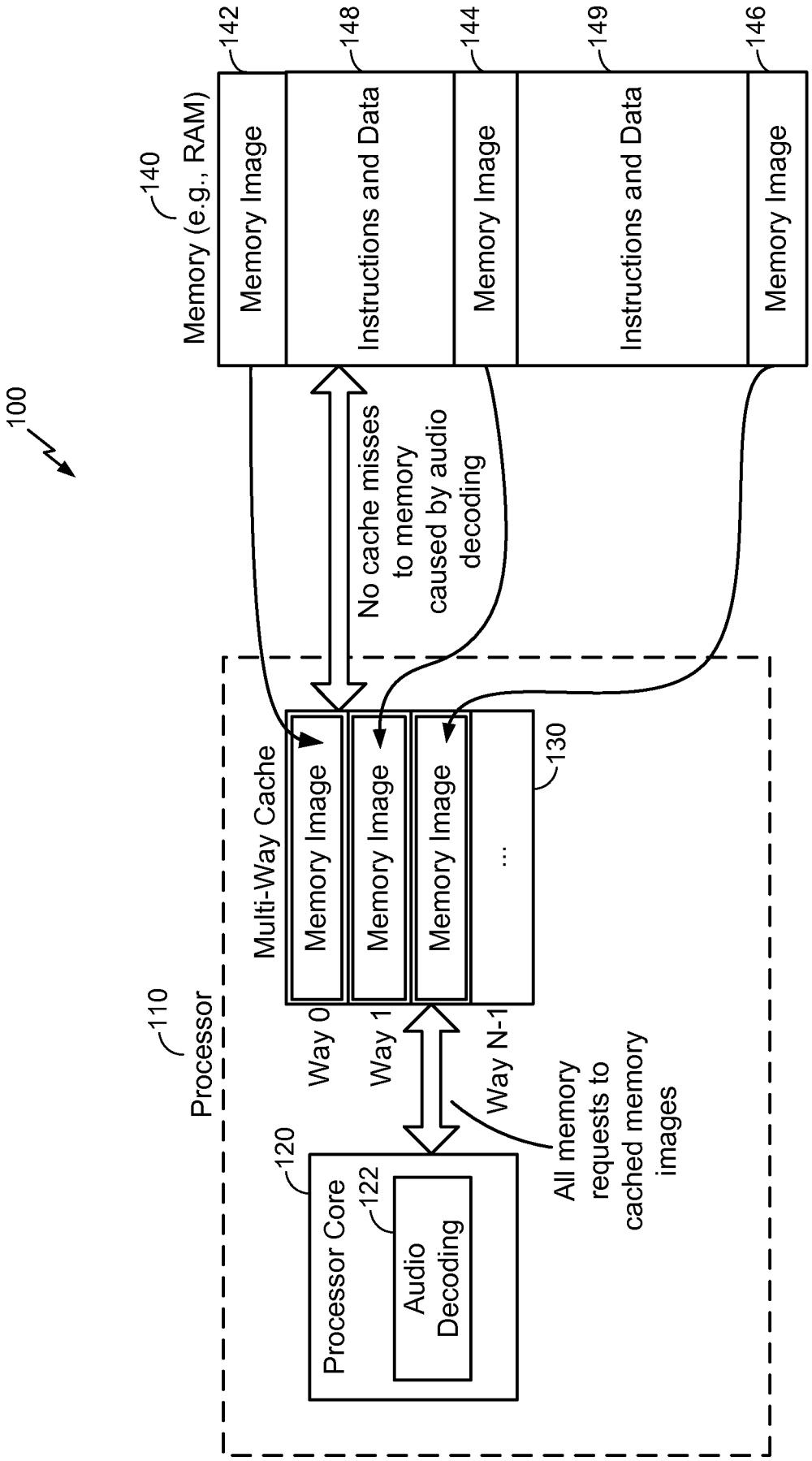
100
140
Memory (e.g., RAM)
142
Memory Image
148
Instructions and Data
144
Memory Image
149
Instructions and Data
146
Memory Image
No cache misses to memory caused by audio decoding
110
Processor
Multi-Way Cache
Memory Image
Memory Image
Memory Image
...
130
Way 0
Way 1
Way N-1
120
Processor Core
122
Audio Decoding
All memory requests to cached memory images

FIG. 1

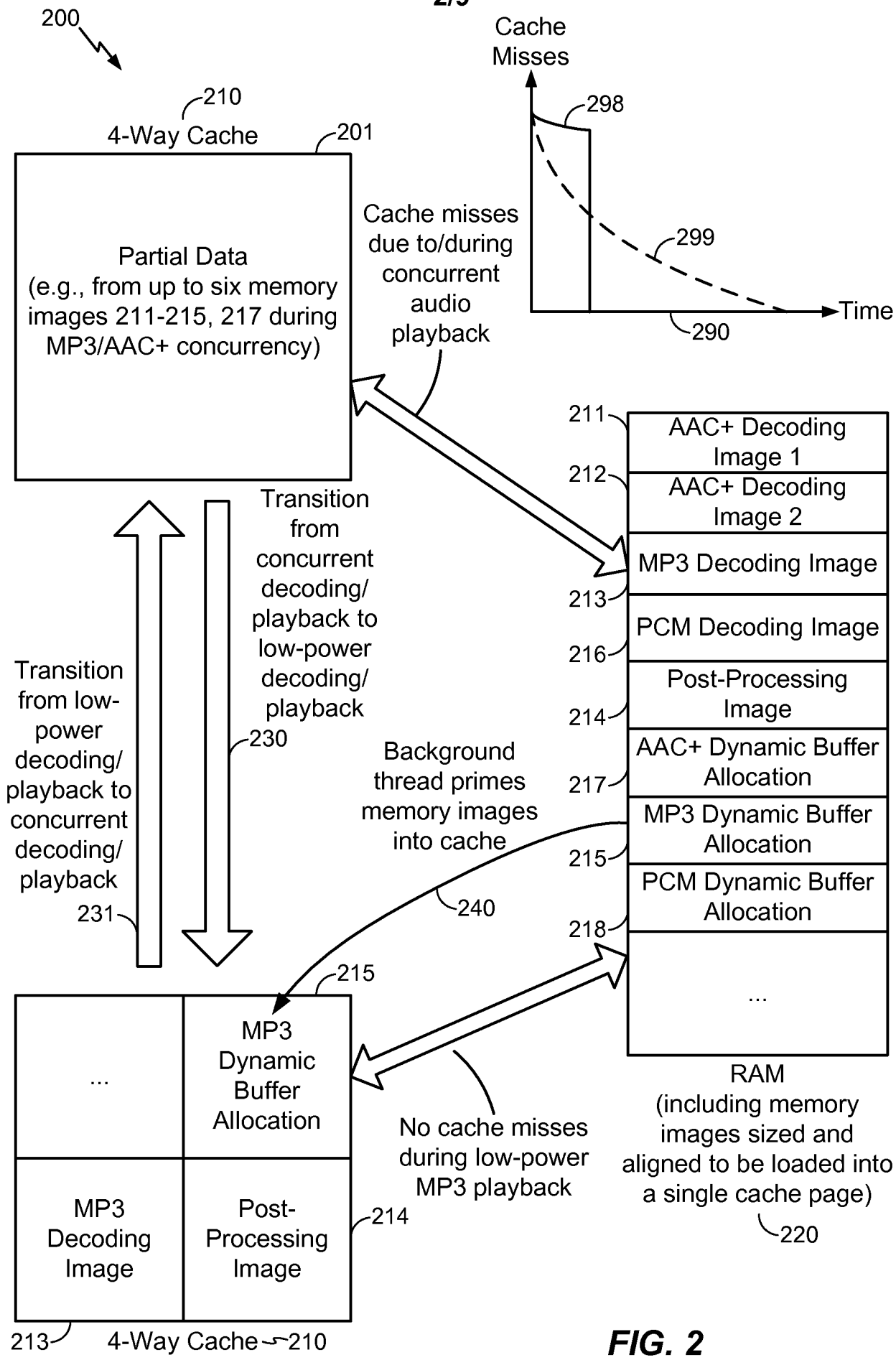
200
210
4-Way Cache
201
Partial Data
(e.g., from up to six memory images 211-215, 217 during MP3/AAC+ concurrency)
Cache Misses
298
299
290
Time
Cache misses due to/during concurrent audio playback
211
AAC+ Decoding Image 1
212
AAC+ Decoding Image 2
MP3 Decoding Image
213
PCM Decoding Image
216
Post-Processing Image
214
AAC+ Dynamic Buffer Allocation
217
MP3 Dynamic Buffer Allocation
215
PCM Dynamic Buffer Allocation
218
...
RAM
(including memory images sized and aligned to be loaded into a single cache page)
220
Transition from concurrent decoding/ playback to low-power decoding/ playback
230
Transition from low-power decoding/ playback to concurrent decoding/ playback
231
Background thread primes memory images into cache
240
No cache misses during low-power MP3 playback
215
...
MP3 Dynamic Buffer Allocation
MP3 Decoding Image
Post-Processing Image
214
213
4-Way Cache
210

FIG. 2

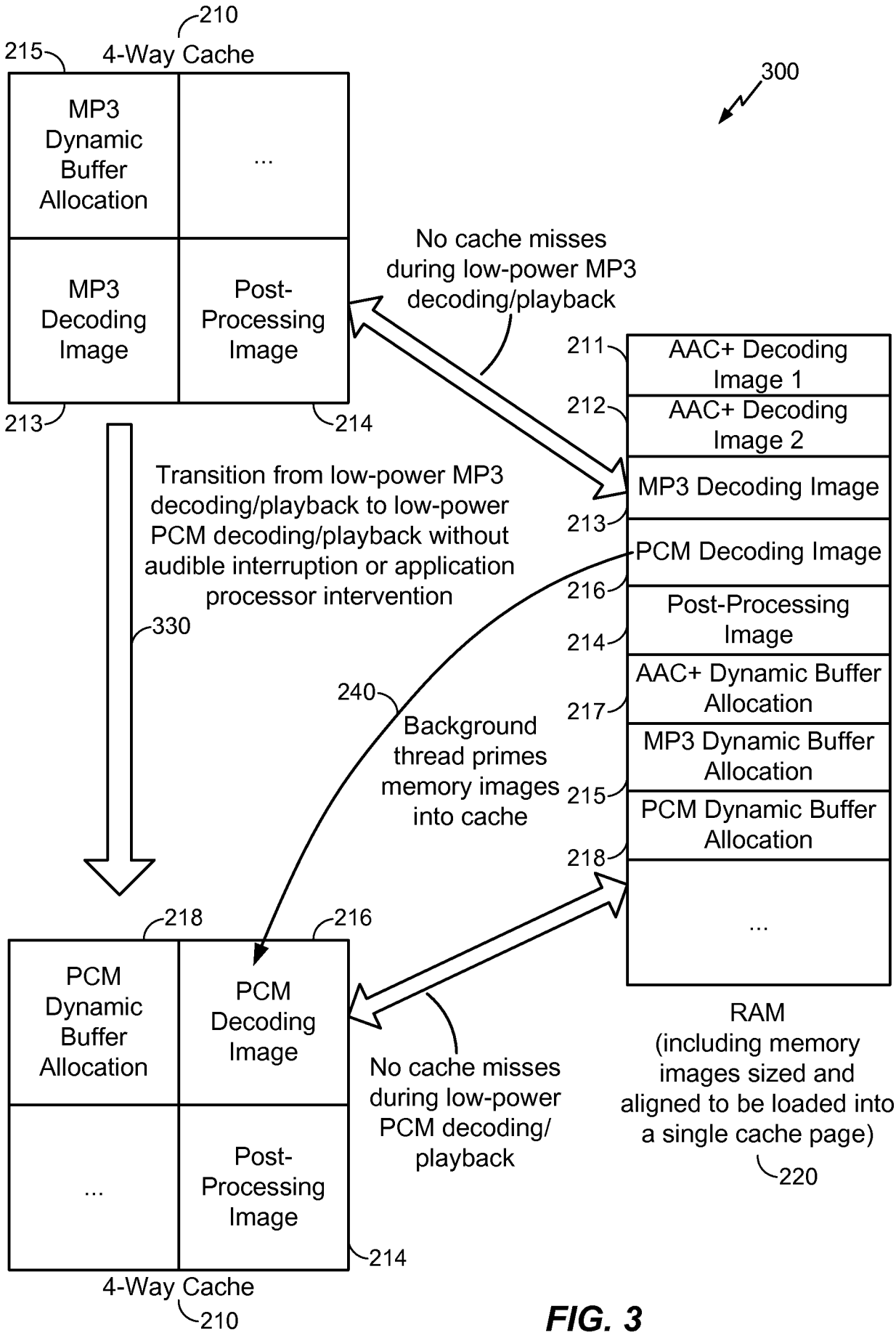
210
4-Way Cache
215
MP3 Dynamic Buffer Allocation
...
MP3 Decoding Image
Post-Processing Image
213
214
300
No cache misses during low-power MP3 decoding/playback
211
AAC+ Decoding Image 1
212
AAC+ Decoding Image 2
MP3 Decoding Image
213
PCM Decoding Image
216
Post-Processing Image
214
AAC+ Dynamic Buffer Allocation
217
MP3 Dynamic Buffer Allocation
215
PCM Dynamic Buffer Allocation
218
...
RAM
(including memory images sized and aligned to be loaded into a single cache page)
220
Transition from low-power MP3 decoding/playback to low-power PCM decoding/playback without audible interruption or application processor intervention
330
240
Background thread primes memory images into cache
218
216
PCM Dynamic Buffer Allocation
PCM Decoding Image
...
Post-Processing Image
214
No cache misses during low-power PCM decoding/playback
4-Way Cache
210

FIG. 3

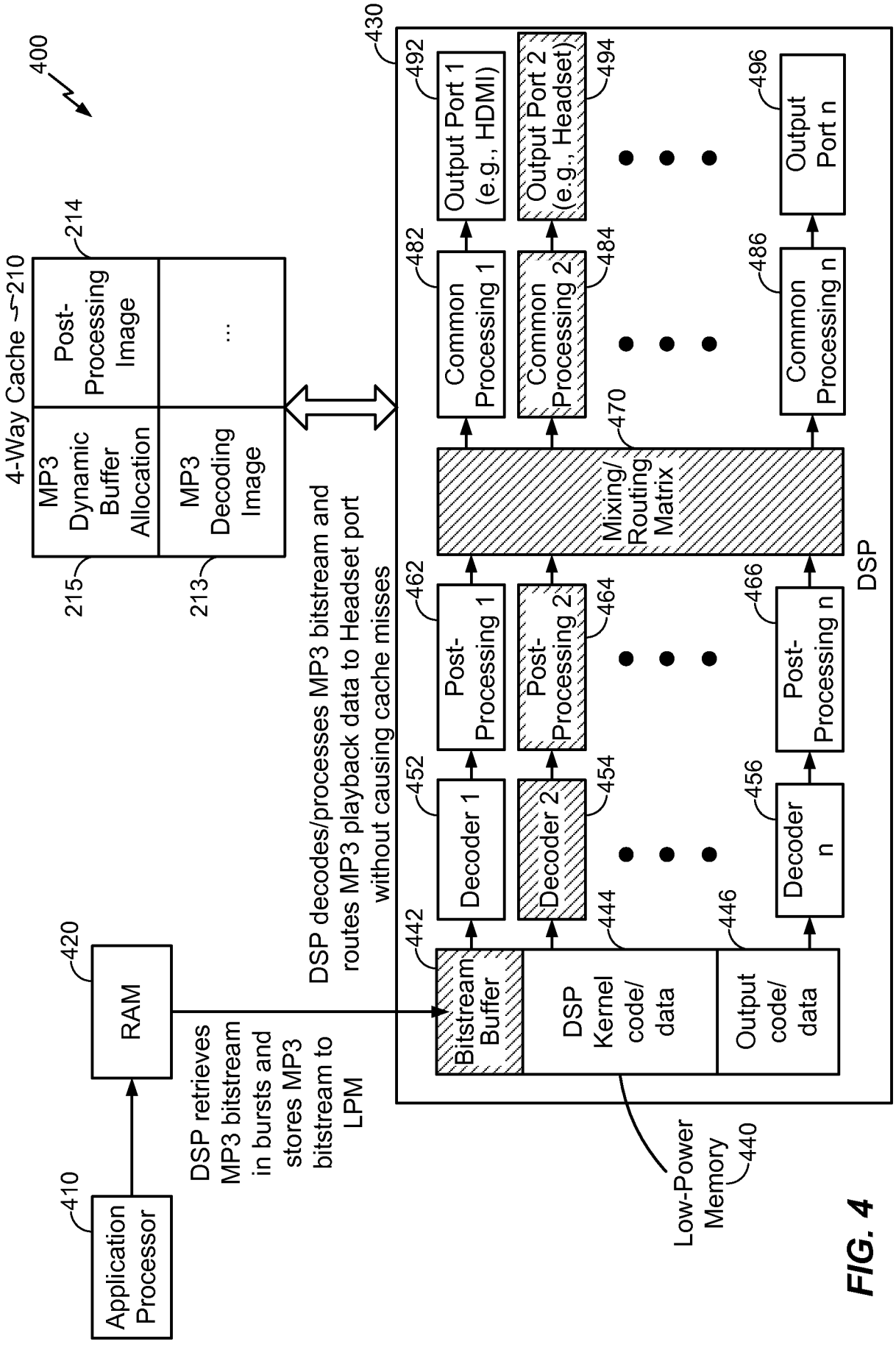
400
4-Way Cache
210
214
Post-Processing Image
...
MP3 Dynamic Buffer Allocation
MP3 Decoding Image
215
213
430
492
Output Port 1 (e.g., HDMI)
494
Output Port 2 (e.g., Headset)
496
Output Port n
482
Common Processing 1
484
Common Processing 2
486
Common Processing n
470
Mixing/ Routing Matrix
462
Post-Processing 1
464
Post-Processing 2
466
Post-Processing n
452
Decoder 1
454
Decoder 2
456
Decoder n
442
Bitstream Buffer
444
DSP Kernel code/ data
446
Output code/ data
DSP
420
RAM
410
Application Processor
DSP retrieves MP3 bitstream in bursts and stores MP3 bitstream to LPM
DSP decodes/processes MP3 bitstream and routes MP3 playback data to Headset port without causing cache misses
Low-Power Memory
440

FIG. 4

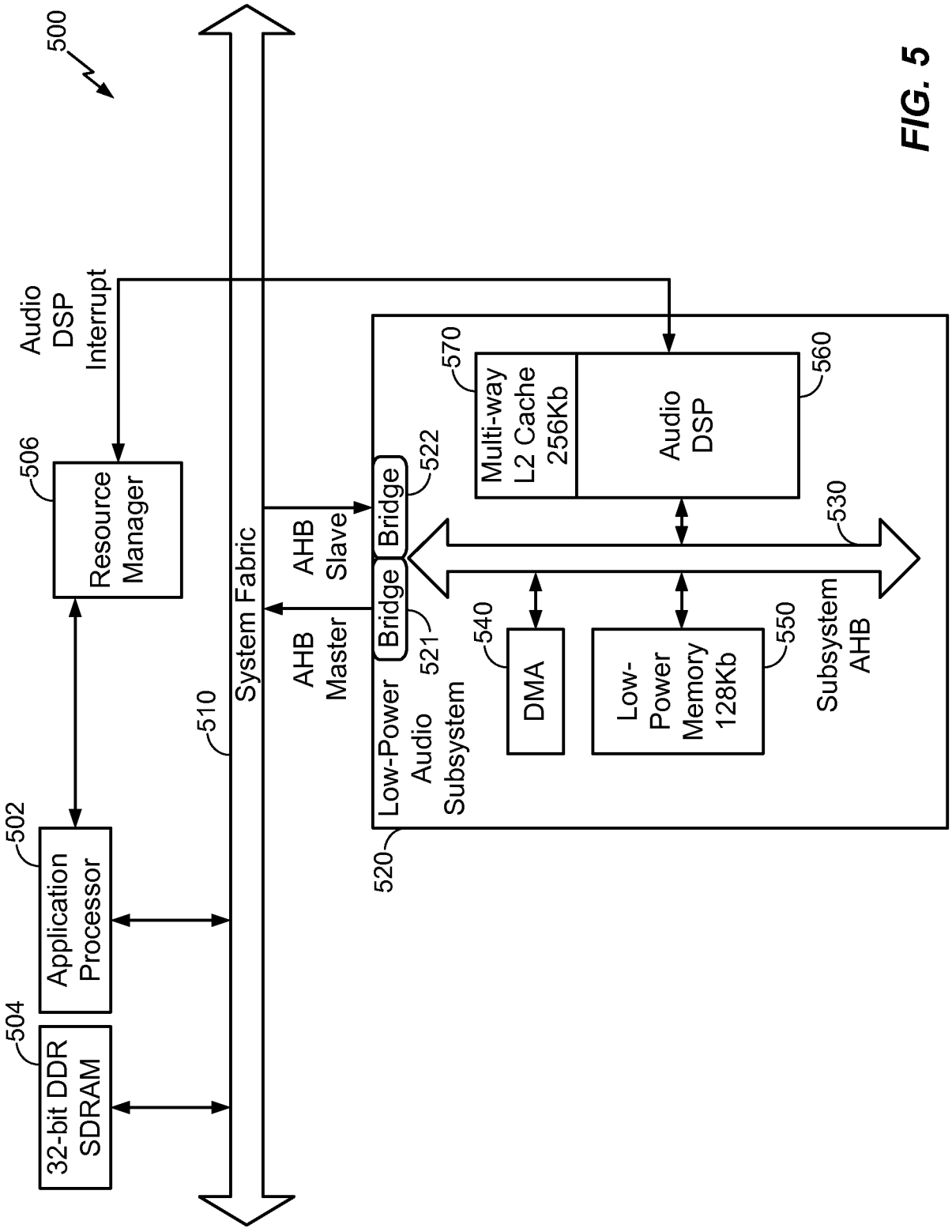
500
Audio DSP Interrupt
506
Resource Manager
502
Application Processor
504
32-bit DDR SDRAM
510
System Fabric
AHB Slave
AHB Master
Bridge
Bridge
522
521
520
Low-Power Audio Subsystem
570
Multi-way L2 Cache 256Kb
560
Audio DSP
530
540
DMA
550
Low-Power Memory 128Kb
Subsystem AHB

FIG. 5

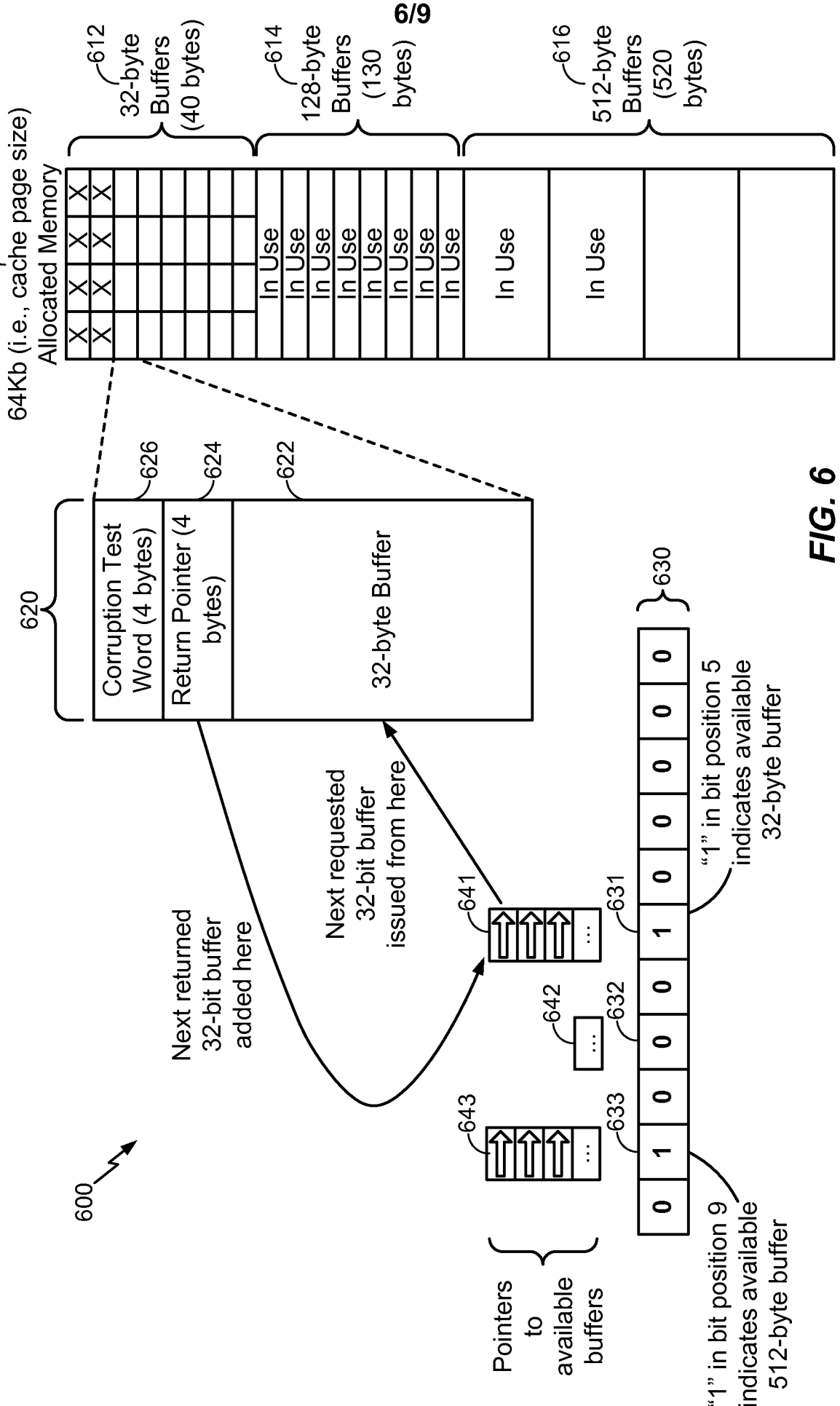
610
64Kb (i.e., cache page size) Allocated Memory
612
32-byte Buffers (40 bytes)
614
128-byte Buffers (130 bytes)
616
512-byte Buffers (520 bytes)
In Use
620
Corruption Test Word (4 bytes)
626
Return Pointer (4 bytes)
624
32-byte Buffer
622
Next returned 32-bit buffer added here
Next requested 32-bit buffer issued from here
641
631
630
642
632
643
633
600
Pointers to available buffers
"1" in bit position 5 indicates available 32-byte buffer
"1" in bit position 9 indicates available 512-byte buffer

FIG. 6

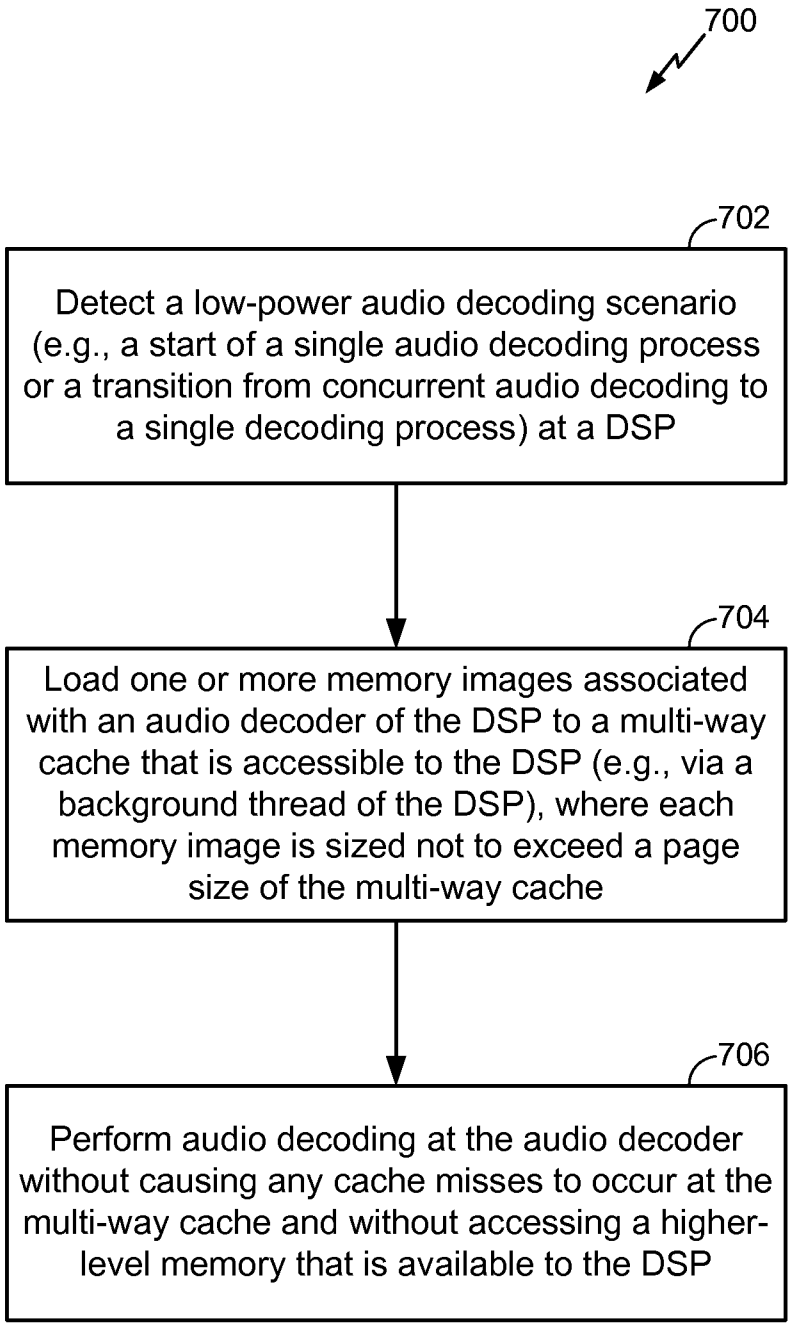
700
702
Detect a low-power audio decoding scenario (e.g., a start of a single audio decoding process or a transition from concurrent audio decoding to a single decoding process) at a DSP
704
Load one or more memory images associated with an audio decoder of the DSP to a multi-way cache that is accessible to the DSP (e.g., via a background thread of the DSP), where each memory image is sized not to exceed a page size of the multi-way cache
706
Perform audio decoding at the audio decoder without causing any cache misses to occur at the multi-way cache and without accessing a higher-level memory that is available to the DSP

FIG. 7

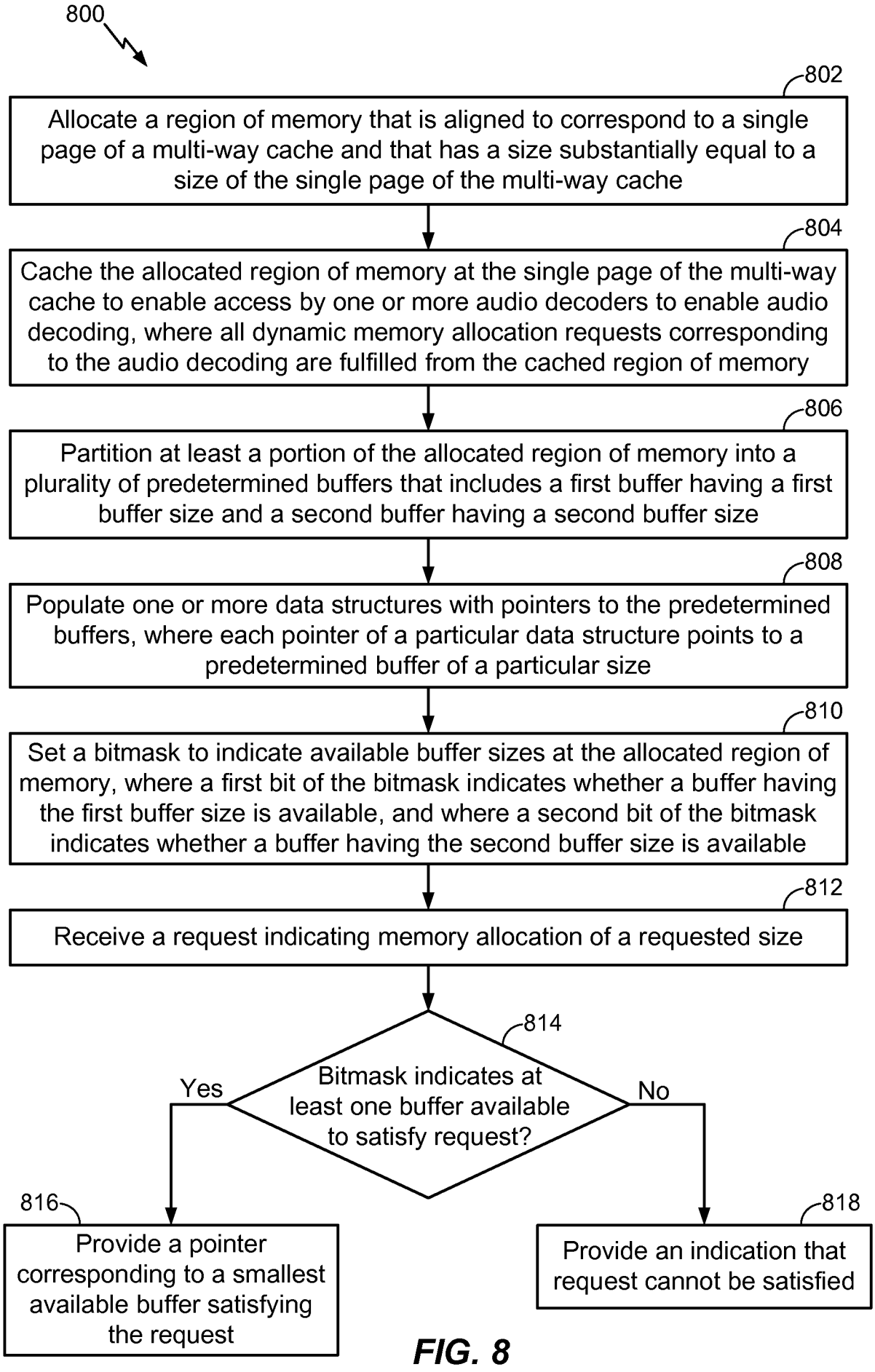
800
802
Allocate a region of memory that is aligned to correspond to a single page of a multi-way cache and that has a size substantially equal to a size of the single page of the multi-way cache
804
Cache the allocated region of memory at the single page of the multi-way cache to enable access by one or more audio decoders to enable audio decoding, where all dynamic memory allocation requests corresponding to the audio decoding are fulfilled from the cached region of memory
806
Partition at least a portion of the allocated region of memory into a plurality of predetermined buffers that includes a first buffer having a first buffer size and a second buffer having a second buffer size
808
Populate one or more data structures with pointers to the predetermined buffers, where each pointer of a particular data structure points to a predetermined buffer of a particular size
810
Set a bitmask to indicate available buffer sizes at the allocated region of memory, where a first bit of the bitmask indicates whether a buffer having the first buffer size is available, and where a second bit of the bitmask indicates whether a buffer having the second buffer size is available
812
Receive a request indicating memory allocation of a requested size
814
Bitmask indicates at least one buffer available to satisfy request?
Yes
No
816
Provide a pointer corresponding to a smallest available buffer satisfying the request
818
Provide an indication that request cannot be satisfied

FIG. 8

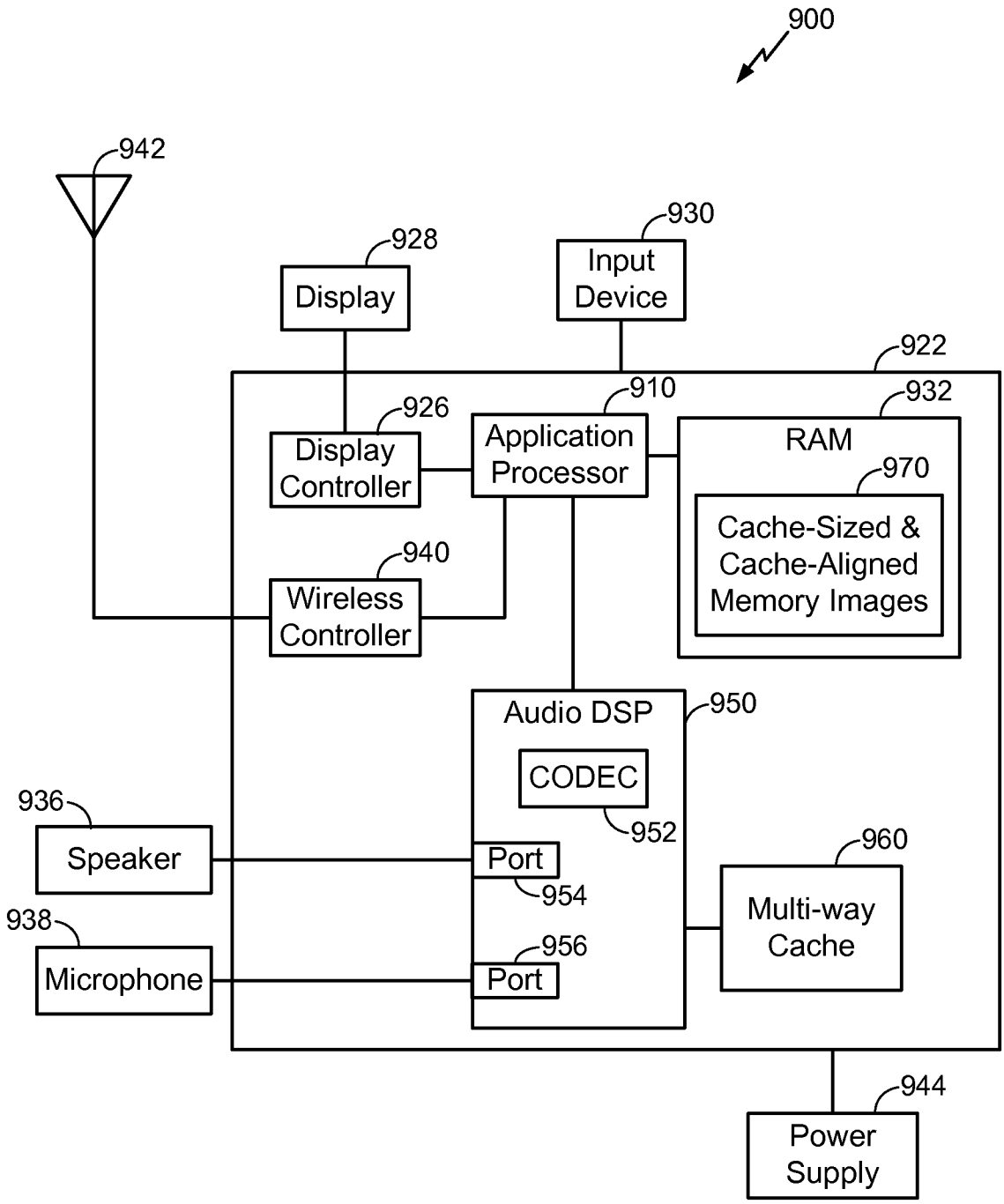
900
942
928
Display
930
Input Device
922
926
Display Controller
910
Application Processor
932
RAM
970
Cache-Sized & Cache-Aligned Memory Images
940
Wireless Controller
Audio DSP
950
CODEC
952
936
Speaker
Port
954
960
Multi-way Cache
938
Microphone
956
Port
944
Power Supply

FIG. 9