

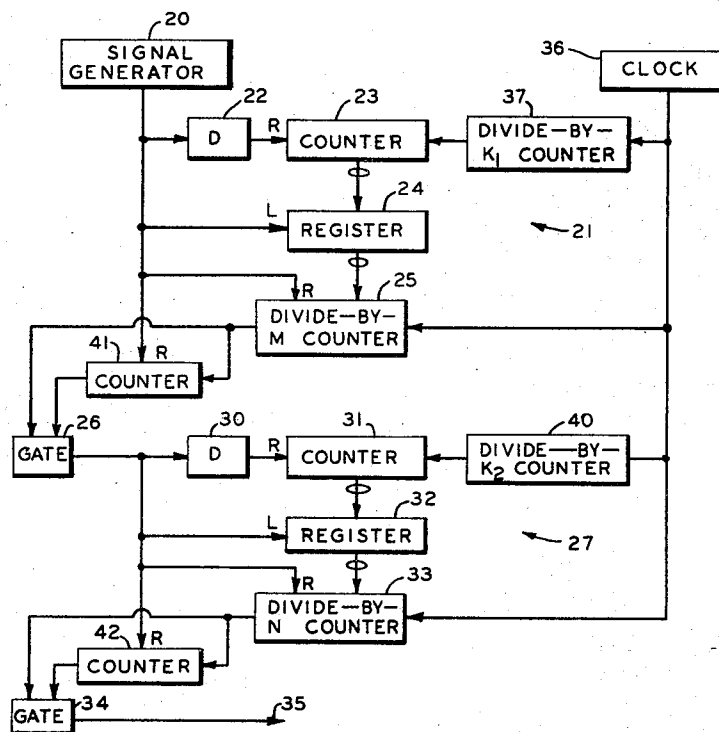
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Primary Examiner—John Zazworsky
Attorney—Norman J. O'Malley et al.

Interpolating apparatus for dividing time intervals of variable duration into an integral number of subintervals is shown wherein the time intervals are divided into a first predetermined number of subintervals each of which are further divided into a second predetermined number of subintervals.

UNITED STATES PATENTS

14 Claims, 2 Drawing Figures



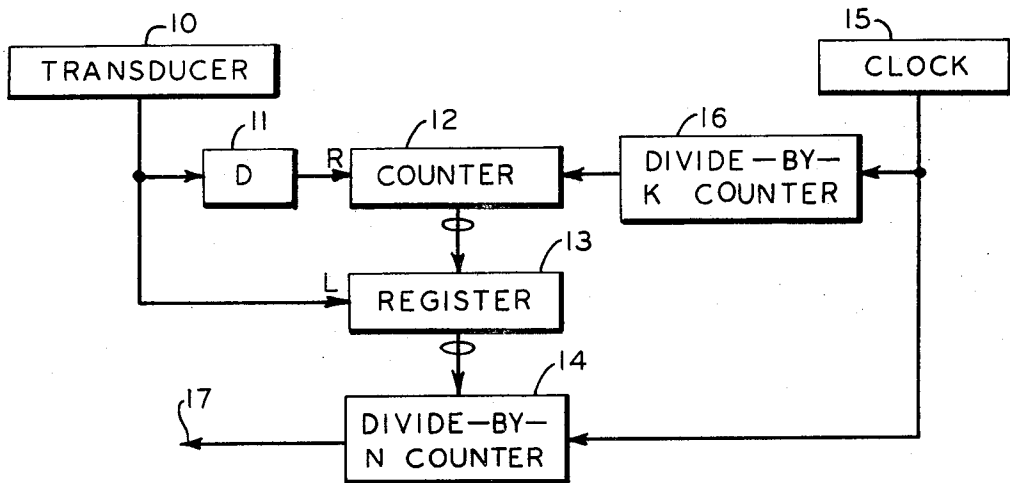


Fig. 1

PRIOR ART

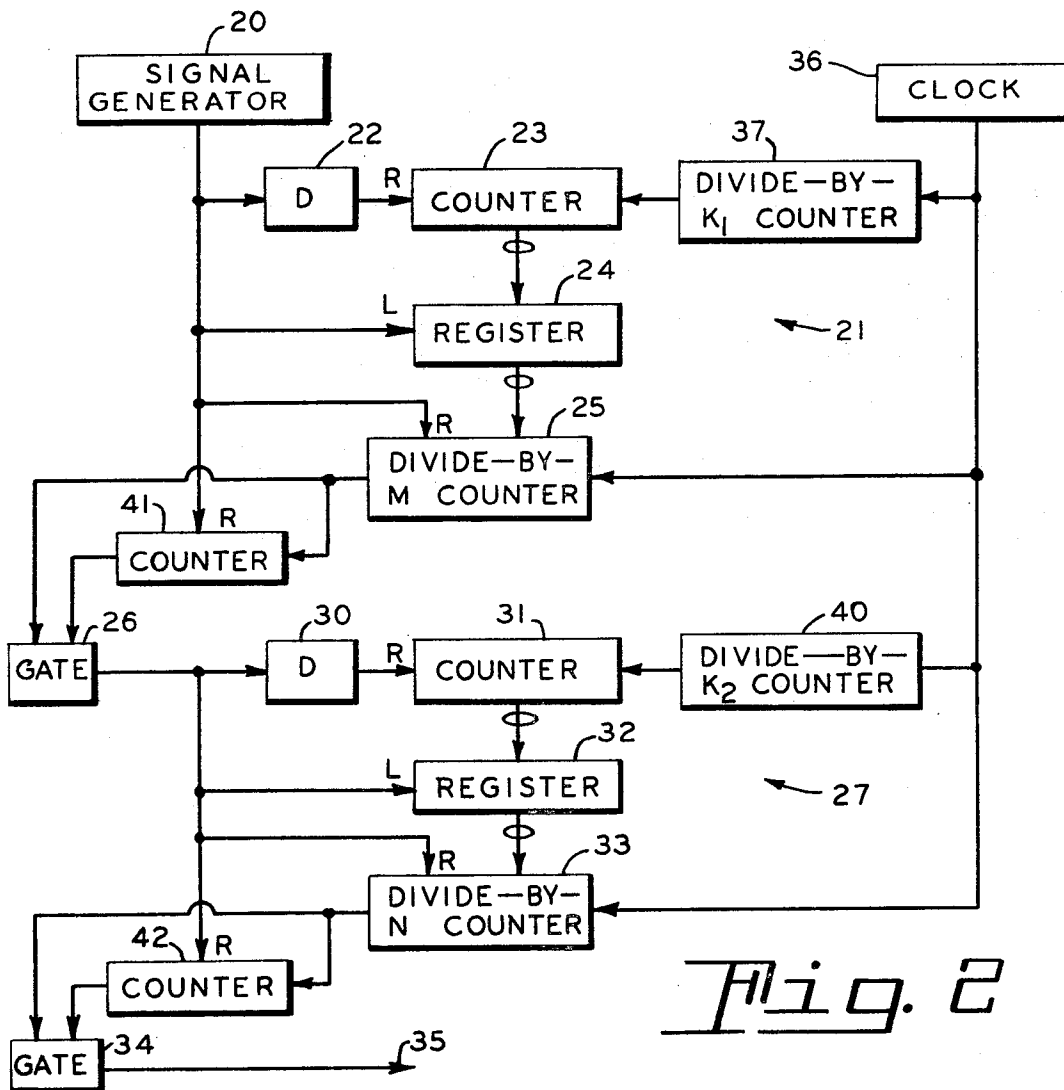


Fig. 2

INTERPOLATING APPARATUS

CROSS-REFERENCE TO RELATED APPLICATION

The copending application of Robert W. Asplund, Ser. No. 201,363, filed Nov. 23, 1971, and assigned to the same assignee as this application, discloses a system wherein this invention can be used.

BACKGROUND OF THE INVENTION

This invention relates to interpolating apparatus for dividing a time interval of variable duration into a predetermined number of subintervals. More particularly this invention relates to interpolating apparatus wherein a time interval is divided into a first predetermined number of subintervals and each of the first subintervals is further divided into a second predetermined number of subintervals.

In the above-identified copending application an electronic ignition timing system for internal combustion engines for reducing or controlling emissions by the engine is disclosed. One of the inputs to the system is a digital signal corresponding to the engine speed as measured by degrees of crankshaft rotation in a predetermined time interval. The disclosed technique for obtaining a signal representative of the degrees of crankshaft rotation includes a transducer that provides a pulse every 90° of crankshaft rotation and an interpolator that provides 90 pulses between each pair of 90° pulses.

To provide satisfactory accuracy, the above-described system requires a relatively high clock frequency which requires better and more expensive components. While satisfactory accuracy may be achieved utilizing bipolar components capable of high frequency operation, implementation of the system with MOS/FET components presents greater difficulties primarily because components operable at sufficiently high clock frequencies may be relatively unattainable. Thus, system accuracy may be compromised, or better and more expensive components are required.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is a primary object of this invention to obviate the above-noted disadvantages of the prior art.

It is a further object of this invention to provide interpolator apparatus which provides increased accuracy.

It is a further object of this invention to provide interpolator apparatus which provides increased accuracy with lower clock frequencies.

It is a still further object of this invention to provide interpolator apparatus that divides a time interval into a predetermined integral number of subintervals by dividing the time interval into a predetermined number of first subintervals and by dividing each of the first subintervals into a predetermined number of second subintervals.

In one aspect of this invention the above objects and other objects and advantages are achieved in interpolating apparatus for dividing a time interval of variable duration into a predetermined integral number of subintervals. The apparatus includes signal generating means for providing reference pulses for determining the duration of the time interval, and first and second interpolating means. The first interpolating means is

connected to the signal generating means for dividing the interval between the reference pulses into a predetermined integral number of first subintervals and for providing pulses indicative of the first subintervals.

The second interpolating means is connected to the first interpolating means for subdividing each of the first subintervals into a predetermined integral number of second subintervals and for providing pulses indicative of the second subintervals. The number of first subintervals multiplied by the number of second subintervals equals the number of subintervals into which the time interval is to be divided.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an interpolator taken from the above-identified copending application and labeled "Prior Art"; and

FIG. 2 is a block diagram of interpolating apparatus in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In FIG. 1 there is shown a transducer 10 which has an output connected via a delay device 11 to a reset input of a counter 12 and to a load input of a register 13. An output of counter 12 is connected in parallel to an input of register 13 which has an output connected in parallel to a divide by N counter 14. A clock 15 has an output connected to an input of counter 14 and to an input of a divide-by-K counter 16 which has an output connected to an input of counter 12. An output of counter 14 is connected to an output terminal 17.

The operation of FIG. 1 is described in the above-identified application. FIG. 1 is considered prior art for the purposes of this application and is illustrated solely to aid in explaining the invention. Transducer 10 provides reference pulses such as pulses representing each 90° of crankshaft rotation of an engine. Counter 12 obtains a count N between reference pulses by counting pulses from counter 16. This count is transferred to register 13 and is used by counter 14 to divide the clock pulses by N. Thus, the interval between reference pulses is divided into K subintervals. In the above-identified application K = 90 so that the pulses provided at output terminal 17 were 1° pulses.

FIG. 2 illustrates the preferred embodiment of the invention. A signal generating means such as signal generator 20 provides reference pulses at an output thereof connected to an interpolating means illustrated as a first level interpolator 21. Interpolator 21 includes a delay device 22 connected between the output of signal generator 20 and a reset input of a counter 23 which has an output connected in parallel to an input of a register 24. The output of signal generator 20 is connected to a load input of register 24 which has an output connected in parallel to an input of a counter 25.

An output of counter 25 is coupled via a gate 26 to an interpolating means illustrated as a second level interpolator 27. Interpolator 27 includes a delay device 30 connected between an output of gate 26 and a reset input of a counter 31 which has an output connected in parallel to an input of a register 32. The output of gate 26 is connected to a load input of register 32 which has an output connected in parallel to an input of a counter 33. Counter 33 has an output connected via a gate 34 to an output terminal 35.

A pulse generating means includes a clock pulse generator 36 which has an output connected to a frequency or pulse rate divider illustrated as a divide-by- K_1 counter 37 and to a frequency or pulse rate divider illustrated as a divide-by- K_2 counter 40. An output of counter 37 is connected to an input of counter 23, while an output of counter 40 is connected to an input of counter 31. The output of clock 36 is further connected to inputs of counters 25 and 33. Register 24 and counter 25 comprise a frequency divider while register 32 and counter 33 comprise another frequency divider.

The output of signal generator 20 is connected to a reset input of a counter 41 and to a reset input of counter 25. The output of counter 25 is connected to an input of counter 41 which has an output connected to an input of gate 26. The output of gate 26 is connected to a reset input of a counter 42 and to a reset input of counter 33. The output of counter 33 is connected to an input of counter 42 which has an output connected to an input of gate 34.

In operation signal generator 20 provides reference pulses that determine the time intervals to be divided. Clock 36 provides pulses at a rate " f " which are coupled to counter 37. Counter 37 counts K_1 clock pulses and then recycles thereby dividing the clock pulse rate by a predetermined integer K_1 . The pulses from counter 37 are coupled to counter 23. Each reference pulse from signal generator 20 causes register 24 to load the number or count in counter 23 and resets counter 23 to zero. The purpose of delay device 22 is to permit register 24 to be loaded before counter 23 is reset. Counter 23 thus counts pulses from counter 37 between successive reference pulses from signal generator 20 to generate numbers or counts M representative of the intervals between the reference pulses. These counts M are successively transferred to register 24.

Counter 25 loads the current count M from register 24 and counts clock pulses down to zero. When counter 25 reaches zero, it provides an output pulse and reloads the count M from register 24 to again count clock pulses to zero. If the interval between two successive reference pulses is X , the count is $M = X(f/K_1)$. Counter 25 divides the clock pulse rate " f " by M to provide pulses at a rate $f/M = K_1/X$. The interval Y between pulses from counter 25 is X/K_1 . Thus, the interval X has been divided into K_1 subintervals by the first interpolator level 21. The reference pulses from signal generator 20 are coupled to the reset input of counter 25 to reset counter 25 to zero. Since counter 25 provides an output pulse each time it reaches zero, the start of the first Y interval is synchronized with the reference pulse beginning each X interval.

The pulses from counter 25 are coupled via gate 26 to the load input of register 32 and via delay device 30 to the reset input of counter 31. Counter 40 is similar to counter 37 but divides the clock rate " f " by a predetermined integer K_2 . Counter 31 generates counts $N = Y(f/K_2)$ between successive pulses from counter 25 similar to the generation of the counts M by counter 23. The counts N are successively transferred to register 32.

Register 32 and counter 33 operate the same as register 24 and counter 25 to divide the clock rate " f " by N . The interval Y between pulses from counter 25 is

further subdivided in the second interpolator level 27 to provide pulses at intervals $Z = Y/K_2 = X/(K_1K_2)$. Thus, the interval X between reference pulses from signal generator 20 has been subdivided into $K = K_1K_2$ subintervals. Counter 33 provides K output pulses via gate 34 to output terminal 35 between each successive pair of reference pulses. In each Y interval the start of the first Z interval is synchronized with the start of the Y interval by the application of the pulses from gate 26 to the reset input of counter 33 to reset counter 33 to zero.

To further explain the advantages of this invention a specific example will be used. The invention, however, is not limited to the specific application or numbers used in the example. In the above-identified copending application transducer 10 of FIG. 1 provides a reference pulse every 90° of rotation of the engine crankshaft. The interpolator divides the interval between the 90° pulses into 90 subintervals so that counter 14 provides 1° pulses at output terminal 17. Thus, $K = 90$. Assume the engine speed is about 5,555 rpm so that the 90° pulses are provided at a rate of about 370 Hz or at intervals of 2.70 milliseconds (ms). Also assume that the clock pulse rate is 900 kHz so that the number in counter 12 will be 27. It will become evident below that these numbers were chosen for arithmetic convenience.

If, for example, the engine speed is slightly greater than 5,555 rpm, the duration of the 90° pulses will be slightly less than 2.7 ms. The count in counter 12 still should be 27, however, the leading edge of the gating interval may just miss one 10 kHz pulse from counter 16 while the trailing edge occurs just before a 10 kHz pulse. Thus, the count will be 26 for a maximum error of one count or an error of 3.7 percent. Similarly, if the engine speed is just below 5,555 rpm, the count can be 28 for a maximum error of 3.7 percent. The maximum percentage error increases with increasing engine speed to 4 percent at 6,000 rpm, for example, and decreases with decreasing engine speed.

When the count N is in error, the 1° pulses from counter 14 are provided at a slightly higher or lower rate than they should be. At 5,555 rpm the 1° pulses should be provided at intervals of 0.030 ms. If the count is 26, however, the intervals will be 0.0289 ms or an error of 3.7 percent. The error is cumulative, however, so that each pulse is further in error. The cumulative error is about 0.1 ms or 3.3° in the position of a pulse at the end of a 90° interval. Thus, about 93 pulses will be provided by counter 14 between successive 90° pulses instead of 90. Similarly, if the count in counter 12 is 28, the interval between 1° pulses will be too long and fewer than 90 pulses will be provided by counter 14.

Assuming, however, that the above error is sufficiently small to provide satisfactory operation, it will now be shown that the error increases greatly if the clock pulse rate is lowered. Accordingly, assume a clock pulse rate of 300 kHz. The count in counter 12 will now be 9. This count can be in error by a maximum of one count or 11.1 percent. When a count of 8 occurs, the spacing of 1° pulses will be 0.0267 ms. Thus, at the end of a 90° interval the cumulative error is about 0.3 ms or 10° in the position of a pulse and about 100 pulses will be provided. In the system described in

the above-identified compending application, the error will be intermittent, that is, there will be oscillation between substantially different spark advances for successive cycles.

Next consider the two-level interpolator of FIG. 2. Assume an engine speed of 5,555 rpm and a clock pulse rate of 300 kHz. Also assume that $K_1 = 15$ and $K_2 = 6$. Note, however, that $K_1 K_2 = K$ so that K_1 and K_2 can be any two numbers that multiply to 90.

Counter 23 thus counts 20 kHz pulses from counter 37 for an interval X of 2.7 ms. Thus, the count M should be 54. This count can be in error by one count or about 2 percent, as was determined above. When the count M is 54, counter 25 provides pulses at the correct 6° intervals (Y) or every 0.18 ms. If M is 53, the interval between 6° pulses will be $Y = 0.1767$ ms. The error after 15 intervals is about 0.05 ms or 1.7°. Similarly if M is 55, the interval between 6° pulses is $Y = 0.1833$ ms and the cumulative error is about 0.05 ms or 1.7°.

When M is 55, the last pulse will be about 1.7° late. Thus, counter 25 will be counting when the 90° pulse ending the interval is provided. The 90° pulse is coupled to the reset input of counter 25 to reset counter 25 to zero. Since counter 25 provides an output pulse each time it reaches zero the first 6° pulse in an interval is synchronized with the 90° pulse that marks the beginning of the interval. Thus, synchronization prevents cumulative errors from carrying over to the next cycle.

When M is 53, the last pulse will be about 1.7° early so that an extra 6° pulse will occur just before the 90° pulse ending the interval is provided. Counter 41 and gate 26 prevent this extra 6° pulse from being coupled to interpolator 27. Counter 41 counts the 6° pulses from counter 25. After 14, 6° pulses occur, counter 41 inhibits gate 26 so that the 15th pulse that may occur just before a 90° pulse is not coupled through gate 26. The 90° pulses reset counter 41. Note that in the arrangement described, the 6° pulse that occurs when counter 25 is reset by a 90° pulse is coupled through gate 26 but is not counted by counter 41. Many other arrangements or circuits can also be used to prevent extra pulses from occurring. In any event, 15 and only 15 pulses will be coupled through gate 26 in each 90° interval.

The 6° pulses coupled through gate 26 normally will mark intervals of $Y = 0.18$ ms when the engine speed is 5,555 rpm. When the count M is in error by one count, the interval will be $Y = 0.1767$ ms or $Y = 0.1833$ ms. Interpolator 27 subdivides each of these intervals into six 1° intervals. When the 6° interval is $Y = 0.18$ ms, counter 31 counts 50 kHz pulses for 0.18 ms to generate a count N of 9. This count can also be in error by $\pm$ one count. When the 6° interval is $Y = 0.1767$ ms, the count N will be either 8 or 9. When the 6° interval is $Y = 0.1833$ ms, N will be either 9 or 10. Thus, N will be either 8, 9, or 10.

Counter 33 is reset to zero by each 6° pulse from gate 26 so that the first 1° pulse in each 6° interval is synchronized with the 6° pulse to prevent cumulative error from one 6° interval to the next. Counter 46 and gate 34 operate the same as counter 41 and gate 26 to prevent more than six 1° pulses from occurring in any 6° interval.

Assume a set of conditions that produce maximum error, that is, N is 8 and the 6° pulse interval is $Y = 0.1767$ ms. In this case the 1° pulses will be provided at $Z = 0.0267$ ms intervals so that the sixth pulse in a 6° interval occurs about 0.0167 ms or 0.6° early. Since counter 42 and gate 34 prevent an extra pulse from occurring, no error occurs except in the position of a particular pulse. The last or 90th 1° pulse can occur about 0.06 ms or 2° early.

Next, assume the conditions that produce maximum error in the opposite direction, that is, N is 10 and the 6° pulse interval is $Y = 0.1833$ ms. The 1° pulse interval is $Z = 0.0333$ ms. The sixth 1° pulse in an interval occurs 0.1667 ms after the first pulse in the interval. Since counter 33 is reset by each 6° pulse, no cumulative error occurs. The last 6° pulse occurs about 0.0467 ms or 1.6° late so that the last 6° interval is short. If N is 10 during the interpolation of the last 6° interval, only four 1° pulses will be provided during the last interval. The position of the last pulse is thus in error by about 2°.

Any other combination of counts N and intervals Y will produce less error than those described above. An additional source of error can occur due to the error in the last 6° interval in a 90° interval. In both interpolators 21 and 27 the counts M and N obtained during one interval are used to divide the clock pulse rate during the next interval. Thus, during the last 6° interval in a 90° interval, counter 31 acquires a count N which is used to interpolate 1° pulses during the next succeeding 6° interval. The last 6° interval, however, can be so short that the count N is less than 8 or so long that the count N is greater than 10. If the count is less than 8, counter 42 and gate 34 will prevent more than six pulses from occurring during the next 6° interval. If the count is greater than 10, however, one less 1° pulse may occur thereby increasing the total error by 1°.

Acceleration or deceleration can also cause the count in counter 23 to be either low or high because of the change in the interval of the 90° pulses. The error due to acceleration or deceleration may cause the 6° intervals to be too long or short, especially the last 6° interval, however, this error also affects the interpolator of FIG. 1 in a similar manner.

In summary, it is clear from the above analysis that the preferred embodiment of the invention disclosed in FIG. 2 is more accurate than the apparatus illustrated in FIG. 1 even when the preferred embodiment of the invention utilizes a much lower clock frequency. At higher clock frequencies greater accuracy than that described can be provided by apparatus in accordance with the invention.

While there has been shown and described what is at present considered the preferred embodiments of the invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the scope of the invention as defined by the appended claims.

What is claimed is:

1. Interpolating apparatus for dividing a time interval of variable duration into a predetermined integral number, K , of subintervals comprising:

signal generating means for providing at least two reference pulses for determining the duration of said time interval;

first interpolating means connected to said signal generating means for dividing said interval between said reference pulses into a predetermined integral number, K_1 , of first subintervals and for providing pulses indicative of each of said first subintervals; and

second interpolating means connected to said first interpolating means for subdividing each of said first subintervals into a predetermined integral number, K_2 , of second subintervals, where K_1 multiplied by K_2 is equal to K , and for providing pulses indicative of each of said second subintervals.

2. Interpolating apparatus as defined in claim 1 further including pulse generating means connected to said first and second interpolating means for providing first pulses at a rate f , second pulses at a rate f/K_1 to said first interpolating means, and third pulses at a rate of f/K_2 to said second interpolating means.

3. Interpolating apparatus as defined in claim 2 wherein said first interpolating means includes a first counter connected to said signal generating means and to said pulse generating means for counting said second pulses for an interval determined by said reference pulses to generate a count M and a first frequency divider connected to said first counter and to said pulse generating means for dividing said first pulses by said count M to provide said pulses indicative of each of said first subintervals, and said second interpolating means includes a second counter connected to said pulse generating means and to said first frequency divider for counting said third pulses for intervals determined by said pulses indicative of said first subintervals to generate a count N for each of said first subintervals and a second frequency divider connected to said second counter and to said pulse generating means for dividing said first pulses by the counts N to provide said pulses indicative of each of said second subintervals.

4. Interpolating apparatus as defined in claim 3 wherein said first and second frequency dividers include first and second registers connected to said first and second counters, respectively, and third and fourth counters connected to said first and second registers, respectively, and to said pulse generating means whereby said third and fourth counters each count said first pulses in groups equal to the counts M and N , respectively.

5. Interpolating apparatus as defined in claim 4 wherein said signal generating means is connected to said third counter for resetting said third counter each time a reference pulse occurs, and said third counter is connected to said fourth counter for resetting said fourth counter each time one of said pulses indicative of each of said first subintervals occurs.

6. Interpolating apparatus as defined in claim 1 wherein the number K is 90.

7. Interpolating apparatus as defined in claim 6 wherein the number K_1 is 15 and the number K_2 is 6.

8. Interpolating apparatus as defined in claim 5 wherein the number K is 90, the number K_1 is 15, and the number K_2 is 6.

9. Interpolating apparatus for use in an internal combustion engine control system for dividing time intervals of variable durations between reference pulses provided by a signal generating means representative of numbers of degrees of rotation of the crankshaft of said engine into a predetermined number, K , of subintervals comprising:

pulse generating means for providing first pulses at a rate f , second pulses at a rate f/K_1 where K_1 is a predetermined integer, and third pulses at a rate f/K_2 where K_2 is a predetermined integer and $K_1 \times K_2 = K$;

first interpolating means connected to said pulse generating means and to said signal generating means for dividing each of said time intervals between said reference pulses into K_1 first subintervals and for providing pulses indicative of said first subintervals; and

second interpolating means connected to said pulse generating means and to said first interpolating means for subdividing each of said first subintervals into K_2 second subintervals and for providing pulses indicative of said second subintervals.

10. Interpolating apparatus as defined in claim 9 wherein said first interpolating means includes a first counter connected to said signal generating means and to said pulse generating means for counting said second pulses for time intervals determined by said reference pulses to generate a count, M , for each of said time intervals and a first frequency divider connected to said first counter and to said pulse generating means for dividing the rate of said first pulses by said count M , and said second interpolating means includes a second counter connected to said first frequency divider and to said pulse generating means for counting said third pulses for said first subintervals determined by pulses provided by said first frequency divider to generate a count, N , for each of said first subintervals and a second frequency divider connected to said second counter and to said pulse generating means for dividing the rate of said first pulses by said count N .

11. Interpolating apparatus as defined in claim 10 wherein said first frequency divider includes a third counter connected to receive said count M and said first pulses for counting said first pulses in groups of M pulses, and said second frequency divider includes a fourth counter connected to receive said count N and said first pulses for counting said first pulses in groups of N pulses.

12. Interpolating apparatus as defined in claim 11 wherein said signal generating means is connected to said third counter for synchronizing the start of said third counter with said reference pulses, and said third counter is connected to said fourth counter for synchronizing the start of said fourth counter with pulses provided by said third counter.

13. Interpolating apparatus as defined in claim 12 wherein K is 90, K_1 is 15, and K_2 is 6.

14. Interpolating apparatus as defined in claim 9 wherein K is 90, K_1 is 15, and K_2 is 6.

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