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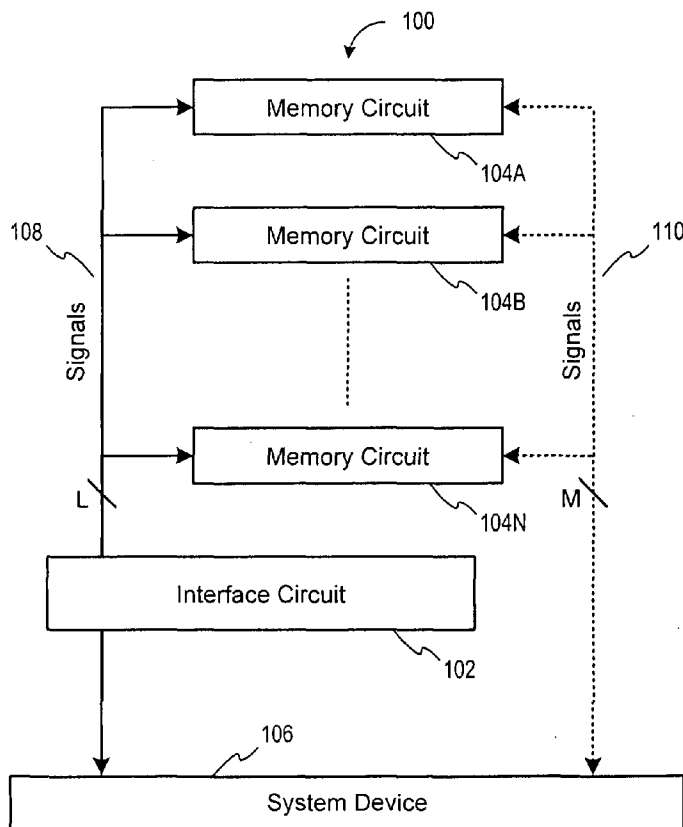
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(54) Title: MEMORY CIRCUIT SYSTEM AND METHOD



(57) Abstract: A memory circuit system (Figure 1) and method are provided in the context of various embodiments. In one embodiment, an interface circuit (102) remains in communication with a plurality of memory circuits (104) and a system. The interface circuit is operable to interface the memory circuits and the system for performing various functionality (e.g. power management, simulation/emulation, etc.).

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B. FIELDS SEARCHED
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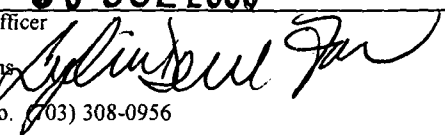
C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/0206738 A (JEDDELOH et al) 20 June 2003 (20.06.2003), entire document.	121-176 and 179-198

Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
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