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(54) Title of the Invention: **Interrupt generating unit**
 Abstract Title: **Interrupt Generating Unit**

(57) A microcontroller 2 has a processor 6, peripherals 18, 20, 22, 24, 26, a programmable peripheral interconnect (PPI) 10, and an interrupt-generating unit 17. An event-generating one of the peripherals 18, 20, 22, 24, 26 is configured to signal an event to the PPI 10. The interrupt-generating unit 17 is arranged to send an interrupt to the processor 6 in response to receiving a task signal from the PPI 10. The PPI 10 is configured to access a memory in which a mapping can be stored between (i) an event of a first peripheral 18, 20, 22, 24, 26 and (ii) a task of the interrupt-generating unit 17, so as to cause the PPI 10 to respond to a signal of the event from the first peripheral by sending a task signal for the task to the interrupt-generating unit 17.

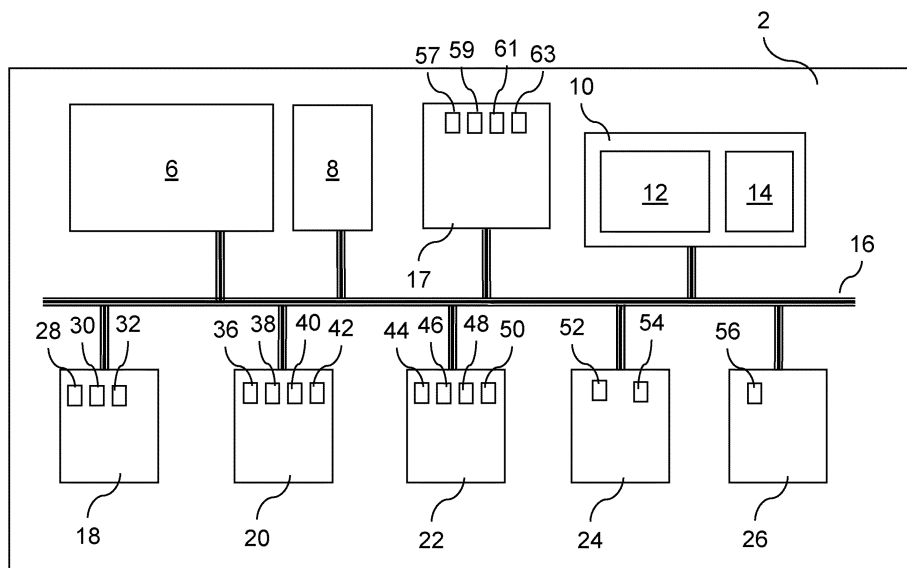


Figure 1

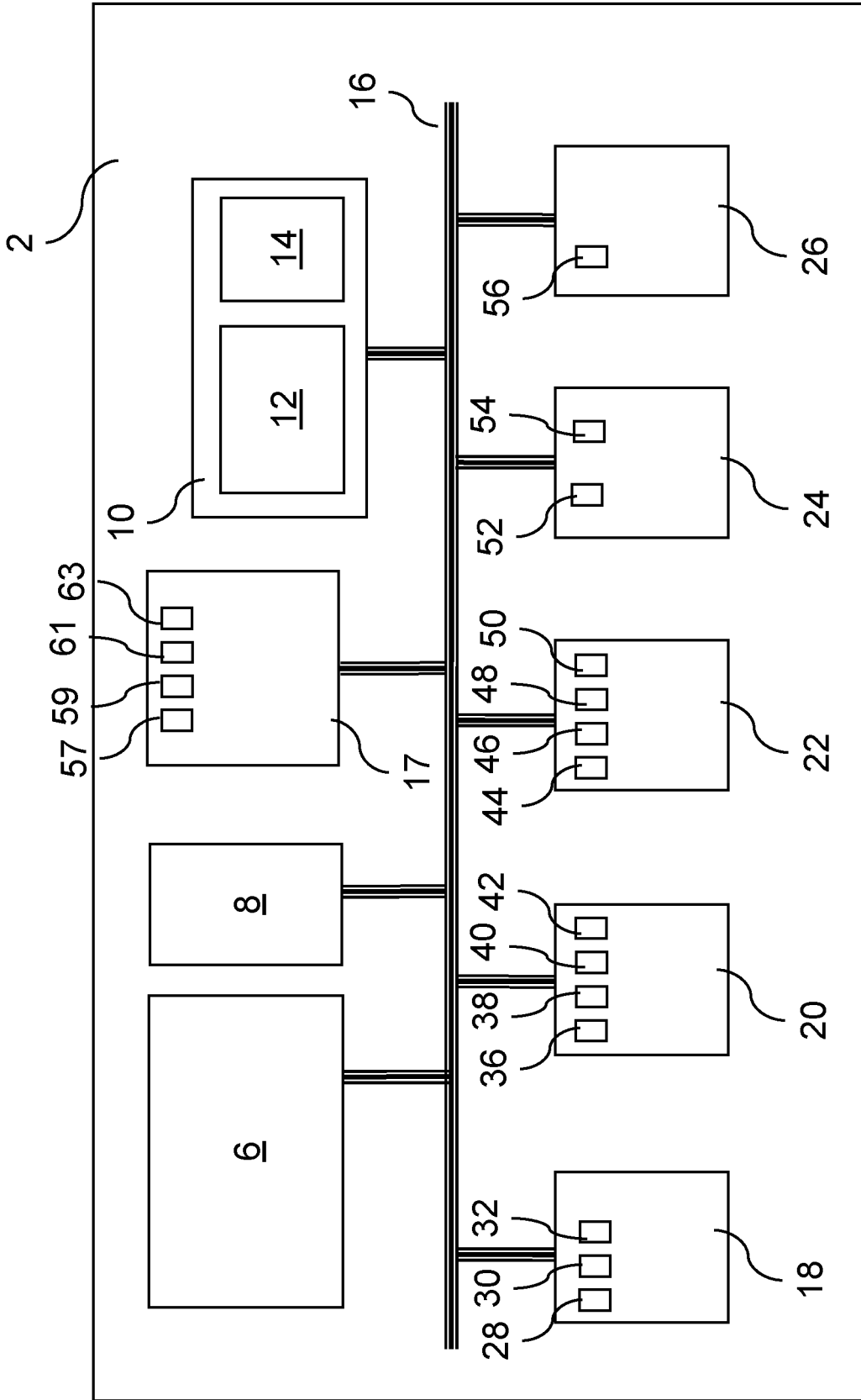


Figure 1

Mapping #	Event Register	Task Register
1	0x100	0x500
2	0x300	0x620
3
...

Figure 2

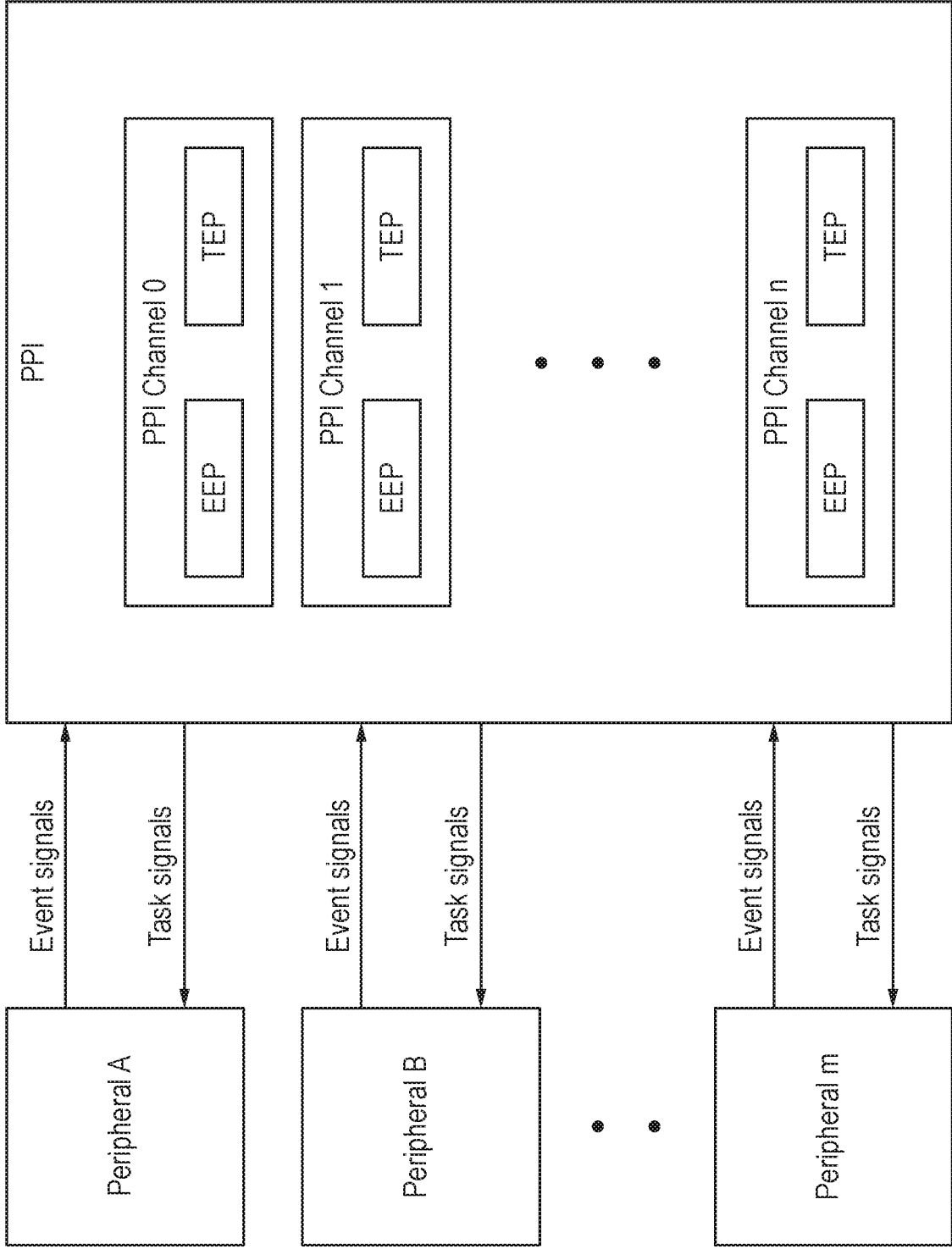


Figure 3

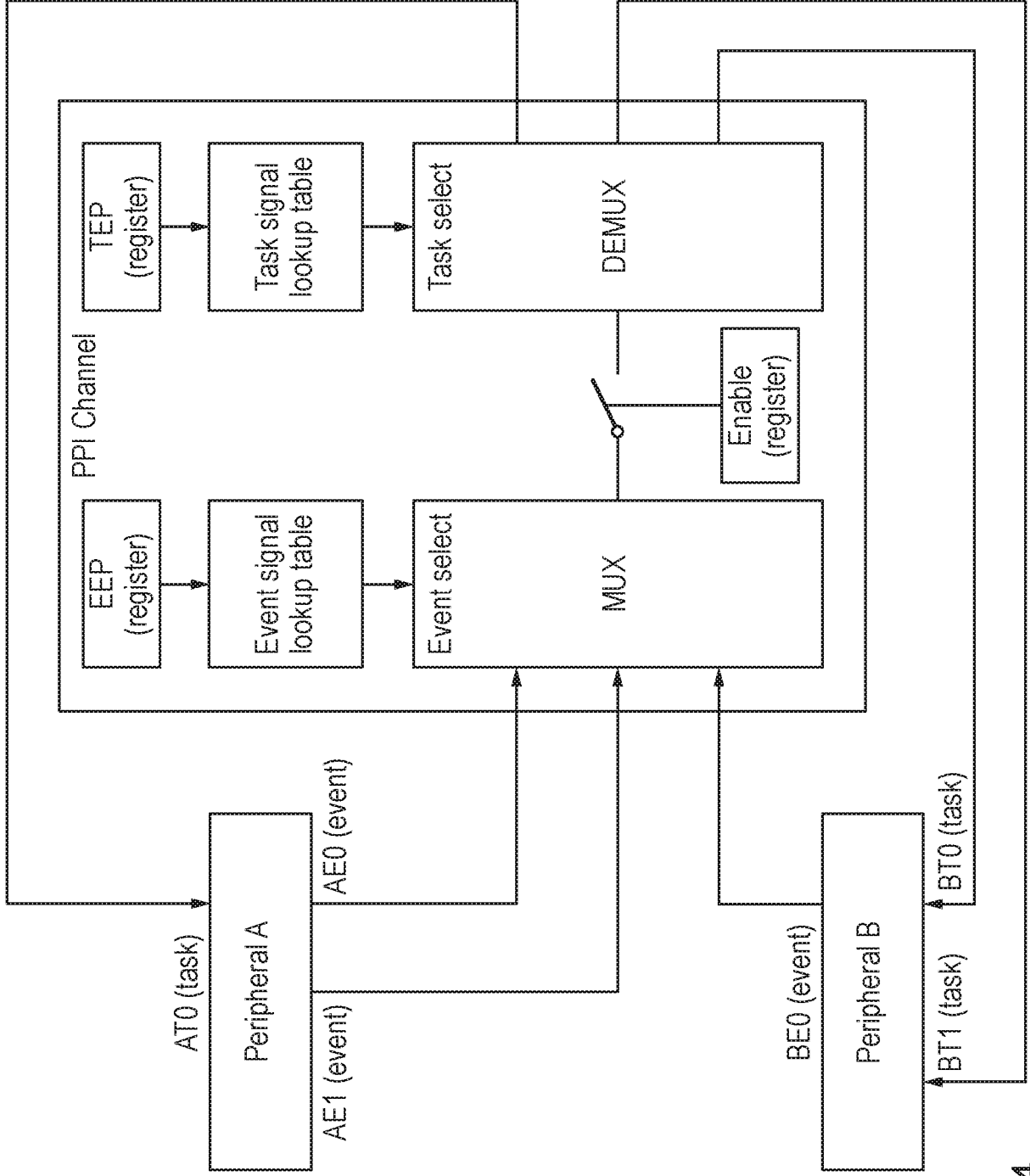


Figure 4

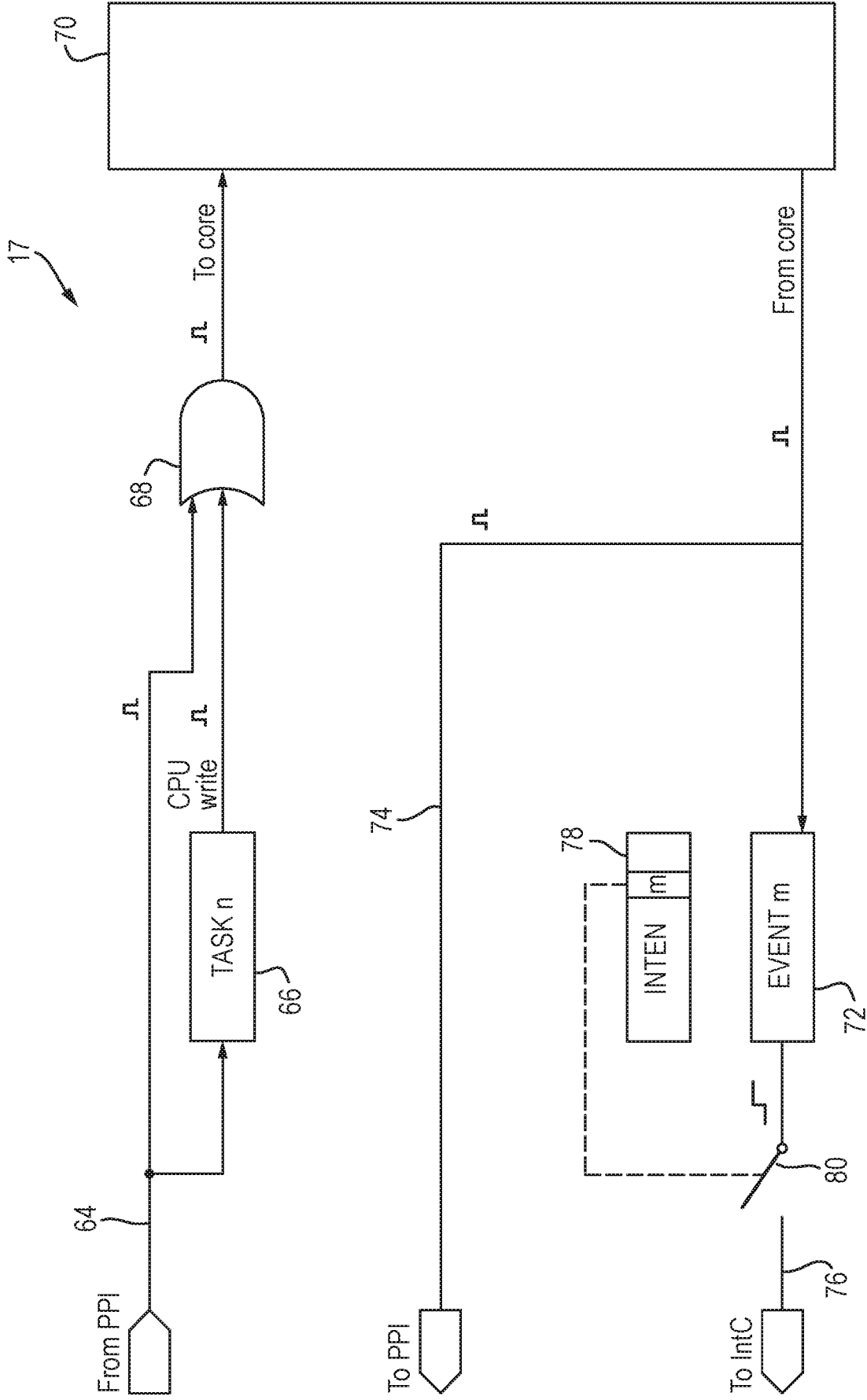


Figure 5

Interrupt Generating Unit

This invention relates to a microcontroller.

5 Microcontrollers are often used in applications where timing is important, such as in radio devices. There are situations where it can be important that two tasks involving one or more peripherals are initiated by a processor on a microcontroller essentially simultaneously. The device may, for example, need to initiate communication over a serial interface and start a timer at precisely the same time. This would ordinarily be
10 done by instructing the processor to initiate a first one of the tasks and then immediately instructing it to initiate the other task. However, even if these are carried out using adjacent software instructions, it is still possible that the processor might receive an interrupt after triggering the first task, but before triggering the second task. This can lead to undesirable behaviour.

15

This problem can be mitigated to an extent by masking certain interrupts at critical times, or by setting different priorities on different interrupts. However, neither of these approaches is perfect, and they also introduce additional complexity to the software.

20 In an arrangement described here for reference purposes, a microcontroller comprises:

- a processor;
- a plurality of peripherals;
- a programmable peripheral interconnect;
- 25 an event-generating unit; and
- a memory, storing software,

wherein:

the event-generating unit comprises an event-generating register, addressable
by the processor;

30 the event-generating unit is connected to the programmable peripheral interconnect; and

the event-generating unit is arranged to detect a predetermined change to the contents of the event-generating register and, in response to detecting such a

predetermined change, to signal an event to the programmable peripheral interconnect;

each of the peripherals is connected to the programmable peripheral interconnect;

5 each of the peripherals is configured to respond to a task signal from the programmable peripheral interconnect by performing a respective task;

the programmable peripheral interconnect is configured to access a mapping memory in which a plurality of mappings can be stored, each mapping an event of the event-generating unit to a task of one of the peripherals;

10 the programmable peripheral interconnect is configured so that, when a mapping is stored in the mapping memory from an event of the event-generating unit to a task of one of the peripherals, the programmable peripheral interconnect will respond to a signal of the event from the event-generating unit by sending a task signal to the peripheral;

15 the programmable peripheral interconnect is configured so that, when the mapping memory stores mappings from one event of the event-generating unit to two or more different tasks, the programmable peripheral interconnect will send the two or more respective task signals within a predetermined maximum time from receiving a signal of the event; and

20 the software comprises instructions, executable by the processor, to (i) store, in the mapping memory, mappings from one event of the event-generating unit to at least two different peripheral tasks, and (ii) make said predetermined change to the contents of the event-generating register.

25 Thus it will be seen by those skilled in the art that, in accordance with such an arrangement, the software, when executed, causes two or more peripheral tasks to be triggered atomically, and within a predetermined maximum time frame. Because only a single processor write instruction is used to initiate the peripheral tasks, there is no risk of the triggering of the two tasks being interrupted by a processor interrupt.

30

The predetermined maximum time may have any value, but is preferably 10 microseconds or less; more preferably 1 microsecond or less; and most preferably 0.1 microsecond or less. It is preferably sufficiently low that two or more tasks can be regarded, for practical purposes, as being triggered simultaneously. The

35 predetermined maximum time may be less than 100 processor clock cycles; more

preferably, it may less than 10 or 5 clock cycles. In some implementations, it may be less than one processor clock cycle. The predetermined maximum time is preferably constant for all mappings. Preferably, the programmable peripheral interconnect is arranged to send the two or more respective task signals simultaneously (e.g., to
5 within one cycle of a clock signal provided to the programmable peripheral interconnect or provided to the processor). In this case, there is preferably a constant time delay between the programmable peripheral interface receiving a signal of an event and sending two or more task signals that are mapped to the event, for all possible mappings.

10

Programmable peripheral interconnects are already known—for example, as described in WO 2013/088121 by the present applicant. In some preferred implementations, the programmable peripheral interconnects is substantially the same as a programmable peripheral interconnect described in WO 2013/088121, the entire contents of which
15 are incorporated herein by reference, although this is not essential.

20

The programmable peripheral interconnect preferably also supports the programming of peripheral-to-peripheral channels. In some implementations, the microcontroller also comprises one or more peripherals that are event-generating, being configured to signal an event to the programmable peripheral interconnect (PPI). The programmable peripheral interconnect is preferably arranged so that a mapping can be stored between an event of a first peripheral and a task of a second peripheral, and so that, when a mapping is stored in memory between an event of a first peripheral and a task of a second peripheral, the interconnect will provide a channel by sending a
25 task signal to the second peripheral in response to a signal of the event from the first peripheral. In this way, the programmable peripheral interconnect may conveniently interface with the event-generating unit in the same way as it interfaces with an event-generating peripheral. In some implementations, the event-generating unit may be regarded as a type of event-generating peripheral.

30

The peripherals are not limited to any particular type, and may include such peripherals as: a timer, a UART, a voltage comparator, an encryption engine, an analogue-to-digital converter (ADC), a digital-to-analogue converter (DAC), a radio transmitter, a radio receiver, and so on. An event may be signalled from a peripheral
35 in response to any input, change of state, satisfying of a criterion, etc., as will be

familiar to one skilled in the art—for example, when a timer reaches a target value. The tasks may be any function or operation which can be performed by the peripheral, such as transmitting data over an interface.

5 The event-generating unit may be arranged to signal only a single type of event, but it is preferably able to signal a plurality of different events. These may be signalled over different respective event lines, or using different respective event registers. The event-generating unit may have a plurality of event-generating registers, addressable by the processor. Each event-generating register may be associated with a different
10 respective event. The different events can preferably be identified uniquely in a stored mapping—for example, by using the address of the event-generating register as an identifier, or by using some other predetermined set of identifiers.

It will be appreciated that, unlike a conventional peripheral, where events signify some
15 change of state in the peripheral (e.g., the completion of some operation), an event from the event-generating unit has no intrinsic meaning, but is instead given significance by the processor (or other component) that causes it, by writing to the event-generating register.

20 The PPI may be connected to the peripherals and/or the event-generating unit by respective lines for each event and task over which event and task signals can be sent; i.e. one line for each event or task. The signals may be pulses or encoded values. Incoming lines may connect to one or more multiplexers within the PPI; e.g. with one multiplexer for each channel. Outgoing lines may leave from one or more
25 demultiplexers within the PPI; e.g. with one demultiplexer for each channel. The PPI may be configured to set or control a multiplexer and a demultiplexer of a channel in accordance with a mapping stored in memory.

In some implementations, the PPI may access the task registers or event registers, or
30 both, of peripherals and/or the event-generating unit over a bus, e.g. over an address bus using memory-mapped input/output (MMIO). The PPI may thus receive an event signal through a change in the contents of the associated event register and/or may send a task signal by changing the contents of the associated task register. The PPI may be connected to a bus (e.g. a system bus which may comprise an address bus,
35 data bus and control bus) to which the processor is also connected. The same bus

may connect the peripherals and/or the event-generating unit to the processor. The PPI may detect a change in the contents of an event register by reading the event register at intervals; e.g. regular polling; or by receiving an interrupt from the event-generating peripheral or the event-generating unit. On receiving an interrupt, the PPI
5 may then read the contents of a corresponding event register.

An event register or task register may contain a single bit (i.e. for signalling a flag or binary signal), or it may comprise a plurality of bits, e.g. 8, 16 or 32 bits.

10 The event-generating unit may signal an event to the programmable peripheral interconnect (PPI) over an event signal line. Alternatively, it may signal the event through a change to a register, in which case the PPI may be configured to poll the register at intervals in order to detect the change. This register may be the event-generating register itself, or a separate event register for the event-generating unit.
15

In some implementations, the identification of a task in a mapping is the address of a task register, associated with the task, as described in WO 2013/088121. However, this is not essential, and the identification of a task of a task-receiving peripheral could, for example, comprise (i) a peripheral-identifier and (ii) a task-identifier or signal-line-
20 identifier, unrelated to the address of any associated task register (which may or may not be present on the peripheral).

A task-receiving peripheral may comprise a task register, addressable by the processor, associated with a task, and be configured to perform that task in response
25 to a change in the contents of the task register. A mapping between an event of a first peripheral and a task of a second peripheral may then comprise (i) an identification of the event of the first peripheral, and (ii) the address of a task register associated with the task. The PPI may be configured so that, when a mapping is stored in memory between an event of a first peripheral and a task of a second peripheral, the
30 interconnect will provide a channel by sending a task signal to the second peripheral in response to a signal of the event from the first peripheral.

An event-generating peripheral may comprise an event register, addressable by the processor, associated with an event. While the event register may be located
35 immediately adjacent logic associated with the peripheral on an integrated circuit, this

is not essential and it may be situated some distance away from other elements of the peripheral; the same is true for the task register. The registers may comprise any suitable memory structure. The peripheral may change the contents of the event register when signalling an event; for example, by writing a binary '1' to the event register whenever it signals an event.

In some implementations, the identification of an event of a first peripheral in a mapping is the address of an event register associated with the event. In this way, a channel can be configured simply by storing two register addresses in memory: an event-register address and a task-register address. Software running on the processor might do this via a function call or might write the addresses directly to the memory where the mapping is stored. This is not essential, however, and the identification of the event of the first peripheral could comprise a peripheral identifier and an event or signal line identifier, unrelated to the address of any associated event register which may or may not be present.

The event-generating unit preferably comprises at least one event register, addressable by the processor, associated with an event of the event-generating unit. In some implementations the event-generating register is the event register. In other implementations, the event register is separate (i.e. has a different address) from the event-generating register. The unit may be configured so that a predetermined change to the event-generating register may cause a predetermined change to the event register. The event-generating register may, in some implementations, be a task register for the event-generating unit. The event-generating unit may comprise a plurality of event-generating registers and a plurality of event registers. Each event-generating register may be associated with a respective one of the event registers, such that a change to one of the event-generating registers causes a change to an associated one of the event registers.

The event-generating unit may comprise logic that associates two or more event-generating registers with one event—e.g., requiring predetermined changes in two different event-generating registers, possibly in a predetermined order, before signalling a particular event. In other words, the event-generating unit may comprise logic for sending an event signal when, or only when, a criterion relating to two or more

event-generating registers is met. Such logic may be fixed (i.e., hard-wired), or it may be programmable.

5 In some implementations, the event-generating unit is able to receive a task signal from the programmable peripheral interconnect (e.g. over a task line, or by way of a change to the contents of the event-generating register), and to respond by signalling an event to the programmable peripheral interconnect. This may be useful if the event-generating unit is also configured to send interrupts to the processor when signalling an event, as explained in more detail below.

10

An event of the event-generating unit may be identified in a mapping in the same way as an event of an event-generating peripheral is identified—e.g. by the address of an associated event register, or by some other identifier unique to the event.

15 The PPI is programmable in the sense that it can be programmed or configured to define connections between peripherals using one or more mappings. The PPI need not necessarily comprise its own a processing unit for executing software instructions, although it may do so.

20 A mapping in the mapping memory may take any suitable form. In some implementations, the address of an event register and the address of a task register, or pointers to these registers, may be stored as related entries in an array, table or database. For example, the PPI may maintain a table having a number of rows, each corresponding to a different channel, and two columns, the first for identifying an event
25 register and the second for identifying a task register. It will be appreciated such an array or table can be a logical construct and need not necessarily be limited to any particular physical locations of the data in memory. The PPI may comprise a first set of registers for storing task-register addresses and a second set of registers for storing event-register addresses. There may be an equal number of registers in each set. A
30 register in the first set may control a multiplexer which is connected to a demultiplexer controlled by a corresponding register in the second set, thereby defining a channel.

The memory may be separate from the PPI, e.g. in a separate region of silicon or on a different chip, but is preferably an integrated component of the PPI, which can reduce
35 access times. The memory may be volatile (e.g. RAM) or non-volatile (e.g. EEPROM

or flash). The mappings are preferably stored in one or more registers which are preferably addressable by the processor. Each channel provided by the PPI may have one associated event end-point register and one associated task end-point register, which may be suitable for storing an address of an event register and an address of a task register respectively. Some of the channels may use these registers to store other types of event and/or task identifiers.

The mapping or mappings may be written to the memory by the PPI or by the processor, or by both. The processor may indirectly establish a channel between peripherals by instructing the PPI to store the appropriate mapping.

The PPI preferably comprises, or can access, one or more lookup tables which it can use to look up a register address from a mapping in order to determine a particular event line or task line (or event port or task port) corresponding to that register address. It may then select the line or port as input or output for a channel (e.g. by controlling a multiplexer or demultiplexer appropriately). The lookup table may take any suitable form, and need not necessarily be implemented as a physical table in memory.

The PPI may support any number of channels; e.g. 1, 8, 16, 32 or more. A channel can be any physical (e.g. electrical) or logical connection between an event input port or line to the PPI and a task output port or line from the PPI. A channel may link one or more inputs to one or more outputs (e.g. using logic gates to define branches or forks along the channel path).

The PPI preferably comprises a mechanism for allowing a channel to be enabled and/or disabled. The PPI may comprise a bit-field register, having one bit associated with each channel, and be configured so that a channel is enabled if its associated bit in the bit-field register is set to a predetermined value (e.g. a binary 1).

An event-generating peripheral may have more than one event register. Similarly, a task-receiving peripheral may have more than one task register.

As already explained, the PPI is configurable to respond to one event signal by sending two or more task signals, potentially to different task-receiving peripherals. In

some implementations this may be accomplished by storing a plurality of mapping relations in the mapping memory, each mapping the event (e.g., identified by an event register address) to a different respective task (e.g., identified by respective task register addresses). In other implementations, it may be accomplished by storing a
5 single mapping relation which maps one event to two or more tasks directly; e.g. by having a table stored in the mapping memory comprising three or more columns, one for the event, and two or more further columns for respective tasks.

The event-generating unit preferably has no outputs other than one or more event
10 lines to the PPI, zero or more interrupt lines to the processor, and zero or more registers. It preferably has no inputs other than a clock input, one or more registers, and zero or more task lines. The event-generating unit is typically much simpler than a conventional peripheral. It is preferably smaller than any other peripheral on the microcontroller, in terms of its number of components or its number of gates. It
15 preferably has no timing mechanism (unlike a timer peripheral). It preferably has no data input mechanism, other than zero or more event registers, task registers and configuration registers (unlike a serial interface, or digital-to-analogue converter, for example, which have connections for receiving and transmitting arbitrary data to other components or devices).

20

The event-generating unit may comprise circuitry for sending an interrupt to the processor when signalling an event. The interrupt may be a maskable interrupt or a non-maskable interrupt. It may have an input for enabling and/or disabling the sending of an interrupt to the processor when signalling a particular event. The event-
25 generating unit may comprise one or more configuration registers for configuring the event-generating unit to send an interrupt to the processor when it detects a change to the contents of the event-generating register. The unit may comprise separate configuration registers for configuring maskable and non-maskable interrupts respectively.

30

The ability to send an interrupt to the processor is particularly useful when the event-generating unit comprises an input for receiving a task signal from the programmable peripheral interface. This then allows the programmable peripheral interface to be programmed so that an event on a peripheral can cause the event-generating unit to
35 send an interrupt to the processor. This can be useful if the peripheral is not capable

of sending an interrupt itself, or if the peripheral has been assigned only a limited number of interrupts (e.g., one interrupt), meaning that all interrupts from the peripheral must be processed in a limited number of interrupt service routines (e.g., one interrupt service routine). By using the PPI and the event-generating unit to send
5 an interrupt to the processor instead, the peripheral can effectively increase the number of different interrupts (e.g. with different interrupt numbers) that it can cause to be sent to the processor. This can simplify the programming of the interrupt service routine. It can also, for processors that support interrupts at different priority levels, enable a peripheral to interrupt the processor at a plurality of different interrupt levels,
10 which may greater than the number of interrupt levels that were accessible to the peripheral without using the event-generating unit.

For example, a peripheral might have one event called "NEWVALUE" that occurs every 100us, and another event called "ERROR" which it signals only when something
15 goes wrong. The peripheral might, however, only have one interrupt line to the processor, and so be unable to interrupt at a higher priority for the "ERROR" event. However, by configuring a PPI channel between the peripheral and the event-generating unit so that a signal of the "ERROR" event from the peripheral will cause the PPI to activate a task line on the event-generating unit, and by setting the event-
20 generating unit to send a high-priority interrupt to the processor when it receives a signal over that task line, the peripheral can be provided with the capacity to send an "ERROR" interrupt to the processor at high priority. This can enable the processor to respond quickly to the "ERROR" event.

25 In some implementations, the microcontroller may comprise a plurality of event-generating units, each connected to the processor by a set of interrupt lines, each set having a different respective interrupt priority level. Alternatively, one event-generating unit may have one or more tasks (or events) which can be used to send an interrupt at a first priority level, and one or more other tasks (or events) which can be used to send
30 an interrupt at a second priority level. The association between the tasks (or events) and the interrupt priority levels may be fixed or may be configurable (e.g., according to one or more register values on the event-generating unit).

This idea of using a unit connected to the programmable peripheral interconnect to generate processor interrupts is novel and inventive and thus, from one aspect, the invention provides a microcontroller comprising:

- 5 a processor;
- a plurality of peripherals;
- a programmable peripheral interconnect; and
- an interrupt-generating unit,

wherein:

10 an event-generating one of the peripherals is configured to signal an event to the programmable peripheral interconnect;

the interrupt-generating unit is arranged to send an interrupt to the processor in response to receiving a task signal from the programmable peripheral interconnect;

15 the programmable peripheral interconnect is configured to access a memory in which a mapping can be stored between (i) an event of a first peripheral and (ii) a task of the interrupt-generating unit or of a second peripheral; and

20 the programmable peripheral interconnect is configured so that, when a mapping is stored in memory between an event of a first peripheral and a task of the interrupt-generating unit, the programmable peripheral interconnect will respond to a signal of the event from the first peripheral by sending a task signal for the task to the interrupt-generating unit.

Any feature of any of the preceding arrangements and implementations may be a feature of this aspect also. In particular, the interrupt-generating unit may be an event-generating unit. It may therefore be arranged to detect a predetermined change to the
25 contents of an event-generating register and, in response to detecting such a predetermined change, to signal an event to the programmable peripheral interconnect. It may be an event-generating unit as previously described. The interrupt-generating unit may have any of the features of the event-generating units described herein. The programmable peripheral interconnect (PPI) may have any of
30 the features of the PPIs described previously.

The interrupt-generating unit may be connected to the programmable peripheral interconnect by a task line, and may send the task signal over the task line. Alternatively, it may write to a task register, which is monitored by the programmable
35 peripheral interconnect.

The event-generating peripheral may be configured to signal an event to the programmable peripheral interconnect over an event line. Alternatively, it may write to an event register, which is monitored by the programmable peripheral interconnect.

5

The interrupt-generating unit is preferably arranged to send the interrupt in direct response to receiving a task signal—preferably within a predetermined maximum time from receiving the task signal, or at a constant time delay after receiving a task signal.

10 The microcontroller may comprise a memory storing software, the software comprising instructions, executable by the processor, to store, in the mapping memory, a mapping from an event of the event-generating peripheral to a task of the interrupt-generating unit.

15 Although the event-generating register or registers are said to be part of the event-generating unit, it will be appreciated that this does not limit their physical location on the microcontroller. The event-generating registers are preferably addressable by the processor, e.g. over the bus. They can preferably be written to and/or read from by the processor. Each event-generating register may occupy a contiguous region of
20 memory, or it may be split across a plurality of locations. A register, as referred to herein, may be only a single bit long (possibly within a larger bit field), or it may comprise a plurality of bits (e.g. a 32-bit word).

The microcontroller preferably comprises volatile and/or non-volatile memory, such as
25 RAM and/or flash memory. A part of the memory may store program code.

The processor may be any suitable processor. In some embodiments it is a processor from ARM™, such as a processor from ARM™'s Cortex™ range. The microcontroller may comprise a plurality of buses, such as a processor bus and a peripheral bus. The
30 event-generating unit is preferably connected to one or more buses.

The microcontroller is preferably an integrated device, although it may, of course, require some off-chip components, such as a crystal, capacitors, etc., in order to operate. These components may be regarded as part of the microcontroller, or they
35 may be regarded as distinct from the microcontroller.

The interrupt- or event-generating unit is preferably a separate hardware module in the microcontroller, distinct from the processor. The interrupt- or event-generating unit may comprise analogue and/or digital components, including transistors, resistors, capacitors, etc., arranged to provide the functions described herein. The microcontroller may, of course, have other peripherals that are not connected to the programmable peripheral interconnect by a task line or that are not connected by an event line.

10 In some embodiments, the microcontroller comprises a radio transceiver. It may be a radio-on-a-chip device.

The following numbered sentences disclose certain arrangements for reference purposes.

15

- I. A microcontroller comprising:
a processor;
a plurality of peripherals;
a programmable peripheral interconnect;
20 an event-generating unit; and
a memory, storing software,

wherein:

the event-generating unit comprises an event-generating register, addressable by the processor;

25

the event-generating unit is connected to the programmable peripheral interconnect; and

the event-generating unit is arranged to detect a predetermined change to the contents of the event-generating register and, in response to detecting such a predetermined change, to signal an event to the programmable peripheral

30

interconnect;

each of the peripherals is connected to the programmable peripheral interconnect;

each of the peripherals is configured to respond to a task signal from the programmable peripheral interconnect by performing a respective task;

the programmable peripheral interconnect is configured to access a mapping memory in which a plurality of mappings can be stored, each mapping an event of the event-generating unit to a task of one of the peripherals;

5 the programmable peripheral interconnect is configured so that, when a mapping is stored in the mapping memory from an event of the event-generating unit to a task of one of the peripherals, the programmable peripheral interconnect will respond to a signal of the event from the event-generating unit by sending a task signal to the peripheral;

10 the programmable peripheral interconnect is configured so that, when the mapping memory stores mappings from one event of the event-generating unit to two or more different tasks, the programmable peripheral interconnect will send the two or more respective task signals within a predetermined maximum time from receiving a signal of the event; and

15 the software comprises instructions, executable by the processor, to (i) store, in the mapping memory, mappings from one event of the event-generating unit to at least two different peripheral tasks, and (ii) make said predetermined change to the contents of the event-generating register.

20 II. A microcontroller as described in numbered sentence I, wherein the predetermined maximum time is 10 microseconds or less.

25 III. A microcontroller as described in numbered sentence I or II, wherein the programmable peripheral interconnect is arranged to send the two or more respective task signals simultaneously.

30 IV. A microcontroller as described in numbered sentence III, wherein there is a constant time delay between the programmable peripheral interface receiving a signal of an event and sending two or more task signals that are mapped to the event, for all possible mappings,

35 V. A microcontroller as described in any preceding numbered sentence, comprising one or more peripherals that are event-generating, being configured to signal an event to the programmable peripheral interconnect, wherein the programmable peripheral interconnect is arranged so that, when a mapping is stored in the mapping memory between an event of a first peripheral and a task of a second

peripheral, the programmable peripheral interconnect will provide a channel by sending a task signal to the second peripheral in response to a signal of the event from the first peripheral.

5 VI. A microcontroller as described in any preceding numbered sentence, wherein the event-generating unit is arranged to signal a plurality of different events.

VII. A microcontroller as described in numbered sentence VI, wherein the event-generating unit has a plurality of event-generating registers, addressable by the
10 processor, wherein each event-generating register is associated with a different respective event.

VIII. A microcontroller as described in any preceding numbered sentence, wherein the event-generating unit is able to receive a task signal from the programmable
15 peripheral interconnect.

IX. A microcontroller as described in any preceding numbered sentence, wherein the programmable peripheral interface is connected to the peripherals and to the event-generating unit by respective lines for each event and task.
20

X. A microcontroller as described in any preceding numbered sentence, wherein the programmable peripheral interface comprises at least one event register, addressable by the processor, associated with an event of the event-generating unit.

25 XI. A microcontroller as described in numbered sentence X, wherein the event register is separate from the event-generating register and wherein the event-generating unit is configured so that a predetermined change to the contents of the event-generating register will cause a predetermined change to the contents of the event register.

30 XII. A microcontroller as described in any preceding numbered sentence, wherein the event-generating unit comprises a plurality of event-generating registers and a plurality of event registers, wherein each event-generating register is associated with a respective one of the event registers, such that a change to one of the event-
35 generating registers causes a change to an associated one of the event registers.

XIII. A microcontroller as described in numbered sentence X, wherein the event-generating register is the event register.

5 XIV. A microcontroller as described in any preceding numbered sentence, wherein the event-generating unit has no outputs other than one or more event lines to the PPI; zero or more interrupt lines to the processor; and zero or more registers.

XV. A microcontroller as described in any preceding numbered sentence, wherein
10 the event-generating unit has no inputs other than a clock input, one or more registers, and zero or more task lines.

XVI. A microcontroller as described in any preceding numbered sentence,
15 comprising circuitry for sending an interrupt to the processor when signalling an event.

XVII. A microcontroller as described in any preceding numbered sentence,
20 comprising a plurality of event-generating units, each connected to the processor by a set of interrupt lines, each set of interrupt lines having a different respective interrupt priority level.

Certain preferred embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a schematic drawing showing components of a first system embodying the invention.

25 Figure 2 is a table representing a memory structure storing mappings between peripheral registers;

Figure 3 is a schematic drawing of several peripherals connected to a PPI in a second system embodying the invention;

30 Figure 4 is a schematic drawing of elements relating to a particular channel within the PPI; and

Figure 5 is a schematic drawing showing an event-generating unit.

Figure 1 shows a microcontroller (MCU) 2 (e.g. an integrated circuit or a multi-chip module) which includes a central processing unit (CPU) 6, a main memory 8, and a

PPI 10, having a logic area 12 and an internal memory 14. The CPU 6 and PPI 10 are both connected to a bus 16.

Also connected to the bus 16 are an event-generating unit 17 and five exemplary peripherals: a timer 18, a digital-to-analogue converter (DAC) 20, a UART 22, a hardware encryption engine 24, a voltage comparator 26.

The timer 18 has an output event register 28, an overflow event register 30 and an input task registers 32. The DAC 20 has two conversion-finished event registers 36, 38 and two trigger task registers 40, 42. The UART 22 has an RX received event register 44, a TX complete event register 46, an RX trigger task register 48 and a TX trigger task register 50. The hardware encryption engine 24 has an encryption-finished event register 52 and a trigger task register 54, while the voltage comparator 26 has a single comparator output event register 56. Some of the registers are single-bit registers, while others can hold a multi-bit value. Of course, other embodiments may have different peripherals, and the peripherals may have any number of event or task registers.

The event-generating unit 17 has a first event register 57, a second event register 59, a first task register 61 and a second task register 63. Of course, other embodiments may have different numbers of event or task registers. In this embodiment, the event-generating unit 17 is arranged so that the first task triggers the first event, and so that the second task triggers the second event. In other embodiments, there may be more complex logic mapping task to events.

The registers of the peripherals 18-26 and the event-generating unit 17 share a memory addressing space with the main memory 8 and the PPI memory 14, so that they can be accessed using memory-mapped I/O by the PPI logic 12 and optionally by the CPU 6.

The bus 16 may be a single bus, as shown, or it may be formed from two or more separate buses.

In use, the CPU 6 might, for example, instruct the PPI 10 to create a channel connecting one of the DAC 20 conversion-finished events to the UART 22 trigger task,

so that the UART 22 transmits data after a DAC conversion has completed. On receiving this instruction, the PPI 10 creates a new entry in a table held in its memory 14, linking the address of the DAC 20 conversion-finished register 36 and the address of the UART 22 trigger task register 48.

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The CPU 6 might also, for example, instruct the PPI 10 to create a channel connecting the first event register 57 of the event-generating unit 17 to the TX trigger task register 50 of the UART 22, and another channel connecting the same first event register 57 of the event-generating unit 17 to an input task register 32 of the timer 18. In this way,
10 the CPU 6 can start the timer 18 at the same time as the UART 22 starts a transmission by writing a '1' bit to the first task register 61 of the event-generating unit 17. This process is atomic—i.e. it won't be interrupted by a CPU 6 interrupt.

Figure 2 shows an exemplary logical data structure which may be stored in the PPI's
15 memory 14. It has a number of rows, each of which contains a mapping number, an event register address and a task register address.

The PPI logic 12 is configured to poll every event register listed in the table periodically, to determine when a value in the register changes. When a change is
20 detected, the PPI logic 12 writes the new value (or a predetermined value, such as a binary '1') to all task registers which are mapped to the particular event register in the table.

The PPI logic 12 may optionally be configured to perform some processing on a new
25 value in the event register and instead write a result of the processing to one or more of the task registers. For example, if the event register contains a multi-bit value, the PPI logic 12 might determine whether it is higher than the previous value and write a one bit to a single-bit task register in accordance with a mapping in the memory 14. The PPI 10 could be instructed as to what processing (if any) to perform by the CPU 6.
30 The type of processing may be stored as a further column in the mapping table.

If the CPU 6 wants to deactivate a channel, it can do this straightforwardly by causing the relevant entry in the table stored in the PPI's memory 14 to be erased. It does not need to instruct the peripherals directly (although it may of course also do this, in some
35 circumstances).

Figures 3 - 5 relate to a set of embodiments in which the PPI 10 is connected to the peripherals 18-26 and the event-generating unit 17 by individual lines for each respective event and task signal. This may be done as an alternative to using the memory-mapped input/output as described above, or the MCU 2 might support both modes of communication (e.g., to allow the CPU 6 to interact with the peripherals via registers, and to allow the PPI 10 to interact with the peripherals via dedicated lines).

Figure 3 shows m peripherals which are connected to a PPI (which may be the same PPI 10 as above, or a different PPI). The event-generating unit 17 can be regarded as another peripheral for these purposes. The PPI provides n channels, each of which has an associated event end-point register (EEP) and task end-point register (TEP). Each of these registers can hold the address of a register on one of the peripherals.

Figure 4 provides more detail of elements associated with one of these n channels. Each of the channels has a similar set of elements. The channel's EEP is connected to an event signal lookup table which cross-references a set of peripheral event register addresses with an internal event line identifier which relates to one of the inputs to a multiplexer (MUX) in the PPI, associated with the channel. The PPI is configured to set the MUX to select the input associated with the address contained in the EEP.

Similarly, the channel's TEP is connected to a task signal lookup table which cross-references a set of peripheral task register addresses with an internal task line identifier which relates to one of the output of a demultiplexer (DEMUX) in the PPI, associated with the channel. The PPI is configured to set the DEMUX to select the output associated with the address contained in the TEP

Two peripherals A, B are connected to the channel's MUX. One of these may be an event-generating unit. Peripheral A can provide two event signals AE0, AE1, each of which has its own line into the MUX. Peripheral B can provide a single event signal BE0 which also has a line into the MUX. Similar lines will connect to the multiplexers of the other $n - 1$ channels (not shown).

The channel's DEMUX is connected to three output lines, one leading to a task input AT0 on peripheral A and two leading to different task inputs BT0, BT1 on peripheral B.

5 Within the PPI, the output from the MUX is connected through a switch to the input to the DEMUX. The connection is made when the switch is closed, so that an event signal (e.g. a pulse) from one of the peripheral selected by the MUX is passed to the DEMUX and thence on to a selected task input of one of the peripherals. The switch's state is controlled by a register, writable to by a CPU (not shown).

10 In some alternative arrangements, one channel may have multiple demultiplexers, each connected to the output of the channel's MUX. In this way, a single event can be forked so as to trigger a plurality of peripheral tasks.

15 The PPI is arranged to issue task signals within a predetermined maximum time from receiving an incoming event channel. In some embodiments, this time delay is constant for all channels. Signals on different or forked channels are handled in parallel.

20 Figure 5 figuratively illustrates the internals of the event-generating unit 17.

For a particular task n , the event-generating unit 17 is connected to the PPI 10 by an input task line 64 along which a task signal can be sent to trigger the task n . The event-generating unit 17 also has a task register 66 associated with the task n which sends a signal to trigger the task if firmware running on the CPU 6 writes a binary '1' to the task register 66. The contents of the task register 66 may also be updated automatically by the event-generating unit 17 when the PPI sends a task signal over the task line 64. The task line 64 from the PPI and an output indicating the state of the task register 66 are combined in a logical OR gate 68 and sent to the core 70 of the event-generating unit 17.

30 In a straightforward embodiment, the core 70 simply connects each task n with a respective event n in a one-to-one mapping. In more complex embodiments, the core 70 may include logic which associates one or more tasks to one or more events—for example, requiring both "task 1" and "task 2" to be triggered, in that order, before signalling "event 1".

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The core 70 can output an event signal for an event m . This causes the contents of an associated event register 72 to change to indicate that an event has been signalled (e.g., by changing the contents of a single-bit register from a binary '0' to a binary '1').

5 The same event signal is also split and sent to the PPI 10 over event output line 74.

This change to the event register 72 can also be configured to cause a signal to be sent over an interrupt signal line 76 to an interrupt controller in the CPU 6. Whether or not this interrupt signal is sent depends on the state of an interrupt-enable register 78, which can be written to by the CPU 6. If a binary '1' has been written in a bit position
10 corresponding to the event n then the switch 80 is closed and the interrupt signal will be sent.

The CPU 6 can use the event-generating unit 17, in combination with the PPI 10, in a
15 number of different ways.

For example, the CPU 6 may configure the PPI 10 to trigger two or more peripheral tasks in response to receiving a signal for an event n from the event-generating unit 17. The CPU 6 can then write a '1' bit to the task register 66 on the event-generating
20 unit 17, which will cause the event-generating unit 17 to send an event signal to the PPI 10 over the n th event signal line 74. The PPI 10 will then trigger all of the tasks simultaneously and atomically.

In another example, the CPU 6 may activate the m th interrupt signal line 76, and may
25 create a mapping for the PPI 10 that establishes a channel from an event of a peripheral to the m th input task line to the event-generating unit 17. The peripheral can then cause an interrupt to be sent to the CPU 6 by signalling the event to the PPI 10 over the appropriate event line connecting the peripheral to the PPI 10. In this way, the peripheral may be able to interrupt the CPU 6 at a different priority from a priority
30 assigned to its own interrupt line to the CPU 6.

It will be appreciated by those skilled in the art that the invention has been illustrated by describing one or more specific embodiments thereof, but is not limited to these
embodiments; many variations and modifications are possible, within the scope of the
35 accompanying claims.

Claims

1. A microcontroller comprising:
 - a processor;
 - a plurality of peripherals;
 - 5 a programmable peripheral interconnect; and
 - an interrupt-generating unit,wherein:
 - an event-generating one of the peripherals is configured to signal an event to the programmable peripheral interconnect;
 - 10 the interrupt-generating unit is arranged to send an interrupt to the processor in response to receiving a task signal from the programmable peripheral interconnect;
 - the programmable peripheral interconnect is configured to access a memory in which a mapping can be stored between (i) an event of a first peripheral and (ii) a task of the interrupt-generating unit or of a second peripheral; and
 - 15 the programmable peripheral interconnect is configured so that, when a mapping is stored in memory between an event of a first peripheral and a task of the interrupt-generating unit, the programmable peripheral interconnect will respond to a signal of the event from the first peripheral by sending a task signal for the task to the interrupt-generating unit.
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2. A microcontroller as claimed in claim 1, wherein the interrupt-generating unit is also an event-generating unit, arranged to detect a predetermined change to the contents of an event-generating register and, in response to detecting such a predetermined change, to signal an event to the programmable peripheral
25 interconnect.
3. A microcontroller as claimed in claim 1 or 2, wherein the interrupt-generating unit is arranged to send the interrupt within a predetermined maximum from receiving the task signal.
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4. A microcontroller as claimed in any preceding claim, wherein the interrupt-generating unit is arranged to send the interrupt at a constant time delay after receiving the task signal.

5. A microcontroller as claimed in any preceding claim, comprising a plurality of interrupt-generating units, each connected to the processor by a set of interrupt lines, each set of interrupt lines having a different respective interrupt priority level.
- 5 6. A microcontroller as claimed in any preceding claim, comprising a memory storing software, the software comprising instructions, executable by the processor, to store, in the mapping memory, a mapping from an event of the event-generating peripheral to a task of the interrupt-generating unit.
- 10 7. A microcontroller as claimed in any preceding claim, wherein the interrupt-generating unit is connected to the programmable peripheral interconnect by a task line.
8. A microcontroller as claimed in any preceding claim, wherein the interrupt-
15 generating unit is a separate hardware module in the microcontroller, distinct from the processor.
9. A microcontroller as claimed in any preceding claim, wherein the
20 microcontroller is a radio-on-a-chip device.



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Claims searched: 1-9

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Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1-9	WO 2013/088121 A1 (NORDIC SEMICONDUCTOR ASA) see e.g. the abstract, page 12 line 29 - page 1 line 28, page 17 lines 20-21 and figure 1
A	-	US 2008/258760 A1 (CYPRESS SEMICONDUCTOR CORP) see e.g. the abstract and paragraph 50

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^X :

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Worldwide search of patent documents classified in the following areas of the IPC

G06F

The following online and other databases have been used in the preparation of this search report

WPI, EPODOC, INSPEC

International Classification:

Subclass	Subgroup	Valid From
G06F	0013/24	01/01/2006
G06F	0009/54	01/01/2006
G06F	0013/20	01/01/2006