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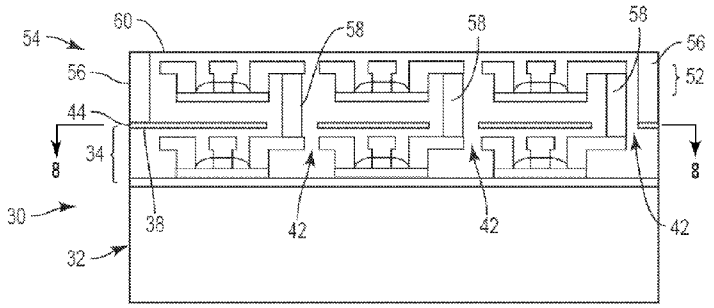

FIG. 7

(57) Abstract: A three-dimensional (3-D) integrated circuit (3DIC) with a graphene shield is disclosed. In certain embodiments, at least a graphene layer (38) is positioned between two adjacent tiers (34, 52) of the 3DIC. A graphene layer is a sheet like layer made of pure carbon, at least one atom thick with atoms arranged in a regular hexagonal pattern. A graphene layer may be disposed between any number of adjacent tiers in the 3DIC. In exemplary embodiments, the graphene layer provides an electromagnetic interference shield between adjacent tiers or layers in the 3DIC to reduce crosstalk between the tiers. In other exemplary embodiments, the graphene layer(s) can be disposed in the 3DIC to provide a heat sink that directs and dissipates heat to peripheral areas of the 3DIC. In some embodiments, the graphene layer(s) are configured to provide both EMI shielding and heat shielding.

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THREE-DIMENSIONAL (3D) INTEGRATED CIRCUITS (3DICS) WITH GRAPHENE SHIELD AND RELATED FABRICATION METHOD

PRIORITY APPLICATION

[0001] The present application claims priority to U.S. Patent Application Serial No. 13/765,061 filed on February 12, 2013 entitled "THREE-DIMENSIONAL (3-D) INTEGRATED CIRCUITS (3DICS) WITH GRAPHENE SHIELD, AND RELATED COMPONENTS AND METHODS," which is incorporated herein by reference in its entirety.

RELATED APPLICATION

[0002] The present application is related to U.S. Patent Application Serial No. 13/765,080, filed on February 12, 2013, entitled "ION REDUCED, ION CUT-FORMED THREE DIMENSIONAL, INTEGRATED CIRCUITS (3DICS), AND RELATED METHODS AND SYSTEMS."

BACKGROUND

I. Field of the Disclosure

[0003] The technology of the disclosure relates to three-dimensional integrated circuits (3DICs).

II. Background

[0004] Mobile communication devices have become common in current society. The prevalence of these mobile devices is driven in part by the many functions that are now enabled on such devices. Demand for such functions increases processing capability requirements and generates a need for more powerful batteries. Within the limited space of the housing of the mobile communication device, batteries compete with the processing circuitry. These and other factors contribute to a continued miniaturization of components and power consumption within the circuitry.

[0005] Miniaturization of the components impacts all aspects of the processing circuitry including the transistors and other reactive elements in the processing circuitry. One miniaturization technique involves arranging integrated circuits in not just an x-y coordinate system, but also in a z-coordinate system. That is, current miniaturization

techniques use three-dimensional (3D) integrated circuits (ICs) (3DICs) to achieve higher device packing density, lower interconnect delay, and lower costs. Currently, there are several techniques to manufacture or form 3DICs.

[0006] A first technique to form a 3DIC is selective epitaxial layer growth. Selective epitaxial layer growth can produce acceptably decent quality ICs, but this technique is expensive due to the rigorous requirements associated with the process. A second technique to form a 3DIC is a wafer-on-wafer manufacturing technique, whereby electronic components are built on two or more semiconductor wafers separately. The two or more semiconductor wafers are stacked, aligned, bonded, and diced into 3DICs. Through silicon vias (TSVs) are required and provided to effectuate electrical connections between the stacked wafers. Misalignment or TSV defects in any of the stacked wafers can result in an entirely defective integrated circuit due to the interdependence of the IC on the various layers. A third technique to form a 3DIC is a die-on-wafer technique, whereby electronic components are built on two semiconductor wafers. In this technique, one wafer is sliced and the singulated dice are aligned and bonded onto die sites of the second wafer. This die-on-wafer technique can also suffer from alignment issues. A fourth technique to form a 3DIC is a die-on-die technique whereby electronic components are built on multiple dice and then stacked, aligned, and bonded. This approach suffers from the same misalignment problem which may render the final 3DIC unusable.

[0007] A fifth technique to form a 3DIC is a monolithic technique, whereby electronic components and their connections are built in layers on a single semiconductor wafer. The layers are assembled through an ion-cutting process. The use of the layers in this fashion eliminates the need for precise alignment and TSVs. In the monolithic approach, a receptor wafer is prepared with integrated components thereon. An oxide layer forms on a top surface of the receptor wafer. A donor wafer is prepared by subjecting the donor wafer to an ion (typically hydrogen) implantation process. The surface of the donor wafer with the ion implantation is then stacked onto the oxide layer of the receptor wafer. The oxide layer of the receptor wafer bonds with the surface of the donor wafer through an annealing process. The donor wafer is then removed, transferring a silicon layer to the receptor wafer. Additional electronic components and interconnects are fabricated over the transfer silicon layer sequentially. The monolithic approach is less expensive than epitaxial growth and eliminates the risk

of misalignment, resulting in more functional devices than the techniques that rely on wafer-to-wafer, wafer-to-die, or die-to-die alignment.

[0008] The monolithic approach makes integrated circuits with small footprints, but the density of active components in the three-dimensional integrated circuit generates relatively greater amounts of heat than a simple two-dimensional integrated circuit. High temperatures can negatively impact performance of the active components in the circuit. Further, by arranging the circuit in three dimensions instead of just two dimensions, new opportunities for electromagnetic interference (EMI) or crosstalk between circuits are also created. EMI also negatively impacts performance of the active components in the circuit.

SUMMARY OF THE DETAILED DESCRIPTION

[0009] Embodiments disclosed in the detailed description include three-dimensional (3-D) integrated circuits (3DICs) with a graphene shield. Related components and methods are also disclosed. In certain embodiments disclosed herein, at least a graphene layer is positioned between two adjacent tiers of the 3DIC. A graphene layer is a sheet like layer made of pure carbon, at least one atom thick with atoms arranged in a regular hexagonal pattern. A graphene layer may be disposed between any number of adjacent tiers in the 3DIC. In exemplary embodiments, the graphene layer provides an electromagnetic interference (EMI) shield between adjacent tiers or layers in the 3DIC to reduce crosstalk between the tiers. Crosstalk between components in adjacent tiers in a 3DIC can negatively impact the performance of the 3DIC. In other exemplary embodiments, the graphene layer(s) can be disposed in the 3DIC to provide a heat sink that directs and dissipates heat to peripheral areas or heat sink of the 3DIC. In some embodiments, the graphene layer(s) are configured to provide both EMI shielding and heat shielding.

[0010] In this regard in one embodiment, a monolithic 3DIC is disclosed, the 3DIC comprises a first semiconductor integrated circuit tier comprising a first component. The 3DIC also comprises a second semiconductor integrated circuit tier comprising a second component vertically positioned relative to the first semiconductor integrated circuit tier. The 3DIC also comprises at least one graphene layer disposed between the first and second semiconductor integrated circuit tiers in such a manner that the at least one graphene layer is not part of the first or second component.

[0011] In another embodiment, a monolithic three-dimensional integrated circuit is disclosed. The 3DIC comprises a first means for providing a semiconductor tier comprising a first component. The 3DIC also comprises a second means for providing a semiconductor tier comprising a second component vertically positioned relative to the first means for providing the semiconductor tier. The 3DIC also comprises at least one graphene layer disposed between the first and second means for providing semiconductor tiers in such a manner that the at least one graphene layer is not part of the first or second component.

[0012] In another embodiment a method of forming a monolithic three-dimensional integrated circuit is disclosed. The method comprises providing a first semiconductor tier comprising a first component. The method also comprises positioning at least one layer of graphene on a surface of the first semiconductor tier. The method also comprises electrically isolating the first component from the at least one layer of graphene. The method also comprises providing a second semiconductor tier comprising a second component over the at least one layer of graphene such that the at least one layer of graphene is between the first and second semiconductor tiers and the second component is electrically isolated from the at least one layer of graphene.

BRIEF DESCRIPTION OF FIGURES

[0013] Figures 1A-1D illustrate exemplary conventional steps in an ion cutting process to assemble a three-dimensional (3-D) integrated circuit (IC) (3DIC);

[0014] Figure 2 illustrates a flow chart setting forth an exemplary conventional process for ion cutting;

[0015] Figure 3 illustrates an exemplary graphene transfer in the construction of a 3DIC;

[0016] Figure 4 illustrates an exemplary etching step in the construction of a 3DIC;

[0017] Figure 5 illustrates an exemplary silicon transfer step in the construction of a 3DIC;

[0018] Figure 6 illustrates an exemplary second tier creation step in the construction of a 3DIC;

[0019] Figure 7 illustrates an exemplary completed 3DIC including a graphene shield;

[0020] Figure 8 illustrates an exemplary cross-sectional view of the 3DIC of Figure 7 taken along lines 8-8;

[0021] Figure 9 is a flowchart illustrating an exemplary process for the construction of a 3DIC as illustrated in Figures 3-8; and

[0022] Figure 10 is a block diagram of an exemplary processor-based system that can include the shielded 3DIC of Figure 8.

DETAILED DESCRIPTION

[0023] With reference now to the drawing figures, several exemplary embodiments of the present disclosure are described. The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any embodiment described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments.

[0024] Embodiments disclosed in the detailed description include three-dimensional (3-D) integrated circuits (3DICs) with a graphene shield. Related components and methods are also disclosed. In certain embodiments disclosed herein, at least a graphene layer is positioned between two adjacent tiers of the 3DIC. A graphene layer is a sheet like layer made of pure carbon, at least one atom thick with atoms arranged in a regular hexagonal pattern. A graphene layer may be disposed between any number of adjacent tiers in the 3DIC. In exemplary embodiments, the graphene layer provides an electromagnetic interference (EMI) shield between adjacent tiers or layers in the 3DIC to reduce crosstalk between the tiers. Crosstalk between components in adjacent tiers in a 3DIC can negatively impact the performance of the 3DIC. In other exemplary embodiments, the graphene layer(s) can be disposed in the 3DIC to provide a heat sink that directs and dissipates heat to peripheral areas of the 3DIC. In some embodiments, the graphene layer(s) are configured to provide both EMI shielding and heat shielding.

[0025] Before discussing embodiments of a shielded 3DIC that includes a thermal shield and an EMI shield, a brief overview of a conventional process used in the assembly of a three-dimensional integrated circuit is provided with reference to Figures 1A-1D and Figure 2. The discussion of exemplary embodiments of a three-dimensional integrated circuit with a thermal and EMI shield begins below with reference to Figure 3.

[0026] In this regard, Figure 1A illustrates a first step of a conventional process to create a three-dimensional integrated circuit (3DIC). Specifically, a receptor wafer 10 is provided having a substrate 12 such as a silicon (Si) substrate. The substrate 12 may be referred to as a substrate means. A first tier of electronic components (generically indicated at 14) are grown on the substrate 12 as is well known. An oxide layer 16 is grown over the electronic components 14. Concurrently a donor wafer 18 is prepared. The donor wafer 18 may be referred to as a donor means. The donor wafer 18 may also be a silicon material. The donor wafer 18 is implanted with ions to form an ionized region 22, which effectively separates a handling portion 20 from a donor portion 24. Conventional implantation processes allow the creation of a localized, high concentration zone (sometimes called a Delta implant zone). In an exemplary process, the ions are hydrogen ions. An oxide layer 26 is grown on the donor portion 24.

[0027] With reference to Figure 1B, the donor wafer 18 is stacked on top of the receptor wafer 10 such that the oxide layer 16 is in contact with the oxide layer 26. The oxide layers 16, 26 may be referred to as a means for bonding. The oxide layers 16, 26 bond and are annealed through a relatively low temperature process (e.g., between approximately 250°C and 350°C). Following annealing, the donor wafer 18 is cleaved from the receptor wafer 10 as illustrated in Figure 1C. The oxide layer 26, the donor portion 24, and a cleaved portion 22A of the ionized region 22 remain attached to the receptor wafer 10 and a residual portion 22B of the ionized region 22 remains on the handling portion 20 of the donor wafer 18 as is well understood.

[0028] After cleaving, with reference to Figure 1D additional electronic components 28, such as transistors are grown on the donor portion 24 to form a second tier of electronic components30. Additional tiers of electronic components beyond the second tier of electronic components 30 (not illustrated) may be created by repeating the process to create a multi-level or multi-tier 3DIC.

[0029] With Figures 1A-1D providing a visual depiction of an exemplary conventional ion cutting process 50, this conventional ion cutting process 50 is further presented in flow chart form in Figure 2. The conventional ion cutting process 50 begins with the preparation of the receptor wafer 10 (block 52). Preparation of the receptor wafer 10 involves preparing the substrate 12 and may involve doping, curing, cutting, or other techniques as is well understood. Once prepared, a first tier of electronic components 14 are grown on the receptor wafer 10 (block 54). Once the

electronic components 14 are grown, an oxide layer 16 is grown on the receptor wafer 10 (block 56, see also Figure 1A).

[0030] With continued reference to Figure 2, concurrently or sequentially, ions are implanted in the donor wafer 18 to form the ionized region 22 (block 58, see also Figure 1A). As noted above, the ions are, in an exemplary embodiment, hydrogen ions. Oxide layer 26 is grown on the donor wafer 18 as well. The donor wafer 18 is placed on the receptor wafer 10 (block 60, see also Figure 1B). The donor wafer 18 is annealed (typically at a temperature range of approximately 250 to 350°C) (block 62), fusing the oxide layers 16, 26. The annealing takes place until cracking of the ionized region 22 takes place, which enables the transfer of a donor portion 24 and cleaved portion 22A from the donor wafer 18 to the receptor wafer 10. This transfer is referred to as cleaving the donor wafer 18 (block 64, see also Figure 1C). In exemplary methodologies the donor portion 24 is approximately 1.3 μm thick. Following the transfer, a second tier of electronic components 30 may be grown on the donor portion 24 (block 66, see also Figure 1D).

[0031] In conventional processes such as that shown in Figure 2 resulting in the 3DIC 26, heat may accumulate within the 3DIC as the electronic components within the tiers of electronic components 14, 24 consume power. Likewise, electronic components within a first tier of electronic components 14 may have crosstalk with electronic components within a second tier of electronic components 24 and vice versa. As the number of tiers of electronic components increases, the heat and crosstalk issues are exacerbated. Failure to dissipate heat negatively impacts the 3DIC by changing the conductivity of the materials in the 3DIC and, if the heat is too great, the materials may melt and reflow in such a manner that the 3DIC is ruined. Likewise, crosstalk, while not likely to destroy the device, causes signals intended for the operation of a first device to show up in a second device, causing the second device to operate in an undesired manner. Alternatively, such crosstalk may exceed relevant laws and regulations (e.g., the Federal Communications Commission (FCC) imposes limits on the amount of EMI radiation a device may emit). Failure to comply with such laws and regulations may mean that the device cannot be sold in certain jurisdictions or markets (e.g., failure to comply with FCC rules means that the device may not operate in the US). The present disclosure addresses these issues by providing an EMI shield between tiers of electronic components. In an exemplary embodiment, the EMI shield is a

graphene layer. As noted above, a graphene layer is a sheet like layer made of pure carbon, at least one atom thick with atoms arranged in a regular hexagonal pattern. Graphene is ten times as thermally conductive as copper and has one hundred times the electron mobility of silicon and accordingly, acts as both a thermal shield and an EMI shield that reduces crosstalk.

[0032] In this regard, Figure 3 illustrates an under construction 3DIC 30 with a substrate 32. In an exemplary embodiment, the substrate 32 may be silicon. A first tier of electronic components 34 have been created on the substrate 32 using conventional processes. A layer of oxide 36 may encapsulate or top the first tier of electronic components 34. A layer of graphene 38 is applied to the layer of oxide 36 using a polymethyl methacrylate (PMMA) holding substrate 40. Use of such PMMA holding substrates 40 to transfer graphene is understood within the art. In an exemplary embodiment, the layer of graphene 38 is formed from a layer of graphene a single atom thick. In another exemplary embodiment, the layer of graphene is formed from a layer of graphene more than one atoms thick (i.e, a bi-layer). It should be noted that for the layer of graphene 38 to be an effective EMI shield, the layer of graphene 38 is not electrically connected to any component within the first tier of electronic components 34. That is, the layer of graphene 38 is electrically isolated from the components within the first tier of electronic components 34.

[0033] The PMMA holding substrate 40 is removed and the layer of graphene 38 is etched into a pattern that includes one or more apertures 42 as illustrated in Figure 4. In an exemplary embodiment, the apertures 42 are proximate an edge 44 of the under construction 3DIC 30. In another exemplary embodiment, the apertures 42 are spaced inwardly from the edge 44 of the under construction 3DIC 30. In an exemplary embodiment, the etching may be performed through any conventional technique as desired. In another exemplary embodiment, the apertures 42 are made through some process other than etching.

[0034] With reference to Figure 5, an oxide layer 46 is grown over the layer of graphene 38 and used to bond to another layer of silicon 48 through an ion cut process. The top 50 of the layer of silicon 48 may be subjected to a chemical mechanical polish and oxidation process to remove excess ions as described in U.S. Patent Application Serial No. 13/765,080, entitled "ION REDUCED, ION CUT-FORMED THREE-DIMENSIONAL (3D) INTEGRATED CIRCUITS (IC) (3DICS), AND RELATED

METHODS AND SYSTEMS", filed February 12, 2013. The new layer of silicon 48 may be doped (e.g., p-doping, n-doping) as desired. Still other well known preparatory steps may be included in the ion cutting process.

[0035] With reference to Figure 6, a second tier of electronic components 52 are grown on the under construction 3DIC 30 and in particular grown on the layer of silicon 48. Individual components 53 may be positioned relative to apertures 42 to effectuate vias as will be explained below with reference to Figures 7 and 8. It should be noted that for the layer of graphene 38 to be an effective EMI shield, the layer of graphene 38 is not electrically connected to any component 53 within the second tier of electronic components 52. That is, the layer of graphene 38 is electrically isolated from the components 53 within the second tier of electronic components 52.

[0036] With reference to Figure 7, a completed 3DIC 54 is illustrated. The completed 3DIC 54 includes thermal vias 56 positioned proximate the edge 44. The layer of graphene 38 is an excellent heat conductor, and together with the thermal vias 56, heat may be conveyed from the center of the 3DIC 54 to an edge 44 and dissipated. In an exemplary embodiment, the thermal vias are directly connected to the layer of graphene 38 such that heat may pass from the layer of graphene 38 to the thermal via 56. The placement of the thermal vias 56 proximate the edge 44 allows heat to dissipate from the edge of the completed 3DIC 54. Such heat dissipation effectively removes heat from the center portions of the completed 3DIC 54 and protects the completed 3DIC 54 from overheating. Additionally, inter-tier connect vias 58 may be positioned interiorly spaced relative to the edge 44 to connect individual components in the first tier of electronic components 34 with individual components in the second tier of electronic components 52. The inter-tier connect vias 58 extend through the apertures 42. In an exemplary embodiment, the layer of graphene 38 is connected to ground (not illustrated). By grounding the layer of graphene 38, an effective EM shield is created.

[0037] A cross-sectional view of the completed 3DIC 54 is illustrated in Figure 8. As illustrated, the completed 3DIC 54 may include interior thermal vias 56 (one shown) as well as the interiorly positioned inter-tier connect vias 58. As illustrated in both Figures 7 and 8, the inter-tier connect vias 58 are spaced from the edges of the apertures 42 so that there is no electrical connection between the layer of graphene 38 and the inter-tier connect vias 58. Preservation of the electrical isolation between the inter-tier

connect vias 58 and the layer of graphene 38 helps preserve the EM shielding function of the layer of graphene 38.

[0038] While not illustrated, it should be appreciated that additional tiers may be grown on top of the second tier of electronic components 52. Such additional tiers may also have a shield positioned therebetween as discussed herein. As a further note, while graphene is described in the exemplary embodiments herein, other substances may also be used as the shield. However, graphene is well suited for the purpose outlined herein because of its combination of thermal conductivity and electron mobility. Accordingly, other suitable materials may include those having a thermal conductivity at least five times greater than copper and an electron mobility at least fifty times greater than silicon.

[0039] The process 70 of forming the completed 3DIC 54 is summarized with reference to Figure 9. The process 70 begins with the substrate 32 being prepared (block 72). Such preparation may include doping, creation of isolation trenches and the like as is well understood. The process 70 continues with the growth of the first tier of electronic components 34 (block 74). Such growth may be done through epitaxial growth, vapor deposition, etching, or the like as is well understood.

[0040] With continued reference to Figure 9, the process 70 continues by placing a layer of graphene 38 over the first tier of electronic components 34 (block 76). The layer of graphene 38 may be transferred through the use of a PMMA holding substrate 40 as previously described. The process 70 continues with the apertures 42 created in the layer of graphene 38 through a predefined pattern (block 78). The apertures 42 may be created through etching or similar process as desired.

[0041] With continued reference to Figure 9, the process continues by transferring the second silicon layer 48 over the layer of graphene 38 (block 80). The second silicon layer 48 may be transferred through an ion cutting process as is well known. The second silicon layer 48 may be processed (block 82) to remove ions, smooth the surface and otherwise prepare the second silicon layer 48 for the second tier of electronic components 52. That is, after processing the second silicon layer 48, the second tier of electronic components 52 is defined (block 84). The definition of the second tier of electronic components 52 may be through epitaxial growth, vapor deposition, etching, or the like as is well understood. The vias 56 and 58 are then formed (block 86) and the

completed 3DIC 54 of Figure 7 is finished. Additional tiers of electronic components with additional shielding layers may be provided if desired.

[0042] The 3DIC with graphene shield according to embodiments disclosed herein may be provided in or integrated into any processor-based device. Examples, without limitation, include a set top box, an entertainment unit, a navigation device, a communications device, a fixed location data unit, a mobile location data unit, a mobile phone, a cellular phone, a computer, a portable computer, a desktop computer, a personal digital assistant (PDA), a monitor, a computer monitor, a television, a tuner, a radio, a satellite radio, a music player, a digital music player, a portable music player, a digital video player, a video player, a digital video disc (DVD) player, and a portable digital video player.

[0043] In this regard, Figure 10 illustrates an example of a processor-based system 110 that can employ a 3DIC. In this example, the processor-based system 110 includes one or more central processing units (CPUs) 112, each including one or more processors 114. The CPU(s) 112 may have cache memory 116 coupled to the processor(s) 114 for rapid access to temporarily stored data. The CPU(s) 112 is coupled to a system bus 118 and can intercouple master devices and slave devices included in the processor-based system 110. As is well known, the CPU(s) 112 communicates with these other devices by exchanging address, control, and data information over the system bus 118. For example, the CPU(s) 112 can communicate bus transaction requests to the memory controller 120. Although not illustrated in Figure 10, multiple system buses 118 could be provided, wherein each system bus 118 constitutes a different fabric.

[0044] Other devices can be connected to the system bus 118. As illustrated in Figure 10, these devices can include a memory system 122, one or more input devices 124, one or more output devices 126, one or more network interface devices 128, and one or more display controllers 130, as examples. The input device(s) 124 can include any type of input device, including but not limited to input keys, switches, voice processors, etc. The output device(s) 126 can include any type of output device, including but not limited to audio, video, other visual indicators, etc. The network interface device(s) 128 can be any devices configured to allow exchange of data to and from a network 132. The network 132 can be any type of network, including but not limited to a wired or wireless network, private or public network, a local area network (LAN), a wide local area network (WLAN), and the Internet. The network interface

device(s) 128 can be configured to support any type of communication protocol desired. The memory system 122 can include one or more memory units 134(0-N).

[0045] The CPU(s) 112 may also be configured to access the display controller(s) 130 over the system bus 118 to control information sent to one or more displays 136. The display controller(s) 130 sends information to the display(s) 136 to be displayed via one or more video processors 138, which process the information to be displayed into a format suitable for the display(s) 136. The display(s) 136 can include any type of display, including but not limited to a cathode ray tube (CRT), a liquid crystal display (LCD), a plasma display, etc.

[0046] Those of skill in the art will further appreciate that the various illustrative logical blocks, modules, circuits, and algorithms described in connection with the embodiments disclosed herein may be implemented as electronic hardware, instructions stored in memory or in another computer-readable medium and executed by a processor or other processing device, or combinations of both. The arbiters, master devices, and slave devices described herein may be employed in any circuit, hardware component, integrated circuit (IC), or IC chip, as examples. Memory disclosed herein may be any type and size of memory and may be configured to store any type of information desired. To clearly illustrate this interchangeability, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. How such functionality is implemented depends upon the particular application, design choices, and/or design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.

[0047] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a processor, a DSP, an Application Specific Integrated Circuit (ASIC), an FPGA or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a

combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0048] The embodiments disclosed herein may be embodied in hardware and in instructions that are stored in hardware, and may reside, for example, in Random Access Memory (RAM), flash memory, Read Only Memory (ROM), Electrically Programmable ROM (EPROM), Electrically Erasable Programmable ROM (EEPROM), registers, a hard disk, a removable disk, a CD-ROM, or any other form of computer readable medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a remote station. In the alternative, the processor and the storage medium may reside as discrete components in a remote station, base station, or server.

[0049] It is also noted that the operational steps described in any of the exemplary embodiments herein are described to provide examples and discussion. The operations described may be performed in numerous different sequences other than the illustrated sequences. Furthermore, operations described in a single operational step may actually be performed in a number of different steps. Additionally, one or more operational steps discussed in the exemplary embodiments may be combined. It is to be understood that the operational steps illustrated in the flow chart diagrams may be subject to numerous different modifications as will be readily apparent to one of skill in the art. Those of skill in the art will also understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0050] The previous description of the disclosure is provided to enable any person skilled in the art to make or use the disclosure. Various modifications to the disclosure will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other variations without departing from the spirit or scope of the disclosure. Thus, the disclosure is not intended to be limited to the examples and

designs described herein, but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. A monolithic three-dimensional (3-D) integrated circuit (3DIC), comprising:

a first semiconductor integrated circuit tier comprising a first component;

a second semiconductor integrated circuit tier comprising a second component vertically positioned relative to the first semiconductor integrated circuit tier; and

at least one graphene layer disposed between the first and second semiconductor integrated circuit tiers in such a manner that the at least one graphene layer is not part of the first or second component.

2. The monolithic 3DIC of claim 1, wherein the at least one graphene layer is coupled to ground and provides electromagnetic shielding between the first and second semiconductor integrated circuit tiers.

3. The monolithic 3DIC of claim 1, wherein the at least one graphene layer is configured to conduct heat away from interiorly positioned active elements within the first and second semiconductor integrated circuit tiers.

4. The monolithic 3DIC of claim 1, wherein the at least one graphene layer defines at least one aperture.

5. The monolithic 3DIC of claim 4, further comprising a conductive via passing through the at least one aperture and coupling a first active component in the first semiconductor integrated circuit tier and a second active component in the second semiconductor integrated circuit tier.

6. The monolithic 3DIC of claim 1, further comprising a thermal via thermally contiguous to the at least one graphene layer.

7. The monolithic 3DIC of claim 4, wherein the monolithic 3DIC comprises an exterior edge and the at least one aperture is proximate the exterior edge.

8. The monolithic 3DIC of claim 4, wherein the monolithic 3DIC comprises a center and the at least one aperture is proximate the center.

9. The monolithic 3DIC of claim 4, wherein the monolithic 3DIC comprises an exterior edge and the at least one aperture is spaced inwardly from the exterior edge.

10. The monolithic 3DIC of claim 7, further comprising a thermal via passing through the at least one aperture.

11. The monolithic 3DIC of claim 1, further comprising a bonding layer bonding the first semiconductor integrated circuit tier to the second semiconductor integrated circuit tier and wherein the at least one graphene layer is positioned below the bonding layer in the first semiconductor integrated circuit tier.

12. The monolithic 3DIC of claim 1, further comprising a bonding layer bonding the first semiconductor integrated circuit tier to the second semiconductor integrated circuit tier and wherein the at least one graphene layer is positioned above the bonding layer in the second semiconductor integrated circuit tier.

13. The monolithic 3DIC of claim 11, wherein the bonding layer comprises an annealed oxide layer.

14. The monolithic 3DIC of claim 1 integrated into a semiconductor die.

15. The monolithic 3DIC of claim 1, further comprising a device selected from the group consisting of: a set top box, an entertainment unit, a navigation device, a communications device, a fixed location data unit, a mobile location data unit, a mobile phone, a cellular phone, a computer, a portable computer, a desktop computer, a personal digital assistant (PDA), a monitor, a computer monitor, a television, a tuner, a radio, a satellite radio, a music player, a digital music player, a portable music player, a digital video player, a video player, a digital video disc (DVD) player, and a portable digital video player, into which the monolithic 3DIC is integrated.

16. A monolithic three-dimensional (3-D) integrated circuit (3DIC), comprising:

a first means for providing a semiconductor tier comprising a first component;

a second means for providing a semiconductor tier comprising a second component vertically positioned relative to the first means for providing the semiconductor tier; and

at least one graphene layer disposed between the first and second means for providing semiconductor tiers in such a manner that the at least one graphene layer is not part of the first or second component.

17. A method of forming a monolithic three-dimensional (3-D) integrated circuit (3DIC) comprising:

providing a first semiconductor tier comprising a first component;

positioning at least one layer of graphene on a surface of the first semiconductor tier;

electrically isolating the first component from the at least one layer of graphene; and

providing a second semiconductor tier comprising a second component over the at least one layer of graphene such that the at least one layer of graphene is between the first and second semiconductor tiers and the second component is electrically isolated from the at least one layer of graphene.

18. The method of claim 17, further comprising providing an aperture in the at least one layer of graphene.

19. The method of claim 18, further comprising a conductive via through the aperture to couple electrically a first element in the first semiconductor tier to a second element in the second semiconductor tier.

20. The method of claim 18, further comprising a thermal via through the aperture to conduct heat within the monolithic 3DIC.

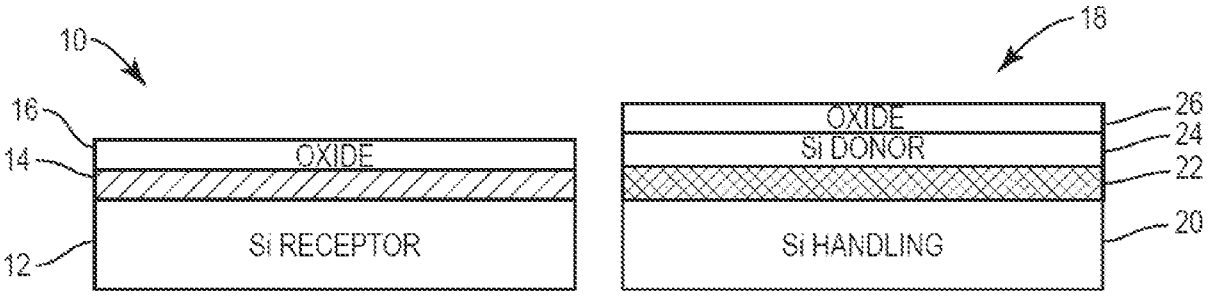

FIG. 1A
PRIOR ART

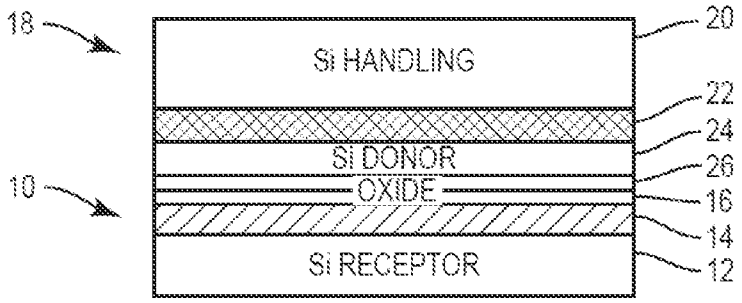

FIG. 1B
PRIOR ART

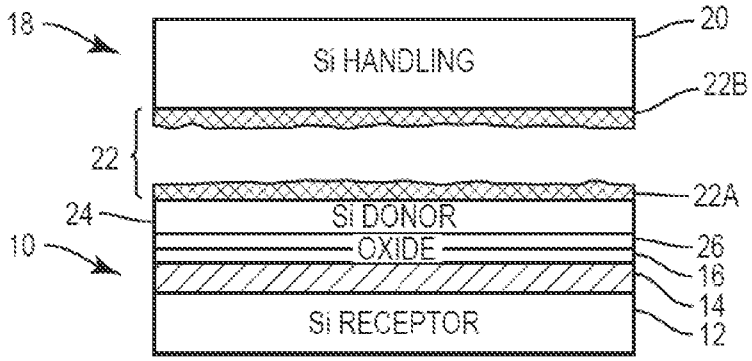

FIG. 1C
PRIOR ART

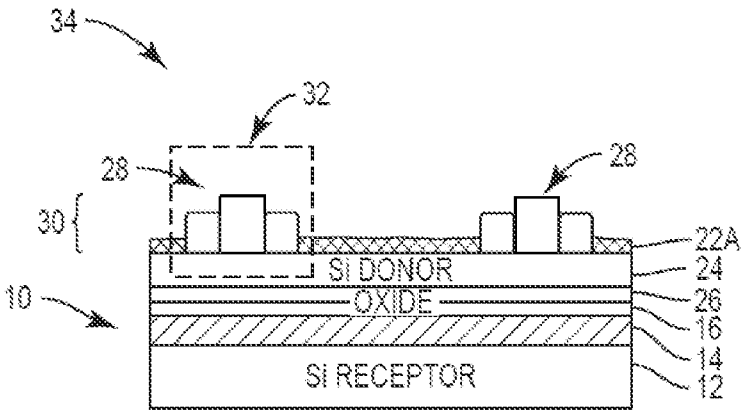

FIG. 1D
PRIOR ART

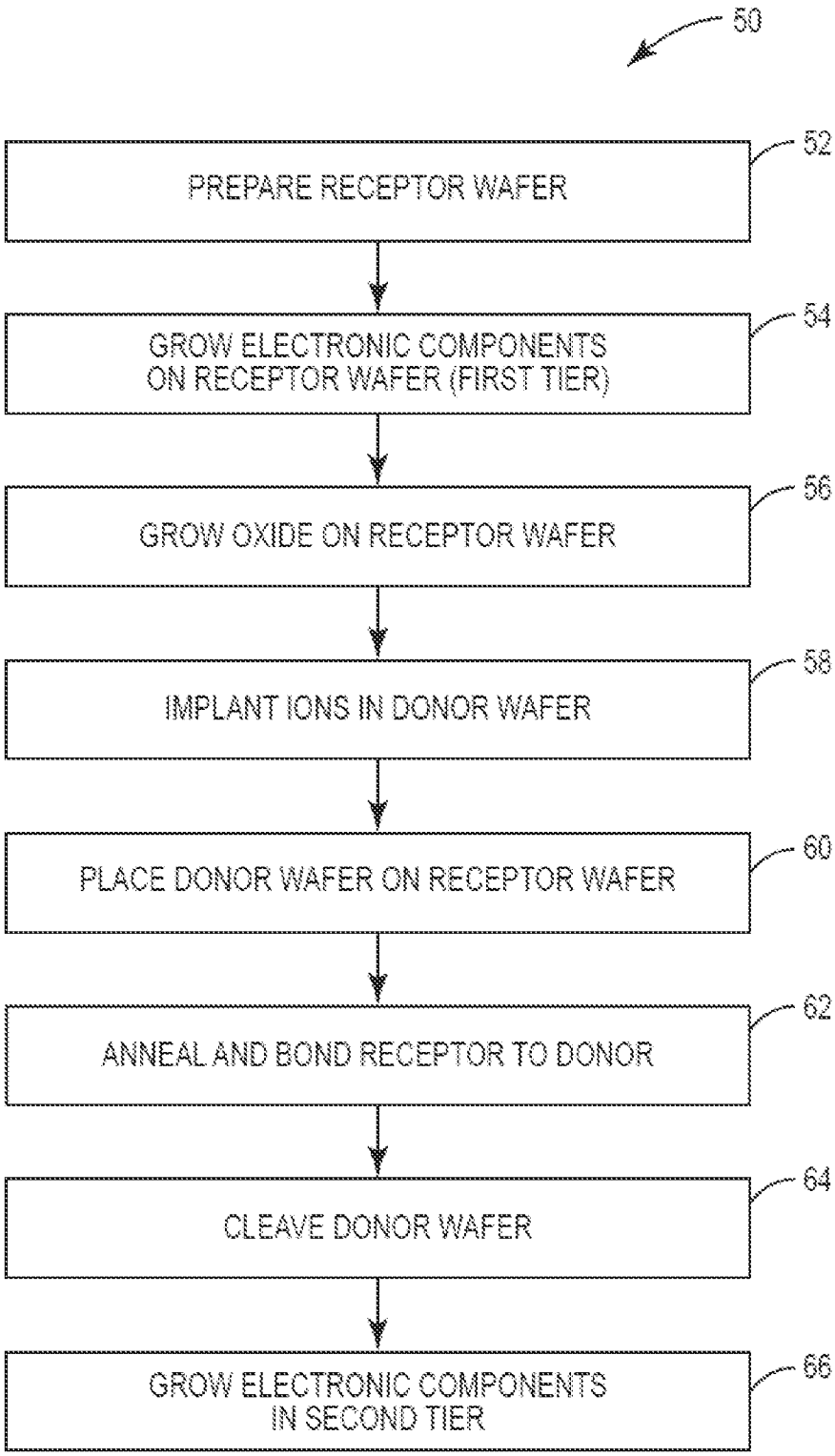

FIG. 2
PRIOR ART

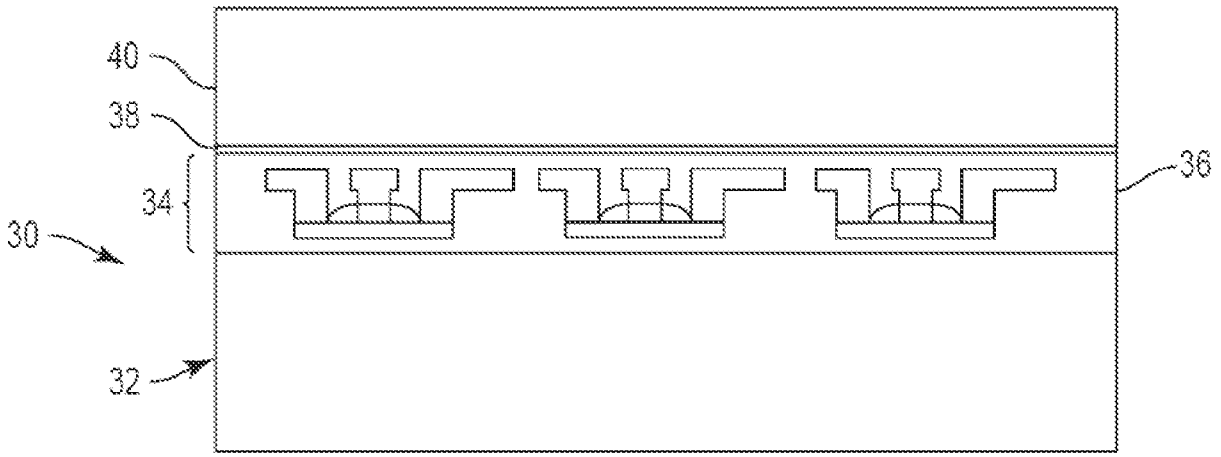

FIG. 3

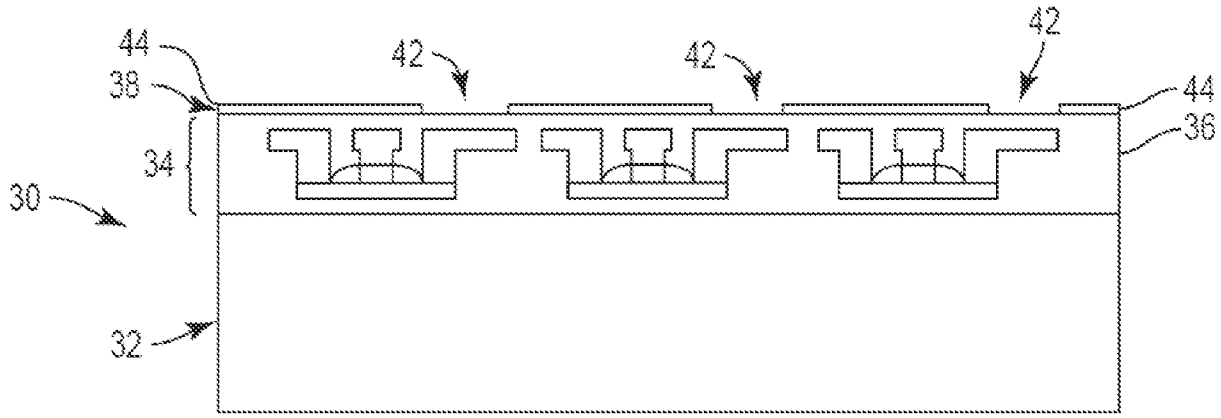

FIG. 4

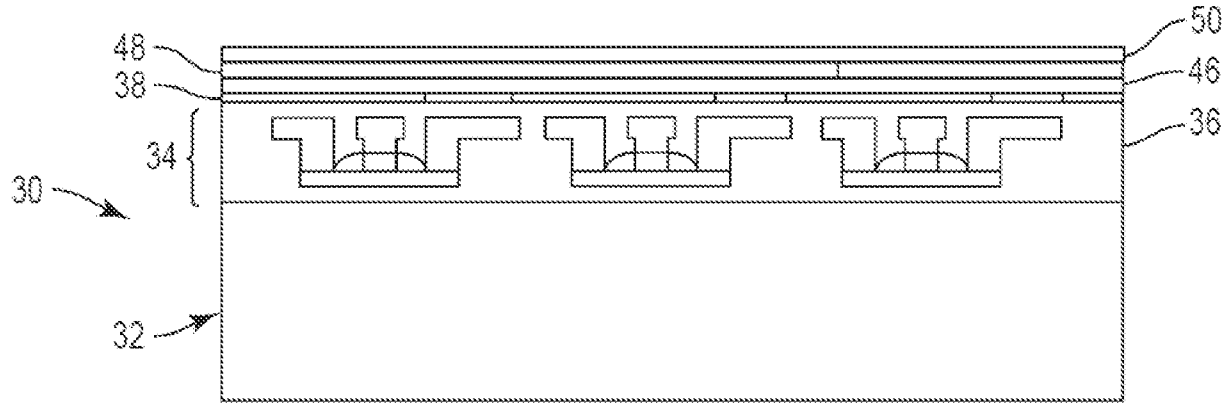

FIG. 5

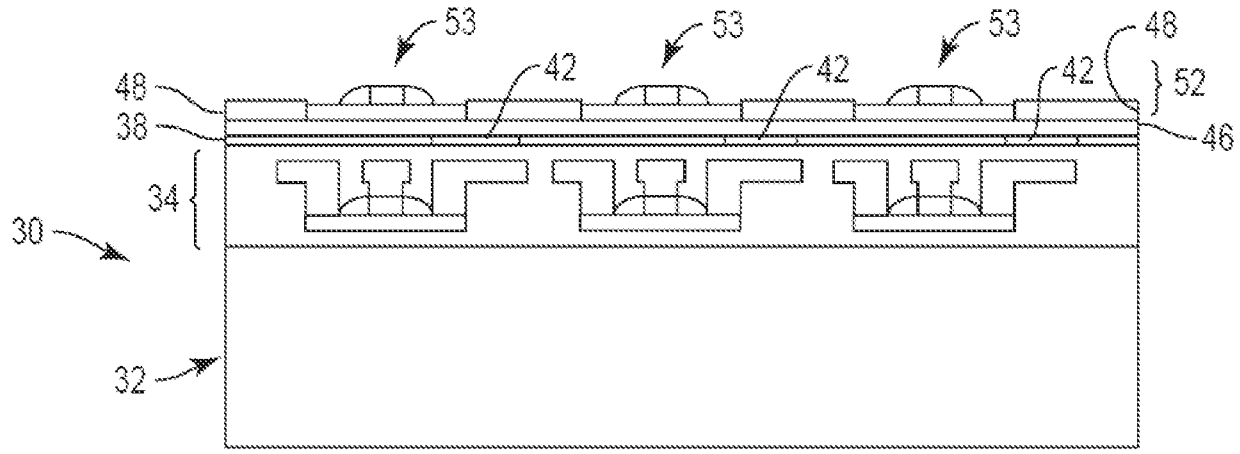
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FIG. 6

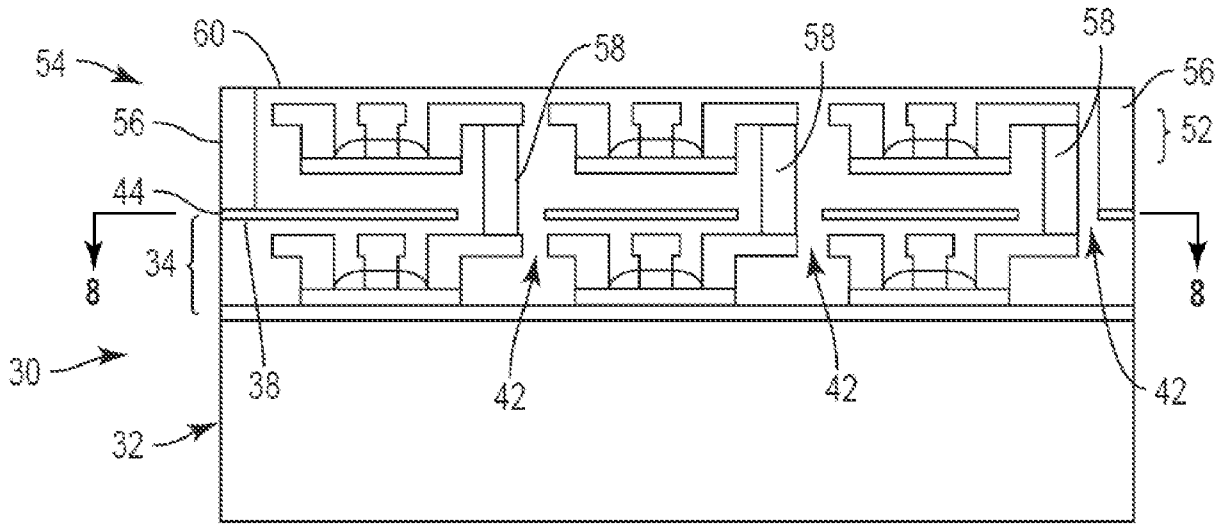
60
58
58
58
54
56
56
52
44
34
8
8
30
38
42
42
42
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FIG. 7

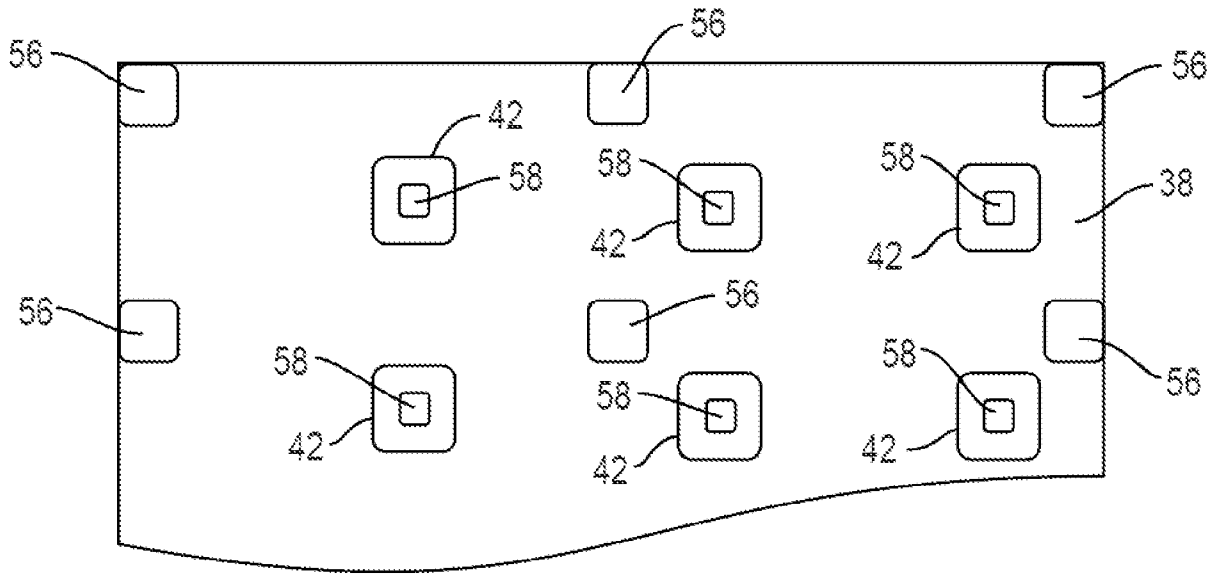

FIG. 8

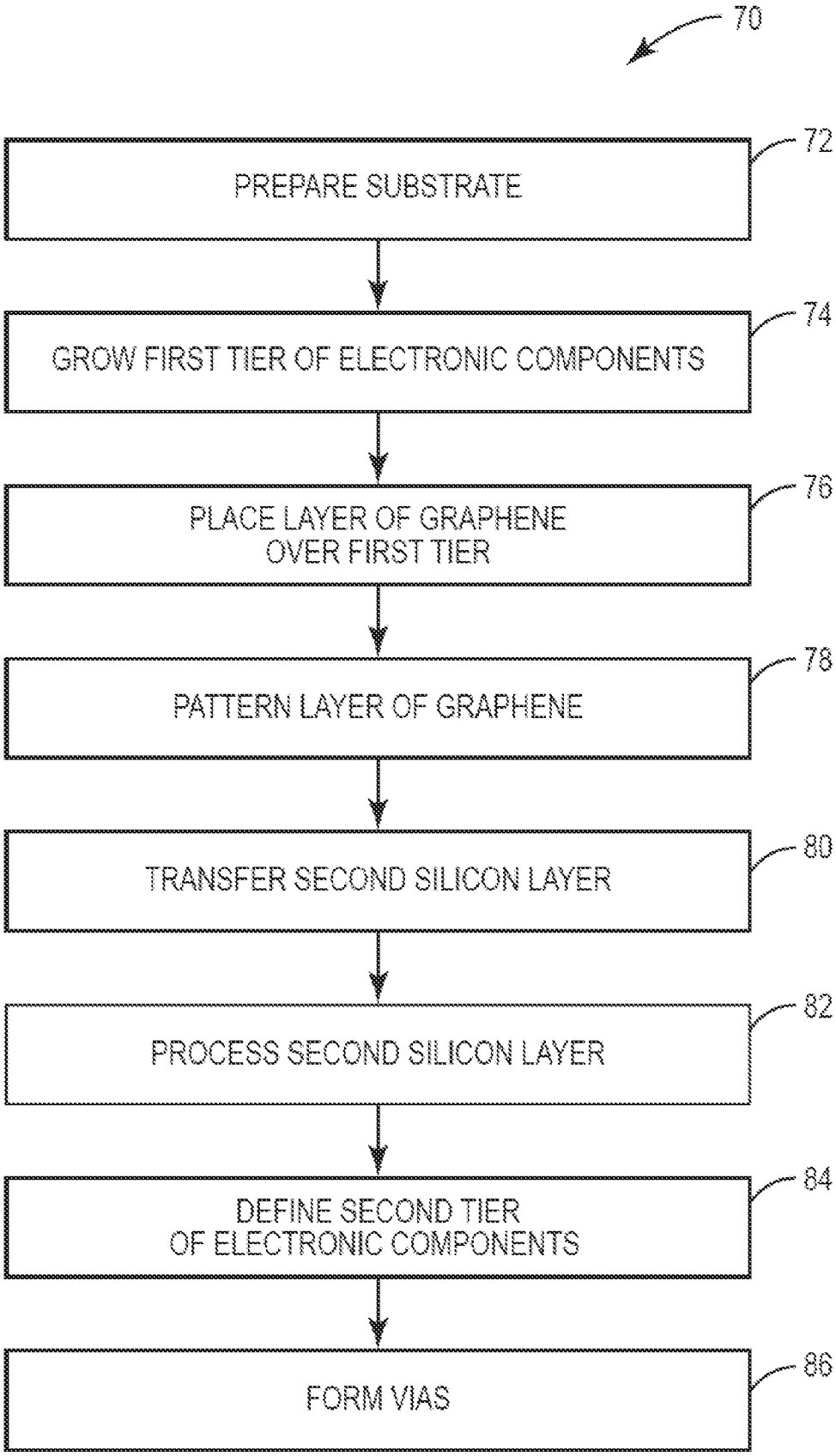
70
PREPARE SUBSTRATE
72
GROW FIRST TIER OF ELECTRONIC COMPONENTS
74
PLACE LAYER OF GRAPHENE OVER FIRST TIER
76
PATTERN LAYER OF GRAPHENE
78
TRANSFER SECOND SILICON LAYER
80
PROCESS SECOND SILICON LAYER
82
DEFINE SECOND TIER OF ELECTRONIC COMPONENTS
84
FORM VIAS
86

FIG. 9

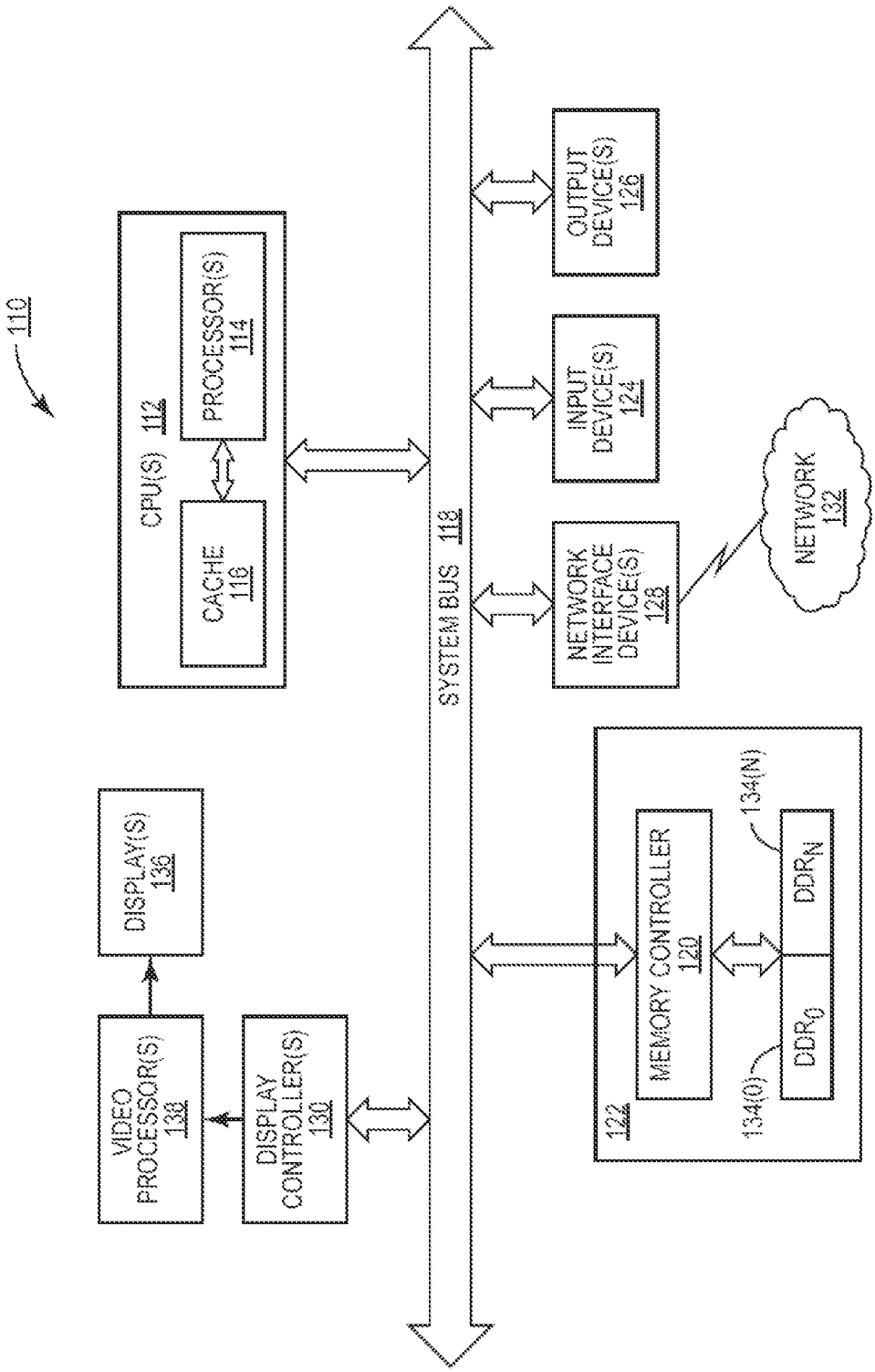
110
CPU(S) 112
PROCESSOR(S) 114
CACHE 116
SYSTEM BUS 118
OUTPUT DEVICE(S) 126
INPUT DEVICE(S) 124
NETWORK INTERFACE DEVICE(S) 128
NETWORK 132
DISPLAY(S) 136
VIDEO PROCESSOR(S) 138
DISPLAY CONTROLLER(S) 130
122
MEMORY CONTROLLER 120
134(N)
DDR$_N$
DDR$_0$
134(0)

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/015279

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/367 H01L23/373 H01L27/02 H01L27/06
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/313227 A1 (OR-BACH ZVI [US] ET AL) 13 December 2012 (2012-12-13) paragraph [0072]; figure 8 paragraph [0128] - paragraph [0135]; figures 33A-33F -----	1-20
X	US 2012/129301 A1 (OR-BACH ZVI [US] ET AL) 24 May 2012 (2012-05-24) paragraph [1027]; figure 112 paragraph [1006]; figure 167 -----	1,3-5, 7-9, 11-19
A	WO 2011/112300 A1 (IBM [US]; GUO DECHAO [US]; HEN SHU-JEN [US]; LIN CHUNG-HSUN [US]; SU N) 15 September 2011 (2011-09-15) paragraph [0016] - paragraph [0017]; figures 1(a)-1(c) paragraph [0020]; figure 1(g) -----	1,4, 16-18

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 April 2014	22/04/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Le Gallo, Thomas

1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/015279

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-20

   Monolithic three-dimensional integrated circuit including a graphene layer and related fabrication method

1.1. claim: 2

   Electromagnetic shielding in the monolithic 3DIC

1.2. claims: 3, 4, 6-10, 18, 20

   Heat removal from the monolithic 3DIC and related methods

1.3. claims: 5, 19

   Electrical connections between the components within the 3DIC and related methods

1.4. claims: 11-13

   Mechanical connection between the first and the second semiconductor integrated circuit tier within the 3DIC

1.5. claim: 14

   Integration of a monolithic 3DIC into a semiconductor die

1.6. claim: 15

   Devices into which a monolithic 3DIC can be implemented

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/015279

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012313227 A1	13-12-2012	NONE	
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