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(54) Title: MULTI-CHIP LED DEVICES

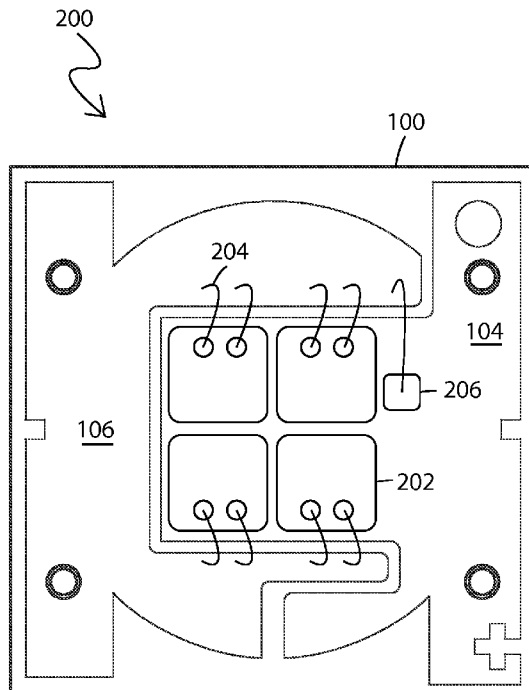


FIG. 2

(57) **Abstract:** Multi-chip LED devices (200, 300) are described. Embodiments of the present invention provide multi-chip LED devices (200, 300) with relatively high efficiency and good color rendering. The LED device (200, 300) includes a plurality of interconnected LED chips (202, 302) and an optical element such as a lens. The optical element may be molded from silicone. The LED chips (202, 302) may be connected in parallel. In some embodiments, the LED device (200, 300) includes a submount (100), which may be made of a ceramic material such as alumina or aluminum nitride. Wire bonds (204, 304, 305) can be connected to the LED chips (202, 302) so that all the wire bonds tend the outside of a group of LED chips. Various sizes and types of LED chips may be used, including vertical LED chips and sideview LED chips.

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MULTI-CHIP LED DEVICES

DESCRIPTION

Background Art

Light emitting diode (LED) lighting systems are becoming more prevalent as
5 replacements for existing lighting systems. LEDs are an example of solid state lighting
(SSL) and have advantages over traditional lighting solutions such as incandescent and
fluorescent lighting because they use less energy, are more durable, operate longer, can
be combined in multi-color arrays that can be controlled to deliver virtually any color
light, and contain no lead or mercury. In many applications, one or more LED chips (or
10 dies) are mounted within an LED package or on an LED module, and such a device may
make up part of a lighting unit, lamp, "light bulb" or more simply a "bulb," which
includes one or more power supplies to power the LEDs. An LED bulb may be made
with a form factor that allows it to replace a standard threaded incandescent bulb, or any
of various types of fluorescent lamps.

15 Color reproduction can be an important characteristic of any type of artificial
lighting, including LED lighting. Color reproduction is typically measured using the
color rendering index (CRI). The CRI is a relative measurement of how the color
rendition of an illumination system compares to that of a theoretical blackbody radiator.
In practical terms, the CRI is a relative measure of the shift in surface color of an object
20 when lit by a particular lamp. The CRI equals 100 if the color coordinates of a set of test
surfaces being illuminated by the lamp are the same as the coordinates of the same test
surfaces being irradiated by the theoretical blackbody radiator. Daylight has the highest
CRI (100), with incandescent bulbs being relatively close (about 95), and fluorescent
lighting being less accurate (70-85). With multi-chip LED devices, the color of the light

from the device will be affected by the color of light emitted by each chip in the device. Chips must be mixed appropriately to maintain the desired color parameters for a device, including the CRI.

5

Disclosure of Invention

Embodiments of the present invention provide multi-chip LED devices with relatively high efficiency and good color rendering for use in lighting systems. In some embodiments, an LED device includes a plurality of interconnected LED chips and an optical element disposed to affect light from the LED chips. In some embodiments, the optical element is less than 5 mm in diameter while maintaining a clearance between any of the LED chips and an edge of the optical element such that the clearance is approximately 0.2 to 0.8 the maximum width of the plurality of LED chips. In some embodiments, the lens is less than 4 mm in diameter. In some embodiments, the clearance is approximately 0.3 to 0.65 the maximum width of the plurality of LED chips. In some embodiments, at least some of the LED chips are connected in parallel.

In some embodiments, the optical element, which may be a lens, is about 3.1 mm in diameter. In some embodiments, the optical element is a molded silicone lens and a submount for the device is a ceramic material such as alumina or aluminum nitride. In some embodiments the plurality of LED chips is selected to maximize the CRI of the LED device. In some embodiments, the LED device, when the LED chips are energized, the device emits light with an efficiency of at least 80 lm/W and the CRI is at least 80. In some embodiments, the LED device emits light with an efficiency of at least about 89 lm/W and the CRI is at least 82.

In some embodiments, a plurality of wire bonds are connected to the LED chips, wherein each wire bond is connected between an LED chip and the submount and the plurality of wire bonds are arranged so that all the wire bonds tend to the outside of the plurality of LED chips. In some embodiments, at least some of the plurality of LED chips are vertical LED chips. In some embodiments, at least some of the plurality of LED chips are sideview LED chips.

Brief Description of the Drawings

FIG. 1 is a top-down view of an LED submount according to example
10 embodiments of the present invention.

FIG. 2 is a top-down view of a multi-chip LED device according to an embodiment of the invention. In this case, each LED is connected via the bottom mounting surface of the chip and a wire bond on top of the chip. The device of FIG. 2 makes use of the submount of FIG. 1 and the lens and its distortion are omitted for
15 clarity.

FIG. 3 is a top-down view of a multi-chip LED device according to another embodiment of the invention. In this case, two wire bonds on top of each LED chip are used to connect the chip. The device of FIG. 3 again makes use of the submount of FIG. 1 and the lens and its distortion are omitted for clarity.

20 FIG. 4 is an electrical schematic diagram of the LED devices of FIGs. 2 and 3.

FIG. 5 is a top-down view of an LED submount according to other example embodiments of the present invention.

FIGs. 6-9 are top-down views of various high density, multi-chip LED devices according to example embodiments of the invention. The embodiments shown in FIGs.

6-9 all make use of the submount of FIG. 5 and the lens and its distortion are omitted for clarity.

FIG. 10 is a top-down view of an LED submount according to further example embodiments of the present invention.

5 FIGS. 11 and 12 are top-down views of various high density, multi-chip LED devices according to example embodiments of the invention. The embodiments shown in FIGS. 11 and 12 make use of the submount of FIG. 10 and the lens and its distortion are omitted for clarity.

10 FIG. 13 is a generalized electrical schematic diagram of the LED devices of FIGS. 5-8.

FIG. 14 is a perspective view of a complete high-density multi-chip LED device according to an example embodiment of the invention.

FIG. 15 is a top-down, schematic illustration of an embodiment of the invention indicating how appropriate lens size is determined.

15

Best Mode(s) for Carrying Out the Invention

Embodiments of the present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

20

It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be
5 termed a first element, without departing from the scope of the present invention. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

It will be understood that when an element such as a layer, region or substrate is referred to as being “on” or extending “onto” another element, it can be directly on or
10 extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” or extending “directly onto” another element, there are no intervening elements present. It will also be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or
15 intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present.

Relative terms such as “below” or “above” or “upper” or “lower” or “horizontal” or “vertical” may be used herein to describe a relationship of one element, layer or region
20 to another element, layer or region as illustrated in the figures. It will be understood that these terms are intended to encompass different orientations of the device in addition to the orientation depicted in the figures.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein,

the singular forms “a”, “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises” “comprising,” “includes” and/or “including” when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but
5 do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms used herein
10 should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

Unless otherwise expressly stated, comparative, quantitative terms such as “less” and “greater”, are intended to encompass the concept of equality. As an example, “less”
15 can mean not only “less” in the strictest mathematical sense, but also, “less than or equal to.”

FIG. 1 is a top-down view of a submount 100 for an LED device according to example embodiments of the invention. Submount 100 of FIG. 1 includes a rigid base 102 that, as an example, can be made of a ceramic material such as alumina or aluminum
20 nitride. Submount 100 also includes a patterned metal layer shaped to provide connectivity to LED chips fixed to the submount. Metal layer portion 104 is for connection to the anodes of the LED chips fixed to the submount, and metal layer portion 106 is for connection to the cathodes of said LED chips. The metal layer can be initially deposited on the ceramic base and then etched to form the desired pattern, can be

formed and fixed to the base with adhesive, or produced in any other suitable fashion. The metal layer can include various holes and notches for alignment during manufacturing, visible identification and the like, such as connection points 108 for connecting wires from the positive side of the power source to the LED device and
5 connection points 109 for connecting wires from the negative side of the power source to the LED device. Connection points may be formed of additional metal or solder deposited on the metal layer.

FIG. 2 is a top-down view of an LED device 200 according to example embodiments of the invention. LED device 200 makes use of submount 100 as
10 described in FIG. 1. LED device 200 includes a plurality of interconnected LED chips 202 fastened to metal layer portion 104 of the submount. In this particular example, four LED chips are used. The anodes of the LED chips are on the bottom of the chips in this view and are in contact with metal layer portion 104, which is in turn connected to the positive terminal of a power source supplying current to the LED chips. The cathodes of
15 the LED chips are connected by wire bonds 204 to metal layer portion 106, which is in turn connected to the negative terminal of the power source. Thus, in this example embodiment, the four LED chips are connected in parallel.

Staying with FIG. 2, LED device 200 includes an electrostatic discharge (ESD) protection chip 206, also fastened to metal layer portion 104. ESD chip 206 is connected
20 with a wire bond to metal layer portion 106. It should also be noted that the wire bonds 204 connected between an LED chips and the submount are arranged so that all the wire bonds are disposed on the outside of the group of four LED chips used in LED device 200. This arrangement allows the plurality of LED chips to be placed close together and be relatively small but still have relatively high efficiency and output. Additionally, four

chips can be combined in various color combinations to achieve a desired CRI, color temperature, or other color-related characteristic.

LED chips 202 and ESD chip 206 of FIG. 2 can be fastened to the submount with conductive adhesive, solder, a welding process, or in any of various other ways. The device is completed with an optical element, for example a lens, placed on top of the device and fastened in place to affect light from the LED chips. Both the lens and the distortion it would introduce when the device is viewed are omitted from FIG. 2 for clarity of illustration, but an example lens is illustrated later in connection with another embodiment of the invention. Both the term “optical element” and the term “lens” as used in this disclosure are intended in their broadest sense. Such an element may affect light by bending and/or concentrating light rays, by color mixing, or by a combination of these effects. A phosphor could also be used to provide wavelength conversion. A lens for use with an LED device of an embodiment of the invention may be made of glass or plastic, may be molded in place or elsewhere, or otherwise formed or attached to the device as desired. For example, the lens may be molded in place from silicone. In example embodiments, a clearance is maintained between the edge of any of the plurality of interconnected LED chips and the edge of the lens. In some embodiments, the clearance is approximately 0.2 to 0.8 the maximum width across the LED chips. The clearance can also be from 0.3 to 0.65 the width of the LED chips. In a more specific example with four LED chips, if the maximum width of the LED chips is 1.4 mm, the lens clearance is about 0.9 mm, or about 0.643 the maximum width of the LED chips.

LED chips 202 of FIG. 2 may be selected from various light color bins to provide a combined light output with a high color rendering index (CRI). The desired color mixing may be achieved, for example, using blue, green, amber, red and/or red-orange

LED chips. One or more of the chips may be in a package with a phosphor or may otherwise have a locally applied phosphor. An example of selecting chips from various color bins to produce desired color characteristics is described in U.S. Patent Application 2010/0140633, published January 10, 2010, which is incorporated herein by reference.

5 A detailed example of using groups of LEDs emitting light of different wavelengths to produce substantially white light can be found in issued U.S. Patent 7,213,940, which is incorporated herein by reference.

In some example embodiments, the lens for an LED device such as LED device 200 of FIG. 2 may be less than 5 mm in diameter or less than 4 mm in diameter. In some
10 embodiments the lens may be about 3.1 mm in diameter and may include LED chips of about 700 microns in size, meaning the chips are about 700 microns wide on a side. The chips may be about or less than 1000 microns in size, about or less than 700 microns in size, about or less than 500 microns in size, or about or less than 300 microns in size. An LED device like that shown in FIG. 2 may have an efficiency of at least 80 lumens/Watt
15 (lm/W) and a CRI of at least 80. The LED device may have an efficiency of at least 89 lm/W and a CRI of at least 82. The design of the LED device can be adapted so that various types of LED chips could be used, such as direct-bond chips, flip-chips, and chips with substrates made of sapphire, silicon carbide, silicon or other materials.

FIG. 3 is a top-down view of an LED device 300 according to some example
20 embodiments of the invention. LED device 300 again makes use of submount 100 as described in FIG. 1. LED device 300 includes a plurality of interconnected LED chips 302 fastened to metal layer portion 104 of the submount. In this example, the LED chips are so-called "sideview" LEDs, for each of which the connection points for both the anode and cathode are on top. The anodes of the LED chips are connected to metal layer

portion 104 with wire bonds 304, and the cathodes of the LED chips are connected by wire bonds 305 to metal layer portion 106. In this example embodiment, the four LED chips are again connected in parallel.

Staying with FIG. 3, LED device 300 includes an electrostatic discharge (ESD) protection chip 306, fastened to metal layer portion 104. ESD chip 306 is also connected with a wire bond to metal layer portion 106. It should also be noted that the wire bonds connected between the plurality of LED chips and the submount are arranged so that all the wire bonds tend to the outside of the group of four LED chips used in LED device 300 as much as possible. This arrangement again allows the LED chips to be placed close together. As before, the LED chips can be combined in various color combinations to achieve a desired CRI, color temperature, or other color-related characteristic.

LED chips 302 of FIG. 3 can be fastened to the submount with adhesive, or in any of various other ways. Since these sideview chips have both connections on top, the adhesive need not be conductive. As before, the device is completed with an optical element, for example a lens, placed on top of the device and fastened in place to affect light from the LED chips. Both the lens and the distortion it would introduce when the device is viewed are omitted from FIG. 3 for clarity of illustration, but an example lens is illustrated later in connection with another embodiment of the invention. Both the term “optical element” and the term “lens” as used in this disclosure are intended in their broadest sense. Such an element may affect light by bending and/or concentrating light rays, by color mixing, or by a combination of these effects. A phosphor could also be used to provide wavelength conversion. A lens for use with an LED device of an embodiment of the invention may be made of glass or plastic, may be molded in place or elsewhere, or otherwise formed or attached to the device as desired. For example, the

lens may be molded in place from silicone. In example embodiments, a clearance is again maintained between the edge of any of the plurality of interconnected LED chips and the edge of the lens. In some embodiments, the clearance is approximately 0.2 to 0.8 the maximum width across the LED chips. The clearance can also be from 0.3 to 0.65 the width of the LED chips. LED chips 302 of FIG. 3 may again be selected from various light color bins to provide a combined light output with a high color rendering index (CRI). The desired color mixing may be achieved, for example, using blue, green, amber, red and/or red-orange LED chips. One or more of the chips may be in a package with a phosphor or may otherwise have a locally applied phosphor.

10 In some example embodiments, the lens for an LED device such as LED device 300 of FIG. 3 may be less than 5 mm in diameter or less than 4 mm in diameter. In some embodiments the lens may be about 3.1 mm in diameter. LED chips of various sizes and shapes may be used. A typical sideview chips has a rectangular top, angled sides, and a smaller, rectangular bottom. The sides of the rectangle can vary between about 100 and 15 500 microns, and the chip may have a thickness of 100 to 150 microns.

FIG. 4 is an electronic schematic diagram of the circuit of the LED devices from FIGS. 2 and 3. Circuit 400 includes four LEDs 402 connected in parallel to form a single group of LEDs. Current to illuminate the LEDs is supplied by power source 405. ESD protection device 406 is connected in parallel with the LEDs.

20 FIG. 5 is a top-down view of a submount 500, which can be used for various LED devices according to example embodiments of the invention. Submount 500 of FIG. 5 includes a rigid base 502 that, as an example, can be made of plastic, or as a further example can be made of a ceramic material such as alumina or aluminum nitride. Submount 500 includes a patterned metal layer shaped to provide connectivity to LED

chips fixed to the submount. This patterned metal layer includes semicircular areas of metal to which LED chips can be bonded. Metal layer portion 504 is for connection to the anodes of one group of LED chips fixed to the submount, and metal layer portion 506 is for connection to the anodes of another group of LED chips. Metal layer portion 508 is for connection to some of the cathodes of LED chips in the first group of LED chips, and metal layer portion 510 is for connection to some of the cathodes in the other group of LED chips. Metal layer portion 510 is connected to protruding rail 512 and metal layer portions 506 and 508 are connected by interconnection rail 514. Rails 512 and 514 run near each other and form a centrally located connection bus, or more simply, a central bus to which wire bonds from some of the cathodes of the LED chips are connected. A central bus or central connection bus within the meaning of this disclosure is a part of the metal layer of a submount where portions to be connected to different LEDs or different terminals of the LEDs come close together to allow connections that enable relatively high chip-density. Such a central bus typically has one or more connection rails providing at least some of the connection portions. In this example, wire bonds from some of the cathodes of LED chips from the first group of LED chips are connected to rail 514 and wire bonds from some of the cathodes of LED chips in the additional group of LED chips are connected to rail 512.

The metal layer can be initially deposited on the base and then etched to form the desired pattern, can be formed and fixed to the base with adhesive, molded into a base, or produced in any other suitable fashion. The metal layer can include various holes and notches for alignment during manufacturing, visible identifications and the like, as well as connection points, such as connection points 520 for connecting wires from the positive side of the power source to the LED device and connection points 522 for

connecting wires from the negative side of the power source to the LED device.

Connection points may be formed of additional metal or solder deposited on the metal layer.

FIG. 6 is a top-down view of an LED device 600 according to some example
5 embodiments of the invention. LED device 600 makes use of submount 500 as
described in FIG. 5. LED device 600 includes twelve LED chips arranged in two
groups. Six LED chips 610 are fastened to metal layer portion 504 of the submount and
are connected in parallel. The anodes are on the bottom of the LED chips 610 and are in
contact with metal layer portion 504, which is in turn connected to the positive terminal
10 of a power source supplying current to the device via connection points 520. Six LED
chips 612 are fastened to metal layer portion 506 of the submount and are also connected
in parallel. The anodes of the LED chips 612 are in contact with metal layer portion 506.

Still referring to FIG. 6, the cathodes of all of the LED chips are connected by
wire bonds to metal layer portions of submount 500 as follows. Wire bonds from the
15 cathodes of LED chips 610 are connected to metal layer portions of the submount. More
specifically, wire bonds 614 are connected to interconnection rail 514 of the central bus
of submount 500, and wire bonds 616 are connected to metal layer portion 508 of the
submount. Wire bonds from the cathodes of LED chips 612 are also connected to metal
layer portions of the submount. More specifically, wire bonds 618 are connected to
20 extension rail 512 of the central bus of submount 500, and wire bonds 620 are connected
to metal layer portion 510 of the submount 500.

Staying with FIG. 6, LED device 600 includes an electrostatic discharge (ESD)
protection chip 630, fastened to metal layer portion 510 and connected with a wire bond
to metal layer portion 504. Metal layer portion 504 is connected to the positive terminal

of a power source supplying current to the LED device. Metal layer portion 510 is connected to the negative terminal of a power source supplying current to the LED device. The wire bonds connected between the LED chips within each group of six LED chips in LED device 600 and the submount are arranged so that all the wire bonds in a group are disposed on the outside of the group of six LED chips, allowing the LED chips in a group to be placed close together and this density of the LED chips in a group allows LED device 600 to be relatively small but still have a relatively high efficiency and output. Also, the patterning of the metal layer portions of the submount together with the arrangement of wire bonds interconnects the LED chips within a group in parallel while the groups themselves are connected in series.

The LED chips and ESD chip of LED device 600 of FIG. 6 can be fastened to the submount with conductive adhesive, solder, a welding process, or in any of various other ways. As before, the device is completed with an optical element placed on top of the device to affect light from the LED chips. Both the optical element and the distortion it would introduce when the device is viewed are omitted in FIG. 6 for clarity of illustration, but an example lens is discussed later with respect to FIG. 14. Again, an optical element, for example, a lens, may affect light by bending and/or concentrating light rays, by color mixing, or by a combination of these effects. A phosphor could also be used to provide wavelength conversion. A lens or other optical element for use with an LED device of embodiments of the invention may be made of glass or plastic, may be molded in place or elsewhere, or otherwise formed or attached to the device as desired. In example embodiments, a clearance is again maintained between the edge of any of the plurality of interconnected LED chips and the edge of the lens. In some embodiments, the clearance is approximately 0.2 to 0.8 the maximum width across the LED chips. The

clearance can also be from 0.3 to 0.65 the width of the LED chips. In a more specific example, if the maximum width of the LED chips is 5.6 mm, the lens clearance is about 1.7 mm, or about 0.303 the maximum width of the LED chips.

As before, the LED chips in the device of FIG. 6 may be selected from various
5 light color bins to provide a combined light output with a high CRI. In some example
embodiments, the lens for an LED device such as LED device 600 of FIG. 6 may be less
than 12 mm in diameter. In some embodiments, the lens may be less than 10 mm in
diameter, less than 9 mm in diameter, or less than 8 mm in diameter. In some
embodiments the lens may be about 9.1 mm in diameter and may use identical LED
10 chips of about 1000 microns in size, meaning the chips are about 1000 microns wide on a
side. However, chips of various sizes may be used. The chips may be about or less than
2000 microns in size, about or less than 1000 microns in size, about or less than 700
microns in size or about or less than 500 microns in size. Also, mixed chip sizes may be
used in a single device. A specific example embodiment with mixed chip sizes is
15 described later in this disclosure with respect to FIG. 9. An LED device like that shown
in FIG. 6 may have an efficiency of at least, 80, 85, or 90 lumens/Watt (lm/W) and a CRI
of at least 80. The LED device may have an efficiency of about 95 lm/W and a CRI of at
least 82. The efficiency of such an LED device with a warm white color, often desired
for incandescent replacement lighting, may be as much as about 100 lm/W. However, if
20 the device is binned for a cool white color, an efficiency of as much as about 150 lm/W
can be achieved. The design of the LED device of FIG. 6 can be adapted so that various
types of LED chips could be used, such as direct-bond chips, flip-chips, and chips with
substrates made of sapphire, silicon carbide, silicon or other materials.

FIGs. 7 and 8 are top-down views of LED devices that are similar to the device shown in FIG. 6, but which include more LED chips in each group. FIG. 7 is a top-down view of an LED device 700 according to some example embodiments of the invention. LED device 700 makes use of submount 500 as previously described. LED device 700 includes fourteen LED chips arranged in two groups. Seven LED chips 710 are fastened to metal layer portion 504 of the submount and are connected in parallel. Seven LED chips 712 are fastened to metal layer portion 506 of the submount and are also connected in parallel. As before, the anodes of the LED chips are in contact with portions of the metal layer of submount 500.

Still referring to FIG. 7, the cathodes of all of the LED chips are connected by wire bonds to metal layer portions of submount. Wire bonds 714 are connected to interconnection rail 514 of the central bus of submount 500, and wire bonds 716 are connected to metal layer portion 408 of the submount. Wire bonds 718 are connected to extension rail 512 of the central bus of submount 500, and wire bonds 720 are connected to metal layer portion 510 of the submount 500. LED device 700 includes an electrostatic discharge (ESD) protection chip 730, fastened to metal layer portion 510 with a wire bond connected to metal layer portion 504. As before, metal layer portion 504 is connected to the positive terminal of a power source and metal layer portion 510 is connected to the negative terminal. The wire bonds connected between the LED chips within each group of seven LED chips in LED device 700 and the submount are again arranged so that all the wire bonds in a group are disposed on the outside of the group of seven LED chips, allowing the LED chips in a group to be placed close together. The LED chips within a group are connected in parallel while the groups of chips are connected in series.

The LED chips and ESD chip of LED device 700 of FIG. 7 can be fastened to the submount with conductive adhesive, solder, a welding process, or in any of various other ways. As before, the device is completed with an optical element placed on top of the device to affect light from the LED chips. Both the optical element and the distortion it would introduce when the device is viewed are omitted in FIG. 7 for clarity of illustration. Again, an optical element, for example, a lens, may affect light by bending and/or concentrating light rays, by color mixing, or by a combination of these effects. A phosphor could also be used to provide wavelength conversion. A lens or other optical element for use with an LED device of any embodiment of the invention may be made of glass or plastic, may be molded in place or elsewhere, or otherwise formed or attached to the device as desired. In example embodiments, clearance is maintained between the edge of any of the plurality of interconnected LED chips and the edge of the lens as previously described.

As before, the LED chips in the device of FIG. 7 may be selected from various light color bins to provide a combined light output with a high CRI. In some example embodiments, the lens for an LED device such as LED device 700 of FIG. 7 may be less than 12 mm in diameter. In some embodiments, the lens may be less than 10 mm in diameter, less than 9 mm in diameter, or less than 8 mm in diameter. In some embodiments the lens may be about 9.1 mm in diameter and may use identical LED chips of about 1000 microns in size, meaning the chips are about 1000 microns wide on a side. However, of various sizes, materials, and types may be used, as described with respect to FIG. 6. An LED device like that shown in FIG. 7 may have an efficiency of at least, 80, 85, or 90 lumens/Watt (lm/W) and a CRI of at least 80. The LED device may have an efficiency of about 95 lm/W and a CRI of at least 82. The efficiency of such an

LED device with a warm white color, often desired for incandescent replacement lighting, may be as much as about 100 lm/W. However, if the device is binned for a cool white color, an efficiency of as much as about 150 lm/W can be achieved.

FIG. 8 is a top-down view of an LED device 800 according to some example
5 embodiments of the invention. LED device 800 makes use of submount 500 as
previously described, and includes sixteen LED chips arranged in two groups. Eight
LED chips 810 are fastened to metal layer portion 504 of the submount. Eight LED
chips 812 are fastened to metal layer portion 506 of the submount. As before, the anodes
of the LED chips are in contact with portions of the metal layer of submount 500. The
10 cathodes of all of the LED chips in device 800 are connected by wire bonds to metal
layer portions of the submount. Wire bonds 814 are connected to interconnection rail
514 of the central bus of submount 500, and wire bonds 816 are connected to metal layer
portion 408 of the submount. Wire bonds 818 are connected to extension rail 512 of the
central bus of submount 500, and wire bonds 820 are connected to metal layer portion
15 510 of the submount 500.

Still referring to FIG. 8, device 800 includes an electrostatic discharge (ESD)
protection chip 830, fastened to metal layer portion 510 and connected by a wire bond to
metal layer portion 504. As before, metal layer portion 504 is connected to the positive
terminal of a power source and metal layer portion 510 is connected to the negative
20 terminal. The wire bonds connected between the LED chips within each group of eight
LED chips in LED device 800 and the submount are again arranged so that all the wire
bonds in a group are disposed on the outside of the group of eight LED chips, allowing
the LED chips in a group to be placed close together. The LED chips within a group are
connected in parallel while the groups are connected in series.

The LED chips and ESD chip of LED device 800 of FIG. 8 can be fastened to the submount with conductive adhesive, solder, a welding process, or in any of various other ways. As before, the device is completed with an optical element placed on top of the device to affect light from the LED chips. Both the optical element and the distortion it would introduce when the device is viewed are omitted in FIG. 8 for clarity of illustration. Again, an optical element, for example, a lens, may affect light by bending and/or concentrating light rays, by color mixing, or by a combination of these effects. A phosphor could also be used to provide wavelength conversion. A lens or other optical element for use with an LED device of any embodiment of the invention may be made of glass or plastic, may be molded in place or elsewhere, or otherwise formed or attached to the device as desired. Clearance is maintained between the edge of any of the plurality of interconnected LED chips and the edge of the lens as previously described.

As before, the LED chips in the device of FIG. 8 may be selected from various light color bins to provide a combined light output with a high CRI. In some example embodiments, the lens for an LED device such as LED device 800 of FIG. 8 may be less than 12 mm in diameter. In some embodiments, the lens may be less than 10 mm in diameter, less than 9 mm in diameter, or less than 8 mm in diameter. In some embodiments the lens may be about 9.1 mm in diameter and may use identical LED chips of about 1000 microns in size, meaning the chips are about 1000 microns wide on a side. However, of various sizes, materials, and types may be used, as described with respect to FIG. 6. An LED device like that shown in FIG. 8 may have an efficiency of at least, 80, 85, or 90 lumens/Watt (lm/W) and a CRI of at least 80. The LED device may have an efficiency of about 95 lm/W and a CRI of at least 82. The efficiency of such an LED device with a warm white color, often desired for incandescent replacement

lighting, may be as much as about 100 lm/W. However, if the device is binned for a cool white color, an efficiency of as much as about 150 lm/W can be achieved.

As previously mentioned, an embodiment of the invention does not need to use LED chips of equal size. FIG. 9 is a top-down view of an LED device 900 in which
5 different sizes of LED chips are used. LED device 900 makes use of submount 500 as described in FIG. 4. LED device 900 includes sixteen LED chips, including chips of two different sizes, arranged in two groups. Six LED chips 910 of one size and two LED chips 911 of a smaller size are fastened to metal layer portion 504 of the submount and are connected in parallel. The anodes of the LED chips 910 and 911 are on the bottoms
10 of the chips and are in contact with metal layer portion 504, which is in turn connected to the positive terminal of a power source supplying current to the device via connection points 520. Six LED chips 912 of one size and two LED chips 913 of a smaller size are fastened to metal layer portion 506 of the submount and are also connected in parallel. The anodes of the LED chips 912 and 913 are on the bottoms of the chips and are in
15 contact with metal layer portion 506.

Still referring to FIG. 9, the cathodes of all of the LED chips are connected by wire bonds to metal layer portions of submount 500 as follows. Wire bonds 914 are connected from the cathodes of some of LED chips 910 to interconnection rail 514 of the central bus of submount 500, and wire bonds 916 are connected from the rest of LED
20 chips 910 to metal layer portion 508 of the submount. Wire bonds 917 are connected from the cathodes of smaller LED chips 911 to metal layer portion 408 of the submount. Wire bonds 918 from the cathodes of some of LED chips 912 are connected to extension rail 512 of the central bus of submount 500, and wire bonds 920 are connected from the cathodes of the remainder of LED chips 912 to metal layer portion 510 of the submount

500. Wire bonds 921 are connected from the cathodes of smaller LED chips 913 to metal layer portion 508 of the submount.

Staying with FIG. 9, LED device 900 includes an electrostatic discharge (ESD) protection chip 930 connected as previously described. Metal layer portion 504 is
5 connected to the positive terminal of a power source supplying current to the LED device. Metal layer portion 510 is connected to the negative terminal of a power source supplying current to the LED device. The wire bonds connected between the LED chips within each group of eight, mixed size LED chips in LED device 900 and the submount are arranged so that all the wire bonds in a group are disposed on the outside of the group
10 of LED chips, allowing the LED chips in a group to be placed close together. Also, the patterning of the metal layer portions of the submount together with the arrangement of wire bonds interconnects the LED chips within a group in parallel while the groups of chips are connected in series.

As with the other embodiments, the LED chips and ESD chip of LED device 900
15 of FIG. 9 can be fastened to the submount with conductive adhesive, solder, a welding process, or in any of various other ways. As before, the device is completed with an optical element placed on top of the device to affect light from the LED chips. Both the optical element and the distortion it would introduce when the device is viewed are omitted in FIG. 9 for clarity of illustration. Again, an optical element, for example, a
20 lens, may affect light by bending and/or concentrating light rays, by color mixing, or by a combination of these effects. A phosphor could also be used to provide wavelength conversion. A lens or other optical element for use with an LED device of any embodiment of the invention may be made of glass or plastic, may be molded in place or elsewhere, or otherwise formed or attached to the device as desired. In example

embodiments, an appropriate clearance is again maintained between the edge of any of the plurality of interconnected LED chips and the edge of the lens.

As before, the LED chips in the device of FIG. 9 may be selected from various light color bins to provide a combined light output with a high CRI. In some example
5 embodiments, the lens for an LED device such as LED device 900 of FIG. 9 may be less than 12 mm in diameter. In some embodiments, the lens may be less than 10 mm in diameter, less than 9 mm in diameter, or less than 8 mm in diameter. In some
embodiments the lens may be about 9.1 mm in diameter. Various numbers of chips of various sizes may be combined in different ways to form a device according to
10 embodiments of the invention. Chips of two different size, three different sizes or four different sizes may be used. Larger LED chips of about 1000 microns in size, meaning the chips are about 1000 microns wide on a side, can be used. However, of various sizes may be used. The larger chips may be about or less than 2000 microns in size, about or less than 1000 microns in size, about or less than 700 microns in size or about or less
15 than 500 microns in size. The smaller chips may be 1000 microns, 700 microns, 500 microns in size, or smaller.

The ability to use multiple LED chips of different sizes allows a designer to “tune” the multi-chip LED device for the desired combination of voltage, current density and light output. Smaller chips can also be used to fill in spaces between or around
20 larger chips to achieve greater chip density. LED chips of different sizes have different current densities for the same drive current, as larger chips have a lower forward voltage for the same drive current than smaller chips due to current density. LED chips of different sizes can be mixed together in either embodiments of the invention using one group of chips, such as the embodiment described with respect to FIG. 2, or in

embodiments with two groups of chips where parallel groups are connected in series, such as those described with respect to FIGs. 6-9. An LED device like that shown in FIG. 9 may have an efficiency of at least, 80, 85, or 90 lumens/Watt (lm/W) and a CRI of at least 80. The LED device may have an efficiency of about 95 lm/W and a CRI of at least 82. The efficiency of such an LED device with a warm white color, often desired for incandescent replacement lighting, may be as much as about 100 lm/W. However, if the device is binned for a cool white color, an efficiency of as much as about 150 lm/W can be achieved. The design of the LED device of FIG. 9 can again be adapted so that various types of LED chips could be used, such as direct-bond chips, flip-chips, and chips with substrates made of sapphire, silicon carbide, silicon or other materials.

FIG. 10 is a top-down view of another submount 1000, which can be used for various LED devices according to example embodiments of the invention. Submount 1000 of FIG. 10 again includes a rigid base 1002 that, as an example, can be made of plastic, or as a further example can be made of a ceramic material such as alumina or aluminum nitride. Submount 1000 includes a patterned metal layer shaped to provide connectivity to LED chips fixed to the submount. This patterned metal layer again includes semicircular areas of metal to which vertical LED chips can be bonded. Metal layer portion 1004 is for connection to the anodes of one group of LED chips fixed to the submount, and metal layer portion 1006 is for connection to the anodes of another group of LED chips. Metal layer portion 1008 is for connection to some of the cathodes of LED chips in the first group of LED chips, and metal layer portion 1010 is for connection to some of the cathodes in the other group of LED chips. Metal layer portion 1010 is connected to protruding rail 1012 and metal layer portions 1004 and 1006 are both adjacent to this rail, and near each other. Like the submount shown in FIG. 5, rail

1012 and the adjacent portions of the metal layer form a centrally located connection bus, or more simply, a central bus to which wire bonds from some of the cathodes of the LED chips are connected.

The metal layer can be initially deposited on the base and then etched to form the
5 desired pattern, can be formed and fixed to the base with adhesive, molded into a base, or produced in any other suitable fashion. The metal layer can include various holes and notches for alignment during manufacturing, visible identifications and the like, as well as connection points, such as connection points 1020 for connecting wires from the positive side of the power source to the LED device and connection points 1022 for
10 connecting wires from the negative side of the power source to the LED device. Connection points may be formed of additional metal or solder deposited on the metal layer.

FIG. 11 is a top-down view of an LED device 1100 according to some example
embodiments of the invention. LED device 1100 makes use of submount 1000 as
15 described in FIG. 10. LED device 1100 includes twelve LED chips arranged in two groups. Six LED chips 1120 are fastened to metal layer portion 1006 of the submount and are connected in parallel. The anodes are on the bottom of the LED chips 1120 and are in contact with metal layer portion 1006. Six LED chips 1121 are fastened to metal layer portion 1004 of the submount and are also connected in parallel. The anodes of the
20 LED chips 1121 are in contact with metal layer portion 1004.

Still referring to FIG. 11, the cathodes of all of the LED chips are connected by wire bonds to metal layer portions of submount 1000. Wire bonds from the cathodes of LED chips 1120 are connected to metal layer portions of the submount. More specifically, wire bonds 1122 are connected to interconnection rail 1012 of the central

bus of submount 1000, and wire bonds 1123 are connected to metal layer portion 1010 of the submount. Wire bonds from the cathodes of LED chips 1121 are also connected to metal layer portions of the submount. More specifically, wire bonds 1125 are connected to a nearby part of metal layer portion 1006 of submount 1000, and wire bonds 1126 are
5 connected to metal layer portion 1008 of the submount 1000.

Staying with FIG. 11, LED device 1100 includes an electrostatic discharge (ESD) protection chip 1130, fastened to metal layer portion 1010 and connected with a wire bond to metal layer portion 1004. Metal layer portion 1004 is connected to the positive terminal of a power source supplying current to the LED device via connection points
10 1020. Metal layer portion 1010 is connected to the negative terminal of a power source supplying current to the LED device via connection points 1022. The wire bonds connected between the LED chips within each group of six LED chips in LED device 1100 and the submount are arranged so that all the wire bonds in a group are disposed on the outside of the group of six LED chips, allowing the LED chips in a group to be
15 placed close together and this density of the LED chips in a group allows LED device 1100 to be relatively small but still have a relatively high efficiency and output. Also, the patterning of the metal layer portions of the submount together with the arrangement of wire bonds interconnects the LED chips within a group in parallel while the groups themselves are connected in series. Other series and parallel combinations can be
20 implemented.

The LED chips and ESD chip of LED device 1100 of FIG. 11 can be fastened to the submount with conductive adhesive, solder, a welding process, or in any of various other ways. As before, the device is completed with an optical element placed on top of the device to affect light from the LED chips. Both the optical element and the distortion

it would introduce when the device is viewed are omitted in FIG. 11 for clarity of illustration, but an example lens is discussed later with respect to FIG. 14. Again, an optical element, for example, a lens, may affect light by bending and/or concentrating light rays, by color mixing, or by a combination of these effects. A phosphor could also be used to provide wavelength conversion. In example embodiments, a clearance is again maintained between the edge of any of the plurality of interconnected LED chips and the edge of the lens. In some embodiments, the clearance is approximately 0.2 to 0.8 the maximum width across the LED chips. The clearance can also be from 0.3 to 0.65 the width of the LED chips. In a more specific example, if the maximum width of the LED chips is 5.6 mm, the lens clearance is about 1.7 mm, or about 0.303 the maximum width of the LED chips.

As before, the LED chips in the device of FIG. 11 may be selected from various light color bins to provide a combined light output with a high CRI. In some example embodiments, the lens for an LED device such as LED device 1100 of FIG. 11 may be less than 12 mm in diameter. In some embodiments, the lens may be less than 10 mm in diameter, less than 9 mm in diameter, or less than 8 mm in diameter. In some embodiments the lens may be about 9.1 mm in diameter and may use identical LED chips of about 1000 microns in size, meaning the chips are about 1000 microns wide on a side. However, chips of various sizes may be used. The chips may be about or less than 2000 microns in size, about or less than 1000 microns in size, about or less than 700 microns in size or about or less than 500 microns in size. An LED device like that shown in FIG. 11 may have an efficiency of at least, 80, 85, or 90 lumens/Watt (lm/W) and a CRI of at least 80. The LED device may have an efficiency of about 95 lm/W and a CRI of at least 82. The design of the LED device of FIG. 11 can be adapted so that

various types of LED chips could be used, such as direct-bond chips, flip-chips, and chips with substrates made of sapphire, silicon carbide, silicon or other materials. The efficiency of such an LED device with a warm white color, often desired for incandescent replacement lighting, may be as much as about 100 lm/W. However, if the device is binned for a cool white color, an efficiency of as much as about 150 lm/W can be achieved.

FIG. 12 is a top-down view of an LED device 1200 according to some example embodiments of the invention. LED device 1200 again makes use of submount 1000 as described in FIG. 10. LED device 1200, however, includes two different kinds of LED chips. LED chips 1220 are positioned and connected in the same fashion as the LED chips 1120 in FIG. 11 that were fastened to metal rail 1012. LED chips 1221 are fastened to metal layer portion 1004 of the submount. Device 1200 however, also includes sideview LED chips 1240, each of which has wire bonds connected to the top for both the anode and the cathode. LED chips 1240 are also rectangular in shape instead of square in shape. Wire bonds 1242 connect the anodes and wire bonds 1244 connect the cathodes to the appropriate metal layer portion. Thus, high density LED multi-chip devices according to embodiment of the invention can include different types and shapes of LEDs. Any of various types can be used alone, or different types, sizes and shapes of LEDs can be combined.

Staying with FIG. 12, LED device 1200 includes an electrostatic discharge (ESD) protection chip 1230, fastened to metal layer portion 1010 and connected with a wire bond to metal layer portion 1004. Metal layer portion 1004 is connected to the positive terminal of a power source supplying current to the LED device via connection points 1020. Metal layer portion 1010 is connected to the negative terminal of a power source

supplying current to the LED device via connection points 1022. The wire bonds connected between the LED chips within each group of six mixed-type LED chips in LED device 1200 and the submount are again arranged so that all the wire bonds in a group are disposed on the outside of the group of six LED chips, allowing the LED chips
5 in a group to be placed close together and this density of the LED chips in a group allows LED device 1200 to be relatively small but still have a relatively high efficiency and output. Also, the patterning of the metal layer portions of the submount together with the arrangement of wire bonds interconnects the LED chips within a group in parallel while the groups themselves are connected in series. Other series and/or parallel combinations
10 of LEDs are possible with all of the submounts shown in the various embodiments described herein.

As before, device 1200 of FIG. 12 is completed with an optical element placed on top of the device to affect light from the LED chips. Both the optical element and the distortion it would introduce when the device is viewed are omitted in FIG. 12 for clarity
15 of illustration, but an example lens is discussed later with respect to FIG. 14. In an embodiment with mixed chip sizes and shapes, a clearance is again maintained between the edge of any of the plurality of interconnected LED chips and the edge of the lens. In some embodiments, the clearance is approximately 0.2 to 0.8 the maximum width across the LED chips. The clearance can also be from 0.3 to 0.65 the width of the LED chips.
20 In a more specific example, if the maximum width of the LED chips is 5.6 mm, the lens clearance is about 1.7 mm, or about 0.303 the maximum width of the LED chips.

As before, the LED chips in the device of FIG. 12 may be selected from various light color bins to provide a combined light output with a high CRI. In some example embodiments, the lens for an LED device such as LED device 1200 of FIG. 12 may be

less than 12 mm in diameter. In some embodiments, the lens may be less than 10 mm in diameter, less than 9 mm in diameter, or less than 8 mm in diameter. In some embodiments the lens may be about 9.1 mm in diameter and may use identical LED chips of about 1000 microns in size, meaning the chips are about 1000 microns wide on a side. However, chips of various sizes may be used. The chips may be about or less than 2000 microns in size, about or less than 1000 microns in size, about or less than 700 microns in size or about or less than 500 microns in size. An LED device like that shown in FIG. 12 may have an efficiency of at least, 80, 85, or 90 lumens/Watt (lm/W) and a CRI of at least 80. The LED device may have an efficiency of about 95 lm/W and a CRI of at least 82. Again, The efficiency of such an LED device with a warm white color, often desired for incandescent replacement lighting, may be as much as about 100 lm/W. However, if the device is binned for a cool white color, an efficiency of as much as about 150 lm/W can be achieved.

FIG. 13 is a generalized, electronic schematic diagram of the circuit of the LED devices from FIGs. 6-12. Circuit 1300 includes multiple LEDs 1302 connected in parallel to form a first group of LEDs connected in parallel. Multiple LEDs 1303 are connected in parallel to form a second group of LEDs connected in parallel. The two groups of parallel LEDs are in turn connected in series. Current to illuminate the LEDs is supplied by power source 1305. ESD protection device 1306 is connected in parallel across the entire LED circuit spanning both groups of LEDs.

FIG. 14 is a perspective view of LED device 1100 previously shown and described with respect to FIG. 11. In FIG. 14, the optical element, lens 1150 is visible over the two groups of six LED chips and submount 1000. The distortion introduced by the lens can also be seen. In the view of FIG. 14, device 1100 is positioned so that the

plus sign in the metal layer is in the top left corner. As previously mentioned, a lens for use with an LED device of an embodiment of the invention may be made of glass or plastic, may be molded in place or elsewhere, or otherwise formed or attached to the device as desired. For example, the lens may be molded in place from silicone. FIG. 14 illustrates a lens used with the embodiment of the LED device previously shown in FIG. 11, however, essentially the same type and appearance of lens can be used with any of the embodiments described herein, with appropriate adjustment in the size of the lens for the number of LED chips and size of the substrate used.

FIG. 15 illustrates the how the clearance between the LED chips and the edge of the lens is determined for embodiments of the invention. The view of FIG. 15 is purely schematic. In this example, fourteen identical LED chips are represented by squares 1502. The outer edge of the lens is represented by circle 1504. Circle 1506 circumscribes the LED chips at their widest point. Area 1508 is the clearance area, with the size of the clearance defined by length 1510. As previously described, this size, in example embodiments, can be approximately 0.2 to 0.8 the maximum width across the LED chips. The clearance can also be from 0.3 to 0.65 the width of the LED chips.

Hi density multi-chip devices as described herein, especially as exemplified by the embodiments shown in FIGs. 5-15 can be made with many types of LED chips. Vertical chips have been used extensively in these embodiments, but flip-chip and sideview chips can also be used, and sideview style chips have also been shown in some of these specific embodiments. Chips with low reabsorption, especially for blue light, can assist in improving light output. Square submounts have been shown, but submounts of various shapes and sizes can be used. Submounts can be ceramic as in previous examples, metal, or plastic. A plastic submount may have a metal slug to aid in heat

sinking. Various semiconductor materials can be used for the LEDs, including silicon carbide and sapphire. The layouts provide for high-density and very efficient light output in part by placement of wire bonds needed to interconnect the LED chips. The specific submount metal pattern designs minimize light absorption by the submount, and
5 also help increase light output.

The characteristics described above can enable a high-density device light that described to be used in a solid-state replacement for a bright halogen bulb such as the now popular MR16 halogen multi-reflector bulb. In example embodiments, the device size is about 10 mm on a side. It is possible, by the use of smaller LED chips, or fewer,
10 larger LED chips to still achieve very high efficiency in a small package, for example, a package less than 5 mm on a side or less than 3.5 mm on a side. Four 1000-micron LED chips could be replaced with one 2000-micron LED chip. A device could also be scaled to exactly the maximum size that would fit in an LED bulb of a form factor appropriate for a specific incandescent or halogen bulb, such as the previously mentioned MR16
15 bulb.

Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art appreciate that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown and that the invention has other applications in other environments. This application is intended to
20 cover any adaptations or variations of the present invention. The following claims are in no way intended to limit the scope of the invention to the specific embodiments described herein.

CLAIMS

1. An LED device comprising:
 - a plurality of interconnected LED chips; and
 - an optical element disposed to affect light from the LED chips;
 - 5 wherein the optical element is less than 5 mm in diameter while maintaining a clearance between any of the LED chips and an edge of the optical element such that the clearance is from approximately 0.2 to 0.8 the width of the plurality of interconnected LED chips.
- 10 2. The LED device of claim 1 wherein the optical element is less than 4 mm in diameter.
3. The LED device of claim 2 wherein the clearance is from approximately 0.3 to 0.65 the width of the plurality of interconnected LED chips.
- 15 4. The LED device of claim 2 wherein the LED chips are connected in parallel and are mounted on a ceramic submount.
5. The LED device of claim 4 wherein the optical element is molded from
20 silicone.
6. The LED device of claim 5 wherein at least some of the plurality of interconnected LED chips are vertical LED chips.

7. The LED device of claim 6 where, when the LED chips are energized, the device emits light with an efficiency of at least 80 lm/W and a color rendering index of at least 80.

5 8. The LED device of claim 7 wherein the optical element is about 3.1 mm in diameter, the efficiency is at least about 89 lm/W and the CRI is at least 82.

9. The LED device of claim 5 wherein at least some of the plurality of interconnected LED chips are sideview LED chips.

10

10. The LED device of claim 9 where, when the LED chips are energized, the device emits light with an efficiency of at least 80 lm/W and a color rendering index of at least 80.

15 11. The LED device of claim 10 wherein the optical element is about 3.1 mm in diameter, the efficiency is at least about 89 lm/W and the CRI is at least 82.

12. An LED device comprising:

a submount;

20

a plurality of LED chips fixed to the submount;

a plurality of wire bonds, each connected between an LED chip and the submount, the plurality of wire bonds arranged so that all the wire bonds tend to the outside of the plurality of LED chips; and

an optical element disposed to affect light from the plurality of LED chips.

13. The LED device of claim 12 wherein the optical element comprises silicone
5 and the submount comprises ceramic.

14. The LED device of claim 13 wherein at least some of the plurality of LED chips are connected in parallel.

10 15. The LED device of claim 14 wherein the plurality of LED chips comprises four LED chips.

16. The LED device of claim 15 wherein at least some of the plurality of LED chips are vertical LED chips.

15

17. The LED device of claim 16 where, when the LED chips are energized, the device emits light with an efficiency of at least 80 lm/W and a color rendering index of at least 80.

20 18. The LED device of claim 17 wherein the optical element is about 3.1 mm in diameter, the efficiency is at least about 89 lm/W and the CRI is at least 82.

19. The LED device of claim 15 wherein at least some of the plurality LED chips are sideview LED chips.

20. The LED device of claim 19 where, when the LED chips are energized, the device emits light with an efficiency of at least 80 lm/W and a color rendering index of at least 80.

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21. The LED device of claim 20 wherein the optical element is about 3.1 mm in diameter, the efficiency is at least about 89 lm/W and the CRI is at least 82.

22. An LED device comprising:

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a ceramic submount;

a plurality of LED chips fixed to the submount, wherein the plurality of LED chips is selected to maximize a color rendering index (CRI) of the LED device; and

a silicone lens disposed to affect light from the plurality LED chips.

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23. The LED device of claim 22 wherein at least some of the plurality of LED chips are vertical LED chips.

24. The LED device of claim 23 where, when the LED chips are energized, the device emits light with an efficiency of at least 80 lm/W and the CRI is at least 80.

20

25. The LED device of claim 24 wherein the optical element is about 3.1 mm in diameter, the efficiency is at least about 89 lm/W and the CRI is at least 82.

26. The LED device of claim 22 wherein at least some of the plurality of LED chips are sideview LED chips.

27. The LED device of claim 26 where, when the LED chips are energized, the device emits light with an efficiency of at least 80 lm/W and the CRI is at least 80.

28. The LED device of claim 27 wherein the optical element is about 3.1 mm in diameter, the efficiency is at least about 89 lm/W and the CRI is at least 82.

29. A method of assembling an LED device, the method comprising:
selecting a plurality of LED chips to maximize a color rendering index (CRI) of the LED device.
fixing the plurality of LED chips to a ceramic submount;
interconnecting the plurality of LED chips; and
attaching a silicone lens to the ceramic submount to affect light from the LED chips.

30. The method of claim 29 further comprising making the ceramic submount from alumina.

31. The LED device of claim 30 wherein at least some of the plurality of LED chips are vertical LED chips.

32. The LED device of claim 30 wherein at least some of the plurality of LED chips are sideview LED chips.

33. The method of claim 29 further comprising making the ceramic submount
5 from aluminum nitride.

34. The LED device of claim 33 wherein at least some of the plurality of LED chips are vertical LED chips.

10 35. The LED device of claim 33 wherein at least some of the plurality of LED chips are sideview LED chips.

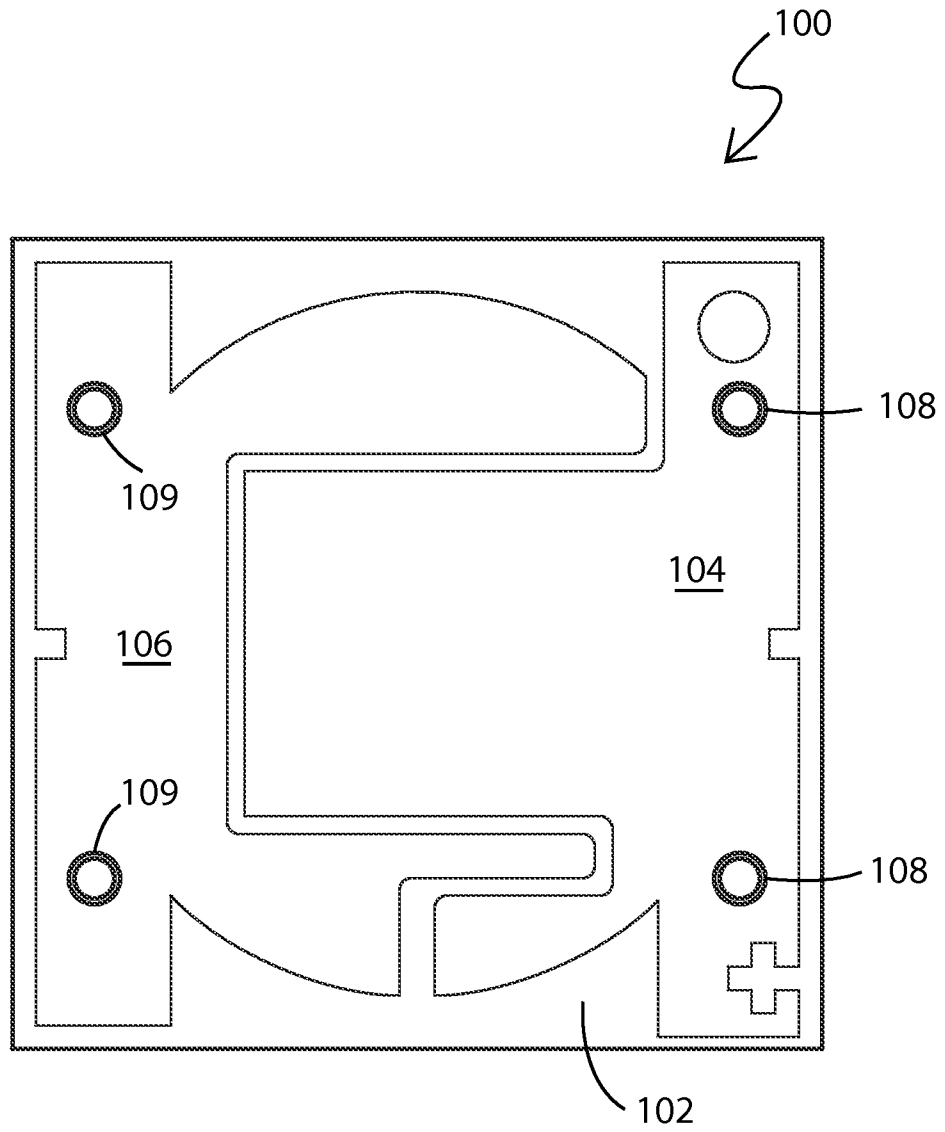


FIG. 1

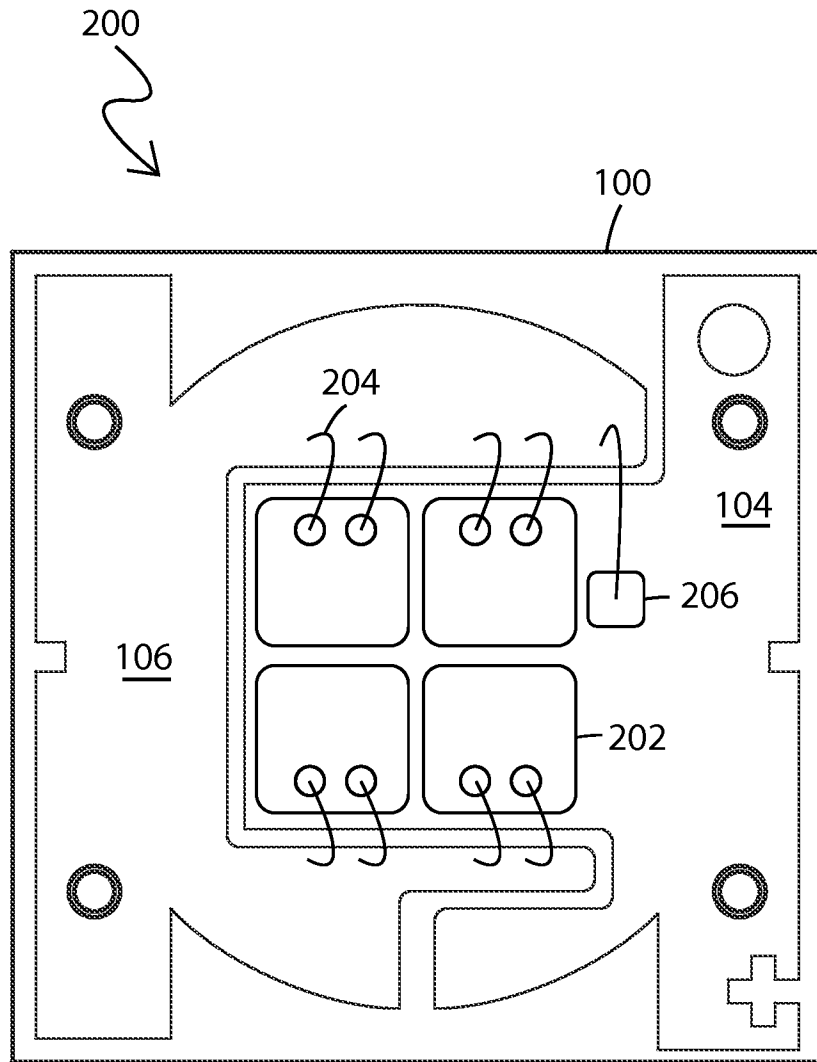


FIG. 2

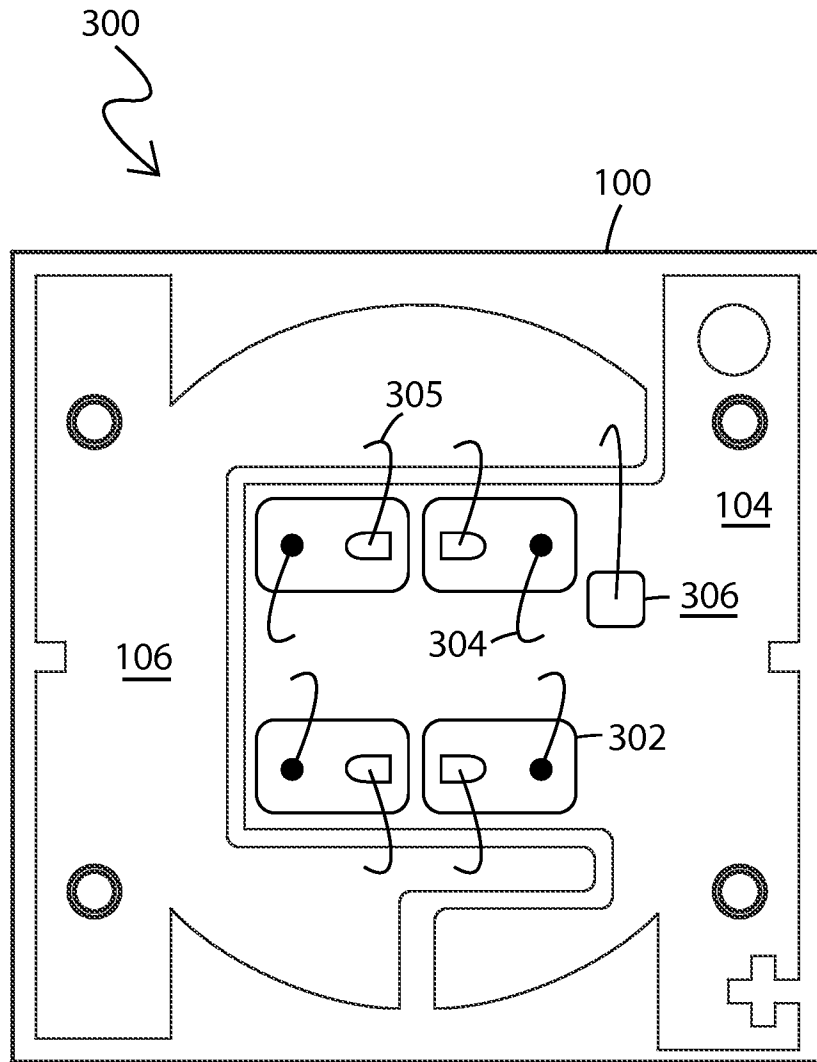


FIG. 3

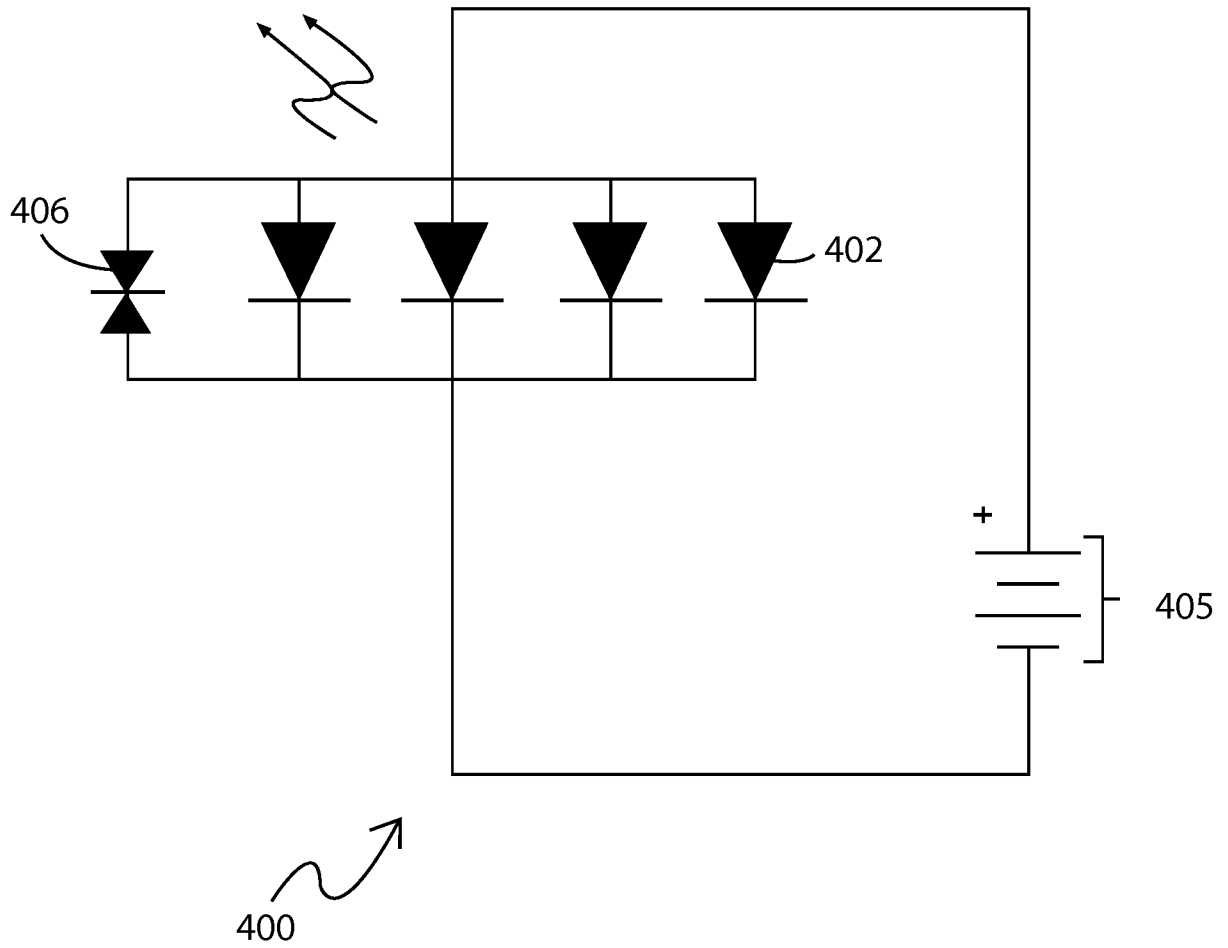


FIG. 4

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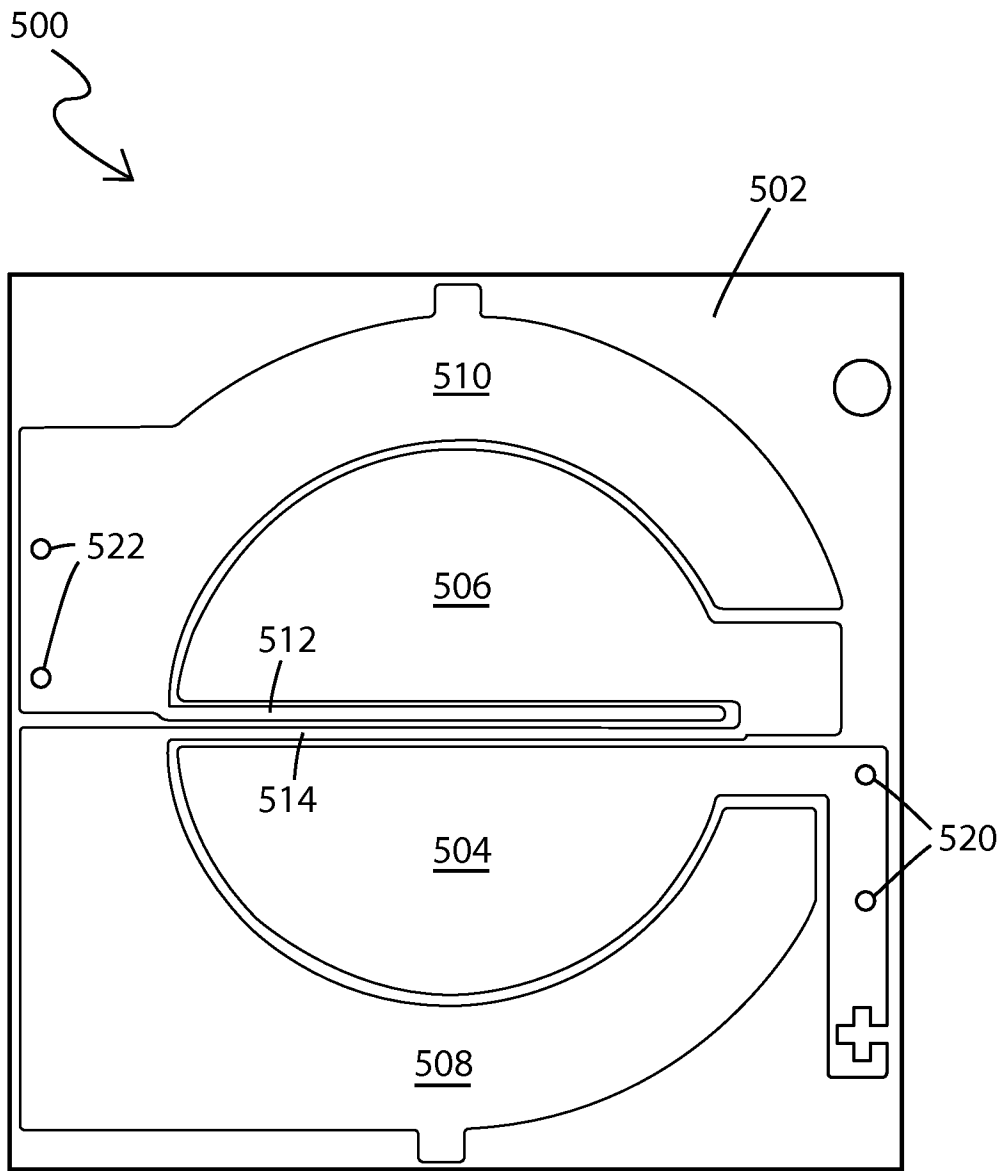


FIG. 5

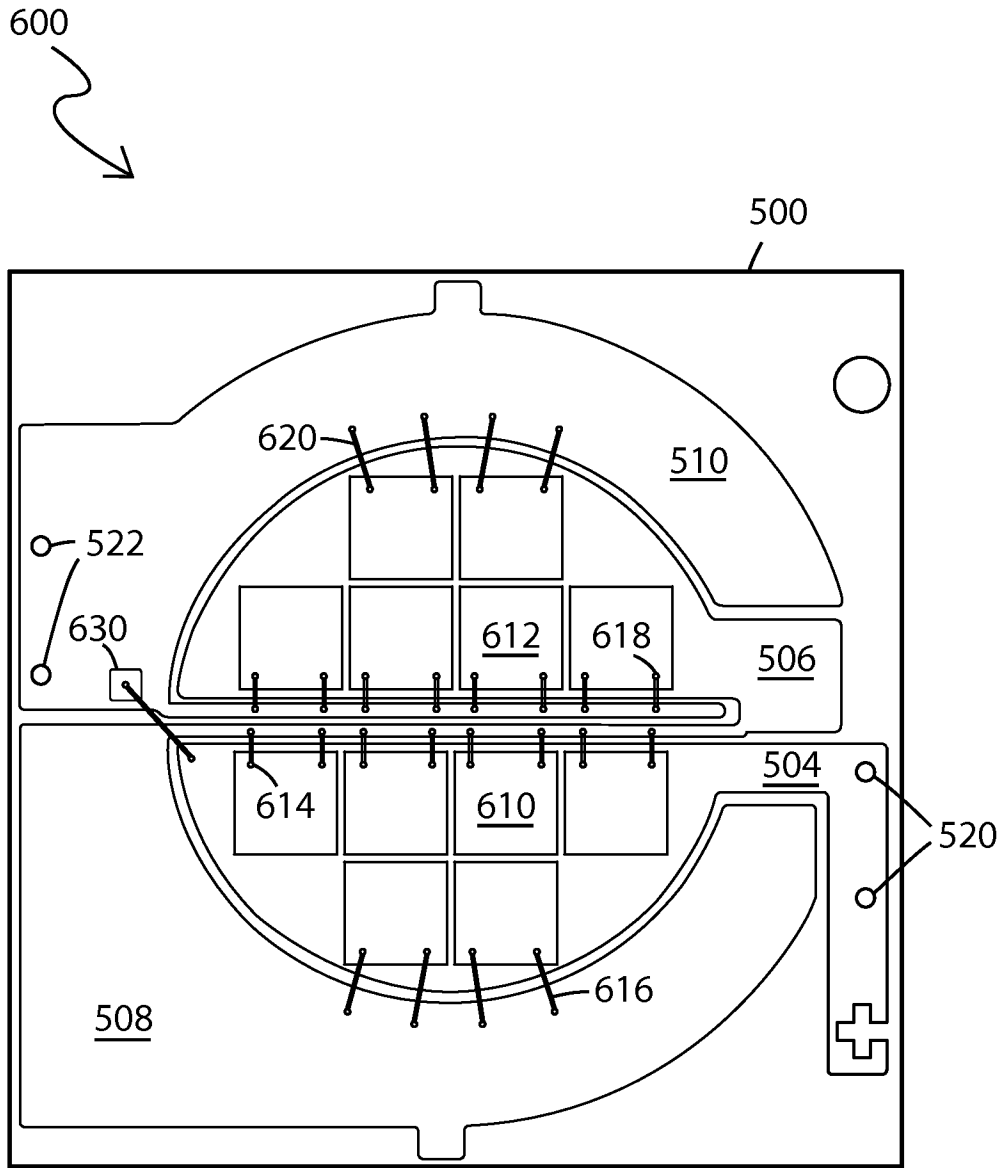


FIG. 6

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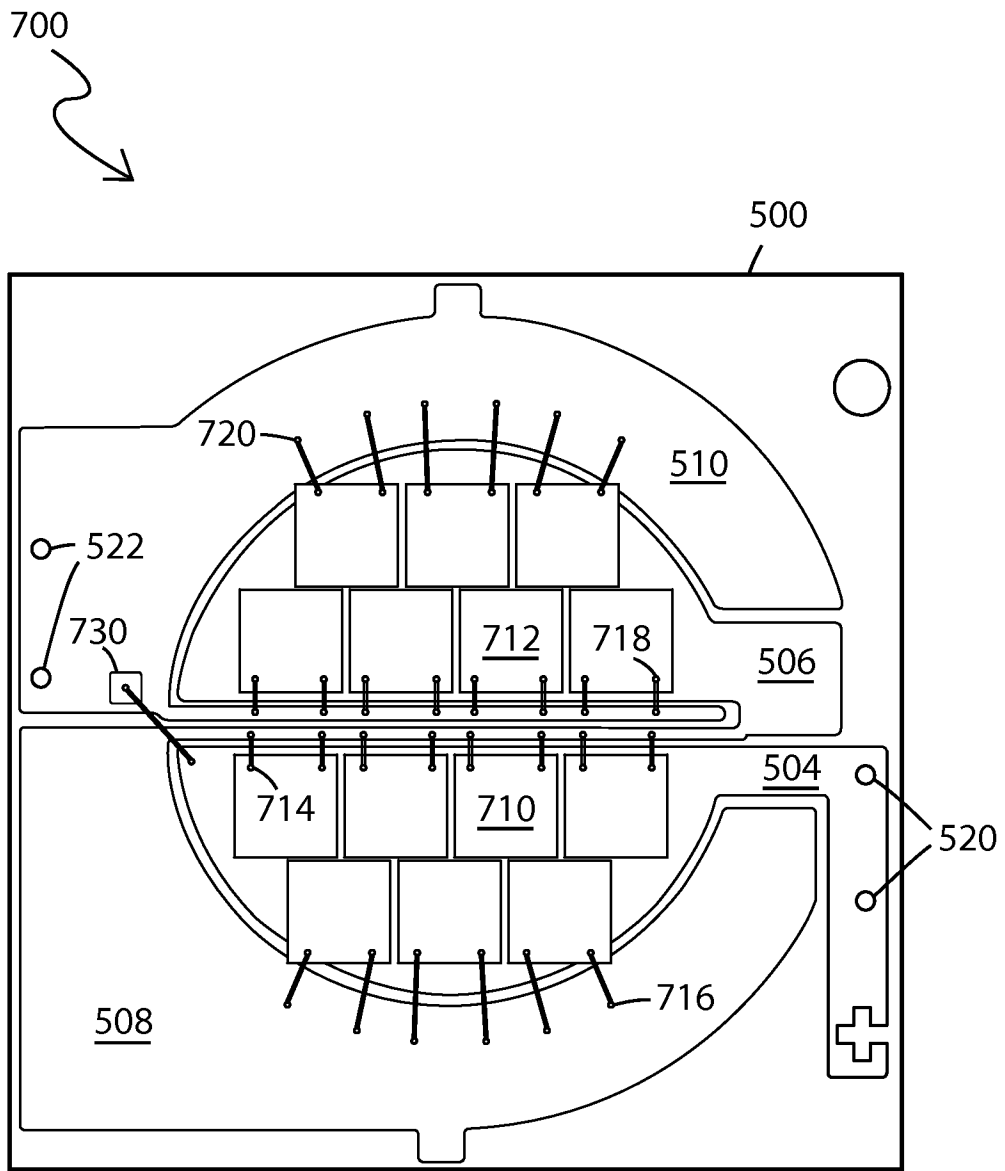


FIG. 7

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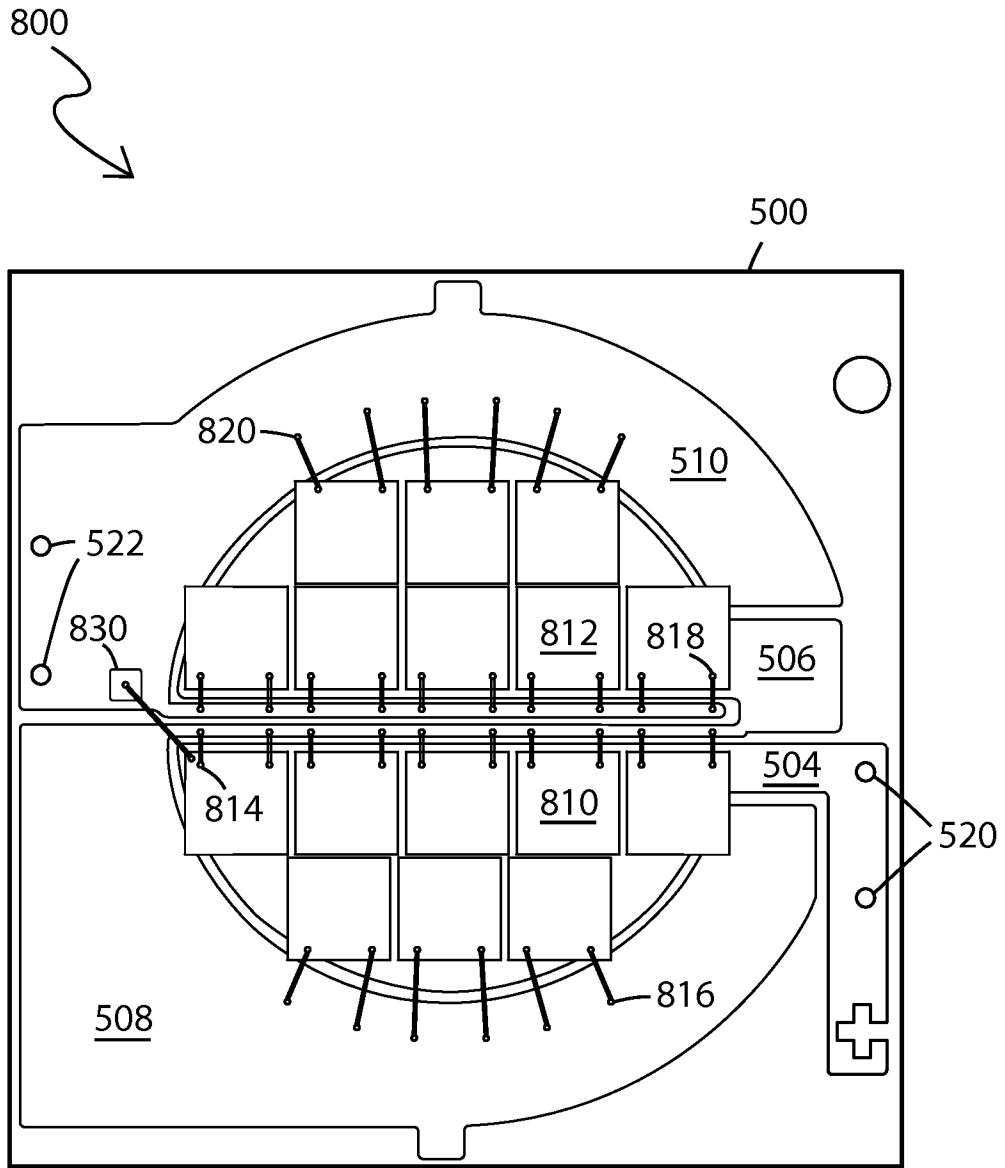


FIG. 8

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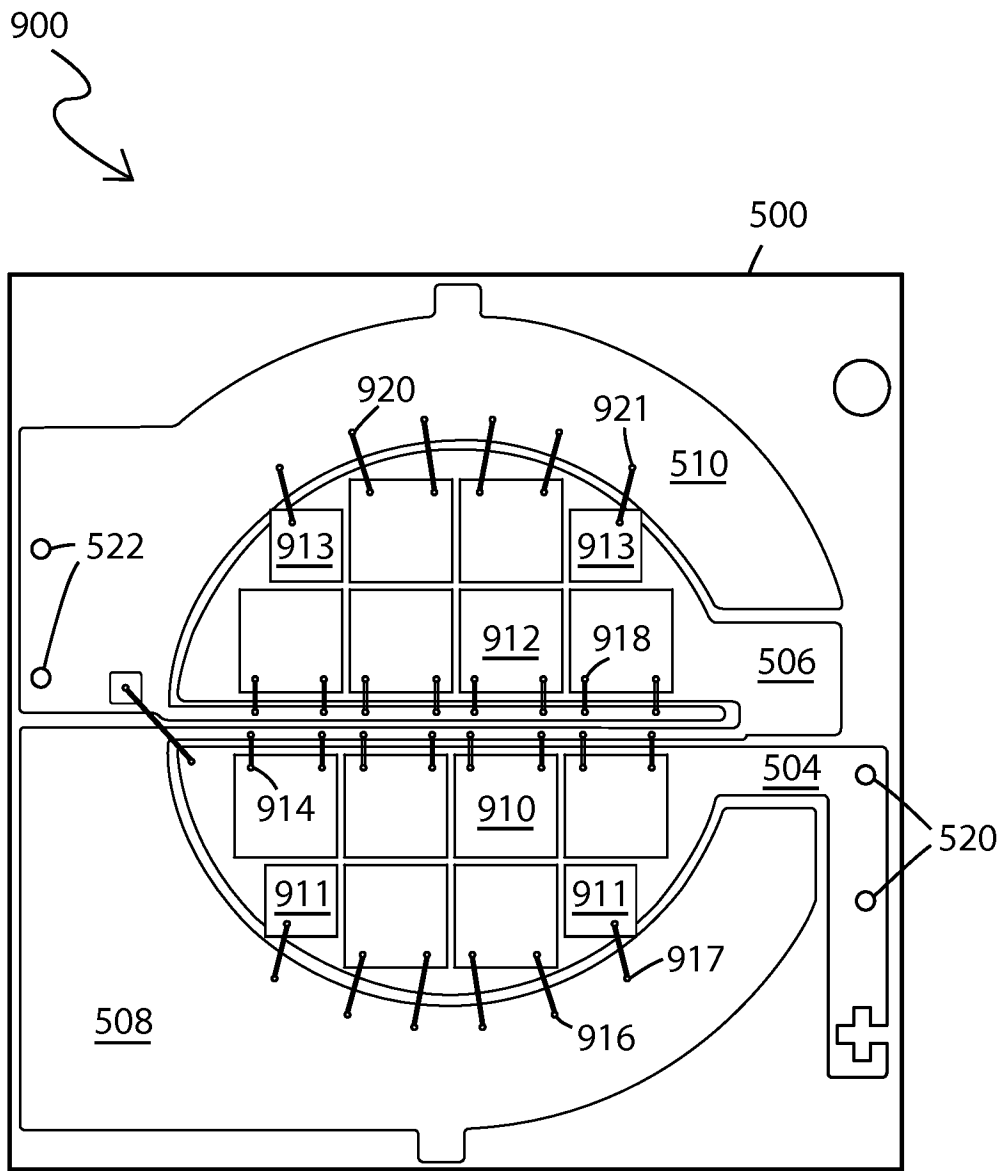


FIG. 9

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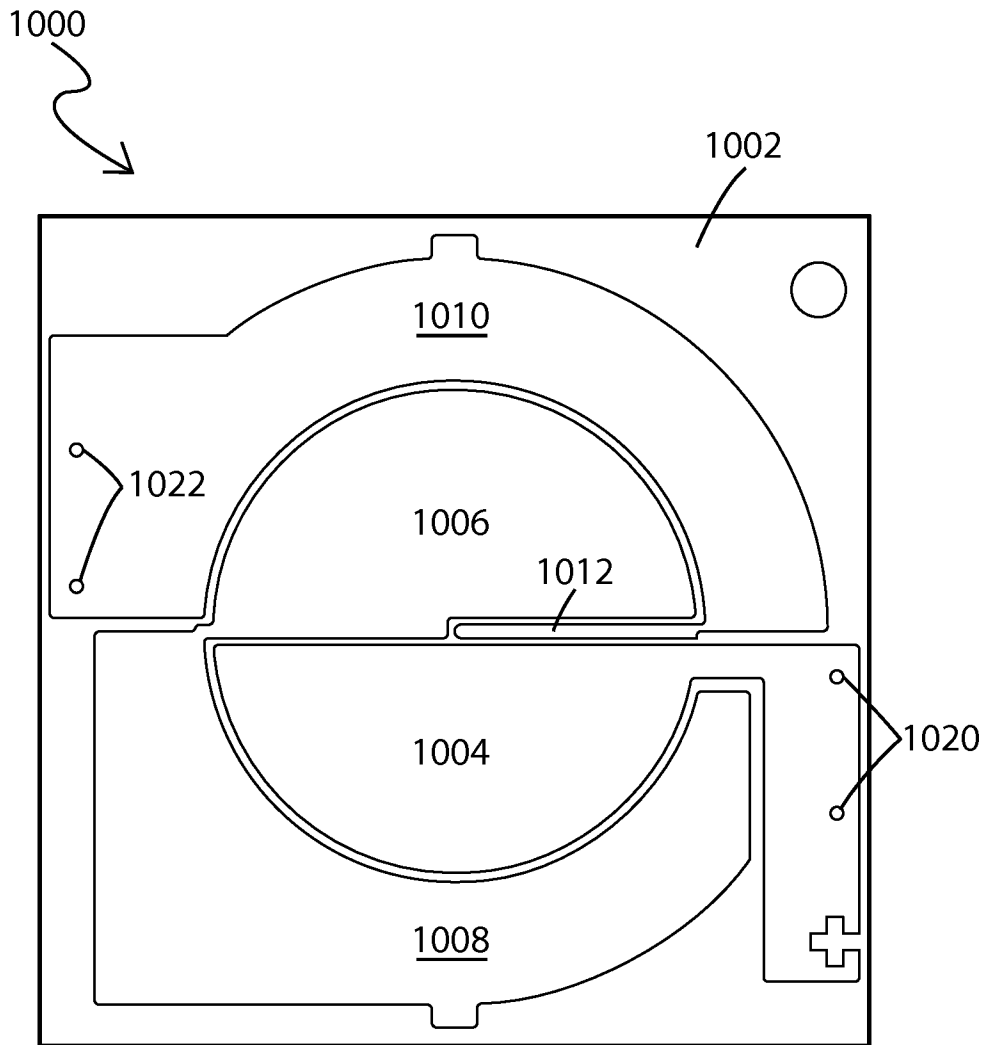


FIG. 10

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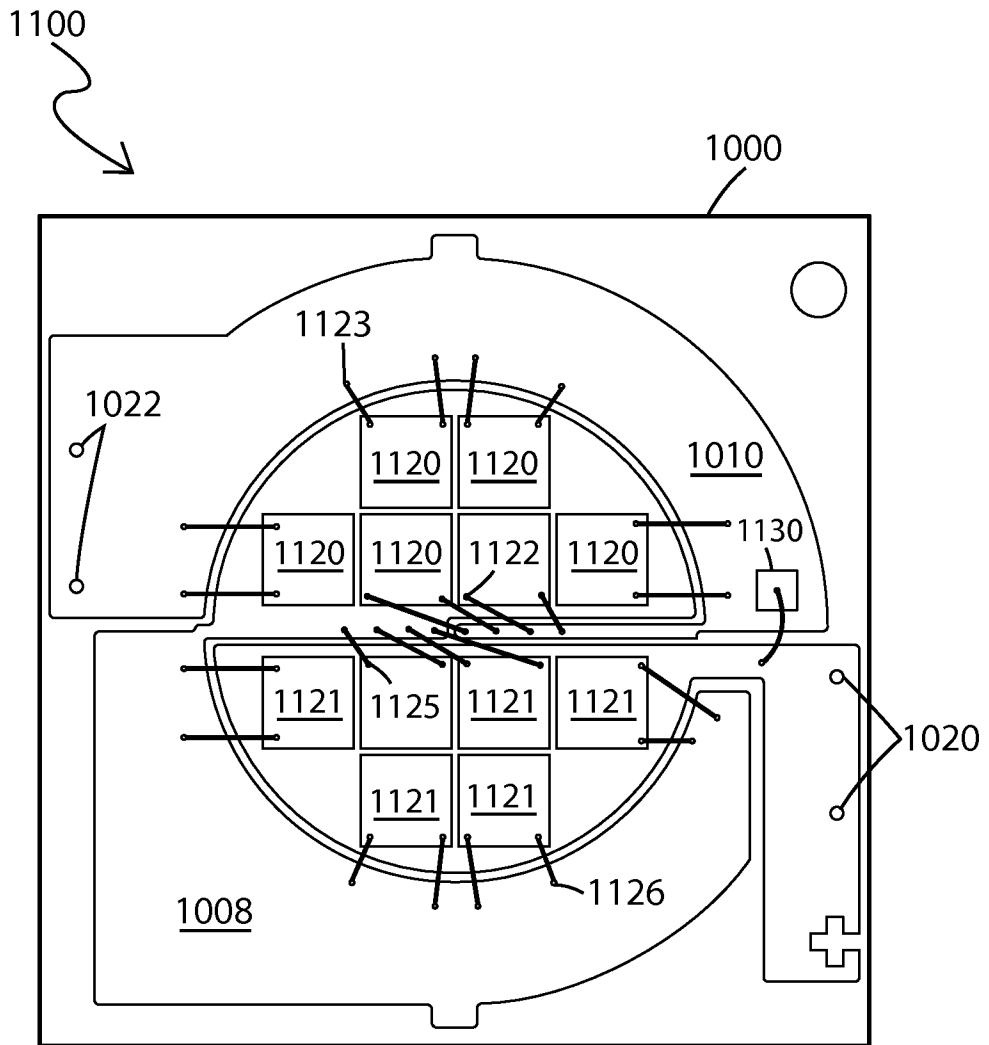


FIG. 11

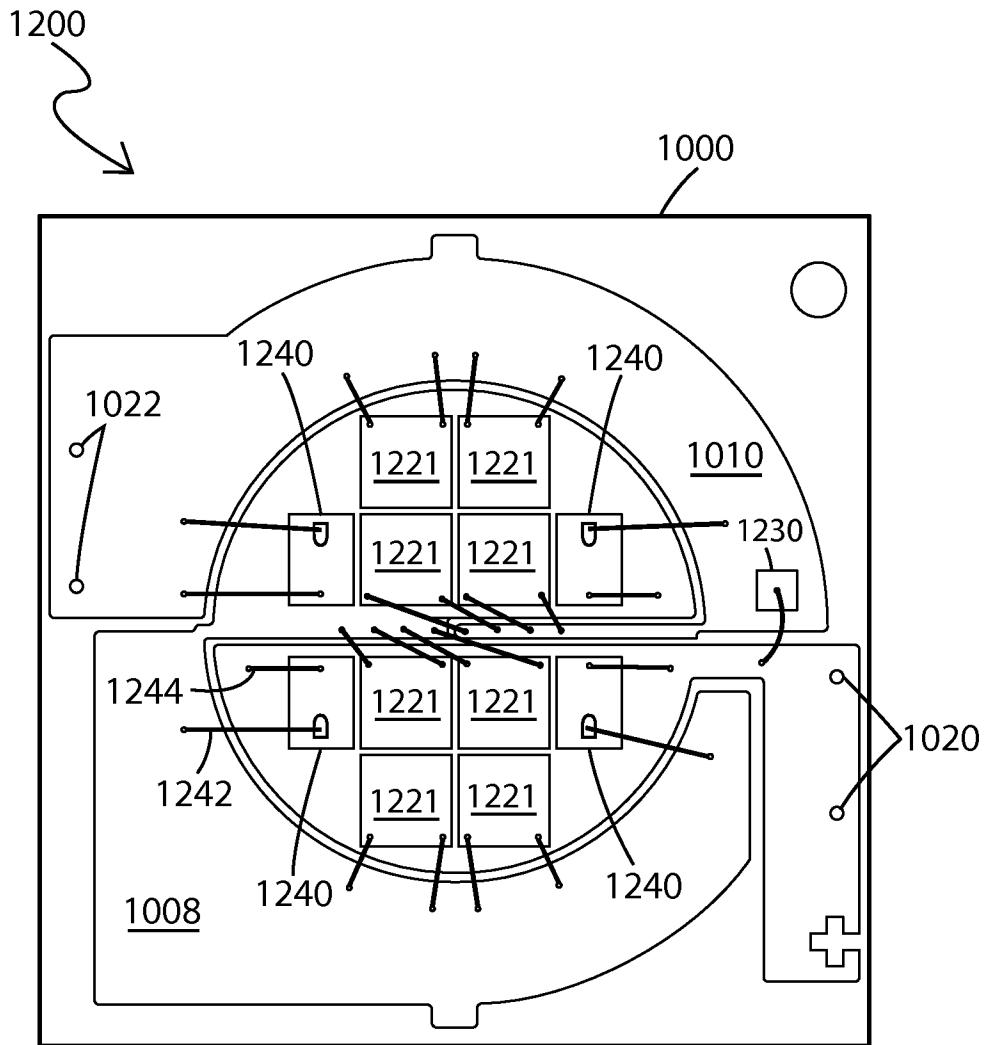


FIG. 12

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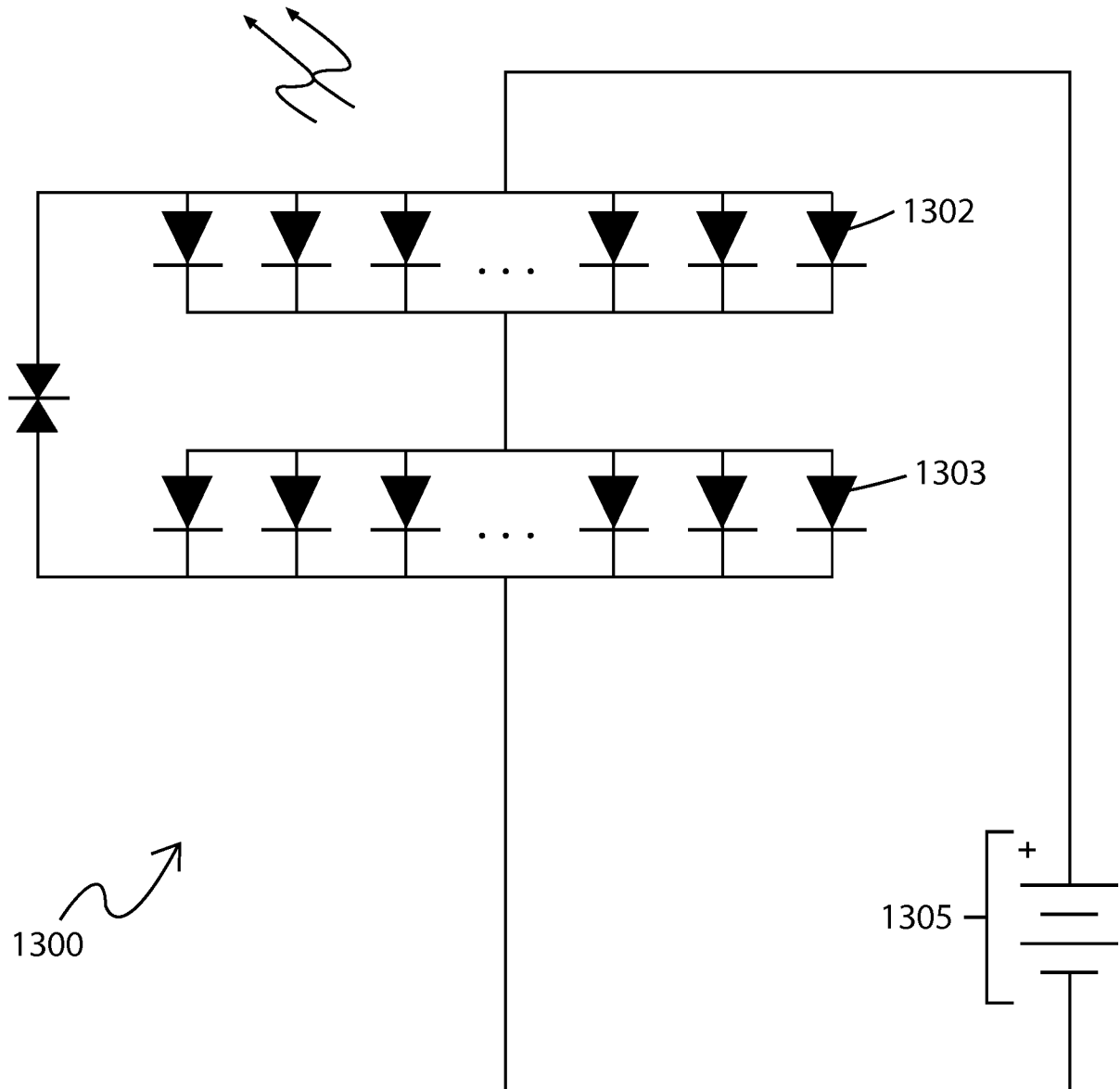


FIG. 13

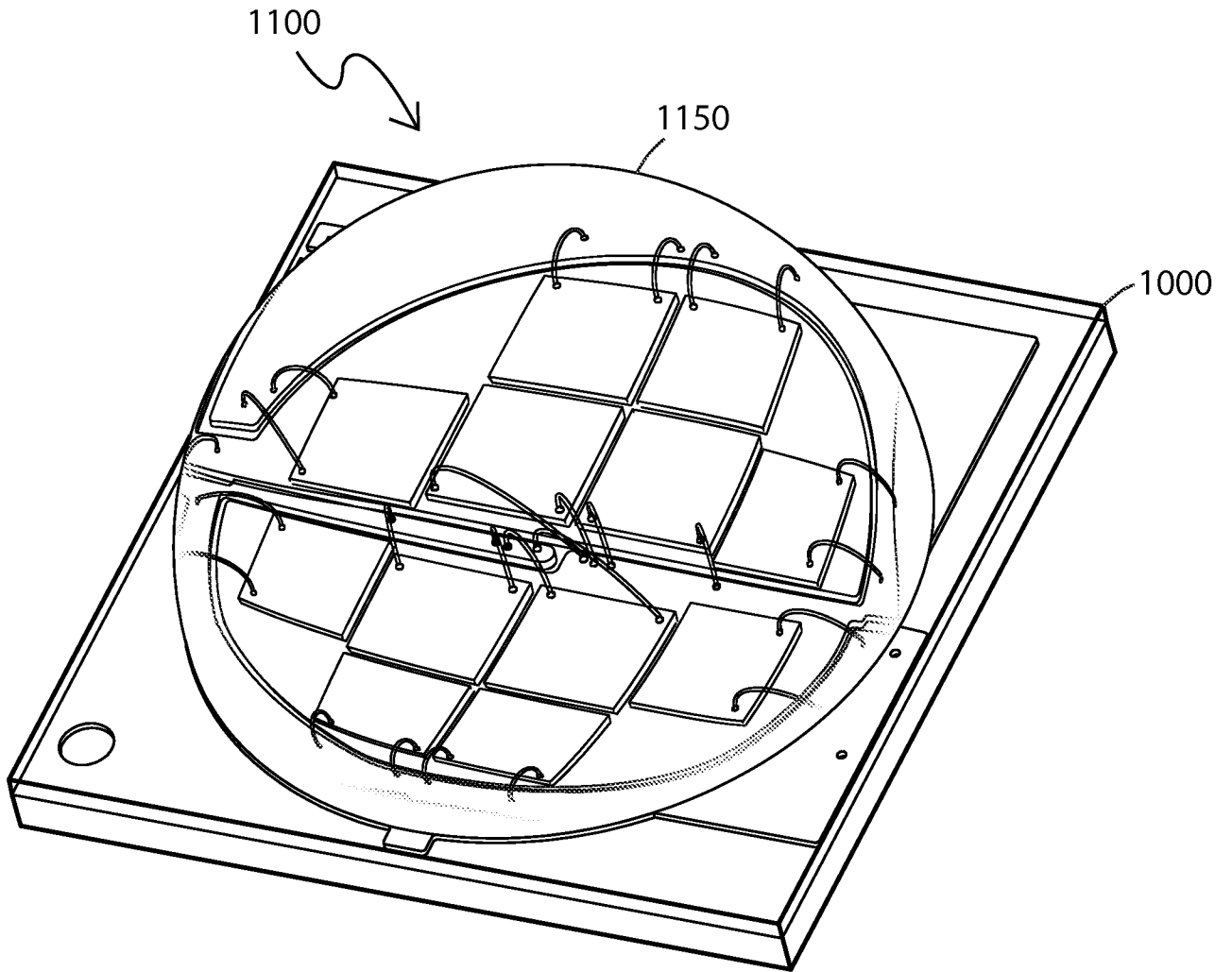


FIG. 14

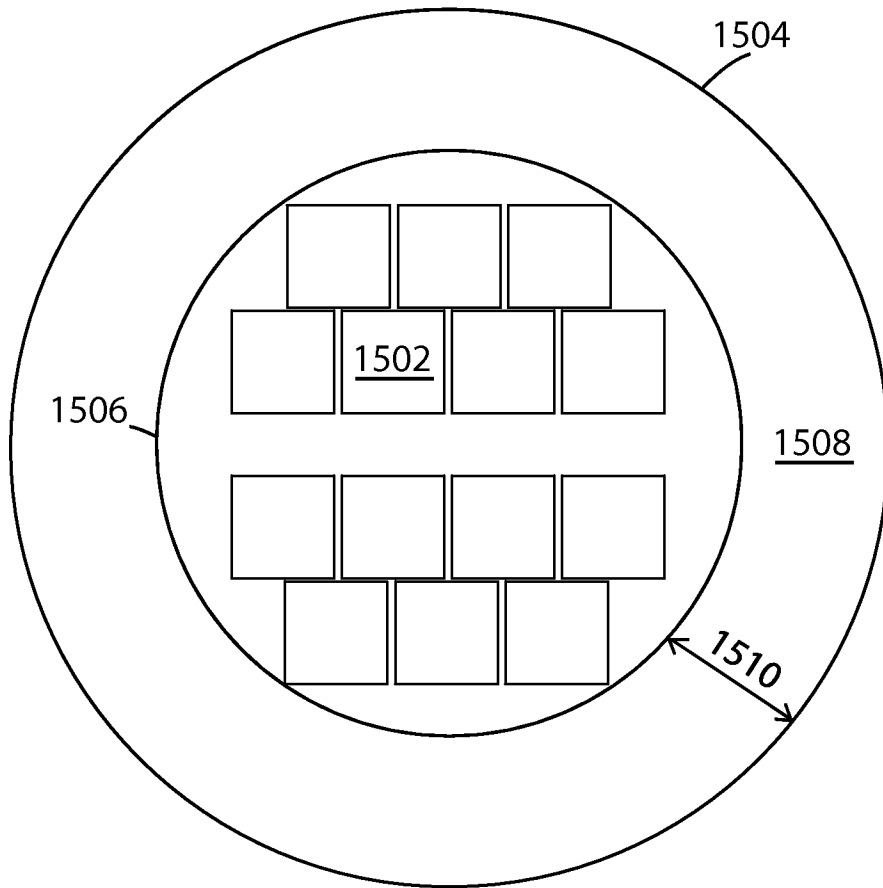


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/052102

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L25/075 H01L33/62
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/050908 A1 (YUAN THOMAS [US] ET AL) 26 February 2009 (2009-02-26)	1-11, 22-35
Y	paragraphs [0007], [0037], [0057], [0059], [0060], [0090], [0091] figures 4a-d,5	12-21
X	US 2010/103660 A1 (VAN DE VEN ANTONY P [CN] ET AL) 29 April 2010 (2010-04-29) paragraphs [0068] - [0071] figures 4a-c,5-7	22,29
Y	US 2007/085944 A1 (TANAKA TOSHIAKI [JP] ET AL) 19 April 2007 (2007-04-19) paragraphs [0110], [0137] figure 61	12-21

Further documents are listed in the continuation of Box C.

See patent family annex.

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Date of the actual completion of the international search 29 November 2011	Date of mailing of the international search report 06/12/2011
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Adams, Richard
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/US2011/052102

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