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(54) SENSE AMPLIFIER FOR DISCRIMINATING BETWEEN TWO VOLTAGE LEVELS

(71) We, MOSTEK CORPORATION, a corporation organised under the laws of the State of Delaware, United States of America and of 1215 West Crosby Road, Carrollton, Dallas County, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates generally to a sense amplifier for discriminating between two voltage levels. The sense amplifier may be used, for example, in the dynamic random access memory comprising a large scale integrated MOSFET circuit which is disclosed in UK Patent Application No. 52563/76 (Serial No. 1,566,408).

It is presently known in the industry how to fabricate dynamic random access read/write memories using MOSFET integrated circuit technology. These circuits typically utilize 4,096 or 16,384 storage cells each comprised of a capacitive storage node and a single transistor connecting the node to a column or digit line. For a 4096 bit system, the storage cells are typically arranged in an array of sixty-four rows and sixty-four columns. Data is stored in a cell by charging the digit line to either ground potential or a voltage somewhat less than the drain supply voltage, while momentarily turning the transistor on by bringing a row enable line high to store the voltage of the digit line on the storage node. A logic "0" is stored when the voltage on the node is less than some selected voltage between the drain supply voltage, typically +12 volts, and the source supply voltage or ground, and a logic "1" when the stored voltage is greater than the selected voltage. A typical value for the arbitrary voltage level is about five volts. Data is read from a storage cell by first precharging the digit line to some voltage, and then after termination of the precharge, turning the transistor connecting the cell to the digit line on. If a logic "0" is stored on the node, the voltage of the column line is decreased by a greater amount or increased by a lesser amount than when a logic "1" is stored .These two ultimate levels of voltage on the digit line are then discriminated by a sense amplifier to read the logic "1" or logic "0" from the cell.

One method for discriminating between the different voltage changes on the digit line is described in U.K. Patent Application No. 50439/75 (Serial No. 1,533,997) corresponding U.S. Patent Specification No. 3,969,706). This method samples the voltage on the digit line before the cell is addressed and compares this sampled voltage with the voltage on the digit line after the cell is addressed. This system has proven successful and has been commercially employed. Another approach to the problem is typified by U.S. Patents No. 3588844 and 3514765 issued to Christensen. In this system, the digit line is divided into equal parts and connected to a balanced sense amplifier. This type of system has been employed by various workers in the art with varying degrees of success. However, various embodiments of this type of system have heretofore consumed D.C. power, or have alternatively required an unreasonable period of time for precharge, or have alternatively required an unreasonable period of time to read data, or have alternatively resulted in an unacceptably low level voltage on the digit line which should remain high, or have alternatively required additional means to restore the digit line to an appropriately high level, or have alternatively required a larger signal and, hence, a larger storage cell for proper sensing.

The present invention provides a sense amplifier for discriminating between two voltage levels, comprising:

first and second input nodes for receiving the two voltage levels;

third, fourth and fifth nodes;

a first transistor connecting the third node to the fifth node;

a second transistor connecting the fourth node to the fifth node;

a third transistor connecting the first input node to the third node;

a fourth transistor connecting the second input node to the fourth node;

the voltage on the gate of the first transistor being responsive to the voltage on the fourth node;

the voltage on the gate of the second transistor being responsive to the voltage on the third node; and

first circuit makes for holding a precharge voltage on the fifth node while the voltage levels on the first and second input nodes are established on the third and fourth nodes via the third and fourth transistors, and then causing the voltage on the fifth node to be discharged to permit the first or second transistor to discharge the third or fourth node in a predetermined preference determined by the relative voltage levels on the third and fourth nodes, the circuit means including fifth and sixth transistors providing parallel discharge paths for the fifth node, the sixth transistor having a substantially large conductance than the fifth transistor such that the fifth node is discharged at a relatively slow rate when the fifth transistor is turned on while the sixth transistor is off and at a relatively fast rate when the sixth transistor is turned on.

The sense amplifier of this invention will be better understood by reference to the following detailed description of a dynamic random access memory together with reference to the accompanying drawings, wherein:

Figure 1 is a schematic circuit diagram of a dynamic random access memory;

Figure 2 is a schematic diagram illustrating a typical subcomponent used to operate a portion of the circuit of Figure 1; and

Figure 3 is a timing diagram which serves to illustrate the operation of the circuit of Figure 1.

Referring now to the drawings, a portion of a dynamic random access memory is indicated generally by the reference numeral 10 in Figure 1. The system may typically include 4,096 or 16,384 binary storage cells formed on a single integrated circuit which also includes the appropriate control circuitry. The control circuitry not herein disclosed in detail may be any prior art control circuitry such as that described in U.K. Patent Application No. 50439/75. (Serial No. 1,533,997). Four of the storage cells are indicated by the reference character S in Figure 1. Each storage cell is comprised of a capacitive storage node 12 and a field effect transistor 14 which are connected in series between a digit line DL_1 or $\overline{DL}_1$ and V_{DD}, i.e. the drain supply voltage.

Storage cells S are arrayed in equal numbers of rows and columns, typically 64 for a 4,096 bit system, and 128 for a 16,384 bit system. (The orientation of the figure being convenient in laying out the drawing and the terms 'row' and 'column' having the usual significance as known from the art). For ease of discussion, only the first column of storage cells will be discussed, although it will be understood that another 63 columns of identical configurations would be provided in a typical system. Half of the 64 storage cells S arrayed in each column are connected to a true digit line DL_1 and the other half are connected to a complement digit line $\overline{DL}_1$ as illustrated in Figure 1. Each of the digit lines DL_1 and $\overline{DL}_1$ are the same geometric configuration and are connected to the same number of storage cells S. In addition a dummy cell $\overline{SD}$ is connected to digit line DL_1 and another dummy cell SD is connected to digit line $\overline{DL}_1$ to establish a reference voltage on one of the digit lines as will presently be described. The gates of all of the storage cells S in a common row are connected to a row select line RS. Row select lines RS_{31}—RS_{34} are illustrated in Figure 1. Of course, it will be understood that row select lines RS_1—RS_{30} and RS_{35}—RS_{64} have been omitted in order to simplify the illustrations.

The true digit line DL_1 is connected to the true input node 28 of a latching differential amplifier by the channel of a first transistor 20 and the complement digit line $\overline{DL}_1$ is connected to the complement input node 30 of the latching differential amplifier by the channel of a second transistor 22. The latching differential amplifier includes third and fourth transistors 24 and 26 which connect input nodes 28 and 30 to a latch bus 32. The gate of the third transistor 24 is cross coupled to the complement input node 30 and the gate of the fourth transistor 26 is cross coupled to the true input node 28. The latch bus 32 is pulled toward ground at a relatively slow rate when transistor 34 is turned on by the clock signal L_1, and at a much faster rate when transistor 36 is turned on by clock signal L_2 because transistor 36 has a substantially larger conductance than transistor 34. Clock signal L_1 goes high slightly before clock signal L_2 for purposes which will presently be described in connection with Figure 3.

The gates of all transistors 20 and 22 for the 64 digit lines are connected to a common node 40 which may be precharged to V_{DD} through transistor 42. The gate of transistor 42 is connected to V_{DD} through

transistor 44, the gate of which is controlled by precharge signal P_3. The gate of transistor 42 is capacitively boosted above V_{DD} by capacitor 43 receiving clock signal L_3 which occurs after transistor 44 has been turned off by precharge signal P_3 as will presently be described. Node 40 is capacitively coupled to latch bus 32 by capacitor 46 to assist the stray capacitance of transistors 20 and 22 in driving node 40 above V_{DD} as will presently be described.

The true and complement digit lines DL and $\overline{DL}$ of all 64 columns are precharged from node 50 through transistors 52 and 54, the gates of which are controlled by the common precharge signal P_3. Node 50 is driven to V_{DD} through a transistor 56, the gate of which is controlled by precharge signal P_2 which goes above V_{DD}. Data may be written in an addressed cell, or read from an addressed cell by true and complement data buses DB and $\overline{DB}$ and column select transistors 60 and 62, respectively, the gates of which are controlled by a column select line CS_1.

Dummy cells SD and $\overline{SD}$ each have a capacitance approximately one-half the capacitance of a data storage cell S. Dummy cell SD is enabled by line 66 whenever any one of the row select lines RS_1—RS_{32} associated with digit line DL_1 is active. Similarly, dummy cell SD is enabled by line 68 whenever any one of the row select lines associated with digit line DL_1 is active. The storage node of dummy cell SD is precharged to ground potential through transistor 70, and the storage node of dummy cell $\overline{SD}$ is precharged to ground potential through transistor 72 when precharge signal P_1 applied to lines 74 and 76 is high as will be presently be described.

Precharge clock signals P_2 and P_3 both require voltages above the drain supply voltage V_{DD} for satisfactory operation of the circuit as will hereafter, be described in greater detail. The drain supply voltage V_{DD} is usually the maximum externally generated supply voltage available in the circuit and in the commercial embodiment of the present invention is +12 volts, since N-channel silicon gate process technology is employed. It is desired for P_2 and P_3 to have high levels of approximately +16 volts. A suitable system for producing a clock voltage greater than the drain supply voltage V_{DD} is illustrated schematically in Figure 2. This system is described in detail in U.K. Patent Application No. 52561/76. (Serial No. 1,525,810). This system utilizes a plurality of delay stages 80, 82 and 83. The output of delay stage 80 is applied to the input of delay stage 82, the output of which is applied to the input of delay stage 83. The output of delay stage 82 is fed back to delay stage 80 to isolate the output node 84 from delay stage 80. The output of delay stage 83 is capacitively coupled to node 84 by capacitor 86. Thus as a result of a precharge timing signal P_A to delay stage 80, node 84 is first driven substantially to V_{DD} after one delay period. A short time later, the output of delay stage 82 turns the output of delay stage 80 off, thus isolating the voltage on node 84. Then when the output of delay stage 83 subsequently goes to V_{DD} node 84 is capacitively boosted above V_{DD}. This circuitry easily provides an output of 16 volts from a supply voltage V_{DD} of 12 volts. Other suitable systems may be employed to produce the precharge clock signals P_2 and P_3 above V_{DD}.

The operation of the circuit of Figure 1 may best be understood by referring to the timing diagram of Figure 3. Figure 3 illustrates the voltage with respect to time of precharge signals P_1, P_2 and P_3 by means of time lines 100, 102 and 104, respectively. The voltage on the one active row select line RS_1 through RS_{64} and also the appropriate dummy cell enable line RS_D or $\overline{RS_D}$ is indicated by time line 106. All other row select lines RS_1 through RS_{64} and the other dummy cell enable line remain at ground potential. Latch clock signals L_1, L_2, and L_3 are indicated by time lines 108, 110, and 112, respectively. The voltage resulting on latch bus 32 is represented by time line 114, and the voltages resulting on the true and complement digit lines DL and $\overline{DL}$ are represented by time lines 116 and 118 respectively. The voltage on the addressed column select line CS is represented by time line 120, and the resulting voltages on the true data bus DB and the complement data bus $\overline{DB}$ are represented by time lines 122 and 124, respectively.

During the precharge period, i.e., the period between active cycles, precharge signal P_1 is at V_{DD}, i.e., +12 volts, and precharge signals P_2 and P_3 are above V_{DD} at +16 volts. As a result of P_1 being high, transistors 70 and 72 are turned on to discharge the nodes of dummy cells SD and $\overline{SD}$ to ground or 0 volts. P_2 is at +16 volts so that transistor 56 is turned on and node 50 is charged fully to V_{DD}. The digit line precharge signal P_3 is at +16 volts so that digit lines DL and $\overline{DL}$ are all charged to +12 volts as indicated by lines 116 and 118 in Figure 3.

As will hereafter be more evident, node 40, which is represented by time line 126 in Figure 3, is at +16 volts as a result of capacitive coupling through the gates of transistors 20 and 22 of all sixty-four columns and also capacitor 46. In this regard, it will be appreciated that transistor 42 is non-conductive even though node 40 has been bootstrapped above V_{DD} because its gate and effective source node in this

condition are both at V_{DD}. Since V_{DD} is applied to the gates of both transistors 24 and 26, the latch bus 32 will be precharged to V_{DD} less one threshold, or about +10 volts.

At the start of an active cycle, precharge signal P_1 goes from +12 volts to ground, as represented by event 100a, so as to turn transistors 70 and 72 off, and precharge signal P_2 falls from +16 to +12 volts, as represented by event 102a, so that transistor 56 is effectively turned off since node 50 is also at V_{DD}. At this stage, it will be noted that precharge signal P_3 is still at +16 volts for a short time after transistor 56 is turned off to permit the voltages on digit lines DL_1 and $\overline{DL_1}$ to precisely equalize through transistors 52 and 54, even though noise in the voltage supply V_{DD} together with unequal capacitive values of the digit lines or unequal conductances of transistors 52 and 54 may have otherwise resulted in unequal voltages on digit lines DL_1 and $\overline{DL_1}$, at the instant transistor 56 turned off. Then precharge signal P_3 goes to ground, trapping the precisely equal precharge voltages on digit lines DL_1 and $\overline{DL_1}$ at a level substantially equal to V_{DD}, as represented by event 104a. After precharge signal P_3 is at ground, the one row select line identified by the row address signals applied to the chip goes from 0 volts to +12 volts as represented by event 106a. At the same time, the appropriate dummy cell is also addressed. For example, assume row select line RS_{31} is active. In that event, dummy cell SD would be enabled by line 66 going from 0 to +12 volts. If a logic "0" is stored in the addressed storage cell, the voltage on digit line DL_1 would drop to a greater extent than the voltage on digit line $\overline{DL_1}$ because of the fact that the capacitance 12 of the storage cell is approximately twice the capacitance of the dummy cell. Since the node 40 is at +16 volts, this change in the voltage on digit lines DL_1 and $\overline{DL_1}$ is freely transferred to input nodes 28 and 30 of the differential amplifier. However, the latch bus 32 is still one threshold below the precharge voltage of digit lines DL_1 and $\overline{DL_1}$ so that conductance does not yet occur through either transistor 24 or 26. Next latch clock signal L_1 goes from 0 to +12 volts, thus beginning to slowly discharge the latch bus 32 as represented by event 114a. As the voltage of latch bus 32 begins to fall, transistor 24 begins to conduct before transistor 26 because node 30 has a slightly higher voltage than node 28. As transistor 24 conducts, node 28 is progressively lowered almost as fast as latch bus 32 so that transistor 26 remains essentially off, thus keeping node 30 high and progressively increasing, the gate-to-source bias on transistor 24. This condition is greatly assisted by the fact that initially transistor 20 has a low gate voltage with respect to its source voltage and thus provides considerable resistance between node 28 and digit line DL_1. Since node 28 has a relatively small capacitance compared to that of digit line DL_1, node 28 can be quickly discharged by relatively small currents through transistor 24. After a very short period of time, the differential voltage between nodes 28 and 30 increases substantially and latch clock signal L_2 goes high as represented by event 110a which causes latch bus 32 to discharge at a much greater rate as represented by event 114b in Figure 3. As latch bus 32 transitions to ground, both transistors 24 and 20 become increasingly more conductive so that digit line DL_1 is very rapidly discharged to ground as represented by event 116b. However, digit line DL_1 remains near V_{DD}, typically +11 volts, as represented by event 118b.

Because of the capacitive coupling between node 40 and the digit lines DL_1 and $\overline{DL_1}$ provided by the stray capacitance of all the transistors 20 and 22 of all columns as well as the capacitor 46 between node 40 and latch bus 32, node 40 is also pulled down to approximately +12 volts as digit line DL_1 is pulled to ground as represented by event 126a.

If a logic "1" had been stored in the addressed storage cell, on the other hand, as defined by a voltage in the cell greater than +5.0 volts, then data line DL_1 would have a voltage greater than data line $\overline{DL_1}$ after the row select signal 106a. This would result in digit line DL_1 remaining high as represented by dotted line 116c and digit line $\overline{DL_1}$ would go low as represented by dotted line 118c in Figure 3 when the voltage on the latch bus transitioned low in response to events 108a and 110a of latch clock signals L_1 and L_2. It is for this case, i.e., proper sensing of a high stored voltage, that the dummy cell is required. Without it, there would be nothing to provide the negative voltage transition on digit line $\overline{DL_1}$ and thus provide the differential voltage necessary for proper sensing.

When the column select line CS goes from 0 to +12 volts as indicated by event 120a, true data bus DB goes from a precharge level of +12 volts to 0 volts as represented by event 122a, assuming that a logic "0" was stored in the addressed storage cell attached to the true digit line DL_1, and complement data bus $\overline{DB}$ remains at +12 volts as represented by event 124a. On the other hand, if a logic "1" had been stored in the addressed storage cell attached to the true digit line DL_1, then the true data bus DB would remain high as represented by dotted line 122b and the complement

data bus $\overline{DB}$ would go to ground as represented by dotted line 124b.

As previously mentioned, the gate of transistor 42 was precharged to V_{DD} during the precharge period while signal P_3 was at +16 volts. During the active cycle, P_3 transitioned to 0 volts, thus turning transistor 44 off and trapping approximately +12 volts on the gate of transistor 42. After node 40 has been discharged to about +12 volts as a result of digit lines DL_1 or $\overline{DL_1}$ and latch bus 32 going to ground, latch clock signal L_3 goes from 0 to +12 volts as indicated by event 112a in Figure 3. This signal is coupled through capacitor 43 to the gate of transistor 42, thus driving the gate substantially above V_{DD} to ensure that node 40 is established at +12 volts as represented by event 126b. In normal operation, this merely overcomes leakage from node 40, but during start up provides the initial +12 volt charge before capacitive boosting occurs as will now be described.

At the end of an active cycle, row select line 106 goes to ground at event 106b and column select line CS goes to ground at event 120b so that the transistors of the addressed storage cell and the addressed dummy cell are turned off and so that column address transistors 60 and 62 are turned off. Latch clock signal L_3 also goes to ground as represented by event 112b, pulling the gate of transistor 42 back to approximately V_{DD} so that node 40 can be capacitively boosted above V_{DD}. Latch clock signals L_1 and L_2 also go to ground as represented by events 108b and 110b.

Precharge signals P_1 and P_3 then go to +12 volts as represented by events 100b and 104b, and precharge signal P_3 goes to +16 volts at event 104c, which is approximately two delay stages later than event 104b as a result of the operation of a circuit such as illustrated in Figure 2. Precharge signal P_2 may conveniently transition from +12 volts to +16 volts at the same time as represented by event 102b.

As precharge signal P_3 goes positive at event 104b, transistors 52 and 54 turn on so that the digit line DL_1, $\overline{DL_1}$ which has been discharged to ground begins to charge positively as represented by either the solid line 116d or by the dotted line 118d in Figure 3. This charging continues during the precharge period as precharge signal P_3 goes to +16 volts at event 104c and is facilitated by the fact that precharge signal P_2 also goes to +16 volts so that node 50 is rapidly charged all the way to V_{DD} of +12 volts. From lines 116 and 118 of Figure 3, it will be noted that the digit line DL_1 or $\overline{DL_1}$ which remained near V_{DD} is initially partially discharge when transistors 52 and 54 are turned on, as represented by events 116e and 118e.

The latch bus 32 is precharged through transistor 20 and 24, and through transistors 22 and 26, of all of the columns to a voltage level one threshold below V_{DD} as represented by event 114c.

Node 40, which is now isolated because transistor 42 was turned off when latch clock signal L_3 went to ground at event 112b, is capacitively boosted back to about +16 volts, as represented by event 126c, because of the stray capacitance of transistors 20 and 22 of all columns and of capacitor 46 which is added to enhance this boosting. It will be appreciated that either the true or complement digit line DL_1 or $\overline{DL_1}$ of every column is discharged during each row address cycle so that the combined stray capacitance of 64 transistors contributes to boosting node 40 above V_{DD} as the 64 digit lines are recharged from ground to +12 volts. As a result, node 40 is normally capactively boosted to about +16 volts during the precharge cycle.

The data buses DB and $\overline{DB}$ are similarly precharged to +12 volts as represented by events 122c and 124c by circuitry which is not illustrated. In the preferred embodiment of the present system, precharge circuitry similar in function to that used to precharge the digit lines DL_1 and $\overline{DL_1}$ is also used to precharge the true and complement data buses DB and $\overline{DB}$ and this fact causes the recharge events 122c and 124c to have similar characteristics to the lines illustrating the recharge of lines DL_1 and $\overline{DL_1}$.

It should be noted that since the digit lines DL_1 and $\overline{DL_1}$ start at V_{DD} rather than V_{DD} less one threshold, and since the resistive means minimizes the conduction through one of the cross coupled transistors, the digit line that started at the higher initial voltage normally finishes with the voltage above V_{DD} less one threshold. After completion of a cycle, as cell that started with a voltage level just above the minimum level for a logic "1" finishes with a voltage of V_{DD} less one threshold. Conversely, a cell that started with a voltage level just below the maximum level for a logic "0" finishes with a voltage of ground. Thus the act of reading a cell followed by pulling the latch clock signals to ground refreshes poor logic levels stored in the cell to the optimum logic levels.

Reference is made to our U.K. Patent No. 1525810 and to our copending application nos 52563/76; (Serial No. 1,566,408) 31200/78 (Serial No. 1,567,148) and 32332/78 (Serial No. 1,567,149).

WHAT WE CLAIM IS:—

1. A sense amplifier for discriminating between two voltage levels, comprising:

first and second input nodes for receiving the two voltage levels;

third, fourth and fifth nodes;

a first transistor connecting the third node to the fifth node;

a second transistor connecting the fourth node to the fifth node;

a third transistor connecting the first input node to the third node;

a fourth transistor connecting the second input node to the fourth node;

the voltage on the gate of the first transistor being responsive to the voltage on the fourth node;

the voltage on the gate of the second transistor being responsive to the voltage on the third node; and

first circuit means for holding a precharge voltage on the fifth node while the voltage levels on the first and second input nodes are established on the third and fourth nodes via the third and fourth transistors, and then causing the voltage on the fifth node to be discharged to permit the first or second transistor to discharge the third or fourth node in a predetermined preference determined by the relative voltage levels on the third and fourth nodes, the first circuit means including fifth and sixth transistors providing parallel discharge paths for the fifth node, the sixth transistor having a substantially larger conductance than the fifth transistor such that the fifth node is discharged at a relatively slow rate when the fifth transistor is turned on while the sixth transistor is off and at a relatively fast rate when the sixth transistor is turned on.

2. The sense amplifier of Claim 1 further comprising:

second circuit means for biasing the gate nodes of the third and fourth transistors sufficiently high to substantially equalize the voltage levels on the first and third nodes and to substantially equalize the voltage levels on the second and fourth nodes before the voltage on the fifth node is discharged.

3. The sense amplifier of Claim 2 further comprising:

third circuit means for precharging the first and second input nodes and the third and fourth nodes to substantially the same predetermined voltage level, and the fifth node unit the voltage level on the fifth node is such as to make the first and second transistors substantially nonconductive;

whereby an input signal may be applied by reducing the voltage on at least one of the input nodes after the nodes are precharged.

4. Then sense amplifier of Claim 3 wherein:

the second circuit means comprises means for precharging the gate nodes of the third and fourth transistors and then isolating the gates before the first, second, third and fourth nodes are precharged whereby the gate nodes will be capacitively boosted above the precharge voltage at least partially by the stray capacitance of the third and fourth transistors as the first, second, third and fourth nodes are precharged.

5. The sense amplifier of Claim 2 wherein the gate nodes of the third and fourth transistors are electrically common.

6. The sense amplifier of Claim 3 wherein the third circuit means includes

means for at least momentarily interconnecting the first and third nodes with the second and fourth nodes after precharge to equalize the predetermined voltage levels.

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Reference has been directed in pursuance of section 9, subsection (1) of the Patents Act 1949, to patent No. 1,374,215.

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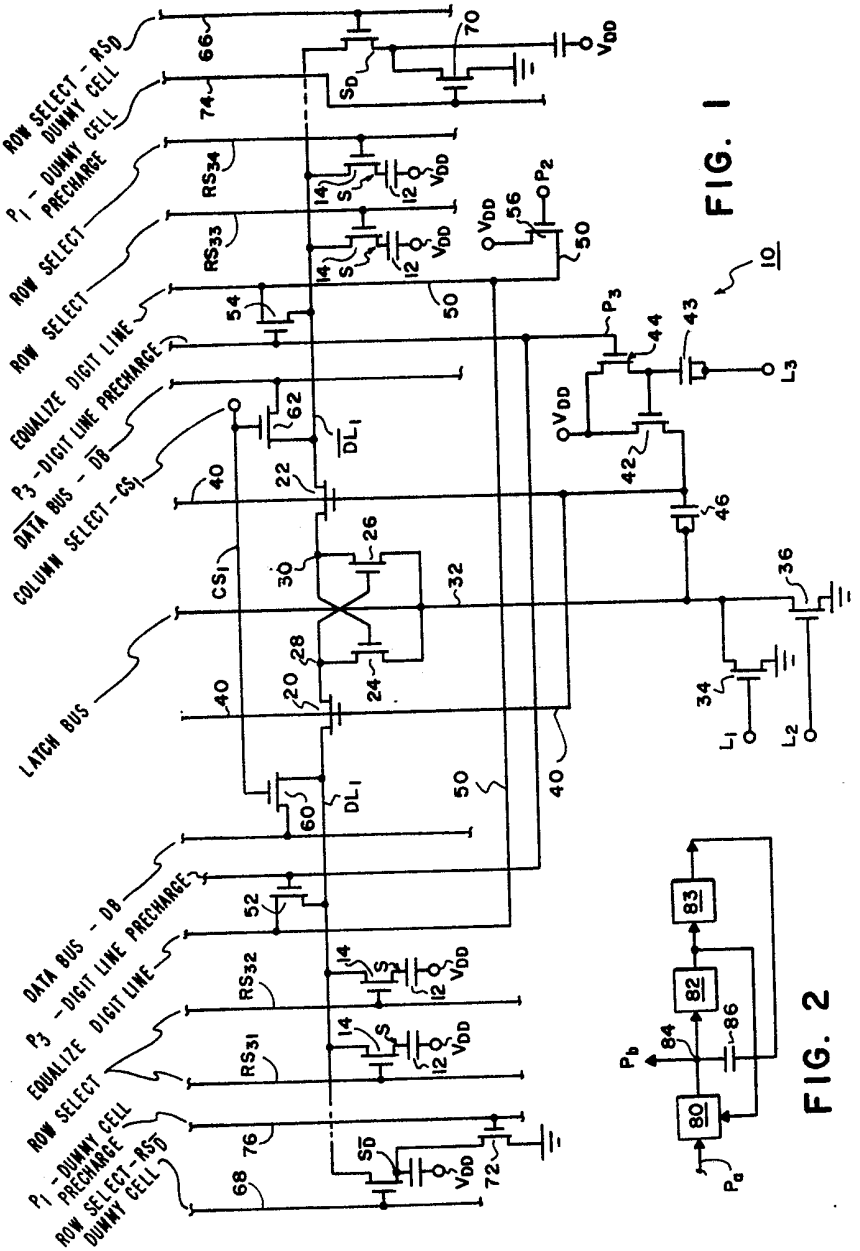
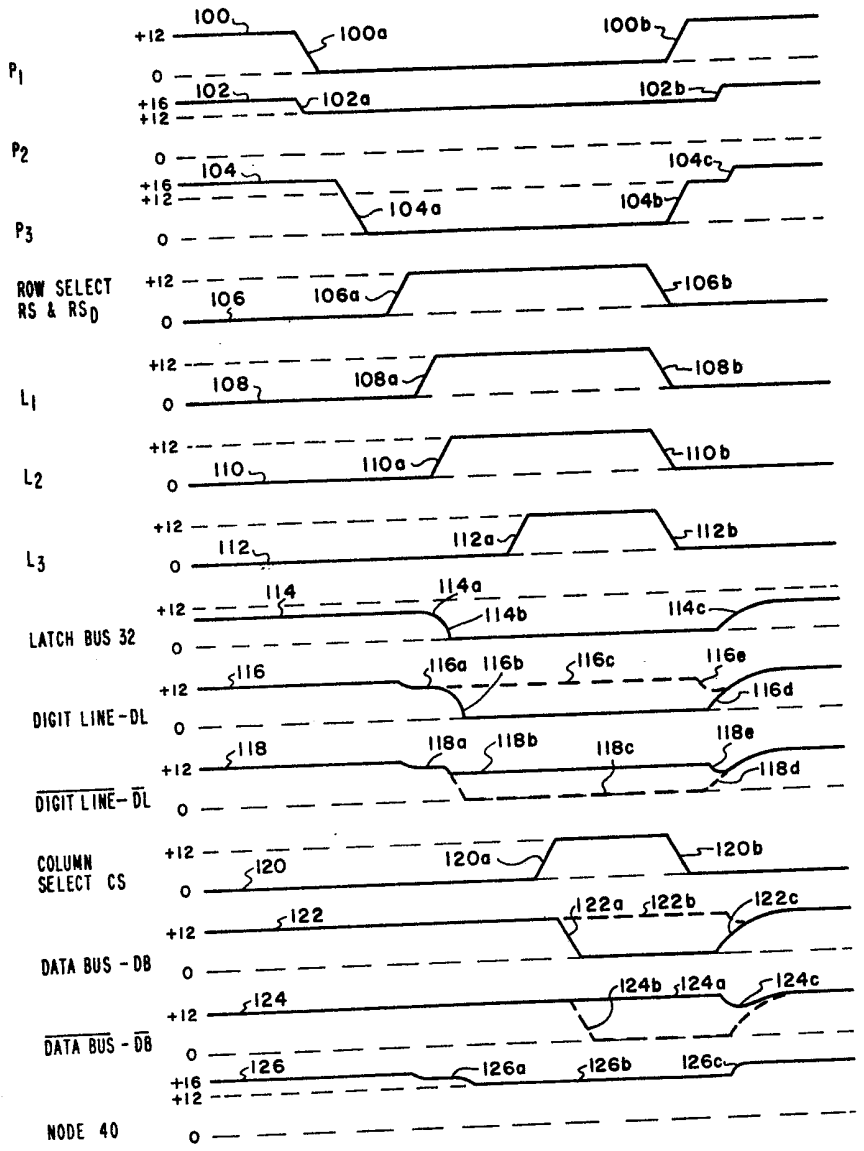

ROW SELECT - RSD
DUMMY CELL
P1 - DUMMY CELL PRECHARGE
ROW SELECT
ROW SELECT
EQUALIZE DIGIT LINE
P3 - DIGIT LINE PRECHARGE
DATA BUS - DB
COLUMN SELECT - CS1
LATCH BUS
DATA BUS - DB
P3 - DIGIT LINE PRECHARGE
EQUALIZE DIGIT LINE
ROW SELECT
P1 - DUMMY CELL PRECHARGE
ROW SELECT - RSD
DUMMY CELL
VDD
P1
P2
P3
L1
L2
L3
DL1
CS1
RS34
RS33
RS32
RS31
SD
10

FIG. 1

83
82
80
86
84
Pb
Pa

FIG. 2


P1
P2
P3
ROW SELECT RS & RSD
L1
L2
L3
LATCH BUS 32
DIGIT LINE-DL
DIGIT LINE-DL
COLUMN SELECT CS
DATA BUS - DB
DATA BUS - DB
NODE 40
+12
0
+16
100
100a
100b
102
102a
102b
104
104a
104b
104c
106
106a
106b
108
108a
108b
110
110a
110b
112
112a
112b
114
114a
114b
114c
116
116a
116b
116c
116d
116e
118
118a
118b
118c
118d
118e
120
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124c
126
126a
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126c

FIG. 3