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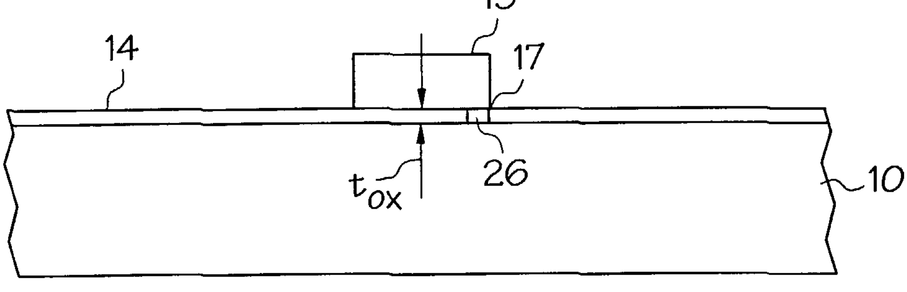

(57) Abstract: A process for the fabrication of an integrated circuit which provides a FET device having reduced GIDL current is described. A semiconductor substrate is provided wherein active regions are separated by an isolation region, and a gate oxide layer is form on the active regions. Gate electrodes are formed upon the gate oxide layer in the active regions. An angled, high dose, ion implant is performed to selectively dope the gate oxide layer beneath an edge of each gate electrode in a gate-drain overlap region, and the fabrication of the integrated circuit is completed.

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METHOD AND DEVICE TO REDUCE GATE-INDUCED DRAIN LEAKAGE (GIDL) CURRENT IN THIN GATE OXIDE MOSFETs

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of reducing Gate Induced Drain Leakage (GIDL) current by selectively increasing electrical gate oxide thickness only in the gate/drain overlap region during the fabrication of integrated circuits.

In the fabrication of integrated circuits, as the sizes of semiconductor devices, such as state-of-the-art Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), are scaled down, performance issues regarding the current driving capabilities of these devices exist. Since the current driving capability is a function of both source resistance and gate oxide thickness, better performance in these devices is achievable through thinner gate oxide and spacer layers. However, it has been observed that as the gate oxide is made thinner, gate-induced drain leakage (GIDL) currents degrade the performance of these devices as the GIDL currents become a larger percentage of the total sub-threshold leakage current. The GIDL currents are due to electrons from the valence band tunneling to the conduction band as a result of excessive band bending in the gate/drain overlap region. As these semiconductor devices scale down, the layer thickness of the gate oxide must continue to be reduced in order to provide for suitable gate control over the sub-threshold region. Also, doping density in the channel and source/drain regions must increase to improve punch through characteristics and increase drives. Unfortunately, it has been observed that by increasing the doping density in the channel and source/drain regions, the surface electric field also increases, resulting in more band bending and hence, even more GIDL current. Thus, difficulties exist in providing a scaled down semiconductor device having a suitable balance between high current driving capability and low GIDL current.

One approach for reducing GIDL currents involves symmetrical oxidation in order to provide a thick gate oxide only in the regions of the gate-source and gate-drain overlap. The thick gate oxide in the gate-drain region reduces GIDL. However, having a thick gate oxide in the gate-source region increases source resistance, which in turn, reduces the current driving capability of the device.

Another approach is disclosed by U.S. Patent 5,684,317 to Hwang, who teaches forming a thick oxide layer only in the gate-drain region in order to reduce GIDL current without increasing source resistance. The material thickness of the oxide layer in the gate-drain region is increased by implanting an oxidation accelerating material, such as chlorine or fluorine, to physically grow a thicker gate oxide layer in that region. Due to the presence of the oxidation accelerating material, the oxide layer in the gate-drain region grows faster than the remaining portions on the substrate. However, having an increased material thickness of the oxide layer in the gate-drain region hampers current drives of the transistor and also cause increased stress in the active area near the overlap region due to volume expansion.

Accordingly, a need exists for a scaled-down semiconductor device having a thinner gate oxide with improved electrical performance which overcomes the disadvantages of the prior art. The semiconductor device and its method of fabrication should be cost effective and manufacturable, should be easily integrated into an existing process flow, and should not significantly increase the cycle time of the process flow.

The present invention provides a method by which field effect transistor (FET) devices are produced having lower gate induced drain leakage (GIDLs) than FET devices with a similarly thick gate oxide layer formed by conventionally known methods. The method of the present invention, as explained hereafter, may be used in the fabrication of all N-channel, P-channel, and CMOS FET devices.

The method of the present invention employs a non-orthogonal ion implant process by which the gate-oxide layer in the gate-drain overlap region of a FET device is selectively doped with fluorine or chlorine ions. The dosage of the ion implant is such that the ion concentration increases the 'electrical' gate oxide thickness near the gate-source/drain corners, thereby lowering the dielectric constant of the gate-oxide layer in the gate-drain overlap region without actual thickness growth to the ion doped gate-oxide layer. Since GIDL is exponentially dependent on the magnitude of the surface electrical field, even a slight reduction in the electrical field results in a dramatic reduction in GIDL. Accordingly, supplementing existing FET fabrication processes with the method of the preset invention, lowers the effective surface electrical field in the overlap region, and thereby minimizes GIDL in FET devices wherein the present invention is practiced.

The method of the present invention may be employed in any FET device which is susceptible to increased GIDLs due to a 'thin' gate oxide layer. The method of the present invention may be practiced upon N-MOSFET devices within integrated circuits including but not limited to Dynamic Random Access Memory (DRAM) integrated circuits, Static Random Access Memory (SRAM) integrated circuits, Erasable Programmable Read-Only Memory (EPROM), and Application Specific Integrated Circuits (ASICs). Also, the method of the present invention has broad applicability and may be practiced upon P-MOSFET and CMOS devices within integrated circuits, as the process is applicable to the fabrication of those devices.

In accordance with one aspect of the present invention, provided is a circuit structure comprising a semiconductor layer; an oxide layer formed on the semiconductor layer; a polysilicon layer formed on the oxide layer; a gate structure formed from the polysilicon layer, the gate structure having a defined leading edge; and an overlap region beneath the gate structure and adjacent the leading edge having a predetermined ion implant concentration, the predetermined implant concentration is sufficient to increase the electrical gate oxide thickness in the overlap region.

In accordance with another aspect of the present invention, provided is a method for fabricating a structure on a semiconductor layer comprising the steps of forming an oxide layer on a semiconductor layer; forming a polysilicon layer on the oxide layer; patterning the polysilicon layer into a gate structure having a defined leading edge, and to expose the oxide layer; and implanting ions into the oxide layer at an overlap region beneath the gate structure and adjacent the defined leading edge to a predetermined ion implant concentration which is sufficient to increase the electrical gate oxide thickness only in the overlap region without thickness growth of the oxide layer, the ions being implanted at a tilt angle non-orthogonal to the plane of the semiconductor layer.

In accordance with still another aspect of the present invention, provided is a method of reducing Gate Induced Drain Leakage (GIDL) current within Field Effect Transistors (FETs) comprising the steps of: forming on a semiconductor substrate a field effect transistor structure comprising a gate oxide layer, a gate electrode on the gate oxide layer and two source/drain regions formed within the semiconductor substrate; annealing the semiconductor substrate; implanting ions into the gate oxide layer beneath the gate electrode and adjacent the drain region, which defines an overlap region, to a predetermined ion implant concentration which is sufficient to increase electrical gate oxide thickness only in the overlap region, the ions being implanted at a tilt angle non-orthogonal to the plane of the semiconductor substrate; and completing the fabrication of the semiconductor substrate.

An object of the present invention is to provide a method of reducing gate induced drain leakage current by selectively increasing the electrical gate oxide thickness only in the gate/drain overlap region during the fabrication of integrated circuits.

Another object of the invention is to provide a manufacturable method for fabricating integrated circuits which will result in reduced gate induced drain leakage.

Other objects, features and advantages will appear more fully in the course of the following discussion.

FIG. 1, schematically illustrates in cross-sectional representation a partially completed FET circuit device formed on a semiconductor substrate by conventional processes of the prior art;

FIGS. 2A through 2C illustrate process steps in fabricating a gate structure in accordance with an aspect of the present invention; and

FIGS. 3A through 3D, schematically illustrate a series of cross-sectional representations which illustrate the progressive stages in completing the fabrication of a FET device in accordance with a process of the present invention.

The same reference numerals refer to the same parts through the various figure embodiments.

FIG. 1 is an illustration of a portion of a partially completed FET device 2, which can be formed by any known conventional method. As an example, and generally speaking, the FET device 2 is manufactured by the known local oxidation of silicon (LOCOS) process where portions of a semiconductor layer or substrate 10, through a lithographic mask, are oxidized to form field isolation regions 12. Field isolation regions 12 define active device regions and provide lateral isolation between adjacent devices also formed by the same mask in and on the surface of the substrate 10. For the sake of clarity, the field isolation regions 12 between devices have been only partially shown. Additionally, the formation of the lithographic mask is done by conventional lithography and etching techniques. It is to be appreciated that substrate 10 may be one or more semiconductor layers or structures, which includes active and operable portions of semiconductor devices, of various dopant concentrations, either dopant polarity, and various crystallographic orientations, but preferably, the present invention is practiced upon a silicon structure having a 100 crystallographic orientation. Further, since the disclosure applies equally well to both N and P surface-channel devices, for brevity we present the case of N-MOSFET devices only. The process is analogous for P-MOSFET. Accordingly, the substrate 10 is p-doped, meaning that the primary carriers of the substrate 10 are "positive" holes. In P-MOSFET devices, the first conductivity type is "negative" due to the n-doped substrate having electrons as the primary carriers.

After forming the isolation regions 12, a dielectric layer or gate oxide layer 14 is formed upon the cleaned active device regions of the substrate 10 by thermal oxidation, as is conventional in the art. Next, a gate electrode 16 comprised of an in-situ doped polysilicon layer 18 is deposited upon the gate oxide layer 14 by a known method such as low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), or physical vapor deposition (PVD). The polysilicon layer 18 is etched, as is conventional in the art, to provide a desired pattern for the gate electrode 16 within the active region of the substrate 10. Although the thickness of the gate oxide layer 14 is preferably about 20Å to about 80Å, because gate oxide thickness (t_{ox}) depends on its technology node, it is believed that the method of the present invention is useful with any technology node where thinner gate oxides layers are required. Additionally, and also dependent on the technology node, for the preferred embodiment of the present invention, the total thickness of the polysilicon layer 18 and the gate electrode 16 patterned from the highly doped polysilicon layer is preferably about 200Å to about 1000Å .

Generally, although not necessary for the practice if the invention, further materials may be deposited to form additional material layers upon the polysilicon layer 18 of the gate electrode 16. The typical material of these layers include metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks), which are used with the purpose to improve the electrical characteristics of the device. In a preferred embodiment, a relatively thin layer of titanium nitride (TiN) is deposited on the polysilicon layer 18 to form a barrier layer 20. The barrier layer 20 is then blanketed with a tungsten (W) layer 22 to complete the formation of the gate electrode 16.

As seen in FIGS. 2A through 2C, which generally illustrate the process steps in fabricating a gate structure in accordance with an aspect of the present invention, the gate oxide layer 14 is grown on the semiconductive substrate 10, preferably a silicon substrate, by thermal oxidation. A polysilicon layer is deposited on the oxide layer 14, and patterned using a photoetching process to form a gate structure 15. The surface of the gate structure 15 which contacts the gate oxide 14 has a leading edge 17. Next, as shown in FIG. 2B, a photoresist layer 23 is provided over the surface of the substrate 10 and patterned to expose a portion of both the oxide layer 14 and the gate structure 15. Implanting with an angled, high dose, low energy, ion implant 24 is conducted with conventional equipment to selectively dope with ions at an overlap region 26 of the oxide layer 14.

As shown in FIG. 2C, the overlap region 26 is beneath the gate structure 15 adjacent its leading edge 17. The ion implant 24 is preferably fluorine, and alternatively, may be chlorine or any other ion that lowers the dielectric constant of the oxide layer 14. In the preferred embodiment, the fluorine ions are implanted at: (1) a tilt angle of from about 5 to about 15 degrees from an axis orthogonal to the plane of the substrate 10, (2) an ion implantation dose of from about 1E13 to about 1E14 atoms per square centimeter, and (3) an ion implantation energy of from about 10 KeV to about 20 KeV. Although, the preferred range to the angle of ion implantation is about 5 degrees to about 15 degrees, it is to be appreciated that the ion implant angle depends on the stack height of the gate structure 15. It is to be appreciated that implanting of the fluorine ion implant 24 is tailored to attain a preferred ion concentration of about 1E18 atoms per cubic centimeter beneath the gate structure 15 at the overlap region 26. Doping the overlap region 26 to this preferred concentration selectively alters (lowers) the dielectric constant of the gate oxide layer 14 near the overlap region.

As shown in FIG. 2C, with the photoresist layer 23 removed, doping to the preferred ion concentration increases the "electrical gate oxide" thickness in the overlap region 26 without physically growing or increasing t_{ox} of the oxide layer 14 as in prior art methods. Accordingly, with the gate structure formed by the present invention, further fabrication of the semiconductive substrate 10 may continue to complete circuit devices.

One such device that can be formed by the processes of the present invention is a field effect transistor. The fabrication of the FET device is shown by FIGS. 3A through 3D which schematically illustrated a series of cross-sectional representations of the progressive stages. FIG. 3A starts with the partially completed FET device 2, formed in accordance with (but not necessarily) the prior art methods discussed in regards to FIG. 1. Prior to conducting ion implanting of the ion implant 24 at the overlap region 26, as previously explained above with regards to FIGS. 2A through 2C, a short reoxidation is performed on the substrate 10. Several methods may be used to reoxidize or anneal the semiconductor substrate 10 including but not limited to thermal methods, Rapid Thermal Processing (RTP) methods, and laser assisted processing methods. For the preferred embodiment of the present invention, the substrate 10 is annealed through a thermal method at a temperature of about 800 to about 900 degrees centigrade for a time period of about 10 to about 15 minutes.

After the above short reoxidation period, ion implanting of the ion implant 24 is conducted with conventional equipment to selectively dope with ions at the overlap region 26 of the gate-oxide layer 14 and the polysilicon layer 18 of the gate electrode 16. As before, the ion implant 24 is preferably fluorine, and alternatively, may be chlorine or any other ion that lowers the dielectric constant of the gate oxide layer 14. Additionally, what is important is that for a typical FET device 2, the preferred implanting of the fluorine ion implant 24 is tailored to attain an ion concentration of about 1E18 atoms per cubic centimeter at the gate-poly/gate-oxide interface beneath gate electrode 16 adjacent the drain region 30b. Doping the gate-drain overlap region 26 to this preferred concentration selectively alters (lowers) the dielectric constant of the gate oxide layer 14 near the overlap region 26, and thus increases the "electrical gate oxide" thickness in the overlap region 26 without physically growing a thicker gate oxide layer 24 as in prior art methods.

As illustrated in FIGS. 3B through 3D, the remainder of the fabrication steps continue in any conventional manner after the above described ion implantation step of FIG. 3A to complete the FET device 2. As shown by FIG. 3B, further provided on the FET device 2, adjacent both sides of the gate electrode 16 and extending to the field isolation regions 12, are impurity diffusion regions consisting of a source region 28a and drain region 28b. The edges of source/drain regions 28a and 28b adjacent the gate electrode 16 define a channel region 29 at the surface of the substrate 10. The source/drain regions 28a and 28b are typically formed in a two-stage implantation process with an impurity dopant material to form a lightly doped drain (LDD) and then a heavily doped drain(HDD). If the impurity dopant material used for forming the source/drain regions 28a and 28b is n-type, where electrons are used in the source/drain regions as the primary carriers, then the resulting MOSFET is an N-MOSFET ("n-channel") transistor device. For example, arsenic or phosphorus at a dose of between about 2E15 to about 5E15 atoms per square centimeter and with an energy of between about 5KeV to about 15KeV may be used to produce the n-channel doped drain 28a and 28b. Conversely, if the source/drain dopant material is p-type, where holes in the source and drain regions are used as the primary carriers, then the resulting MOSFET is a P-MOSFET ("p-channel") transistor device. For example, boron di-flouride at a dose of between about 2E15 to about 5E15 atoms per squared centimeter and with an energy of between about 10KeV to about 25 KeV may be used to produce the p-channel doped drain 28a and 28b. If FET device 2 is formed with a combination of n-channel and p-channel transistors on the same substrate 10, then the resulting MOSFET is a complementary FET (CMOS), and may comprise of a plurality of N-MOSFETs and a plurality of complimentary P-MOSFETs on the same substrate 10.

In forming the source/drain regions 28a and 28b, a first ion implantation is made using the gate electrode 16 and the field isolation regions 12 to mask the substrate, in order to form the more lightly doped portions of LDD source/drain regions 30a and 30b. Generally, although not necessary for the practice if the invention, as shown by FIG. 3C, provided on both sides of the gate electrode 16 are electrode spacers 32. The electrode spacers 32 may be formed from materials including but not limited to insulating materials such as silicon oxides, silicon nitrides and silicon oxynitrides. Various processes are used to form electrode spacers 32. Such processes include Reactive Ion Etch (RIE), and the above mentioned material deposition methods. Typically, electrode spacers 32 are formed by depositing an oxide film, such as tetraethoxysilane (TEOS) oxide at between about 600 to about 720 degrees centigrade to a thickness of between about 300 Å to about 700 Å. A second ion implantation is performed to complete the source/drain regions 28a and 28b with HDD source/drain regions 34a and 34b. In the illustrated FET device 2, the source/drain regions 20 may be doped with any n-type or p-type dopant or combinations of different n-type dopants or p-type dopants might be used to achieve different diffusion profiles. Further, it is to be appreciated that the angled ion implantation step of the present invention, if desired, could be carried out at this stage in the fabrication of the FET device

2, as there are no apparent advantages or disadvantage in performing this step before or after the formation of either the LDD, the spacers, or even the HDD.

Subsequent to forming the source/drain regions 28a and 28b into substrate 10, substrate 10 is once again annealed to recrystallize the source/drain regions 24a and 24b. As before, the annealing of the source/drain regions 28a and 28b may also be accomplished through thermal methods, Rapid Thermal Processing (RTP) methods, and laser assisted methods. For the preferred embodiment of the present invention, the semiconductor substrate is annealed RTP at a temperature of about 800 to about 1000 degrees centigrade and a time period of about 10 seconds to about 20 seconds to form the recrystallized source/drain regions 28a and 28b.

Referring now to FIG. 3D, there is shown a cross-sectional schematic diagram illustrating the last series of process steps in forming a FET in accord with the preferred embodiment of the present invention. Shown in FIG. 3D are patterned interlevel dielectric layers 36a, 36b and 36c. Patterned interlevel dielectric layers 36a, 36b and 36c are formed by patterning through photolithographic and etching methods as are known in the art of a blanket interlevel dielectric layer formed upon the substrate 10. Blanket interlevel dielectric layers may be formed from insulating materials including but not limited to silicon oxides, silicon nitrides and silicon oxynitrides. These insulating layers may be formed upon semiconductor substrates through methods including but not limited to Chemical Vapor Deposition (CVD) methods, Plasma Enhanced Chemical Vapor Deposition (PECVD) methods and Physical Vapor Deposition (PVD) methods.

For the preferred embodiment of the present invention, the patterned interlevel dielectric layers 36a, 36b and 36c are formed through patterning via photolithographic and etching methods as are known in the art of a blanket interlevel dielectric layer formed from a silicon oxide material deposited upon the substrate 10 through a Chemical Vapor

Deposition (CVD) process employing Tetra Ethyl Ortho Silicate (TEOS) as the source material. Although insulating layers formed through other methods and materials may also be employed, the preferred method and material provide a simple and well known process conventional in the art. The bottoms of the apertures between the patterned interlevel dielectric layers 36a and 36b and the patterned interlevel dielectric layers 36b and 36c are etched through the gate oxide layer 14 to expose surfaces of the source/drain regions 28a and 28b, respectively. Conductive contact studs 38a and 38b, which are formed respectively into the apertures between the patterned interlevel dielectric layers 36a and 36b and the patterned interlevel dielectric layers 36b and 36c, contact the exposed surfaces of the source/drain regions 28a and 28b, respectively. The conductive contact studs 38a and 38b are conventional to the art and may be formed from conductive materials including but not limited to metals, metal alloys and polysilicon deposited upon a semiconductor substrate through methods including, but not limited to, thermal evaporation methods, electron beam assisted evaporation methods, and CVD methods. For the preferred embodiment of the present invention, the conductive contact studs 38a and 38b are preferably formed from a thin titanium nitride barrier layer of thickness from about 200 to about 1000 angstroms upon which is formed a thicker conductive tungsten layer. The tungsten layer is of sufficient thickness to completely fill the apertures within the interlevel dielectric layers 36a, 36b and 36c.

Upon forming the conductive contact studs 38a and 38b within the patterned interlevel dielectric layers 36a, 36b and 36c, there is formed an FET device 2 of the preferred embodiment of the present invention within an integrated circuit, which has a reduced GIDL over conventional FET devices of similar design. It is to be appreciated that the method of the present invention has advantages over prior art methods in that it reduces GIDL currents without compromising other device characteristics like sub-vt and drives. Accordingly, the new electrical flow produced by the application of the method of the present invention allows reduction of gate oxide thickness per scaling rules for deep submicron geometries. Accordingly, the process of the invention can be used in any double (or more) polysilicon process for making such integrated circuit devices as DRAM, SRAM, EPROM, ASIC or the like.

Having thus described the present invention in detail and by reference to preferred embodiments thereof, it will be apparent that modifications and variations are possible without departing from the scope of the invention detailed in the appended claims.

CLAIMS

1. A circuit structure comprising:

a semiconductor layer;

an oxide layer formed on said semiconductor layer; a polysilicon layer formed on said oxide layer;

a gate structure formed from said polysilicon layer, said gate structure having a defined leading edge; and

an overlap region beneath said gate structure and adjacent said leading edge having a predetermined ion implant concentration, said predetermined implant concentration being sufficient to increase the electrical gate oxide thickness in said overlap region.

2. The circuit structure according to claim 1, wherein said predetermined ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

3. A circuit structure comprising:

a semiconductor layer;

a source region and a drain region in said semiconductor layer which are lightly doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

a gate electrode located on said gate oxide layer, the portion of said gate oxide layer which is beneath said gate electrode and adjacent said drain region, and which defines an overlap region, having an ion implant concentration which is effective to lower the surface electrical field in said overlap region.

4. The circuit structure according to claim 3, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

5. The circuit structure according to claim 3, wherein said source region and said drain region are heavily doped with a second conductivity dopant.

6. The circuit structure according to claim 3, further including a pair of spaces adjacent said gate electrode.

7. The circuit structure according to claim 3, wherein said gate electrode is comprised of polysilicon.

8. The circuit structure according to claim 3, wherein said gate electrode is a gate stack.

9. The circuit structure according to claim 3, wherein said gate electrode is comprised of a layer of polysilicon, and one or more additional layers selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks).

10. The circuit structure according to claim 3, wherein said gate electrode is comprised of a layer of polysilicon, a layer of titanium nitride deposited on said polysilicon layer, and a layer of tungsten deposited on said titanium layer.

11. The circuit structure according to claim 3, further including a pair of conductive studs and an interlevel dielectric layer provided on said semiconductive layer, said interlevel

dielectric layer have a pair of throughbores, each accommodating one of each said pair of conductive studs, and one of each said pair of conductive studs contacting one of each said source/drain regions.

12. A circuit structure comprising:

a semiconductor layer;

a first dopant-type MOS transistor is situated on said semiconductor layer having:

a source region and a drain region in said semiconductor layer which are doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

a gate electrode located on said gate oxide layer, the portion of said gate oxide layer which is beneath said gate electrode and adjacent said drain region, and which defines an overlap region, having an ion implant concentration which is effective to lower the surface electrical field in said overlap region; and,

a second-type dopant MOS transistor which is complementary to said first dopant-type MOS transistor, said second-type dopant MOS transistor is situated on said semiconductor layer and includes a second gate oxide layer, two complementary source/drain regions which are doped with a second conductivity-type dopant, and a complementary gate electrode located on said second gate oxide layer.

13. The circuit structure according to claim 12, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

14. The circuit structure according to claim 12, wherein the portion of said second gate oxide layer which is beneath said complimentary gate electrode and adjacent said complimentary drain region, and which defines a second overlap region, having an ion implant concentration which is effective to lower the surface electrical field in said second overlap region.

15. A method for fabricating a structure on a semiconductor layer comprising the steps of:

forming an oxide layer on a semiconductor layer; forming a polysilicon layer on said oxide layer;

patterning said polysilicon layer into a gate structure having a defined leading edge, and to expose said oxide layer; and

implanting ions into said oxide layer at an overlap region beneath said gate structure and adjacent said defined leading edge to a predetermined ion implant concentration, which is sufficient to increase the electrical gate oxide thickness only in said overlap region without thickness growth of said oxide layer, said ions are implanted at a tilt angle non-orthogonal to the plane of said semiconductor layer.

16. A method according to claim 15, wherein said predetermined ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

17. A method according to claim 15, wherein the tilt angle is from about 5 to about 15 degrees from an axis orthogonal to the plane of the semiconductor layer.

18. A method according to claim 15, wherein said ion is selected from the group consisting of fluorine and chlorine.

19. A method according to claim 15, wherein said ion is fluorine and said implanting step is carried out at an ion implantation dose of from about 1E13 to about 1E14 atoms per square centimeter, and an ion implantation energy of from about 10 KeV to about 20 KeV.

20. A method according to claim 15, further including the step of annealing said semiconductor layer at a temperature of about 800 to about 900 degrees centigrade for a time period of about 10 to about 15 minutes.

21. A method according to claim 15, wherein said oxide layer thickness is about 20 to about 80 angstroms.

22. A method according to claim 15, further comprising forming electrode spacers on both sides of said gate structure.

23. A method according to claim 15, wherein said gate structure is comprised of polysilicon.

24. A method according to claim 15, wherein said gate structure is a gate stack.

25. A method according to claim 24, wherein said gate stack is comprised of a layer of polysilicon, and additional layers selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks).

26. A method according to claim 15, wherein said gate structure is a gate electrode comprised of a layer of polysilicon, a layer of titanium nitride deposited on top of said polysilicon layer, and a layer of tungsten deposited on top of said titanium layer.

27. A method according to claim 15, wherein said oxide layer is formed by low pressure chemical vapor deposition to a thickness of between about 20 to about 80 Angstroms.

28. A method according to claim 15, further comprising forming a lightly doped drain source/drain region structure within the semiconductor layer adjoining said gate structure.

29. A method according to claim 28, wherein said lightly doped regions are n-type regions formed by implanting ions, selected from the group consisting of phosphorus and arsenic, with a dosage of between about 2E15 to about 5E15 atoms per centimeter squared at an energy of between about 5 to about 15 KeV.

30. A method according to claim 28, wherein said lightly doped regions are p-type regions formed by implanting boron di-fluoride ions with a dosage of between about 2E15 to about 5E15 atoms per centimeter squared at an energy of between about 10 to about 25 KeV.

31. A method according to claim 15, further comprising forming a heavily doped drain source/drain region structure within the semiconductor layer adjoining the gate structure.

32. A method according to claim 31, wherein said heavily doped regions are n-type regions formed by implanting ions, selected from the group consisting of phosphorus and arsenic, with a dosage of between about 2E15 to about 5E15 atoms per centimeter squared at an energy of between about 5 to about 15 KeV.

33. A method according to claim 31, wherein said heavily doped regions are p-type regions formed by implanting boron di-fluoride ions with a dosage of between about 2E15 to about 5E15 atoms per centimeter squared at an energy of between about 10 to about 25 KeV.

34. A method according to claim 15, further comprising forming electrode spacers on both sides of said gate structure.

35. A method according to claim 34, wherein said electrode spacers have widths of between about 300 to about 700 Angstroms.

36. A method according to claim 15, wherein said step of implanting is performed before said step of forming said polysilicon layer.

37. A method according to claim 15, wherein said step of implanting is performed before said step of patterning said polysilicon layer.

38. A method of reducing Gate Induced Drain Leakage (GIDL) current within Field Effect Transistors (FETs) comprising the steps of:

forming on a semiconductor layer a field effect transistor structure comprising a gate oxide layer, a gate electrode on the gate oxide layer and two source/drain regions formed within said semiconductor layer;

annealing said semiconductor layer;

implanting ions into said gate oxide layer beneath said gate electrode and adjacent said drain region, which defines an overlap region, to a predetermined ion implant concentration which is sufficient to increase electrical gate oxide thickness only in said overlap region, said ions being implanted at a tilt angle non-orthogonal to the plane of the semiconductor layer; and

completing the fabrication of said semiconductor layer.

39. A method according to claim 38, wherein said FET formed on said semiconductor layer is a plurality of a first FET with a first dopant type and said semiconductor layer also includes a plurality of a second FET with a second dopant type, said second FET being complimentary to said first FET.

40. A method according to claim 38, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

41. A method according to claim 38, wherein the tilt angle is from about 5 to about 15 degrees from an axis orthogonal to the plane of the semiconductor layer.

42. A method according to claim 38, wherein said ion is selected from the group consisting of fluorine and chlorine.

43. A method according to claim 38, wherein said ion is fluorine and said implanting step is carried out at an ion implantation dose of from about 1E13 to about 1E14 atoms per square centimeter, and an ion implantation energy of from about 10 KeV to about 20 KeV.

44. A method according to claim 38, wherein said annealing step is at a temperature of about 800 to about 1000 degrees centigrade for a time period of about 10 to about 20 seconds.

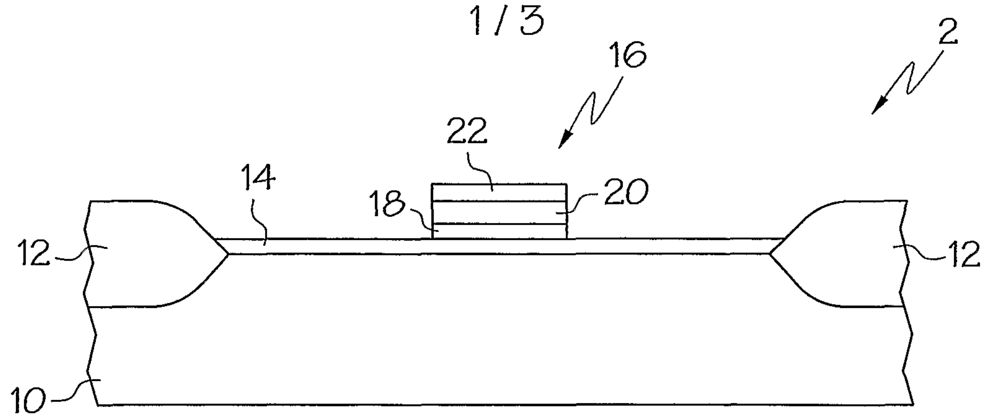

FIG. 1
(PRIOR ART)

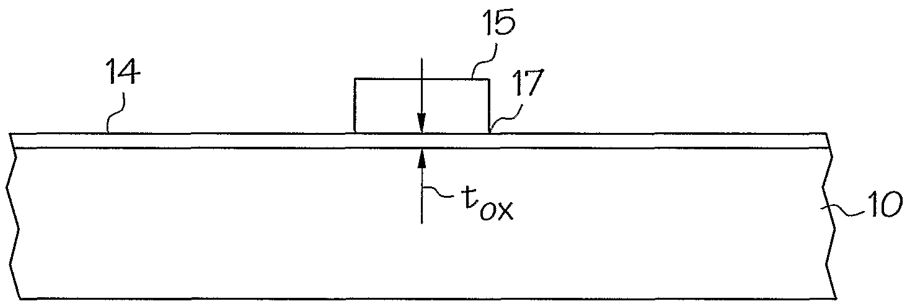

FIG. 2A

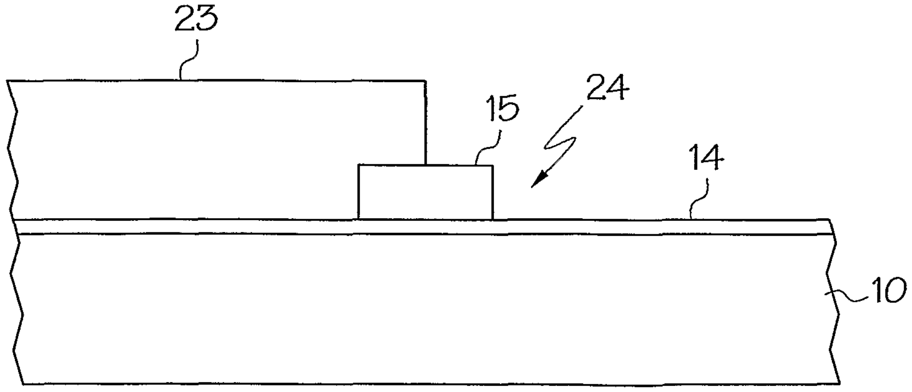

FIG. 2B

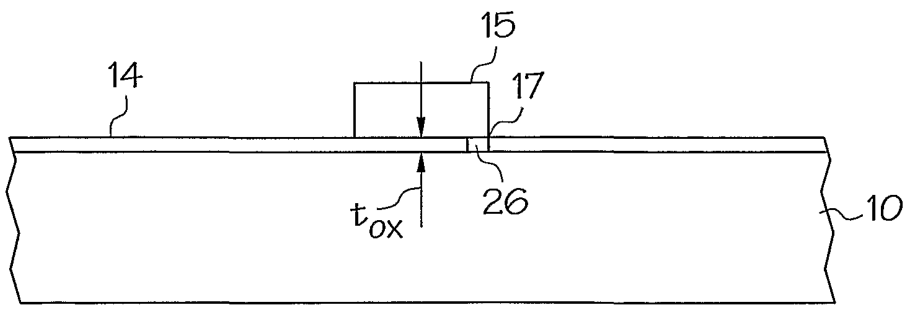

FIG. 2C

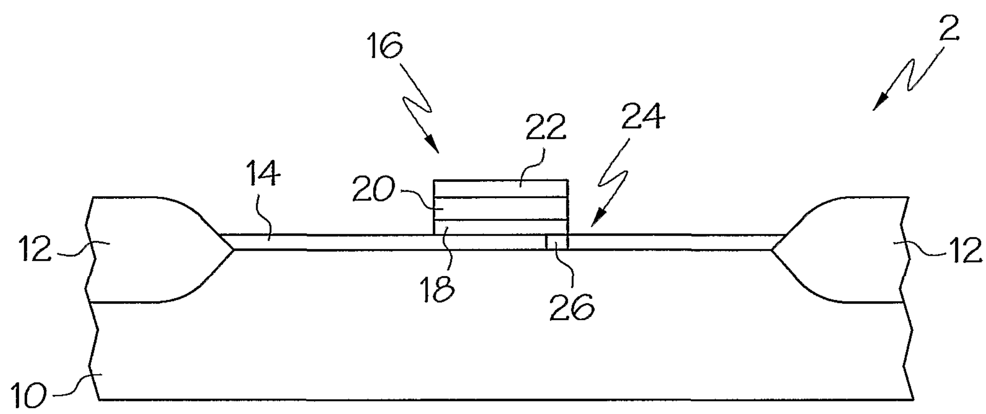

FIG. 3A

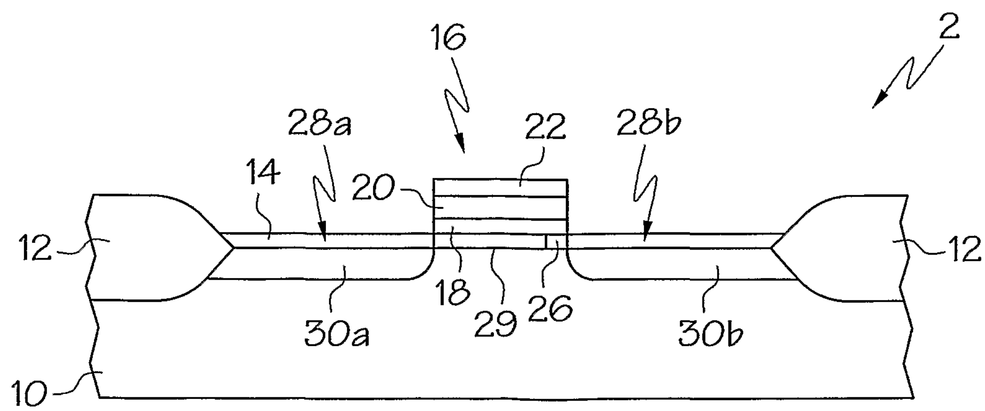

FIG. 3B

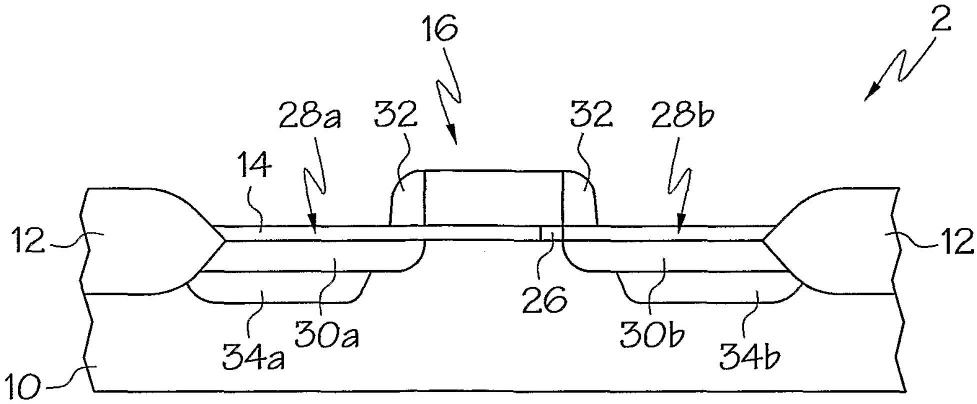
16
2
28a
32
32
28b
14
12
12
26
34a
30a
30b
34b
10

FIG. 3C

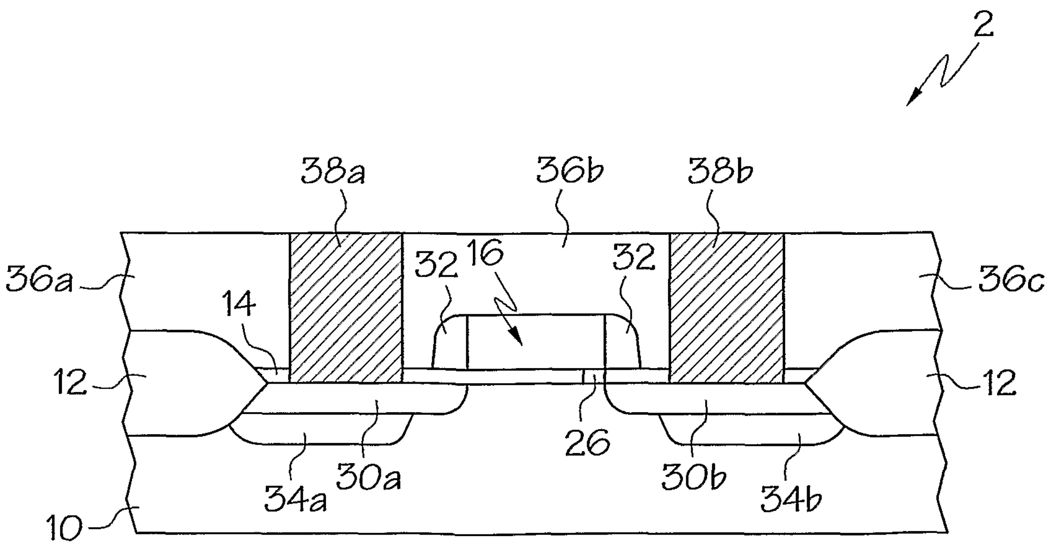
2
38a
36b
38b
36a
32
16
32
36c
14
12
12
26
34a
30a
30b
34b
10

FIG. 3D