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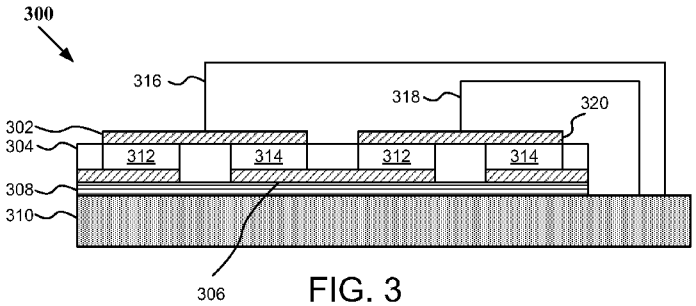

FIG. 3

(57) Abstract: An apparatus, system, and method for a thermoelectric generator. In some embodiments, the thermoelectric generator comprises a first thermoelectric region and a second thermoelectric region, where the second thermoelectric region may be coupled to the first thermoelectric region by a first conductor. In some embodiments, a second conductor may be coupled to the first thermoelectric region and a third conductor may be coupled to the second thermoelectric region. In some embodiments, the first conductor may be in a first plane, the first thermoelectric region and the second thermoelectric region may be in a second plane, and the second conductor and the third conductor may be in a third plane.

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DESCRIPTION

APPARATUS, SYSTEM, AND METHOD FOR ON-CHIP THERMOELECTRICITY GENERATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. provisional application no. 61/367,267 filed July 23, 2010, the entire contents of which is specifically incorporated herein by reference.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0002] This invention relates to thermoelectricity generation and more particularly relates to an apparatus system and method for on-chip thermoelectricity generation.

[0003] In transistor technology, scaling is a continuous trend which ensures increased performance, typically at the cost of higher power dissipation. This dissipation is usually turned into heat, which may be energy that is lost. Thermoelectric generators, or thermogenerators, convert heat to electricity using a phenomenon called the Seebeck effect after Thomas Johann Seebeck.

SUMMARY OF THE INVENTION

[0004] A thermoelectric generator is presented. In some embodiments, the thermoelectric generator comprises a first thermoelectric region and a second thermoelectric region, where the second thermoelectric region may be coupled to the first thermoelectric region by a first conductor. In some embodiments, a second conductor may be coupled to the first thermoelectric region and a third conductor may be coupled to the second thermoelectric region. In some embodiments, the second conductor may be coupled to a first surface of the first thermoelectric region. The first conductor may be coupled to a second surface of the first thermoelectric region. In some embodiments, the first conductor may be coupled to a first surface of the second thermoelectric region. In some embodiments, the third conductor may be coupled to a second surface of the second thermoelectric region.

[0005] In some embodiments, the first, second, or third conductor may be a metal, such as copper. In some embodiments, the first, second or third conductor may be conductive material such as polysilicon.

[0006] In some embodiments, the first or second thermoelectric region may be a semiconductor. In some embodiments, the first or second thermoelectric region may be Bismuth Telluride. In some embodiments, the fist thermoelectric region may be n-doped Bismuth Telluride. In some embodiments, the second thermoelectric region may be p-doped Bismuth Telluride.

[0007] In some embodiments, the first conductor may be in a first plane. In some embodiments, the first thermoelectric region and the second thermoelectric region may be in a second plane. The second plane may be more parallel than perpendicular to first plane. In some embodiments, the second plane may be parallel, or substantially parallel, to the first plane. In some embodiments, the second conductor and the third conductor may be in a third plane, where the third plane is more parallel than perpendicular to the first plane. In some embodiments, the third plane may be parallel, or substantially parallel, to the second plane. In some embodiments, the first plane may be adjacent to the second plane and the second plane may be adjacent to the third plane.

[0008] In some embodiments, the first conductor may be coupled to the first thermoelectric region on a first surface, where the first surface of the thermoelectric region is between the first plane and the second plane. In some embodiments, the second conductor may be coupled to the first thermoelectric region on a second surface of the first thermoelectric region, where the second surface of the thermoelectric region is between the second plane and the third plane.

[0009] In some embodiments, the first conductor may be coupled to the second thermoelectric region on a first surface of the second thermoelectric region, where the first surface of the thermoelectric region is between the first plane and the second plane. In some embodiments, the third conductor may be coupled to the second thermoelectric region on a second surface of the second thermoelectric region, where the second surface of the thermoelectric region is between the second plane and the third plane.

[0010] A method for fabricating a thermoelectric generator is also presented. In some embodiments, the method includes forming a first conductor. In some embodiments, the method

also includes depositing a first thermoelectric region, where the first thermoelectric region may be coupled to the first conductor. In some embodiments, the method may also include depositing a second thermoelectric region, where the second thermoelectric region may be coupled to the first conductor. In some embodiments, the method may also include depositing a second conductor coupled to the first thermoelectric region and depositing a third conductor coupled to the second thermoelectric region.

[0011] In some embodiments, the method may include depositing a first mask layer on a conductor layer. The method may include selectively removing the mask layer. The method may also include etching the conductor from areas where the mask layer was removed.

[0012] In some embodiments, the method may include depositing the first thermoelectric region comprises. The method may also include depositing a second mask layer on the first conductor. In some embodiments, the method may include depositing a third mask layer on the second mask layer and/or selectively removing portions of the third mask layer. The method may also include etching the second mask layer, and depositing a first thermoelectric material.

[0013] In some embodiments, the method may include depositing a fourth mask layer. In some embodiments, the method may include selectively removing portions of the fourth mask layer, etching the second mask layer, and/or depositing a second thermoelectric material.

[0014] In some embodiments the method may include depositing a conductor layer coupled to the first thermoelectric region and the second thermoelectric region, depositing a fifth mask layer, selectively removing the fifth mask layer, and/or etching the conductor layer.

[0015] A semiconductor device is also presented. In some embodiments, the semiconductor device may include an integrated circuit, and/or a first thermoelectric region, a second thermoelectric region, where the second thermoelectric region is coupled to the first thermoelectric region by a first conductor. In some embodiments, the semiconductor device may include a second conductor coupled to the first thermoelectric region, and/or a third conductor coupled to the second thermoelectric region, where the first thermoelectric region and the second thermoelectric region are thermally coupled to the integrated circuit.

[0016] In some embodiments, the first thermoelectric region and the second thermoelectric region may be configured to provide electrical current to the integrated circuit.

[0017] In some embodiments, the first conductor may be in a first plane. The first thermoelectric region and the second thermoelectric region may be in a second plane, where the second plane is more parallel than perpendicular to first plane. In some embodiments, the second plane may be parallel, or substantially parallel, to the fist plane. In some embodiments, the second conductor and the third conductor may be in a third plane, where the third plane is more parallel than perpendicular to the first plane. In some embodiments, the third plane may be parallel, or substantially parallel, to the fist plane. In some embodiments, the integrated circuit may be in a fourth plane, where the fourth plane is more parallel than perpendicular to the first plane. In some embodiments, the fourth plane is parallel, or substantially parallel, to the first plane. In some embodiments, the fourth plane may be adjacent to the first plane. In some embodiments, the fourth plane may not be adjacent to the third plane.

[0018] The term "coupled" is defined as connected, although not necessarily directly, and not necessarily mechanically.

[0019] The terms "a" and "an" are defined as one or more unless this disclosure explicitly requires otherwise.

[0020] The term "substantially" and its variations are defined as being largely but not necessarily wholly what is specified as understood by one of ordinary skill in the art, and in one non-limiting embodiment "substantially" refers to ranges within 10%, preferably within 5%, more preferably within 1%, and most preferably within 0.5% of what is specified.

[0021] The terms "comprise" (and any form of comprise, such as "comprises" and "comprising"), "have" (and any form of have, such as "has" and "having"), "include" (and any form of include, such as "includes" and "including") and "contain" (and any form of contain, such as "contains" and "containing") are open-ended linking verbs. As a result, a method or device that "comprises," "has," "includes" or "contains" one or more steps or elements possesses those one or more steps or elements, but is not limited to possessing only those one or more elements. Likewise, a step of a method or an element of a device that "comprises," "has," "includes" or "contains" one or more features possesses those one or more features, but is not limited to possessing only those one or more features. Furthermore, a device or structure that is configured in a certain way is configured in at least that way, but may also be configured in ways that are not listed.

[0022] Other features and associated advantages will become apparent with reference to the following detailed description of specific embodiments in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The following drawings form part of the present specification and are included to further demonstrate certain aspects of the present invention. The invention may be better understood by reference to one or more of these drawings in combination with the detailed description of specific embodiments presented herein.

[0024] FIGs. 1A-1P are schematic block diagrams illustrating one embodiment of a fabrication flow for making a thermoelectric generator.

[0025] FIG. 2 is a top view of a thermoelectric generator.

[0026] FIG. 3 is a schematic block diagram of a thermoelectric generator coupled to a substrate.

DETAILED DESCRIPTION

[0027] Various features and advantageous details are explained more fully with reference to the nonlimiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. Descriptions of well known starting materials, processing techniques, components, and equipment are omitted so as not to unnecessarily obscure the invention in detail. It should be understood, however, that the detailed description and the specific examples, while indicating embodiments of the invention, are given by way of illustration only, and not by way of limitation. Various substitutions, modifications, additions, and/or rearrangements within the spirit and/or scope of the underlying inventive concept will become apparent to those skilled in the art from this disclosure.

[0028] FIGs. 1A-1P illustrate one embodiment of a fabrication flow for a thermoelectric generator. Referring to FIG. 1A, the flow begins with a substrate 104 that may be in the form of a wafer. In some embodiments, the substrate may be silicon or buried oxide silicon. In some embodiments, the substrate may be gallium nitride. On top of the substrate 104 is a first conductor layer 102. In some embodiments the first conductor layer 102 may be copper or it may

be polysilicon. The first conductor layer 102 may be deposited using chemical vapor deposition (CVD). After the first conductor layer 102 is deposited, the wafer may be primed in hexamethyldisilazane (HMDS) to promote better adhesion of photoresist. A first mask layer 106 is then deposited on the first conductor layer 102, as shown in FIG. 1B. The first mask layer 106 may be a photoresist layer or other material used in photolithography. After the photoresist is deposited, a prebaking process may be performed and the resist may then be exposed and developed.

[0029] FIG. 1C shows additional steps in this flow for making a thermoelectric generator. The first mask layer 106 is etched in some areas. The first mask layer 106 may be etched using a wet etch process. The etching exposes the first conductor layer 102 in some areas.

[0030] As shown in FIG. 1D, the first conductor layer 102 may then be etched to create separate segments of a first conductor 103. Although FIG. 1D only shows the etching in 2 dimensions, the separate segments of the first conductor 103 may have different shapes.

[0031] FIG. 1E shows additional steps in this flow for making a thermoelectric generator. First the first mask layer 106 is removed and the wafer is cleaned. Second a layer of insulator 108 is deposited on the wafer. In some cases the insulator 108 may be silicon nitride (Si_3N_4) and may be deposited using CVD. The layer of insulator 108 may be relatively thick because it creates a well that holds the thermoelectric material. In some cases, a relatively thick layer of thermoelectric material is necessary to efficiently create electrical power.

[0032] FIG. 1F shows how a second mask layer 110 is deposited on the insulator 108. The mask layer 110 is patterned so that the insulator 108 is exposed in areas that are laterally adjacent to the areas of the first conductor layer 102 that have been etched.

[0033] FIG. 1G shows how the insulator 108 has been etched away in regions where the second mask layer was not present. This etch process exposes the insulator 102 in areas not previously exposed. Additionally, FIG. 1G shows how the second mask layer 110 has been removed.

[0034] FIG. 1H shows the first thermoelectric material 112 deposited onto the wafer. In some embodiments, the first thermoelectric material 112 is n-type Bi_2Te_3. The first thermoelectric material 112 fills the well left in the insulator 108. FIG. 1I shows how the first thermoelectric

material 112 creates two regions that are coupled to the first conductor 103 and separated by the insulator layer 108.

[0035] FIG. 1J shows a third mask layer 114 that is deposited onto the first thermoelectric material 112 and the insulator 108. The third mask layer may be a photoresist and is patterned to not cover portions of the insulator 108. The insulator 108 may then be etched to expose the first conductor 103, as shown in FIG. 1K.

[0036] FIG. 1L shows how a second thermoelectric material 116 is deposited onto the third mask layer 114 and the exposed portions of the first conductor 103. The second thermoelectric material 116 may be p-type $(Bi,Sb)_2Te_3$. The second thermoelectric material is coupled to the first conductor, but is isolated from the first thermoelectric material 112 by insulator 108.

[0037] FIG. 1M shows the wafer after the insulator 108 has been reduced to expose the first thermoelectric material 112. In some embodiments, the insulator may be reduced by a chemical mechanical polishing process. After this process, the first thermoelectric material 112 and the second thermoelectric material 116 are exposed on the top side. Additionally, each region of first thermoelectric material 112 is coupled to an adjacent region of second thermoelectric material 116 by the first conductor 103.

[0038] FIG. 1N shows the process of depositing the second conductor layer 118 followed by depositing a fourth mask layer 120. The second conductor layer 118 may be deposited using the same processes as may be used for depositing the first conductor layer 102. The photoresist 120 may then be patterned to expose the second conductor 118 in areas between the first thermoelectric region 112 and the second thermoelectric region 116. The second conductor 118 may then be etched where the fourth mask layer 120 is not present to create the second conductor 122 and the third conductor 124. Finally, the fourth mask layer 120 may be removed, leaving the structure shown in FIG. 1P.

[0039] As seen in FIG. 1P, alternating regions of a first thermoelectric region 112 and second thermoelectric region 116 are coupled by the first conductor 103, the second conductor 122, and the third conductor 124. Although this figure only shows four regions (two of a first thermoelectric region 112 and two of a second thermoelectric region 116), this pattern may be repeated many times, which results in several regions being connected in series.

[0040] The second conductor 122 is coupled to a second surface of the first thermoelectric region 112, which in FIG. 1P is the top surface of the second thermoelectric region 112. The first conductor 103 is coupled to a first surface of the first thermoelectric region 112, which in FIG. 1P is the bottom surface of the second thermoelectric region 112.

[0041] The first conductor 103 is coupled to a first surface of the second thermoelectric region 116, which in FIG. 1P is the bottom surface of the second thermoelectric region 116. The third conductor 124 is coupled to a second surface of the second thermoelectric region 116, which is the top surface of the second thermoelectric region 116.

[0042] The first conductor 103, the second conductor 122, and the third conductor 124 may be made out of metal. In some embodiments, the metal may be copper. Alternatively, the conductors may be made out of polysilicon.

[0043] The first thermoelectric region 112, and the second thermoelectric region 116 may be a semiconductor, and that semiconductor may be Bismuth Telluride. The first thermoelectric region 112 is n-doped Bismuth Telluride, and the second thermoelectric region is p-doped Bismuth Telluride.

[0044] As seen in FIG. 1P, the first conductor 103 is in a first plane. The first thermoelectric regions 112 and the second thermoelectric regions 116 are in a second plane. In this figure, the second plane is adjacent, parallel, and directly above the first plane. In some embodiments, the second plane is more parallel than perpendicular to first plane. The second conductor 122 and the third conductor 124 are in a third plane. In this figure, the third plane is adjacent, parallel, and directly above the second plane. In some embodiments, the third plane is more parallel than perpendicular to the first plane.

[0045] The first conductor 103 is coupled to the first thermoelectric region 112 on a first surface, where the first surface of the first thermoelectric region 112 is between the first plane and the second plane. In FIG. 1P, the first surface of the first thermoelectric region 112 is the bottom of the first thermoelectric region 112, which is between the first plane and the second plane.

[0046] The second conductor 122 is coupled to the first thermoelectric region 112 on a second surface of the first thermoelectric region 112, where the second surface of the thermoelectric region is between the second plane and the third plane.

[0047] The first conductor 103 is coupled to the second thermoelectric region 116 on a first surface of the second thermoelectric region, where the first surface of the thermoelectric region is between the first plane and the second plane.

[0048] The third conductor 124 is coupled to the second thermoelectric region 116 on a second surface of the second thermoelectric region 116, where the second surface of the thermoelectric region 116 is between the second plane and the third plane.

[0049] FIG. 2 shows a top view of one embodiment of a thermoelectric generator 200. As seen in this figure, there are alternating regions of second conductor 122 and third conductor 124, where the conductors are separated by the insulator 108. Although not shown, there is a first thermoelectric region 112 and second thermoelectric region 116 between each section of second conductor 122 and third conductor 124. Therefore, if an appropriate temperature gradient were applied to the thermoelectric generator 200, one could extract electrical energy by attaching electrical leads to the third conductor 124 labeled as 202 and the second conductor 122 labeled as 204. One advantage of this configuration is that several thermoelectric regions 112 and 118 may be connected in series in a convenient package. The package is fabricated on a wafer, which may be compact and may be precisely manufactured. Additionally, a large number of thermoelectric regions may be fabricated to be configured in series, which may simplify the connections. Only two connections may be necessary for the thermoelectric generator, and both connections may be made on the same side of the wafer. By having both connections on the same side of the wafer, the bottom surface may be able to be more accurately coupled to the heat source. In some embodiments, the thermoelectric generator may also be fabricated on a semiconductor wafer that also contains an integrated circuit. In some embodiments, the thermoelectric generator may be fabricated directly on top of an integrated circuit, which may allow for increased thermal coupling and a decrease in overall size.

[0050] FIG. 3 shows one embodiment of a semiconductor device 300 may use a thermoelectric generator to power the device itself. The device includes a substrate 310, which may be an integrated circuit such as a processor. Processors may produce significant amount of heat, which is typically dissipated using a heat sink and/or a fan. As used herein, the heat can be captured, converted to electrical energy and sent back to the processor or some other circuit.

[0051] In some embodiments, the thermoelectric generator is made of a first thermoelectric region 312, a second thermoelectric region 314. In this embodiment, the second thermoelectric region 314 is coupled to the first thermoelectric region 312 by a first conductor 306. A second conductor 320 is coupled to the first thermoelectric region 312, and third conductor 302 is coupled to the second thermoelectric region 314. In this embodiment, the first thermoelectric region 312 and the second thermoelectric region 314 are thermally coupled to the substrate 310. In this embodiment, there is a thermally conductive layer 308 that helps to thermally couple the substrate 310 and the thermoelectric generator. The thermally conductive layer 308 may be thermal grease.

[0052] A fourth conductor 318 connects the second conductor 320 to the substrate 310. A fifth conductor 316 connects the third conductor 302 to the substrate. The fourth and fifth conductors 318 and 316 are able to take the electricity generated by the first and second thermoelectric regions 312 and 314 and divert it to the substrate 310. Although not shown, the fourth and fifth conductors 318 and 316 may terminate in a power control module. The power control module may take the output of the thermoelectric generator and put it into a format that is useful for the substrate 310. For example, if the substrate 310 is a processor, the power control module would convert the power generated by the thermoelectric generator to the appropriate voltage and current necessary for the processor. Additionally, the power control module could combine different power sources to provide power to the substrate 310 as supply and demand for power change. For example, when the processor first starts running, it will be cool and not cause much power to be produced in the thermoelectric generator. Therefore, power for the processor would need to originate from another source. As the chip heats up and the thermoelectric generator begins to produce more power, the power control module could use the power from the thermoelectric generator and reduce the amount it draws from other sources.

[0053] All of the methods disclosed and claimed herein can be made and executed without undue experimentation in light of the present disclosure. While the apparatus and methods of this invention have been described in terms of preferred embodiments, it will be apparent to those of skill in the art that variations may be applied to the methods and in the steps or in the sequence of steps of the method described herein without departing from the concept, spirit and scope of the invention. In addition, modifications may be made to the disclosed apparatus and components may be eliminated or substituted for the components described herein where the same or similar results would be achieved. All such similar substitutes and modifications apparent to those

skilled in the art are deemed to be within the spirit, scope, and concept of the invention as defined by the appended claims.

CLAIMS

1. A thermoelectric generator comprising:
   a first thermoelectric region;
   a second thermoelectric region, where the second thermoelectric region is coupled to the first thermoelectric region by a first conductor;
   a second conductor coupled to the first thermoelectric region; and
   a third conductor coupled to the second thermoelectric region.

2. The thermoelectric generator of claim 1, where the first conductor is coupled to a first surface of the first thermoelectric region.

3. The thermoelectric generator of claim 1, where the second conductor is coupled to a second surface of the first thermoelectric region.

4. The thermoelectric generator of claim 1, where the first conductor is coupled to a first surface of the second thermoelectric region.

5. The thermoelectric generator of claim 1, where the third conductor is coupled to a second surface of the second thermoelectric region.

6. The thermoelectric generator of claim 1, where the first conductor is metal.

7. The thermoelectric generator of claim 6, where the first conductor is copper.

8. The thermoelectric generator of claim 1, where the first conductor is polysilicon.

9. The thermoelectric generator of claim 1, where the second conductor is metal.

10. The thermoelectric generator of claim 9, where the second conductor is copper.

11. The thermoelectric generator of claim 1, where the second conductor is polysilicon.

12. The thermoelectric generator of claim 1, where the third conductor is metal.

13. The thermoelectric generator of claim 12, where the third conductor is copper.

14. The thermoelectric generator of claim 1, where the third conductor is polysilicon.

15. The thermoelectric generator of claim 1, where the first thermoelectric region is a semiconductor.

16. The thermoelectric generator of claim 1, where the second thermoelectric region is a semiconductor.

17. The thermoelectric generator of claim 1, where the first thermoelectric region is Bismuth Telluride.

18. The thermoelectric generator of claim 17, where the first thermoelectric region is n-doped Bismuth Telluride.

19. The thermoelectric generator of claim 1, where the second thermoelectric region is Bismuth Telluride.

20. The thermoelectric generator of claim 19, where the second thermoelectric region is p-doped Bismuth Telluride.

21. The thermoelectric generator of claim 1, where:
the first conductor is in a first plane;
the first thermoelectric region and the second thermoelectric region are in a second plane, where the second plane is more parallel than perpendicular to first plane;
the second conductor and the third conductor are in a third plane, where the third plane is more parallel than perpendicular to the first plane.

22. The thermoelectric generator of claim 21, where the first plane is adjacent to the second plane and the second plane is adjacent to the third plane.

23. The thermoelectric generator of claim 21, where the first conductor is coupled to the first thermoelectric region on a first surface, where the first surface of the thermoelectric region is between the first plane and the second plane.

24. The thermoelectric generator of claim 21, where the second conductor is coupled to the first thermoelectric region on a second surface of the first thermoelectric region, where the second surface of the thermoelectric region is between the second plane and the third plane.

25. The thermoelectric generator of claim 21, where the first conductor is coupled to the second thermoelectric region on a first surface of the second thermoelectric region, where the first surface of the thermoelectric region is between the first plane and the second plane.

26. The thermoelectric generator of claim 21, where the third conductor is coupled to the second thermoelectric region on a second surface of the second thermoelectric region, where the second surface of the thermoelectric region is between the second plane and the third plane.

27. A method for fabricating a thermoelectric generator comprising:
forming a first conductor;
depositing a first thermoelectric region, where the first thermoelectric region is coupled to the first conductor;
depositing a second thermoelectric region, where the second thermoelectric region is coupled to the first conductor;
depositing a second conductor coupled to the first thermoelectric region; and
depositing a third conductor coupled to the second thermoelectric region.

28. The method of claim 27, where forming the first conductor comprises:
depositing a first mask layer on a conductor layer;
selectively removing the mask layer; and
etching the conductor from areas where the mask layer was removed.

29. The method of claim 27, where depositing the first thermoelectric region comprises:
depositing a second mask layer on the first conductor;
depositing a third mask layer on the second mask layer;
selectively removing portions of the third mask layer;

etching the second mask layer; and

depositing a first thermoelectric material.

30. The method of claim 27, where depositing the second thermoelectric region comprises:

depositing a fourth mask layer;

selectively removing portions of the fourth mask layer;

etching the second mask layer; and

depositing a second thermoelectric material.

31. The method of claim 27, where depositing a second conductor coupled to the first thermoelectric region comprises:

depositing a conductor layer coupled to the first thermoelectric region and the second thermoelectric region;

depositing a fifth mask layer;

selectively removing the fifth mask layer; and

etching the conductor layer.

32. A semiconductor device comprising:

an integrated circuit;

a first thermoelectric region;

a second thermoelectric region, where the second thermoelectric region is coupled to the first thermoelectric region by a first conductor;

a second conductor coupled to the first thermoelectric region;

a third conductor coupled to the second thermoelectric region;

where the first thermoelectric region and the second thermoelectric region are thermally coupled to the integrated circuit.

33. The semiconductor device of claim 32, where the first thermoelectric region and the second thermoelectric region are configured to provide electrical current to the integrated circuit.

34. The semiconductor device of claim 32, where:

the first conductor is in a first plane;

the first thermoelectric region and the second thermoelectric region are in a second plane, where the second plane is more parallel than perpendicular to first plane;

the second conductor and the third conductor are in a third plane, where the third plane is more parallel than perpendicular to the first plane; and

the integrated circuit is in a fourth plane, where the fourth plane is more parallel than perpendicular to the first plane.

35. The semiconductor device of claim 34, where the integrated circuit is thermally coupled to the first conductor on the first plane.

36. The semiconductor device of claim 34, where the integrated circuit is thermally coupled to the second conductor on the third plane.

37. The semiconductor device of claim 34, where the fourth plane is adjacent to the first plane.

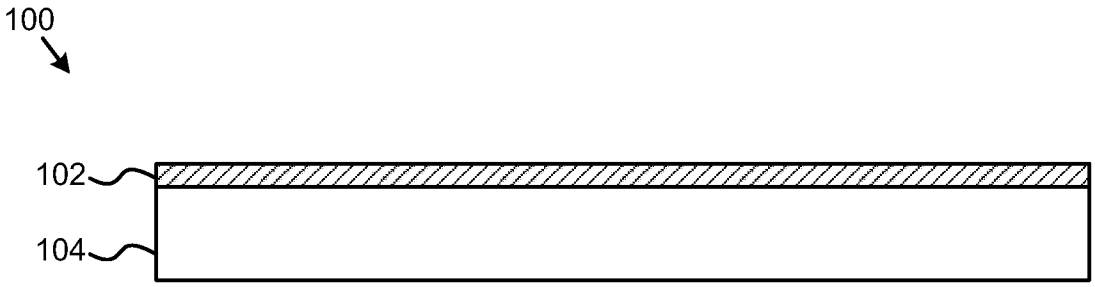

FIG. 1A

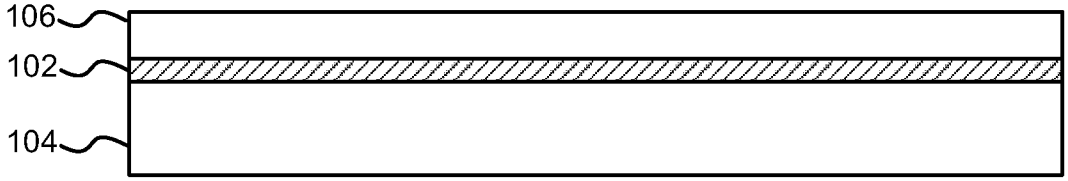

FIG. 1B

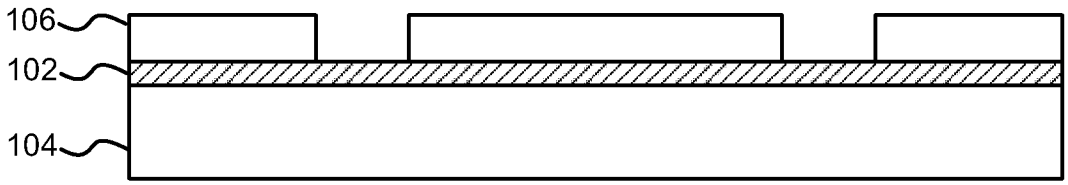

FIG. 1C

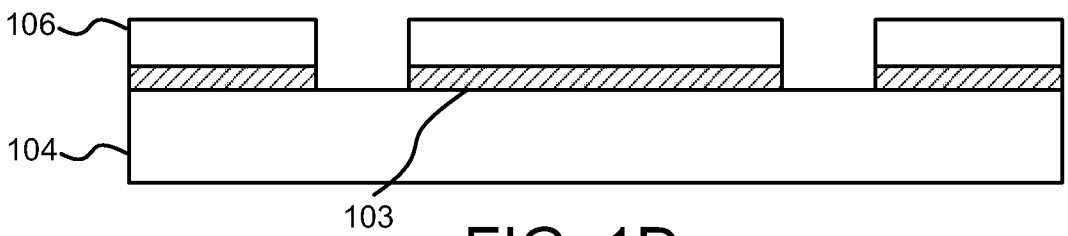

FIG. 1D

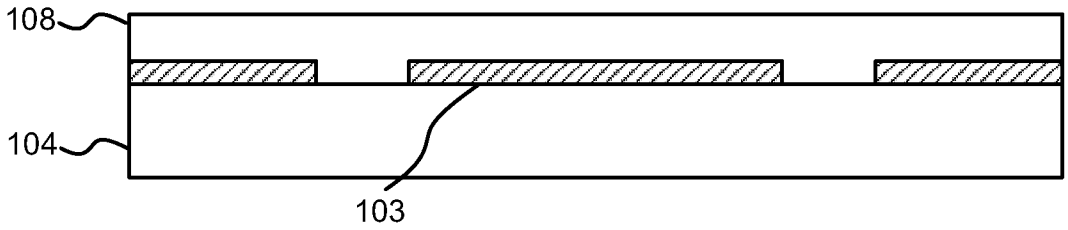

FIG. 1E

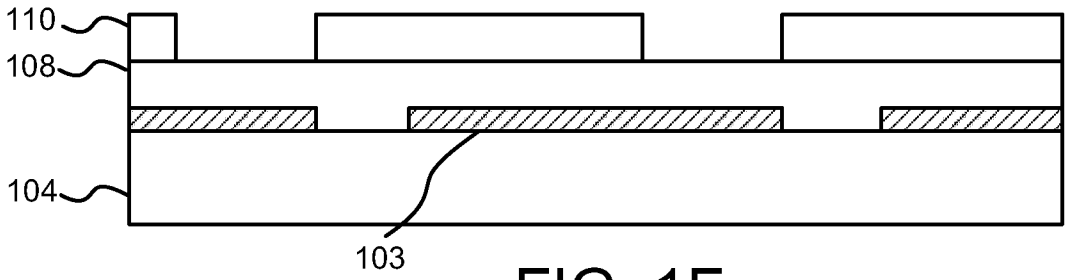

FIG. 1F

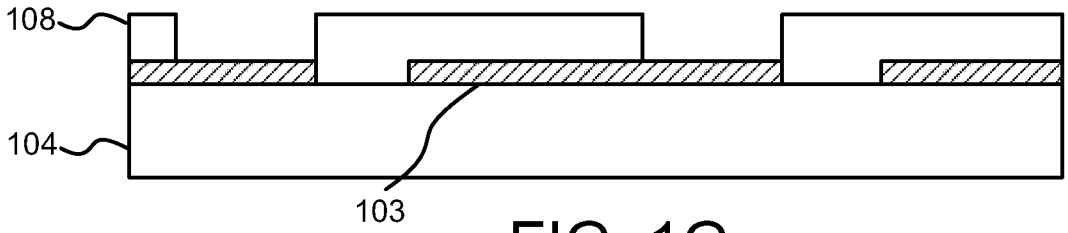

FIG. 1G

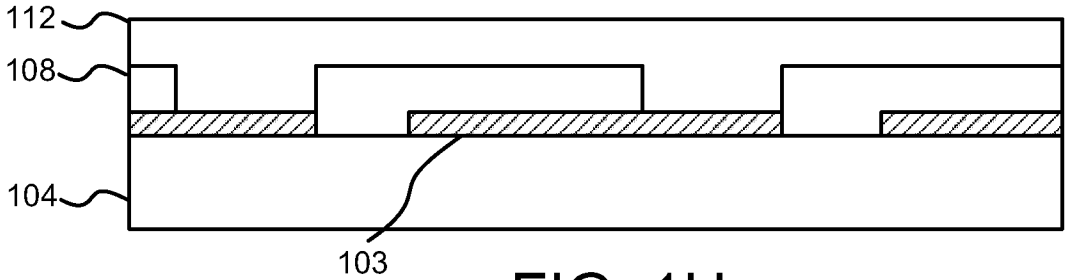

FIG. 1H

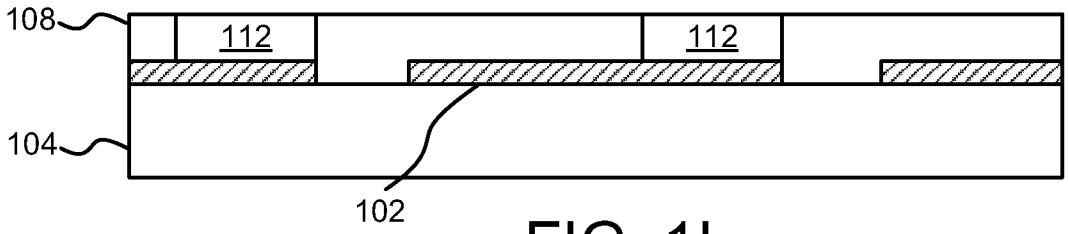

FIG. 1I

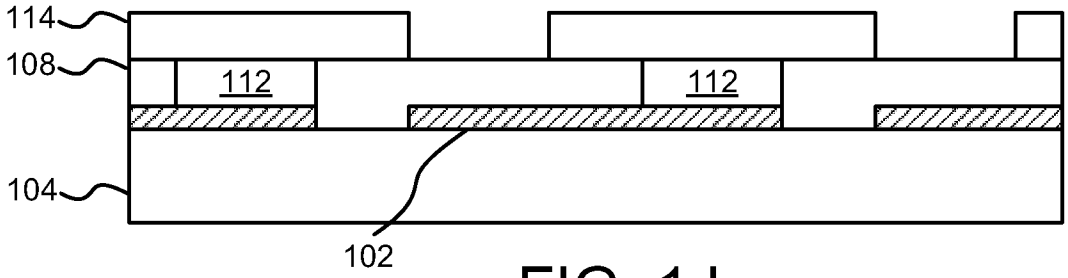

FIG. 1J

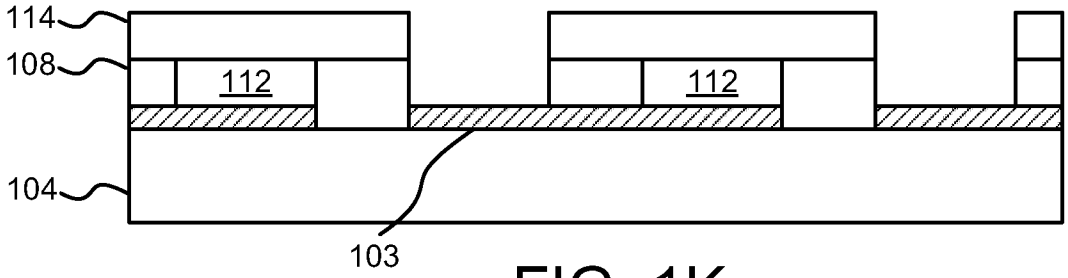

FIG. 1K

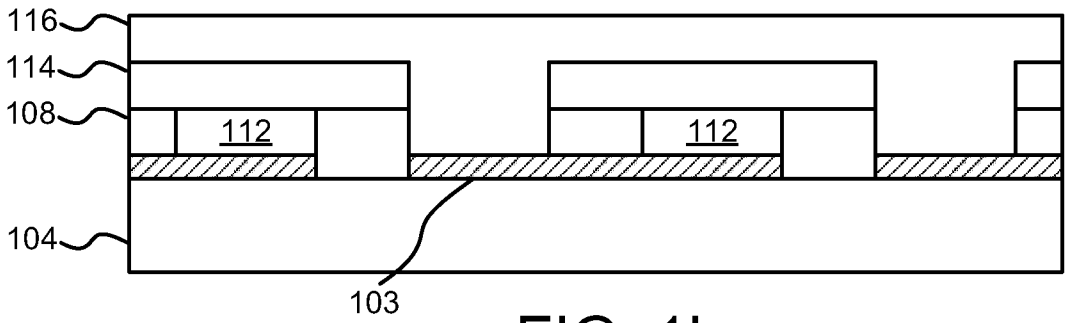

FIG. 1L

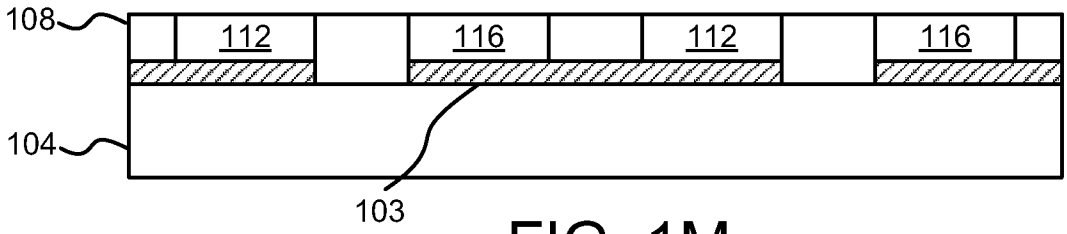

FIG. 1M

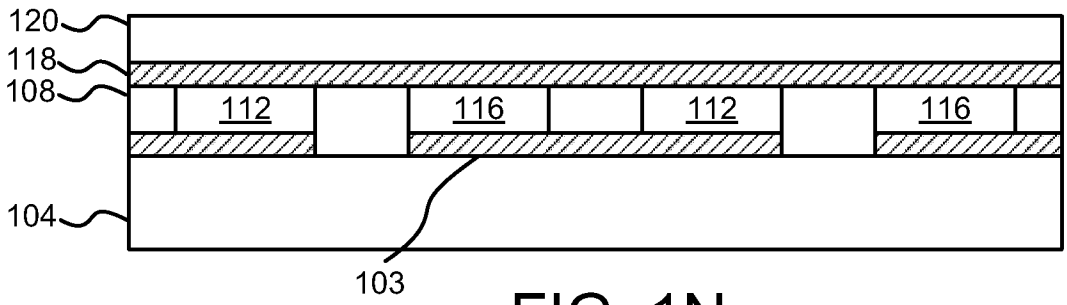

FIG. 1N

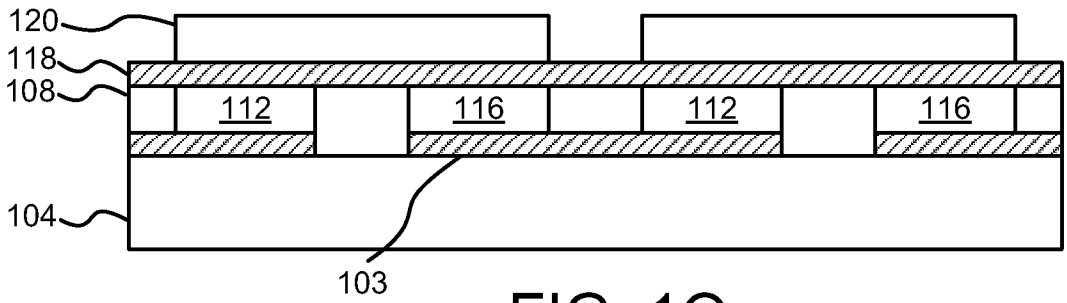

FIG. 1O

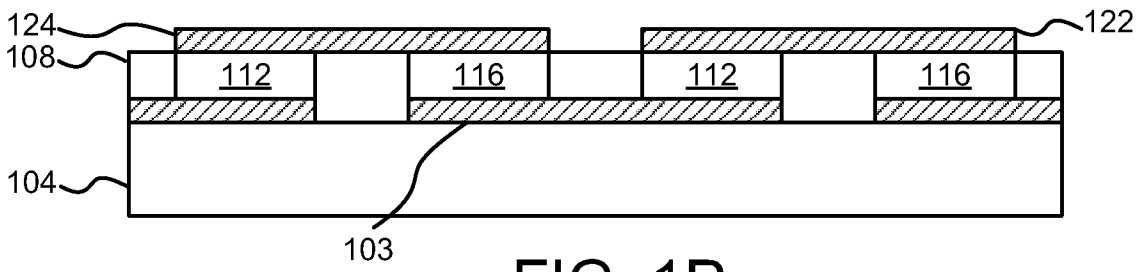

FIG. 1P

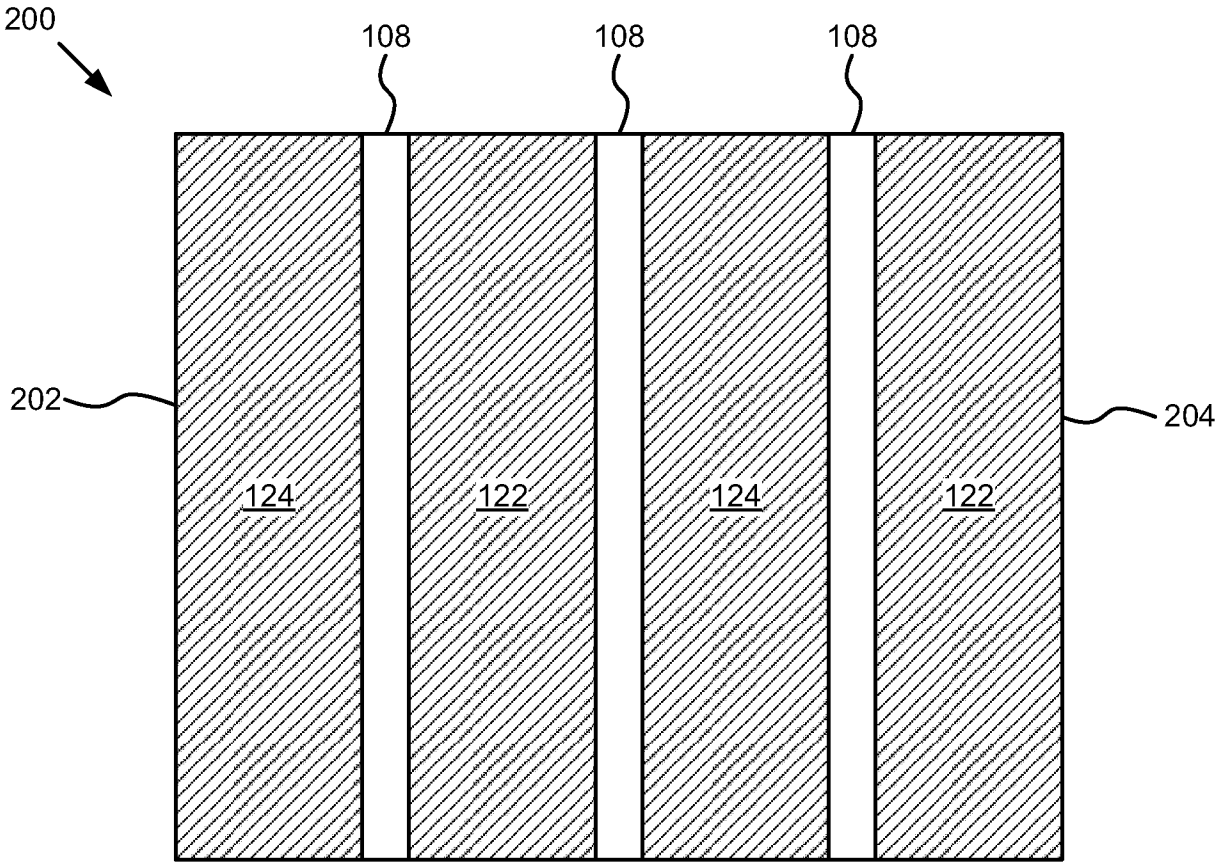

FIG. 2

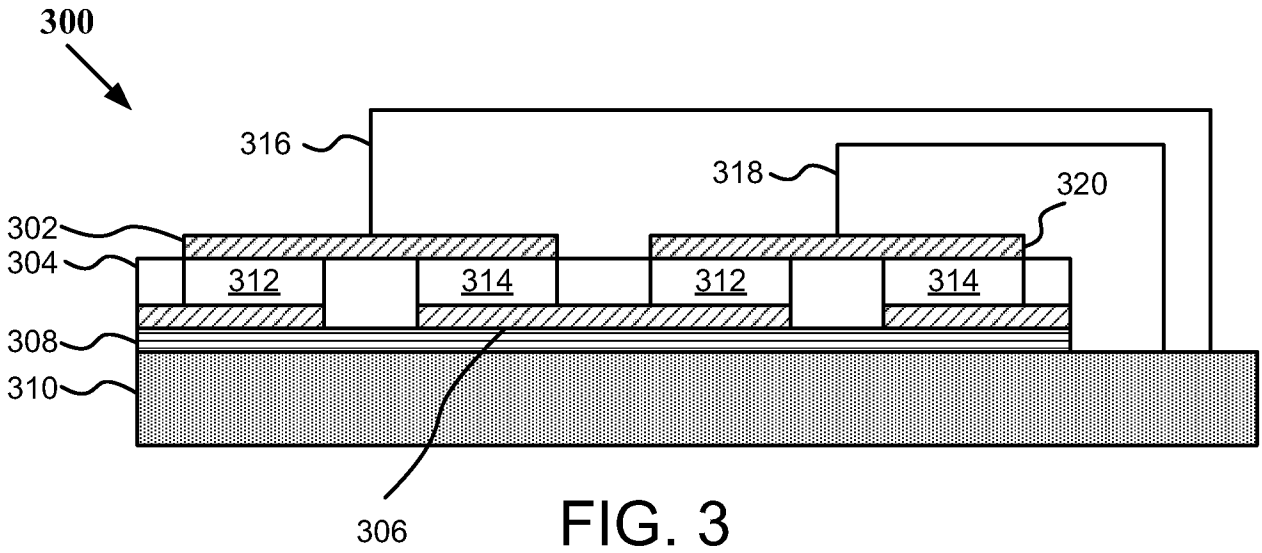

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/044881

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/16 H01L35/32 H01L35/34
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2010/010520 A2 (NXP BV [NL]; KOCHUPURACKAL JINESH BALAKRISHNA PILLAI [NL]; KLOOTWIJK J) 28 January 2010 (2010-01-28) page 3, line 6 - page 6, line 9; figures 1-7	1-37
X	US 2006/137732 A1 (FARAHANI MOHAMMAD M [US] ET AL) 29 June 2006 (2006-06-29)	1-32, 34-37
A	paragraph [0017] - paragraph [0035]; figures 1-10	33
X	US 6 559 538 B1 (POMERENE ANDREW T S [US] ET AL) 6 May 2003 (2003-05-06)	1-32, 34-37
A	column 2, line 8 - column 4, line 39; figures 1-3	33

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 December 2011	09/12/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kirkwood, Jonathan

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/144403 A1 (MORAND JEAN-LUC [FR]) 10 June 2010 (2010-06-10)	1-31
A	paragraph [0021] - paragraph [0031]; figures 1-3 paragraph [0033] - paragraph [0034]; figure 4	32-37

X	STRASSER M ET AL: "Micromachined CMOS thermoelectric generators as on-chip power supply", SENSORS AND ACTUATORS A, ELSEVIER SEQUOIA S.A., LAUSANNE, CH, vol. 114, no. 2-3, 1 September 2004 (2004-09-01), pages 362-370, XP004534498, ISSN: 0924-4247, DOI: 10.1016/J.SNA.2003.11.039 page 367, right-hand column, paragraph 3 - page 369, left-hand column, paragraph 1; figures 1, 8,9	1-16, 21-37

A	EP 1 840 980 A1 (ST MICROELECTRONICS SRL [IT]) 3 October 2007 (2007-10-03) figures 3-24	1-31

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2011/044881

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2010010520 A2	28-01-2010	CN 102099917 A	15-06-2011
		EP 2308091 A2	13-04-2011
		US 2011128727 A1	02-06-2011
		WO 2010010520 A2	28-01-2010
US 2006137732 A1	29-06-2006	CN 101091246 A	19-12-2007
		EP 1834354 A1	19-09-2007
		JP 2008526035 A	17-07-2008
		KR 20070095377 A	28-09-2007
		SG 158173 A1	29-01-2010
		US 2006137732 A1	29-06-2006
		WO 2006072063 A1	06-07-2006
US 6559538 B1	06-05-2003	US 6559538 B1	06-05-2003
		US 2003129783 A1	10-07-2003
US 2010144403 A1	10-06-2010	CN 101681919 A	24-03-2010
		EP 2132777 A1	16-12-2009
		US 2010144403 A1	10-06-2010
		WO 2008142317 A1	27-11-2008
EP 1840980 A1	03-10-2007	NONE	