An apparatus having a display, a receiver and an image controller is disclosed. The display has a plurality of addressable pixels. The receiver receives a signal from the public switched telephone network including an image definition for controlling the pixels and the image controller directly controls the pixels with the image definition received in the signal.
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Method, Apparatus and System for Pixel Control of a Remote Display on a Remote Telephony Device

Cross References to Related Application
This is a continuation-in-part of co-pending patent application number 09/084,197, filed May 26, 1998.

Background on the Invention
1. Field of the Invention
This invention relates to pixel control of a display on a remote telephony device. More particularly, it relates to such control using the public switched telephone network.

2. Description of Related Art
Visual display screens are popular components of modern telephones and other customer premises equipment (CPE). Such screens are used to display important information such as CPE operating instructions or the identity of a calling party, for example.

Conventionally, a CPE receives information encoded in the American Standard Code for Information Interchange (ASCII) format. Using this code a unique number is assigned to each upper and lowercase letter, to the digits 0 through 9, to common symbols such as "&", to common European accented letters such as "É", and to a number of graphics primitives such as "\". When the CPE receives an ASCII code, it retrieves a plurality of pixel control codes from a lookup table, often referred to as a character set, and uses the pixel control codes to control individual pixels on a display to display the corresponding letter, digit or symbol at the CPE.

This simple arrangement has proven quite satisfactory for many users and uses. However, it has significant limitations. Most notably, ASCII codes represent only 256 standard symbols. As a result, only European languages can be encoded and graphic images can be formed only as a
rudimentary combination of ASCII symbols, in particular the graphics primitives.

To overcome the language problem, one might consider programming a CPE to use a code that better represents the language used in a particular telecommunications market. This would require the manufacture of distinct CPEs for each market, which would increase costs and limit such CPEs to use in only one market. Alternatively, additional character sets may be included in a CPE; however, this increases memory requirements which also increases cost.

What would be desirable is a method and apparatus that enables pixel control of a display by a remote device over the public switched telephone network. The present invention is directed to such a method and apparatus.

SUMMARY OF THE INVENTION
The present invention addresses the above need by providing a method and apparatus that enables pixel control of a display on a remote telephony device and particularly provides for such control using the public switched telephone network. This allows a telecommunications provider to download to telephony equipment at a customer’s premises, a graphic image for display on the equipment, independently of any character sets contained within the telephony equipment. It also enables a telecommunications provider to provide advertising or operating instructions, for example, to users in any desired language. In other words, it allows telecommunications providers to provide better service to their customers.

In accordance with one aspect of the invention, there is provided a method including receiving a message including an image definition for controlling pixels on a display, storing the image definition, and directly controlling the display with the image definition.
The message may be received from the public switched telephone network using the Analog Display Services Interface (ADSI) protocol with special data parameters, or other protocols may be used.

Preferably, the message is stored in a message queue at the remote telephony device. In one embodiment the message queue stores a single message and in another embodiment, the message queue stores a plurality of messages. In one embodiment, the image definition is copied directly from the message queue to a display control buffer and individual bits of bytes in the image definition directly control individual corresponding pixels of the display. In another embodiment, the image definition is copied from the message queue to a storage area in the remote telephony device and is selectively copied to the display buffer as needed. For example, an image definition for a logo of the telecommunications services provider may be copied to the display buffer for display while the telephone is not in use. Once copied to the display buffer, individual bits of bytes in the image definition directly control individual corresponding pixels on the display.

In accordance with another aspect of the invention, there is provided an apparatus having a receiver for receiving a message including an image definition for controlling pixels on a display, memory for storing the image definition, and an image controller for directly controlling the display with the image definition.

In accordance with another aspect of the invention, there is provided a system including a stored program computer system and an apparatus as described above for receiving a message from the stored program computer system. The stored program computer system is programmed to produce network transmissible messages including data representing bit-mapped images to be displayed on the display. The stored program computer system includes a public access network
interface for transmitting the network transmissible messages to the apparatus using the public switched telephone network.

5 The stored program computer system may be situated at a central office and the network transmissible messages may be transmitted over the public switched telephone network using any appropriate format. Such format may include an FSK modulation scheme, for example. More particularly, the messages may be sent using the ADSI protocol or an extension thereof.

Other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

20 In drawings which illustrate embodiments of the invention,

Figure 1 is a schematic representation of a system for pixel control of a display on a remote telephony device using the public switched telephone network, according to a first embodiment of the invention;

Figure 2 is a block diagram of a telephony device according to the first embodiment of the invention;

Figure 3 is a schematic representation of an analog display services interface message structure;

Figure 4 is a schematic representation of a message queue buffer maintained by the telephony device of Figure 2;
Figures 5A and 5B together form a flowchart representing a message handling algorithm run by the telephony device shown in Figure 2;

Figure 6 is a schematic representation of a display buffer maintained by the telephony device in Figure 2;

Figure 7 is a flowchart representing an alternate message handling routine run by the telephony device shown in Figure 2;

Figure 8 is a flowchart of a display routine run by the telephony device shown in Figure 2.

Figure 9 is a schematic representation of a display of the telephony device shown in Figure 2.

**DETAILED DESCRIPTION**

As shown in Figure 1, an embodiment of a system for pixel control of a display on a remote telephony device in accordance with the present invention is designated generally by the reference character 10. The system includes a stored program computer system (SPCS) shown generally at 12, a public switched telephone network 14 and a display telephone shown generally at 16.

The stored program computer system (SPCS) 12 is operable to communicate with a central office or a server (not shown) configured to specifically transmit custom data traffic, which may be FSK modulated analog display services interface (ADSI) messages, through the public switched telephone network to the display telephone 16. Such messages include an image definition for controlling pixels on a display 18 of the display telephone 16. The display telephone 16 is generally remote of the SPCS 12 and thus acts as a remote telephony device.
The display telephone 16 acts to receive messages produced by the SPCS and to store the image definition contained therein and to directly control the display 18 with the image definition.

Alternatively, the telephony device may include a computer capable of receiving messages and controlling a display in accordance with the image definition contained with such messages.

The way in which the telephony device directly controls the display in response to messages is explained beginning with reference to Figure 2, in which the telephony device is shown generally at 16 and includes a processor circuit 22 connected to an input/output (I/O) circuit 24, random access memory (RAM) 26, FLASH memory 28 and read only memory (ROM) 30.

The I/O circuit 24 is connected to a dual tone multi-frequency (DTMF) driver circuit 32, a CPE alerting signal (CAS) detector 34, a Frequency Shift Keying (FSK) receiver 36, a display interface 38, a handset interface 40 and a keyboard interface 42. The I/O circuit 24 includes a DTMF data register 44 which is writable by the processor circuit 22 to control the DTMF driver circuit 32. The DTMF driver circuit 32 is connected to a transmit/receive audio circuit having a first terminal 48 connected to a hookswitch 50 which is further connected to a telephone line or central office line 52 having conventional tip and ring terminals 54 and 56 and a telephone line termination network 58. FSK modulated ADSI messages transmitted by the SPCS 12 are received on the central office line 52 by a telephone line interface shown generally at 59 including the telephone line termination network 58, the CPE alerting signal detector 34 and the FSK receiver 36.

The CPE alerting signal detector 34 is connected to the central office line 52 and is operable to render active a
caller alerting signal when such signal is received on the central office line 52. The state of the caller alerting signal is indicated in a CAS register 66 which is readable by the processor circuit 22. Just before the SPCS 12 transmits a message, it transmits a CPE alerting signal to signal the processor circuit 22 that a message is about to be sent.

When the message is sent, it is received at the FSK receiver 36. The FSK receiver 36 is connected to the central office line 52 and is operable to detect frequency shift keyed data thereon and to produce binary data corresponding thereto, which is stored in an FSK data receive register 68 in the I/O circuit 24. The FSK receiver 36 and the FSK data receive register 68 in the I/O circuit 24 therefore form a receiver and act to receive messages including image definitions transmitted by the SPCS 12 on the central office line 52.

As shown in Figures 1 and 3, the stored program computer system 12 cooperates with the public switched telephone network 14 to send ADSI messages of the type shown in Figure 3 to the display telephone 16 using frequency shift keying and coding in a manner similar to that in which calling line identification information is transmitted from the public switched telephone network to a telephone.

As shown in Figures 2 and 4, to facilitate receipt of messages of the type shown in Figure 3, the RAM 26 is partitioned to include a message queue 110, a message queue write pointer register 112, a message queue read pointer register 114, a current message end pointer register 116 and a current parameter end pointer register 118. The RAM is also partitioned to include a display buffer 119, an associated display buffer write pointer register 121 and a display buffer read pointer register 123.
As shown in Figure 3, the messages produced and transmitted by the stored program computer system have a structure designated generally by the reference character 70. If the intended recipient of the message is a Type I or Type II CPE, the message structure includes a message type field 72, a message length field 74 and a plurality of parameter units, one of which is shown at 76. Alternatively, if the intended recipient is a Type III CPE, the message structure further includes a message number field 78.

The message type field 72 is used to hold a code representing the type of message. In this embodiment, a predefined message type code defines the message as a displayable type.

The message length field 74 holds a value indicative of the overall length of the message in bytes, starting with and including the message type field 72 and ending with and including a checksum field (not shown) after the last parameter unit.

Each parameter unit 76 has the same format and includes a parameter type field 80, a parameter length field 82 and a parameter data field 84. The parameter type field 80 is used to hold a predefined code identifying the type of parameter information to follow in the parameter data field 84. In this embodiment, a predefined code is used to identify parameter data which relates to data for controlling the display; in other words, the data is an image definition for controlling pixels on the display. The parameter length field 82 is used to hold a number representing the number of bytes forming the parameter data field 84. The parameter data field 84 is used to hold data, in particular, data representing an image definition for controlling the display 18 on the display telephone 16 shown in Figure 1.
In one scenario, the parameter data field 84 simply holds a plurality of bytes in a predefined sequence which act as the image definition. For example, a first byte 86 may be used to control a first group 88 of eight pixels on the display 18 shown in Figure 1, while a second byte 90 may be used to control a second group 92 of eight pixels on the display 18.

Alternatively, the parameter data field 84 may include a plurality of bytes defining an application code 94, an action code byte 96, a storage location code 98 and a plurality of byte pairs, one of which is shown at 100 in which a display location byte 102 identifies an intended storage address of a pixel data byte 104 for controlling pixels on the display. For example, if the first group of pixels 88 shown in Figure 1 is associated with storage location 1, the byte intended to control this group of pixels would be in a pair in which the associated display location byte is 1. In other words, the display location byte 102 identifies the particular group of pixels on the display which is to be controlled by the associated pixel data byte of the pair. Thus, in this alternate way of defining the image definition in the message from the SPCS, the pairs of bytes represent the image definition.

Alternatively, as shown at 101 in Figure 3, a single display location code field 102 may be provided with a plurality of pixel data byte fields 104 following such that the display location code may be used to define a record into which the pixel data bytes are copies. In this manner, separate images or character sets may be stored in respective records in an image holding area 240 in the FLASH memory 28.

Referring to Figure 4, messages defined using either method are received and stored in the message queue 110 in the RAM. The message queue is essentially a first in first out (FIFO) buffer for receiving messages of the types shown in Figure 3 with successive fields of the message being stored in successive corresponding memory locations. It will be
appreciated that when messages intended for a Type III CPE are to be received, the message queue shown further includes a message number storage location 120. The RAM and message queue implemented therein act to store a message or a plurality of messages and more particularly, to store the image definition contained within the parameter data portion(s) 2 of a message or messages.

To facilitate storage of incoming messages, the message queue write pointer register 112 holds an address identifying a location in the RAM 26 where a next byte of a next received message is to be written, upon receipt of such next byte. The contents of the message queue write pointer register 112 are controlled by a conventional ADSI message receiver routine depicted at 132 in Figure 2 which stores messages in the message queue 110. The ADSI message receiver routine is stored in the ROM 30.

The ADSI message receiver routine 132 is operable to control the processor circuit 22 to receive ADSI messages on the central office line 52 and deposit such messages in the message queue, hence the ADSI message receiver routine increments the message queue write pointer register 112 as messages are received and stored in the message queue buffer shown in Figure 4. Individual bytes of the message are stored in successive locations in the message queue so that the relative positions of respective fields of the message are known and disposed linearly in the address space of the RAM. When a message has been fully received and verified for accuracy, the ADSI message receiver routine 132 presents a software interrupt to the processor circuit 22.

Effectively, the message queue read pointer register 114 is used to hold an address in RAM 26, identifying a current location of the message queue 110 which is to be read. The contents of the current message end pointer register 116 identify the last byte of the message currently being read, and the contents of the current parameter end pointer
register 118 identify the location of the last parameter data field within a given parameter unit of the message.

In order to control the display in response to messages in the message queue, the ROM 30 further includes a message handler routine 134, a display routine 136, a conventional ADSI message handler routine 138, a conventional non-bit-map parameter handler routine 140 and an alternate message handler routine 220. The conventional routines are well understood by those skilled in the art and will not be described here.

The message handler routine is shown generally at 134 in Figures 5A and 5B. Where the message includes parameter data of the type including application codes 94, the alternate message handler routine shown in Figure 7 is run in place of the message handler routine 134.

As shown in Figures 3, 5a, 5b and 7, the message handler routine 134 is initiated upon receipt of a software interrupt from the ADSI message receiver routine, the software interrupt indicating that a new message has been deposited in the message queue. The message handler routine begins with a first block 170 which directs the processor circuit 22 to set the contents of the message queue read pointer register 114 to point to the beginning of the message, in other words, to point to the memory location holding the type field of the message.

Block 172 then directs the processor circuit to compare the contents of the currently addressed message queue location to the contents of a message type code register 150 in the FLASH memory 28 to determine whether or not the message type is a displayable type or whether the contents of the MSG type field are equal to "SDC". If the message is not of the displayable type, and the contents of the MSG type field are not equal to SDC, block 174 directs the processor circuit to
execute the conventional ADSI message handler routine 138 and the message handler routine 134 is ended.

If the message is of the displayable type, block 176 directs the processor circuit to increment the contents of the message queue read pointer register 114. This pointer therefore now points to a location holding the contents of the message length field 74 of the message. Block 178 then directs the processor circuit to calculate a value for the current message end pointer as the sum of the contents of the message queue read pointer register 114 and the contents of the message length field 74, less one, and to store the value so calculated in the current message and pointer register 116. This sets the contents of the current message end pointer register 116 to the address of the checksum field in the message queue 110.

Block 180 then directs the processor circuit to increment the contents of the message queue read pointer to point to the parameter type field 80 of the message. Block 182 then directs the processor circuit to read the contents of the parameter type field 80 and to compare such contents with the contents of a bit-map parameter code field 152 stored in the FLASH memory 28. If such contents are not equal, the processor circuit is directed to block 184 where it is directed to call the non-bit-map parameter handler 140. Upon completion of this routine, the processor circuit is directed back to block 182. It will be appreciated that the non-bit-map parameter handler 140 adjusts the contents of the message queue read pointer register 114 and the contents of the current parameter end pointer register 118 as required, to cause the message queue read pointer register 114 to hold an address of the next parameter type field in the message queue 110 when the non-bit-map parameter handler 140 at block 184 has finished executing.

If at block 182 the parameter type indicates the parameter is a bit-map parameter, block 186 directs the processor
circuit to increment the message queue read pointer register 114 to cause it to point to the parameter length field 82 of the current parameter unit. Block 188 then directs the processor circuit to calculate a new current parameter end pointer register 118 value as the sum of the message queue read pointer register 114 contents and the parameter length field contents less one. Block 190 then directs the processor circuit to increment the message queue read pointer register 114 to point to the first data byte of the parameter data field 84 of the currently addressed parameter unit.

As shown in Figure 5B and Figure 6, block 192 then directs the processor circuit to increment the contents of the display buffer write pointer register 121 shown in Figure 6, to point to the next available location in the display buffer 119.

As shown in Figure 6, the display buffer 119 is a FIFO buffer. The display buffer write pointer register 121 in RAM 26 identifies a location in RAM identifying the next available location in the display buffer 119, and the contents of the display buffer read pointer register 123 identify a location in RAM, the contents of which are to be provided to the display interface 38 for display on the display 18 shown in Figure 1. Basically, the display buffer includes a plurality of memory locations for holding at least one image definition or, more particularly, data for controlling respective groups of pixels on the display.

Referring back to Figure 5B, after incrementing the contents of the display buffer write pointer register, block 194 directs the processor circuit to copy the contents of the currently addressed data byte of the parameter data field 84 into the currently addressed location of the display buffer 119 as indicated by the contents of the display buffer write pointer register 121. Thus, at least a portion of the
message from the message queue is copied into the display buffer.

Block 196 then directs the processor circuit to increment the message queue read pointer register 114 to point to the next data byte and block 198 directs the processor circuit to determine whether or not the message queue read pointer register contents currently point to the end of the parameter data field, i.e., are equal to the contents of the current parameter end pointer register 118. If not, the processor circuit is directed back to block 192 for continued processing. The processor circuit thus stays in a loop including blocks 192-198 until all data bytes of the parameter data field of the message have been copied to the display buffer 119.

When the contents of the message queue read pointer register 114 are equal to the contents of the current parameter end pointer register 118, block 200 directs the processor circuit to copy the contents of the last data byte in the parameter data field to the location identified by the display buffer write pointer register 121.

Block 201 then directs the processor circuit to increment the contents of the message queue read pointer register 114 and block 202 directs the processor circuit to determine whether the current contents of the message queue read pointer register 114 are equal to the contents of the current message end pointer register 116 indicating that the contents of the message queue read pointer register point to the checksum value. If not, then the processor circuit is directed back to block 182 in Figure 5A. If, however, the message queue read pointer register contents point to the checksum field, the entire message has been read and the message handling algorithm is completed.

Alternatively, if at block 172 of Figure 5A, the contents of the message type field are "SDC", block 173 directs the
processor circuit to run the alternate message handler routine depicted generally by the reference character 220 in Figure 7 is run.

5 As shown in Figure 7, the alternate message handler routine begins with a first block 222 which directs the processor circuit 22 to address the message queue 110 shown in Figure 4. Block 224 then directs the processor circuit 22 to determine whether or not the contents of the parameter type field 80 are equal to a pre-defined code, which in this embodiment is 151D. If the contents of this field are not equal to the indicated value, the processor circuit 22 is directed to an alternate parameter handler, not part of this invention.

10 If the above test succeeds, block 226 directs the processor circuit to determine whether or not the application code 94 specified in the data field 84 are equal to "D", "S", "P" and "L", to indicate that the parameter data relate to a display application. If the contents of the application code fields are not equal to these values respectively, the processor circuit is directed to an alternate application code handler, not part of this invention.

15 If the above field contents are equal to the indicated values, block 228 directs the processor to read the action code byte 96 and determine whether or not it is equal to a first value, in this case 01H. If so, then the processor circuit is directed to block 229 which directs it to initialize variables to render it operable to receive further messages. Block 230 then directs the processor to control the DTMF driver circuit 32 shown in Figure 2, to send a DTMF "B" on the central office line to the SPCS 12 shown in Figure 1. The code 01H is thus interpreted as an initialization request.

20 Block 231 directs the processor to determine whether or not the variables have been initialized, i.e., whether or not
the processor is ready to receive data. If the processor is not ready to receive data, block 233 directs the processor to send a DTMF "A" back to the central office. Otherwise, if the processor is ready to receive data, block 232 directs the processor to determine whether or not the action code byte is equal to a second pre-defined code 02H, for example. If so, block 234 directs the processor circuit to download the pixel data bytes 104, for example, into corresponding locations in the display buffer 119 shown in Figure 6, as specified by associated respective display location bytes 102. The processor is then directed by block 230 to send a DTMF "B" back to the SPCS to acknowledge successful loading of the image definition.

If the action code byte is not equal to the second pre-defined code, block 236 directs the processor to determine whether the action code byte is equal to a third pre-defined value, 03H, for example. If so, block 238 directs the processor circuit 22 to download the pixel data byte 104, for example, into corresponding locations in an image holding area 240 in the FLASH memory 28 shown in Figure 2, as specified by associated respective display location bytes 102, for example.

Alternatively, the pixel data byte 104 may be loaded into a particular one of the plurality of records in the image holding area 240. The processor circuit is then directed by block 230 to send a DTMF "B" back to the SPCS to acknowledge successful loading of the image definition.

If the action code byte is not equal to the codes 01, 02, or 03 but is equal to 04, block 237 directs the processor to block 239. Block 239 directs the processor to copy the contents of a predefined one of the pixel data bytes into a record selector register 241 in the FLASH memory. In this instance, the predefined one of the pixel data bytes is used to specify a record in the FLASH memory, which is to be used as a default record for supplying character bitmap or
lookup table. Thus, character bitmaps for English, Chinese and Hindi, may be stored in separate records in the FLASH memory and one of these is selectively set as a default bitmap by the contents of the record selector register 241.

The effect of the message handler routine 134 and the alternate message handler routine 220 is to parse the message queue 110 to copy parameter data associated with a bit-map parameter type image definition to the display buffer 119 or into the image holding area 240 or to load the record selector register 241 with a record selection byte identifying a default record in FLASH memory for use in character display or image display.

The processor circuit 22 cooperates with the display buffer 119 and the display interface 38 to act as an image controller for directly controlling the display with the image definition held in the display buffer 119. To facilitate this, as shown in Figures 2, 6 and 8, the processor runs the display routine designated generally by the reference character 136. The display routine includes a first block 252 which directs the processor circuit 22 to copy a byte from the location identified by the contents of the display buffer read pointer register 123, to the display interface 38. Block 254 then directs the processor circuit to increment the contents of the display buffer read pointer register 123 to point to the next location in the display buffer 119. The processor circuit is then directed back to block 252 to copy the contents of the next location to the display interface 38 and so on.

The display routine 136 serves to successively address each location in the display buffer 119 and copy the contents of such locations to the display interface 38.

The display 18 and display interface 38 are shown in greater detail in Figure 9. The display includes a rectangular array of pixels, eighty pixels in the horizontal direction...
and sixteen pixels in the vertical direction, although a display having any dimensions would work. Each pixel is individually addressable. The display includes an internal display controller 260 having clock, data and synchronization inputs 262, 264 and 266 respectively. The internal display controller 260 includes internal counters and address generators (not shown) for successively addressing individual pixels on the display in response to signals received at the clock input 262 and data input 264.

When the synchronization input 266 is rendered active, the internal counters and address generators reset to point to a first pixel 268. The current state of the data input 264 while the first pixel 268 is being addressed, determines whether or not that pixel appears dark or light. On receiving a falling edge of a clock signal at the clock input 262, the internal address generators and counters cooperate to address a second pixel 270 located vertically downward adjacent the first pixel 268. While the second pixel 270 is being addressed, a signal appearing at the data input 264 determines whether or not the second pixel 270 appears dark or light. As successive falling edges of clock signals are received at the clock input 262, the pixels are successively addressed in a raster scan manner from top to bottom and left to right. Alternatively, they may be scanned left to right and top to bottom, or in any other convenient sequence.

The display interface 38 is implemented from a serial communications port and has a byte-wide data input 272, a clock input 274, a clock output 276, a data output 278 and a synchronization signal output 280.

The clock input 274 receives a conventional clock signal at a relatively high frequency. The display interface 38 reduces the clock frequency to a suitable frequency to ensure that each pixel on the display is addressed at a
sufficiently rapid rate to avoid the appearance of flicker in the display.

The display interface 38 further has a write signal input 282 which is rendered active by the I/O circuit 24 shown in Figure 2, when a byte of data is presented to the byte-wide input 272. The display interface serializes the byte-wide data appearing at the byte-wide data input 272 and presents such data to the data output 278 in a most significant bit first format. Thus, on receiving a first byte at the byte-wide input 272, such byte is used to control the first group of eight pixels 88, disposed vertically downwardly in the first column beginning with the first pixel 268 on the display 18. The next successive byte received at the byte-wide input 272 is used to control the next group of eight consecutive pixels 92 on the display, which are disposed vertically beneath the first group of eight pixels, in this embodiment. In this manner, the individual bits of bytes of the image definition successively received at the byte-wide input 272 control respective corresponding pixels on the display.

As shown in Figure 1, at the stored program computer system 12, successive bytes to be included in parameter data portions of an ADSI message for controlling a display on a remote display telephone 16 are assembled in order to create a desired visual effect on the display. Because each individual bit of each byte is used to control a respective pixel on the display and because the groups of pixels which are controlled by successive bytes are known, the stored program computer system can assemble together successive bytes for creating virtually any image to be displayed on the display. In addition, by assembling and transmitting records of bytes to the remote display telephone, a plurality of character bitmaps or images may be downloaded to the telephone. After having downloaded a record or a plurality of records, various character sets or images are available at the telephone. ADSI message handling routines
within the telephone may be used to download control programs known as ADSI Feature Download Management (FDM) scripts, which could interact with the records to selectively use the contents of the records to produce display images or characters specified by such records. Thus, knowing that certain records are available in a telephone, appropriate scripts can be downloaded to interact with such records to produce desired display images.

It will be appreciated that bit-map generation is performed at the stored program computer system 12 where greater computing power is available to assemble such information. The display telephone 16 serves to present the information received in the messages, on the display.

Because any image can be created at the SPCS 12 and can be communicated to the display telephone 16, there is facilitated the communication of bit-mapped images and the communication of bit-mapped text characters which allows text messages in any language to be displayed on the display telephone 16. This allows display images to be customized to user preferences.

**Alternatives**

In an alternative embodiment, messages similar to those used for conveying calling line identification (CLID) information may be used instead of ADSI messages to convey image definitions to the telephone.

In a further alternative embodiment, the image definition is compressed at the SPCS 12 before transmission to the display telephone 16. Correspondingly, the compressed image definition is decompressed at the display telephone 16 for display on the display 18.

While specific embodiments of the invention have been described and illustrated, such embodiments should be considered illustrative of the invention only and not as
limiting the invention as construed in accordance with the accompanying claims.
What is claimed is:

1. An apparatus comprising:
   a) a display having a plurality of pixels;
   b) a receiver for receiving a signal from the public switched telephone network, the signal including an image definition for controlling said pixels on said display; and
   c) an image controller for directly controlling said pixels with said image definition.

2. An apparatus as claimed in claim 1 wherein said receiver includes a telephone line interface for receiving messages from a telephone line.

3. An apparatus as claimed in claim 2 wherein said receiver includes an FSK receiver.

4. An apparatus as claimed in claim 3 wherein said receiver includes a processor circuit for receiving messages according to an analog display services interface (ADSI) protocol.

5. An apparatus as claimed in claim 2 further including a message queue for receiving a plurality of messages from said receiver.

6. An apparatus as claimed in claim 5 wherein said image controller includes at least one display buffer for storing codes representing said image definition.

7. As apparatus as claimed in claim 6 wherein said image controller is operable to copy at least a portion of a message from said message queue into said at least one display buffer.
8. An apparatus as claimed in claim 6 wherein said image controller addresses individual pixels on said display and controls addressed pixels with data from said at least one display buffer.

9. An apparatus as claimed in claim 6 wherein said image controller addresses individual pixels on said display in a predefined order, and controls addressed pixels with corresponding bits in said at least one display buffer.

10. An apparatus as claimed in claim 9 wherein said at least one display buffer includes a plurality of memory locations for holding data for controlling respective groups of pixels on said display.

11. An apparatus as claimed in claim 10 wherein said image controller communicates the contents of said plurality of memory locations to said display in an order corresponding to an order in which said pixels are addressed by said image controller.

12. A system including the apparatus of claim 1 and further comprising a stored program computer system programmed to produce network transmissible signals including image definitions for receipt by said apparatus, said stored program computer system including a public access network interface for transmitting said network transmissible signals to said apparatus.

13. A method for controlling a pixel-addressable display device, the method comprising:

   a) receiving a signal from the public switched telephone network, said signal defining an image definition for controlling pixels on said display device; and
b) directly controlling said pixels with said image definition.

14. A method as claimed in claim 13 wherein receiving includes receiving messages from a telephone line.

15. A method as claimed in claim 13 wherein receiving includes storing a plurality of messages in a message queue.

16. A method as claimed in claim 13 further including storing codes representing said image definition in at least one display buffer.

17. A method as claimed in claim 13 further including storing codes representing said image definition in at least one holding buffer.

18. A method as claimed in claim 16 further including copying at least a portion of said image definition to said at least one display buffer in response to a received signal.

19. A method as claimed in claim 15 wherein storing includes copying at least a portion of a message from said message queue into at least one display buffer.

20. A method as claimed in claim 13 wherein directly controlling includes addressing individual pixels on said display device in a predefined order, and controlling addressed pixels with said image definition.

21. A method as claimed in claim 13 further including transmitting signals on the public switched telephone network, said signals defining said image definition.
22. A method as claimed in claim 21 wherein transmitting includes transmitting said signals in a multiple data messaging format.

23. A method as claimed in claim 21 wherein transmitting includes transmitting said signals in an ADSI data messaging format.

24. A method of controlling a pixel-addressable display device, the method comprising:
   a) producing a message including an image definition for directly controlling pixels on said display device; and
   b) transmitting a signal, representing said message, on the public switched telephone network.

25. A method as claimed in claim 24 wherein transmitting includes transmitting said signals in a multiple data messaging format.

26. A method as claimed in claim 24 wherein transmitting includes transmitting said signals in an ADSI data messaging format.
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MESSAGE HANDLING ROUTINE

NEW MESSAGE INTERRUPT

SET MESSAGE QUEUE READ POINTER TO BEGINNING OF MESSAGE

MSG TYPE = DISPLAYABLE

Y

INCREMENT MQRP

CMEP = MQRP+1+MSG LEN

INCREMENT MQRP

N

GO TO ALTERNATE MESSAGE HANDLER

SDC

CONF ADSI MSG HANDLER

RETURN

A

B

PARA TYPE = BITMAP

Y

INCREMENT MQRP

CPEP = MQRP+1+PARALEN

INCREMENT MQRP

N

NON-BITMAP PARAMETER HANDLER

FIG. 5A

SUBSTITUTE SHEET (RULE 26)
FIG. 6
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 H04M1/00 H04M3/50 H04M11/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H04M H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<tr>
<td>Y</td>
<td>US 5 524 141 A (BRAUN DAVID A ET AL) 4 June 1996 (1996-06-04) abstract; figures 1,3A column 7, line 50 - column 8, line 51 column 9, line 30 - line 60</td>
<td>6,8-11, 16,18-20</td>
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Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

* Special categories of cited documents:

* A* document defining the general state of the art which is not considered to be of particular relevance
* E* earlier document published on or after the international filing date
* L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
* O* document referring to oral disclosure, use, exhibition or other means
* P* document published prior to the international filing date but later than the priority date claimed

Date of the actual completion of the international search

13 August 1999

Date of mailing of the international search report

26/08/1999

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel: (+31-70) 340-2040, Tx: 31 651 epo nl, Fax: (+31-70) 340-3016

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| P,A      | EP 0 880 271 A (OKI ELECTRIC IND CO LTD)  
abstract; figure 3  
the whole document | 9, 11, 20                |
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