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(71) Applicant (for all designated States except US): **ARM Limited** [—/GB]; 110 Fulbourn Road, Cherry Hinton, Cambridge CB1 9NJ (GB).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **SANDHU, Bal S** [US/US]; 40242 Dolerita Avenue, Fremont, California 94539 (US). **IDGUNJI, Sachin Satish** [IN/US]; 1017 Arlington Ln, San Jose, CA 95129 (US). **FLYNN, David Walter** [GB/GB]; 1 Topcliffe Way, Cambridge Cambridgeshire CB1 8SJ (GB).

(74) Agent: **HORNER, David**; D Young & Co LLP, 120 Holborn, London EC1N 2DY (GB).

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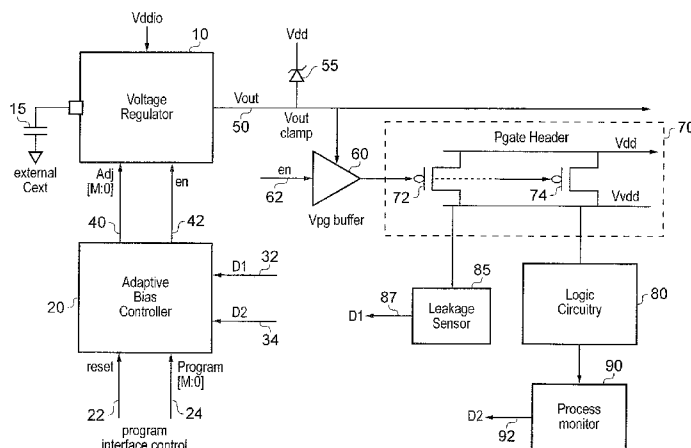


FIG. 1

(57) Abstract: A technique for controlling power gating in an integrated circuit is provided. The integrated circuit comprises a block of components (80) to be power gated, and power gating circuitry (70) for selectively isolating the block of components from the source voltage supply in order to achieve such power gating. Voltage regulator circuitry (10) is used to provide a control voltage (50) to the power gating circuitry when performing such power gating operations, the control voltage being settable to any of a plurality of predetermined voltage levels. An adaptive controller (20) receives operating parameter data (32, 34) from either or both of the block of components and the power gating circuitry, that operating parameter data being indicative of leakage current. The adaptive controller then issues a feedback control signal (40) to the voltage regulator circuitry whose value is dependent on the received operating parameter data. The voltage regulator circuitry is then responsive to the feedback control signal to change the control voltage between the plurality of predetermined voltage levels, until the operating parameter data indicates that a desired leakage current has been obtained within the power gating circuitry.

APPARATUS AND METHOD FOR CONTROLLING POWER GATING IN AN
INTEGRATED CIRCUIT
FIELD OF THE INVENTION

The present invention relates to an apparatus and method for controlling power
5 gating in an integrated circuit.

BACKGROUND OF THE INVENTION

Within an integrated circuit, it is known to employ adaptive power
management or dynamic voltage scaling (DVS) techniques in order to reduce the
power dissipation on a chip. Adaptive power management is becoming ever more
10 important as process geometries decrease. In particular, with leading edge nanometer
technology, the individual components are becoming significantly smaller in size, and
the decrease in size is giving rise to a significant increase in power consumption due to
leakage current, leakage current being the current that is drawn by a component when
it is in theory turned off.

15 As circuits become smaller and smaller due to technology scaling, the supply
voltage to those circuits has to be reduced to reduce dynamic power consumption.
However, a side effect of such scaling is that the threshold voltage and channel length
of the transistors need to be lowered to prevent speed degradation, and this lowering of
the threshold voltage makes the transistors more leaky, i.e. the leakage current
20 increases as the threshold voltage decreases. For example, for each 100mV reduction
in threshold voltage, the sub-threshold leakage current (for a MOSFET transistor this
being the leakage current between the source and drain of the transistor) can increase
by a factor of ten to a hundred.

One common mechanism used in adaptive power management techniques in
25 order to save energy is to shut down blocks of components on a chip when those
blocks of components are not performing any useful function, for example when they
are waiting for instructions from other parts of the system. Such blocks of components
can be shut down using power gating techniques, where power gating circuitry is
placed between a source voltage supply and the block of components, and when it is
30 desired to shut the block of components down, the power gating circuitry isolates the
block of components from the source voltage supply.

However, whilst such power gating techniques have traditionally given rise to
significant energy savings, the ability for such power gating techniques to achieve

significant energy savings is being compromised in integrated circuits based on leading edge nanometer technology, due to the reduced size of the components, and the associated increase in leakage current. For example, power gating circuitry is usually constructed using transistors such as PMOS transistors, and as a transistor's size decreases, its channel length is reduced, and this increases its channel leakage current. Accordingly, it is found that when the transistors in the power gating circuitry are turned off in order to isolate the block of components from the source voltage supply, those transistors are in fact not fully turned off, and significant leakage current through them can occur. This in turn results in the block of components itself not being fully powered down, and accordingly further leakage current being drawn by those components.

One known way to seek to address this problem is to force the power switch transistors of the power gating circuitry into a super cut-off region. For example, considering power gating circuitry formed of PMOS transistors, the voltage on the gate of the PMOS transistors can be driven to a voltage level above the source voltage supply level provided between the source and drain of the transistor. Such a mechanism can significantly reduce leakage current. However, blocks of components may be power gated for significant amounts of time, which means that such power gating transistors are exposed to a gate voltage that exceeds the source voltage supply for significant periods of time. This is undesirable, as such increased gate voltages serve to reduce the operational life (increase "wear out") of the transistors by slowly increasing their threshold voltage. Accordingly, whilst it is desirable to drive the power gating transistors into a super cut-off region in order to reduce leakage current, this has to be balanced against the desired life expectancy for the circuit which is reduced by the driving of such power gating transistors into the super cut-off region.

The article "Gate Bias Circuit for an SCCMOS Power Switch Achieving Maximum Leakage Reduction" by A Valentian et al, IEEE 2007 describes a technique for determining an optimal voltage to be applied to the gate of a power switch transistor in order to maximise leakage gain, dependent on operating conditions. The paper describes a circuit that uses two identical devices configured to measure the sub-threshold current and the gate leakage current. A charge pump is driven to vary the

gate voltage dependent on a comparison between the sub-threshold current and the gate leakage current.

The article "A Super Cut-Off CMOS (SCCMOS) Scheme for 0.5V Supply Voltage with Picoampere Standby Current" by H Kawaguchi et al, IEEE Journal of Solid-State Circuits, Volume 35, No. 10, October 2000, Pages 1498 to 1501, describes a technique for using a four-stage charge pump to overdrive the gate of a low threshold voltage PMOS power gate switch transistor by a voltage that is 400 mV higher than the source voltage supply.

The article "Techniques for Aggressive Supply Voltage Scaling and Efficient Regulation" by A Dancy et al, IEEE 1997 Custom Integrated Circuits Conference, Pages 579 to 586, describes a leakage mitigation technique that uses a triple-well CMOS process to provide substrate voltage control. The logic circuits to be power gated are implemented using low threshold devices and are gated using series connected high threshold switches.

The article "Standby Power Management for a 0.18 μ m Microprocessor" by L Clark et al, ISLPED'02 August 12 to 14, 2002, Monterey, California, USA, Pages 7 to 12, describes a technique to mitigate leakage current using a back-bias scheme.

It would be desirable to provide an improved technique for controlling power gating in an integrated circuit, which enables the leakage current to be controlled whilst also seeking to reduce the impact on wear out of the integrated circuit.

SUMMARY OF THE INVENTION

Viewed from a first aspect, the present invention provides an integrated circuit comprising: a block of components; power gating circuitry configured to receive a source voltage supply, and to provide an internal voltage supply to said block of components, in a normal mode of operation the internal voltage supply being derived from the source voltage supply, and in a power saving mode of operation the power gating circuitry being configured to isolate the internal voltage supply from the source voltage supply; voltage regulator circuitry configured to provide a control voltage to said power gating circuitry during said power saving mode of operation, the control voltage being settable to any of a plurality of predetermined voltage levels; an adaptive controller configured to receive operating parameter data from at least one of the block of components and the power gating circuitry, the operating parameter data being

indicative of leakage current within the power gating circuitry, and the adaptive controller being configured to issue a feedback control signal to the voltage regulator circuitry whose value is dependent on the received operating parameter data; the voltage regulator circuitry being responsive to the feedback control signal to change
5 the control voltage between said plurality of predetermined voltage levels until the operating parameter data indicates a desired leakage current has been obtained within the power gating circuitry.

In accordance with the present invention, voltage regulator circuitry is provided which can set a control voltage applied to the power gating circuitry to any of a
10 plurality of predetermined voltage levels. Based on operating parameter data from either or both of the block of components being power gated and the power gating circuitry, an adaptive controller is configured to issue a feedback control signal to the voltage regulator circuitry. The voltage regulator circuitry changes the control voltage dependent on the feedback control signal until the operating parameter data indicates a
15 desired leakage current has been obtained.

Such an approach provides an adaptive technique for determining the appropriate control voltage to provide to the power gating circuitry, with the aim of reducing the leakage current to an acceptable level, whilst avoiding undue wear out of the power gating circuitry by only providing a control voltage sufficient to achieve the
20 desired leakage current. Through use of such a technique, the control voltage can readily be varied having regard to operating conditions. For example, the higher the operating temperature of the integrated circuit, the greater the leakage current will be. Hence, as the operating temperature increases, the control voltage will need to be varied to seek to bring the leakage current down to an acceptable level. Conversely, if
25 the integrated circuit is running at a low temperature, the leakage current will be less, and may drop below a threshold level that would have been acceptable. In such cases, the control voltage can be changed in order to increase the leakage current, with the aim of reducing wear out of the components within the power gating circuitry.

The power gating circuitry can take a variety of forms. However, in one
30 embodiment, the power gating circuitry comprises at least one PMOS transistor whose gate is driven by the control voltage during said power saving mode of operation, and the control voltage is set to exceed the source voltage supply by an overdrive voltage,

the overdrive voltage being variable so as to enable any of said plurality of predetermined voltage levels to be set as said control voltage.

Hence, in one such embodiment, when the operating parameter data indicates that the leakage current is exceeding the desired leakage current, the adaptive controller is arranged to set the feedback control signal to a value that causes the voltage regulator circuitry to increase the overdrive voltage provided a maximum predetermined voltage level has not been reached. Similarly, when the operating parameter data indicates that the leakage current is below the desired leakage current, the adaptive controller is arranged to set the feedback control signal to a value that causes the voltage regulator circuitry to decrease the overdrive voltage provided a minimum predetermined voltage level has not been reached. By such an approach, it can be seen that the voltage regulator circuitry in combination with the adaptive controller serve to make the leakage current converge on a desired leakage current. Hence, excessive leakage current is prevented by increasing the overdrive voltage, and conversely the overdrive voltage can be reduced in order to reduce wear out of the power gating circuitry when the leakage current is low enough to allow, i.e. where the leakage current is below the desired leakage current. This enables a balance to be achieved between suppressing leakage current and maximising life of the circuitry.

In one embodiment, when the operating parameter data indicates that the leakage current matches the desired leakage current, the adaptive controller is arranged to set the feedback control signal to a value that causes the voltage regulator circuitry to maintain a currently set overdrive voltage. Hence, through adoption of the technique of such embodiments, the circuitry tends to converge on a steady state where a suitable control voltage is arrived at which produces a leakage current matching the desired leakage current.

Whilst the desired leakage current could be specified to be a specific current value, in one embodiment the desired leakage current is specified as a range of leakage current values, thereby enabling the above described convergence to more readily be achieved.

The adaptive controller can take a variety of forms. However, in one embodiment the adaptive controller comprises a state machine that is enabled when said low power mode is entered, the state machine transitioning between a plurality of

states dependent on the received operating parameter data. The use of a state machine to provide the functionalities of the adaptive controller provides a particularly efficient mechanism for achieving the required functionality of the adaptive controller.

In one particular embodiment, following a feedback adjustment state where the value of the feedback control signal is changed, the state machine enters a waiting state where a predetermined event is awaited before the state machine transitions to a monitoring state to monitor the received operating parameter data. This allows a pause to be introduced between each adjustment of the control voltage, to allow the effects of the change in the control voltage to be realised before any further adjustments are made.

The predetermined event which is awaited when the state machine is in the waiting state can take a variety of forms, but in one embodiment the predetermined event is indicative that the control voltage most recently set by the voltage regulator circuitry has reached a steady state. By way of example, the predetermined event may be the elapse of a timer, or may take the form of receipt of a ready signal from the voltage regulator circuitry.

The number of predetermined voltage levels that can be specified for the control voltage can take a variety of forms. However, in one embodiment, the feedback control signal is an M bit value, enabling up to 2^m discrete predetermined voltage levels for the control voltage to be specified. Hence, with a relatively small size of feedback control signal, a relatively large number of discrete predetermined voltage levels may be specified.

In one embodiment, the adaptive controller has an interface via which an initial value of the feedback control signal may be specified. Hence, via such an interface, a microcontroller, or indeed software code, may program an initial value into the adaptive controller, so that on entry to the power saving mode of operation, a corresponding initial voltage level for the control voltage can be used.

The one or more pieces of operating parameter data received by the adaptive controller can be generated in a variety of ways. However, in one embodiment the integrated circuit further comprises one or more monitoring circuits for monitoring said at least one of the block of components and the power gating circuitry in order to produce said operating parameter data.

In one embodiment, such monitoring circuits may comprise a leakage sensor for detecting leakage current in said at least one of the block of components and the power gating circuitry whilst in said low power mode of operation. Alternatively, or in addition, the monitoring circuit may comprise a temperature sensor for monitoring
5 the operating temperature of said at least one of the block of components and the power gating circuitry. As mentioned previously, an increase in temperature will give rise to an increase in leakage current, and hence information about the operating temperature can be used to determine a suitable adjustment to the control voltage.

Alternatively, or in addition, the monitoring circuits may comprise process
10 skew monitoring circuitry for monitoring speed of operation of the block of components during the normal mode of operation. In particular, variations in the silicon on which the integrated circuits are produced will mean that some circuits inherently operate more quickly than other circuits. Process skew monitoring circuitry can determine whether a silicon is fast silicon (i.e. the integrated circuit is operating
15 more quickly than the norm) or slow silicon (i.e. the integrated circuit is operating more slowly than the norm), and this information can be used to determine how to adjust the control voltage. In particular, components constructed on slow silicon have less leakage current than the same components constructed on fast silicon, and hence for an integrated circuit of the slow silicon type, a lower control voltage may be
20 required to achieve the desired level of leakage current. By setting the control voltage to that lower level, the lifetime of the integrated circuit can be increased.

Viewed from a second aspect, the present invention provides a method of controlling power gating in an integrated circuit having a block of components, and power gating circuitry for receiving a source voltage supply and for providing an
25 internal voltage supply to said block of components, in a normal mode of operation the internal voltage supply being derived from the source voltage supply, and in a power saving mode of operation the power gating circuitry being configured to isolate the internal voltage supply from the source voltage supply, the method comprising the steps of: employing a voltage regulator to provide a control voltage to said power
30 gating circuitry during said power saving mode of operation, the control voltage being settable to any of a plurality of predetermined voltage levels; obtaining operating parameter data from at least one of the block of components and the power gating

circuitry, the operating parameter data being indicative of leakage current within the power gating circuitry; issuing a feedback control signal to the voltage regulator whose value is dependent on the received operating parameter data; responsive to the feedback control signal, changing at the voltage regulator the control voltage between
5 said plurality of predetermined voltage levels until the operating parameter data indicates a desired leakage current has been obtained within the power gating circuitry.

Viewed from a third aspect, the present invention provides an integrated circuit comprising: a block of component means; power gating means for receiving a source voltage supply, and for providing an internal voltage supply to said block of
10 component means, in a normal mode of operation the internal voltage supply being derived from the source voltage supply, and in a power saving mode of operation the power gating means for isolating the internal voltage supply from the source voltage supply; voltage regulator means for providing a control voltage to said power gating means during said power saving mode of operation, the control voltage being settable
15 to any of a plurality of predetermined voltage levels; adaptive controller means for receiving operating parameter data from at least one of the block of component means and the power gating means, the operating parameter data being indicative of leakage current within the power gating means, and the adaptive controller means for issuing a feedback control signal to the voltage regulator means whose value is dependent on the
20 received operating parameter data; the voltage regulator means, responsive to the feedback control signal, for changing the control voltage between said plurality of predetermined voltage levels until the operating parameter data indicates a desired leakage current has been obtained within the power gating means.

BRIEF DESCRIPTION OF THE DRAWINGS

25 The present invention will be described further, by way of example only, with reference to embodiments thereof as illustrated in the accompanying drawings, in which:

Figure 1 is a block diagram of an integrated circuit in accordance with a first embodiment;

30 Figure 2 is a diagram illustrating in more detail the operation of the voltage regulator shown in Figure 1 in accordance with one embodiment;

Figure 3 is a finite state machine functional flow diagram illustrating the operation of the adaptive bias controller of Figure 1 in accordance with one embodiment;

Figure 4 is a flow diagram illustrating the operation of the circuitry of Figure 1
5 in accordance with one embodiment; and

Figure 5 is a graph schematically illustrating how the operation of the adaptive bias controller of embodiments serves to bring the leakage current to within an acceptable leakage current range.

DESCRIPTION OF EMBODIMENTS

10 Figure 1 is a block diagram of an integrated circuit in accordance with one embodiment. As shown in Figure 1, an adaptive power controller 20 (referred to in Figure 1 as an adaptive bias controller) is used to control the voltage regulator 10 to produce an output voltage which is used to drive the gates of transistors 72, 74 within a power gate header block 70 when the logic circuitry 80 is being placed in a power
15 saving mode of operation. In particular, in the power saving mode of operation, the voltage regulator 10 produces an output voltage which is transferred by the buffer circuitry 60 to the gates of the transistor 72, 74 in order to turn those transistors off, thereby isolating the logic circuitry 80 from the voltage supply Vdd.

Various monitoring circuits 85, 90 are arranged to output operating parameter
20 data to the adaptive bias controller 20, such operating parameter data being indicative of leakage current within the power gating circuitry 70. This operating parameter data hence provides a feedback mechanism which is used by the adaptive bias controller to vary the control signal sent to the voltage regulator, so as to alter the value of the voltage output over path 50 with the aim of modifying the leakage current until it
25 reaches a desired leakage current. Whilst the desired leakage current can be expressed as a discrete value, it will typically be specified by a range of values.

Considering in more detail the block diagram of Figure 1, it will be seen that the adaptive bias controller 20 has a program interface control input via which the adaptive bias controller can be reset over path 22, and can be programmed over path
30 24. The adaptive bias controller 20 is disabled during system power up by a power on reset signal input over path 22. During this time, the enable signal output by the adaptive bias controller will be disabled, in order to disable operation of the voltage

regulator and to disable the buffer circuitry 60. When the buffer circuitry 60 is disabled, it will provide a logic zero level input to the gates of the various PMOS transistors 72, 74 within the power gating circuitry 70, causing those transistors to turn on, and couple the logic circuitry 80 to the supply voltage Vdd. In particular, in this case, it will be understood that the virtual supply voltage Vvdd is driven to the power supply voltage Vdd by the turning on of the transistor 72, 74.

However, following system power up, whenever it is desired to turn off power to the logic circuitry 80 in order to reduce power consumption of the integrated circuit, the adaptive bias controller 20 is arranged to issue a set enable signal over path 42 to the voltage regulator 10, and over path 62 to the buffer circuitry 60. When the enable signal is set, the voltage regulator 10 is arranged to generate the output voltage Vout over path 50, where the voltage Vout is equal to the supply voltage Vdd plus a variable overdrive voltage Vovr. The magnitude of the overdrive voltage is controlled by a binary value provided by the adaptive bias controller as a multi-bit bus signal over path 40.

When the voltage regulator 10 is first enabled, an initial binary value for the multi-bit bus signal (also referred to herein as the feedback control signal) can be derived from a programmed value input via the program interface controller over path 24. This programmed value may hence be set by a microcontroller or by software code executing on the system. This thus enables the initial value of Vout to be programmable. Whilst this initial programmable value allows some flexibility to choose suitable overdrive voltages for the power gating circuitry, it does not allow the output voltage from the voltage regulator to be tuned having regard to operating characteristics of the integrated circuit which vary during operation of the integrated circuit. Accordingly, as will be discussed in more detail below, a feedback mechanism allowing adaptive control of the overdrive voltage is provided with the aim of maintaining the leakage current within acceptable bounds whilst reducing wear out of the PMOS transistors 72, 74.

In particular, monitoring circuits 85, 90 output operating parameter data D1, D2 over paths 87, 92, respectively, these values being provided as input to the adaptive bias controller 20 over paths 32, 34, respectively. This operating parameter data is indicative of leakage current, and hence enables the adaptive bias controller 20 to vary

the value of the feedback control signal provided over path 40 having regard to the actual observed leakage current. Any changes to the feedback control signal 40 bring about an associated change in the voltage output by the voltage regulator 10 over path 50, which in turn varies the amount by which the power gating transistors 72, 74 are
5 driven into the super cut-off region, this in turn influencing the leakage current.

Various types of monitoring circuit may be provided. In the example shown in Figure 1, a leakage sensor 85 is provided for monitoring the leakage current through the PMOS transistors 72, 74 of the power gating circuitry 70. Whilst the leakage sensor may directly measure leakage current, it may alternatively measure a property
10 which correlates with leakage current, for example temperature. In particular, as the temperature of the integrated circuit rises, this will give rise to an increase in leakage current, and similarly as the temperature drops this will give rise to a decrease in leakage current. However the leakage sensor 85 is constructed, in one embodiment it is arranged to convert the analog signal that it monitors into a digital signal output over
15 path 87.

There are a number of known circuits which could be used to perform this function, but in one embodiment the function is realised with a SAR (successive approximation) data converter. The resolution of the data converter depends on the accuracy desired, but typically a 6-bit SAR data converter circuit would provide a
20 more than adequate level of resolution, in that it would allow up to 64 discrete digital levels to be indicated by the output D1. Typically, there will be a predetermined range of overdrive voltage that may be added by the voltage regulator to the supply voltage Vdd, the lower value in the range corresponding to a minimum overdrive voltage which is required in order to have any appreciable effect on leakage current, and the
25 upper limit on overdrive voltage being determined by the properties of the PMOS transistors, and in particular an upper limit on voltage whereafter excessive wear out of the transistors is likely to occur. In one example embodiment, the range for the overdrive voltage is between 100 and 250mV. The resolution required by the output of a SAR converter will be dependent on the number of discrete voltages within that
30 range that the voltage regulator 10 is able to produce.

In addition to the leakage sensor 85, the integrated circuit of Figure 1 also includes a process monitor 90 for monitoring the speed of operation of the logic

circuitry 80 during its normal mode of operation, i.e. when it is powered up. The process monitor 90 is able to detect process skew, in particular determining whether the silicon is fast silicon (i.e. the integrated circuit is operating more quickly than the norm) or slow silicon (i.e. the integrated circuit is operating more slowly than the norm). This information has a correlation with leakage current, since components constructed on slow silicon have less leakage current than the same components constructed on fast silicon. As with the leakage sensor 85, the process monitor 90 will convert the values that it observes into a digital signal output over path 92. As with the leakage sensor 85, the process monitor 90 may suitably be constructed by a SAR data converter, for example a 6-bit SAR data converter.

Using the combination of the leakage sensor 85 and the process monitor 90, it will be seen that the adaptive bias controller 20 is provided with input signals that enable it to provide as a digital code a feedback control signal to the voltage regulator to adjust the optimal bias voltage to compensate for both leakage and process skew. The value of the voltage regulator output is then adjusted as a function of the process corner and temperature. For example, if the silicon material is “fast skew” and the temperature on the chip is hot, then the leakage current will be at a high level. In that case, the value of the overdrive voltage could be set for example to near the upper limit of 250mV (assuming the earlier mentioned example range of 100 to 250mV) by the voltage regulator 10 in response to a suitable value of feedback control signal input from the adaptive bias controller 20 over path 40. On the other hand, if the silicon material is “slow skew” and the chip temperature is cold, then the leakage current will be at a low level. In that case, the value of the overdrive voltage could be set to near the lower limit of 100mV. By such an approach, the optimal gate bias point can be maintained in order to allow the power gate switches to be reverse biased (in the super cut off range) as much as necessary to reduce the leakage current to an acceptable level, but no more than necessary so as reduce wear out of the power gate switches.

As will be discussed in more detail later with reference to Figure 2, the voltage regulator 10 will typically be coupled to an external capacitance 15 which serves to smooth out the operation of the voltage regulator when varying the output voltage V_{out} . As also shown in Figure 1, the voltage regulator 10 will typically receive an input voltage V_{ddio} which is higher than V_{dd} , thereby enabling the voltage regulator

to generate a voltage V_{out} which is in excess of V_{dd} . In one particular example, the voltage V_{ddio} may be 3.3 volts, whilst the voltage V_{dd} is 1.0 volts.

As also shown in Figure 1, a clamping device 55 may be provided in association with the output path 50 to ensure that the voltage V_{out} cannot exceed V_{dd} by more than the maximum permitted overdrive voltage, hence providing a safety mechanism for ensuring that the PMOS transistors 72, 74 are not provided with a gate voltage exceeding a safe upper limit.

Figure 2 is a diagram illustrating in more detail the operation of the voltage regulator 10 in one embodiment. As shown in Figure 2, a reference voltage generator 200 is provided which, when enabled over path 42, uses the supply voltage V_{dd} and the current value of the feedback control signal over path 40 to generate a reference voltage 220 representing the desired output voltage to be used to drive the gates of the PMOS transistors 72, 74 within the power gating circuitry 70. The reference voltage generator 200 is powered by the power supply V_{ddio} to enable it to generate the required reference voltage.

Via the low pass filter block 240, the comparator 230 compares the output reference voltage 220 with the current voltage present at the node 260, the result of this comparison being used to generate the voltage 250 provided as an input to the gate of the PMOS transistor 255, so as to adjust the voltage at the node 260 until it corresponds to the reference voltage 220. The low pass filter 240, in combination with the external capacitance 15, serves to ensure stability in the operation of the voltage regulator 10 so that the voltage at the node 260 transitions smoothly to the required voltage, and is maintained at that required voltage. The voltage V_{out} present at the node 260 then provides a gate bias voltage to the power gates 72, 74 with the leakage current 76 then varying dependent on the value of that gate bias voltage.

It will be understood by those skilled in the art that the voltage regulator block can be operated in either a linear or a switch mode of operation. If the load to be driven by the output voltage is relatively low (for example 50mA or less), then a linear mode of operation will typically be more appropriate, whilst if the load is relatively high (greater than 50mA) then a switch mode of operation may be more appropriate.

The adaptive bias controller 20 may be constructed in a variety of ways. However, in one embodiment, the adaptive bias controller is formed by a sequential

finite state machine (FSM), which can be arranged to operate as shown in Figure 3. On assertion of a reset signal, the adaptive bias controller enters the initial state 300, where the enable signal is deasserted, and the adaptive gate bias control operation is disabled. When a power saving mode of operation is to be entered, the enable signal
5 can be set to cause the state to transition from the initial state 300 to the state 310. In this state, an initial programmed value for the feedback control signal is used to cause the voltage regulator to produce an output voltage V_{out} corresponding to that initial programmed value.

Thereafter, the state will transition to the adaptive bias state 320 where the
10 adaptive bias controller 20 is responsive to the operating parameter data D1, D2 received over paths 32, 34. If that operating parameter data indicates a relatively high leakage current, i.e. a leakage current in excess of the desired leakage current, then the process transitions to state 330 where the feedback control signal is issued so as to increase the amount of overdrive voltage added to the supply voltage V_{dd} in order to
15 produce the output voltage V_{out} from the voltage regulator 10. Similarly, if the operating parameter data indicates a level of leakage current below the desired level, then the state transitions from the state 320 to the state 340, where the adaptive bias controller 20 issues a feedback control signal so as to reduce the amount of overdrive voltage added to V_{dd} in order to produce the output voltage V_{out} from the voltage
20 regulator 10.

Following either state 330 or state 340, the state machine transitions to state 350, where it awaits a bias update. In particular, during state 350, the adaptive bias controller awaits an indication that the control voltage most recently set by the voltage regulator circuitry has reached a steady state. This may be done for example by
25 waiting for the elapse of a timer which begins counting when the modified feedback control signal is issued at either state 330 or state 340, or by awaiting a ready signal from the voltage regulator 10, which is only output to the adaptive bias controller 20 when the voltage regulator has produced a steady voltage at its output node 260. Once the steady state has been reached, the state transitions from state 350 back to state 320
30 where the operating parameter data D1, D2 is again monitored. This may cause the state machine to transition again to either state 330 or state 340, or if the operating parameter data indicates that the leakage current is currently within the desired leakage

current range, then no action may be required, and the state machine may merely maintain the state 320 until the operating parameter data indicates that some change in the output voltage V_{out} is required (i.e. the leakage current is no longer within the desired leakage current range).

- 5 From the above description, it will be seen that the FSM embodying the adaptive bias controller 20 is able to take account of the fact that the leakage current in the system is ambient temperature, process and operating voltage dependent, and can accordingly reduce the voltage bias applied to the power gating transistors progressively to a lower threshold point when the overall leakage current is low.
- 10 Conversely, as the leakage current increases, the FSM increases the gate bias voltage in order to reduce the leakage current, and can continue to do this until an upper threshold point is reached (e.g. $V_{dd} + 250\text{mV}$ in the earlier mentioned example).

Figure 4 is a flow diagram illustrating the overall operation of the circuit of Figure 1 when used to provide an overdrive voltage to the power gating circuitry. At

15 step 400, it is determined that a low power mode of operation is required, and then the voltage regulation function is enabled at step 405, whereafter an initial value of the feedback control signal is set by the adaptive bias controller 20 at step 410. This causes the voltage regulator 10 to generate an overdrive voltage dependent on the feedback control signal at step 415, this overdrive voltage being between

20 predetermined upper and lower limits as discussed earlier (for example between $V_{dd}+100\text{mV}$ and $V_{dd}+250\text{mV}$).

Thereafter, it is determined at step 420 whether the voltage has reached a steady state, and when the steady state is reached the process proceeds to step 425, where the adaptive bias controller monitors the received operating parameter data. At

25 step 430, the adaptive bias controller then generates a feedback control signal that is dependent on the operating parameter data. Provided it is determined at step 435 that the low power mode should not be exited, the process then loops back to step 415 where an overdrive voltage is generated dependent on the feedback control signal.

As discussed earlier with reference to Figure 3, it will be understood that in

30 situations where the operating parameter data received at step 425 indicates that the current gate bias voltage is producing the desired level of leakage current, then the feedback control signal issued at step 430 will result in the voltage regulator 10

maintaining its current overdrive voltage at step 415 and hence the voltage will already be at the steady state when assessed at step 420.

The process of Figure 4 continues until the system is to return to the active mode of operation, at which point the process branches from step 435 to step 440 where the process ends. At this point the enable signal is de-asserted to disable operation of the voltage regulator 10, and cause the buffer circuitry 60 to provide a logic 0 input to the gates of the transistors 72, 74 within the power gating circuitry 70, causing those transistors to turn on and couple the logic circuitry 80 to the supply voltage Vdd.

Figure 5 is a graph schematically illustrating how the adaptive bias controller 20 and voltage regulator 10 operate in one embodiment to modify the output voltage Vout so as to drive the leakage current to within an acceptable leakage current range, this acceptable leakage current range being bounded by the lines 540, 550 in Figure 5. Accordingly, if the adaptive bias controller monitors the operating parameters at point A 500, it will assess that the operating parameters indicate that the leakage current is lower than the desired range, and accordingly the adaptive bias controller will issue a feedback control signal over path 40 to the voltage regulator 10, to cause the voltage regulator to decrease the overdrive voltage.

When a steady state is reached, and the adaptive bias controller 20 again analyses the operating parameter data at point B 510, it will see that whilst the leakage current has increased, it is still below the desired range, and hence will again issue a feedback control signal to the voltage regulator that causes the overdrive voltage to be reduced.

However, in the example shown in Figure 5, it is assumed that the reduction turns out to be somewhat larger than was appropriate, and accordingly when the operating parameter data is again assessed at point C 515, it is determined that the leakage current is higher than the desired range. As a result, the adaptive bias controller issues a feedback control signal to cause the voltage regulator to increase the overdrive voltage.

When the steady state is then reached, and the operating parameter data is again analysed at point D 520, it is found that the operating parameter data indicates

that the leakage current is within the desired range, and hence no change in the overdrive voltage is performed.

As illustrated by point E 530, the leakage current may naturally vary even whilst the overdrive voltage is being maintained at a steady level, due for example to
5 changes in operating temperature of the circuit. However, whilst the leakage current remains within the acceptable range, no change in the overdrive voltage is made. In one embodiment, only when the operating parameters indicate that the leakage voltage has moved outside of the acceptable range bounded by the points 540, 550 will the adaptive bias controller again seek to modify the feedback control signal in order to
10 alter the bias voltage.

Using the above described technique, the gate-bias control can be applied to power gated subsystems within the chip to support optimal low-power standby modes. One or more power gated regions can share a single voltage regulator, which may be provided within the chip or externally to the chip, enabling a reduction in
15 system/board-level cost whilst supporting fast and efficient power gating (PG), and optional state-retention power-gating (SRPG). The leakage power for the PG switched subsystem is dependent on the silicon process and exponentially scaled with die temperature as a result of the on-chip transistor power gates being imperfect switches.

Although a particular embodiment has been described herein, it will be
20 appreciated that the invention is not limited thereto and that many modifications and additions thereto may be made within the scope of the invention. For example, various combinations of the features of the following dependent claims could be made with the features of the independent claims without departing from the scope of the present invention.

CLAIMS

1. An integrated circuit comprising:
 - 5 a block of components;
power gating circuitry configured to receive a source voltage supply, and to provide an internal voltage supply to said block of components, in a normal mode of operation the internal voltage supply being derived from the source voltage supply, and in a power saving mode of operation the power gating circuitry being configured
10 to isolate the internal voltage supply from the source voltage supply;
voltage regulator circuitry configured to provide a control voltage to said power gating circuitry during said power saving mode of operation, the control voltage being settable to any of a plurality of predetermined voltage levels;
an adaptive controller configured to receive operating parameter data from at
15 least one of the block of components and the power gating circuitry, the operating parameter data being indicative of leakage current within the power gating circuitry, and the adaptive controller being configured to issue a feedback control signal to the voltage regulator circuitry whose value is dependent on the received operating parameter data;
20 the voltage regulator circuitry being responsive to the feedback control signal to change the control voltage between said plurality of predetermined voltage levels until the operating parameter data indicates a desired leakage current has been obtained within the power gating circuitry.
- 25 2. An integrated circuit as claimed in Claim 1, wherein:
the power gating circuitry comprises at least one PMOS transistor whose gate is driven by the control voltage during said power saving mode of operation;
the control voltage is set to exceed the source voltage supply by an overdrive voltage, the overdrive voltage being variable so as to enable any of said plurality of
30 predetermined voltage levels to be set as said control voltage.
3. An integrated circuit as claimed in Claim 2, wherein:

when the operating parameter data indicates that the leakage current is exceeding the desired leakage current, the adaptive controller is arranged to set the feedback control signal to a value that causes the voltage regulator circuitry to increase the overdrive voltage provided a maximum predetermined voltage level has not been reached; and

when the operating parameter data indicates that the leakage current is below the desired leakage current, the adaptive controller is arranged to set the feedback control signal to a value that causes the voltage regulator circuitry to decrease the overdrive voltage provided a minimum predetermined voltage level has not been reached.

4. An integrated circuit as claimed in Claim 2 or Claim 3, wherein when the operating parameter data indicates that the leakage current matches the desired leakage current, the adaptive controller is arranged to set the feedback control signal to a value that causes the voltage regulator circuitry to maintain a currently set overdrive voltage.

5. An integrated circuit as claimed in any preceding claim, wherein the desired leakage current is specified as a range of leakage current values.

6. An integrated circuit as claimed in any preceding claim, wherein the adaptive controller comprises a state machine that is enabled when said low power mode is entered, the state machine transitioning between a plurality of states dependent on the received operating parameter data.

7. An integrated circuit as claimed in Claim 6, wherein following a feedback adjustment state where the value of the feedback control signal is changed, the state machine enters a waiting state where a predetermined event is awaited before the state machine transitions to a monitoring state to monitor the received operating parameter data.

8. An integrated circuit as claimed in Claim 7, wherein the predetermined event is indicative that the control voltage most recently set by the voltage regulator circuitry has reached a steady state.
- 5 9. An integrated circuit as claimed in any preceding claim, wherein the feedback control signal is an M bit value, enabling up to 2^m discrete predetermined voltage levels for the control voltage to be specified.
- 10 10. An integrated circuit as claimed in any preceding claim, wherein the adaptive controller has an interface via which an initial value of said feedback control signal is specified.
11. An integrated circuit as claimed in any preceding claim, further comprising:
one or more monitoring circuits for monitoring said at least one of the block of
15 components and the power gating circuitry in order to produce said operating parameter data.
12. An integrated circuit as claimed in Claim 11, wherein:
said one or more monitoring circuits comprise a leakage sensor for detecting
20 leakage current in said at least one of the block of components and the power gating circuitry whilst in said low power mode of operation.
13. An integrated circuit as claimed in Claim 11 or Claim 12, wherein:
said one or more monitoring circuits comprise a temperature sensor for
25 monitoring the operating temperature of said at least one of the block of components and the power gating circuitry.
14. An integrated circuit as claimed in any of claims 11 to 13, wherein:
said one or more monitoring circuits comprise process skew monitoring
30 circuitry for monitoring speed of operation of the block of components during the normal mode of operation.

15. A method of controlling power gating in an integrated circuit having a block of components, and power gating circuitry for receiving a source voltage supply and for providing an internal voltage supply to said block of components, in a normal mode of operation the internal voltage supply being derived from the source voltage supply,
5 and in a power saving mode of operation the power gating circuitry being configured to isolate the internal voltage supply from the source voltage supply, the method comprising the steps of:

employing a voltage regulator to provide a control voltage to said power gating circuitry during said power saving mode of operation, the control voltage being
10 settable to any of a plurality of predetermined voltage levels;

obtaining operating parameter data from at least one of the block of components and the power gating circuitry, the operating parameter data being indicative of leakage current within the power gating circuitry;

issuing a feedback control signal to the voltage regulator whose value is
15 dependent on the received operating parameter data;

responsive to the feedback control signal, changing at the voltage regulator the control voltage between said plurality of predetermined voltage levels until the operating parameter data indicates a desired leakage current has been obtained within the power gating circuitry.

20

16. An integrated circuit comprising:

a block of component means;

power gating means for receiving a source voltage supply, and for providing an internal voltage supply to said block of component means, in a normal mode of
25 operation the internal voltage supply being derived from the source voltage supply, and in a power saving mode of operation the power gating means for isolating the internal voltage supply from the source voltage supply;

voltage regulator means for providing a control voltage to said power gating means during said power saving mode of operation, the control voltage being settable
30 to any of a plurality of predetermined voltage levels;

adaptive controller means for receiving operating parameter data from at least one of the block of component means and the power gating means, the operating

parameter data being indicative of leakage current within the power gating means, and the adaptive controller means for issuing a feedback control signal to the voltage regulator means whose value is dependent on the received operating parameter data;

- 5 the voltage regulator means, responsive to the feedback control signal, for changing the control voltage between said plurality of predetermined voltage levels until the operating parameter data indicates a desired leakage current has been obtained within the power gating means.

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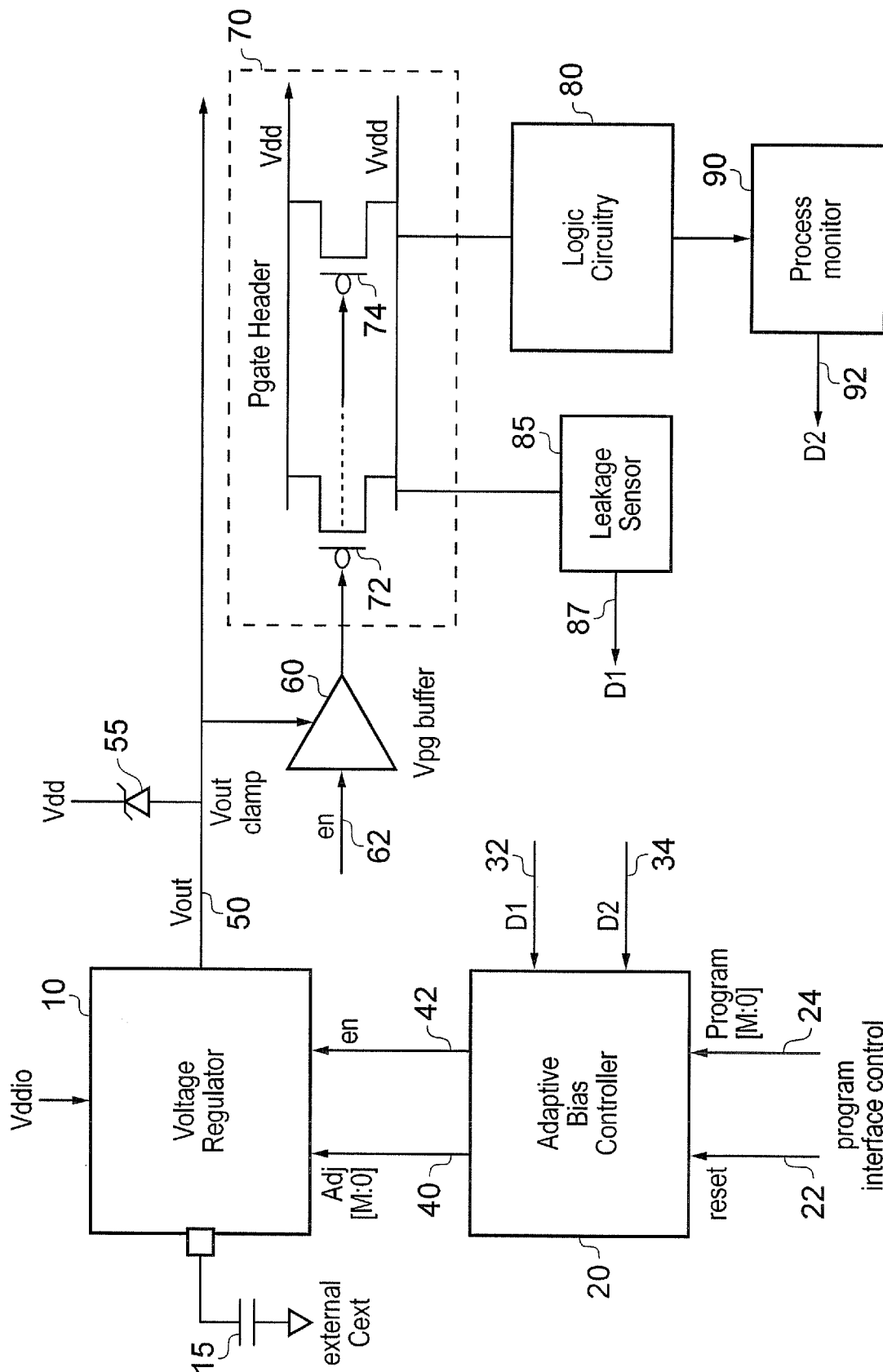


FIG. 1

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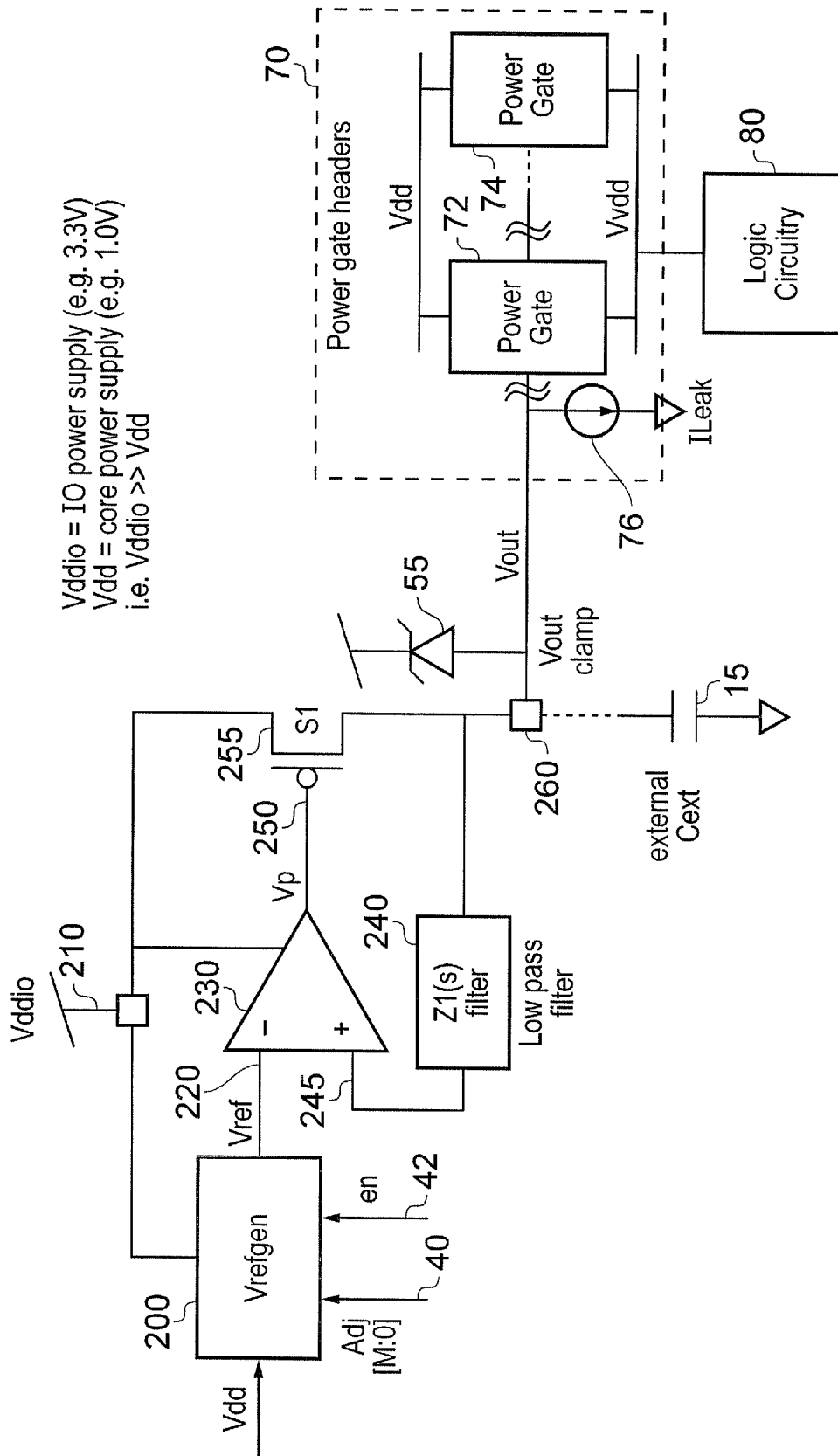


FIG. 2

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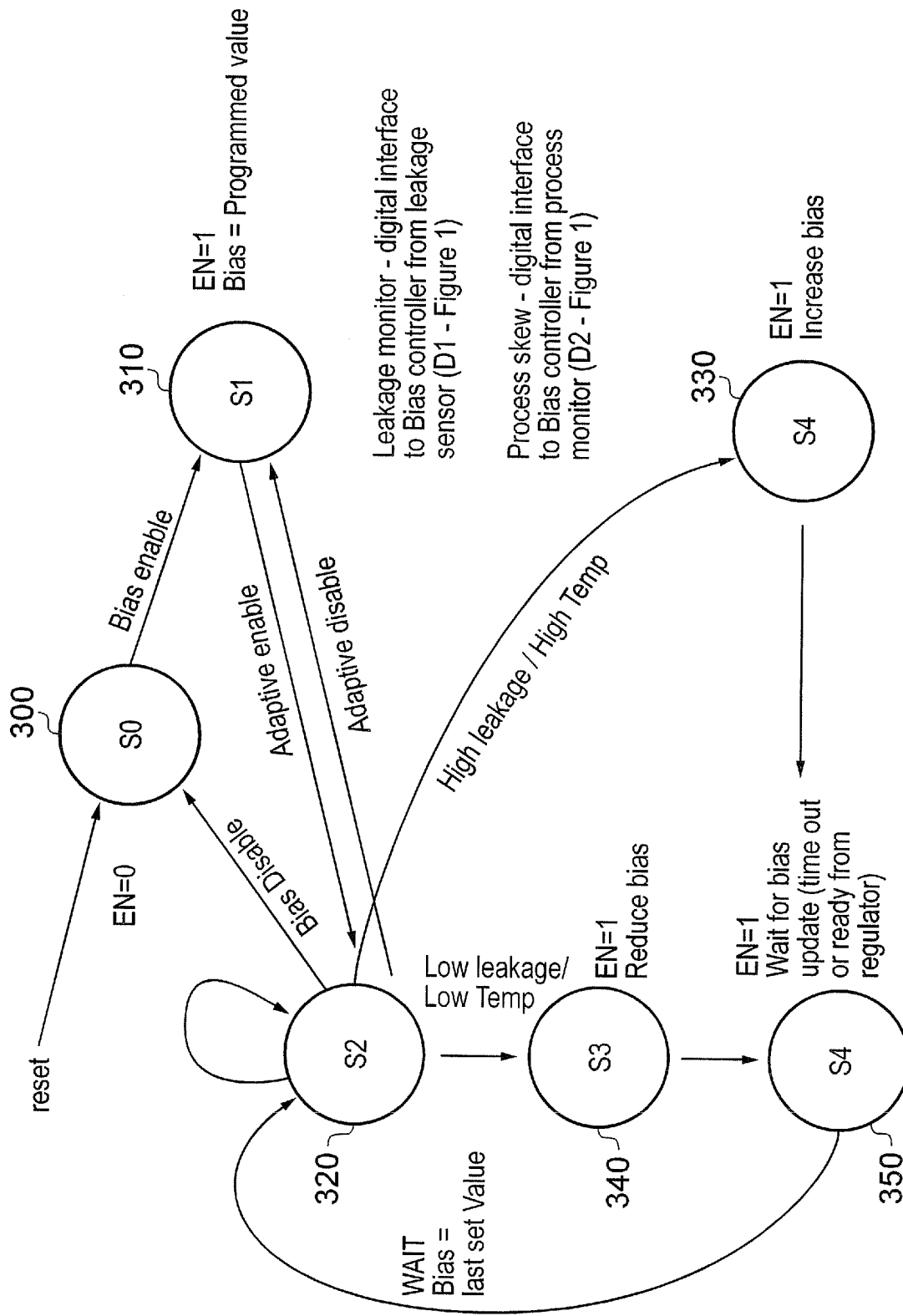


FIG. 3

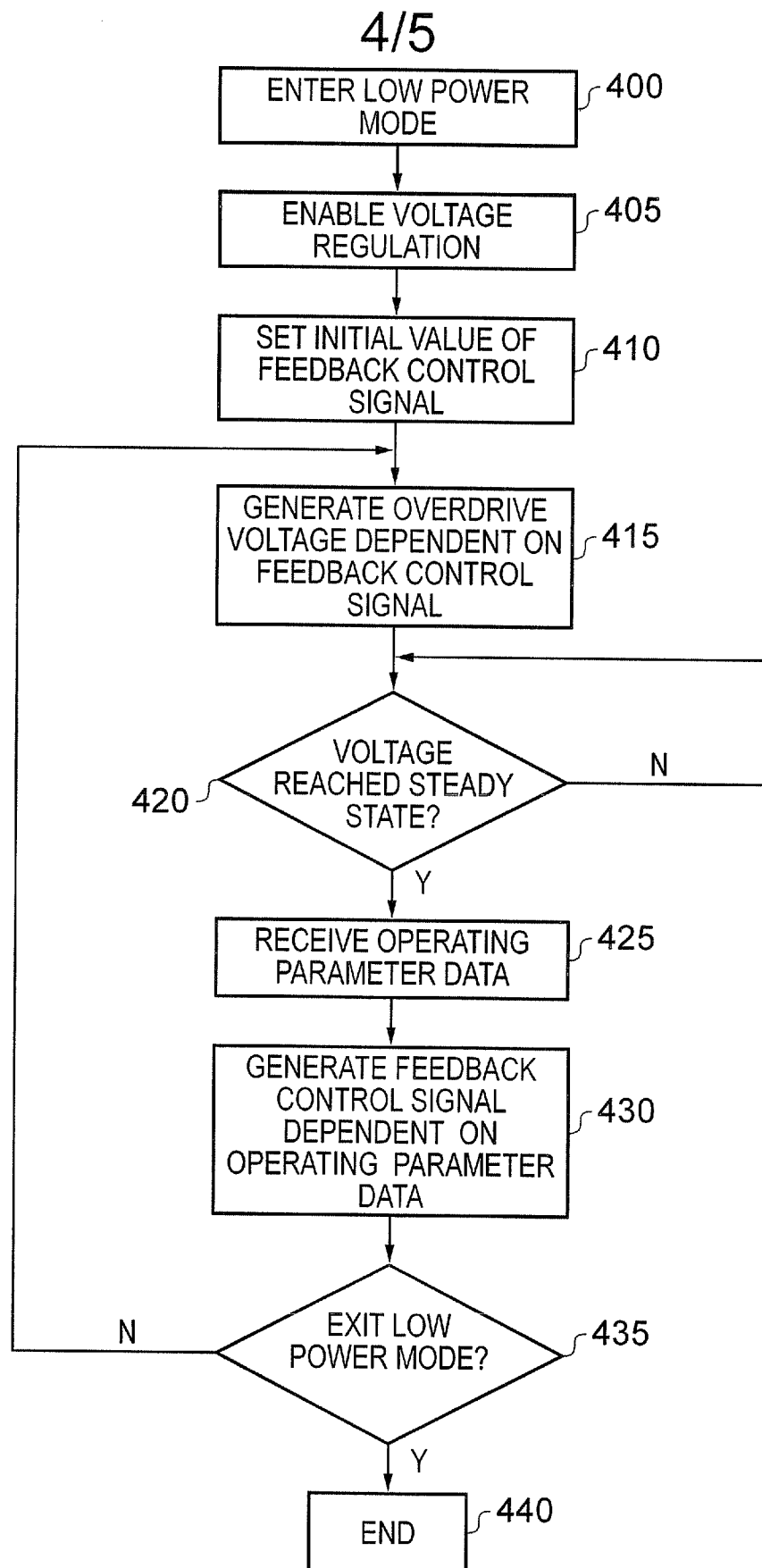


FIG. 4

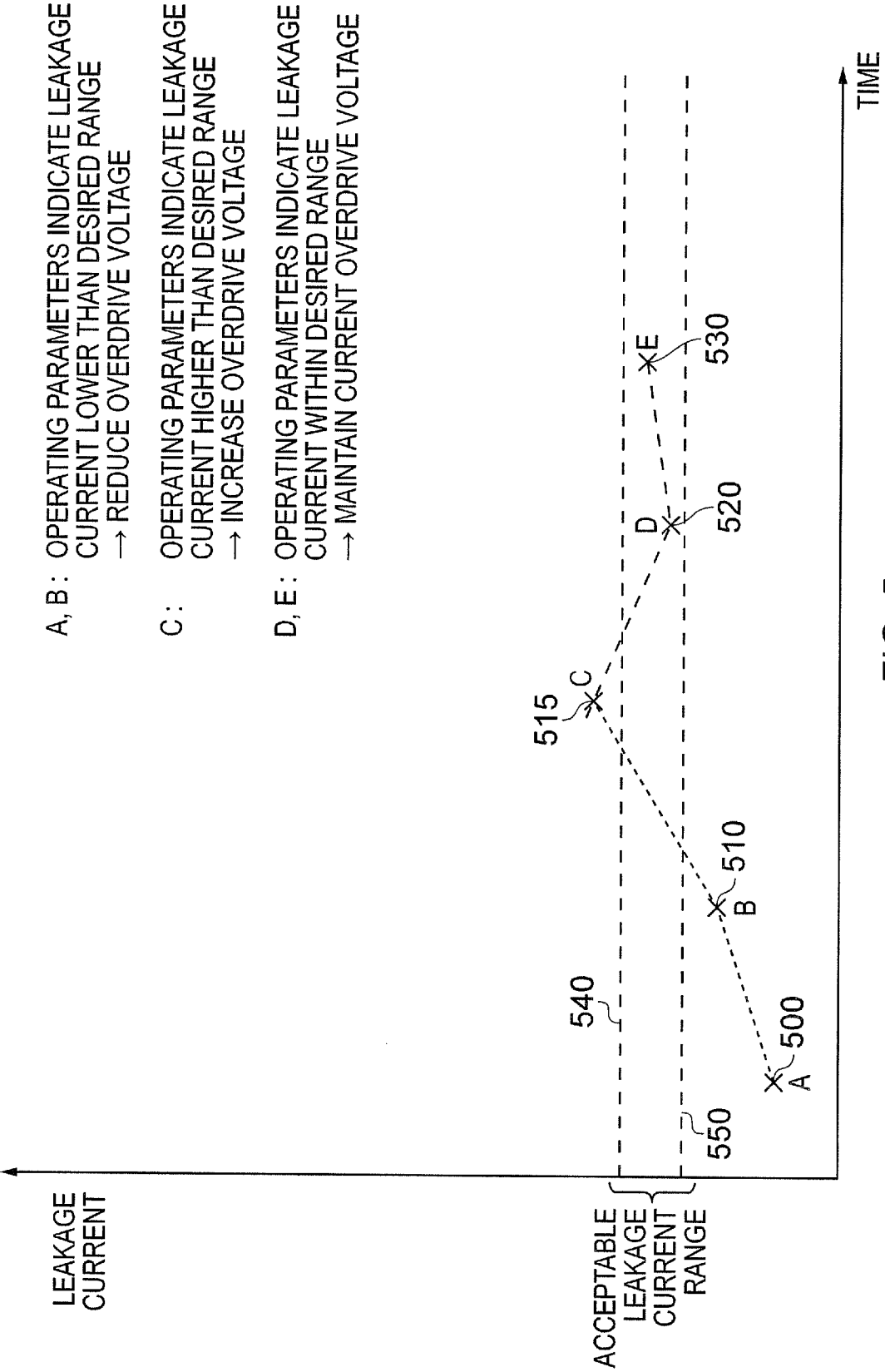


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2011/051986

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03K19/00 H03K19/003 H03K17/14
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03K G11C G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 2 184 855 A1 (COMMISSARIAT ENERGIE ATOMIQUE [FR]) 12 May 2010 (2010-05-12) the whole document	1-16
X	VALENTIAN A ET AL: "Automatic Gate Biasing of an SCCMOS Power Switch Achieving Maximum Leakage Reduction and Lowering Leakage Current Variability", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 40, no. 7, 1 July 2008 (2008-07-01), pages 1688-1698, XP011229244, ISSN: 0018-9200 the whole document	1-16
X	US 2006/006929 A1 (CAPLAN RANDY J [US] ET AL) 12 January 2006 (2006-01-12) the whole document	1-16



Further documents are listed in the continuation of Box C.



See patent family annex.

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- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- "&" document member of the same patent family

Date of the actual completion of the international search

13 December 2011

Date of mailing of the international search report

20/12/2011

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Loiseau, Ludovic

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

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