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(54) Title: COMPLEMENTARY BACK END OF LINE (BEOL) CAPACITOR

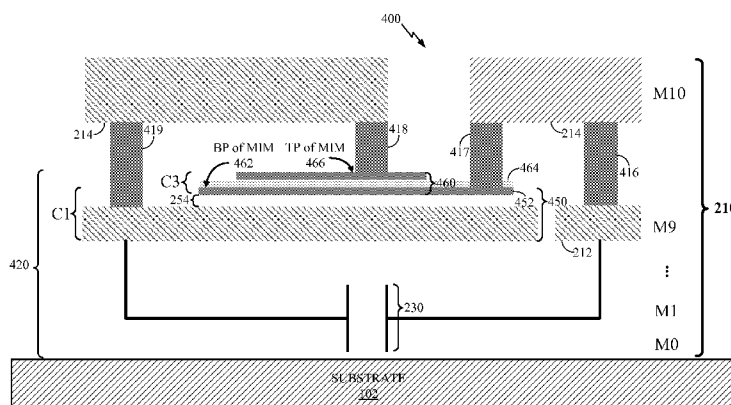


FIG. 4

(57) **Abstract:** A complementary back end of line (BEOL) capacitor (CBC) structure includes a metal oxide metal (MOM) capacitor structure. The MOM capacitor structure is coupled to a first upper interconnect layer of an interconnect stack of an integrated circuit (IC) device. The MOM capacitor structure includes at least one lower interconnect layer of the interconnect stack. The CBC structure may also include a second upper interconnect layer of the interconnect stack coupled to the MOM capacitor structure. The CBC structure also includes at least one metal insulator metal (MIM) capacitor layer between the first upper interconnect layer and the second upper interconnect layer. In addition, CBC structure may also include a MIM capacitor structure coupled to the MOM capacitor structure. The MIM capacitor structure includes a first capacitor plate having a portion of the first upper interconnect layer, and a second capacitor plate having a portion of the MIM capacitor layer(s).





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## COMPLEMENTARY BACK END OF LINE (BEOL) CAPACITOR

### TECHNICAL FIELD

**[0001]** The present disclosure relates generally to capacitors. More specifically, the disclosure relates to a complementary back end of line (BEOL) capacitor structure that combines a metal oxide metal (MOM) capacitor and one or more metal insulator metal (MIM) capacitors from different conductive interconnect layers.

### BACKGROUND

**[0002]** Capacitors are widely used in integrated circuits. FIGURE 1 is a block diagram illustrating a cross section of an integrated circuit (IC) device 100 including an interconnect stack 110. The interconnect stack 110 of the IC device 100 includes multiple conductive interconnect layers (M1, ..., M9, M10) on a semiconductor substrate (e.g., a silicon wafer) 102. The semiconductor substrate 102 supports metal oxide metal (MOM) capacitors 130. In this example, a first MOM capacitor 130A is formed in the M3 and M4 interconnect layers, and a second MOM capacitor 130B is formed in the M5 and M6 interconnect layers. The MOM capacitors 130 (130A and 130B) are formed from lateral conductive fingers of different polarities using the conductive interconnect layers (M3 and M4/M5 and M6) of the interconnect stack 110. An dielectric (not shown) is provided between the conductive fingers.

**[0003]** In this example, the MOM capacitors 130 are formed within the lower conductive interconnect layers (e.g., M1 - M6) of the interconnect stack 110. The lower conductive interconnect layers of the interconnect stack 110 have smaller interconnect widths and spaces. For example, the dimensions of the conductive interconnect layers M3 and M4 are half the size of the dimensions of the conductive interconnect layers M5 and M6. Likewise, the dimensions of the conductive interconnect layers M1 and M2 are half the size of the dimensions of the conductive interconnect layers M3 and M4. The small interconnect widths and spaces of the lower conductive interconnect layers enable the formation of MOM capacitors with increased capacitance density.

**[0004]** As shown in FIGURE 1, the MOM capacitors 130 make use of a lateral (intra layer) capacitive coupling 140 between fingers formed by standard metallization of the conductive interconnects (e.g., wiring lines and vias). The lateral coupling 140

within the MOM capacitors 130 provides improved matching characteristics when compared to the vertical coupling of parallel vertical plate capacitors. The improved matching characteristics of the MOM capacitors 130 are the result of improved process control of the lateral dimensions within the interconnect stack 110. By contrast, the process controls of the vertical dimensions of the conductive interconnect and dielectric layer thickness within the interconnect stack 110 are less precise for providing small value capacitance.

**[0005]** It is becoming significantly more challenging to fabricate high density capacitance. Consequently, using only MOM capacitors in future process technologies may be insufficient to provide high density capacitance for IC devices.

**[0006]** A metal insulator metal (MIM) capacitor in the back end of line (BEOL) layers has been proposed. The MIM capacitor uses vertical plate to plate coupling. This solution, however, involves additional masks as well as a high-K (HiK) oxide deposition process to achieve an increased capacitor density. In addition, MIM capacitors are generally formed between the upper conductive interconnect layers (e.g., M9 and M10) of the interconnect stack 110.

## SUMMARY

**[0007]** The present disclosure describes a complementary back end of line (BEOL) capacitor (CBC) structure that has a combined MIM and MOM structure. The combined structure increases capacitance density.

**[0008]** In one aspect of the present disclosure, a complementary back end of line (BEOL) capacitor (CBC) structure has a metal oxide metal (MOM) capacitor structure coupled to a first upper interconnect layer of an interconnect stack of an integrated circuit (IC) device. The MOM capacitor structure includes at least one lower interconnect layer of the interconnect stack. The CBC structure may also include a second upper interconnect layer of the interconnect stack coupled to the MOM capacitor structure. The CBC structure also includes at least one metal insulator metal (MIM) capacitor layer between the first upper interconnect layer and the second upper interconnect layer. In addition, the CBC structure may also include a MIM capacitor structure coupled to the MOM capacitor structure. The MIM capacitor structure includes a first capacitor plate having at least a portion of the first upper interconnect

layer, and a second capacitor plate having at least a portion of the MIM capacitor layer(s).

**[0009]** According to another aspect of the present disclosure, a method for fabricating a complementary back end of line (BEOL) capacitor (CBC) structure is described. The method includes forming a metal oxide metal (MOM) capacitor structure within lower interconnect layers of an interconnect stack of an integrated circuit (IC) device. The method also includes depositing at least one metal insulator metal (MIM) capacitor layer between a first upper interconnect layer and a second upper interconnect layer of the interconnect stack. The method further includes forming a MIM capacitor structure coupled to the MOM capacitor structure. The MIM capacitor structure includes a first capacitor plate having at least a portion of the first upper interconnect layer, and a second capacitor plate having at least a portion of the MIM capacitor layer(s).

**[0010]** In a further aspect of the present disclosure, a complementary back end of line (BEOL) capacitor (CBC) structure is described. The CBC structure includes a means for storing electric charge coupled to a first upper interconnect layer of an interconnect stack of an integrated circuit (IC) device. The electric charge storing means includes at least one lower interconnect layer of the interconnect stack. The CBC structure may also include a second upper interconnect layer of the interconnect stack coupled to the electric charge storing means. The CBC structure also includes at least one metal insulator metal (MIM) capacitor layer between the first upper interconnect layer and the second upper interconnect layer. In addition, CBC structure may also include a MIM capacitor structure coupled to the MOM capacitor structure. The MIM capacitor structure includes a first capacitor plate as at least a portion of the first upper interconnect layer, and a second capacitor plate as at least a portion of the MIM capacitor layer(s).

**[0011]** This has outlined, rather broadly, the features and technical advantages of the present disclosure in order that the detailed description that follows may be better understood. Additional features and advantages of the disclosure will be described below. It should be appreciated by those skilled in the art that this disclosure may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled

in the art that such equivalent constructions do not depart from the teachings of the disclosure as set forth in the appended claims. The novel features, which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages, will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

**[0012]** The features, nature, and advantages of the present disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings.

**[0013]** FIGURE 1 is a block diagram illustrating an integrated circuit (IC) device including an interconnect stack that contains conventional metal oxide metal (MOM) capacitor structures.

**[0014]** FIGURE 2 shows a cross-sectional view illustrating an integrated circuit (IC) device including a complementary back end of line (BEOL) capacitor structure according to an aspect of the present disclosure.

**[0015]** FIGURE 3 shows a cross-sectional view illustrating an integrated circuit (IC) device including a complementary back end of line (BEOL) capacitor structure according to another aspect of the present disclosure.

**[0016]** FIGURE 4 shows a cross-sectional view illustrating an integrated circuit (IC) device including a complementary back end of line (BEOL) capacitor structure according to a further aspect of the present disclosure.

**[0017]** FIGURE 5 shows a cross-sectional view illustrating an integrated circuit (IC) device including a complementary back end of line (BEOL) capacitor structure according to another aspect of the present disclosure.

**[0018]** FIGURE 6 shows a cross-sectional view illustrating an integrated circuit (IC) device including a complementary back end of line (BEOL) capacitor structure according to an additional aspect of the present disclosure.

**[0019]** FIGURE 7 illustrates a method for fabricating a complementary back end of line (BEOL) capacitor according to an aspect of the present disclosure.

**[0020]** FIGURE 8 shows an exemplary wireless communication system in which an aspect of the disclosure may be advantageously employed.

### DETAILED DESCRIPTION

**[0021]** The detailed description set forth below, in connection with the appended drawings, is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of the various concepts. However, it will be apparent to those skilled in the art that these concepts may be practiced without these specific details. In some instances, well-known structures and components are shown in block diagram form in order to avoid obscuring such concepts. As described herein, the use of the term “and/or” is intended to represent an “inclusive OR”, and the use of the term “or” is intended to represent an “exclusive OR”.

**[0022]** One aspect of the disclosure describes a complementary back end of line (BEOL) capacitor (CBC) structure. In one configuration, a CBC structure combines a metal oxide metal (MOM) capacitor structure and one or more metal insulator metal (MIM) capacitor structures. Combining a MOM capacitor structure with a MIM capacitor structure from different conductive interconnect layers provides the complementary BEOL capacitor structure with increased capacitance area density. In this configuration, the complementary BEOL capacitor structure combines the lateral coupling of the conductive fingers of a MOM capacitor structure with the vertical coupling of the parallel plates of a MIM capacitor structure. The complementary BEOL capacitor structure exhibits increased capacitor area density by combining capacitor structures from different conductive interconnect layers of an interconnect stack. In this configuration, the interconnect stack of an IC device includes multiple conductive interconnect layers (e.g., conductive layers M1 to M10). While the MOM capacitor

structure may be formed using a conventional process, in this configuration, a process for forming a MIM capacitor is altered to form the complementary BEOL capacitor structure.

**[0023]** A MIM capacitor structure may be formed between the upper interconnect layers of an interconnect stack (e.g., M9 and M10). In one configuration, a single one of a top plate or a bottom plate of a MIM capacitor is used to form a MIM capacitor structure between the top/bottom plate of the MIM capacitor and one of the upper conductive interconnect layers that is immediately below the top/bottom plate. In particular, one aspect of the present disclosure couples a MIM capacitor structure with the positive and negative nodes of a MOM capacitor structure to form a complementary BEOL capacitor structure, for example, as shown in FIGURE 2. The use of one of the upper interconnect layers of an interconnect stack as a plate of the MIM capacitor structure enables a simplified fabrication process. Fabrication of the MIM capacitor in this manner avoids an additional deposition and mask for fabricating one of the plates of a MIM capacitor. That is, a MIM capacitor structure is formed between a single MIM capacitor plate and an adjacent upper interconnect layer, for example, as shown in FIGURE 2.

**[0024]** FIGURE 2 shows a cross-sectional view illustrating an integrated circuit (IC) device 200 including a complementary back end of line (BEOL) capacitor (CBC) structure 220 according to one aspect of the disclosure. Representatively, the IC device 200 includes a semiconductor substrate (e.g., a silicon wafer) 102 that supports an interconnect stack 210. In this configuration, the interconnect stack 210 includes multiple conductive interconnects layers (e.g., M0 to M10). Although described with reference to the conductive interconnect layers M0 to M10, the present disclosure may be applied to any IC device that includes an interconnect stack, where the number of the conductive interconnect layers is determined by the relevant process technology. As described herein, the term “semiconductor substrate” may refer to a substrate of a diced wafer or may refer to the substrate of a wafer that is not diced, i.e., a wafer itself. The term “metal” can be any conductive or semiconductive material.

**[0025]** In FIGURE 2, a metal oxide metal (MOM) capacitor structure 230 is formed within the lower conductive interconnect layers (e.g., M1 - M6) of the interconnect stack 110, for example, as shown in FIGURE 1. In this configuration, a



conventional process of forming a metal insulator metal (MIM) capacitor between a first upper interconnect layer 212 (M9) and a second upper interconnect layer 214 (M10) is modified. Rather than using the conventional MIM process to form a bottom plate 262 and a top plate 266 of a MIM capacitor, in this configuration, a MIM capacitor structure 250 includes a top plate 252 and a first upper interconnect layer 212 (e.g., M9) as a bottom plate. That is, the conventional MIM mask or process is modified at this location to skip the mask and deposition for fabricating the top plate of a MIM capacitor that may be formed between the first upper interconnect layer 212 and a second upper interconnect layer 214. The top plate 266 is shown in dotted lines because it will not actually exist in this configuration. (See FIGURE 6 for an example of a MIM capacitor with a top plate 466.)

**[0026]** In this configuration, the top plate 252 of the MIM capacitor structure 250 is formed above the first upper interconnect layer 212 (M9) by using a bottom plate mask of the conventional MIM process. An optional dielectric layer 256 is formed on the top plate 252 of the MIM capacitor structure 250, which is coupled to the second upper interconnect layer 214 with a via 217. In addition, the first upper interconnect layer 212 (M9) is coupled to the second upper interconnect layer 214 (M10) using a via 216.

**[0027]** A capacitance density ( $C_1$ ) of the MIM capacitor structure 250 may be determined as follows:

**[0028]** A distance 254 between the top plate 252 and the first upper interconnect layer 212 (the bottom plate) of the MIM capacitor structure 250 is generally in the range of fifty (50) to one hundred (100) nanometers according to the conventional MIM process. Assuming a dielectric constant ( $k_1$ ) equal to five (5) and a distance 254 between the top plate 252 and the first upper interconnect layer 212 is 50 nanometers, the capacitance density ( $C_1$ ) of the MIM capacitor structure 250 equals approximately 0.89 femtofarads (fF) per micro meter squared ( $\text{fF}/\mu\text{m}^2$ ). A capacitance density of the MOM capacitor structure 230 is approximately  $0.78 \text{ fF}/\mu\text{m}^2$  for each layer (assuming a fine line configuration according to a twenty eight nanometer process technology and a ninety (90) nanometer pitch of one of the lower conductive interconnect layers (e.g., M1 to M6)). The capacitance density ( $C_1$ ) of the MIM capacitor structure 250 is approximately equal to the capacitance density of one lower (or finer) layer of the

MOM capacitor structure 230, when fabricated according to the noted fine line configuration.

**[0029]** FIGURE 3 shows a cross-sectional view illustrating an integrated circuit (IC) device 300 including a complementary back end of line (BEOL) capacitor (CBC) structure 320 according to another aspect of the present disclosure. In one configuration, a MIM capacitor structure 350 includes a top plate 358, a high-K dielectric layer 356 and the first upper interconnect layer 212 (e.g., M9) as a bottom plate. In this configuration, the top plate 358 is fabricated using a modified MIM process to fabricate only a top plate 366 of a MIM capacitor. That is, the conventional MIM process is modified to skip the deposition and mask for fabricating the bottom plate of a MIM capacitor that may be formed between the first upper interconnect layer 212 (M9) and the second upper interconnect layer 214 (M10). In addition, a high-K dielectric layer 356 may be deposited on the top plate 358 to increase a capacitance density (C2) of the MIM capacitor structure 350. A capacitance density of the CBC structure 320 may include the combined parallel capacitance density of the MIM capacitor structure 350 (C2) and the MOM capacitor structure 230.

**[0030]** FIGURE 4 shows a cross-sectional view illustrating an integrated circuit (IC) device 400 including a complementary back end of line (BEOL) capacitor (CBC) structure 420 according to another aspect of the disclosure. In this configuration, a first MIM capacitor structure 450 includes a top plate 452 and the first upper interconnect layer 212 as a bottom plate. That is, the bottom plate of the first MIM capacitor structure 450 corresponds to the first upper interconnect layer 212 (e.g., M9) of the interconnect stack 210. In addition, a second MIM capacitor structure 460 is formed between the first upper interconnect layer 212 (M9) and the second upper interconnect layer 214 (M10). The second MIM capacitor structure 460 includes a bottom plate 462, a dielectric layer 464, and a top plate 466. The bottom plate 462 is coupled to the first upper interconnect layer 212 and the second upper interconnect layer 214 with vias 416 and 417. The top plate 466 is coupled to the first upper interconnect layer 212 and the second upper interconnect layer 214 with vias 418 and 419.

**[0031]** As further illustrated in FIGURE 4, the first MIM capacitor structure 450 and the second MIM capacitor structure 460 share the top plate 452 and the bottom plate 462. That is, the bottom plate of the second MIM capacitor structure 460 also

functions as the top plate 452 of the first MIM capacitor structure 450. The CBC structure 420 may include the combined parallel capacitance density of the first MIM capacitor structure 450 (C1), the second MIM capacitor structure 460 (C3), and the MOM capacitor structure 230.

**[0032]** FIGURE 5 shows a cross-sectional view illustrating an integrated circuit (IC) device 500, including a complementary back end of line (BEOL) capacitor (CBC) structure 520 according to a further aspect of the present disclosure. In this configuration, an upper layer 532 of a MOM capacitor structure 530 is the first upper interconnect layer 212 (M9) of the interconnect stack 210. Although the upper layer 532 of the MOM capacitor structure 530 is shown to include parallel conductive fingers, the conductive fingers of the MOM capacitor structure 530 may be arranged in a parallel, an orthogonal, or other like hybrid configuration. A MIM capacitor structure 550 may share the upper layer 532 of the MOM capacitor structure 530 to provide a bottom plate. In this configuration, the MIM capacitor structure 550 includes a top plate 558, a high-k dielectric layer 556 and a first upper interconnect layer 212 as a bottom plate.

**[0033]** In this configuration, the top plate 558 may be fabricated using a modified MIM process to fabricate only a top plate 566 of a MIM capacitor. That is, the conventional MIM process is modified to skip the mask and deposition for fabricating the bottom plate of a MIM capacitor formed between the first upper interconnect layer 212 and the second upper interconnect layer 214. In addition, a high-K dielectric layer 556 may be deposited on the top plate 558 to increase the capacitance density (C2') of the MIM capacitor structure 550. In this configuration, the capacitance density (C2') of the MIM capacitor structure 550 is less than the capacitance density (C2) of the MIM capacitor structure 350 of FIGURE 3.

**[0034]** FIGURE 6 shows a cross-sectional view illustrating an integrated circuit (IC) device 600 including a complementary back end of line (BEOL) capacitor (CBC) structure 620 according to an additional aspect of the present disclosure. In this configuration, a MIM capacitor structure 460 is formed between the first upper interconnect layer 212 and the second upper interconnect layer 214. The first upper interconnect layer 212, however, is modified so that the first upper interconnect layer 212 does not provide a bottom plate for formation of an additional MIM capacitor

structure, for example, as shown in FIGURE 4. In this configuration, the CBC structure 620 may include the combined parallel capacitance density of the MIM capacitor structure 460 (C3) and the MOM capacitor structure 230.

**[0035]** FIGURE 7 illustrates a method 700 for fabricating a complementary back end of line (BEOL) capacitor (CBC) structure according to an aspect of the disclosure. In block 710, a metal oxide metal (MOM) capacitor structure is formed within the lower interconnect layers of an interconnect stack of an integrated circuit (IC) device. For example, as shown in FIGURE 1, a MOM capacitor 130 is formed within the lower conductive interconnect layers (e.g., M1 - M6) of an interconnect stack 110. In block 712, one or more metal insulator metal (MIM) capacitor layers are deposited between a first upper interconnect layer and a second upper interconnect layer of an interconnect stack.

**[0036]** For example, as shown in FIGURE 2, a conventional process of forming a MIM capacitor between a first upper interconnect layer 212 (M9) and a second upper interconnect layer 214 (M10) is modified. Rather than using the conventional MIM process to form a top plate and a bottom plate of a MIM capacitor, in this configuration, a bottom plate mask and deposition process are used to fabricate a first capacitor plate (top plate 252) of the MIM capacitor structure 250. In addition, a first upper interconnect layer 212 (e.g., M9) provides a second capacitor plate of the MIM capacitor structure 250. In an alternative configuration, a top plate 358 is fabricated using a modified MIM process to fabricate only a top plate 366 of a MIM capacitor, for example, as shown in FIGURE 3. That is, the conventional MIM process is modified to skip the mask and deposition for fabricating the bottom plate of a MIM capacitor that may be formed between the first upper interconnect layer 212 (M9) and the second upper interconnect layer 214 (M10).

**[0037]** Referring again to FIGURE 7, at block 714, a MIM capacitor structure is formed that is coupled to a MOM capacitor structure. For example, as shown in FIGURE 2, the MIM capacitor structure 250 includes at least a portion of the first upper interconnect layer 212 as a first capacitor plate, and a second capacitor plate (top plate 252) includes the bottom capacitor plate formed according to a modified MIM fabrication process. For example, as shown in FIGURE 2, a single one of a top plate or a bottom plate of a MIM capacitor is used to form a MIM capacitor structure between

the top/bottom plate of the conventional MIM capacitor and one of the upper conductive interconnect layers. In particular, one aspect of the present disclosure couples the MIM capacitor structure 250 with the positive and negative nodes of the MOM capacitor structure 230 to form a CBC structure 220, for example, as shown in FIGURE 2.

**[0038]** In one configuration, a complementary back end of line (BEOL) capacitor (CBC) structure of an integrated circuit (IC) device includes a means for storing electric charge coupled to a first upper interconnect layer of an interconnect stack of an integrated circuit (IC) device. The electric charge storing means includes at least one lower interconnect layer of the interconnect stack. In one aspect of the disclosure, the electric charge storing means may be the MOM capacitor structure 230 configured to perform the functions recited by the electric charge storing means. The CBC structure may also include a second upper interconnect layer of the interconnect stack coupled to the electric charge storing means. The CBC structure also includes at least one metal insulator metal (MIM) capacitor layer between the first upper interconnect layer and the second upper interconnect layer. In addition, the CBC structure includes a MIM capacitor structure coupled to the electric charge storing means. The MIM capacitor structure includes a first capacitor plate having at least a portion of the first upper interconnect layer, and a second capacitor plate having at least a portion of the at least one MIM capacitor layer. In another aspect, the aforementioned means may be any device configured to perform the functions recited by the electric charge storing means.

**[0039]** FIGURE 8 shows an exemplary wireless communication system 800 in which an aspect of the disclosure may be advantageously employed. For purposes of illustration, FIGURE 8 shows three remote units 820, 830, and 850 and two base stations 840. It will be recognized that wireless communication systems may have many more remote units and base stations. Remote units 820, 830, and 850 include CBC structures 825A, 825B, and 825C. FIGURE 8 shows forward link signals 880 from the base stations 840 and the remote units 820, 830, and 850 and reverse link signals 890 from the remote units 820, 830, and 850 to base stations 840.

**[0040]** In FIGURE 8, the remote unit 820 is shown as a mobile telephone, remote unit 830 is shown as a portable computer, and remote unit 850 is shown as a

fixed location remote unit in a wireless local loop system. For example, the remote units may be cell phones, hand-held personal communication systems (PCS) units, a set top box, a music player, a video player, an entertainment unit, a navigation device, portable data units, such as personal data assistants, or fixed location data units such as meter reading equipment. Although FIGURE 8 illustrates remote units, which may employ CBC structures 825A, 825B, 825C according to the teachings of the disclosure, the disclosure is not limited to these exemplary illustrated units. For instance, a CBC structure according to aspects of the present disclosure may be suitably employed in any device.

**[0041]** For a firmware and/or software implementation, the methodologies may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. Any machine-readable medium tangibly embodying instructions may be used in implementing the methodologies described herein. For example, software codes may be stored in a memory and executed by a processor unit. Memory may be implemented within the processor unit or external to the processor unit. As used herein the term “memory” refers to any type of long term, short term, volatile, nonvolatile, or other memory and is not to be limited to any particular type of memory or number of memories, or type of media upon which memory is stored.

**[0042]** Although the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the technology of the disclosure as defined by the appended claims. For example, relational terms, such as “above” and “below” are used with respect to a substrate or electronic device. Of course, if the substrate or electronic device is inverted, above becomes below, and vice versa. Additionally, if oriented sideways, above and below may refer to sides of a substrate or electronic device. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may

be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps

**[0043]** The methodologies described herein may be implemented by various means depending upon the application. For example, these methodologies may be implemented in hardware, firmware, software, or any combination thereof. For a hardware implementation, the processing units may be implemented within one or more application specific integrated circuits (ASICs), digital signal processors (DSPs), digital signal processing devices (DSPDs), programmable logic devices (PLDs), field programmable gate arrays (FPGAs), processors, controllers, micro-controllers, microprocessors, electronic devices, other electronic units designed to perform the functions described herein, or a combination thereof.

**[0044]** For a firmware and/or software implementation, the methodologies may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. Any machine or computer readable medium tangibly embodying instructions may be used in implementing the methodologies described herein. For example, software code may be stored in a memory and executed by a processor. When executed by the processor, the executing software code generates the operational environment that implements the various methodologies and functionalities of the different aspects of the teachings presented herein. Memory may be implemented within the processor or external to the processor. As used herein, the term “memory” refers to any type of long term, short term, volatile, nonvolatile, or other memory and is not to be limited to any particular type of memory or number of memories, or type of media upon which memory is stored.

**[0045]** The machine or computer readable medium that stores the software code defining the methodologies and functions described herein includes physical computer storage media. A storage medium may be any available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer. As used herein, disk and/or disc includes compact disc (CD),

laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where *disks* usually reproduce data magnetically, while *discs* reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer readable media.

**[0046]** In addition to storage on computer readable medium, instructions and/or data may be provided as signals on transmission media included in a communication apparatus. For example, a communication apparatus may include a transceiver having signals indicative of instructions and data. The instructions and data are configured to cause one or more processors to implement the functions outlined in the claims.

**[0047]** Although the present teachings and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the technology of the teachings as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular aspects of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding aspects described herein may be utilized according to the present teachings. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.



## CLAIMS

What is claimed is:

1. A capacitor comprising:
  - a metal oxide metal (MOM) capacitor structure coupled to a first upper interconnect layer of an interconnect stack of an integrated circuit (IC) device, the MOM capacitor structure comprising at least one lower interconnect layer of the interconnect stack;
  - a second upper interconnect layer of the interconnect stack coupled to the MOM capacitor structure;
  - at least one metal insulator metal (MIM) capacitor layer between the first upper interconnect layer and the second upper interconnect layer; and
  - a MIM capacitor structure coupled to the MOM capacitor structure, the MIM capacitor structure comprising a first capacitor plate including at least a portion of the first upper interconnect layer, and a second capacitor plate including at least a portion of the at least one MIM capacitor layer.
2. The capacitor of claim 1, further comprising an additional MIM capacitor structure between the first upper interconnect layer and the second upper interconnect layer of the interconnect stack, the additional MIM capacitor structure comprising a first capacitor plate, a dielectric layer, and the first capacitor plate of the MIM capacitor structure as a second capacitor plate.
3. The capacitor of claim 2, in which a first portion of the second upper interconnect layer is coupled to the first capacitor plate of the additional MIM capacitor structure and a second portion of the second upper interconnect layer is coupled to the second capacitor plate of the additional MIM capacitor structure.
4. The capacitor of claim 1, integrated into a cell phone, a hand-held personal communication system (PCS) unit, a set top box, a music player, a video player, an entertainment unit, a navigation device, a portable data unit, and/or a fixed location data unit.

5. A method of fabrication a capacitor comprising:  
forming a metal oxide metal (MOM) capacitor structure within lower interconnect layers of an interconnect stack of an integrated circuit (IC) device;  
depositing at least one metal insulator metal (MIM) capacitor layer between a first upper interconnect layer and a second upper interconnect layer of the interconnect stack; and  
forming a MIM capacitor structure coupled to the MOM capacitor structure, the MIM capacitor structure comprising a first capacitor plate including at least a portion of the first upper interconnect layer, and a second capacitor plate including at least a portion of the at least one MIM capacitor layer.

6. The method of claim 5, further comprising fabricating an additional MIM capacitor structure between the first upper interconnect layer and the second upper interconnect layer of the interconnect stack, the additional MIM capacitor structure comprising a first capacitor plate, a dielectric layer, and the first capacitor plate of the MIM capacitor structure as a second capacitor plate.

7. The method of claim 6, further comprising:  
coupling a first portion of the second upper interconnect layer to the first capacitor plate of the additional MIM capacitor structure; and  
coupling a second portion of the second upper interconnect layer to the second capacitor plate of the additional MIM capacitor structure.

8. The method of claim 5, further comprising integrating the capacitor into a cell phone, a hand-held personal communication system (PCS) unit, a set top box, a music player, a video player, an entertainment unit, a navigation device, a portable data unit, and/or a fixed location data unit.

9. A capacitor comprising:  
a first metal insulator metal (MIM) capacitor structure comprising a first capacitor plate and a first upper interconnect layer of an interconnect stack of an integrated circuit (IC) device as a second capacitor plate; and  
a second MIM capacitor structure between the first upper interconnect layer and a second upper interconnect layer of the interconnect stack, the second MIM capacitor

structure comprising a first capacitor plate, a dielectric layer, and the first capacitor plate of the first MIM capacitor structure as a second capacitor plate.

10. The capacitor of claim 9, in which a first portion of the second upper interconnect layer is coupled to the first capacitor plate of the second MIM capacitor structure and a second portion of the second upper interconnect layer is coupled to the second capacitor plate of the second MIM capacitor structure.

11. The capacitor of claim 9, further comprising a metal oxide metal (MOM) capacitor structure coupled to the first upper interconnect layer of the interconnect stack, the MOM capacitor structure comprising at least one lower interconnect layer of the interconnect stack.

12. The capacitor of claim 9, integrated into a cell phone, a hand-held personal communication system (PCS) unit, a set top box, a music player, a video player, an entertainment unit, a navigation device, a portable data unit, and/or a fixed location data unit.

13. A capacitor comprising:

a means for storing electric charge coupled to a first upper interconnect layer of an interconnect stack of an integrated circuit (IC) device, the charge storing means including at least one lower interconnect layer of the interconnect stack;

a second upper interconnect layer of the interconnect stack coupled to the electric charge storing means;

at least one metal insulator metal (MIM) capacitor layer between the first upper interconnect layer and the second upper interconnect layer; and

a MIM capacitor structure coupled to the electric charge storing means, the MIM capacitor structure comprising a first capacitor plate including at least a portion of the first upper interconnect layer, and a second capacitor plate including at least a portion of the at least one MIM capacitor layer.

14. The capacitor of claim 13, further comprising an additional MIM capacitor structure between the first upper interconnect layer and the second upper interconnect layer of the interconnect stack, the additional MIM capacitor structure comprising a first capacitor plate, a dielectric layer, and the first capacitor plate of the MIM capacitor structure as a second capacitor plate.

15. The capacitor of claim 14, in which a first portion of the second upper interconnect layer is coupled to the first capacitor plate of the additional MIM capacitor structure and a second portion of the second upper interconnect layer is coupled to the second capacitor plate of the additional MIM capacitor structure.

16. The capacitor of claim 13, integrated into a cell phone, a hand-held personal communication system (PCS) unit, a set top box, a music player, a video player, an entertainment unit, a navigation device, a portable data unit, and/or a fixed location data unit.

17. A method of fabrication a capacitor comprising:  
the step of forming a metal oxide metal (MOM) capacitor structure within lower interconnect layers of an interconnect stack of an integrated circuit (IC) device;  
the step of depositing at least one metal insulator metal (MIM) capacitor layer between a first upper interconnect layer and a second upper interconnect layer of the interconnect stack; and  
the step of forming a MIM capacitor structure coupled to the MOM capacitor structure, the MIM capacitor structure comprising a first capacitor plate including at least a portion of the first upper interconnect layer, and a second capacitor plate including at least a portion of the at least one MIM capacitor layer.

18. The method of claim 17, further comprising the step of fabricating an additional MIM capacitor structure between the first upper interconnect layer and the second upper interconnect layer of the interconnect stack, the additional MIM capacitor structure comprising a first capacitor plate, a dielectric layer, and the first capacitor plate of the MIM capacitor structure as a second capacitor plate.

19. The method of claim 18, further comprising:  
the step of coupling a first portion of the second upper interconnect layer to the first capacitor plate of the additional MIM capacitor structure; and  
the step of coupling a second portion of the second upper interconnect layer to the second capacitor plate of the additional MIM capacitor structure.

20. The method of claim 17, further comprising the step of integrating the capacitor into a cell phone, a hand-held personal communication system (PCS) unit, a

set top box, a music player, a video player, an entertainment unit, a navigation device, a portable data unit, and/or a fixed location data unit.

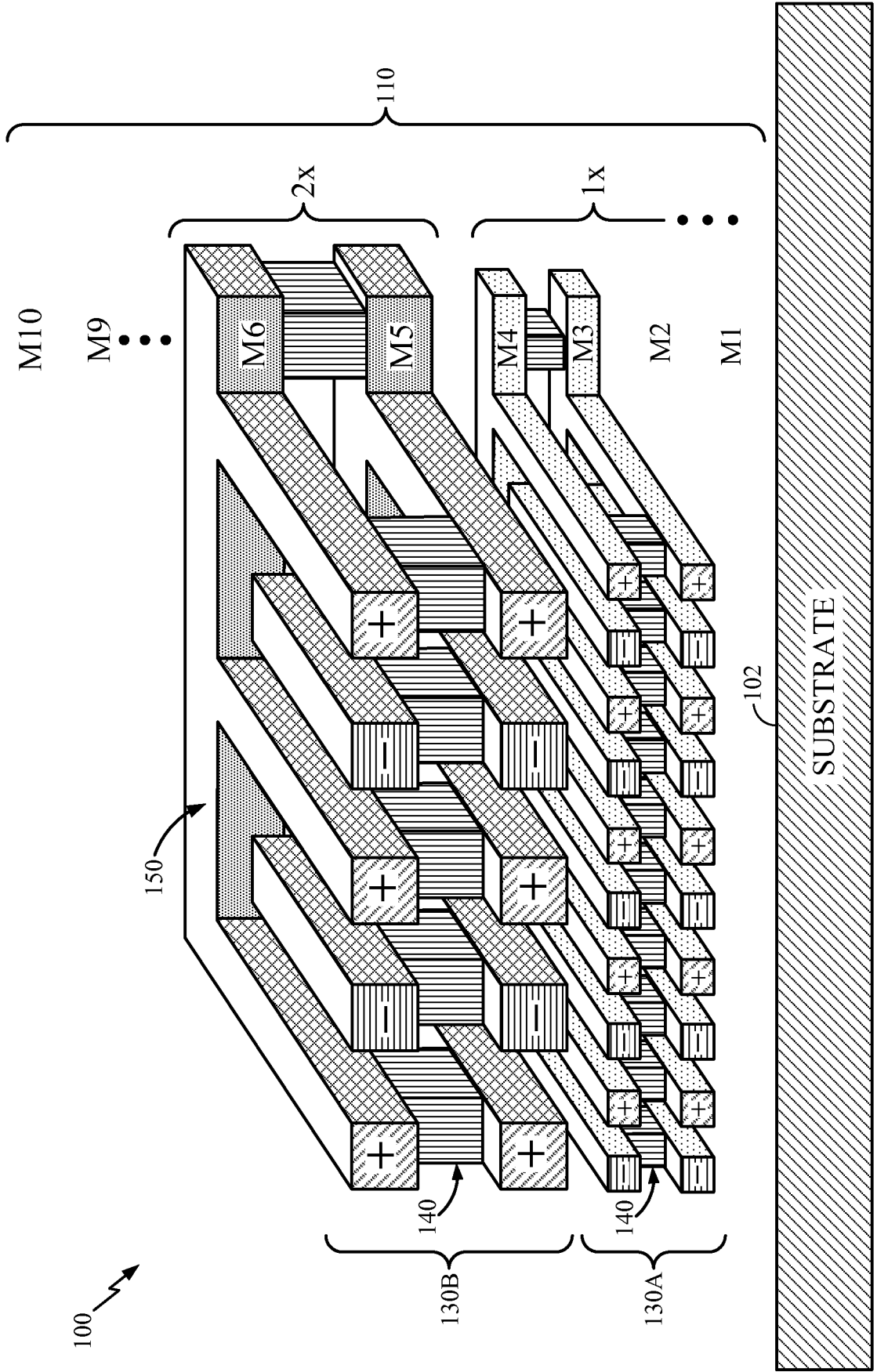


FIG. 1  
PRIOR ART

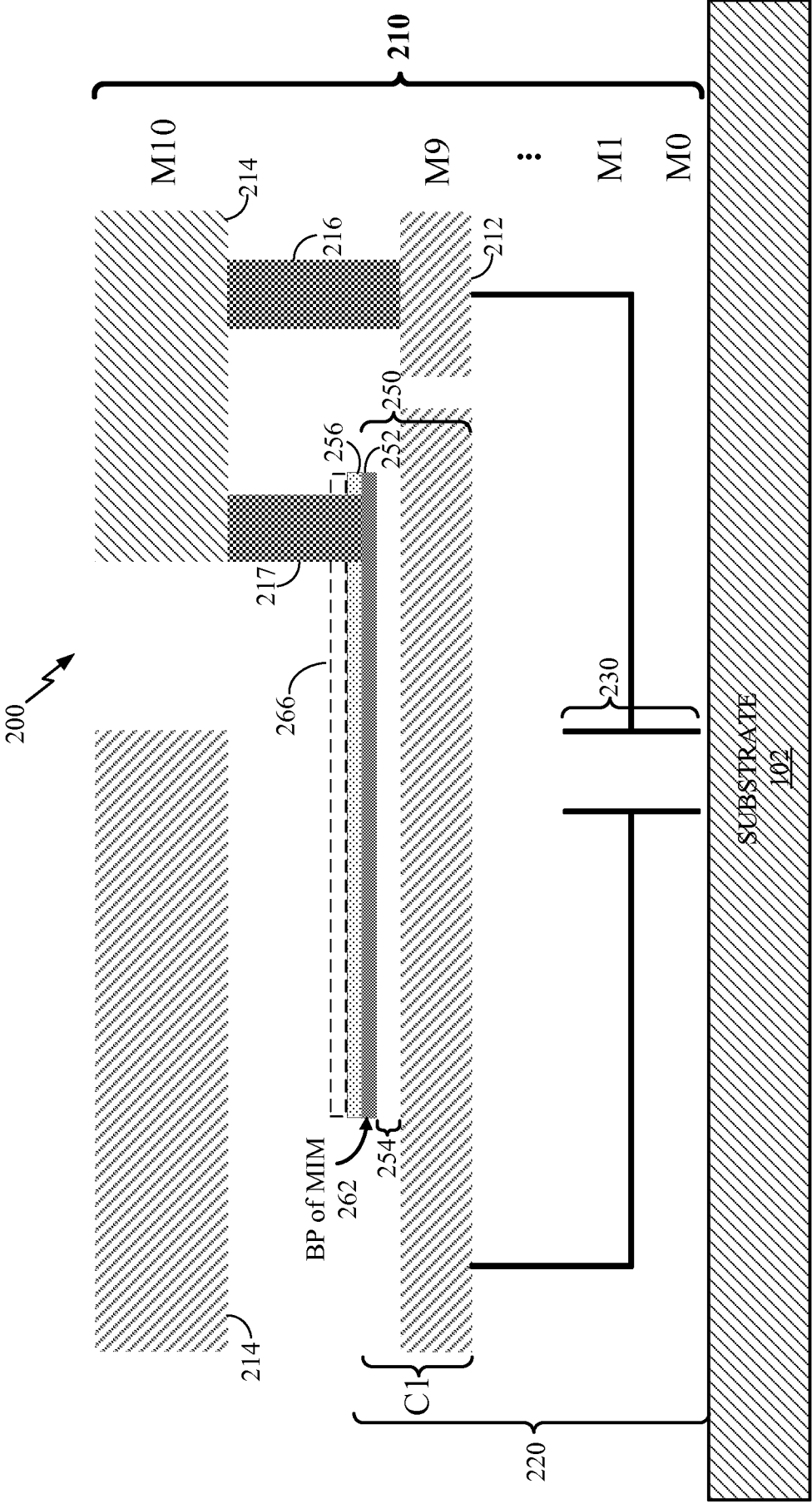


FIG. 2

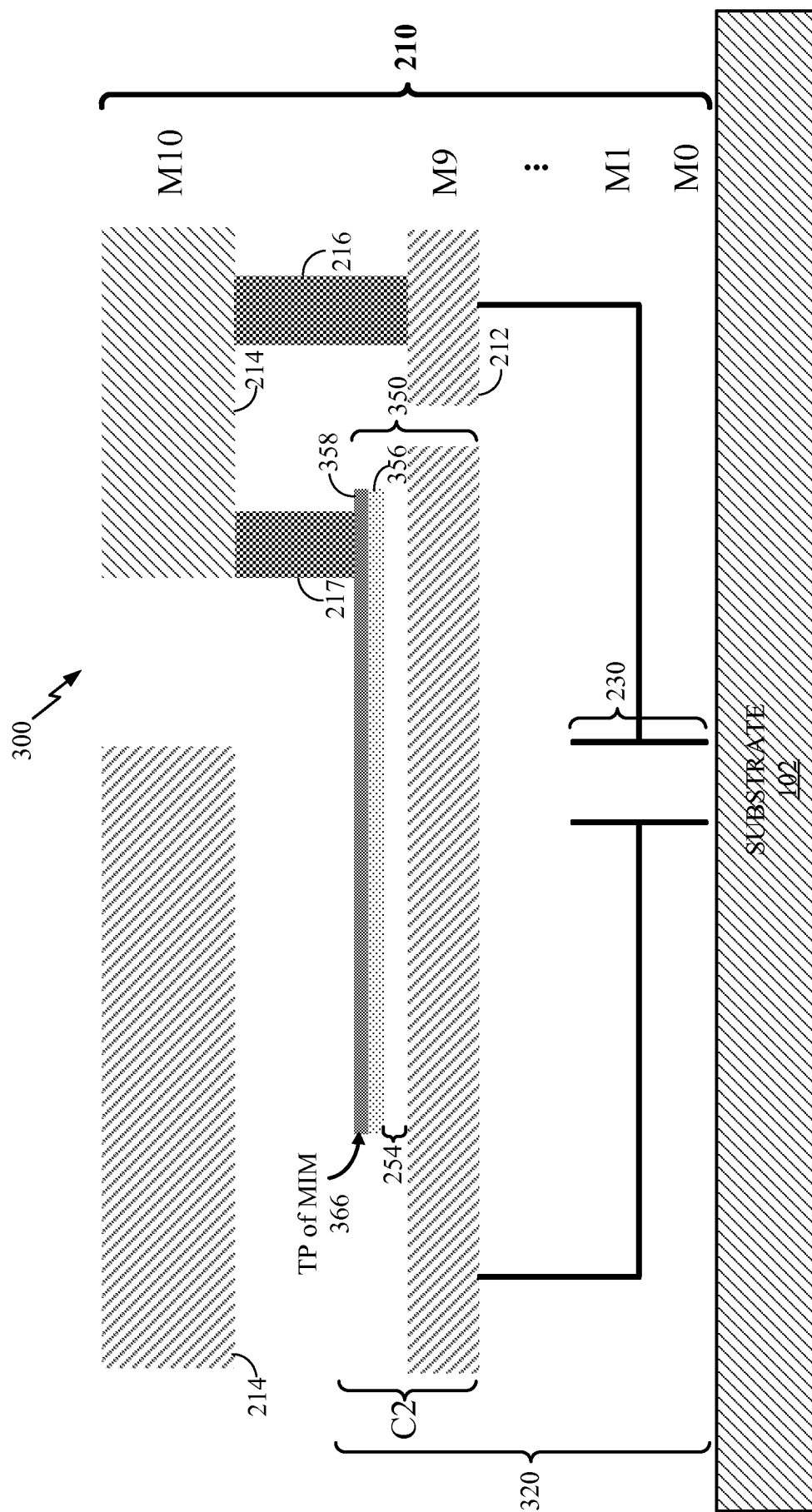


FIG. 3



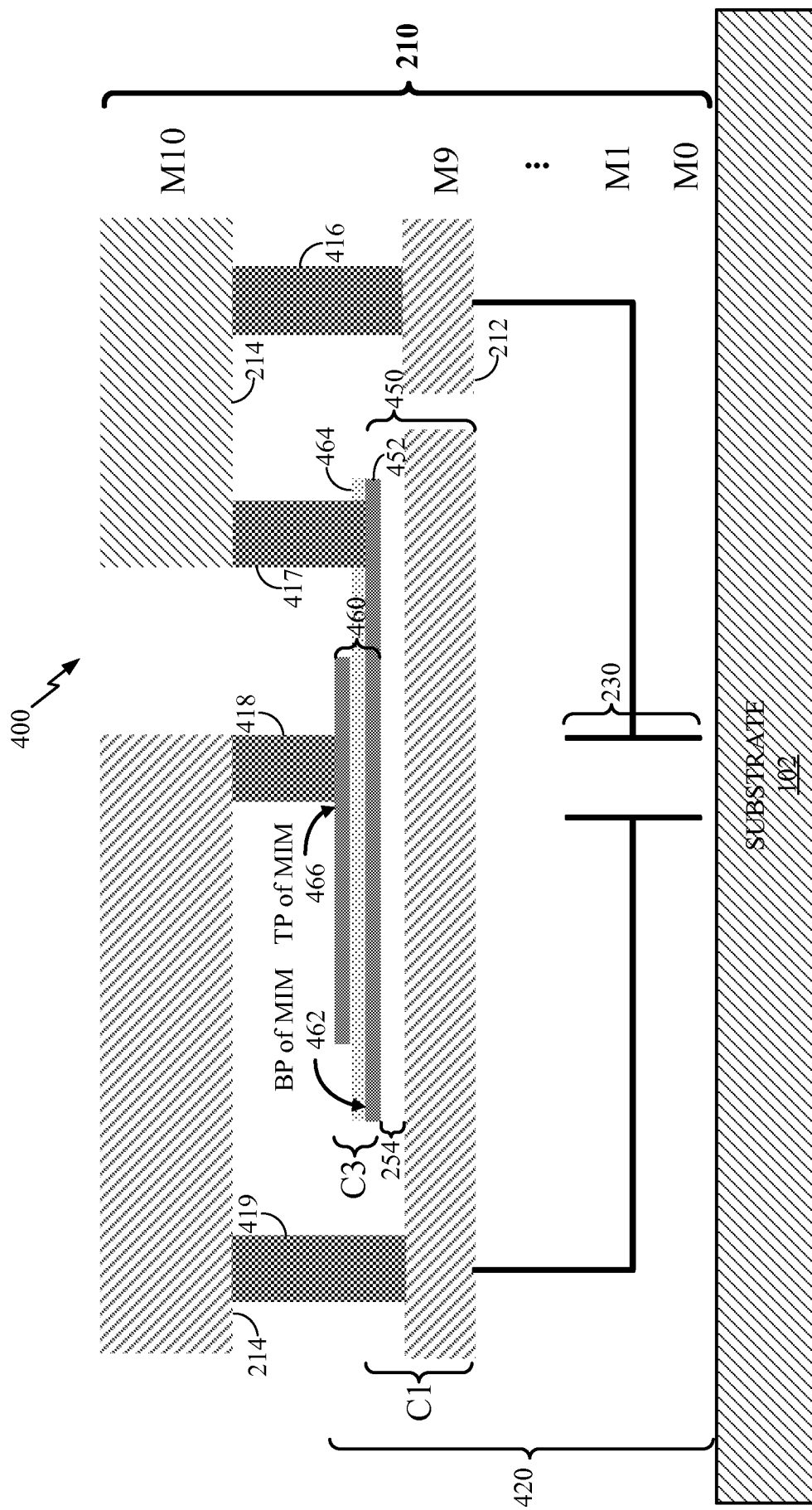


FIG. 4

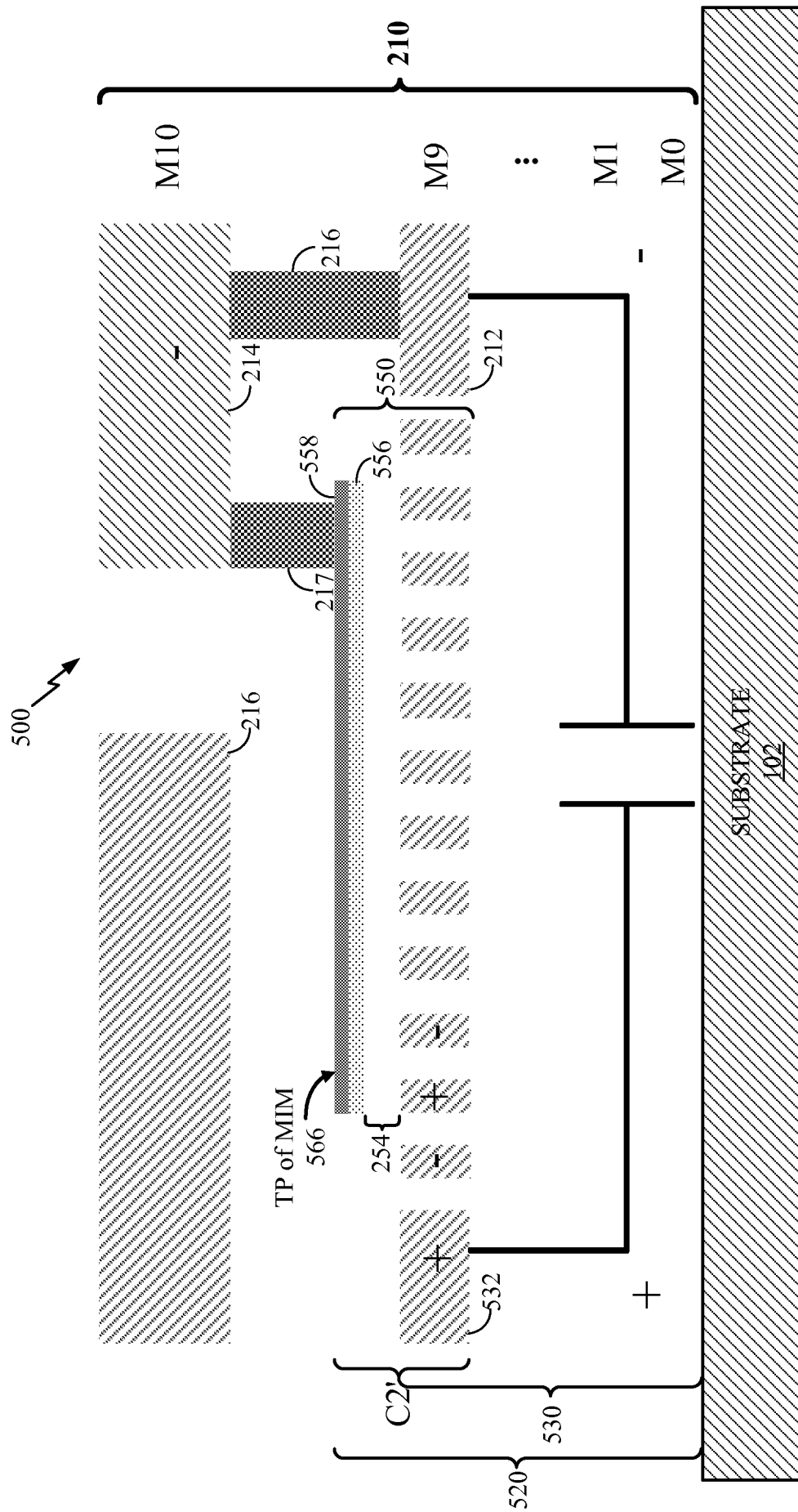


FIG. 5

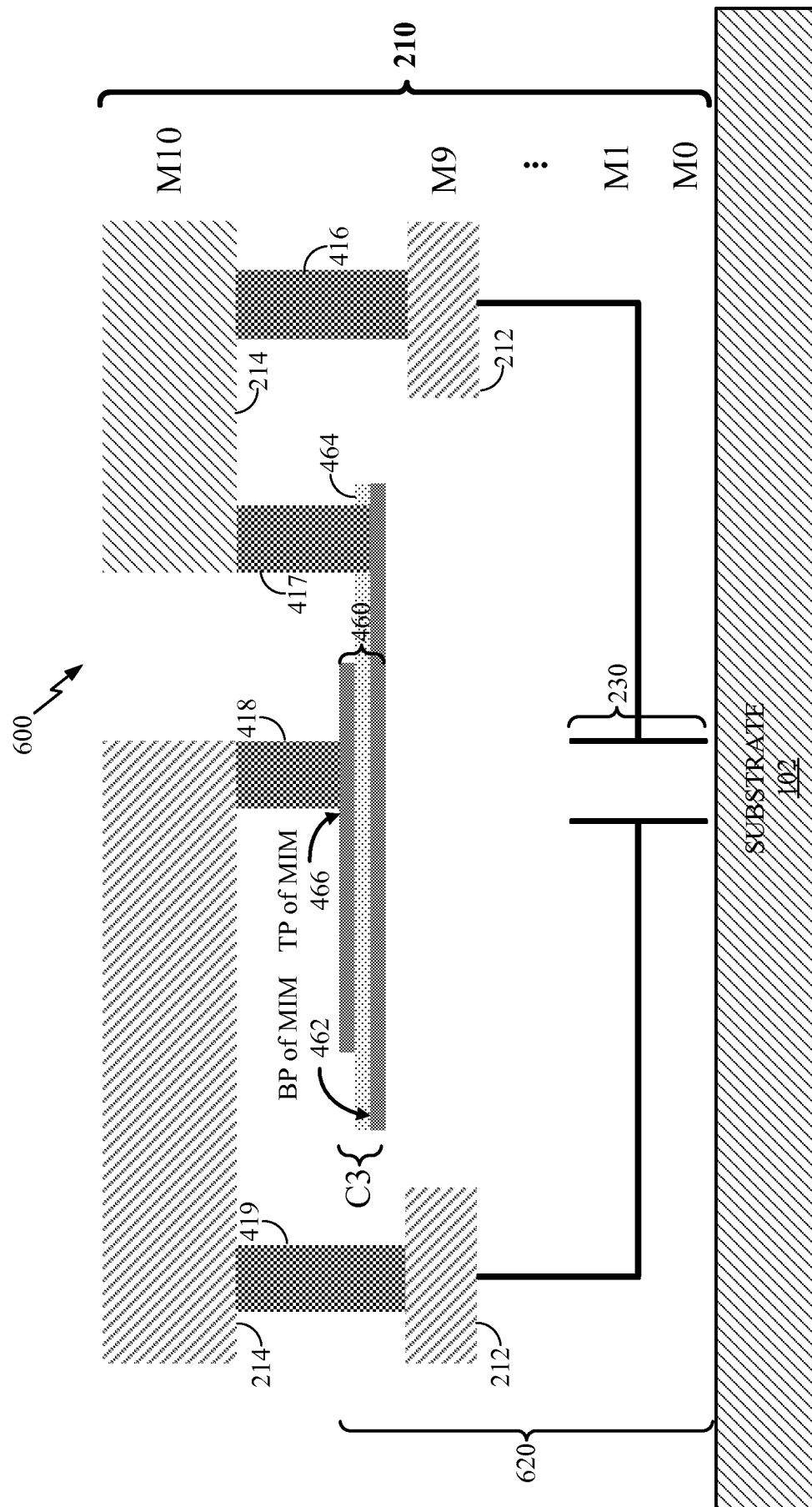


FIG. 6

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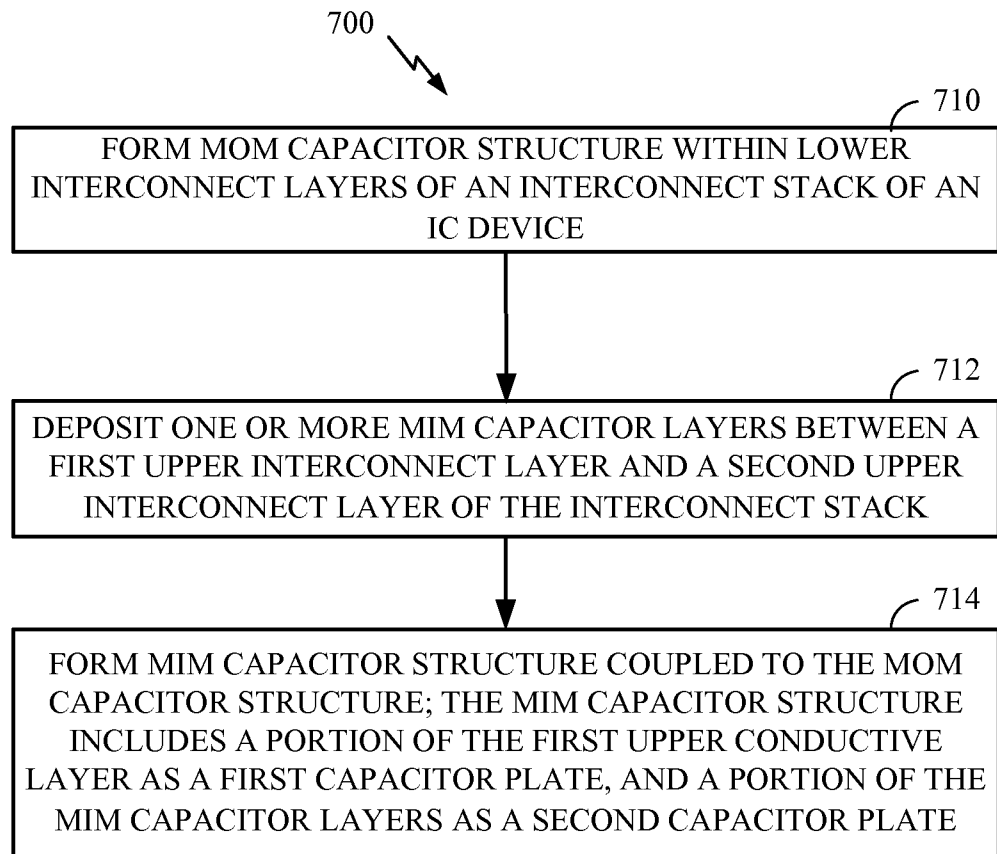


FIG. 7

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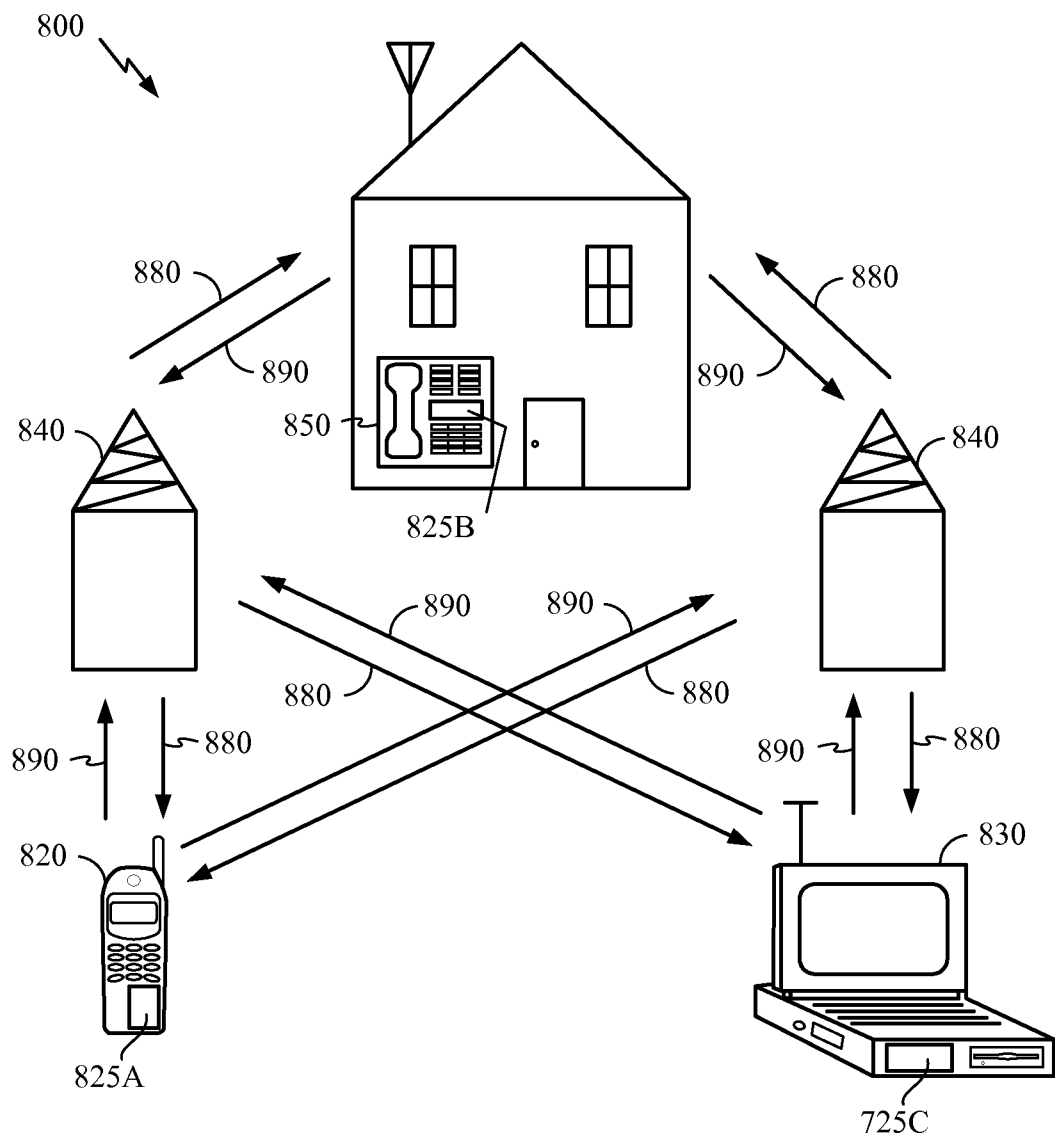


FIG. 8

## INTERNATIONAL SEARCH REPORT

International application No

PCT/US2014/015855

## A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L23/522  
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Further documents are listed in the continuation of Box C.



See patent family annex.

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"&amp;" document member of the same patent family

Date of the actual completion of the international search

20 June 2014

Date of mailing of the international search report

30/06/2014

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Authorized officer

Zeisler, Peter

## INTERNATIONAL SEARCH REPORT

International application No

PCT/US2014/015855

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 2006/180895 A1 (CHEN YUEH-YOU [TW] ET AL) 17 August 2006 (2006-08-17) paragraphs [0017] - [0021]; figure 1 -----	1,5,13, 17
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