(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 January 2001 (04.01.2001)

PCT

(10) International Publication Number
WO 01/01471 A1

(51) International Patent Classification[7]: H01L 21/311

(21) International Application Number: PCT/US00/16556

(22) International Filing Date: 14 June 2000 (14.06.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/340,743 28 June 1999 (28.06.1999) US

(71) Applicant: LAM RESEARCH CORPORATION [US/US]; Building CA-1, 4650 Cushing Parkway, Fremont, CA 94538 (US).

(72) Inventors: NI, Tuqiang; 5415 Ontario Common, Fremont, CA 94555 (US). TRAN, Nancy; 978 Junesong Way, San Jose, CA 95133 (US).

(74) Agent: BROCK, Joe, A.; Hickmann Stephens Coleman & Hughes, LLP, P.O. Box 52037, Palo Alto, CA 94303 (US).

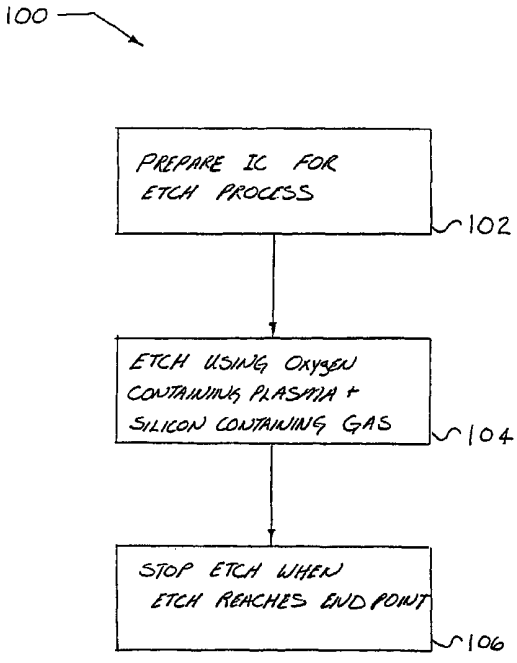
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*

[Continued on next page]

(54) Title: A METHOD AND APPARATUS FOR SIDE WALL PASSIVATION FOR ORGANIC ETCH



(57) Abstract: A robust method for etching an organic low-k insulating layer on a semiconductor device, as disclosed herein, includes introducing into a processing chamber a substrate with an organic insulating layer and an overlying mask layer having an aperture. A plasma is then developed within the chamber from an oxidizing gas and a passivation gas. The passivation gas is preferably either a silicon containing gas or a boron containing gas, or both. The ratio of the oxidizing gas to the passivation gas is preferably at least 10:1. In addition, an inert carrier gas may be provided. The plasma is then used to etch the organic insulating layer through the mask layer, thereby forming a via having essentially vertical sidewalls in the organic low-k insulating layer.

WO 01/01471 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

A METHOD AND APPARATUS FOR SIDE WALL PASSIVATION FOR ORGANIC ETCH

BACKGROUND OF THE INVENTION

The present invention relates generally to semiconductor processing and, more particularly to methods for etching organic insulating layers.

The present day semiconductor industry continually strives to increase device performance by reducing device dimensions and increasing device packing densities. For a given chip size, increasing the device packing density can be achieved by reducing the vertical and lateral distance separating active devices, with a resulting reduction in dielectric thickness (often referred to as inter-metal oxide or IMO) between layers. Unfortunately, reducing dielectric thickness increases interlayer capacitance, which results in diminished high frequency performance of the integrated circuit.

In integrated circuits, conventional insulating layers, such as silicon dioxide and silicon nitride, generally have dielectric constants "k" of about 3.9 and above. For example, the dielectric constant of silicon dioxide is about 3.9, and the dielectric constant of silicon nitride is about 9.0. As the feature scales shrink in IC devices it becomes desirable to reduce the dielectric constant of the insulating layer to reduce the inter-layer capacitance.

Since the dielectric constant "k" of some organic materials, such as FLARE from AlliedSignal, Inc. and SiLK from Dow Chemical, is generally less than 2.7, organic materials can be used as a low-k organic insulating layers for chip fabrication. However, the organic materials present problems during a conventional etch process. Most notably, etching organic materials using conventional methods results in the organic insulating layer having via sidewalls that are undercut and bowed.

Figure 1A is an illustration showing a cross-sectional view of a prior art integrated circuit structure 10 having an organic insulating layer 12 prior to a plasma etch. More particularly, integrated circuit structure 10 includes an organic insulating layer 12, a silicon dioxide hardmask layer 14 disposed above the organic insulating layer 12, and an organic resist mask 16 formed

above the silicon dioxide hardmask layer 14. Figure 1B shows the integrated circuit structure 10 after etching the silicon dioxide hardmask layer 14 by a suitable oxide-etch process though the resist mask 16. Figure 1C shows the integrated circuit structure 10 after etching ("oxidizing") the organic insulating layer 12 using conventional oxygen containing gases. A conventional etch of organic low-k materials in a plasma chamber typically employs oxygen containing gases such as O_2, CO_2, and SO_2. In the presence of plasma, oxygen atoms and ions are formed. Atomic oxygen reacts with organic material and forms CO, H_2O, and CO_2 as by products. However, spontaneous reactions between the atomic oxygen and the organic low-k materials occur. The reactions between the atomic oxygen and the organic low-k insulating layer cause isotropic etching, which results in undercut and bowing of the organic insulating layer 12 as illustrated by the bowed profile of sidewalls 18.

To counter undercut and bowing in the sidewalls 18, gases such as C_2H_4 are sometimes used during organic etch. Figure 1D shows the integrated circuit structure 10 after etching the organic insulating layer 12 using C_2H_4 containing gases. The C_2H_4 forms a C_xH_y polymer on the etch sidewall during the etch process. The result is a sidewall 18 which is sometimes less undercut and bowed than the sidewall profile resulting from conventional oxygen containing gases. However, this approach is difficult to control, and does not always result in an improved sidewall 18 profile. The amount of improvement depends on the parameters used to control the sidewall 18 profile, resulting in an approach which is delicate and lacking robustness.

Another approach used to counter undercut and bowing in the sidewall 18 profile during an organic etch is the use of high energy sputtering. Prior art Figure 1E shows the integrated circuit structure 10 after etching the organic insulating layer 12 using high energy sputtering. The high energy sputtering causes sputtering of SiO_2 from the silicon dioxide hardmask layer 14 to create sidewall passivation. However, the high energy sputtering can cause damage 20 to the hardmask layer 14 during the etch process. In addition, when a deep etch is needed, high energy sputtering is often insufficient to cause sidewall passivation coating near the bottom of the via, again resulting in an undercut and bowed sidewall 18 profile.

All of the organic etch approaches discussed above fail to provide a consistent, robust etch process which provides a sidewall profile in an organic insulating layer that is not undercut or bowed. Accordingly, there exist a need for a robust organic etch process that does not cause damage to the IC, and provides better sidewall profiles.

SUMMARY OF THE INVENTION

The present invention meets the aforementioned requirements by providing a process that etches organic insulating layers utilizing an oxidizing gas and a passivation gas. The passivation gas reacts with oxygen atoms or oxygen molecules to form a nonvolatile passivation film which deposits on the sidewalls of vias being formed in the organic insulating layer. The passivation film provides sidewall passivation which essentially inhibits isotropic etch of the organic insulating layer. Thus, the resultant via sidewall profile in the organic insulating layer is essentially vertical with respect to the plane of the insulating layer.

One aspect of the present invention teaches a method for anisotropically etching an organic insulating layer through an aperture in a mask layer. A substrate, with an organic insulating layer and an overlying mask layer having an aperture, is introduced into a processing chamber. A plasma is then developed within the chamber from an oxidizing gas and a passivation gas. The passivation gas is preferably either a silicon containing gas or a boron containing gas, or both. The ratio of the oxidizing gas to the passivation gas is preferably at least 10:1. An inert carrier gas may also be provided. The plasma is then used to etch the organic insulating layer through the mask layer.

Another aspect of the present invention teaches an etch system for organic layers. The organic etch system includes a chamber which is receptive to a substrate provided with an organic insulating layer to be etched. Also included is a gas inlet mechanism connecting an oxidizing gas and a passivation gas source. The passivation gas is derived from the group including silicon containing gases and boron containing gases. The ratio of the oxidizing gas to the passivation gas is preferably at least 10:1. Further included in the system is a pair of electrodes disposed within the chamber, and an RF generator coupled to the electrode pair so that a plasma is formed with the oxidizing gas and the passivation gas which etches exposed portions of the organic insulating layer.

As stated above, the present invention has the ability to produce accurate vias having essentially vertical sidewall profiles in organic insulating layers. The ability to produce accurate vias allows the use of organic low-k insulating layers in integrated circuit fabrication. The organic low-k insulating layers lower the interlayer capacitance, and thereby increase high frequency performance of the integrated circuit.

These and other advantages of the present invention will become apparent to those skilled in the art upon a reading of the following descriptions and a study of the various figures of the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention, together with further advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawings in which:

FIGURE 1A is an illustration showing a cross-sectional view of a prior art integrated circuit structure prior to a plasma etch;

FIGURE 1B is an illustration showing a cross-sectional view of the prior art integrated circuit structure after etching the silicon dioxide layer;

FIGURE 1C is an illustration showing a cross-sectional view of the prior art integrated circuit structure after etching the organic insulating layer using conventional oxygen containing gases;

FIGURE 1D is an illustration showing a cross-sectional view of the prior art integrated circuit structure after etching the organic insulating layer using C_2H_4 containing gases;

FIGURE 1E is an illustration showing a cross-sectional view of the prior art integrated circuit structure after etching the organic insulating layer using high energy sputtering;

FIGURE 2A is an illustration showing a cross-sectional view of an integrated circuit structure prior to a plasma etch in accordance with a preferred embodiment of the present invention;

FIGURE 2B is an illustration showing a cross-sectional view of an integrated circuit structure after etching the silicon dioxide layer in accordance with a preferred embodiment of the present invention;

FIGURE 2C is an illustration showing a cross-sectional view of an integrated circuit structure after etching the organic insulating layer using a silicon containing passivation gas in accordance with a preferred embodiment of the present invention;

FIGURE 3 is a flow chart showing a method for etching an organic insulating layer in accordance with one embodiment of the present invention;

FIGURE 4 is an illustration showing an organic insulating layer etching system in accordance with one embodiment of the present invention; and

FIGURE 5 is an illustration showing an organic insulating layer etching system having multiple gas inlets in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figures 1A-1E were described in terms of the prior art. A preferred embodiment of the present invention will now be described with reference to Figures 2A-2C. Figure 2A is an illustration showing an integrated circuit structure 30 prior to plasma etch in accordance with a preferred embodiment of the present invention. The integrated circuit 30 includes an organic low-k insulating layer 32, a silicon dioxide layer 34 disposed above the organic low-k insulating layer 32, and an organic resist mask 36 formed above the silicon dioxide layer 34.

A process in accordance with the present invention begins with an etch of the silicon dioxide layer 34 preferably utilizing a gas such as CF_4. Other gases such as C_2F_6, CHF_3, and SF_6 are also suitable for use in the etching process. Process parameters for etching silicon dioxide are well known to those skilled in the art. The result of the etch is shown in Figure 2B.

After etching the silicon dioxide layer 34, a mixture of a passivation gas and an oxidizing gas are formed into a plasma to anisotropically etch the organic insulating layer 32 through an aperture 35 in the silicon dioxide layer 34. Figure 2C is an illustration showing the integrated circuit structure 30 after etching the organic low-k insulating layer 32 using a passivation gas added to an oxygen containing plasma. The passivation gas can be either a silicon containing gas, such as SiH_4, SiF_4, or $SiCl_4$, or a boron containing gas, such as BCl_3.

More particularly, plasma including a passivation gas and an oxidizing gas is used to etch vias in the organic low-k insulating layer 32. The passivation gas reacts with oxygen atoms or oxygen molecules to form a nonvolatile passivation film 38 during this process. The type of passivation film 38 is determined by the type of passivation gas utilized, for example, silicon containing gases result in an SiO_2 passivation film, while boron containing gases result in a B_2O_2 passivation film. The passivation film 38 deposits on the sidewalls of the vias 39 as they form in the organic low-k insulating layer 32. Normally, spontaneous reactions between atomic oxygen from the plasma and the organic insulating layer cause isotropic etching, which results in undercut and bowing in the sidewall 40 profile. However, the sidewall passivation film 38 of the present invention provides sidewall passivation which essentially inhibits isotropic etch resulting from spontaneous reactions between atomic oxygen and the organic insulating layer. Thus, the sidewall 40 profile of the present invention is essentially vertical with respect to the plane of the insulating layer.

Referring next to Figure 3, a method 100 for etching an organic low-k insulating layer in accordance with one embodiment of the present invention will now be described. In an initial

operation 102, an integrated circuit is prepared for the organic insulating layer etch process. Typically, this preparation includes etching the silicon dioxide layer with a fluorocarbon-containing gas such as CF_4, C_2F_6, CHF_3, and/or SF_6. As will be apparent to those skilled in the art, fluorine from the fluorocarbon-containing gas reacts with the silicon in the silicon dioxide layer during the etch process. The actual process parameters for etching silicon dioxide are also well know to those skilled in the art. Having etched the silicon dioxide layer, the integrated circuit structure is then ready for the organic insulating layer etch.

The method 100 continues with an organic insulating layer etch, in an operation 104. After etching the silicon dioxide layer, a mixture of a passivation gas and an oxidizing gas are formed into a plasma to anisotropically etch the organic insulating layer through an aperture in the silicon dioxide layer. The passivation gas can be either a silicon containing gas, such as SiH_4, SiF_4, or $SiCl_4$, or a boron containing gas, such as BCl_3. In addition, the oxygen to passivation gas ratio in the plasma preferably does not exceed 10:1. However, during an organic insulating layer etch having a longer etch time, the oxygen to passivation gas ratio is typically about 100:1, in order to avoid over passivation of the via sidewalls. Over passivation of via sidewalls may cause etch stop and sloped via sidewalls from passivation film buildup, and therefore should be avoided. On the other hand, during a highly active organic insulating layer etch having a shorter etch time, the oxygen to passivation gas ratio is typically about than 50:1, in order to avoid under passivation of the via sidewalls. Using these ratios of oxygen containing gas to silicon containing gas, the organic etch rate is in the range of about 0.4-2.0 μ/min, resulting in an organic layer etch time of between 1-2 minutes.

To elaborate further, the plasma, including the passivation gas and the oxidizing gas, is used to etch vias in the organic low-k insulating layer. The passivation gas reacts with oxygen atoms or oxygen molecules to form a nonvolatile passivation film. The type of passivation film formed is determined by the type of passivation gas utilized in the plasma. For example, silicon containing gases result in an SiO_2 passivation film, while boron containing gases result in a B_2O_2 passivation film. The passivation film deposits on the sidewalls of the vias as they form in the organic insulating layer. Normally, spontaneous reactions between atomic oxygen from the plasma and the organic insulating layer cause isotropic etching which results in undercut and bowing in the sidewall profile. However, the sidewall passivation film of the present invention provides sidewall passivation which essentially inhibits isotropic etch resulting from spontaneous reactions between atomic oxygen and the organic low-k insulating layer. Thus, the sidewall profile of the present invention is essentially vertical with respect to the plane of the insulating layer.

Finally, in an operation 106, the organic low-k insulating layer etch process is stopped when the etch reaches an end point. Dry etch equipment used in a typical semiconductor production environment requires the availability of effective diagnostic and etch end point detection tools. Four common methods for determining the end point of dry etch processes are: laser reflectivity; optical emission spectroscopy; direct observation of the etched surface through a viewing port on the chamber, by a human operator; and mass spectroscopy.

Plasma etching systems as described above consist of several components. Figure 4 is an illustration showing an organic insulating layer etching system 50 in accordance with one embodiment of the present invention. The organic insulating layer etching system 50 includes a chamber 52 receptive to a substrate 62 provided with an organic insulating layer to be etched, a gas inlet mechanism 54 connecting to an oxidizing gas and a passivation gas source 56, a pair of electrodes 58 disposed within the chamber 50, and an RF generator 60 coupled to the electrodes 58. In some instances the upper electrode can by omitted by grounding the RF generator 60 to the chamber 52.

After the substrate 62 is prepared for the organic low-k insulating layer etch, it is placed in the chamber 52. The gas inlet mechanism 54 is then used to release, into the chamber 52, the oxidizing gas and the passivation gas from the gas source 56. The RF generator 60 is then used to create a plasma 61 containing the oxidizing and passivation gases in the chamber 52. The passivation gas reacts with oxygen atoms, molecules, or ions to form a nonvolatile passivation film on via sidewalls. The type of passivation film formed is determined by the type of passivation gas utilized. For example, silicon containing gases result in a SiO_2 passivation film, while boron containing gases result in a B_2O_2 passivation film. The passivation film deposits on the via sidewalls formed in the organic insulating layer of the substrate 62. Normally, spontaneous reactions between atomic oxygen from the plasma and the organic low-k insulating layer cause isotropic etching which results in undercut and bowing in the sidewall profile. However, the sidewall passivation film of the present invention provides sidewall passivation which essentially inhibits isotropic etch resulting from spontaneous reactions between atomic oxygen and the organic insulating layer. Thus, the sidewall profile of the present invention is essentially vertical with respect to the plane of the organic insulating layer.

In another embodiment of the present invention, the oxidizing and passivation gases are kept separate until released into the plasma containing chamber 52. Figure 5 is an illustration showing an organic insulating layer etching system 70 having multiple gas inlets in accordance with one embodiment of the present invention. The organic insulating layer etching system 70

includes a chamber 52 receptive to a substrate 62 provided with an organic low-k insulating layer to be etched, multiple gas inlet mechanisms 54 connecting to an oxidizing gas source 56A and a passivation gas source 56B, a pair of electrodes 58 disposed within the chamber 50, and an RF generator 60 coupled to the electrodes 58. As described above, in some cases the upper electrode can be omitted by grounding the RF generator 60 to the chamber 52.

Some passivation gases, such as SiF_4 and $SiCl_4$ can be premixed with the oxidizing gas before being released into the plasma containing chamber 52. In such cases, the organic insulating layer etching system only requires a single gas inlet 54 and gas source 56, as shown in Figure 4. However, some passivation gases, such as SiH_4, cannot be premixed with the oxidizing gas before being released in the plasma containing chamber 52, because such passivation gases will react with the oxygen before being released into the plasma. In these cases, multiple gas inlets 54 and gas sources 56A, 56B are needed. One gas source 56A contains the oxidizing gas, while the other gas source 56B contains the passivation gas. The gas inlet mechanisms 54 are then used to release the oxidizing gas and the passivation gas into the plasma containing chamber 52 in the proper ratio, usually under automated (e.g., computer) control. The oxygen to passivation gas ratio in the plasma preferably does not exceed 10:1. However, during an organic insulating layer etch having a longer etch time, the oxygen to passivation gas ratio is typically about than 100:1, in order to avoid over passivation of the via sidewalls. On the other hand, during a highly active organic insulating layer etch having a shorter etch time, the oxygen to passivation gas ratio is typically about than 50:1, in order to avoid under passivation of the via sidewalls. Using these ratios of oxygen containing gas to silicon containing gas, the organic etch rate is in the range of about 0.4-2.0 μ/min, resulting in an organic layer etch time of between 1-2 minutes.

While this invention has been described in terms of several preferred embodiments, there are many alterations, permutations, and equivalents which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

What is claimed is:

CLAIMS

1. A method for anisotropically etching an organic insulating layer through an aperture in a mask layer, comprising:

introducing a substrate provided with an organic insulating layer and an overlying mask layer having an aperture into a processing chamber; and

creating a plasma within said chamber having components derived from an oxidizing gas and a passivation gas, wherein the passivation gas is derived from the group consisting essentially of silicon containing gasses and boron containing gasses, wherein the ratio of said oxidizing gas to said passivation gas is at least 10:1, whereby said organic insulating layer is etched through said aperture in said mask layer.

2. A method as recited in claim 1, wherein the ratio of said oxidizing gas to said passivation gas is at least 50:1.

3. A method as recited in claim 1, wherein the ratio of said oxidizing gas to said passivation gas in at least 100:1

4. A method as recited in claim 1, wherein the passivation gas is SiF_4.

5. A method as recited in claim 1, wherein the passivation gas is $SiCl_4$.

6. A method as recited in claim 1, wherein the passivation gas is SiH_4.

7. A method as recited in claim 1, wherein the passivation gas is BCl_3.

8. A method as recited in claim 1, wherein the overlying mask includes a plurality of apertures.

9. An etch system for organic insulating layers comprising:

a chamber receptive to a substrate provided with an organic insulating layer to be etched;

a gas inlet mechanism connecting an oxidizing gas and a passivation gas source, wherein said passivation gas is derived from the group consisting essentially of silicon containing gasses and boron containing gasses, such that the ratio of said oxidizing gas to said passivation gas is at least 10:1;

at least one electrode disposed within said chamber; and

an RF generator coupled to said at least one electrode, whereby a plasma is formed with said oxidizing gas and said passivation gas which etches exposed portions of said organic insulating layer.

10. A system as recited in claim 9, further comprising a plurality of gas inlet mechanisms connecting a separate oxidizing gas source and a separate passivation gas source.

11. A system as recited in claim 10, wherein the gas inlet mechanisms release the oxidizing gas and the passivation gas into the chamber such that the ratio of oxidizing gas to passivation gas is at least 10:1.

12. A system as recited in claim 9, wherein the ratio of said oxidizing gas to said passivation gas is at least 50:1.

13. A system as recited in claim 9, wherein the ratio of said oxidizing gas to said passivation gas in at least 100:1

14. A system as recited in claim 9, wherein the passivation gas is SiF_4.

15. A system as recited in claim 9, wherein the passivation gas is $SiCl_4$.

16. A system as recited in claim 9, wherein the passivation gas is SiH_4.

17. A system as recited in claim 9, wherein the passivation gas is BCl_3.

18. A method for making an integrated circuit structure having an organic dielectric layer provided with a via having essentially vertical sidewalls, comprising:

introducing a substrate provided with an organic insulating layer and an overlying mask layer having an aperture into a processing chamber; and

creating a plasma within said chamber having components derived from an oxidizing gas and a passivation gas, said passivation gas derived from the group consisting essentially of silicon containing gasses and boron containing gasses, wherein the ratio of said oxidizing gas to said passivation gas is at least 10:1, whereby said organic insulating layer is etched through said aperture in said mask layer.

19. A method as recited in claim 18, wherein the ratio of said oxidizing gas to said passivation gas is at least 50:1.

20. A method as recited in claim 18, wherein the ratio of said oxidizing gas to said passivation gas in at least 100:1.

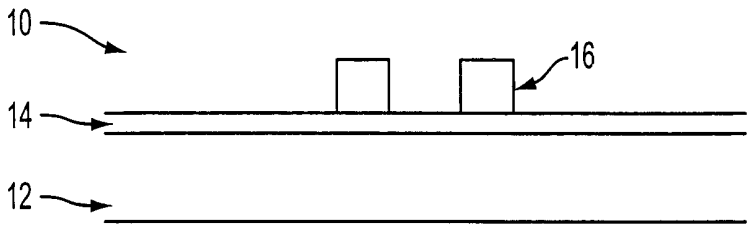


FIG. 1A
(PRIOR ART)

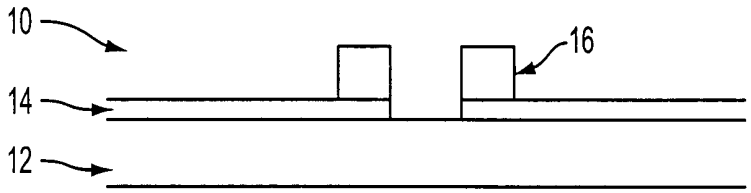


FIG. 1B
(PRIOR ART)

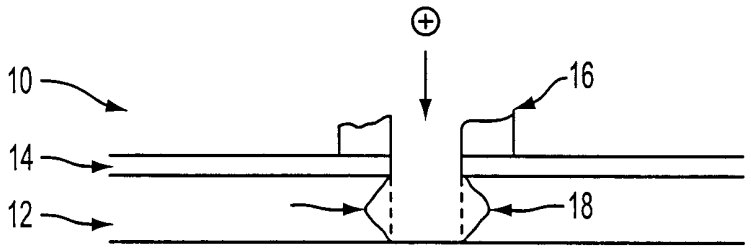


FIG. 1C
(PRIOR ART)

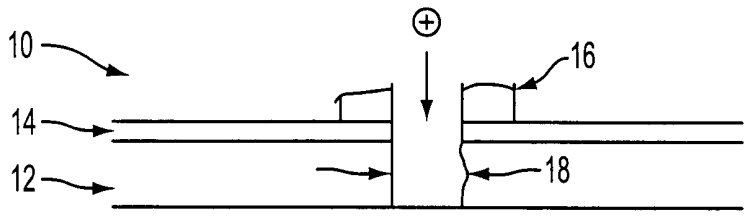


FIG. 1D
(PRIOR ART)

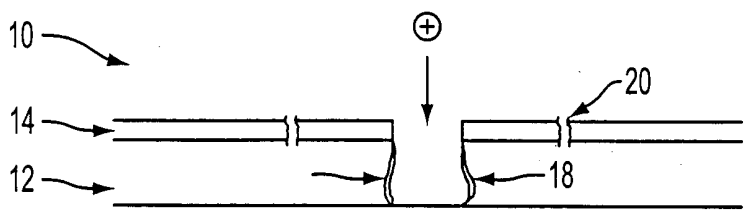


FIG. 1E
(PRIOR ART)

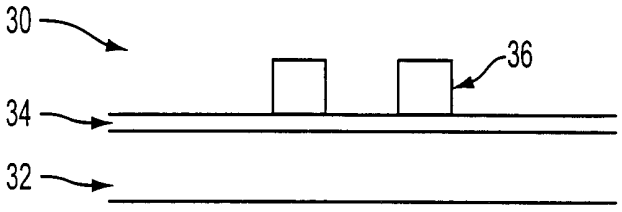


FIG. 2A

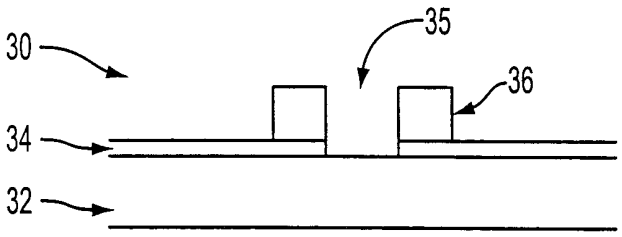


FIG. 2B

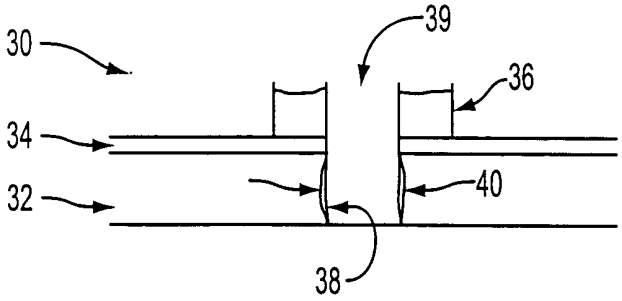


FIG. 2C

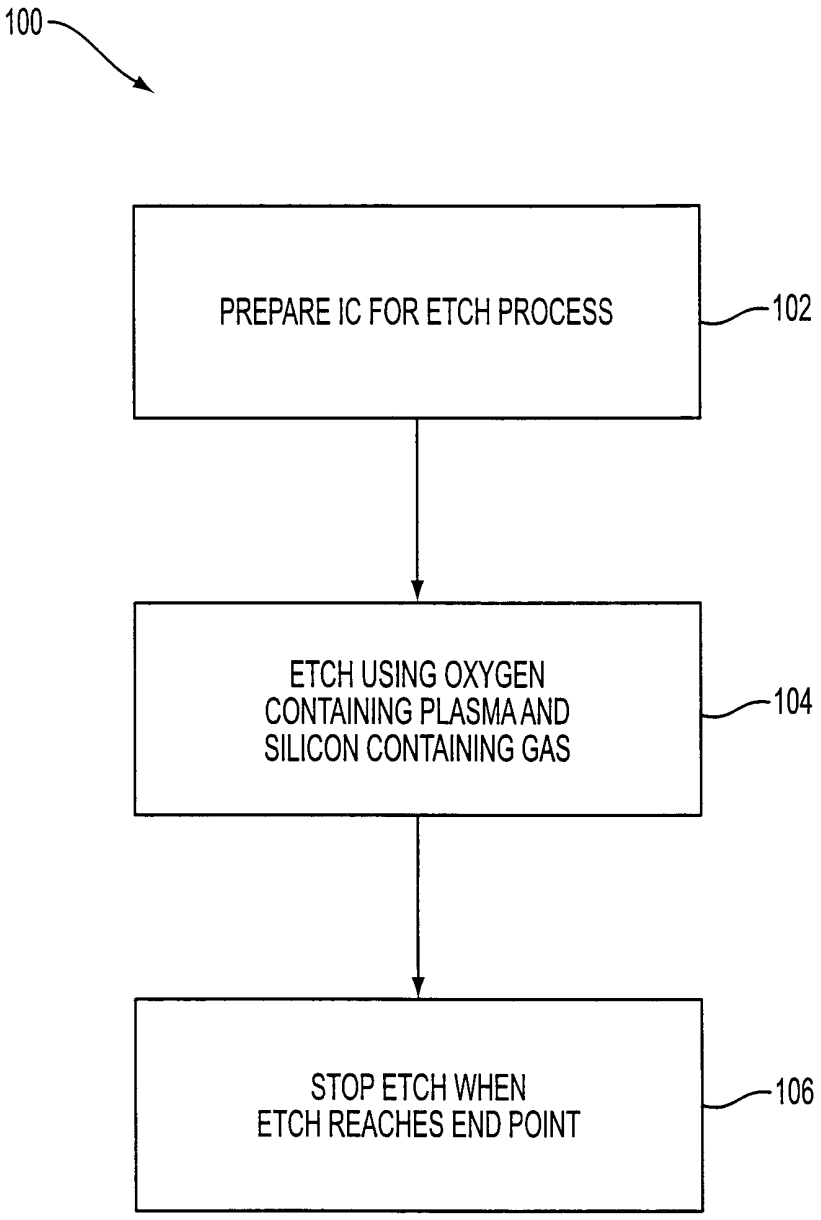

100
PREPARE IC FOR ETCH PROCESS
102
ETCH USING OXYGEN CONTAINING PLASMA AND SILICON CONTAINING GAS
104
STOP ETCH WHEN ETCH REACHES END POINT
106

FIG. 3

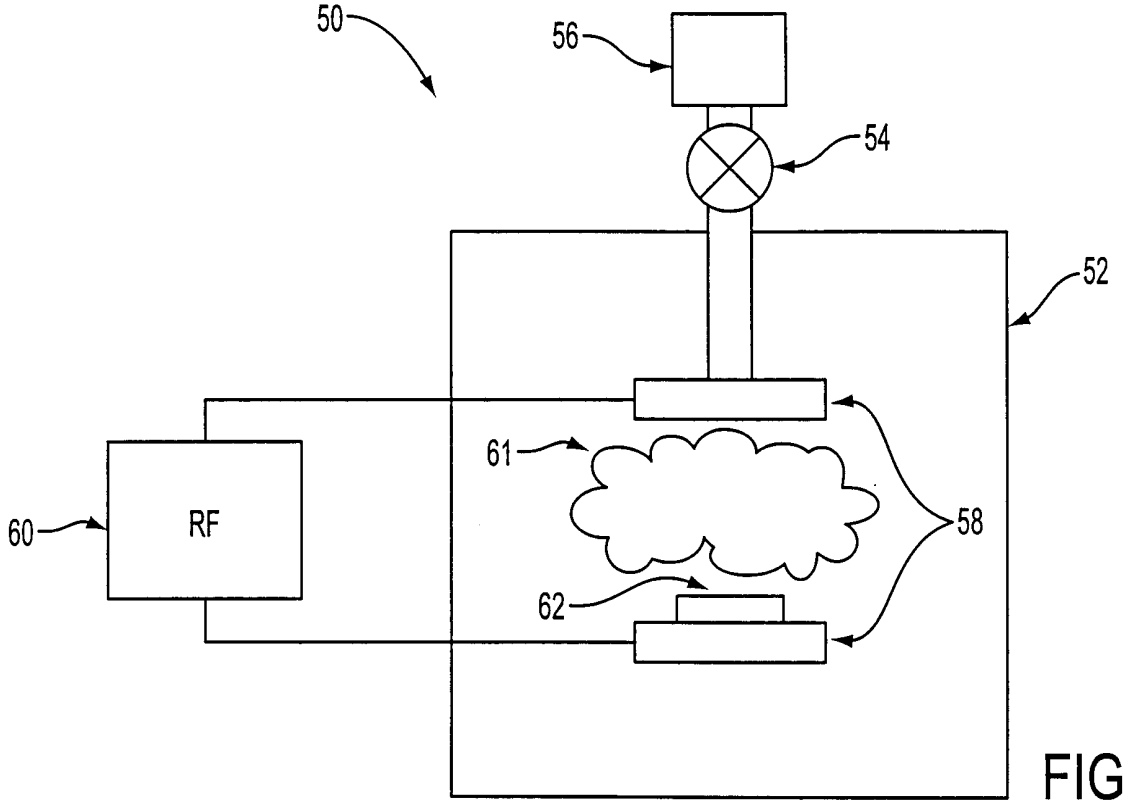


FIG. 4

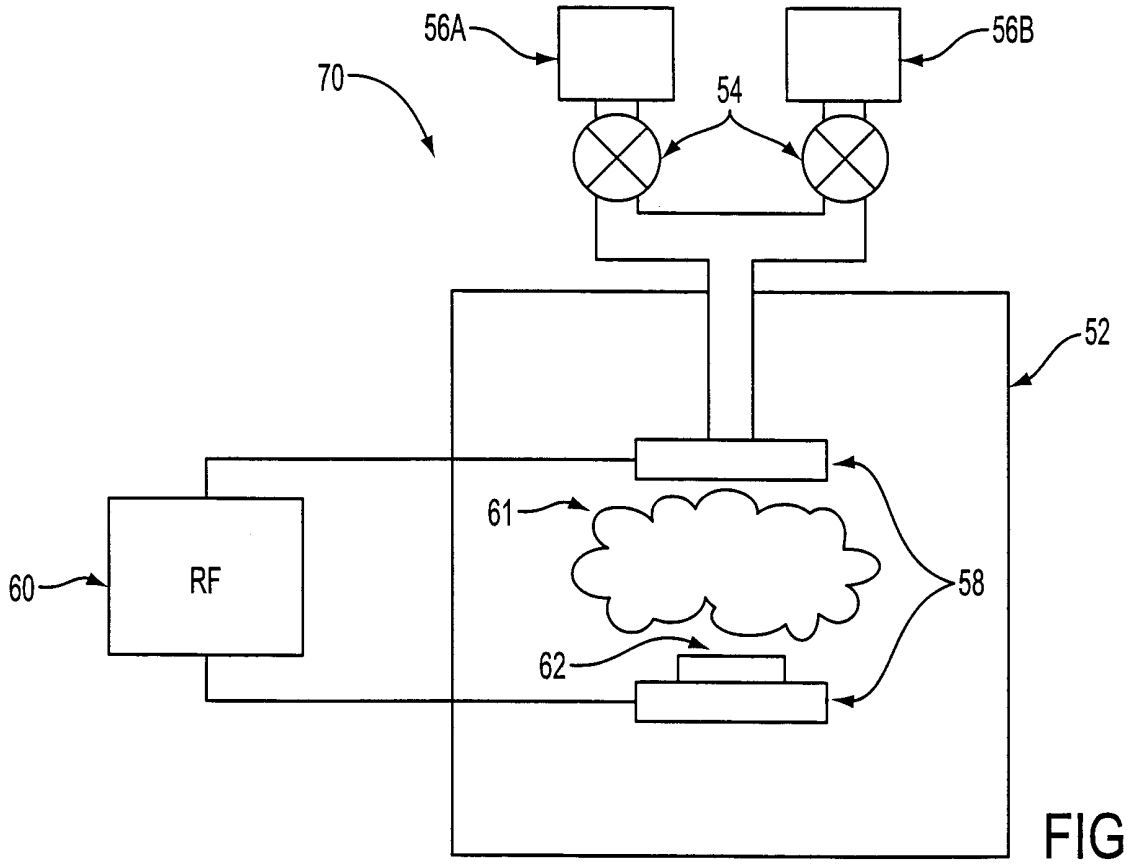


FIG. 5

INTERNATIONAL SEARCH REPORT

In. ational Application No
PCT/US 00/16556

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/311

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 10, 31 August 1998 (1998-08-31) -& JP 10 144676 A (TOKYO ELECTRON LTD), 29 May 1998 (1998-05-29) abstract paragraphs '0013!,'0024!,'0025!; figures 2,3,5 -& EP 0 933 802 A (TOKYO ELECTROM LTD) 4 August 1999 (1999-08-04) paragraphs '0018!,'0019!,'0025!-'0030!; figures 2,3,5	1,2,6, 9-13, 16-19
X A	EP 0 368 732 A (FUJITSU LTD) 16 May 1990 (1990-05-16) column 4, line 30 -column 5, line 6	9,11-15, 17 1,2,4,5, 7,8,18, 19

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 September 2000	02/10/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Szarowski, A

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/US 00/16556

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 661 204 A (MATHUR VISHNU ET AL) 28 April 1987 (1987-04-28) abstract	1,18
A	US 4 303 467 A (SCORNAVACCA FRANK ET AL) 1 December 1981 (1981-12-01) figure 1	9,10,14

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int tional Application No
PCT/US 00/16556

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 10144676 A	29-05-1998	EP 0933802 A	04-08-1999
		WO 9821745 A	22-05-1998
EP 0368732 A	16-05-1990	JP 2224240 A	06-09-1990
		JP 2610337 B	14-05-1997
		JP 3019335 A	28-01-1991
		JP 2125611 A	14-05-1990
		DE 68923247 D	03-08-1995
		DE 68923247 T	26-10-1995
		KR 9607635 B	07-06-1996
		US 5447598 A	05-09-1995
US 4661204 A	28-04-1987	AU 581110 B	09-02-1989
		AU 6549886 A	19-05-1987
		EP 0244462 A	11-11-1987
		JP 63501186 T	28-04-1988
		WO 8702626 A	07-05-1987
US 4303467 A	01-12-1981	CA 1117400 A	02-02-1982
		DE 2848691 A	17-05-1979
		FR 2408913 A	08-06-1979
		GB 2008499 A,B	06-06-1979
		JP 54089484 A	16-07-1979
		NL 7811183 A	15-05-1979