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A semiconductor chip and a method of manufacture thereof

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WO89/05038 A1
WO88/10008 A1

(58) Field of search

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UK CL(Edition L) **H1K KHAE KJAX**
INT CL[5] **H01L**
updated as appropriate

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226≤254

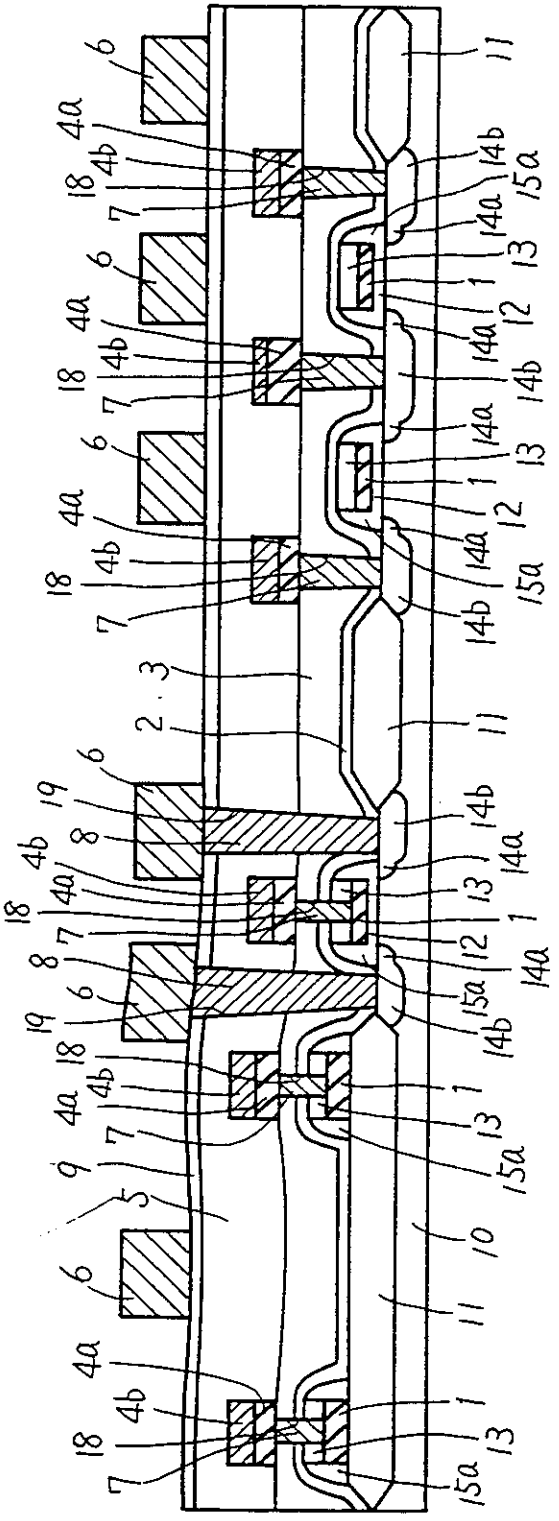


FIG. 1

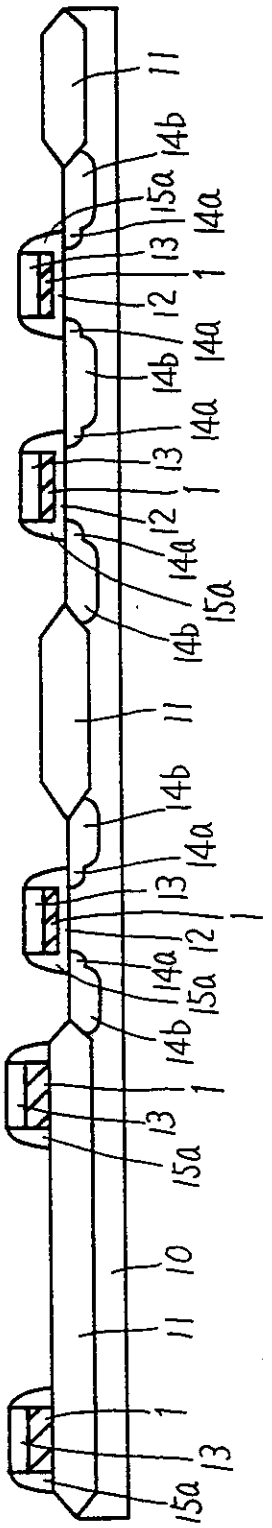

11
14b
15a
14a
13
1
12
14a
14b
14a
13
1
12
14a
15a
14b
11
14b
14a
13
1
12
14a
15a
14b
1
13
15a
10
11
1
13
15a

FIG. 2

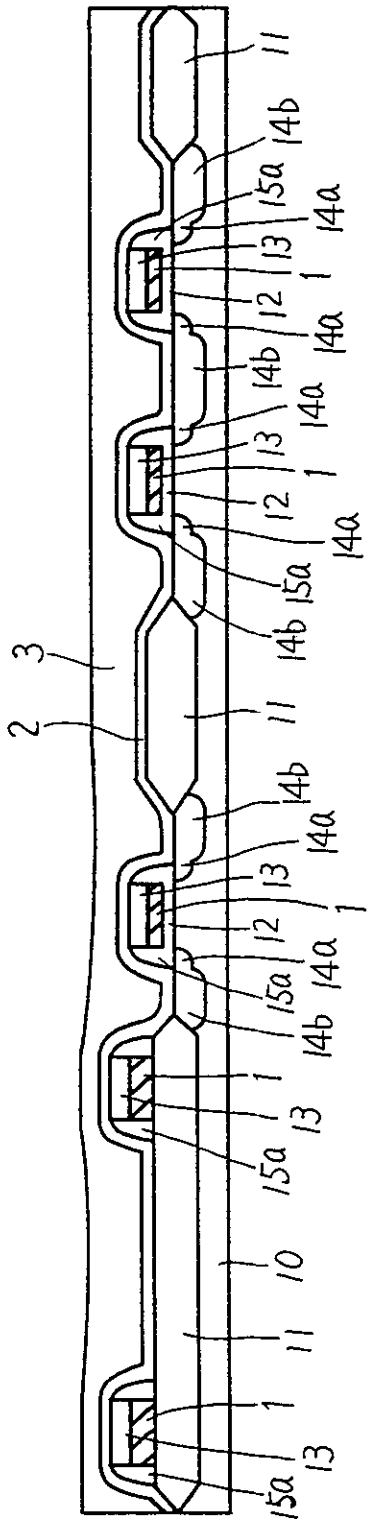

11
14b
15a
14a
13
1
12
14a
14b
14a
13
1
12
14a
15a
14b
3
2
11
14b
14a
13
1
12
14a
15a
14b
1
13
15a
10
11
1
13
15a

FIG. 3

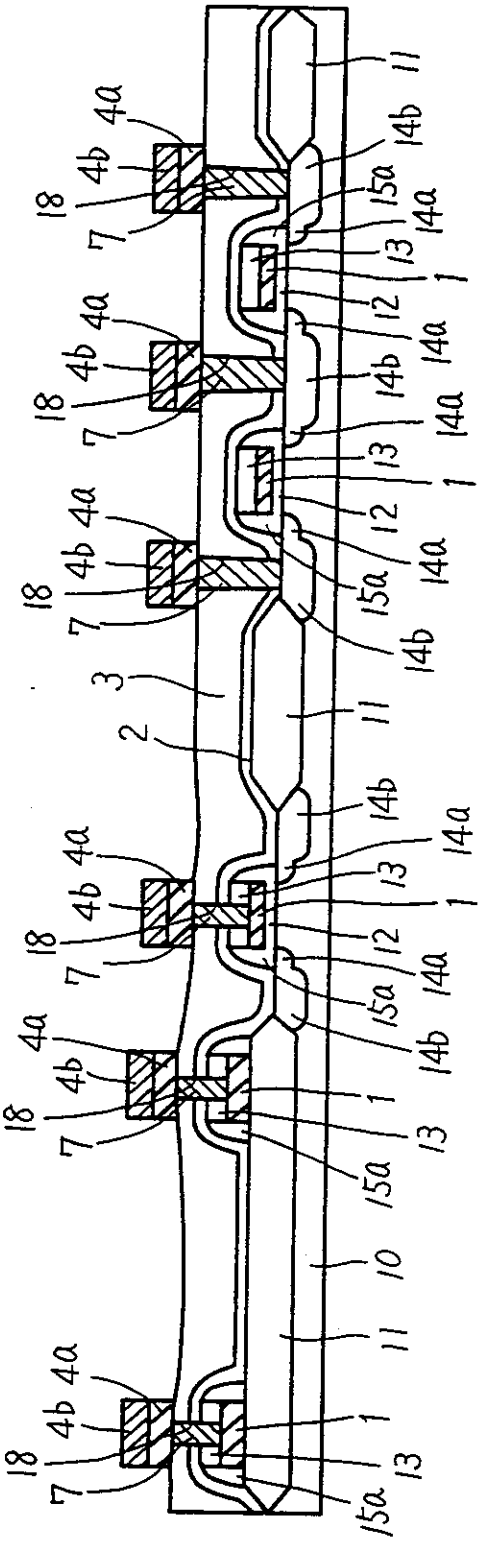

11
14b
15a
14a
13
1
12
14a
14b
14a
13
1
12
14a
15a
14b
3
2
11
14b
14a
13
1
12
14a
15a
14b
1
13
15a
10
11
1
13
15a
18
7
4b
4a

FIG. 4

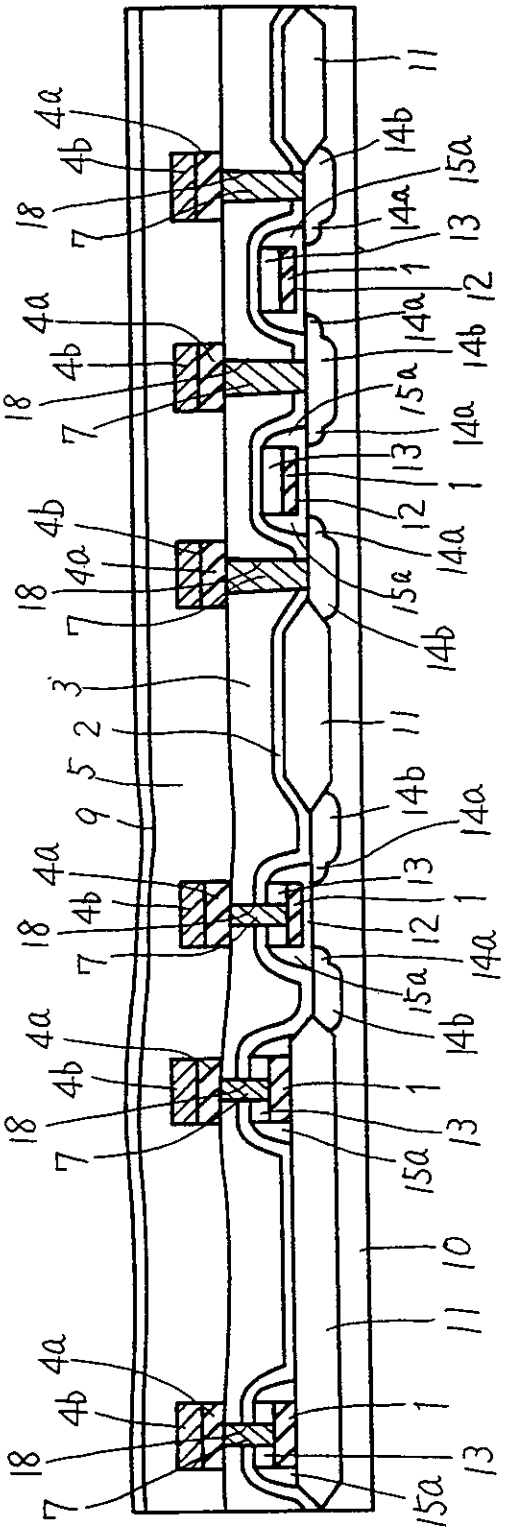

11
14b
15a
14a
13
1
12
14a
14b
15a
14a
13
1
12
14a
15a
14b
11
14b
14a
13
1
12
14a
15a
14b
1
13
15a
10
11
1
13
15a
4a
4b
18
7
3
2
5
9

FIG. 5

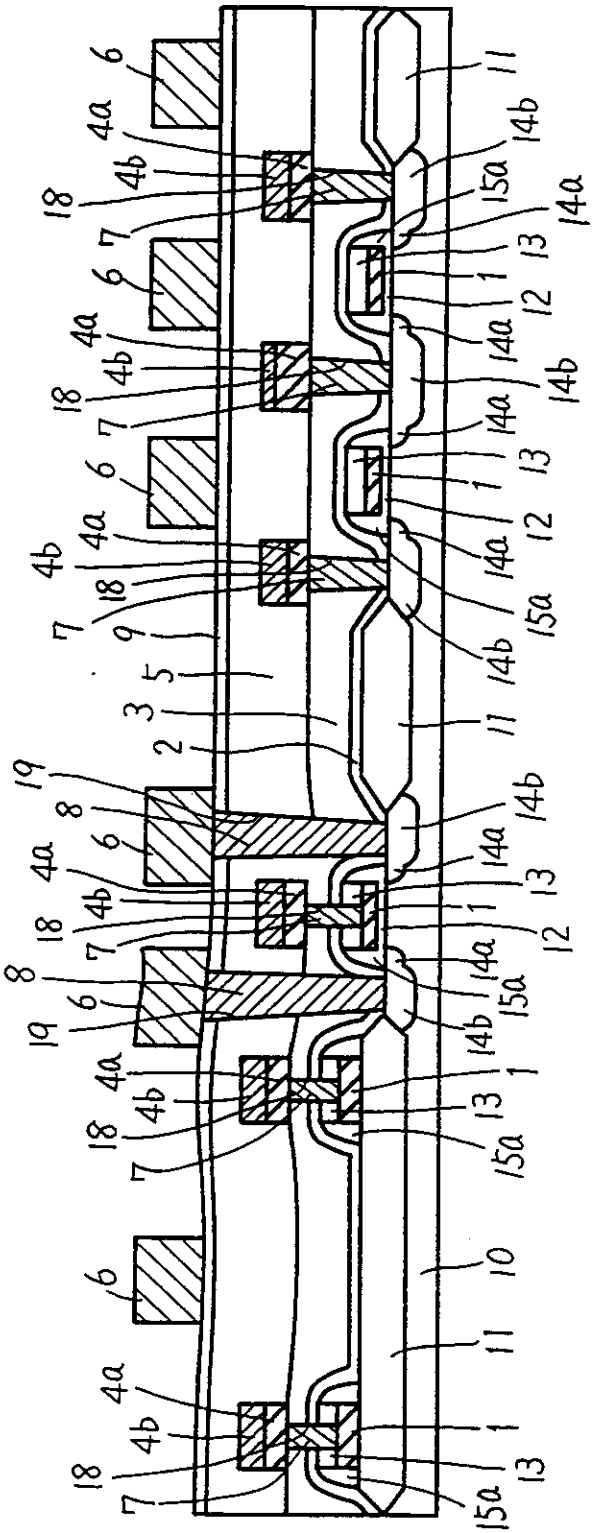
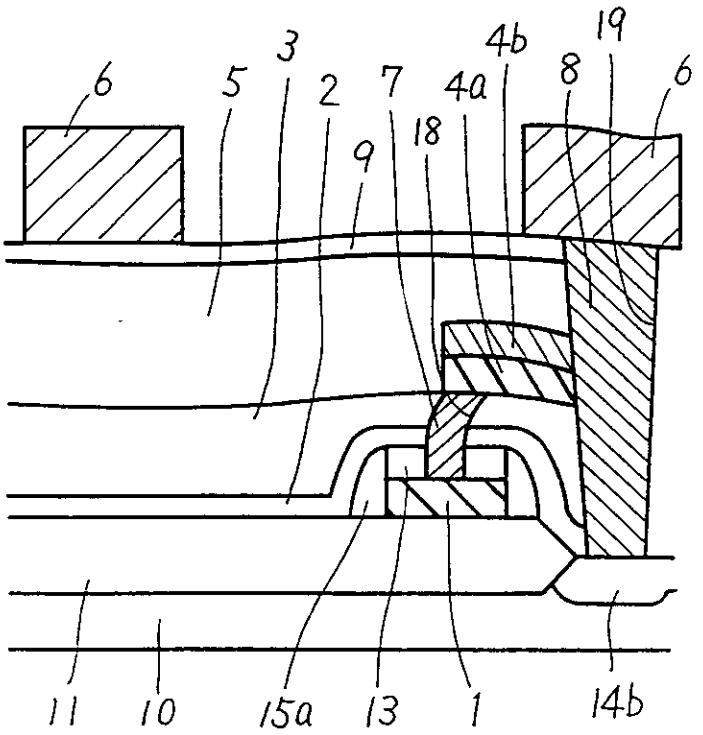


FIG. 6

FIG. 7



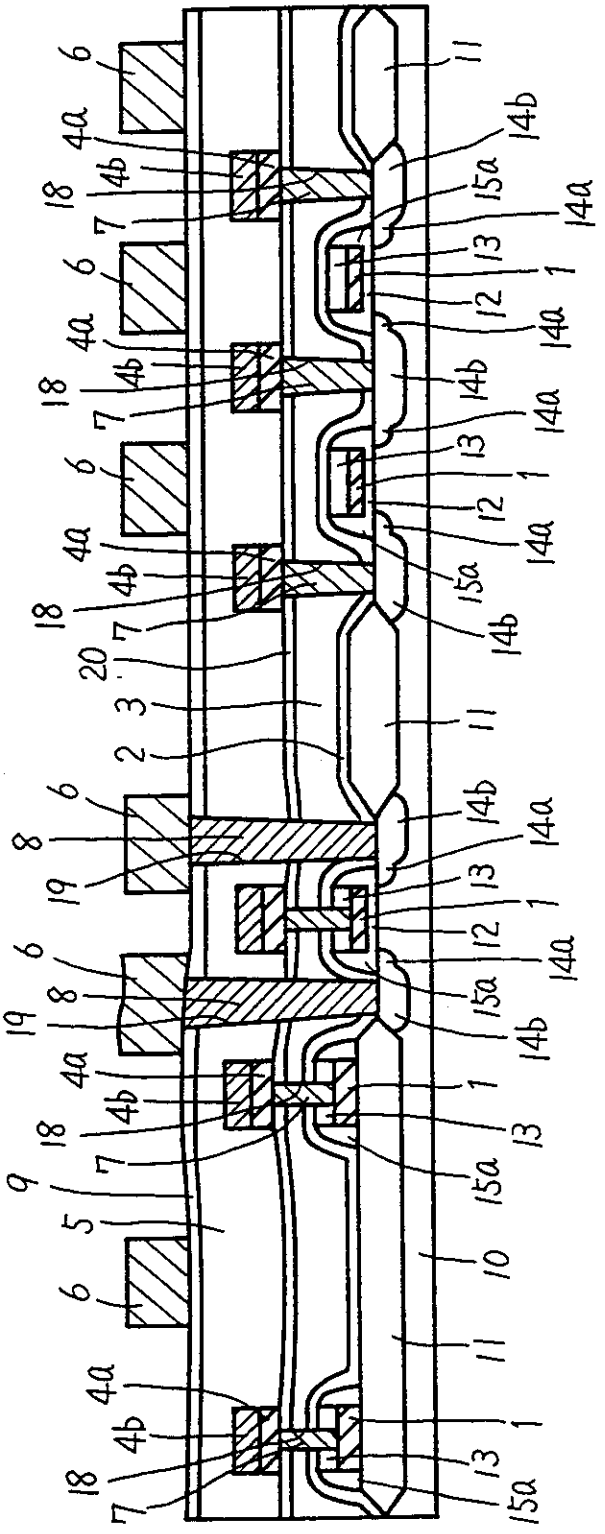


FIG. 8

FIG. 9

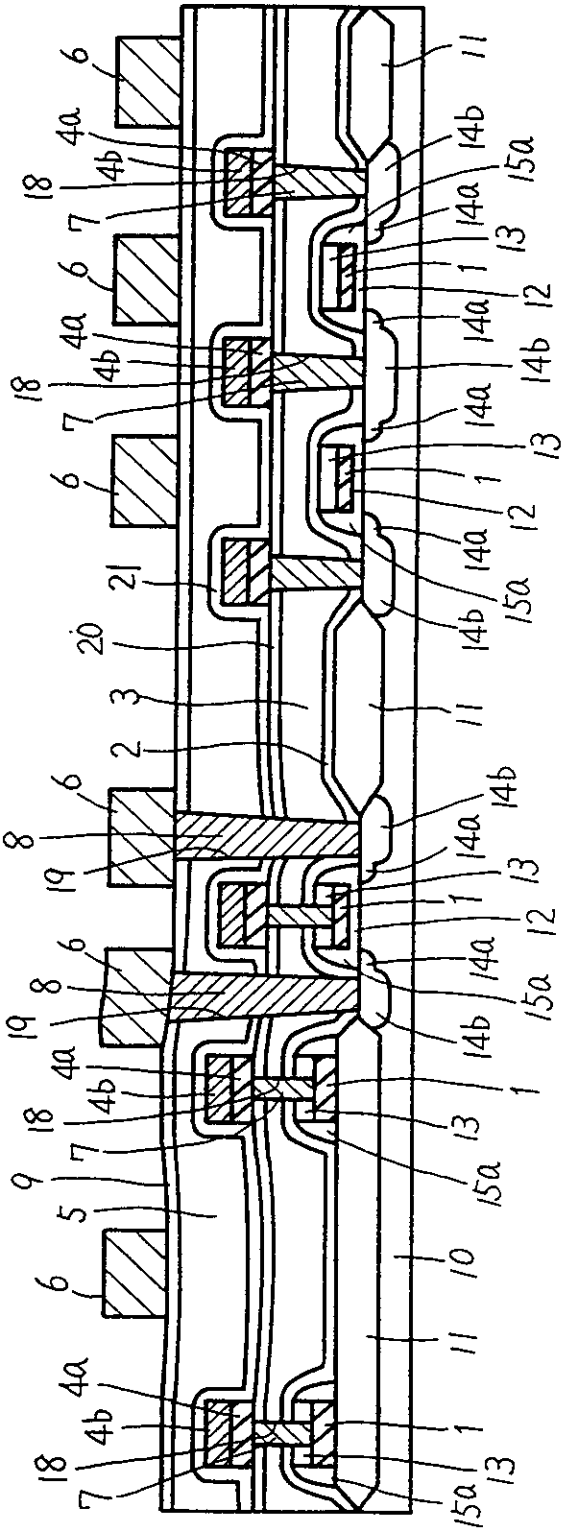

6
4a
4b
18
7
6
4a
4b
18
7
6
21
20
3
2
6
8
19
6
8
19
4a
4b
18
7
9
5
6
4a
4b
18
7
11
14b
15a
14a
13
1
12
14a
14b
14a
13
1
12
14a
15a
14b
11
14b
14a
13
1
12
14a
15a
14b
1
13
15a
10
11
1
13
15a

FIG. 10

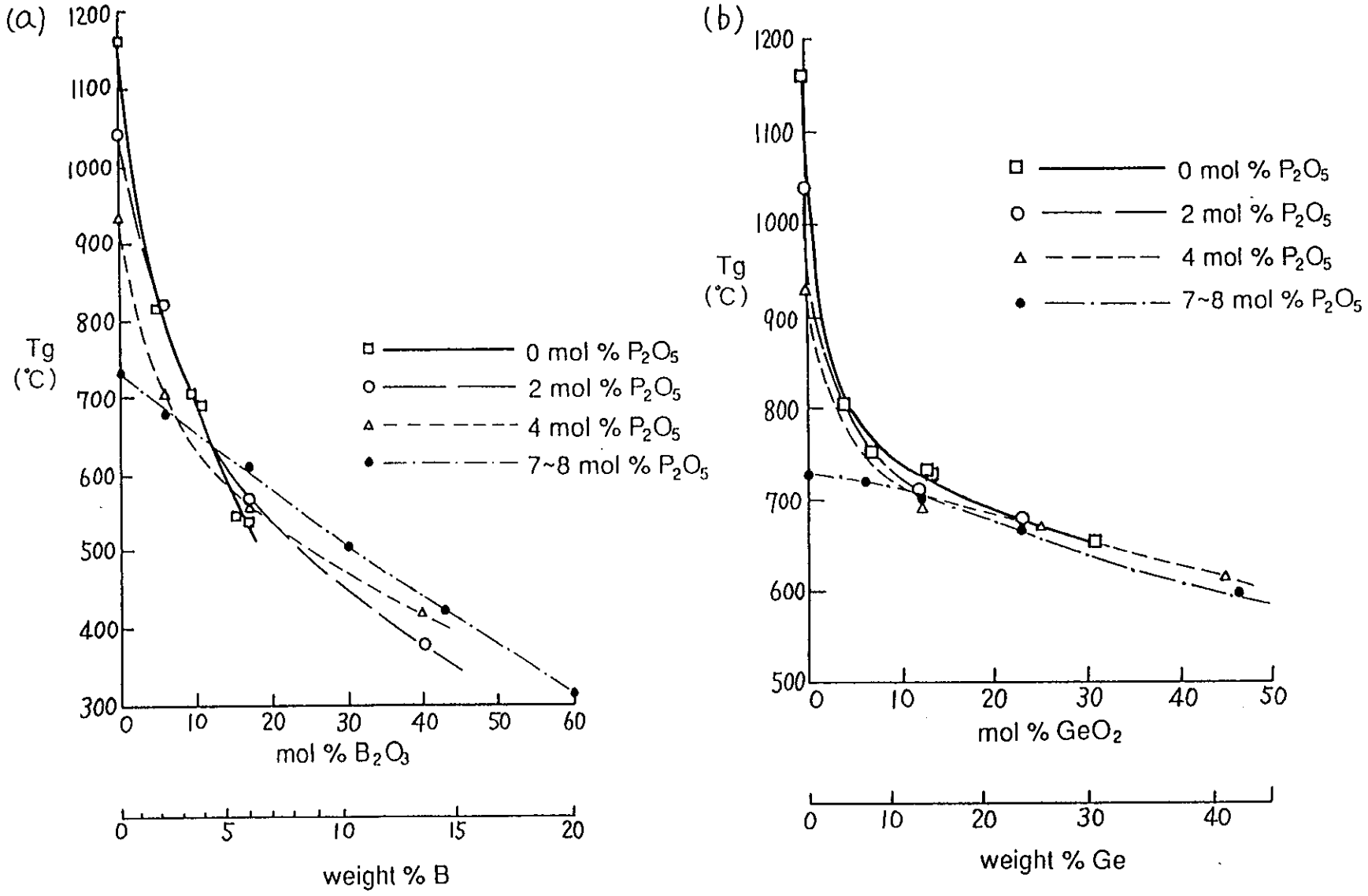

(a)
Tg (℃)
1200
1100
1000
900
800
700
600
500
400
300
0 mol % P_2O_5
2 mol % P_2O_5
4 mol % P_2O_5
7~8 mol % P_2O_5
0 10 20 30 40 50 60
mol % B_2O_3
0 5 10 15 20
weight % B
(b)
Tg (℃)
1200
1100
1000
900
800
700
600
500
0 mol % P_2O_5
2 mol % P_2O_5
4 mol % P_2O_5
7~8 mol % P_2O_5
0 10 20 30 40 50
mol % GeO_2
0 10 20 30 40
weight % Ge

FIG. 11

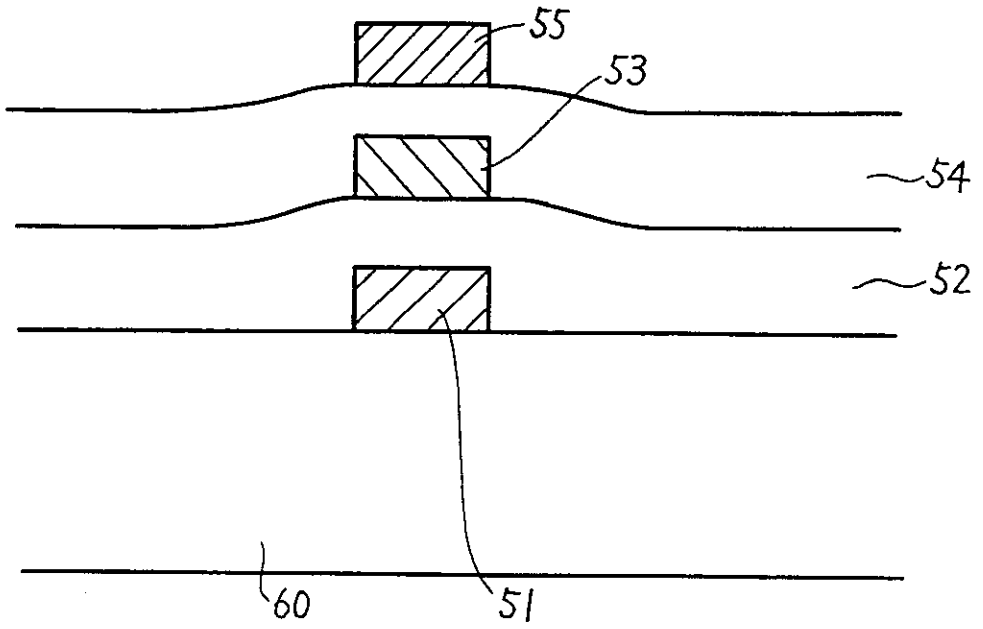

55
53
54
52
60
51

FIG. 12

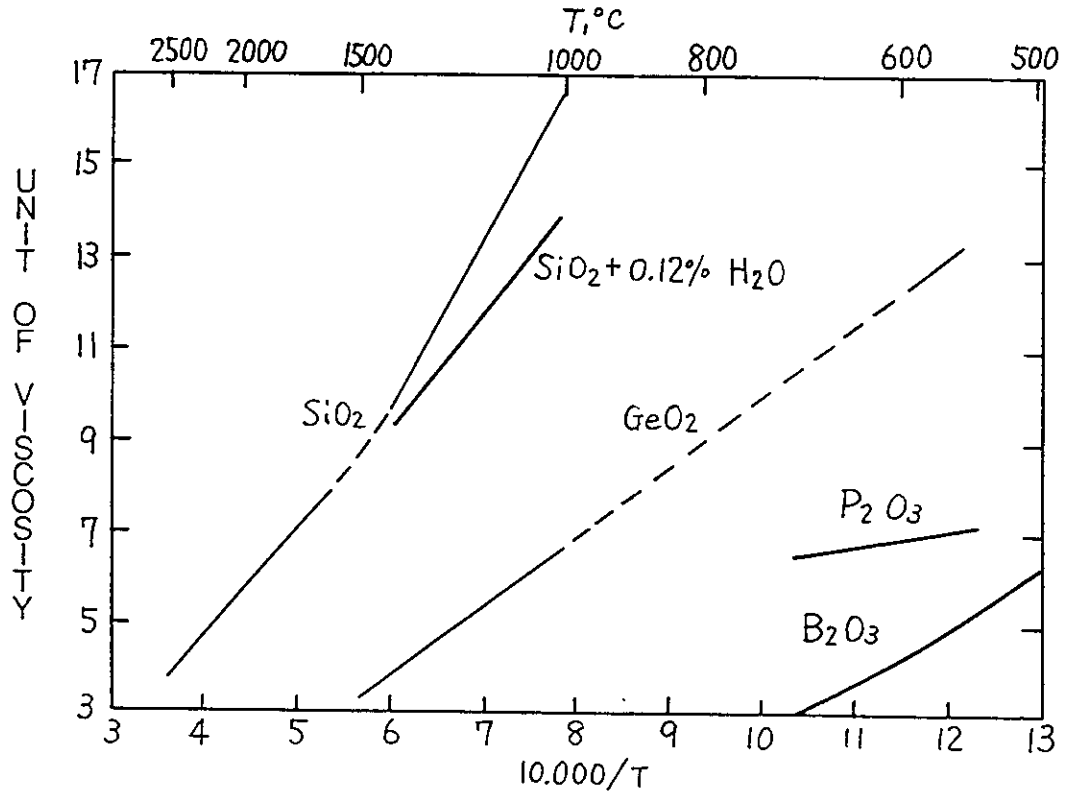

T,°C
2500 2000 1500 1000 800 600 500
17 15 13 11 9 7 5 3
UNIT OF VISCOSITY
SiO2+0.12% H2O
SiO2
GeO2
P2 O3
B2 O3
3 4 5 6 7 8 9 10 11 12 13
10.000/T

FIG. 13

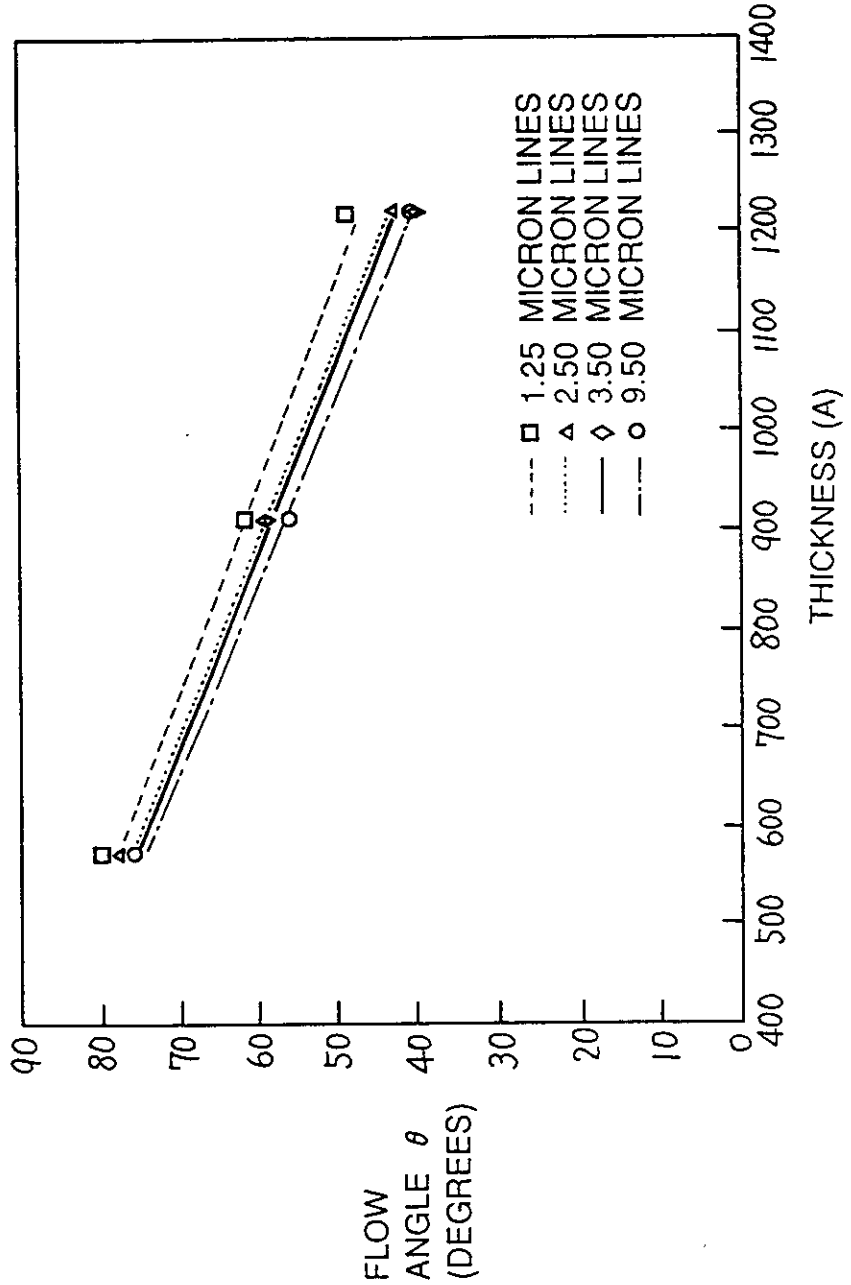
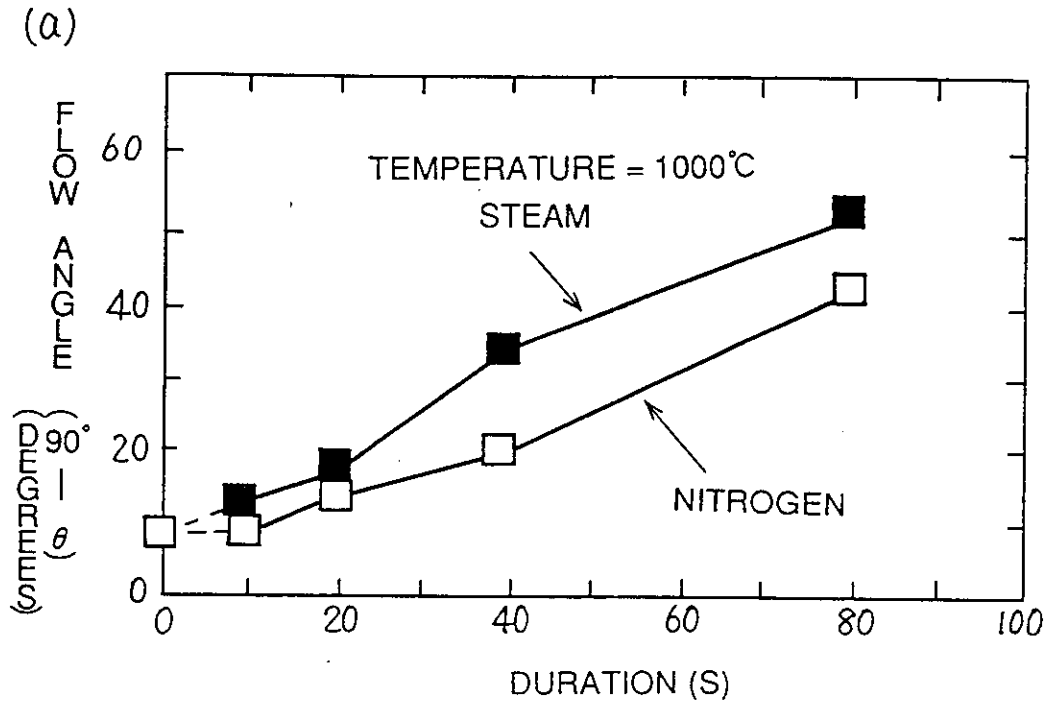
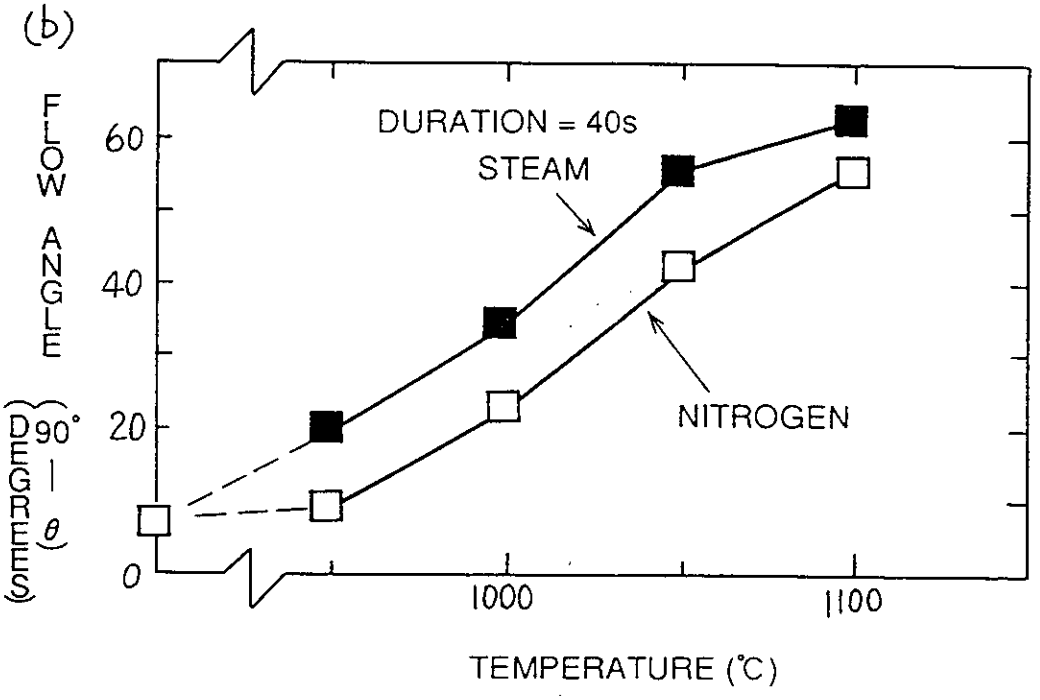

FLOW ANGLE θ (DEGREES)
90
80
70
60
50
40
30
20
10
0
400
500
600
700
800
900
1000
1100
1200
1300
1400
THICKNESS (A)
1.25 MICRON LINES
2.50 MICRON LINES
3.50 MICRON LINES
9.50 MICRON LINES

FIG. 14


(a)
FLOW ANGLE (DEGREES) 90° - θ
60
40
20
0
TEMPERATURE = 1000°C
STEAM
NITROGEN
0
20
40
60
80
100
DURATION (S)


(b)
FLOW ANGLE (DEGREES) 90° - θ
60
40
20
0
DURATION = 40s
STEAM
NITROGEN
1000
1100
TEMPERATURE (°C)

PRIOR ART

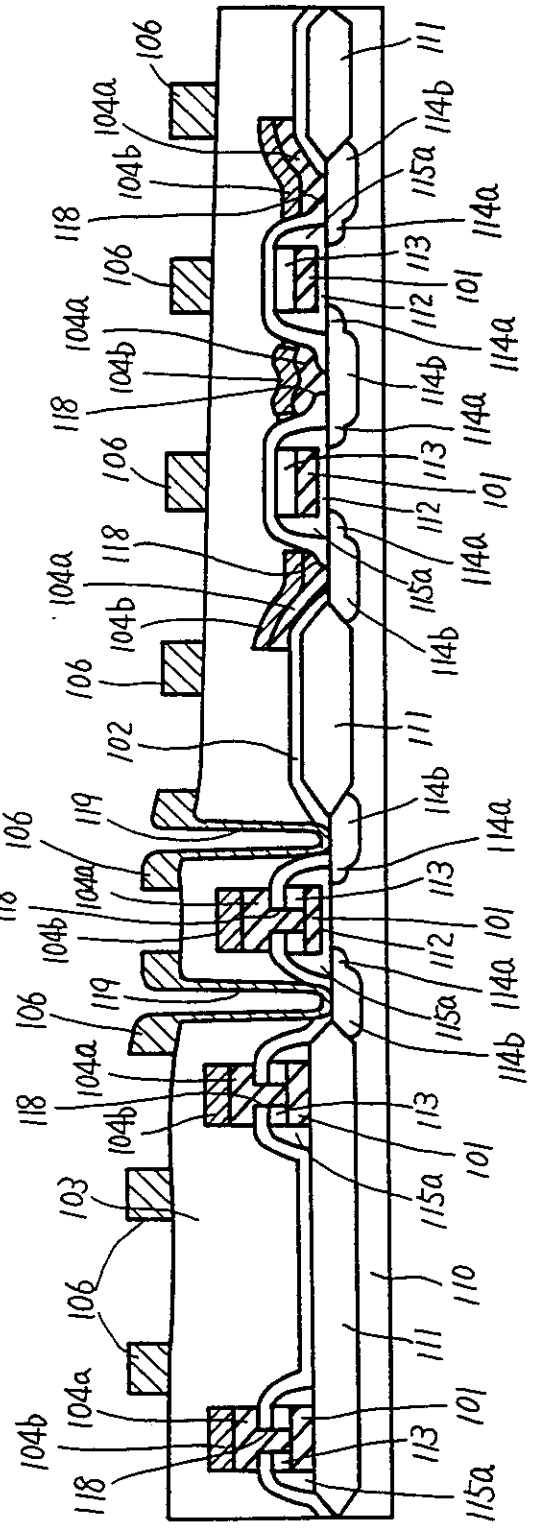
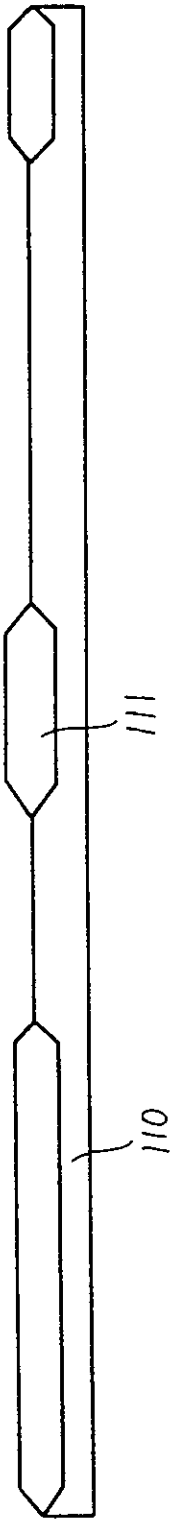
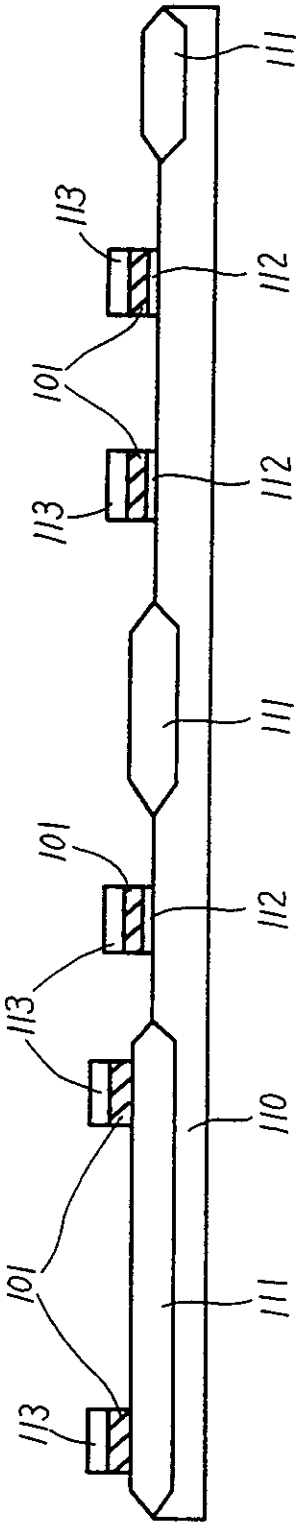


FIG. 15



PRIOR ART

FIG. 16



PRIOR ART

FIG. 17

PRIOR ART

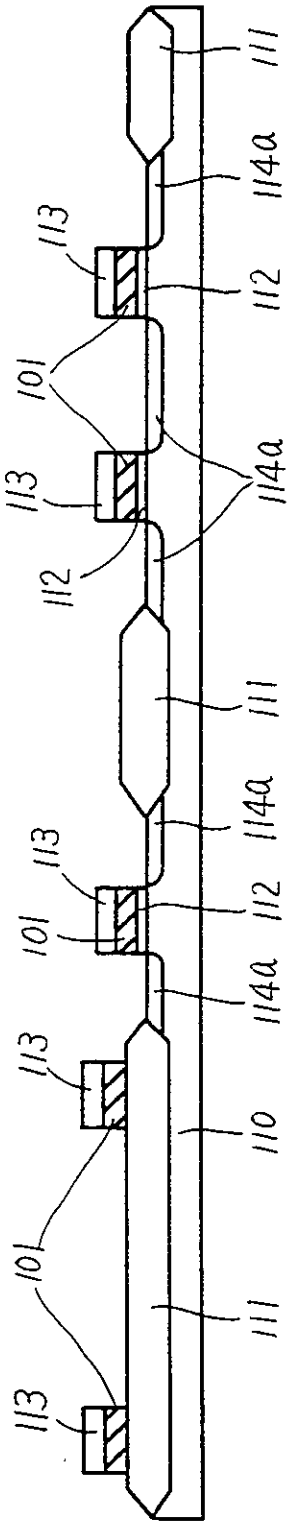
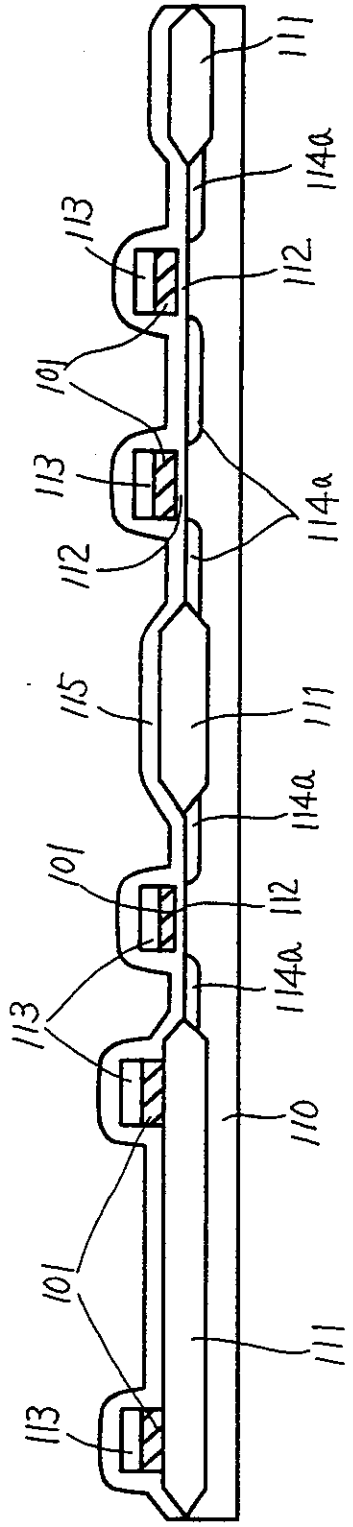


FIG. 18



PRIOR ART

FIG. 19

PRIOR ART

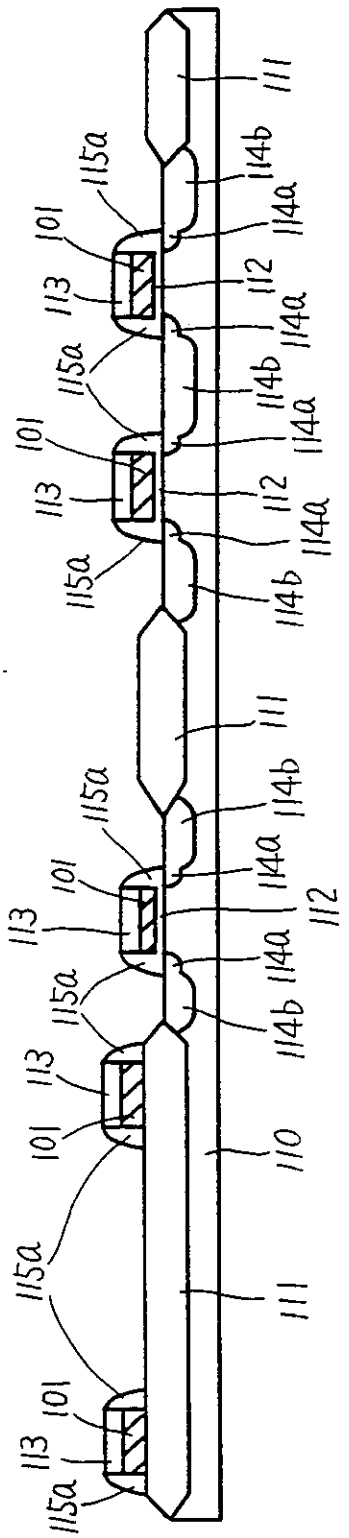


FIG. 20

PRIOR ART

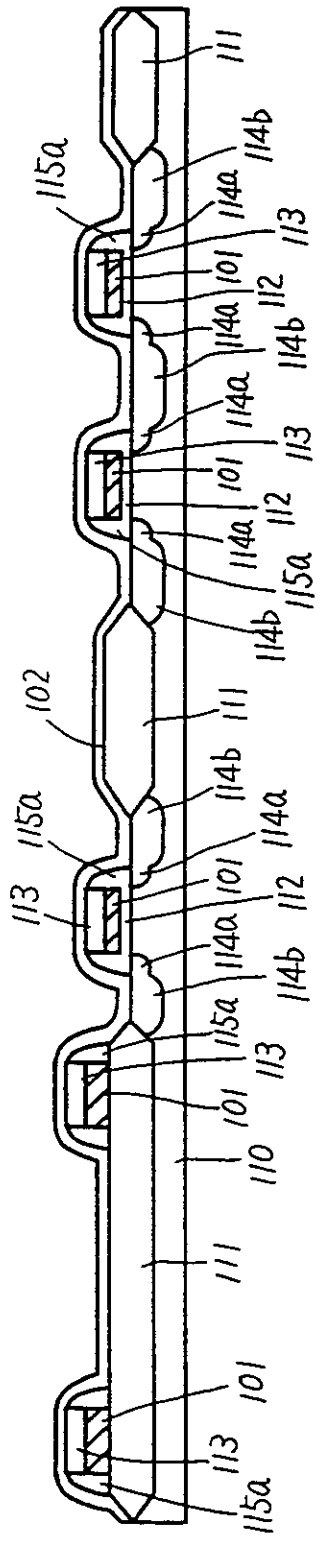


FIG. 21

PRIOR ART

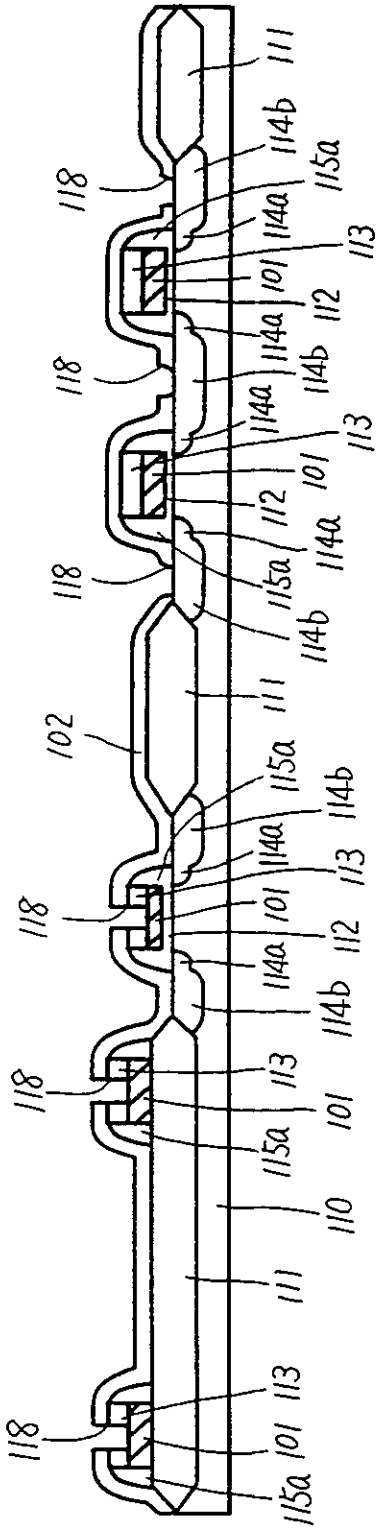


FIG. 22

PRIOR ART

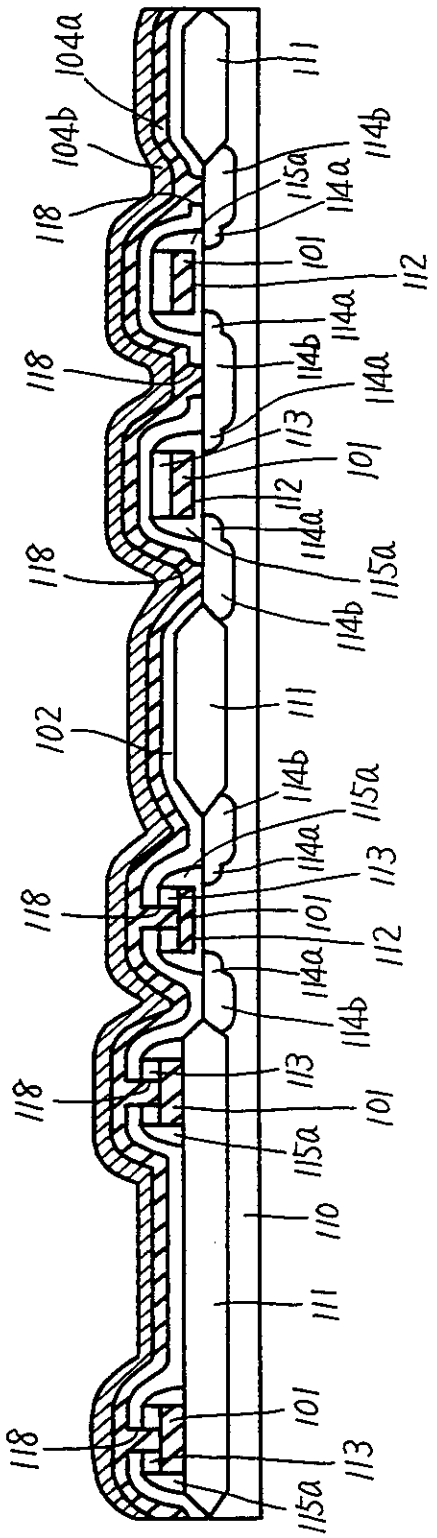


FIG. 23

PRIOR ART

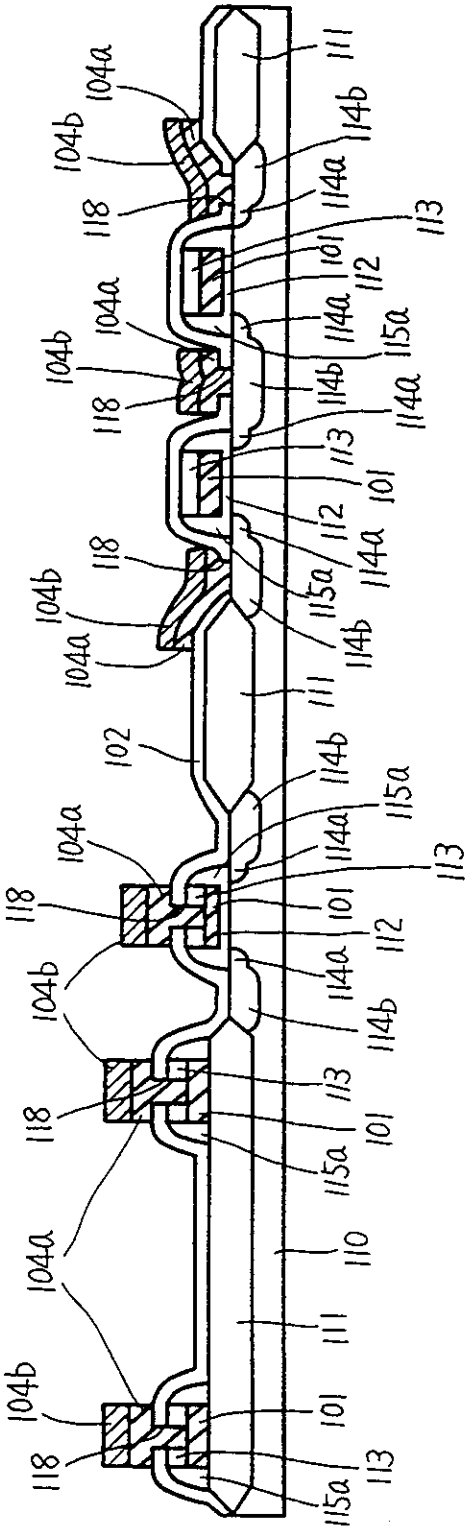


FIG. 24

PRIOR ART

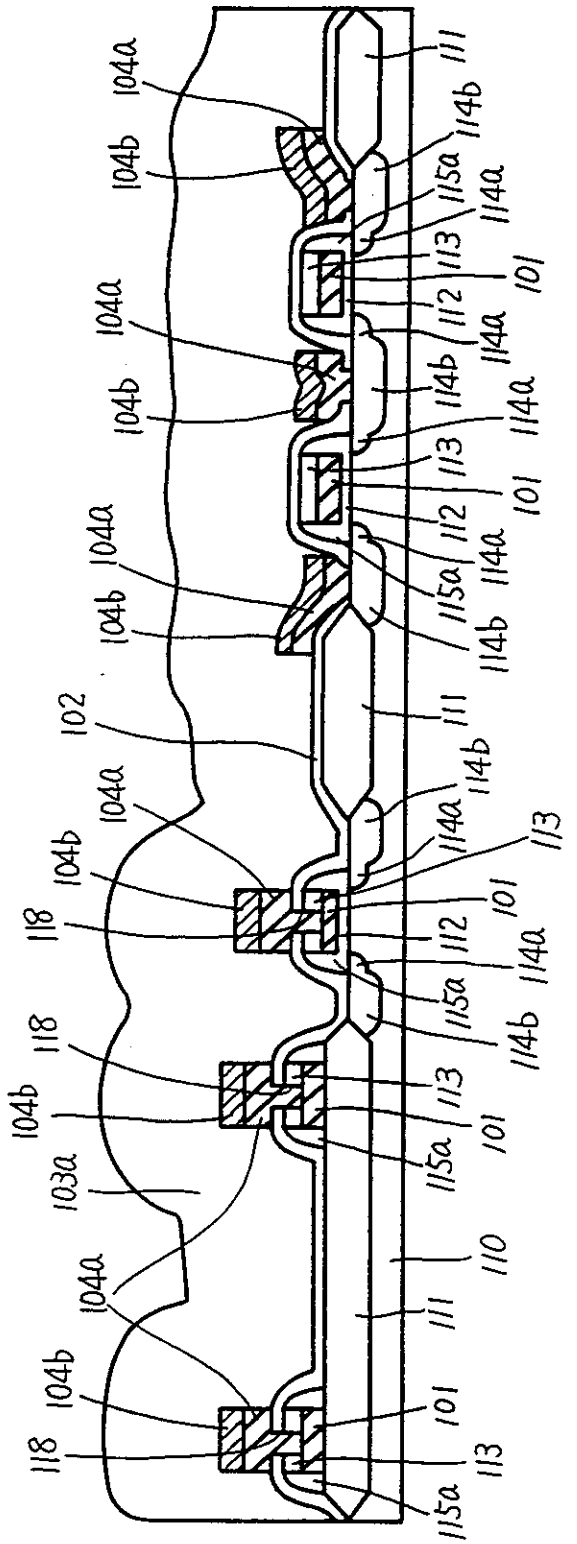


FIG. 25

PRIOR ART

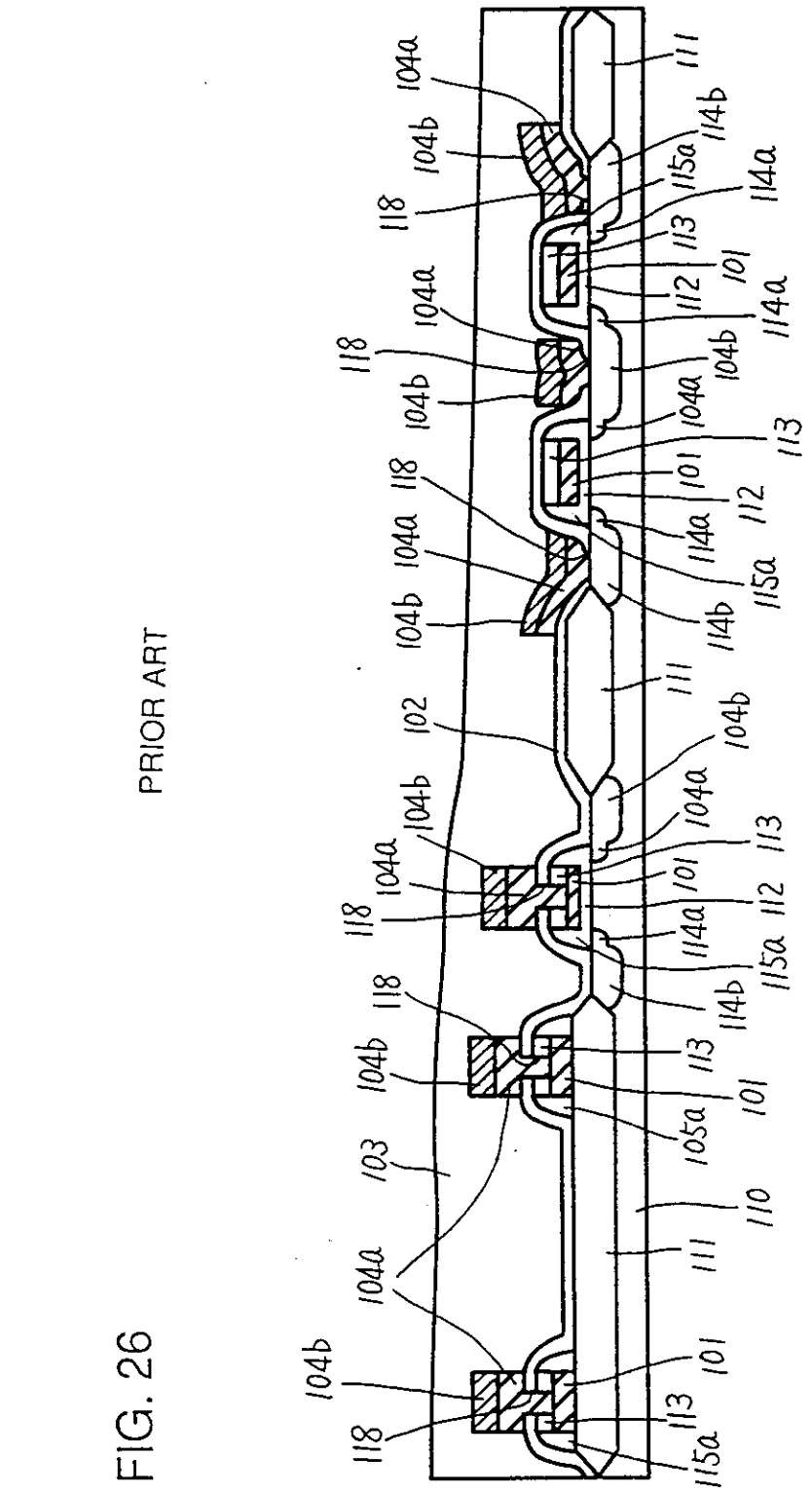


FIG. 26

PRIOR ART

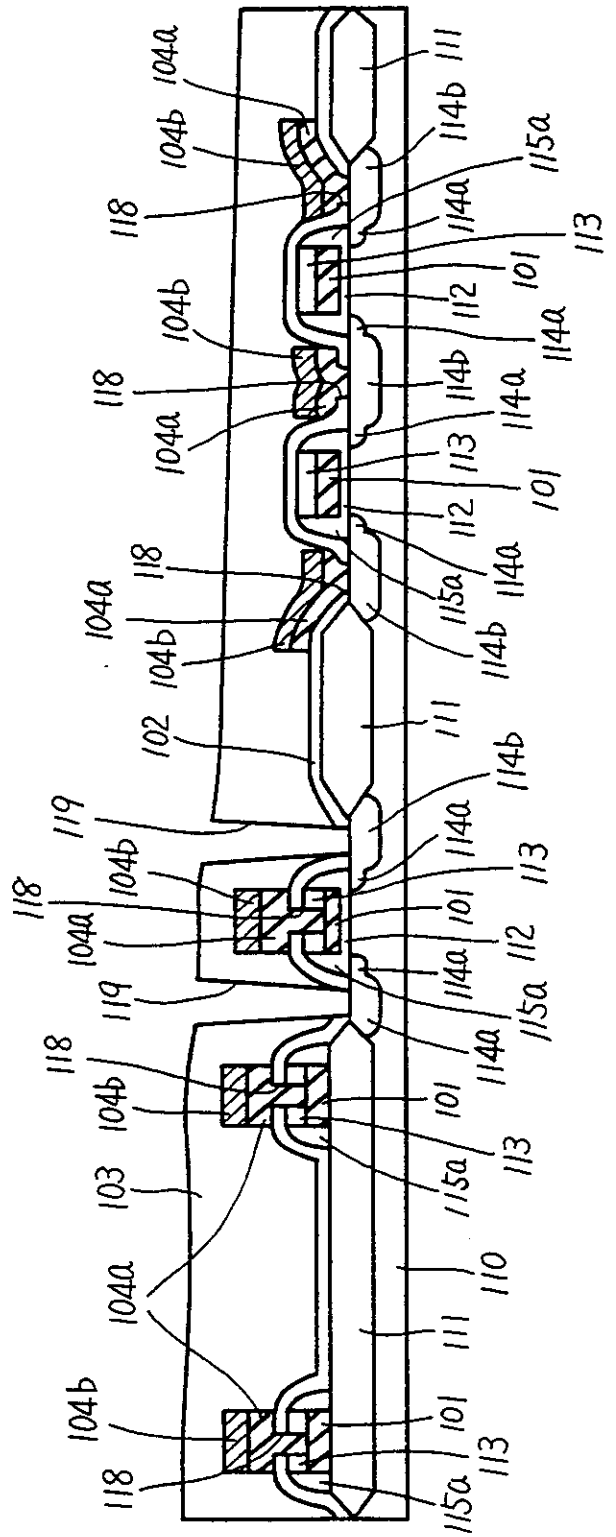


FIG. 27

PRIOR ART

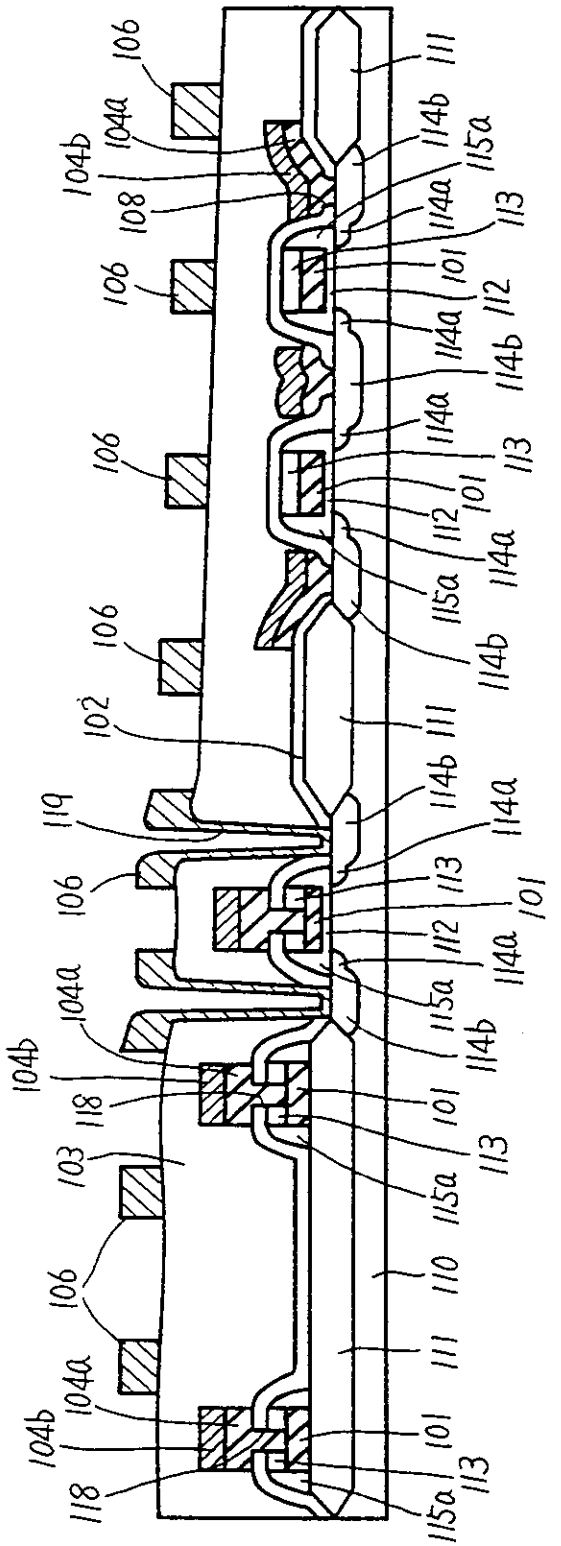


FIG. 28

FIG. 29

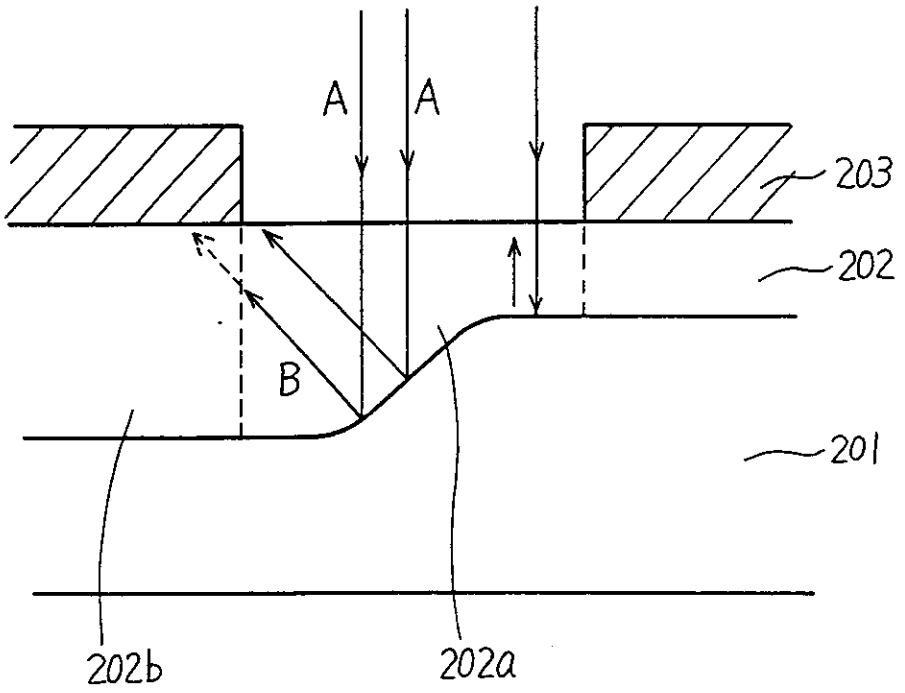


FIG. 30

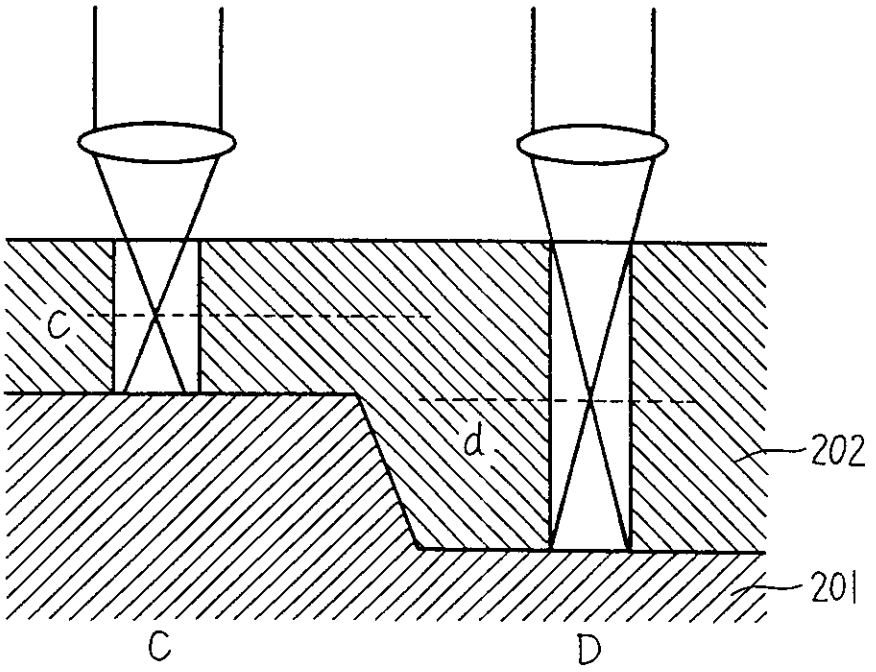


FIG. 31

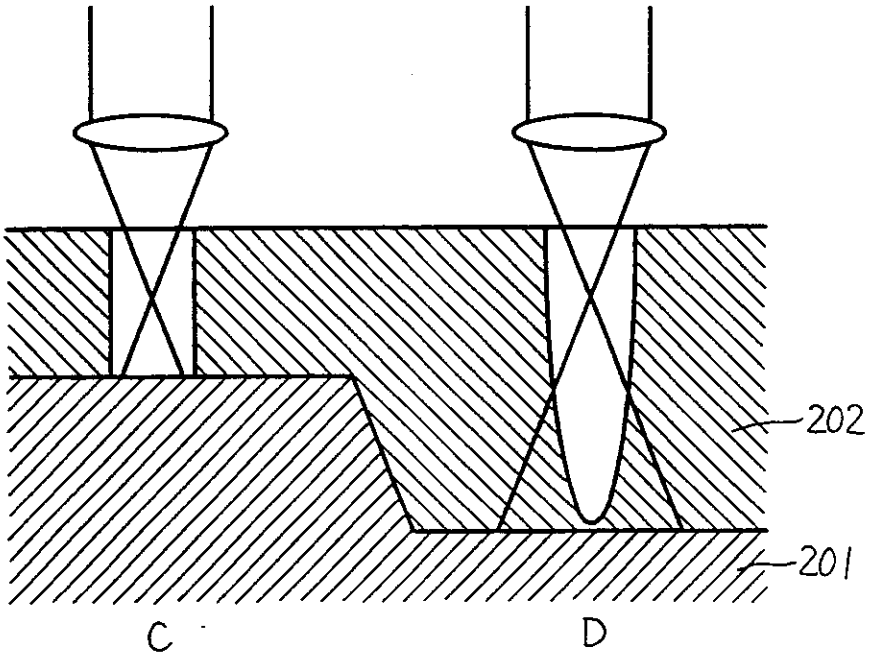


FIG. 32

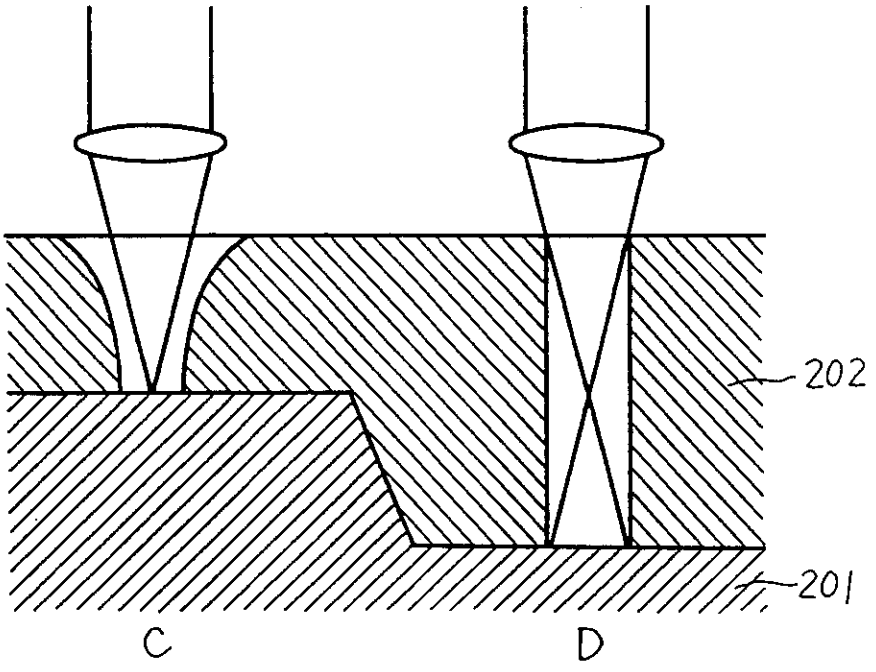


FIG. 33

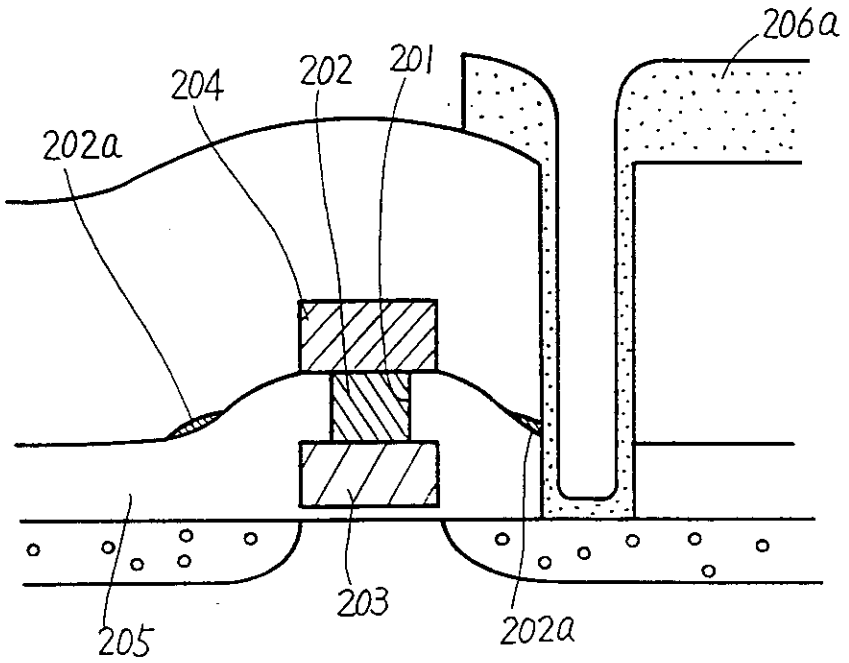
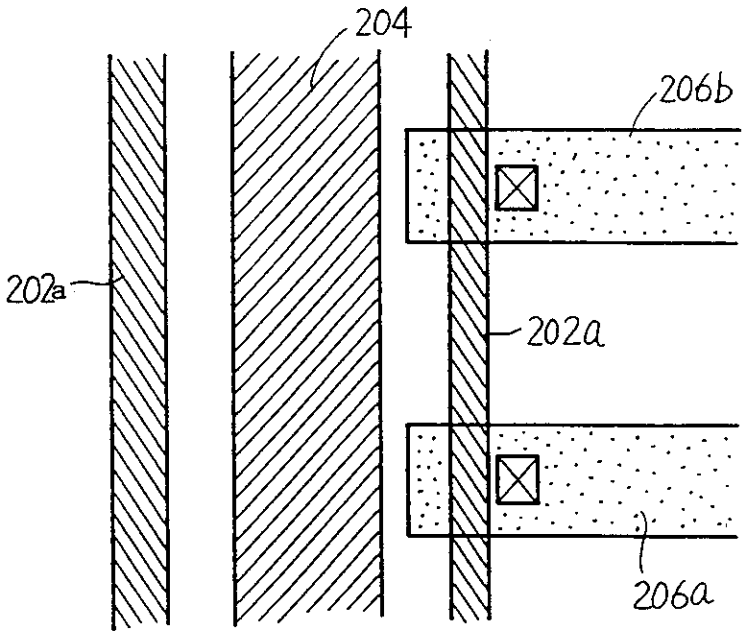


FIG. 34



2265254

A SEMICONDUCTOR CHIP AND A METHOD OF MANUFACTURE THEREOF

Field of the invention

The present invention relates to a semiconductor chip and a method of manufacturing the same, and more particularly, to a semiconductor chip including an insulating layer having a highly planarised surface and a method of manufacturing thereof. The term "semiconductor device" used hereinafter refers to such a semiconductor chip.

Description of the Background Art

A structure of a conventional semiconductor device will first be described.

Fig. 15 is a sectional view of a conventional semiconductor device schematically showing a structure thereof. Referring to Fig. 15, an isolation oxide film 111 of approximately 300 - 800nm in thickness is formed on the surface of a semiconductor substrate 110 of silicon. An element such as a MOSFET is provided in the region isolated by the isolation oxide film 111. This MOSFET is formed of impurity diffusion layers 114a and 114b serving as the source and drain, a gate oxide film 112, and a polycrystalline silicon film 101 serving as a gate.

The impurity diffusion layers 114a and 114b implementing the source and drain are formed on the

surface of the semiconductor substrate 110, and include a portion of low concentration 114a and a portion of high concentration 114b. A gate oxide film 112 is formed on the surface of the semiconductor substrate 110 so as to span over the impurity diffusion layers 114a and 114b. A polycrystalline silicon film 101 implementing a gate is formed on the surface of the gate oxide film 112. A silicon oxide film 113 is formed on the surface of the polycrystalline silicon film 101. A sidewall 115a is formed at the sidewall of the polycrystalline silicon film 101 and the silicon oxide film 113.

A thin silicon oxide film or a nitride film 102 is formed all over the surface of the semiconductor substrate 110 having a MOSFET formed therein. A connection hole 118 is formed in the thin silicon oxide film/nitride film 102. A portion of the surface of the impurity diffusion layer 114b or the polycrystalline silicon film 101 is exposed in the connection hole 118. A polycrystalline silicon film 104a is formed on the surface of the thin silicon oxide film/nitride film 102 so as to be in contact with the exposing portion of the impurity diffusion layer 114b and the polycrystalline silicon film 101. A refractory metal thin film 104b is formed on the surface of the polycrystalline silicon film 104a. An interconnection layer is formed of the polycrystalline silicon film 104a

and the refractory metal thin film 104b. On the entire surface of the thin silicon oxide film/nitride film 102 on which this interconnection layer is formed, an interlayer insulating layer 103 including impurities is formed to cover the interconnection layer. The interlayer insulating layer 103 is subjected to planarization. A connection hole 119 is formed in the interlayer insulating layer 103. A portion of the surface of the impurity diffusion region 114b not connected to the polycrystalline silicon film 104a is exposed in the connection hole 119. An interconnection layer 106 of an alloy of aluminum and copper is formed on the surface of the insulating layer 103 so as to form contact with the exposed portion of the impurity diffusion layer 114b.

A conventional semiconductor device has a structure as described in the foregoing.

Next, a method of manufacturing a conventional semiconductor device will be described hereinafter.

Figs. 16 - 28 are sectional views of a conventional semiconductor device schematically showing the manufacturing steps thereof. Referring to Fig. 16, an isolation oxide film 111 of approximately 300 - 800nm in film thickness is formed by local oxidation on the surface of a semiconductor substrate 110 of silicon.

Referring to Fig. 17, a gate oxide film 112 of 5 -

30nm in film thickness is formed by thermal oxidation on an exposing region of the semiconductor substrate 110 not covered with the isolation oxide film 111. Then, a polycrystalline silicon film 101 including phosphorus and arsenic and a silicon oxide film 113 are formed on the surface of the semiconductor substrate 110 by chemical vapor deposition. The gate oxide film 112, the polycrystalline silicon film 101, and the silicon oxide film 113 are patterned by photolithography and RIE.

Referring to Fig. 18, impurity ions are implanted to the semiconductor substrate 110 using the polycrystalline silicon film 101, the silicon oxide film 113, and the isolation oxide film 111 as a mask. By this ion implantation, an impurity diffusion layer 114a is formed on the exposed surface of the semiconductor substrate 110.

Referring to Fig. 19, a silicon oxide film 115 is formed to a thickness of 50 - 300nm on the surface of the semiconductor substrate 110 by chemical vapor deposition.

Referring to Fig. 20, the silicon oxide film 115 is etched by RIE to form a sidewall 115a at the sidewall of the polycrystalline silicon film 101 and the silicon oxide film 113. Impurity ions are implanted into the semiconductor substrate 110 using the sidewall 115a, the silicon oxide film 113, and the isolation oxide film 111 as a mask to form an impurity diffusion layer 114b. A two

layered structure of a portion of high impurity concentration and a portion of low impurity concentration is formed by these impurity diffusion layers 114b and 114a. By the formation of the impurity diffusion layers, a MOS transistor is implemented of impurity diffusion layers 114a, 114b, a gate oxide film 112, and a polycrystalline silicon film 101.

Referring to Fig. 21, a thin silicon oxide film or a nitride film 102 is deposited so as to cover an element such as a MOS transistor formed on the surface of the semiconductor substrate 110.

Referring to Fig. 22, a connection hole 118 is formed in the thin silicon oxide film/nitride film 102 by photolithography and RIE. A portion of the surface of the impurity diffusion layer 114b or the polycrystalline silicon film 101 is exposed in the connection hole 118. In the exposure process of the polycrystalline silicon film 101, the silicon oxide film 113 is also etched.

Referring to Fig. 23, a polycrystalline silicon film 104a and a refractory metal thin film 104b are formed all over the surface of the thin silicon oxide film/nitride film 102 by chemical vapor deposition. The polycrystalline silicon film 104a is electrically connected to the impurity diffusion layer 114b or the polycrystalline silicon film 101 via the connection hole

118.

Referring to Fig. 24, the polycrystalline silicon film 104a and the refractory metal thin film 104b are patterned by photolithography and RIE. By this patterning process, an interconnection layer constituted by the polycrystalline silicon film 104a and the refractory metal thin film 104b is formed.

Referring to Fig. 25, an oxide film 103a including impurities is deposited on the surface of the semiconductor substrate 110 so as to cover the interconnection layer formed of the polycrystalline silicon film 104a and the refractory metal thin film 104b.

Referring to Fig. 26, the oxide film 103a including impurities is subjected to thermal treatment at a temperature of 800°C - 1000°C for planarization. Following the thermal treatment, the oxide film 103a including impurities is reduced in film thickness by an overall etching. A thin oxide film or a nitride film is deposited on the surface of the oxide film 103a including impurities. Thus, an interlayer insulating layer 103 is obtained.

Referring to Fig. 27, a connection hole 119 is formed in the interlayer insulating layer 103 by photolithography and RIE. The connection hole 119 is formed to reach the impurity diffusion layer 114b that is not electrically

connected to the polycrystalline silicon film 104a.

Referring to Fig. 28, an aluminum-copper alloy film is deposited on the surface of the interlayer insulating layer 103 by sputtering. By patterning this aluminum-copper alloy film by photolithography and RIE, an interconnection layer 106 is formed. This interconnection layer 106 is electrically connected to the impurity diffusion layer 114b via the connection hole 119.

A conventional semiconductor device is formed as described in the foregoing.

Because a conventional semiconductor device was formed as described above, the surface of the interlayer insulating layer 103 was insufficient in planarization. An interlayer insulating layer 103 having a surface lacking planarization will generate problems as set forth in the following.

Fig. 29 is a sectional diagram schematically showing a state of exposing a resist. Referring to Fig. 29, a resist 202 is applied on the surface of an underlying layer 201. The resist 202 is patterned to a desired configuration using a mask 203. In this patterning process, the light of exposure is introduced in a direction indicated by the arrow A only into a region 202a that should be exposed defined by the mask 203. However, the presence of a stepped portion in the underlying layer

201 will cause the light of exposure to be reflected in the direction indicated by arrow B. This reflected light in the direction of arrow B will expose a region 202b which should not be actually exposed. This means that it is difficult to expose the resist 202 to a desired configuration if there is a stepped portion in the underlying layer 201. Thus, it will be difficult to pattern the resist 202 properly to a desired configuration.

Fig. 30 is a sectional diagram schematically showing the optimum focusing position in exposing a resist. Referring to Fig. 30, a resist 202 is applied on the surface of an underlying layer 201. A stepped portion in the underlying layer 201 will result in a resist 202 differing in thickness according to the portion thereof. A difference in thickness will mean that the optimum focusing position of the light of exposure for exposing the resist 202 will also differ. More specifically, the optimum focusing position of the light of exposure at the respective positions of C and D is c and d, respectively, as shown in Fig. 30. If exposure is carried out conforming to the focus at position C, the pattern at position D will be degraded in configuration. Conversely, if exposure is carried out conforming to the focus at position D, the pattern at position C is degraded in

configuration as shown in Fig. 32. It is therefore difficult to properly pattern the resist 202 in a desired configuration.

As described above, the resist 202 cannot be patterned to a desired configuration if there is a stepped portion in the underlying layer 201. If etching is carried out using such a resist of unsatisfactory configuration as a mask, the dimension of the finished product will differ from the design dimension. Such an offset in the finished dimension will be a fatal disadvantage in the attempt to reduce the size of semiconductor devices, with difficulty in the formation of patterns of connection holes and metal interconnection layers.

There is also a problem which will be described hereinafter in the case of filling a connection hole with a plug if the surface of the interlayer insulating layer of Fig. 28 is not sufficient in planarization.

Figs. 33 and 34 are a sectional view and a plan view, respectively, of a semiconductor device schematically showing a problem encountered by filling the connection hole with a plug. Referring to Figs. 33 and 34, a plug 202 is formed in a connection hole 201. An upper conductive layer 204 is electrically connected to a lower conductive layer 203 by means of the plug 202. This plug

202 is obtained by etching a conductive layer deposited all over the surface of the insulating layer 205. An insufficient planarisation of the surface of the insulating layer 205 will result in a residue 202a at the stepped portion on the surface of the insulating layer 205 at the time of plug formation. There is a possibility of other interconnection layers 206a and 206b being short circuited by this residue 202a, as shown in Fig. 34. There was a problem of degradation in electrical reliability such as shorting of the interconnection layers due to generation of a residue in the stepped portion if planarisation was not sufficient in the surface of the interlayer insulating layer 103 shown in Fig. 28.

SUMMARY OF THE INVENTION

The present invention is intended to facilitate formation of patterns of connection holes and metal interconnection layers in accordance with miniaturisation by reducing the surface stepped portion of an insulating layer in a semiconductor device.

The present invention is also intended to improve electrical reliability of a semiconductor device by reducing the surface stepped portion of an insulating layer in a semiconductor device.

Semiconductor chips, and methods of their manufacture, in accordance with this invention, are defined by the claims appended.

A method of manufacturing a semiconductor device according to the present invention includes the steps of forming a first patterned conductive layer on the main surface of a semiconductor substrate, forming a first insulating layer to cover the second conductive layer, planarising the free surface of the first insulating layer under a first condition, forming a second patterned conductive layer on the planarised surface of the first insulating layer, forming a second insulating layer to cover the second conductive layer, planarising the free surface of the second insulation layer under a second condition differing from the first condition, whereby the second insulating layer is planarised while the state of planarisation of the first insulating layer is maintained and forming a third conductive layer on the surface of the planarised second insulating layer.

In this method of manufacturing a semiconductor device, the first and second insulating layers are made to flow individually, so that a stepped portion on the surface of the second insulating layer is reduced significantly. That is to say, a stepped portion generated at the surface of the second insulating layer is even smaller because the second insulating layer is formed after planarisation of the first insulating layer. The stepped portion on the surface of the second insulating layer can be further reduced because a planarisation process is also applied to the second

insulating layer. Thus, the second insulating layer has a highly planarised surface to facilitate patterning of the resist on the second insulating layer to a desired configuration. Furthermore, there is less possibility of a residue being left at the stepped portion on the surface at the time of plug formation because the surface of the second insulating layer has a highly planarised surface. Therefore, electrical reliability is improved without shorting by the residue occurring between conductive layers.

This method, for example, may include the steps of forming a first patterned layer of a conductive material on the surface of a semiconductor substrate, forming a first insulating layer of a material that flows at a first predetermined

temperature to cover the first patterned layer, wherein the first insulating layer is heated at the first predetermined temperature to have a planarized upper surface, forming a second patterned layer of a conductive material on the surface of the first insulating layer, forming a second insulating layer of a material that flows at a second predetermined temperature lower than the first predetermined temperature to cover the second patterned layer, wherein the second insulating layer is heated at the second predetermined temperature to have a planarized upper face.

In this example of a manufacturing method of a semiconductor device, the first insulating layer and the second insulating layer are made to flow individually, so that the stepped portion on the surface of the second insulating layer is reduced significantly. That is to say, the stepped portion generated at the surface of the second insulating layer is smaller because the second insulating layer is formed after the planarization of the first insulating layer. The stepped portion on the surface of the second insulating layer can further be reduced because a planarization process is also applied to the second insulating layer. Thus, the second insulating layer has a highly planarized surface to facilitate patterning of the resist on the second insulating layer to

a desired configuration. Furthermore, there is less possibility of a residue left at the stepped portion on the surface at the time of plug formation because the surface of the second insulating layer has a highly planarized surface. Therefore, the electrical reliability is improved without shorting occurring between conductive layers by the residue.

Because the first insulating layer is made to flow by a first predetermined temperature, and the second insulation film is made to flow by a second predetermined temperature that is lower than the first predetermined temperature, the first insulating layer will not attain a flowing state at the time of the flow of the second insulating layer. Therefore, deviation of the position of the second conductive layer formed on the surface of the first insulating layer due to a flow of the first insulating layer will not occur. That is to say, there is no offset in the position of the second conductive layer. Therefore, electrical reliability is improved because the second patterned layer is prevented from being electrically connected to another conductive layer caused by offset in position.

There will be described in detail a semiconductor chip embodying the present invention which includes a first conductive layer, a first insulating layer, a second conductive layer, a second insulating layer, and a third conductive layer. The first conductive layer is formed on the surface of a semiconductor substrate. The first insulation film has a first glass transition temperature and a planarised surface, and is formed to cover the first insulating layer. The second conductive layer is formed on the surface of the planarised first insulating layer. The second insulating layer has a second glass transition temperature that is lower than the first glass transition temperature and a planarised surface, and is formed to cover the second conductive layer. The third conductive layer is formed on the surface of the planarised second insulating layer.

Since this semiconductor chip includes a first insulating layer having a first glass transition temperature and a second insulating layer having a second glass transition temperature, it is possible during manufacture to apply a planarisation process individually for the first and second insulating layers. A surface stepped portion of the second insulating layer can be reduced effectively. That is to say, a step on the surface of the second insulating layer can be reduced because the second insulation film is formed after planarisation of the first insulation film. The stepped

portion on the surface of the second insulation film can further be reduced because the second insulation film is also subjected to planarization. Thus, the second insulation film will result in a highly planarized surface to facilitate patterning of the resist above the insulating layer to a desired configuration. Furthermore, a residue will not be left at the stepped portion at the time of plug formation because the second insulating layer has a highly planarized surface. Therefore, shorting caused by a residue will not occur between other conductive layers, so that the electrical reliability is improved.

Because the first insulating layer has a first glass transition temperature and the second insulating layer has a second glass transition temperature that is lower than the first glass transition temperature, there will be no flow of the first insulating layer when the second insulating layer located above the first insulating layer is subjected to a planarization process. Therefore, deformation of the second insulating layer formed on the surface of the first insulating layer due to a flow of the first insulating layer will not occur. In other words, the position of the second conductive layer will not be offset. Thus, the electrical reliability is improved because the second conductive layer will not be

electrically connected to another conductive layer by an offset in position.

An alternative embodiment includes a first conductive layer, a first insulating layer, a second insulating layer, a third insulating layer, a second conductive layer, a fourth insulating layer, a fifth insulating layer, a sixth insulating layer, and a third conductive layer. The first conductive layer is formed on the surface of a semiconductor substrate. The first insulating layer is formed on the semiconductor substrate to cover the first conductive layer. The second insulating layer has a first glass transition temperature, and is formed on the first insulating layer. The third insulating layer is formed on the second insulating layer. The second conductive layer is formed on the surface of the third insulating layer. The fourth insulating layer is formed on the third insulating layer to cover the surface of the second conductive layer. The fifth insulating layer is formed on the fourth insulating layer, and has a second glass transition temperature lower than the first glass transition temperature. The sixth

insulating layer is formed on the fifth insulating layer. The third conductive layer is formed on the surface of the fifth insulating layer.

This semiconductor device has the first, the third, the fourth, and the sixth insulating layers. The first insulating layer prevents impurities of an upper layer to diffuse into the first conductive layer and also prevents oxidation of the first conductive layer in the planarization process of the surface of the second insulating layer, for example. The third insulating layer fixes the second conductive layer to prevent deviation of the position of the second conductive layer, and also prevents impurities from a lower layer to diffuse into the second conductive layer in the planarization process of the surface of the fifth insulating layer, for example. The fourth conductive layer prevents deviation of the position of the second conductive layer, prevents diffusion of impurities from an upper layer into the second conductive layer, and prevents oxidation of the second conductive layer in the planarization process of the surface of the fifth insulating layer, for example. When a conductive layer is formed on the surface of the sixth insulating layer, for example, the sixth insulating layer prevents diffusion of impurities from a lower layer to this conductive layer and prevents corrosion therein.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view schematically showing a structure of a semiconductor device according to an embodiment of the present invention.

Figs. 2 - 6 are sectional views of the semiconductor device of Fig. 1 showing the manufacturing steps thereof.

Fig. 7 is an enlarged sectional view of a semiconductor device schematically showing a problem caused by the first impurity concentration and the second impurity concentration being identical.

Fig. 8 is a sectional view schematically showing a structure of a semiconductor device according to another embodiment of the present invention.

Fig. 9 is a sectional view schematically showing a structure of a semiconductor device according to a further embodiment of the present invention.

Fig. 10 is a graph showing the change in glass transition temperature in accordance with a change in the impurity concentration of the insulating layer.

Fig. 11 is a sectional view schematically showing a structure of a semiconductor device in which the first insulating layer is formed of a material different from that of the second insulating layer.

Fig. 12 is a graph showing the relationship between temperature and viscosity of various material.

Fig. 13 is a graph showing the flow angle θ in accordance with a change in the thickness of the insulating layer including impurities.

Fig. 14 shows the flow angle θ in accordance with a change in the ambient at the time of the planarization process.

Fig. 15 is a sectional view schematically showing a structure of a conventional semiconductor device.

Figs. 16 - 28 are sectional views of the conventional semiconductor device of Fig. 15 showing the manufacturing steps thereof.

Fig. 29 schematically shows the state of exposing a resist.

Fig. 30 is a sectional view schematically showing the optimum focusing position in exposing a resist.

Figs. 31 and 32 are sectional views schematically showing the state of problems encountered relevant to the focusing position in exposing the resist.

Fig. 33 is a sectional view schematically showing the state of a problem encountered by filling a connection hole with a plug.

Fig. 34 is a plan view schematically showing the state of a problem encountered by filling a connection

hole with a plug.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A semiconductor device according to an embodiment of the present invention will be described hereinafter.

Referring to Fig. 1, an isolation oxide film 11 of approximately 300 - 800nm in thickness is formed on the surface of a semiconductor substrate 10 of silicon. An element such as a MOSFET is formed in each region on the semiconductor substrate 10 isolated by the isolation oxide film 11. The MOSFET is implemented by impurity diffusion layers 14a and 14b forming the source and drain, a gate oxide film 12, and a polycrystalline silicon film 1 forming a gate.

The impurity diffusion layers 14a and 14b serving as the source and drain are formed on the surface of the semiconductor substrate 10. The gate oxide film 12 is formed on the surface of the semiconductor substrate 10 to extend over the source and drain of the impurity diffusion layers 14a and 14b. The polycrystalline silicon film 1 serving as a gate is formed on the surface of the gate oxide film 12. The first conductive layer is formed of a MOSFET including the polycrystalline silicon film 1. The silicon oxide film 13 is formed on the surface of the polycrystalline silicon film 1. A sidewall 15a is formed at the sidewalls of the gate oxide film 12, the

polycrystalline silicon film 1, and the silicon oxide film 13.

A thin silicon oxide film or a nitride film 2 is formed on the surface of the semiconductor substrate 10 having the MOSFET formed therein to cover each element. A planarized oxide film 3 having a first concentration of impurity is formed on the surface of the thin silicon oxide film/nitride film 2. This is the first insulation film. The oxide film 3 has a first glass transition temperature depending on the first impurity concentration. A glass transition temperature is defined as the temperature at which the insulating layer begins to flow. A connection hole is formed in the thin silicon oxide film/nitride film 2 and the oxide film 3. A portion of the surface of the impurity diffusion layer 14b or the polycrystalline silicon film 1 is exposed in the connection hole 18. The silicon oxide film 13 is also etched to form a connection hole exposing a portion of the surface of the polycrystalline silicon film 1. A plug 7 formed of polycrystalline silicon film is filled in the connection hole 18. The plug 7 is electrically connected to the impurity diffusion layer 14b or the polycrystalline silicon film 1. A polycrystalline silicon film 4a is formed in contact with the plug 7 on the surface of the oxide film 3 including impurities. A refractory metal

silicide 4b is formed on the surface of the polycrystalline silicon film 4a. The second conductive layer is formed of the polycrystalline silicon film 4a and the refractory metal silicide 4b. The second conductive layer is electrically connected to the impurity diffusion layer 14b or the polycrystalline silicon film 1 via the plug 7. An oxide film 5 having a second impurity concentration is formed on the surface of the oxide film 3 so as to cover the second conductive layer formed of the polycrystalline silicon film 4a and the refractory metal silicide 4b. The second impurity concentration of the oxide film 5 is higher than the first impurity concentration of the oxide film 3. The oxide film 5 is the second insulating layer. The oxide film 5 has a second glass transition temperature depending on the second impurity concentration. A second thin silicon oxide film or a nitride film 9 is formed all over the surface of the oxide film 5. A connection hole 19 is formed in the first thin silicon oxide film/nitride film 2, the oxide film 3, the oxide film 5, and the second thin silicon oxide film/nitride film 9. A portion of the surface of the impurity diffusion layer 14b not electrically connected to the plug 7 is exposed in the connection hole 19. The connection hole 19 is filled with a plug 8 formed of tungsten. The plug 8 is electrically

connected to the impurity diffusion layer 14b. An interconnection layer 6 of aluminum-copper alloy which is the third conductive layer is formed on the surface of the second silicon oxide film/nitride film 9 in contact with the plug 8. The interconnection layer 6 constitutes the third conductive layer.

The semiconductor device according to an embodiment of the present invention has a structure as described above.

A method of manufacturing this semiconductor device according to an embodiment of the present invention will be described hereinafter.

Referring to Fig. 2, the process up to the formation of a MOS transistor constituted by impurity diffusion layers 14a, 14b, the gate oxide film 12, and the polycrystalline silicon film 1 is similar to that of a conventional one and will not be repeated.

Referring to Fig. 3, a first thin silicon oxide film/nitride film 2 is formed to cover an element such as a MOS transistor by chemical vapor deposition. An oxide film 3 having the first impurity concentration is deposited all over the surface of the first silicon oxide film/nitride film 2. The oxide film 3 has the surface planarized by thermal treatment. Then, the whole surface of the oxide film 3 is etched to be reduced in thickness.

Referring to Fig. 4, a connection hole 18 is formed by photolithography and RIE in the oxide film 3 having a surface of favorable planarization. A polycrystalline silicon film is formed all over the surface of the oxide film 3 by chemical vapor deposition. This polycrystalline silicon film is etched by RIE to form a polycrystalline silicon plug 7 filling the connection hole 18. The polycrystalline silicon plug 7 is electrically connected to the polycrystalline silicon film 1. The polycrystalline silicon film 4a and the refractory metal thin film 4b are deposited on the whole surface of the oxide film 3. The polycrystalline silicon film 4a and the refractory metal thin film 4b are patterned by photolithography and RIE to form a second conductive layer having a composite film layer of a polycrystalline silicon film 4a and a refractory metal silicide 4b in contact with the polycrystalline silicon plug 7. The second conductive layer is electrically connected to the impurity diffusion layer 14b or the polycrystalline silicon film 1 via the polycrystalline silicon plug 7.

Referring to Fig. 5, an oxide film 5 having a second impurity concentration higher than the first impurity concentration is deposited on the surface of the oxide film 3 having the first impurity concentration so as to cover the second conductive layer. The oxide film 5 is

subjected to planarization at a thermal treatment temperature lower than that of the planarization of the oxide film 3. Following the planarization process, the oxide film 5 has all its surface etched to be reduced in thickness. A second thin silicon oxide film/nitride film 9 is deposited all over the surface of the planarized oxide film 5. The temperature of the thermal process for planarizing the oxide film 5 having the second impurity concentration must be set to a low level such that the oxide film 3 having the first impurity concentration is not softened. More specifically, the glass transition temperature of the oxide film 5 must be lower than that of the oxide film 3.

Referring to Fig. 6, a connection hole 19 is formed by photolithography and RIE in the first silicon oxide film/nitride film 2, the oxide film 3, the oxide film 5, the second silicon oxide film/nitride film 9. A portion of the surface of the impurity diffusion layer 14b not electrically connected to the polycrystalline silicon plug 7 is exposed in the connection hole 19. Impurities are implanted into the connection hole 19. A thermal treatment is applied to activate the implanted impurities. This thermal process is carried out at a temperature lower than the softening temperature of the oxide film 5. Then, a tungsten thin film including tungsten fluoride (WF_6) is

formed by chemical vapor deposition on the surface of the second silicon oxide film/nitride film 9. The tungsten thin film is etched by RIE to form a tungsten plug 8 filling the connection hole 19. An aluminum-copper alloy film is deposited by sputtering on the surface of the second silicon oxide film/nitride film 9. The aluminum-copper alloy film is patterned by photolithography and RIE to form a third conductive layer 6 of aluminum-copper alloy on the surface of the second silicon oxide film/nitride film 9 in contact with the tungsten plug 8. The third conductive layer 6 is electrically connected to the impurity diffusion layer 14b via the tungsten plug 8.

The semiconductor device according to an embodiment of the present invention is manufactured as described above.

The functions of the first and second silicon oxide films/nitride films 2 and 9 of Fig. 1 will be described hereinafter.

Referring to Fig. 1, the first thin silicon oxide film/nitride film 2 prevents the impurities of the oxide film 3 from diffusing into the underlying polycrystalline silicon film 1 and the impurity diffusion layers 14a and 14b during the thermal treatment of the planarization process. The thermal treatment for the planarization of the oxide film 3 may be carried out in an oxidizing

ambient such as steam ambient using a diffusion furnace. In this case, the first silicon oxide film/nitride film 2 prevents the oxidation of the polycrystalline silicon film 1 and impurity diffusion layers 14a and 14b.

The second thin silicon oxide film/nitride film 9 prevents the impurities of the oxide film 5 from diffusing into the overlying third conductive layer 6. In an ambient including humidity, boron oxide which is the impurity included in the oxide film 5 is precipitated at the surface layer to form acid. The second silicon oxide film/nitride film 9 suppresses corrosion of the interconnection caused by this acid to prevent degradation in the reliability of the interconnection. The second silicon oxide film/nitride film 9 further has an effect to improve the adherence of the resist in patterning the third conductive layer 6.

The method of forming the silicon oxide film, the silicon nitride film, the conductive layer, and the plug is not limited to that described in the above embodiment, and other methods may be used. Although examples of polycrystalline silicon and tungsten are described as the material of the plug in the present embodiment, aluminum or the like may be used. The impurities included in the interlayer insulating layer of the oxide film 3 or the oxide film 5 can be at least an impurity of phosphorus,

boron, arsenic, and the like. The impurity is preferably one that reduces the glass transition temperature of the interlayer insulating layer. Because a higher level of planarization can be obtained as the film is thicker, the deposited film thickness of the oxide film 3 and 5 is set to be substantially equivalent to the stepped portion. The method of reducing the thickness of the oxide films 3 and 5 by etching may be carried out according to a method by hydrofluoric acid (HF), by RIE, or by abrasion of a silicon oxide film by chemical mechanical abrasion (Journal of Electrochemical Society, vol. 138, page 1778). Although the above embodiment was described as having three layers of the first, the second, and the third conductive layers, the present invention is applicable to a semiconductor device having conductor layers more than three layers.

The disadvantage of the oxide film 3 and the oxide film 5 of Fig. 1 having the same impurity concentration is described hereinafter.

Referring to Fig. 7, the oxide film 5 having the second impurity concentration is subjected to thermal treatment for the planarization of the stepped portion, whereby the oxide film 5 is softened to attain a flowing state. If the impurity concentration of the oxide film 3 is identical to that of the oxide film 5, the oxide film 3

will also attain a flowing state during the thermal process for the planarization of the oxide film 5. This flow will deform the oxide film 3. The second conductive layers 4a and 4b formed on the surface of the oxide film 3 will be moved according to the deformation of the oxide film 3 to result in position offset. This deviation in the position of the second conductive layers 4a and 4b will incur a possibility of forming contact with the adjacent conductive region 8. If the second conductive layers 4a and 4b are brought into contact with the adjacent conductive region 8, there will be a disadvantage of generation of electrical defect in the semiconductor device.

A structure of a semiconductor device according to another embodiment of the present invention will be described hereinafter.

Referring to Fig. 8, a third thin silicon oxide film or a nitride film 20 is formed all over the surface of the third oxide film 3 having the first impurity concentration. The second conductive layers 4a and 4b are formed on the surface of the third silicon oxide film/nitride film 20 to be electrically connected to the impurity diffusion layer 14b or the polycrystalline silicon film 1. The structure of the other components is identical to that of the semiconductor device according to

the first embodiment of the present invention shown in Fig. 1, and their description will not be repeated.

The third thin silicon oxide film/nitride film 20 serves to fix the oxide film 3, and also serves to suppress the offset in position of the second conductive layers 4a and 4b occurring during the thermal treatment for the planarization of the oxide film 5. Furthermore, the third thin silicon oxide film/nitride film 20 prevents the impurities of the oxide film 3 having the first impurity concentration from diffusing into the second conductive layers 4a and 4b, and also the corrosion of the second conductive layers 4a and 4b due to the hygroscopicity of the impurities to improve the adherence of the resist at the time of pattern formation of the second conductive layers 4a and 4b.

A structure of a semiconductor device according to a further embodiment of the present invention will be described hereinafter.

Referring to Fig. 9, a third silicon oxide film/nitride film 20 is formed all over the surface of the oxide film 3 having the first impurity concentration. The second conductive layers 4a and 4b on the surface of the third thin silicon oxide film/nitride film 20 are electrically connected to the impurity diffusion layer 14b and the polycrystalline silicon film 1 via the plug 7. A

fourth thin silicon oxide film or a nitride film 21 is formed on the surface of the third thin silicon oxide film/nitride film 20 so as to cover the second conductive layers 4a and 4b. An oxide film 5 having the second impurity concentration is formed on the surface of the fourth thin silicon oxide film/nitride film 21. The structure of the remaining components is identical to that of the semiconductor device of the first embodiment shown in Fig. 1, and the description thereof will not be repeated.

The fourth silicon oxide film/nitride film 21 serves to fix the second conductive layers 4a and 4b, and also serves to suppress the offset of the position of the second conductive layers 4a and 4b caused by the thermal process for the planarization of the oxide film 5. Furthermore, the fourth silicon oxide film/nitride film 21 prevents the impurities of the oxide film 5 to diffuse into the underlying second conductive layers 4a and 4b, and also prevents oxidation of the second conductive layers 4a and 4b occurring during the thermal process for the planarization of the oxide film 5 carried out under an oxidizing ambient such as steam ambient using a diffusing furnace. Therefore, it is possible to introduce a large amount of impurities into the oxide film 5, so that the thermal process for planarization of the oxide film 5 can

be carried out at a lower temperature.

The present invention has different impurity concentrations in the first insulating layer and the second insulating layer in order to carry out the planarization process individually of the first and second insulating layers. More specifically, the second insulating layer is set to have a low glass transition temperature (softening point) in comparison with the first insulating layer by providing different impurity concentrations between the first and second insulating layers. A change in the glass transition temperature according to the impurity concentration is described in K. Nassau et al., J. Electrochem. Soc.: SOLID-STATE SCIENCE AND TECHNOLOGY, February 1985, pages 409 - 415 with reference to the relationship shown in Figs. 10(A) and (b). Referring to Figs. 10(a) and (b), the abscissa represent the impurity concentration and the ordinate represents the Tg: glass transition temperature. The present invention can employ the impurity concentration shown in Fig. 10.

For example, 5% by mol of B_2O_3 is introduced as the first impurity concentration into the oxide film 3 which is the first insulating layer. 10% by mol of B_2O_3 is introduced as the second impurity concentration into the oxide film 5 which is the second insulating layer. In

this case, the temperature of approximately 820°C is the glass transition temperature of the oxide film 3, and a lower temperature of approximately 700°C is the glass transition temperature of the oxide film 5, as shown in Fig. 10. The present invention is not limited to the impurity concentration shown in Fig. 10, and any impurity may be used provided that the glass transition temperature can be changed by modifying the impurity concentration and that a desirable planarization process can be carried out.

Although the present invention had the impurity concentration changed to modify the glass transition temperatures of the first and second insulating layers, the glass transition temperature thereof may be changed by the following method of (1). Furthermore, the level of planarization can be changed by the methods of (2) and (3).

(1) Change the material or the type of the impurity included in the first and second insulating layers.

(2) Change the thickness of the first and second insulating layers.

(3) Change the ambient of the thermal treatment for the planarization of the first and second insulating layers.

The method of (1) is shown with reference to the structure of a semiconductor device in Fig. 11. Referring

to Fig. 11, a first conductive layer 51 is formed on the surface of a semiconductor substrate 60. A first insulating layer 52 is formed to cover the first conductive layer 51. A second conductive layer 53 is formed on the surface of the first insulating layer 52. A second insulating layer 54 differing from the first insulating layer in material or the type of impurities included is formed so as to cover the second conductive layer 53. A third conductive layer 55 is formed on the surface of the second insulating layer 54.

In this structure, the first insulating layer 52 can include a silicon oxide layer, and the second insulating layer 54 can include a BPSG layer. More specifically, the first insulating layer 52 is subjected to planarization by a SOG (Spin On Glass) method, followed by the second insulating layer 54 covering the second conductive layer 53 on the first insulating layer 52 being subjected to a thermal treatment for planarization.

A difference in viscosity depending on a material under the same temperature is disclosed in the K. Nassau et al., J. Electrochem. Soc.: SOLID-STATE SCIENCE AND TECHNOLOGY, February 1985, pp. 409 - 415 with reference to Fig. 12. The temperature is plotted along the abscissa and the viscosity (unit of viscosity, log viscosity poise) is plotted along the ordinate in Fig. 12. In the present

invention, the materials or types of impurities (such as SiO_2, P_2O_3) shown in Fig. 12 can be employed. The present invention is not limited to the type of materials or impurities shown in Fig. 12, and any material or impurity can be employed provided that the glass transition temperature can be changed by altering the type of material or impurity and that a desirable planarization process can be carried out.

The method of (2) in which the level of planarization is changed according to the thickness of the insulating layer is disclosed in C.Y. Fu, IEDM 85, pp. 602 - 605 with reference to Fig. 13. The abscissa represents the thickness and the ordinate represents the level of planarization of the insulating layer flow angle θ in Fig. 13. That is to say, according to the above-described manufacturing method of the present invention, the oxide film 3 which is the first insulating layer is formed to a first film thickness and then planarized by a thermal treatment, and the oxide film 5 which is the second insulating layer is formed to a second film thickness that is greater than the first film thickness and then subjected to a thermal treatment for planarization. It can be appreciated from Fig. 13 that the flow angle θ is smaller after thermal treatment in proportion to a greater film thickness even if the temperature of the thermal

treatment is identical. This means that the oxide film 5 that is thicker than the oxide film 3 can be planarized to a degree identical to that of the oxide film 3 (flow angle θ) at a thermal treatment temperature that is lower than the thermal treatment temperature of the oxide film 3. The specimen employed is boron glass. The present invention can employ the thickness shown in Fig. 13 for the insulating layer. The present invention does not have the thickness of the insulating layer limited to that shown in Fig. 13, and any thickness can be employed provided that the level of planarization can be changed by altering the thickness of the first and second insulating layers and that a desirable planarization process can be carried out.

The method of (3) in which the level of planarization changes by modifying the ambient of the thermal treatment for the planarization of the insulating layer is disclosed in Jacques S. Mercier, Solid State Technology / July 1987, pp. 85 - 91 with reference to Figs. 14(a) and (b). The level of planarization (flow angle θ) is plotted along the ordinates of Figs. 14(a) and (b). The processing time duration and the temperature of planarization are plotted along the abscissa of Figs. 14(a) and (b), respectively. The specimen is a BPSG film having boron and phosphorus added. The present invention can employ the ambients

(steam ambient, nitrogen ambient) shown in Figs. 14(a) and (b) in the thermal process for planarization. The present invention is not limited to the ambients shown in Figs. 14(a) and (b), and any ambient can be employed provided that the level of planarization of the first and second insulating layers can be changed by modifying the ambient and that a desirable planarization process can be carried out.

The passivation film formed above the aluminum (Aℓ) interconnection layer is generally formed of a PSG film. However, this passivation film can not be subjected to a planarization process that requires a thermal treatment of high temperature because a temperature greater than 600°C will induce the possibility of fusion of the underlying aluminum interconnection layer.

The semiconductor device of the present invention includes a first insulating layer having a first glass transition temperature and a second insulating layer having a second glass transition temperature. Therefore, the second insulating layer has a highly planarized surface to facilitate patterning of the resist over the insulating layer to a desired configuration. Also, the problem of shorting between other conductive layers due to the existence of a residue is eliminated. Furthermore, the problem of the second conductive layer being

electrically connected to another conductive layer caused by an offset in the position of the second conductive layer can be prevented. Thus, the electrical reliability is improved.

The semiconductor device according to another aspect of the present invention includes a first insulating layer formed of a first material and a second insulating layer formed of a second material. Therefore, electrical connection of the second conductive layer to another conductive layer due to an offset in position of the second conductive layer does not occur. Thus, the electrical reliability is improved.

In a method of manufacturing a semiconductor device according to the present invention, the first insulating layer is made to flow at a first temperature and the second insulating layer is made to flow at a second temperature lower than the first temperature. Therefore, the second insulating layer has a highly planarized surface to facilitate the patterning of the resist over the insulating layer to a desired configuration. Also, the problem of shorting between conductive layers due to a residue is eliminated. Furthermore, because an electrical connection of the second conductive layer to another conductive layer caused by an offset in the position of the second conductive layer does not occur, the electrical

reliability is improved.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being limited only by the terms of the appended claims.

CLAIMS:

1. A method of manufacturing a semiconductor chip, comprising steps of:

forming a first patterned conductive layer on the main surface of a semiconductor substrate,

forming a first insulating layer to cover said first conductive layer,

planarising the free surface of said first insulating layer under a first condition,

forming a second patterned conductive layer on the planarised surface of said first insulating layer,

forming a second insulating layer to cover said second conductive layer,

planarising the free surface of said second insulating layer under a second condition differing from said first condition whereby the second insulating layer is planarised while the state of planarisation of said first insulating layer is maintained, and

forming a third patterned conductive layer on the planarised surface of said second insulating layer.

2. The method of manufacturing a semiconductor chip according to claim 1, wherein said first and second conditions are different ambient temperatures applied during planarisation.

3. The method of manufacturing a semiconductor chip

according to claim 1, wherein said first and second conditions are different ambient gases during planarisation.

4. The method of manufacturing a semiconductor chip according to claim 1, wherein said step of planarisation by a first condition comprises a step of spinning the substrate while material of said first insulating layer is applied, and wherein said step of planarisation by a second condition comprises a step of heating the second insulating layer up to a predetermined flow temperature.

5. A method of making a semiconductor chip comprising the steps of:

forming a first patterned layer of conductive material on the surface of a semiconductor substrate,

covering the first patterned layer with a first insulating layer of a material that flows at a first prescribed temperature,

heating the first insulating layer to the first prescribed temperature so as to planarise the upper free surface thereof,

forming a second patterned layer of conductive material on the first insulating layer,

covering the second patterned layer with a second insulating layer of a material that flows at a second

prescribed temperature lower than the first prescribed temperature, and

heating the second insulating layer to the second prescribed temperature so as to planarise the upper free surface thereof.

6. The method of making a semiconductor chip according to claim 5, wherein said first insulating layer and said second insulating layer (5) have an impurity introduced, said first insulating layer having a first impurity concentration, and said second insulating layer having a second impurity concentration differing from said first impurity concentration.

7. The method of making a semiconductor chip according to claim 6, wherein said second impurity concentration is higher than said first impurity concentration.

8. The method of making a semiconductor chip according to claim 5, wherein said first insulating layer is formed to a first thickness to cover said first conductive layer (1), and said second insulating layer is formed to a second thickness differing from said first thickness to cover said second conductive layer.

9. The method of making a semiconductor chip according to claim 8, wherein said second thickness is greater than said first thickness.

10. A semiconductor chip comprising:

a first patterned layer of conductive material formed on the surface of a semiconductor substrate;

a first insulating layer formed to cover said first patterned layer having a first glass transition temperature and a substantially planar upper surface;

a second patterned layer of conductive material formed on the surface of said first insulating layer;

a second insulating layer formed to cover said second patterned layer, having a second glass transition temperature, lower than said first glass transition temperature, and a substantially planar upper surface; and

a third patterned layer of conductive material, formed on the surface of said second insulating layer;

said first, second and third layers of conductive material providing an interconnective conductor structure of said semiconductor chip.

11. The semiconductor chip according to claim 10, wherein said first insulating layer and said second insulating layer comprise an impurity, said first insulating layer having a first impurity concentration, and said second insulating layer having a second impurity concentration different from said first impurity concentration.

12. The semiconductor chip according to claim 11, wherein said second impurity concentration is higher than said first impurity concentration.

13. The semiconductor chip according to claim 12, wherein the impurity introduced into said first insulating layer (3) and the impurity introduced into said second insulating layer are of the same type.

14. The semiconductor chip according to claim 13, wherein said impurity is selected from the group consisting of boron trioxide (B_2O_3), phosphorus pentoxide (P_2O_5), and germanium oxide (GeO_2).

15. The semiconductor chip according to claim 10, wherein said first insulating layer comprises a first impurity, and said second insulating layer comprises a second impurity of a type different from said first impurity.

16. The semiconductor chip according to claim 15, wherein said first impurity comprises phosphorus pentoxide, and said second impurity comprises boron trioxide.

17. The semiconductor chip according to claim 10, wherein said first insulating layer does not comprise an impurity, and said second insulating layer comprises an impurity.

18. The semiconductor chip according to claim 10, further comprising a third insulating layer formed between said semiconductor substrate and said first insulating layer to cover the surface of said first patterned conductive layer

19. The semiconductor chip according to claim 18, wherein said third insulating layer is one of a silicon oxide film and a silicon nitride film.

20. The semiconductor chip according to claim 10, further comprising a fourth insulating layer formed between said second insulating layer and said third patterned conductive layer.

21. The semiconductor device according to claim 20, wherein said fourth insulating layer is one of a silicon oxide film and a silicon nitride film.

22. The semiconductor chip according to claim 10,

further comprising a fifth insulating layer formed between said first insulating layer and said second patterned conductive layer.

23. The semiconductor chip according to claim 22, wherein said fifth insulating layer is one of a silicon oxide film and a silicon nitride film.

24. The semiconductor chip according to claim 10, further comprising a sixth insulating layer formed between said second patterned conductive layer and said second insulating layer to cover the surface of said second patterned conductive layer.

25. The semiconductor chip according to claim 24, wherein said sixth insulating layer is one of a silicon oxide film and a silicon nitride film.

26. The semiconductor chip according to claim 10, further comprising a third insulating layer formed between said semiconductor substrate and said first insulating layer to cover the surface of said first patterned conductive layer; a fourth insulating layer (9) formed between said second insulating layer; and said third patterned conductive layer. a fifth insulating layer formed between said first insulating layer and said second patterned conductive layer; a sixth insulating layer formed between said second insulating layer and said fifth insulating layer to cover said second patterned conductive layer.

27. The semiconductor chip according to claim 10, wherein said first insulating layer has a hole reaching to said first patterned conductive layer, wherein said first and second patterned conductive layers are electrically connected through said hole.

28. The semiconductor chip according to claim 10,

wherein said first patterned conductive layer comprises a gate electrode of a field effect transistor.

29. The semiconductor chip according to claim 10, wherein said second patterned conductive layer comprises an interconnection layer electrically connected to a source/drain region of a field effect transistor.

30. The semiconductor chip according to claim 10, wherein said third patterned conductive layer comprises an interconnection layer electrically connected to a source/drain region of a field effect transistor.

31. The semiconductor chip according to claim 10, wherein said first insulating layer comprises silicon oxide, and wherein said second insulating layer comprises Boron-doped Phospho-Silicate Glass (BPSG).

32. A semiconductor chip constructed, adapted and arranged to operate substantially as described hereinbefore with reference to and as shown in any one of figures 1,8 or 9 of the drawings.

33. A method of making a semiconductor chip, which method is performed substantially as described hereinbefore with reference to figures 2 to 6 and 10 to 14 of the drawings.

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