

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
30 March 2006 (30.03.2006)

PCT

(10) International Publication Number
WO 2006/034271 A1

(51) International Patent Classification⁷: **G02B 6/12, 6/13**

(21) International Application Number:
PCT/US2005/033651

(22) International Filing Date:
19 September 2005 (19.09.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/611,227 17 September 2004 (17.09.2004) US
60/643,196 12 January 2005 (12.01.2005) US

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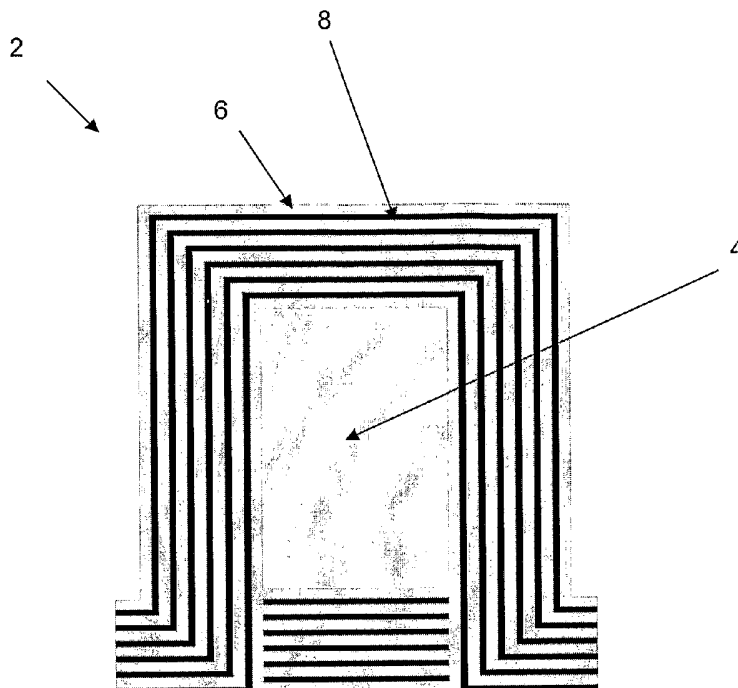
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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,

[Continued on next page]

(54) Title: **SILICON BASED ON-CHIP PHOTONIC BAND GAP CLADDING WAVEGUIDE**



(57) Abstract: A on-chip PC cladded waveguide structure includes a low index layer (4). A photonic crystal high index contrast cladding structure is utilized in guiding optical modes in the core. The photonic crystal cladding structure includes alternating layers of Si and Si₃N₄.

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RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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Published:

- *with international search report*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

SILICON BASED ON-CHIP PHOTONIC BAND GAP CLADDING WAVEGUIDE

PRIORITY INFORMATION

5 This application claims priority from provisional applications Ser. No. 60/643,196 filed January 12, 2005, which is incorporated herein by reference in its entirety, and Ser. No. 60/611227 filed on September 17, 2004, which is also incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

The invention relates to the field of waveguides, and in particular to an on-chip silicon-based Photonic Crystal (PC) cladded waveguide.

Recently, interest in guiding light within low-index materials (including air) has increased, with new devices that use a photonic band gap (PBG) or Bragg reflection to
15 confine light. Specific examples include 2D photonic crystal fibers and ARROW waveguides. Another example, the omniguide fiber, uses high index contrast concentric dielectric layers to enhance the mode confinement in a relatively simple structure. It is difficult to fabricate this structure on a silicon chip. However, the same principle of using 1D omnidirectional mirrors can be applied to an alternative structure that can be
20 fabricated with current microelectronics technology processes (CMOS compatible processes).

SUMMARY OF THE INVENTION

According to one aspect of the invention, there is provided a waveguide structure. The
25 waveguide structure includes a core structure that has low index materials. A photonic crystal cladding structure is utilized in guiding optical modes in the core. The photonic crystal cladding structure includes alternating layers of Si and Si₃N₄.

According to another aspect of the invention, there is provided a method of forming a waveguide structure. The method includes forming a core structure that has low index
30 materials. Furthermore, the method includes forming a photonic crystal cladding structure utilized in guiding optical modes in the core. The photonic crystal cladding structure includes alternating layers of Si and Si₃N₄.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram that illustrates a Photonic Crystal (PC) cladded waveguide;

FIG. 2 is a graph demonstrating the dispersion relation for modes within the band gap of an on-chip PC cladded waveguide;

FIG. 3A is a TEM image of cladding pairs including the bottom cladding PBG layers (Si/Si₃N₄) and SiO₂ core; FIG. 3B is a graph illustrating the measurement and simulation on absolute reflectivity of 5 pairs Si/Si₃N₄ layers;

FIG. 4A is a TEM image of the fabricated PC cladded channel waveguide; FIG. 4B The guided spot from the PC cladded channel waveguide;

FIG. 5 is a schematic diagram of the channel waveguide for use in achieving a sharp bend with either low index core or hollow core propagation;

FIG. 6 is a schematic diagram of a PBG rib waveguide; and

FIG. 7 is a schematic diagram of an asymmetric cladding.

DETAILED DESCRIPTION OF THE INVENTION

An on-chip silicon-based Photonic Crystal (PC) cladded waveguide is designed with low refractive index material for the core, and stratified high index contrast dielectric layers as the cladding. Due to the high index contrast of these materials with each other, they have a large photonic band gap, and may act as omnidirectional reflectors, which means light of all incident angles and polarizations is reflected within a range of wavelengths (e.g., near 1550 nm). In contrast with an index-guided waveguide, it is possible to confine light to a low index core (possibly air). The high index contrast allows the cladding thickness to be less than 2 microns, which is much thinner than the conventional silica optical bench waveguide. This structure can also be used to efficiently transmit light about bends much tighter than found in low index contrast index-guided waveguides.

An on-chip PC cladded waveguide configuration 2 is illustrated in FIG. 1. The inventive on-chip PC waveguide is designed with a low index core layer 4 of SiO₂ (n=1.46) and a high index contrast cladding consisting of pairs of layers 6, 8 of Si (n=3.5) and Si₃N₄ (n=2.0), which each have a quarter wavelength thickness at the target wavelength of 1550 nm. It combines the ease of layer-by-layer fabrication (as discussed below) with low losses that are associated with the presence of a highly reflective mirror on all sides

of the core. Guided modes can be found within the PBG of the 1D Si/Si₃N₄ PC. They can be predicted by comparison with a waveguide made from perfectly reflecting metallic walls.

The dispersion (relation between frequency and axial wavevector) for modes within the
5 band gap of an on-chip PBG waveguide for a core size of 2.5 microns square is shown in FIG. 2. The dispersion of the dielectric waveguide matches pretty well with the metallic waveguide, except for one key difference, which is the phase shift associated with reflections from the dielectric surface. For a perfect metal, the phase shift will always be π , but for a dielectric reflector, it will change with frequency, and generally be less than
10 π for the lower half of the gap and greater than π for the upper half of the gap.

Qualitatively, that leads to a prediction that modes for the metallic waveguide are "pushed" toward the center of the gap. Another consideration is power loss in this structure. Losses will decrease with increasing core size according to a power law, and decrease exponentially with the number of cladding layers (until other loss mechanisms
15 begin to dominate). Based on theoretical considerations, it seems that the TE₀₁ mode should be capable of achieving especially low losses due to its insensitivity to core size in one direction (which allows for the lowest loss in a given modal area).

The on-chip PC waveguide is fabricated with a CMOS-compatible process: the Low Pressure Chemical Vapor Deposition (LPCVD) is used to deposit the Si and Si₃N₄
20 cladding layers and the Low Temperature Oxide (LTO) method is used to make the oxide core. On a 6" Si chip, the 110 nm Si layer is deposited using the LPCVD method at a temperature of 625°C; the 194 nm Si₃N₄ layer is deposited using LPCVD at a temperature of 775°C. After the deposition of the bottom six and a half 1D PBG crystal layers, one can use the LTO method to deposit SiO₂ at 450°C, followed by a 900°C
25 anneal, to obtain a high quality oxide layer with a thickness between 4 and 6 microns. Lithography and high-density plasma etching is then used to define the waveguide core geometry. Finally, the same deposition method (LPCVD) is used to finish the top six and a half Si/Si₃N₄ 1D PC layers.

FIG. 3A is a TEM picture of a 1D PC slab fabricated using this technique, comprising of
30 7 layers 10 of Si₃N₄ and 6 layers 12 of poly-Si arranged in a periodic structure, with top SiO₂ layer 14 and on Si substrate 16. Clearly, the LPCVD deposition method is able to accurately control the thickness and flatness of the Si and Si₃N₄ layers 10, 12, both of which are important to prevent scattering losses. The high index contrast of the Si and Si₃N₄ pairs 10, 12 gives rise to a large PBG and high reflectivity (greater than 99%) for

only a few bilayers. This is illustrated in FIG. 3B, where the measured absolute reflectivity of five Si/Si₃N₄ bilayers 10, 12 is compared with a numerical calculation of the reflectivity of the ideal structure, using the transfer matrix method. The measurement and calculation are in very good agreement with each other, most importantly in the stop band, which extends from 1200nm to 2000nm.

A TEM picture of the final product, the fabricated on-chip PC channel waveguide 16, is shown in FIG. 4A. For the top PC cladding layers 18, each individual Si and Si₃N₄ layer 20, 22 is smooth, even at the curved surface, which shows the high quality of LPCVD's conformal step coverage. From FIG. 4A, one can conclude that CMOS compatible high and low index materials have good thermal and mechanical properties. The on-chip PC cladded waveguide loss is measured at 1550nm using the following procedure: light from a tapered optical fiber is coupled into the waveguide 16, then the guided light emerging from the other end is focused with a lens and collected with a camera. FIG. 4B shows the guided spot imaged by the camera, which demonstrates the presence of one or more well-defined guided modes, which are primarily concentrated in the low index SiO₂ core 24, the waveguide loss is as low as 4 dB/cm for a typical cross section 6μm x 12μm.

In this embodiment, a SiO₂ core 24 is used in the example of on-chip PC cladded channel waveguide structure. However, fabrication need not be restricted to SiO₂ – a hollow core could also be fabricated with a slight change in the procedure. This so-called "core freedom" would give rise to multiple applications, for example, transmission of high intensity beams (e.g., for a CO₂ laser) through a hollow core without absorption or nonlinearity, or to trap light or even modify the rate of emission from an optically active material. It also has unique group-velocity dispersion characteristics, which can be modified with changes to the core. Finally, the on-chip PC cladded waveguide has the advantage of relatively small dimensions, including a tight turning radius compared to low-contrast index-guided fibers.

The inventive photonic crystal cladded waveguide is fully compatible to the current CMOS technology. Si and Si₃N₄ are deposited using LPCVD method and high quality PC cladding layers are realized. Light guiding in the low index core is demonstrated. A thin PBG cladding, made possible by the large index contrast between the Si and Si₃N₄ layers, indicates the advantage of this device over traditional silica optical bench waveguides.

FIG. 5 illustrates a schematic diagram of the channel waveguide 31 for use in achieving a sharp bend. The channel waveguide 31 includes layers 30 of Si₃N₄ and layers 32 of

poly-Si arranged in a periodic structure. Also, the channel waveguide 31 includes a core 34 which allow the propagation of optical modes thru the bent region. Note the core 34 can be either a low index core or hollow core for purposes of this embodiment. Note the layers 30, 32 are formed according in the same fashion as the layers 6, 8, 10, 12 described in FIGs. 1, 3A, and 3B. The layers 30, 32 are arranged to be high index contrast pairs.

FIG. 6 illustrates a schematic diagram of a PBG rib waveguide 35. The rib waveguide 35 includes layers 38 of Si_3N_4 and layers 36 of poly-Si arranged in a periodic structure. Also, the rib waveguide 35 includes a core 40 which allow the propagation of optical modes. Note the core 40 can be a low index core for purposes of this embodiment. Note the layers 36, 38 are formed according in the same fashion as the layers 6, 8, 10, 12 described in FIGs. 1, 3A, and 3B. The layers 36, 38 are arranged to be high index contrast pairs.

FIG. 7 illustrates a schematic diagram of an asymmetric cladding 41 formed according to the invention. The asymmetric cladding 41 includes layers 46 of Si_3N_4 and layers 44 of poly-Si arranged in a periodic structure. Also, one side of the asymmetric cladding 41 includes a silicon dioxide core 42 which allow the propagation of optical modes. Note the core 42 can be another low index core for purposes of this embodiment and sized to between $2\mu\text{m}$ and $4\mu\text{m}$. On the other side of the asymmetric cladding is a Si substrate 48. Note the layers 44, 46 are formed according in the same fashion as the layers 6, 8, 10, 12 described in FIGs. 1, 3A, and 3B. The layers 44, 46 are arranged to be high index contrast pairs.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

- 1 1. A waveguide structure comprising:
 - 2 a core structure comprising low index materials;
 - 3 a photonic crystal cladding structure utilized in guiding optical modes in said core, said
 - 4 photonic crystal cladding structure comprises alternating layers of Si and Si₃N₄.
- 1 2. The waveguide structure of claim 1, wherein said core structure comprises silicon
2 dioxide.
- 1 3. The waveguide structure of claim 1, wherein said core structure comprises a size of a
2 2.5 microns square.
- 1 4. The waveguide structure of claim 1, wherein said a photonic crystal cladding
2 structure is fabricated with a CMOS-compatible process.
- 1 5. . The waveguide structure of claim 1, wherein said alternating layers of Si and Si₃N₄
2 are deposited using LPCVD method.
- 1 6. The waveguide structure of claim 1, wherein said alternating layers comprises a large
2 PBG and high reflectivity greater than 99%.
- 1 7. The waveguide structure of claim 1, wherein said core structure is fabrication using
2 the Low Temperature Oxide (LTO) method.
- 1 8. A method of forming a waveguide structure comprising:
 - 2 forming a core structure comprising low index materials;
 - 3 forming a photonic crystal cladding structure utilized in guiding optical modes in said
 - 4 core, said photonic crystal cladding structure comprises alternating layers of Si and
 - 5 Si₃N₄.
- 1 9. The method of claim 8, wherein said core structure comprises silicon dioxide.
- 1 10. The method of claim 8, wherein said core structure comprises a size of a 2.5 microns
2 square.
- 1 11. The method of claim 8, wherein said a photonic crystal cladding structure is
2 fabricated with a CMOS-compatible process.

- 1 12. . The method of claim 8, wherein said alternating layers of Si and Si₃N₄ are
2 deposited using LPCVD method.
- 1 13. The method of claim 8, wherein said alternating layers comprises a large PBG and
2 high reflectivity greater than 99%.
- 1 14. The method of claim 8, wherein said core structure is fabrication using the Low
2 Temperature Oxide (LTO) method.

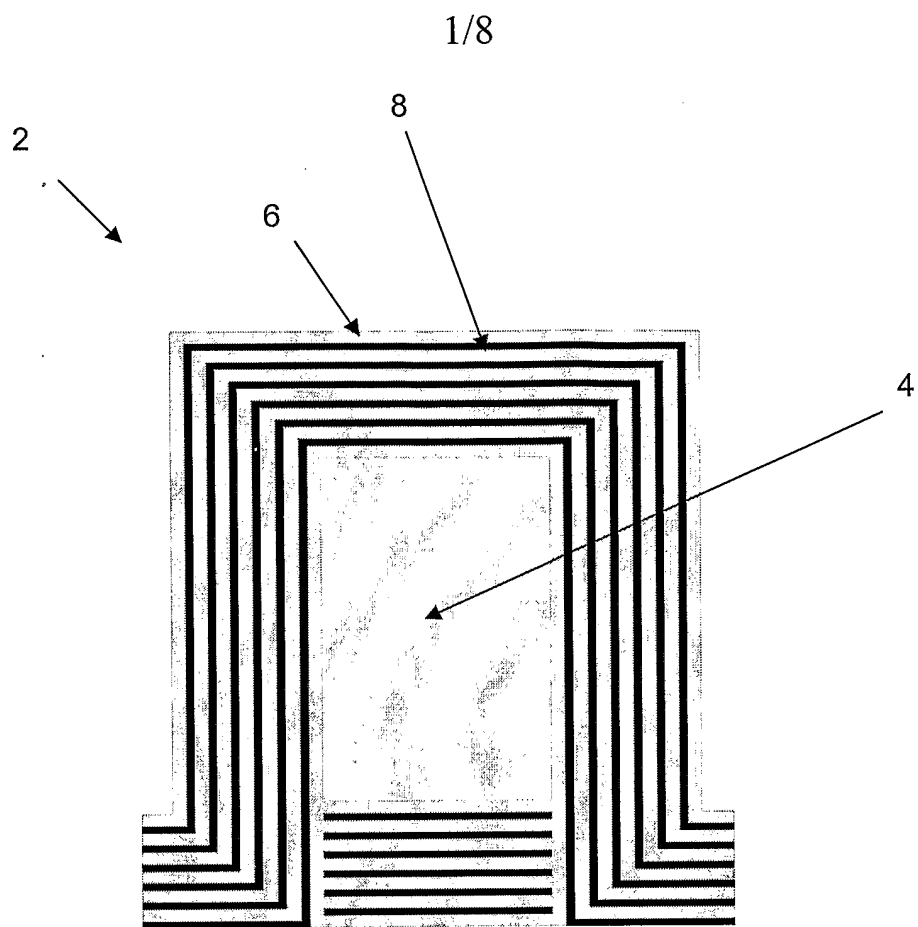


FIG. 1

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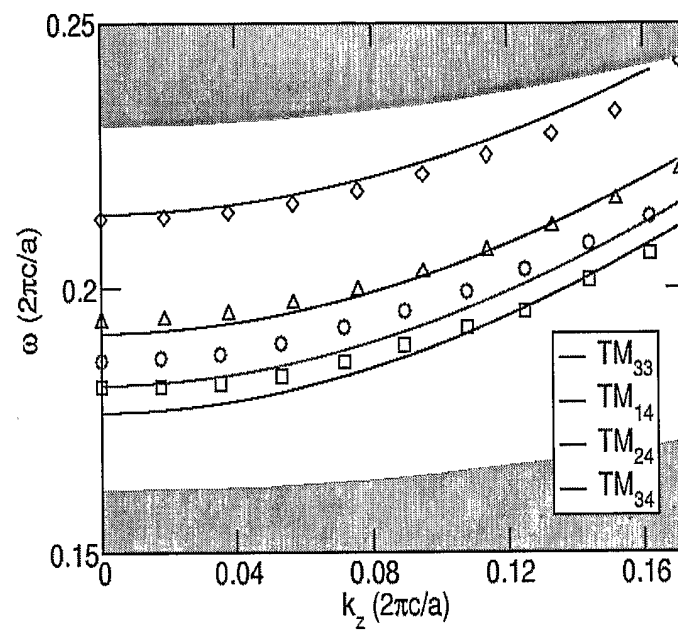


FIG. 2

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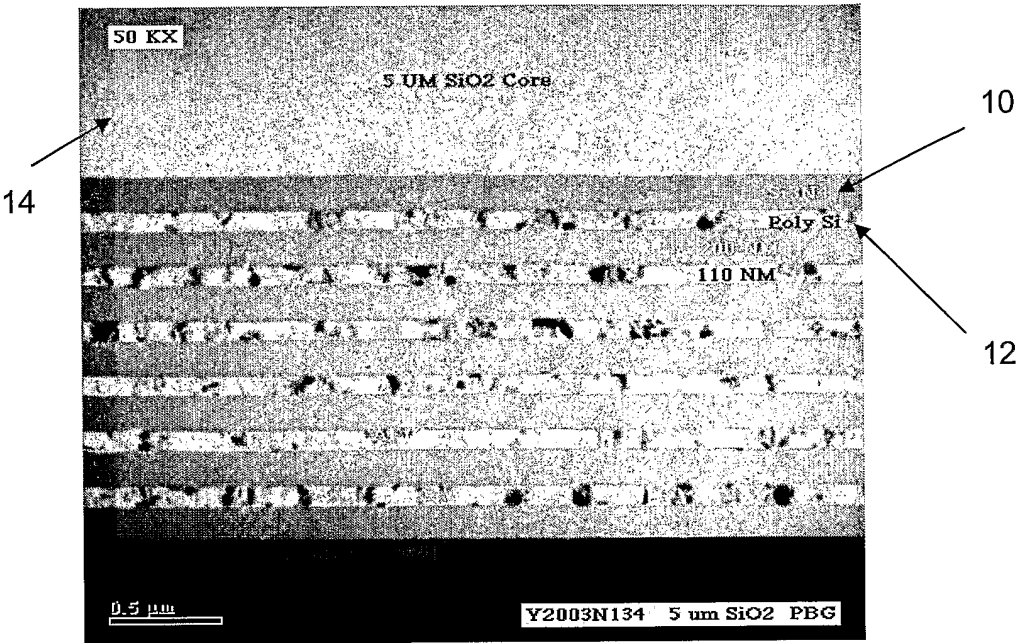


FIG. 3A

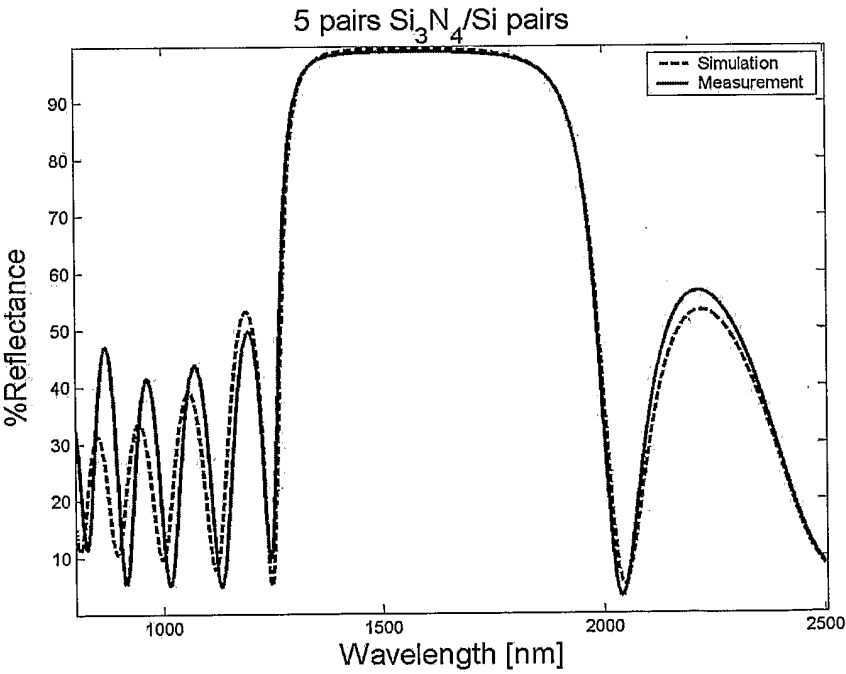


FIG. 3B

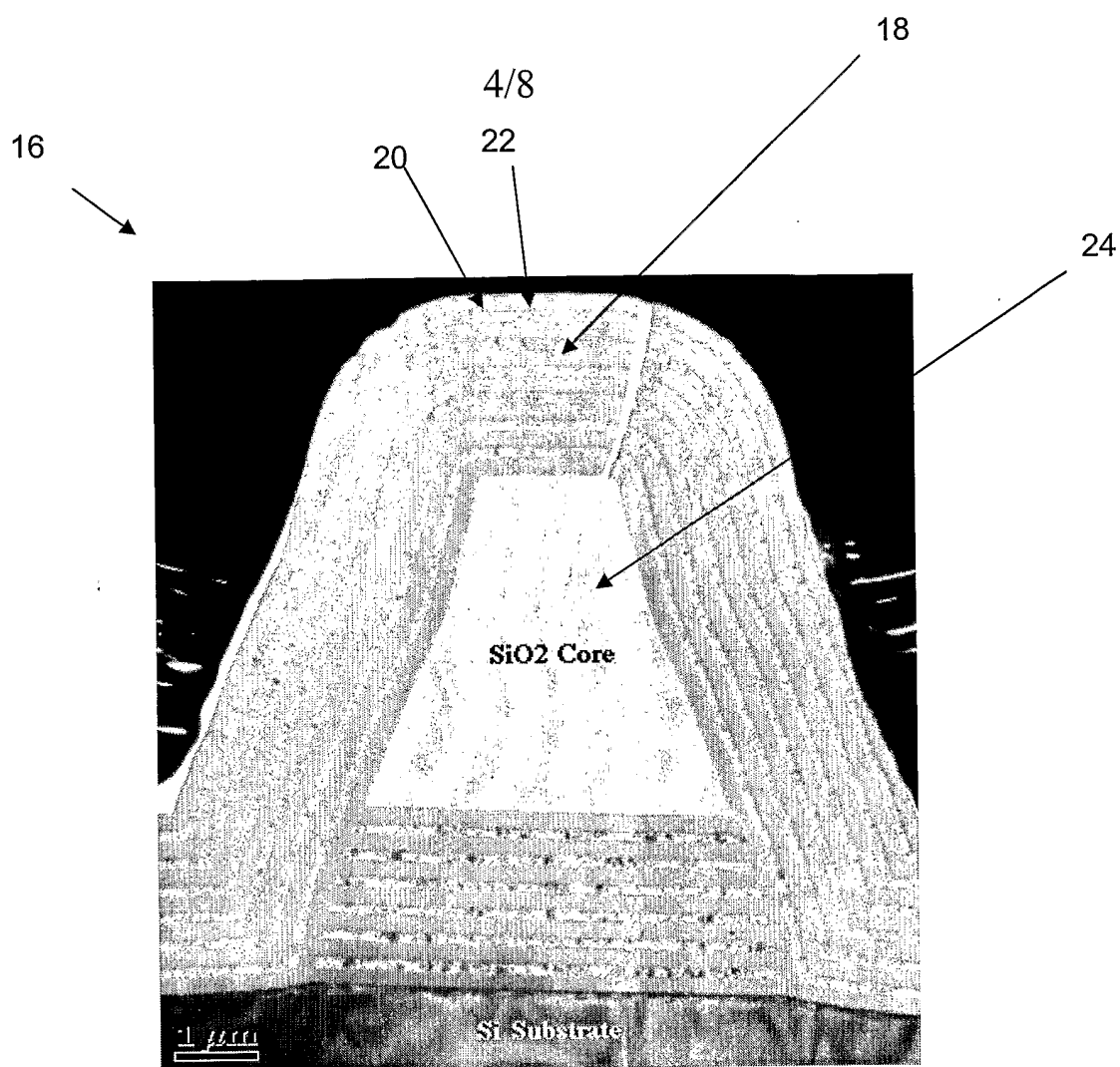


FIG. 4A

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FIG. 4B

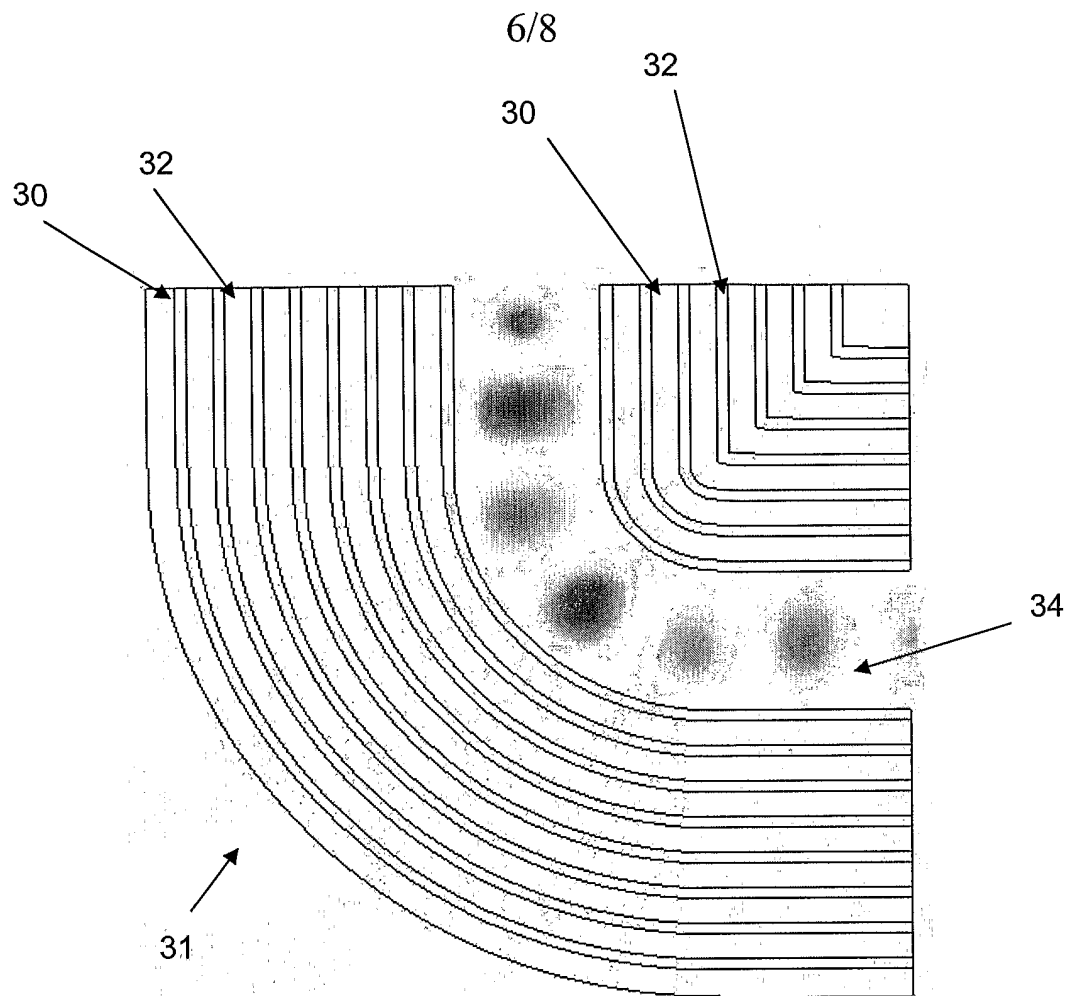


FIG. 5

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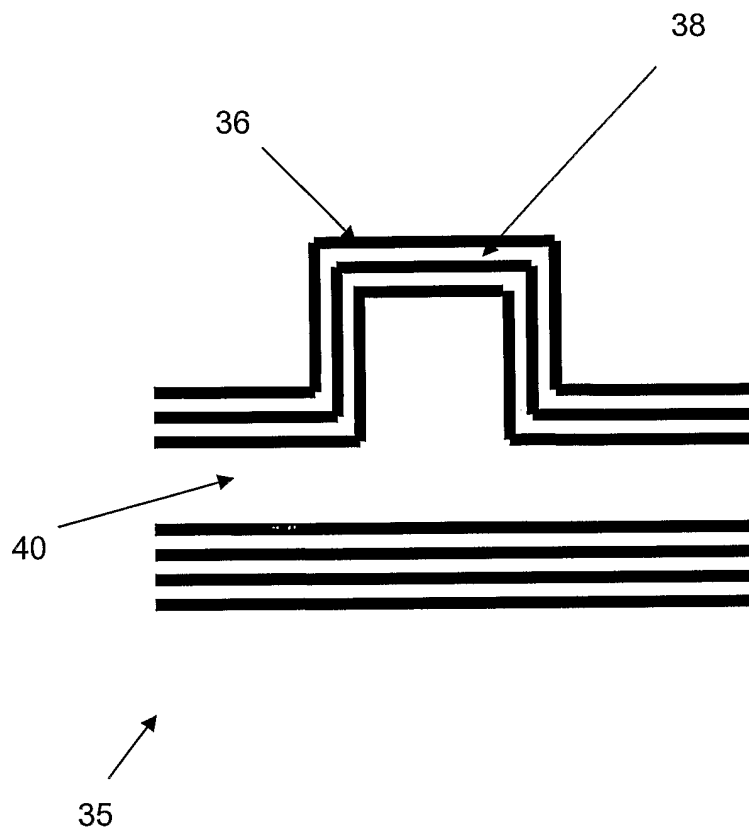


FIG. 6

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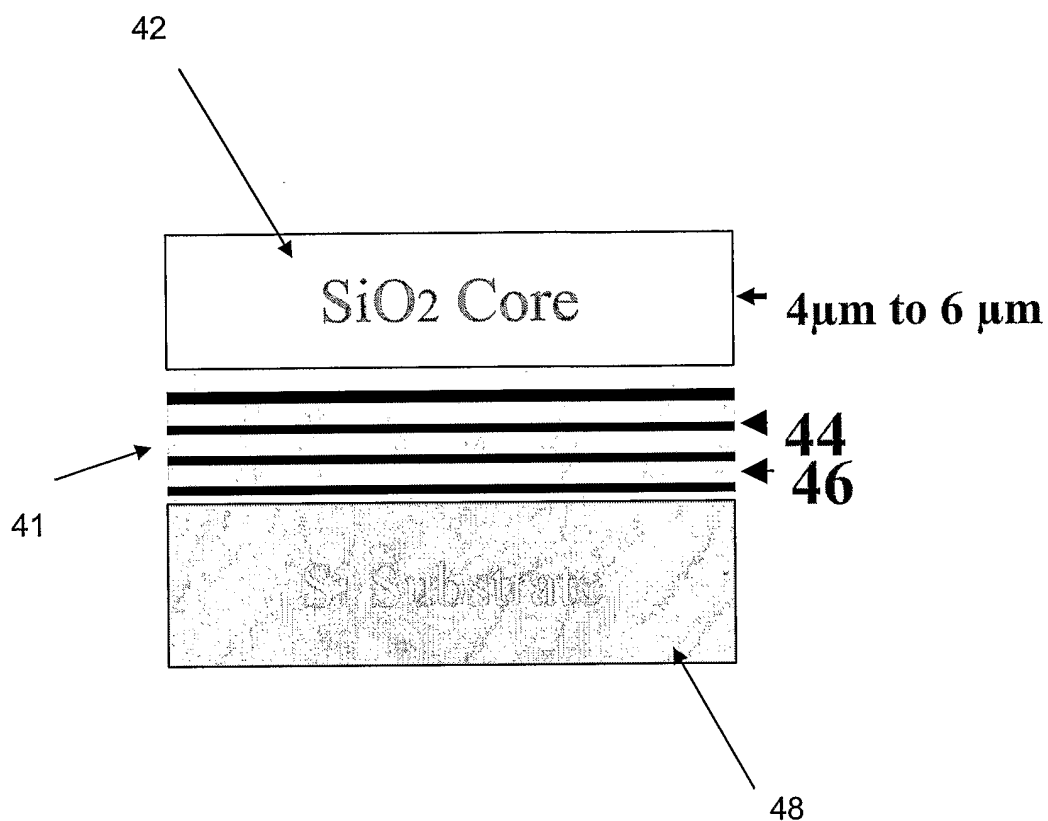


FIG. 7

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/033651

A. CLASSIFICATION OF SUBJECT MATTER
G02B6/12 G02B6/13

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	YI Y; BERMEL P; AKIYAMA S; SANDLAND J G; XIAOMAN DUAN; KIMERLING L C: "Low loss photonic crystal cladding waveguide with large photonic band" CONTRIBUTION W3.4.1 IN ENGINEERED POROSITY FOR MICROPHOTONICS AND PLASMONICS, BOSTON, MA, USA, MRS SYMPOSIUM - 2-4 DEC. 2003 - PROC., no. 1-55899-735-0, 2004, XP008058716 Boston, MA, USA the whole document ----- -/--	1-14

☒ Further documents are listed in the continuation of box C.

☐ Patent family members are listed in annex.

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Date of the actual completion of the international search

20 January 2006

Date of mailing of the international search report

02/02/2006

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/033651

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KIMERLING L C; DAL NEGRO L; SAINI S; YI Y; AHN D; AKIYAMA S; CANNON D; LIU J; ET AL: "Monolithic silicon microphotronics" SILICON PHOTONICS TOPICS IN APPLIED PHYSICS, vol. 94, 2004, pages 89-119, XP008058719 Berlin Heidelberg page 113 - page 114 -----	1,2,4-9, 11,13
X	D. YIN, H. SCHMIDT, J. P. BARBER, AND A. R. HAWKINS: "Integrated ARROW waveguides with hollow cores" OPT. EXPRESS, vol. 12, no. 12, 14 June 2004 (2004-06-14), pages 2710-2715, XP002363659 the whole document -----	1,2,4-9, 11-14