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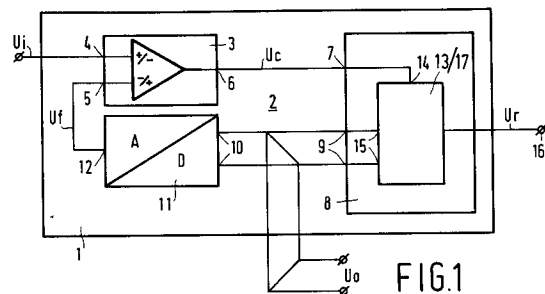
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Hold circuit, mobile station, base station and digital radio communication system comprising such a hold circuit.

In a system for digital radio communication (20) with dynamic channel allocation, the maximum signal strength (U_{max}) is measured in a time slot (TS). For this purpose, the peak value is to be held. This may be effected in the receive section of both a base station (21) and a mobile station (22). An example of such a digital radio communication system (20) is a system operating according to the DECT standard. A hold circuit (1) is known which holds the peak value of an analog input signal (U_i) in analog form. It is an object of this invention to hold the peak value in digital form. To this end the hold circuit (1) comprises in the feedback loop (2) a digital hold element (8) and a digital/analog converter (11) for feeding back the output signal (U_o) to the comparator element (3). In an exemplary embodiment the digital hold element (8) is a counter (13). The invention likewise relates to a hold circuit (1) which holds the minimum value of the input signal (U_i).



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The invention relates to a hold circuit which comprises a comparator element included in a feedback loop, the comparator element having a first input for receiving an analog input signal, and comprises a hold element coupled to the comparator element for holding an extreme value of the analog input signal, the comparator element having a second input for receiving a feedback signal which is a measure for the extreme value.

The invention further relates to a base station and a mobile station intended to receive a radio signal modulated with digital data, which base and mobile stations comprise such a hold circuit.

The invention further relates to a digital radio communication system comprising at least one base station and/or one mobile station, which system comprises such a hold circuit. Such a system may be, for example, a cordless telephone system operating according to the DECT standard.

Such a hold circuit is known as a peak value hold circuit from "Design of MOS VLSI Circuits For Telecommunications" by Yannis Tsvividis and Paolo Antognetti, Prentice Hall 1985. A MOS transistor whose source is connected to a capacitor used as a hold element is controlled by an output voltage of a comparator element. A first input of the comparator element is supplied with an input voltage. The voltage across the capacitor is fed back to a second input of the comparator element. As long as the input voltage exceeds the voltage across the capacitor, the transistor is turned on and the capacitor charged. Once the voltage across the capacitor has exceeded or is equal to the input voltage, the transistor is turned off. The voltage across the capacitor then remains constant.

With such a hold circuit an analog peak value is obtained. In a digital radio communication system with dynamic channel allocation the maximum signal strength is to be measured in a time slot. This may be done by a base station as well as a mobile station. In such a system it is inconvenient to hold the peak value as an analog value. Especially in a cordless telephone system, such as DECT, a digital peak value is even prescribed. The digital peak value could easily be obtained by means of an analog-digital (A/D) converter following the known peak value hold circuit, it is true, but this leads to a more complicated, more expensive arrangement. In addition, an efficient circuit integration asks for a fast change-over from a digital signal environment to digital signals.

It is an object of the invention to provide a hold circuit of the type defined in the opening paragraph which does not have said inconvenience adhered to it.

A hold circuit according to the invention is characterized in that the hold element is a digital hold element a digital output signal of which forms

the extreme value and in that the feedback loop comprises a digital-analog (D/A) converter coupled to the hold element to convert the digital output signal into the feedback signal. This provides a simple and cost-effective circuit which, in addition, requires little space when integrated. Such a circuit usually forming part of a larger unit may also be tested in a digital test environment, a requirement increasingly made on IC's.

An embodiment of the invention is characterized in that the hold element is a counter of which an enable input is coupled to an output of the comparator element. This provides a highly simple embodiment. In addition, the counter may be reset simply and fast with a digital reset signal for rapidly succeeding measurements. In the April issue of 1967 of Electromechanical Design on page 24 a servo A/D converter is described which also comprises a counter, a D/A converter and a comparator element in the feedback loop. Once the servo A/D converter has been started by a start pulse, an input signal of the A/D converter is sampled. A digital sawtooth-shaped signal then increases until its value exceeds the input signal. A conversion result is then available on the output of the A/D converter. In consequence, the A/D converter is not arranged for determining the peak value of a signal during a specific measuring interval.

The invention will be further explained with reference to a drawing in which:

Fig. 1 shows a hold circuit according to the invention,

Fig. 2 shows signals in the hold circuit plotted against time,

Fig. 3 shows a digital radio communication system,

Fig. 4 shows a base station or a mobile station intended to receive a radio signal modulated with digital data, and

Fig. 5 shows a time slot of a system operating according to the DECT standard.

Fig. 1 shows a peak value hold circuit 1 according to the invention, comprising a feedback loop 2 with a comparator element 3 which comparator element has a first input 4 for receiving an input signal U_i and a second input 5 for receiving a feedback signal U_f . An output 6 of the comparator element 3 applies a control signal U_c to an input 7 of a digital hold element 8. An output 9 of the digital hold element 8 produces a digital output signal U_o which is also applied to an input of a D/A converter 11. An output 12 of the D/A converter 11 is coupled to the second input of the comparator element 3. As long as the input signal U_i exceeds the feedback signal U_f , the comparator element 3 produces the control signal U_c , causing the voltage U_o on the output 9 of the digital hold element 8 to increase. If the input voltage U_i is smaller than or

equal to the feedback voltage U_f , the output voltage U_o remains constant. In this manner the peak value of the input voltage U_i is held in digital form for a specific period of time. If the (+)input and the (-)input of the comparator element 3 are reversed, a hold circuit 1 will be obtained that holds the minimum value of an input voltage (U_i).

In an embodiment of the hold circuit 1 according to the invention, the digital hold element 8 is a counter 13, an enable input 14 of which forms the input 7 to the hold element 8 and an output 15 of which forms the output 9 of the hold element 8. As long as the input signal U_i exceeds the feedback signal U_f , the counter 13 continues counting, so that the output value U_o continues rising. Once the feedback signal U_f has exceeded the input signal U_i , the counter 13 continues counting, so that the output value U_o continues rising. Once the feedback signal U_f has exceeded the input signal U_i , the counter stops counting and the output value U_o of the counter 13 remains constant. The counter 13 may be reset by a reset signal U_r applied through the reset input 16. In the case where the hold circuit 1 holds the minimum value, the hold element 8 may be arranged as a down counter 17.

In Fig. 2 the input voltage U_i and the feedback voltage U_f are plotted against time in the case where the hold circuit holds the peak value. The feedback voltage U_f is the analog equivalent to the digital output voltage U_o . The feedback voltage U_f trails the input voltage U_i until it exceeds the input voltage U_i . The voltage U_f then remains constant. Once the input voltage U_i has exceeded the feedback voltage U_f , the voltage U_i in its turn trails the voltage U_f .

Fig. 3 shows a digital radio communication system 20 comprising a plurality of mobile stations MS1, MS2, MS3, MS4 and MS5, and a plurality of base stations BS1, BS2 and BS3. Each of these base stations BS1, BS2 and BS3 is coupled to an exchange 23 over respective data lines D1, D2 and D3.

Fig. 4 shows a telecommunication system 30 which is capable of both transmitting and receiving signals *via* an antenna 31. Such a telecommunication system 30 may be both a mobile station 21 and a base station 22 of the digital radio communication system 20. A transmit or receive function of the telecommunication system 30 is selected by a switch 34. The switch 34 is connected to a receive section 35 and a transmit section 36. A transmit/receive frequency f may be set by a local oscillator 37. The peak value hold circuit 1 is coupled to the receive section 35. The telecommunication system 30 is controlled by a control means 38. In the case where the system 30 is the mobile station 21, the control means 38 is coupled to a signal processing unit 39 which unit customarily

comprises an A/D converter 40, a D/A converter 41 and a CODEC 42 for converting and (de)coding speech in digitized speech and *vice versa*. For the purpose of speech, a microphone 43 and a loudspeaker or other acoustic converter 44 are coupled to the signal processing unit 39 and for the purpose of data, for example, a facsimile device 45 *via* a modem 46. In the case where the telecommunication system 30 is the base station 22, the signals are transmitted to an exchange 23 over data lines D1, D2 or D3.

Fig. 5 shows a time slot TS of the digital radio communication system 20 operating according to what is commonly referred to as the DECT standard (Digital European Cordless Telecommunications). The time slot TS is 416.7 μ s long, an interval DS = 364.5 μ s of which being used for transferring data. The remaining period of time within a time slot is called guard space GS. According to the DECT standard a maximum value U_{max} of the input signal U_i is to be determined during the interval in which data are transferred, including a preceding period ES1 of 10 μ s and a subsequent period ES2 of 10 μ s. In the remaining time of a time slot the maximum value U_{max} is read out and the counter 13 reset.

Claims

1. Hold circuit (1) which comprises a comparator element (3) included in a feedback loop (2), the comparator element having a first input (4) for receiving an analog input signal (U_i), and comprises a hold element (8) coupled to the comparator element (3) for holding an extreme value (U_o) of the analog input signal (U_i), the comparator element (3) having a second input (5) for receiving a feedback signal (U_f) which is a measure for the extreme value (U_o), characterized in that the hold element (8) is a digital hold element a digital output signal of which forms the extreme value (U_o) and in that the feedback loop (2) comprises a digital-analog converter (11) coupled to the hold element (8) to convert the digital output signal (U_o) into the feedback signal (U_f).
2. Hold circuit as claimed in Claim 1, characterized in that the hold element (8) is a counter (13), of which an enable input (7) is coupled to an output (6) of the comparator element (3).
3. Hold circuit as claimed in Claim 2, characterized in that the counter has a reset input (16).
4. Hold circuit as claimed in Claim 1, characterized in that the hold element (8) is a down counter (13) whose enable input (7) is coupled

to an output of the comparator element (3).

5. Base station (22) intended to receive a radio signal modulated with digital data, which base station comprises a hold circuit (1) as claimed in Claim 1, 2 or 3. 5
6. Mobile station (21) intended to receive a radio signal modulated with digital data, which mobile station comprises a hold circuit (1) as claimed in Claim 1, 2 or 3. 10
7. Digital radio communication system (20) comprising at least one base station (22) as claimed in Claim 5 and/or at least one mobile station (21) as claimed in Claim 6. 15

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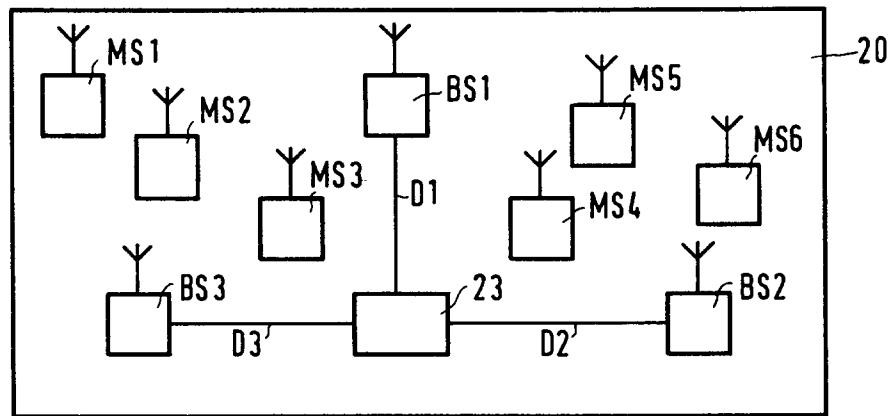
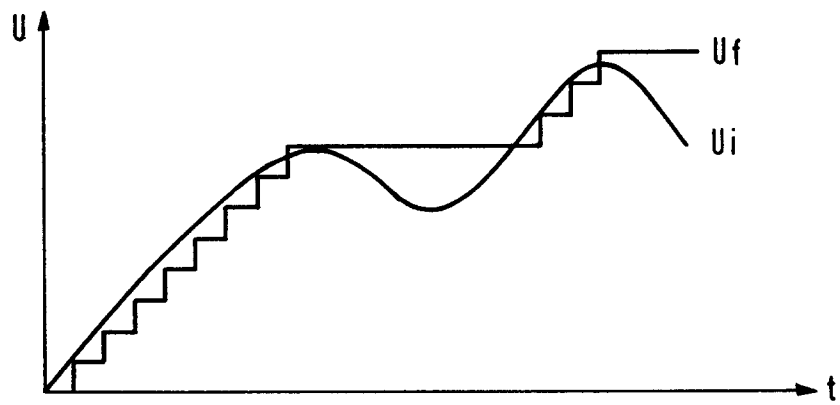
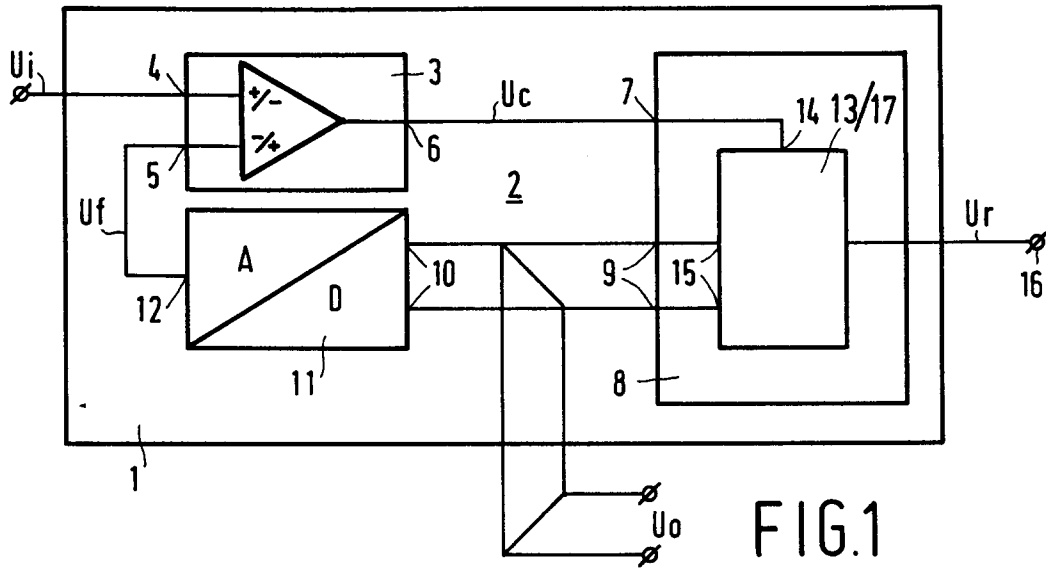


FIG.3

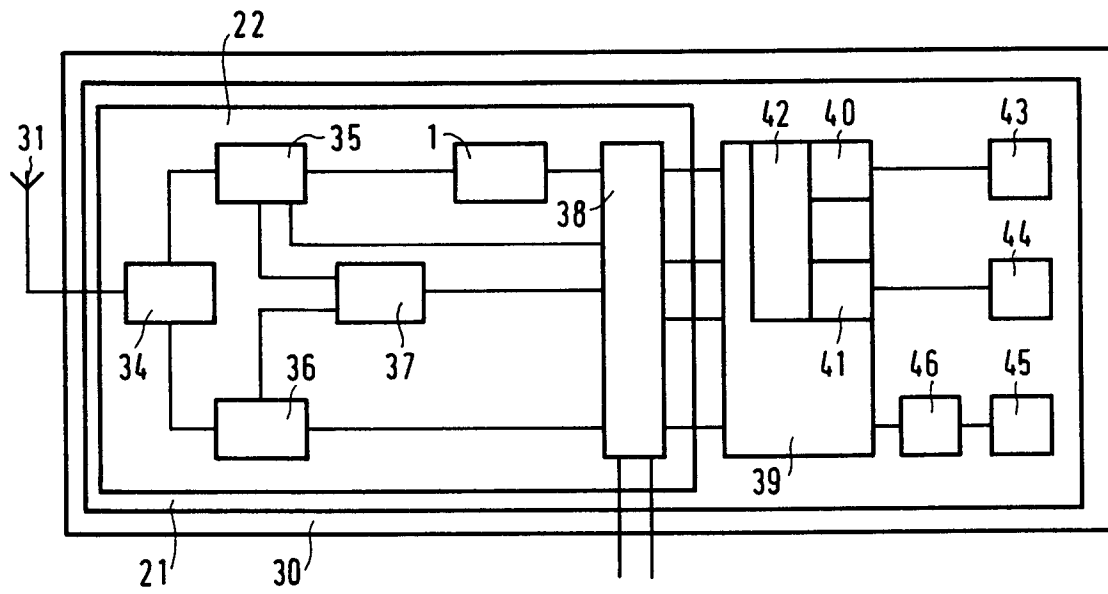


FIG. 4

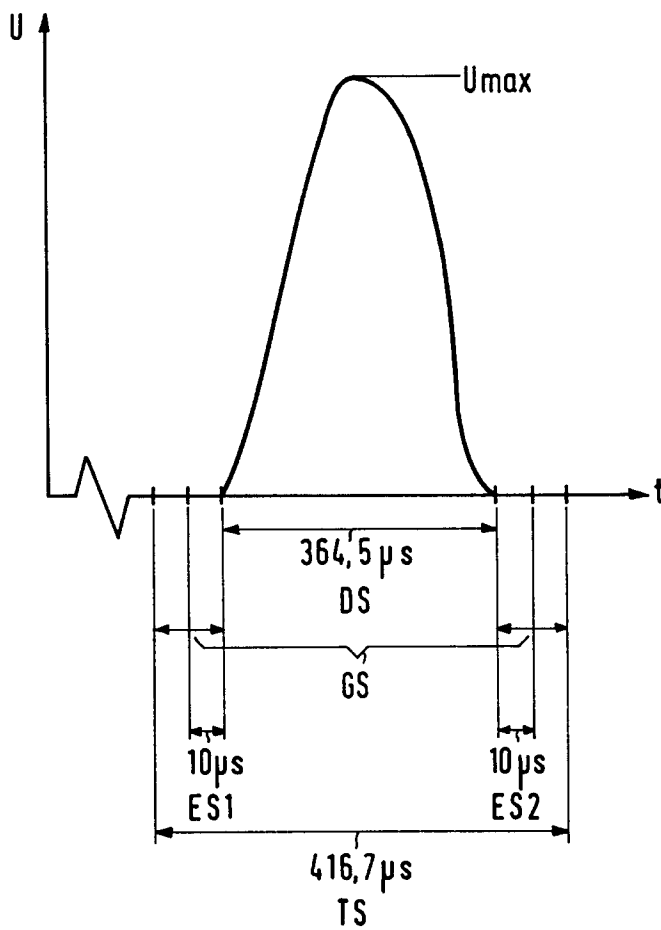


FIG. 5