ELECTROLYTIC GOLD PLATING METHOD OF PRINTED CIRCUIT BOARD

Disclosed is an electrolytic gold plating method of a PCB, which includes (A) forming an electrolytic copper-plated layer, corresponding to a predetermined copper plating resist pattern, on a substrate, (B) forming an electrolytic gold-plated layer, corresponding to a predetermined gold plating resist pattern, on the substrate using an outer layer of the substrate as a first incoming line for electrolytic gold plating use, and (C) removing a portion of the outer layer of the substrate, on which the electrolytic copper-plated layer is not coated.
FIG. 1a
PRIOR ART

FIG. 1b
PRIOR ART

FIG. 1c
PRIOR ART
FIG. 1f
PRIOR ART

FIG. 1g
PRIOR ART
FIG. 1h
PRIOR ART

FIG. 1i
PRIOR ART
FIG. 1j
PRIOR ART

FIG. 1k
PRIOR ART
FIG. 3e

FIG. 3f
ELECTROLYTIC GOLD PLATING METHOD OF PRINTED CIRCUIT BOARD

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention pertains, in general, to an electrolytic gold plating method of a printed circuit board (PCB) and, in particular, to an electrolytic gold plating method of a PCB, in which a copper outer layer or an electroless copper-plated layer of a substrate is used as an incoming line for plating use to form an electrolytic gold-plated layer.

[0003] 2. Description of the Prior Art

[0004] Generally, a process of mounting passive components, active integrated circuits, and the like on a PCB according to a wire bonding manner is classified into an electrolytic gold plating process and an electroless gold plating process.

[0005] In this regard, the electroless gold plating process has a disadvantage of a separation occurring at an interface between copper and nickel during a wire bonding process of the PCB, and thus, the electrolytic gold plating process is more frequently used than the electroless gold plating process. Unlike other processes of surface-treating the PCB without using electricity, the electrolytic gold plating process is advantageous in that an electrolytic gold-plated layer is thick, the productivity is relatively high, and a relatively high peel strength reliability is secured.

[0006] The electrolytic gold plating process may be classified into an electrolytic soft gold plating process and an electrolytic hard gold plating process. In this respect, the electrolytic soft gold plating process is applied to the wire bonding process of typical semiconductor package products because gold particles plated on the PCB are relatively large, porous, and have a relatively low density. On the other hand, the electrolytic hard gold plating process is applied to produce a contact terminal for a battery of a mobile phone because the gold particles plated on the PCB are densely arranged, and have a relatively high density and excellent strength.

[0007] In order to better understand the background of the present invention, a description will be given of the production of a conventional PCB, below.

[0008] FIGS. 1a to 1k are sectional views illustrating the production of the conventional PCB, and FIG. 2 is a plan view of the conventional PCB produced according to a procedure of FIGS. 1a to 1k. At this time, FIGS. 1a to 1k are the sectional views taken along the line a-a' of FIG. 2.

[0009] With reference to FIG. 1a, upper and lower copper foil layers 11b are coated on upper and lower sides of an insulating resin layer 11a to produce a copper clad laminate 11.

[0010] Referring to FIG. 1b, a via hole (b) is formed through the copper clad laminate 11 to electrically connect the upper and lower copper foil layers 11b to each other.

[0011] In FIG. 1c, an electroless copper plating process is conducted to allow an electric current to flow through the via hole (b), thereby forming an electroless copper-plated layer 12 on the upper and lower copper foil layers 11b and a wall of the via hole (b).

[0012] Subsequently, an electrolytic copper plating process is conducted to form an electrolytic copper plating layer 13 on the electroless copper-plated layer 12 on the upper and lower copper foil layers 11b and the wall of the via hole (b) as shown in FIG. 1d. At this time, the electrolytic copper-plated layer 13 has excellent physical properties.

[0013] Coated on the electrolytic copper-plated layer 13, a dry film 20 is exposed and developed using a first artwork film, having a predetermined pattern printed thereon, to be patterned as shown in FIG. 1e. The pattern of the first artwork film may be exemplified by a circuit pattern, a land of the via hole (b), a wire bonding terminal pattern, and an incoming line pattern.

[0014] In FIG. 1f, the resulting copper clad laminate 11 is dipped in an etching solution to remove a portion of the upper and lower copper foil layers 11b, electroless copper-plated layer 12, and electrolytic copper-plated layer 13, which is not coated with the patterned dry film 20. At this time, the patterned dry film 20 acts as an etching resist.

[0015] The dry film 20 coated on the patterned copper clad laminate 11 is then removed as shown in FIG. 1g.

[0016] Subsequently, a solder resist 14 is coated on the patterned copper clad laminate 11, and preliminarily dried as shown in FIG. 1h.

[0017] Referring to FIG. 1i, a second artwork film 30, having a solder resist pattern printed thereon, is mounted on the solder resist 14 coated on the patterned copper clad laminate 11, exposed, and developed to cure a portion of the solder resist 14 corresponding in position to the solder resist pattern of the second artwork film 30.

[0018] After the second artwork film 30 is removed from the patterned copper clad laminate 11, a uncured portion of the solder resist 14 is removed from the patterned copper clad laminate 11 to construct the solder resist pattern on the patterned copper clad laminate 11 as shown in FIG. 1j.

[0019] In FIG. 1k, a wire bonding terminal, that is, an opening (c) of the solder resist pattern on the patterned copper clad laminate 11 is subjected to an electrolytic gold plating process to form the electrolytic gold-plated layer 15 on the patterned copper clad laminate 11.

[0020] Subsequently, an outer structure of the patterned copper clad laminate 11 is formed using a router or a power press to accomplish the PCB 10 as shown in FIG. 2.

[0021] Conventionally, regardless of the circuit pattern, incoming lines 16 for plating use had to be formed on the PCB 10 to form the electrolytic gold-plated layer 15 as shown in the dotted ellipse of FIG. 2.

[0022] With respect to this, the incoming lines 16 are mostly removed in the course of forming the outer structure of the copper clad laminate 11 using the router or power press, but a small portion of the incoming lines 16 remains on the PCB 10. Sometimes, a large portion of the incoming lines 16 may not be removed but remain on the PCB 10 according to a method of designing the PCB 10.
In accordance with the recent trend of a functional improvement and a miniaturization of electronic products, demand for highly fine and integrated circuit patterns of the PCB 10 are increasing. However, the incoming lines 16 remaining on the PCB 10 have no relation to the circuit pattern, thus limiting the degree of freedom in designing the PCB 10.

As well, the incoming lines 16 remaining on the PCB 10 act as a conductor in a relatively high frequency environment caused by an increased data communication speed. Accordingly, the incoming lines 16 act as a sort of antenna to bring about a parasitic inductance.

The parasitic inductance interferes with the electric signals of the circuit pattern to cause an impedance mismatching, which reduces the performances of the electronic products.

Furthermore, a signal to noise ratio of each electronic product is reduced due to the parasitic inductance, leading to the misoperation of the electronic product to reduce the reliability of the electronic product.

SUMMARY OF THE INVENTION

Therefore, the present invention has been made keeping in mind the above disadvantages occurring in the prior arts, and an object of the present invention is to provide an electrolytic gold plating method of a PCB without using a separate incoming line for plating use.

The above object can be accomplished by providing an electrolytic gold plating method of a printed circuit board, which includes (A) forming an electrolytic copper-plated layer, corresponding to a predetermined copper plating resist pattern, on a substrate, (B) forming an electrolytic gold-plated layer, corresponding to a predetermined gold plating resist pattern, on the substrate using an outer layer of the substrate as a first incoming line for electrolytic gold plating use, and (C) removing a portion of the outer layer of the substrate, on which the electrolytic copper-plated layer is not coated.

The electrolytic gold plating method may also include (D) forming a via hole through the substrate, and (E) forming an electrolytic copper-plated layer on the outer layer of the substrate and on a wall of the via hole, prior to the step of (A). At this time, the electrolytic copper-plated layer is used as the first incoming line in the step of (B).

Additionally, the step of (A) includes (A-1) coating a copper plating resist on the electrolytic copper-plated layer of the substrate, and exposing and developing the copper plating resist to form a predetermined copper plating resist pattern on the electrolytic copper-plated layer, (A-2) conducting an electrolytic copper plating process, using the outer layer and electrolytic copper-plated layer of the substrate as a second incoming line for electrolytic copper plating use, to form an electrolytic copper-plated layer, corresponding to the copper plating resist pattern, on the electrolytic copper-plated layer of the substrate, and (A-3) removing the copper plating resist.

The electrolytic gold plating method may also include (D) processing the outer layer of the substrate to be thin, prior to the step of (A).

In this regard, the copper plating resist includes a photosensitive material.

Further, the step of (B) includes (B-1) coating a gold plating resist on the electrolytic copper-plated layer of the substrate, and exposing and developing the gold plating resist to form a predetermined gold plating resist pattern on the electrolytic copper-plated layer, (B-2) conducting an electrolytic gold plating process, using the outer layer and electrolytic copper-plated layer of the substrate as the first incoming line, to form an electrolytic gold-plated layer, corresponding to the gold plating resist pattern, on the electrolytic copper-plated layer of the substrate, and (B-3) removing the gold plating resist.

The electrolytic gold plating method may also include (B-4) conducting an electrolytic nickel plating process, using the electrolytic copper-plated layer as a third incoming line for electrolytic nickel plating use, to form an electrolytic nickel-plated layer, corresponding to the gold plating resist pattern, on the electrolytic copper-plated layer of the substrate after the step of (B-1).

In this respect, the gold plating resist includes a photosensitive material.

Furthermore, the substrate is dipped in an etching solution capable of etching copper, but not gold, to remove a portion of the electrolytic copper-plated layer and the outer layer of the substrate, which is not coated with the electrolytic copper-plated layer, in the step of (C). At this time, the outer layer of the substrate is in contact with the electrolytic copper-plated layer.

As well, the step of (C) includes (C-1) coating an etching resist on the electrolytic copper-plated layer of the substrate, and exposing and developing the etching resist to form a predetermined etching resist pattern, which is not coated with the electrolytic copper-plated layer, on the electrolytic copper-plated layer of the substrate, (C-2) etching a portion of the electrolytic copper-plated layer and outer layer of the substrate, which is not coated with the etching resist pattern, and (C-3) removing the etching resist. At this time, the outer layer is in contact with the electrolytic copper-plated layer.

Furthermore, the etching resist includes a photosensitive material.

In addition, the substrate is dipped in an etching solution to remove a portion of the electrolytic copper-plated layer and the outer layer of the substrate, which is not coated with the electrolytic copper-plated layer, in the step of (C-2). At this time, the outer layer of the substrate is in contact with the electrolytic copper-plated layer.

Furthermore, a portion of the electrolytic copper-plated layer and the outer layer of the substrate, which is not coated with the electrolytic copper-plated layer, is etched through a plasma etching process in the step of (C-2). At this time, the outer layer of the substrate is in contact with the electrolytic copper-plated layer.

The electrolytic gold plating method may also include (D) coating a solder resist on a patterned substrate to form a predetermined solder resist pattern on the patterned substrate after the step of (C).

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and other advantages of the present invention will be more clearly
understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0043] FIGS. 1a to 1k are sectional views illustrating the production of a conventional PCB;

[0044] FIG. 2 is a plan view of the conventional PCB produced according to a procedure of FIGS. 1a to 1k;

[0045] FIGS. 3a to 3k are sectional views illustrating the production of a PCB according to the first embodiment of the present invention;

[0046] FIG. 4 is a plan view of the PCB produced according to a procedure of FIGS. 3a to 3k;

[0047] FIG. 5 is a plan view of a PCB according to the second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0048] Reference now should be made to the drawings, in which the same reference numerals are used throughout the different drawings to designate the same or similar components.

[0049] FIGS. 3a to 3k are sectional views illustrating the production of a PCB according to the first embodiment of the present invention, and FIG. 4 is a plan view of the PCB produced according to a procedure of FIGS. 3a to 3k. At this time, FIGS. 3a to 3k are sectional views taken along the line A-A’ of FIG. 4.

[0050] With reference to FIG. 3a, copper foil layers 112 are coated on both sides of an insulating resin layer 111 to fabricate a substrate 110, that is, a copper clad laminate. At this time, it is preferable that the copper foil layers 112 be thinly coated on the insulating resin layer 111 in consideration of the fact that the copper foil layers 112 are etched and removed in subsequent processes.

[0051] Examples of the copper clad laminate used as the substrate 110 may include a glass/epoxy copper clad laminate, a heat-resistant resin copper clad laminate, a paper/phenol copper clad laminate, a high frequency copper clad laminate, a flexible copper clad laminate, and a complex copper clad laminate. Preferably, the glass/epoxy copper clad laminate, in which the copper foil layers 112 are coated on both sides of the insulating resin layer 111, is used to fabricate a double-sided PCB or a multilayer PCB.

[0052] Referring to FIG. 3b, a via hole (B) is formed through the copper clad laminate to electrically connect an upper and lower copper foil layers 112 to each other.

[0053] In this regard, the via hole (B) is formed at a predetermined position of the copper clad laminate using a computer numerical control drill (CNC drill) or a laser beam.

[0054] The CNC drill is useful to form the via hole (B) through the double-sided PCB or to form a through hole through the multilayer PCB. After the via hole (B) or through hole is formed using the CNC drill, a deburring process is conducted to remove burrs of a copper foil generated in the course of drilling the copper clad laminate, and dust attached to a wall of the via hole (B) and to surfaces of the copper foil layers 112. At this time, the surfaces of the copper foil layers 112 become rough, thus improving an attachment force of copper to the copper foil layers 112 in a copper plating process.

[0055] The laser beam is useful to form a micro via hole through the multilayer PCB. For example, the copper foil layers 112 and the insulating resin layer 111 may be simultaneously holed by a yttrium aluminum garnet (YAG) laser beam, or the insulating resin layer 111 may be holed by a carbon dioxide laser beam after a portion of each copper foil layer 112 corresponding in position to the via hole is etched.

[0056] Meanwhile, a portion of the insulating resin layer 111 of the substrate 110 may be molten due to heat generated in the course of forming the via hole (B) to form a smear on the wall of the via hole (B). Accordingly, it is preferable that a desmear process be conducted after the via hole (B) is formed through the copper clad laminate so as to remove the smear on the wall of the via hole (B).

[0057] In FIG. 3c, an electroless copper plating process is conducted to form an electroless copper-plated layer 120 on the upper and lower copper foil layers 112 and wall of the via hole (B) of the substrate 110.

[0058] In this respect, the wall of the via hole (B) of the substrate 110 is comprised of the insulating resin layer 111, and thus, it is impossible to conduct an electrolytic copper plating process directly after the via hole (B) is formed through the copper clad laminate. Accordingly, the electroless copper plating process is conducted prior to conducting the electrolytic copper plating process to electrically connect the upper and lower copper foil layers 112 to each other through the via hole (B). In the electroless copper plating process, the insulating resin layer 111 is plated by copper without the actions of ions with electricity. In other words, the electroless copper plating process is achieved by the deposition of copper on the copper foil layers 112, and the deposition of copper is promoted by a catalyst. In detail, the catalyst is attached to the surface of each copper foil layer 112 so as to separate copper from a plating solution to deposit copper on the copper foil layer 112. Hence, the electroless copper plating process requires some pre-treating processes.

[0059] For example, the electroless copper plating process may include a degreasing step, a soft etching step, a pretreatment step, a catalyst treating step, a catalyst treating step, an accelerator step, an electroless copper plating step, and an anti-oxidizing step.

[0060] In the degreasing step, oxides, impurities, oils and fats are removed from the surfaces of the copper foil layers 112 using a solution containing acid or alkaline surfactants, and the resulting copper foil layers 112 are rinsed to remove the solution therefrom.

[0061] The soft etching step makes the surfaces of the copper foil layers 112 slightly rough (for example, a roughness of about 1-2 μm) to uniformly deposit copper particles on the copper foil layers 112 and to remove contaminants, which are not removed in the degreasing step, from the copper foil layers 112.

[0062] In the pre-catalyst treating step, the substrate 110 is dipped in a dilute first catalyst-containing chemical to prevent a second catalyst-containing chemical used in the catalyst treating step from being contaminated by the impu-
rities attached to the substrate 110 or to prevent a concentration of the second catalyst-containing chemical from being changed due to the contaminants attached to the substrate 110. Moreover, because the substrate 110 is preliminarily dipped in the first chemical, having the same components as the second chemical, prior to treat the substrate 110 using the second chemical, the treating of the substrate 110 using the catalyst is more preferably achieved. At this time, it is preferable that 1-5% chemical be used in the pre-catalyst treating step.

[0063] In the catalyst treating step, catalyst powder is coated on the copper foil layers 112 and insulating resin layer 111 (the wall of the via hole (B)) of the substrate 110. In this respect, the catalyst powder may be exemplified by Pd—Sn compound powder, and Pd₂⁺—Sn — dissociated from the Pd—Sn compound powder contributes to promoting the plating of the substrate 110 in conjunction with Cu₂⁺ plated on the substrate 110.

[0064] During the electroless copper plating step, it is preferable that the plating solution contain CuSO₄, HCHO, NaOH, and a stabilizer. At this time, it is important to control a composition of the plating solution because chemical reactions constituting the plating process of the substrate 110 must maintain an equilibrium state in order to desirably conduct the plating process. Accordingly, it is necessary to properly replenish each component constituting the plating solution, mechanically agitate the plating solution, and smoothly operate a cycling system of the plating solution so as to desirably maintain the composition of the plating solution. Furthermore, it is necessary to use a filtering device to remove by-products, and the removal of the byproducts using the filtering device contributes to extending a life of the plating solution.

[0065] An anti-oxidizing layer is coated on the substrate 110 to prevent copper from being oxidized due to alkaline components remaining on the copper clad laminate after the electroless copper plating step in the anti-oxidizing step.

[0066] However, the electroless copper-plated layer 120 has poorer physical properties than an electroplating copper-plated layer. Therefore, it is preferable to thinly form the electroless copper-plated layer 120 on the substrate 110.

[0067] Referring to FIG. 3d, a dry film 200 is coated on the electroless copper-plated layer 120, exposed and developed using an artwork film, having a predetermined pattern printed thereon, to be patterned. The pattern of the artwork film 200 may be exemplified by a circuit pattern, a land of the via hole (B), and a wire bonding terminal pattern.

[0068] The dry film 200 includes three films: a cover film, a photosensitive film, and a Mylar film. Of the three films, the photosensitive film substantially acts as a resist layer against ultraviolet light.

[0069] After the artwork film with the predetermined pattern is mounted on the dry film 200, the ultraviolet light is irradiated to the artwork film to expose and develop the dry film 200. At this time, the ultraviolet light is not transmitted through a black portion of the artwork film, which corresponds to the pattern, but through a remaining portion of the artwork film, on which the pattern is not printed, to cure the dry film 200 under the artwork film. The copper clad laminate on which the cured dry film 200 is mounted is dipped in a developing solution to remove an uncured portion of the dry film 200. In this regard, a remaining cured portion of the dry film 200 forms a resist pattern. With respect to this, examples of the developing solution include a sodium carbonate (Na₂CO₃) aqueous solution and a potassium carbonate (K₂CO₃) aqueous solution.

[0070] With reference to FIG. 3e, the substrate 110 on which the patterned dry film 200 is mounted is subjected to the electrolytic copper plating process to form the electrolytic copper-plated layer 130 on the electroless copper-plated layer 120 formed on the upper and lower copper foil layers 112 and wall of the via hole (B). In this regard, the patterned dry film 200 is used as a plating resist, and the upper and lower copper foil layers 112 of the substrate 110 are used as incoming lines for an electrolytic copper plating process.

[0071] At this time, the substrate 110 having the patterned dry film 200 mounted thereon is dipped in the plating solution in a vessel, and subjected to the electrolytic copper plating process using a DC rectifier (direct current rectifier). In this respect, a proper amount of electricity is applied by the DC rectifier to the substrate 110 based on a calculated area of the substrate 110, which is to be plated with copper, thereby depositing copper on the substrate 110 having the patterned dry film 200 mounted thereon.

[0072] The electrolytic copper-plated layer 130 has superior physical properties to the electroless copper-plated layer 120, and it is easy to form the relatively thick electrolytic copper-plated layer 130 on the electroless copper-plated layer 120.

[0073] After the completion of the electrolytic copper plating process, the dry film 200 is removed from the substrate 110 as shown in FIG. 3f.

[0074] In this respect, a delaminating solution, such as sodium hydroxide (NaOH) and potassium hydroxide (KOH), is used to remove the dry film 200 from the substrate 110.

[0075] In FIGS. 3d to 3f, the dry film 200 is used as the plating resist, but a photosensitive liquid may be alternatively used as the plating resist. In the case of using the photosensitive liquid as the plating resist, the photosensitive liquid, which is to be exposed to the ultraviolet light, is coated on the electroless copper plating layer 120 plated on the substrate 110, and then dried to form a photosensitive layer on the electroless copper-plated layer 120. Subsequently, the photosensitive layer is exposed and developed by the ultraviolet light using the patterned artwork film 300 to be patterned. In this respect, the patterned photosensitive layer acts as the plating resist. The substrate 110 having the patterned photosensitive layer mounted thereon is then dipped in the plating solution in the vessel, and subjected to the electrolytic copper plating process using the DC rectifier to form the electrolytic copper-plated layer 130 on the electroless copper-plated layer 120 plated on the upper and lower copper foil layers 112 and the wall of the via hole (B) of the substrate 110. After the completion of the electrolytic copper plating process, the photosensitive layer is removed from the substrate 110. Examples of a process of coating the photosensitive liquid on the substrate 110 include a dip coating process, a roll coating process, and an electrodeposition process.
Referring to FIG. 3g, after a gold plating resist 300 is coated on the electrolytic copper-plated layer 130, the gold plating resist 300 is exposed and developed using an artwork film, having an electrolytic gold plating pattern printed thereon, to be patterned.

The substrate 110 is then subjected to an electrolytic gold plating process using the patterned gold plating resist 300 to form an electrolytic gold-plated layer 150 on the electrolytic copper-plated layer 130 of the substrate 110 as shown in FIG. 3h. Like in the case of the electrolytic copper plating process in FIG. 3e, the electrolytic gold plating process is conducted using the copper foil layers 112 as the incoming lines, and thus, it is not necessary to form a separate incoming line in the electrolytic gold plating process.

Subsequently, the substrate 110 having the electrolytic gold-plated layer 150 mounted thereon is dipped in the plating solution in the vessel, and then subjected to the electrolytic gold plating process using the DC rectifier. At this time, a proper intensity of electricity is applied by the DC rectifier to the substrate 110 based on a calculated area of the substrate 110, which is to be plated with gold, thereby depositing gold on the electrolytic copper-plated layer 130 of the substrate 110.

Additionally, the electrolytic gold plating process may be conducted after nickel is thinly coated on the electrolytic copper-plated layer 130 so as to increase an attachment force of gold to the electrolytic copper-plated layer 130.

Subsequently, the gold plating resist 300 is removed from the substrate 110 as shown in FIG. 3i.

The gold plating resist 300 used in FIGS. 3g to 3i may be the dry film 200 or photosensitive liquid in FIGS. 3d to 3f.

With reference to FIG. 3j, a portion of the electroless copper-plated layer 120 and copper foil layers 112, which is not coated with the electrolytic copper-plated layer 130, is removed from the substrate 110 to pattern the copper clad laminate. At this time, the pattern of the copper clad laminate includes the circuit pattern, the land of the via hole (B), and the wire bonding terminal pattern.

With respect to this, the removal of the electroless copper-plated layer 120 and copper foil layers 112 from the substrate 110 may be conducted according to various processes.

In detail, according to one process, the substrate 110 is dipped in an etching solution capable of etching the electroless copper-plated layer 120 and copper foil layers 112 but not the electrolytic gold-plated layer 150. At this time, a portion of the electroless copper-plated layer 120 and copper foil layers 112 is easily removed from the substrate 110 because pre-treating processes are conducted so as to make the copper foil layers 112 thin in FIG. 3e and the electroless copper-plated layer 120 is thinly formed on the substrate 110. However, the circuit pattern, the land and wall of the via hole (B), or wire bonding terminal pattern include the thick electrolytic copper-plated layer 130 with excellent physical properties as well as the copper foil layers 112 and electroless copper-plated layer 120. Accordingly, the copper foil layers 112 and electroless and electrolytic copper-plated layers 120, 130 are insufficiently etched.

According to another process, an etching resist, such as the dry film 200, is coated on the electroless copper-plated layer 120 of the substrate 110, and is patterned so as to protect the circuit pattern, the land of the via hole (B), or the wire bonding terminal pattern. The resulting substrate 110 is then dipped in the etching solution to remove a useless portion of the electroless copper-plated layer 120 and copper foil layers 112.

According to the third process, the etching resist, such as the dry film 200, is coated on the electroless copper-plated layer 120 of the substrate 110, and is patterned so as to protect the circuit pattern, the land of the via hole (B), or the wire bonding terminal pattern. Subsequently, a useless portion of the electroless copper-plated layer 120 and copper foil layers 112 of the substrate 110 is removed according to a plasma etching process. In this respect, a side wall of the circuit pattern is precisely processed due to an anisotropic etching considered as an advantage of the plasma etching process.

Referring to FIG. 3k, a solder resist 140 is coated on the patterned substrate 110, and then patterned to form a solder resist pattern on the patterned substrate 110.

A detailed description will be given of the formation of the solder resist pattern, below. The solder resist 140 is coated on the patterned substrate 110 and then preliminarily dried. At this time, examples of a process of coating the solder resist 140 on the patterned substrate 110 include a screen printing process, a roller coating process, a curtain coating process, and a spray coating process.

Subsequently, an artwork film having the solder resist pattern printed thereon is mounted on the patterned substrate 110, exposed, and developed to cure a portion of the solder resist 140 corresponding in position to the solder resist pattern. The artwork film and an uncured portion of the solder resist 140 are sequentially removed to form the solder resist pattern on the patterned substrate 110. The primarily cured solder resist 140 is completely cured by the ultraviolet light and a drier, and a residue of the solder resist 140, which is to be removed, and impurities are removed by a plasma.

An exterior structure of the copper clad laminate is then constructed using the router or the power press to accomplish the PCB 100 as shown in FIG. 4.

With reference to FIG. 4, the PCB 100 according to the present invention has no incoming lines as shown in a dotted ellipse. The reason for this is that the electroless copper-plated layer 120 is used as the incoming line for the electrolytic gold plating process and removed from the substrate 110 after the completion of the electrolytic gold plating process.

As described above, FIGS. 3 and 4 illustrate the double-sided PCB, which is fabricated using the copper clad laminate as the substrate 110. However, a single-sided PCB or a multilayer PCB may be fabricated according to the electrolytic gold plating process without using the incoming line, if necessary.

In the case of fabricating the multilayer PCB, a pattern including a ground circuit and a signal process circuit is formed on an inner layer of the multilayer PCB. At
this time, a copper foil is attached to the inner layer using an insulator adhesive resin, such as prepreg, or resin coated copper (RCC) laminated on the inner layer to form an outer layer. The outer layer is then subjected to the electrolytic gold plating process as shown in FIGS. 3a to 3k to accomplish the multilayer PCB.

[0094] FIG. 5 is a plan view of a PCB according to the second embodiment of the present invention.

[0095] As shown in FIG. 5, the PCB 100 according to the present invention is advantageous in that the circuit pattern may be additionally formed instead of the incoming line on a portion of the PCB corresponding to a dotted ellipse of FIG. 5 because it is not necessary to form the incoming line in the course of designing the PCB. Therefore, the degree of freedom is increased in the course of designing the PCB, thereby highly integrating the circuit pattern on the PCB 100.

[0096] The present invention has been described in an illustrative manner, and it is to be understood that the terminology used is intended to be in the nature of description rather than of limitation. Many modifications and variations of the present invention are possible in light of the above teachings. Therefore, it is to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

[0097] As apparent from the above description, the present invention provides an electrolytic gold plating method of a PCB without using an incoming line for plating use.

[0098] Therefore, the electrolytic gold plating method according to the present invention is advantageous in that a circuit pattern is formed instead of the incoming line on a portion of the PCB, on which the incoming line was positioned conventionally, thereby improving the degree of freedom in the course of designing the PCB.

[0099] Another advantage of the electrolytic gold plating method according to the present invention is that a parasitic inductance caused by the incoming line does not occur because the PCB of the present invention has no incoming line.

[0100] Furthermore, the PCB according to the present invention has no incoming line, and thus, the parasitic inductance does not occur, a signal to noise ratio of an electronic product, fabricated using the PCB of the present invention, is improved in a relatively high frequency environment, an impedance matching is easily accomplished, a sudden misoperation of the electronic product is prevented, and electric performances and reliability of the PCB are improved.

What is claimed is:

1. An electrolytic gold plating method of a printed circuit board, comprising:

(A) forming an electrolytic copper-plated layer, corresponding to a predetermined copper plating resist pattern, on a substrate;

(B) forming an electrolytic gold-plated layer, corresponding to a predetermined gold plating resist pattern, on the substrate using an outer layer of the substrate as a first incoming line for electrolytic gold plating use; and

(C) removing a portion of the outer layer of the substrate, on which the electrolytic copper-plated layer is not coated.

2. The electrolytic gold plating method as set forth in claim 1, further comprising:

(D) forming a via hole through the substrate; and

(E) forming an electroless copper-plated layer on the outer layer of the substrate and on a wall of the via hole, prior to the step of (A), the electroless copper-plated layer being used as the first incoming line in the step of (B).

3. The electrolytic gold plating method as set forth in claim 2, wherein the step of (A) comprises:

(A-1) coating a copper plating resist on the electroless copper-plated layer of the substrate, and exposing and developing the copper plating resist to form a predetermined copper plating resist pattern on the electroless copper-plated layer;

(A-2) conducting an electrolytic copper plating process, using the outer layer and electroless copper-plated layer of the substrate as a second incoming line for electrolytic copper plating use, to form an electrolytic copper-plated layer, corresponding to the copper plating resist pattern, on the electroless copper-plated layer of the substrate; and

(A-3) removing the copper plating resist.

4. The electrolytic gold plating method as set forth in claim 2, further comprising:

(D) processing the outer layer of the substrate to be thin, prior to the step of (A).

5. The electrolytic gold plating method as set forth in claim 3, wherein the copper plating resist includes a photosensitive material.

6. The electrolytic gold plating method as set forth in claim 2, wherein the step of (B) comprises:

(B-1) coating a gold plating resist on the electroless copper-plated layer of the substrate, and exposing and developing the gold plating resist to form a predetermined gold plating resist pattern on the electroless copper-plated layer;

(B-2) conducting an electrolytic gold plating process, using the outer layer and electroless copper-plated layer of the substrate as the first incoming line, to form an electrolytic gold-plated layer, corresponding to the gold plating resist pattern, on the electroless copper-plated layer of the substrate; and

(B-3) removing the gold plating resist.

7. The electrolytic gold plating method as set forth in claim 6, further comprising (B-4) conducting an electrolytic nickel plating process, using the electroless copper-plated layer as a third incoming line for electrolytic nickel plating use, to form an electrolytic nickel-plated layer, corresponding to the gold plating resist pattern, on the electroless copper-plated layer of the substrate after the step of (B-1).

8. The electrolytic gold plating method as set forth in claim 6, wherein the gold plating resist includes a photosensitive material.

9. The electrolytic gold plating method as set forth in claim 2, wherein the substrate is dipped in an etching solution capable of etching copper, but not gold, to remove
a portion of the electroless copper-plated layer and the outer layer of the substrate, which is not coated with the electrolytic copper-plated layer, in the step of (C), the outer layer of the substrate being in contact with the electroless copper-plated layer.

10. The electrolytic gold plating method as set forth in claim 2, wherein the step of (C) comprises:

(C-1) coating an etching resist on the electroless copper-plated layer of the substrate, and exposing and developing the etching resist to form a predetermined etching resist pattern, which is not coated with the electrolytic copper-plated layer, on the electroless copper-plated layer of the substrate;

(C-2) etching a portion of the electroless copper-plated layer and outer layer of the substrate, which is not coated with the etching resist pattern, the outer layer being in contact with the electroless copper-plated layer; and

(C-3) removing the etching resist.

11. The electrolytic gold plating method as set forth in claim 10, wherein the etching resist includes a photosensitive material.

12. The electrolytic gold plating method as set forth in claim 10, wherein the substrate is dipped in an etching solution to remove a portion of the electroless copper-plated layer and the outer layer of the substrate, which is not coated with the electrolytic copper-plated layer, in the step of (C-2), the outer layer of the substrate being in contact with the electroless copper-plated layer.

13. The electrolytic gold plating method as set forth in claim 10, wherein a portion of the electroless copper-plated layer and the outer layer of the substrate, which is not coated with the electrolytic copper-plated layer, is etched through a plasma etching process in the step of (C-2), the outer layer of the substrate being in contact with the electroless copper-plated layer.

14. The electrolytic gold plating method as set forth in claim 2, further comprising (D) coating a solder resist on a patterned substrate to form a predetermined solder resist pattern on the patterned substrate after the step of (C).

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