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(54) **Title:** HIGH VOLTAGE WAKE SIGNALING INPUT/OUTPUT FOR 10BASE-T1S SYSTEM BASIS CHIP

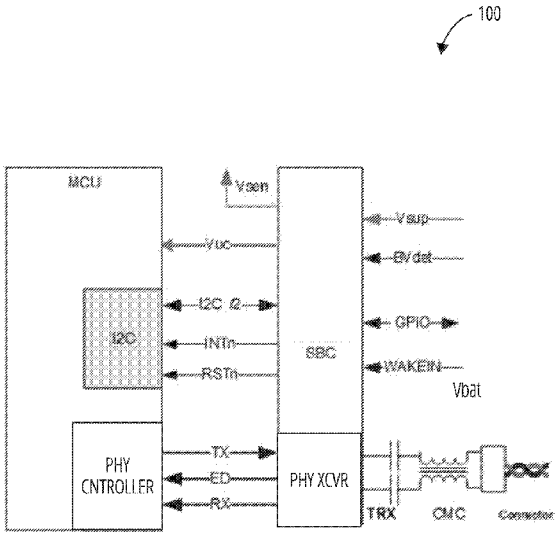

FIG. 1

(57) **Abstract:** A high voltage wake signaling input/output for 10BASE-T1S system basis chip. An apparatus includes a pad associated with wake signaling at a 10BASET 1S PHY, the wake signaling represented by voltage changes between first voltage levels; a system basis chip, comprising: a circuit to change a voltage received from the pad from first voltage levels to second, corresponding voltage levels, the second voltage levels lower than the first voltage levels; and a logic circuit to detect a valid voltage change at the pad responsive to the changed voltage.

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HIGH VOLTAGE WAKE SIGNALING INPUT/OUTPUT FOR 10BASE-T1S SYSTEM BASIS CHIP

FIELD

[0001] Examples relate, generally, to system-basis-chips and system basis chips that implement physical layer devices.

BACKGROUND

[0002] A system basis chip (SBC) is an integrated circuit (IC) that combines multiple functions required for the operation of electronic systems. ICs and SBCs are utilized in a variety of operational context.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] To easily identify the discussion of any particular element or act, the most significant digit or digits in a reference number refer to the figure number in which that element is first introduced.

[0004] FIG. 1 illustrates an aspect of the subject matter in accordance with one example.

[0005] FIG. 2 illustrates an aspect of the subject matter in accordance with one example.

[0006] FIG. 3 illustrates an aspect of the subject matter in accordance with one example.

[0007] FIG. 4 illustrates an aspect of the subject matter in accordance with one embodiment.

[0008] FIG. 5 illustrates an aspect of the subject matter in accordance with one embodiment.

[0009] FIG. 6 illustrates an aspect of the subject matter in accordance with one embodiment.

[0010] FIG. 7 is a block diagram of circuitry that, in some examples, may be used to implement various functions, operations, acts, processes, or methods disclosed herein.

DETAILED DESCRIPTION

[0011] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof, and in which are shown, by way of illustration, specific examples of examples in which the present disclosure may be practiced. These examples are described in sufficient detail to enable a person of ordinary skill in the art to practice the present disclosure. However, other examples may be utilized, and structural, material, and process changes may be made without departing from the scope of the disclosure.

[0012] The illustrations presented herein are not meant to be actual views of any particular method, system, device, or structure, but are merely idealized representations that are employed to describe the examples of the present disclosure. The drawings presented herein are not necessarily drawn to scale. Similar structures or components in the various drawings may retain the same or similar numbering for the convenience of the reader; however, the similarity in numbering does not mean that the structures or components are necessarily identical in size, composition, configuration, or any other property.

[0013] The following description may include examples to help enable one of ordinary skill in the art to practice the disclosed examples. The use of the terms "exemplary," "by example," and "for example," means that the related description is explanatory, and though the scope of the disclosure is intended to encompass the examples and legal equivalents, the use of such terms is not intended to limit the scope of an example or this disclosure to the specified components, steps, features, functions, or the like.

[0014] It will be readily understood that the components of the examples as generally described herein and illustrated in the drawing could be arranged and designed in a wide variety of different configurations. Thus, the following description of numerous examples is not intended to limit the scope of the present disclosure but is merely representative of numerous examples. While the various aspects of the examples may be presented in drawings, the drawings are not necessarily drawn to scale unless specifically indicated.

[0015] Furthermore, specific implementations shown and described are only examples and should not be construed as the only way to implement the present disclosure unless specified otherwise herein. Elements, circuits, and functions may be shown in block diagram form in order not to obscure the present disclosure in unnecessary detail. Conversely, specific implementations shown and described are exemplary only and should not be construed as the only way to implement the present disclosure unless specified otherwise herein. Additionally, block definitions and partitioning of logic between various blocks is exemplary of a specific implementation. It will be readily apparent to one of ordinary skill in the art that the present disclosure may be practiced by numerous other partitioning solutions. For the most part, details concerning timing considerations and the like have been omitted where such details are not necessary to obtain a complete understanding of the present disclosure and are within the abilities of persons of ordinary skill in the relevant art.

[0016] Those of ordinary skill in the art would understand that information and signals may be represented using any of a variety of different technologies and techniques. Some drawings may illustrate signals as a single signal for clarity of presentation and description. It will be understood by a person of ordinary skill in the art that the signal may represent a bus of signals, wherein the bus may have a variety of bit widths and the present disclosure may be implemented on any number of data signals including a single data signal.

[0017] The various illustrative logical blocks, modules, and circuits described in connection with the examples disclosed herein may be implemented or performed with a general purpose processor, a special purpose processor, a Digital Signal Processor (DSP), an Integrated Circuit (IC), an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor (may also be referred to herein as a host processor or simply a host) may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, such as a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. A general-purpose computer including a processor is considered a special-purpose computer while the general-purpose computer executes computing instructions (e.g., software code) related to examples of the present disclosure.

[0018] The examples may be described in terms of a process that is depicted as a flowchart, a flow diagram, a structure diagram, or a block diagram. Although a flowchart may describe operational acts as a sequential process, many of these acts can be performed in another sequence, in parallel, or substantially concurrently. In addition, the order of the acts may be re-arranged. A process may correspond to a method, a thread, a function, a procedure, a subroutine, a subprogram, without limitation. Furthermore, the methods disclosed herein may be implemented in hardware, software, or both. If implemented in software, the functions may be stored or transmitted as one or more instructions or code on computer-readable media. Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another.

[0019] Any reference to an element herein using a designation such as "first," "second," and so forth does not limit the quantity or order of those elements, unless such limitation is explicitly stated. Rather, these designations may be used herein as a convenient method of distinguishing between two or more elements or instances of an element. Thus, a reference to first and second elements does not mean that only two elements may be employed there or that the first element must precede the second element in some manner. In addition, unless stated otherwise, a set of elements may comprise one or more elements.

[0020] As used herein, the term "substantially" in reference to a given parameter, property, or condition means and includes to a degree that one of ordinary skill in the art would understand that the given parameter, property, or condition is met with a small degree of variance, such as, for example, within acceptable manufacturing tolerances. By way of example, depending on the particular parameter, property, or condition that is substantially met, the parameter, property, or condition may be at least 90% met, at least 95% met, or even at least 99% met.

[0021] As used herein, any relational term, such as "over," "under," "on," "underlying," "upper," "lower," without limitation, is used for clarity and convenience in understanding the disclosure and accompanying drawings and does not connote or depend on any specific preference, orientation, or order, except where the context clearly indicates otherwise.

[0022] In this description the term "coupled" and derivatives thereof may be used to indicate that two elements co-operate or interact with each other. When an element is described as being "coupled" to another element, then the elements may be in direct physical or electrical contact or there may be intervening elements or layers present. In contrast, when an element is described as being "directly coupled" to another element, then there are no intervening elements or layers present. The term "connected" may be used in this description interchangeably with the term "coupled," and has the same meaning unless expressly indicated otherwise or the context would indicate otherwise to a person having ordinary skill in the art.

[0023] As used herein, the terms "assert," "de-assert" and derivatives thereof used in reference to a pin, means, respectively, to assert or de-assert a signal associated with the pin (e.g., a signal specifically assigned to the pin or a signal to which the pin is specifically assigned, without limitation).

[0024] A system basis chip (SBC) is an integrated circuit (IC) that combines multiple functions for operation of an electronic system. An SBC typically integrates various, different functions into a single chip, including, as non-limiting examples: power management functions

such as voltage regulators, power switches, or protection circuitry, without limitation, to manage the power supply for the system; communication interfaces such as CAN (Controller Area Network), LIN (Local Interconnect Network), SPI (Serial Peripheral Interface), or I2C (Inter-Integrated Circuit), without limitation; embedded systems such as state machines or microprocessors, without limitation, that control and coordinate tasks; analog functions such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), temperature sensors, and other signal conditioning circuitry; and diagnostic and safety functions, such as monitoring and reporting voltage levels, temperature, or fault conditions, without limitation.

[0025] SBCs are found in a variety of operational context, including automotive and industrial applications. A non-limiting example of an automotive application for SBC is in 10SPE (i.e., 10 Mbps Single Pair Ethernet) networks (also called "10BASE-T1S networks"). 10SPE is a network technology specified in IEEE 802.3 clause 147 and 148. 10SPE may be used to provide a collision free, deterministic transmission on a multi-drop network.

[0026] In some cases, a transceiver (xcvr) and controller of a 10SPE physical layer device (PHY) may be located on different die, as a non-limiting example, so the die undergo different processing conditions. Such an architecture may be referred to herein as a "split-PHY" architecture. The digital blocks of a PHY controller, which are susceptible to damage during high voltage temperature processes may be located on a first die that does not undergo high voltage temperature processes. Analog and digital blocks of a PHY transceiver, which are not susceptible to damage during high voltage temperature processes or require such high voltage temperature processes may be located on a second die that does undergo such high voltage temperature processes.

[0027] The 10SPE Transceiver Interface standard currently under specification development by Technology Committee 14 of the Open Alliance (hereinafter the "TC14") defines a 3-pin hardware interface for communication between a PHY transceiver and PHY controller.

[0028] The 10SPE controller functions are implemented at a microcontroller (MCU) and the 10SPE transceiver functions are implemented at an SBC. In addition to 10SPE transceiver functions, the SBC can implement non-transceiver functions, i.e., functions of the electronic system, such as power management, watchdog circuit, monitors, general purpose input/output (GPIO), without limitation.

[0029] In 10SPE, the SBC's responsibilities include communication transceiver, low-voltage power, observability/control of high voltage domain and functional safety mechanisms for MCU to reach safe state.

[0030] TC14 describes low-power (sleep-wake) behavior of the PHY transceiver for partial networking. Partial networking refers to a feature that enables selective power management and communication capabilities within a network. Partial networking allows certain network nodes or devices to enter a low-power state or sleep state while still maintaining basic communication functionality. In Ethernet networks, partial networking is utilized to optimize power consumption, particularly in automotive or industrial applications. Allowing selected devices to enter a low-power state or sleep state may reduce overall power consumption, extend battery life, or improves energy efficiency, without limitation.

[0031] When an SBC implements a 10SPE PHY transceiver, the SBC may include other functions such as power delivery and watchdog for the MCU and sensors. Hence sleep-wake of the SBC considers sleep-wake of the PHY transceiver as well as sleep-wake of the MCU. However, the drivers (e.g., firmware, configurable state machines, logic circuits, without limitation) that implement a PHY transceiver are typically separate and asynchronous with the driver for the other SBC functions.

[0032] One or more examples relate, generally, to an SBC that executes a power management command only upon the same power management command having been received via the hardware interface (e.g., TC14 compliant three-pin hardware interface, without limitation) and the I2C bus. This ensures that the PHY transceiver and SBC change power state concurrently with the PHY controller and MCU (i.e., the PHY transceiver/SBC and PHY controller/MCU change respective power states concurrently).

[0033] As a non-limiting example, if the power management command is a sleep command then power is not turned OFF at the SBC unless both PHY transceiver and PHY controller are in (or will be in) sleep state.

[0034] As a non-limiting example, an SBC manages provision of power to an MCU and a PHY controller implemented by the MCU and so the SBC is aware of the power state of the PHY controller and MCU via the information and commands it receives from the MCU via the I2C bus. The SBC is aware of the power state of the PHY transceiver because the SBC implements the hardware interface and the PHY transceiver and is aware of power management commands provided via the hardware interface.

[0035] Wake is handled exclusively by the PHY transceiver but wake source status is made available to respective drivers for the PHY transceiver and SBC functions.

[0036] MCUs operate at increasingly lower voltages e.g., 3.3 V. Hence they cannot connect directly to high voltage signals. In antiautomobile the high voltage is nominally battery voltage (e.g., 12V) but can be much higher or lower under stress (e.g.LV124). In other applications e.g., fire alarm systems the nominal voltage may be 24V.

[0037] One or more examples relate, generally, to a system basis chip capable of handling battery voltage signals. Hence changes in a high voltage input can be sensed and qualified by the SBC and MCU informed via interrupt. In the other direction MCU write to register signaled by the SBC as high voltage or GND. The GPIO controls can be implemented in VDDU (always on) domain to enable wake.

- **•10Base-T1S xcvr SBC**
  - •Xcvr and regulated power delivery are the 2 primary functions (uses car battery as power source)
  - •SBC =system basis chip; also refers to non-xcvr functions of chip (e.g., power delivery, watchdog, monitors, GPIO for MCU); GPIO=general purpose I/O pin; I/O=input output
- **•HV GPIO inputs**
  - •OA specifies split-PHY (PMA + PMD-xcvr) with low voltage 3-pin interface (TX,ED,RX) to MCU
    - •cmd=pulse width pattern on TX to make xcvr enter low power
  - •OA=open Alliance, PHY=physical layer, PMA=physical media attachment sub-layer, PMD=physical medium dependent sub-layer, HV=high voltage; VDDU=VDD uninterrupted (power domain) aka always-on domain
  - •Level shifting of high voltage system signals to MCU-compatible levels
  - •Level changes signaled via interrupt
  - •Can be located in VDDU domain e.g., WAKEIN, WAKEIO
- **•HV GPIO outputs**
  - •MCU writes to register signalized to high voltage levels by open-drain driver
  - •Can be located in VDDU domain e.g., WAKEOUT, WAKEIO

[0038] FIG. 1 is a block diagram of a system 100 that implements, among other things, a 10SPE PHY, in accordance with one or more examples. System 100 includes a microcontroller

(MCU) and a system basis chip (SBC). A 10SPE PHY includes a PHY controller implemented by the MCU and a PHY transceiver implemented by the SBC. The PHY controller and PHY transceiver communicate via a three-pin hardware interface that includes pins associated with transmission signaling (TX), energy detection signaling (ED), and reception signaling (RX). The SBC and MCU communicate via an I2C bus and command, control and management pins (represented by INTn, and RSTn, which indicate action needed from the MCU, but which are not intended to limit this disclosure in any way).

[0039] The SBC implements functions of the PHY transceiver, functions of the MCU, functions of sensors, and its own internal functions (SBC functions). Vuc is a supply voltage provided to the MCU from the SBC. Vsen is supply voltage provided to one or more sensors. Vsup is the supply voltage provided to the SBC, may be utilized to provide Vuc and Vsen, e.g., directly or as a regulated version of Vsup. GPIO is a general-purpose input/output. WAKEIN is an input exclusively utilized to receive power management signals (e.g., wake or sleep, without limitation) from an external source. The voltage range of WAKEIN is Vbat to ground. Vbat is a battery voltage, such as an automobile battery. Transmit/receive connections, common mode choke, and connector are physical circuits that connect the SBC to a physical transmission medium such as a twisted pair.

[0040] FIG. 2 a schematic diagram of a pinout for a system basis chip such as the system basis chip depicted by FIG. 1.

[0041] FIG. 3 a circuit diagram of an input/output circuit that can connect a system basis chip's WAKEIN and WAKEOUT pins to a pad. The pad is at Vbat, the internal pins of the SBC utilize Vsup (here, 3.3V).

[0042] A high voltage input stage includes a comparator exhibiting hysteresis (here, a Schmitt trigger). An output of the comparator is coupled - in series or in parallel, as described below - to an internal wake signaling dind, of the SBC. The output of the comparator is switchably coupled to ground by a transistor switch. When the switch is ON the output of the comparator is coupled in parallel to dind, when the switch is OFF the output of the comparator is coupled in series with dind. The switch's gate and the comparator's reference input are coupled to receive the signal en-ind. The input of the comparator is coupled, in parallel to an input node, that is coupled to ground via a capacitor. The input node is switchably coupled to a large resistor, in this example, a 500K ohm resistor by a transistor switch (also called a “switching device”). A gate of the switch is coupled to Vsup (here, 3.3v). In this example it's an n-channel

transistor. The n-ch transistor is coupled in series with the high ohm resistor. The other end of the resistor is coupled to a node that is coupled in parallel to multiple series coupled zener diodes and a pad.

[0043] Not depicted as a signal detector that is used to set an internal bit (e.g., a flag) when a valid voltage change at dind is detected. The valid voltage change is used to infer a valid voltage change at the pad, where a valid voltage change is one that indicates a wakein signal. When VBAT at the pad, that causes 3.3V to be seen at the input of the comparator. When ground at the pad, that causes ground to be seen at the input of the comparator.

[0044] The circuit above the high voltage input stage is the output stage. When doutd and endb are both a 1, the switch does not allow current to flow and so the pad is at VBAT. When doutd and endb are a 0 (ground) the switch allows current to flow and so the pad is at ground.

[0045] FIG. 4 is a schematic diagram of a circuit used to drive a GPIO pin that is in the VBAT domain. CSR is a command status register. EXT Flag, Flags 1, Flags 2, and Flag select are bits of the CSR. A mux selection between Flag 1 and Flag 2 responsive to flag select. The output of the MUX is coupled to GPIO by an inverter. EXT flag is a bit that can be set by the GPIO (e.g., an external wake signal).

[0046] FIG. 5 is a schematic diagram depicting a circuit (the circuit of figure 3) to generate an input signal or output signal.

[0047] The circuit on the left receives a voltage signal having a voltage range of Vbat to ground and converts that voltage signal to a signal at an interval voltage level, and the converted signal is fed to a signal detector that determines whether or not a valid signal was present at the pad based on the internal signal. EXT_Flag of the CSR is set based on the output of the signal detector.

[0048] FIG. 6 is a state diagram depicting behavior of an SBC. The vertices represent states, namely SBC_sleep, SBC_reset, LPwake, LP, SBC_operative, normal, config, transmitting directed edges represent state changes from one state to another state.

[0049] It will be appreciated by those of ordinary skill in the art that functional elements of examples disclosed herein (e.g., functions, operations, acts, processes, or methods) may be implemented in any suitable hardware, software, firmware, or combinations thereof. FIG. 7 illustrates non-limiting examples of implementations of functional elements disclosed herein. In some examples, some or all portions of the functional elements disclosed herein may be performed by hardware capable of carrying out the functional elements.

[0050] FIG. 7 is a block diagram of a circuitry 700 that, in some examples, may be used to implement various functions, operations, acts, processes, or methods disclosed herein. The circuitry 700 includes one or more processors 702 (sometimes referred to herein as "processors 702") operably coupled to one or more data storage devices 704 (sometimes referred to herein as "storage 704"). The storage 704 includes machine executable code 706 stored thereon and the processors 702 include logic circuit 708. The machine executable code 706 information describes functional elements that may be implemented by (e.g., performed by) the logic circuit 708. The logic circuit 708 is adapted to implement (e.g., perform) the functional elements described by the machine executable code 706. The circuitry 700, when executing the functional elements described by the machine executable code 706, should be considered as special purpose hardware for carrying out functional elements disclosed herein. In some examples the processors 702 may perform the functional elements described by the machine executable code 706 sequentially, concurrently (e.g., on one or more different hardware platforms), or in one or more parallel process streams.

[0051] When implemented by logic circuit 708 of the processors 702, the machine executable code 706 adapts the processors 702 to perform operations of examples disclosed herein. By way of non-limiting example, the machine executable code 706 may adapt the processors 702 to perform some or a totality of operations of one or more process discussed herein.

[0052] Also, by way of non-limiting example, the machine executable code 706 may adapt the processors 702 to perform some or a totality of features, functions, or operations disclosed herein for one or more of FIGS. 1, 2, 3, 4, 5, or 6. More specifically, features, functions, or operations disclosed herein for coordinate power state changes.

[0053] The processors 702 may include a general purpose processor, a special purpose processor, a central processing unit (CPU), a microcontroller, a programmable logic controller (PLC), a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field-programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, other programmable device, or any combination thereof designed to perform the functions disclosed herein. A general-purpose computer including a processor is considered a special-purpose computer while the general-purpose computer executes functional elements corresponding to the machine executable code 706 (e.g., software code, firmware code, hardware descriptions) related to examples of the present disclosure. It is noted that a general-purpose processor (may also be referred to herein as a host

processor or simply a host) may be a microprocessor, but in the alternative, the processors 502 may include any conventional processor, controller, microcontroller, or state machine. The processors 702 may also be implemented as a combination of computing devices, such as a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0054] In some examples the storage 704 includes volatile data storage (e.g., random-access memory (RAM)), non-volatile data storage (e.g., Flash memory, a hard disc drive, a solid-state drive, erasable programmable read-only memory (EPROM), without limitation). In some examples the processors 702 and the storage 704 may be implemented into a single device (e.g., a semiconductor device product, a system on chip (SOC), without limitation). In some examples the processors 702 and the storage 704 may be implemented into separate devices.

[0055] In some examples the machine executable code 706 may include computer-readable instructions (e.g., software code, firmware code). By way of non-limiting example, the computer-readable instructions may be stored by the storage 704, accessed directly by the processors 702, and executed by the processors 702 using at least the logic circuit 708. Also, by way of non-limiting example, the computer-readable instructions may be stored on the storage 704, transferred to a memory device (not shown) for execution, and executed by the processors 502 using at least the logic circuit 708. Accordingly, in some examples the logic circuit 508 includes electrically configurable logic circuit 708.

[0056] In some examples the machine executable code 706 may describe hardware (e.g., circuitry) to be implemented in the logic circuit 708 to perform the functional elements. This hardware may be described at any of a variety of levels of abstraction, from low-level transistor layouts to high-level description languages. At a high-level of abstraction, a hardware description language (HDL) such as an IEEE Standard hardware description language (HDL) may be used. By way of non-limiting examples, Verilog, SystemVerilog or very large-scale integration (VLSI) hardware description language (VHDL) may be used.

[0057] HDL descriptions may be converted into descriptions at any of numerous other levels of abstraction as desired. As a non-limiting example, a high-level description can be converted to a logic-level description such as a register-transfer language (RTL), a gate-level (GL) description, a layout-level description, or a mask-level description. As a non-limiting example, micro-operations to be performed by hardware logic circuits (e.g., gates, flip-flops, registers, without limitation) of the logic circuit 708 may be described in a RTL and then converted by a

synthesis tool into a GL description, and the GL description may be converted by a placement and routing tool into a layout-level description that corresponds to a physical layout of an integrated circuit of a programmable logic device, discrete gate or transistor logic, discrete hardware components, or combinations thereof. Accordingly, in some examples the machine executable code 706 may include an HDL, an RTL, a GL description, a mask level description, other hardware description, or any combination thereof.

[0058] In examples where the machine executable code 706 includes a hardware description (at any level of abstraction), a system (not shown, but including the storage 704) implements the hardware description described by the machine executable code 706. By way of non-limiting example, the processors 702 may include a programmable logic device (e.g., an FPGA or a PLC) and the logic circuit 708 may be electrically controlled to implement circuitry corresponding to the hardware description into the logic circuit 708. Also, by way of non-limiting example, the logic circuit 708 may include hard-wired logic manufactured by a manufacturing system (not shown but including the storage 704) according to the hardware description of the machine executable code 706.

[0059] Regardless of whether the machine executable code 706 includes computer-readable instructions or a hardware description, the logic circuit 708 is adapted to perform the functional elements described by the machine executable code 706 when implementing the functional elements of the machine executable code 706. It is noted that although a hardware description may not directly describe functional elements, a hardware description indirectly describes functional elements that the hardware elements described by the hardware description are capable of performing.

[0060] As used in the present disclosure, the terms "module" or "component" may refer to specific hardware implementations to perform the actions of the module or component and/or software objects or software routines that may be stored on and/or executed by general purpose hardware (e.g., computer-readable media, processing devices, without limitation) of the computing system. In some examples, the different components, modules, engines, and services described in the present disclosure may be implemented as objects or processes that execute on the computing system (e.g., as separate threads). While some of the system and methods described in the present disclosure are generally described as being implemented in software (stored on and/or executed by general purpose hardware), specific hardware implementations or

a combination of software and specific hardware implementations are also possible and contemplated.

[0061] As used in the present disclosure, the term "combination" with reference to a plurality of elements may include a combination of all the elements or any of various different subcombinations of some of the elements. For example, the phrase "A, B, C, D, or combinations thereof" may refer to any one of A, B, C, or D; the combination of each of A, B, C, and D; and any subcombination of A, B, C, or D such as A, B, and C; A, B, and D; A, C, and D; B, C, and D; A and B; A and C; A and D; B and C; B and D; or C and D.

[0062] Terms used in the present disclosure and especially in the appended claims (e.g., bodies of the appended claims, without limitation) are generally intended as "open" terms (e.g., the term "including" should be interpreted as "including, but not limited to," the term "having" should be interpreted as "having at least," the term "includes" should be interpreted as "includes, but is not limited to," without limitation). As used herein, the term "each" means "some or a totality." As used herein, the term "each and every" means a "totality."

[0063] Additionally, if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases "at least one" and "one or more" to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim recitation to examples containing only one such recitation, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an" (e.g., "a" and/or "an" should be interpreted to mean "at least one" or "one or more," without limitation); the same holds true for the use of definite articles used to introduce claim recitations.

[0064] In addition, even if a specific number of an introduced claim recitation is explicitly recited, those skilled in the art will recognize that such recitation should be interpreted to mean at least the recited number (e.g., the bare recitation of "two recitations," without other modifiers, means at least two recitations, or two or more recitations, without limitation). Furthermore, in those instances where a convention analogous to "at least one of A, B, and C, without limitation" or "one or more of A, B, and C, without limitation" is used, in general such

a construction is intended to include A alone, B alone, C alone, A and B together, A and C together, B and C together, or A, B, and C together, without limitation.

[0065] Further, any disjunctive word or phrase presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase "A or B" should be understood to include the possibilities of "A" or "B" or "A and B."

[0066] Additional non-limiting examples include:

[0067] While the present disclosure has been described herein with respect to certain illustrated examples, those of ordinary skill in the art will recognize and appreciate that the present invention is not so limited. Rather, many additions, deletions, and modifications to the illustrated and described examples may be made without departing from the scope of the invention as hereinafter claimed along with their legal equivalents. In addition, features from one example may be combined with features of another example while still being encompassed within the scope of the invention as contemplated by the inventor.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

a pad associated with wake signaling at a 10BASET1S PHY, the wake signaling represented by voltage changes between first voltage levels;

a system basis chip, comprising:

a circuit to change a voltage received from the pad from first voltage levels to second, corresponding voltage levels, the second voltage levels lower than the first voltage levels; and

a logic circuit to detect a valid voltage change at the pad responsive to the changed voltage.

2. The apparatus of claim 1, wherein a voltage range of the first voltage levels is defined between a ground voltage and a battery voltage.

3. The apparatus of claim 1, wherein a voltage range of the second voltage levels is defined between a ground voltage and a further voltage lower than the battery voltage.

4. The apparatus of claim 3, comprising:

an input path from the pad to the circuit supplied by the battery voltage and the ground voltage,

wherein the circuit is supplied by the further voltage and the ground voltage.

5. The apparatus of claim 4, wherein the input path includes a big series resistor.

6. The apparatus of claim 1, wherein the system basis chip implements a 10BASET1S PHY transceiver.

7. An apparatus, comprising:

a pad associated with external wake signaling at a 10BASET1S PHY, a voltage range of the external wake signaling defined between a ground voltage and a battery voltage;

a circuit to generate internal wake signaling representative of external wake signaling, a voltage range of the internal wake signaling defined between a ground voltage and a further voltage lower than the battery voltage; and

a logic circuit to determine occurrence of a valid voltage change at the I/O pad utilizing the internal wake signaling.

8. The apparatus of claim 7, wherein the supply voltage is the battery voltage.

9. The apparatus of claim 7, comprising a system basis chip, wherein the system basis chip includes the circuit and the logic circuit.

10. The apparatus of claim 7, comprising: a regulated voltage source.

11. The apparatus of claim 7, comprising: a physical layer transceiver function.

12. The apparatus of claim 7, wherein the regulated voltage source is a low drop-out regulator, and the LDO provides the supply voltage for the PHY transceiver function.

13. An apparatus, comprising:

a pad associated with external wake_out signaling at a 10BASET1S PHY; and

a circuit to generate the external wake_out signaling at the PAD representative of internal wake_out signaling.

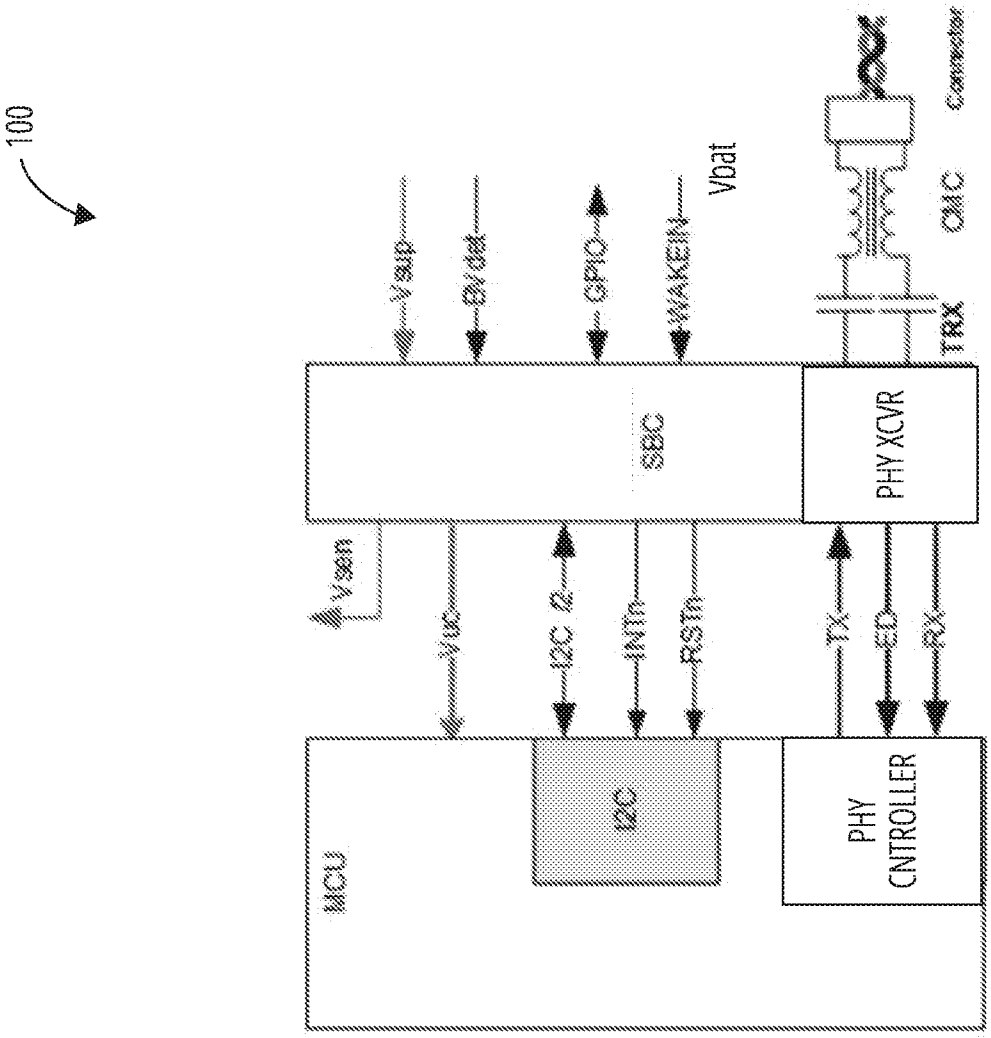
100
Vsup
EN det
GPIO
WAKEIN
Vbat
CAN
TRX
Connector
SBC
PHY XCVR
Vsen
Vuc
I2C
INTn
RSTn
TX
ED
RX
MCU
I2C
PHY CNTROLLER

FIG. 1

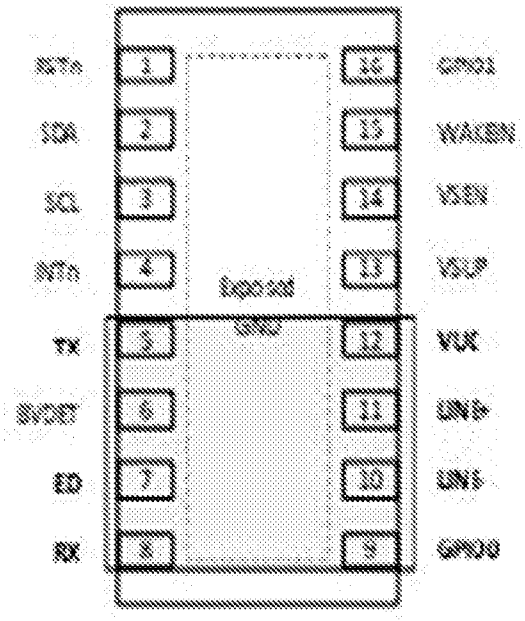

FIG. 2

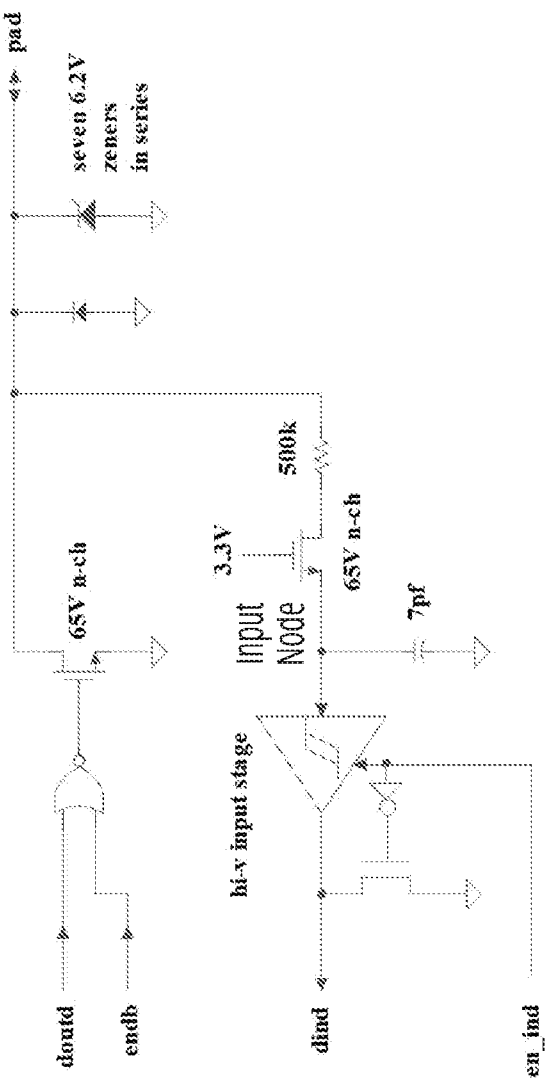
pad
seven 6.2V
zeners
in series
500k
3.3V
65V n-ch
65V n-ch
7pf
input
Node
hi-v input stage
doutd
endb
dind
en_ind

FIG. 3

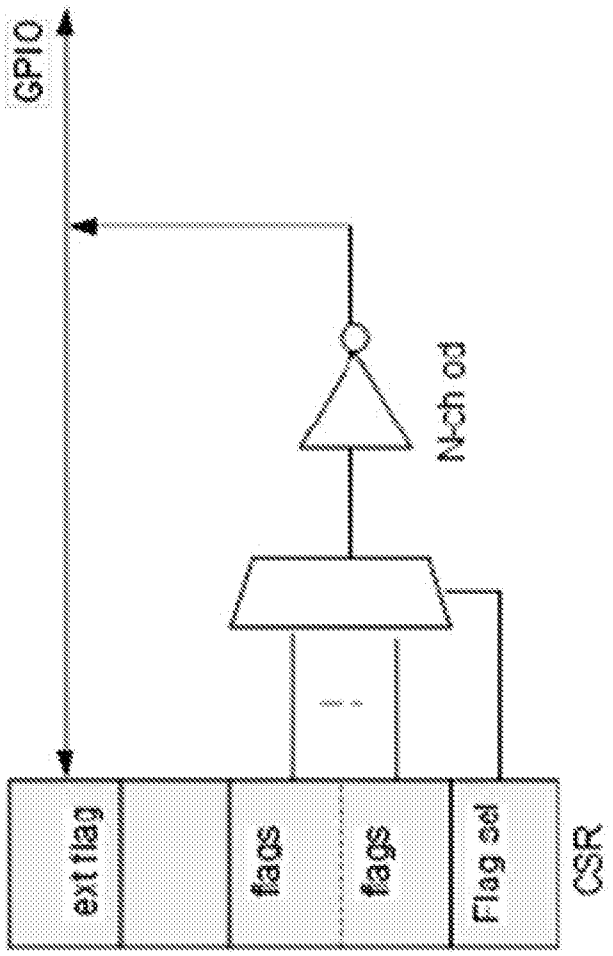

FIG. 4

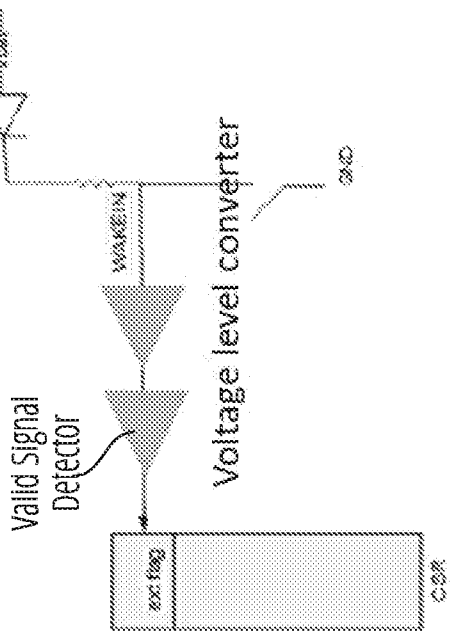

FIG. 5

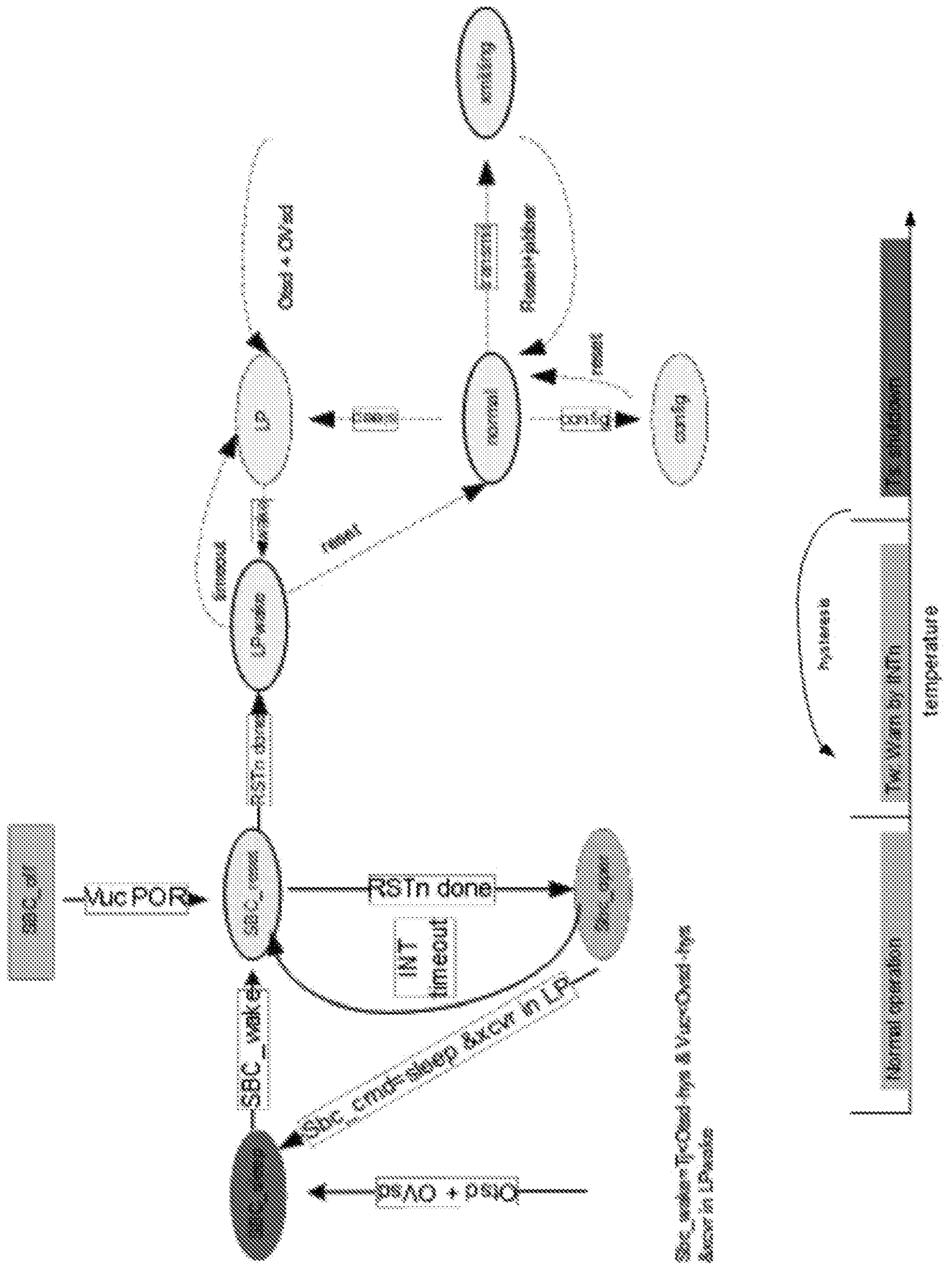
Vuc POR
RSTn done
RSTn done
INT
timeout
config
config
reset
temperature
Otsd + OVsd

FIG. 6

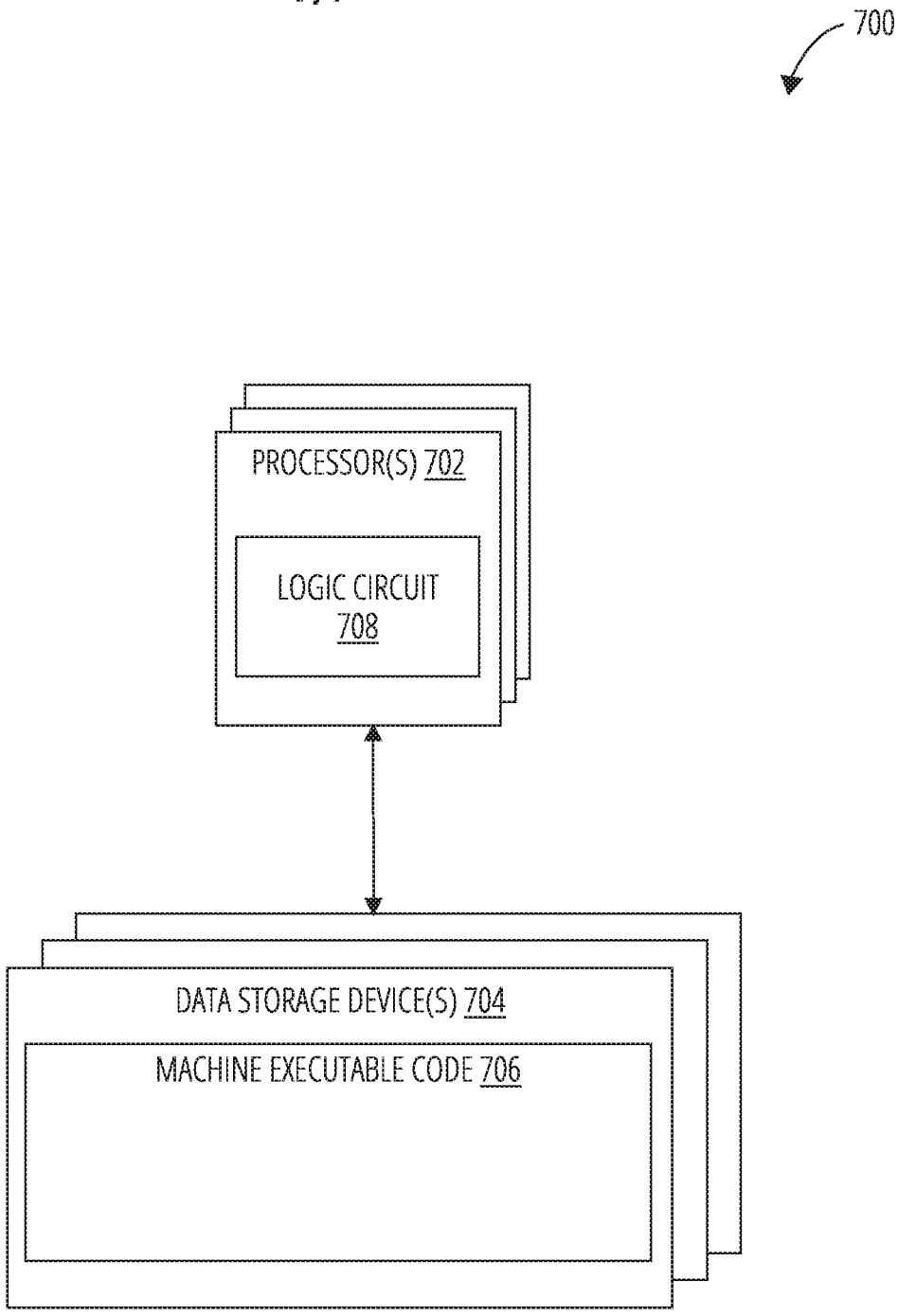
700
PROCESSOR(S) 702
LOGIC CIRCUIT 708
DATA STORAGE DEVICE(S) 704
MACHINE EXECUTABLE CODE 706

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2023/107647

A. CLASSIFICATION OF SUBJECT MATTER

H04B1/40(2015.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H04B, G06F, B60L, B60R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNTXT,ENTXTC,DWPI,IEEE,CNKI:10BASET1,10BASE+,10SPE,pad,PHY, wake, voltage, change, SBC, system basis chip, low+,internal,external,signaling

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2021303050 A1 (MICROCHIP TECHNOLOGY INCORPORATED) 30 September 2021 (2021-09-30) description, paragraphs [0040]-[0077], [0123]-[0132], [0139]-[0147]	1-13
A	CN 114859792 A (NEUSOFT REACH AUTOMOTIVE TECHNOLOGY (SHENYANG) CO., LTD.) 05 August 2022 (2022-08-05) the whole document	1-13
A	CN 115071599 A (WELTMEISTER INTELLIGENT TRAVEL TECHNOLOGY (SHANGHAI) CO., LTD.) 20 September 2022 (2022-09-20) the whole document	1-13
A	WO 2021233219 A1 (BYD CO., LTD.) 25 November 2021 (2021-11-25) the whole document	1-13
A	CN 108227576 A (BEIJING JINGWEI HIRAIN TECHNOLOGY CO., LTD.) 29 June 2018 (2018-06-29) the whole document	1-13

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 March 2024	**20 March 2024**

Name and mailing address of the ISA/CN	Authorized officer
CHINA NATIONAL INTELLECTUAL PROPERTY ADMINISTRATION **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China**	**LI,XiaoLi** Telephone No. **(+86) 010-53961772**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2023/107647

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 211519274 U (HAIMA NEW ENERGY AUTOMOBILE CO., LTD. et al.) 18 September 2020 (2020-09-18) the whole document	1-13

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2023/107647

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2021303050 A1	30 September 2021	US 2023091738 A1	23 March 2023
		WO 2021195663 A1	30 September 2021
		DE 112021001780 T5	05 January 2023
		JP 2023518827 A	08 May 2023
		KR 20220156588 A	25 November 2022
CN 114859792 A	05 August 2022	None	
CN 115071599 A	20 September 2022	None	
WO 2021233219 A1	25 November 2021	CN 113696780 A	26 November 2021
CN 108227576 A	29 June 2018	None	
CN 211519274 U	18 September 2020	None	