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A modified cascode amplifier ✓

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(72) Inventor(s)
Donald Jon Sauer
Todd J Christopher

(73) Proprietor(s)
RCA Licensing Corporation
(Incorporated in USA –
New Jersey)

2 Independence Way
Princeton
New Jersey 08540
United States of America

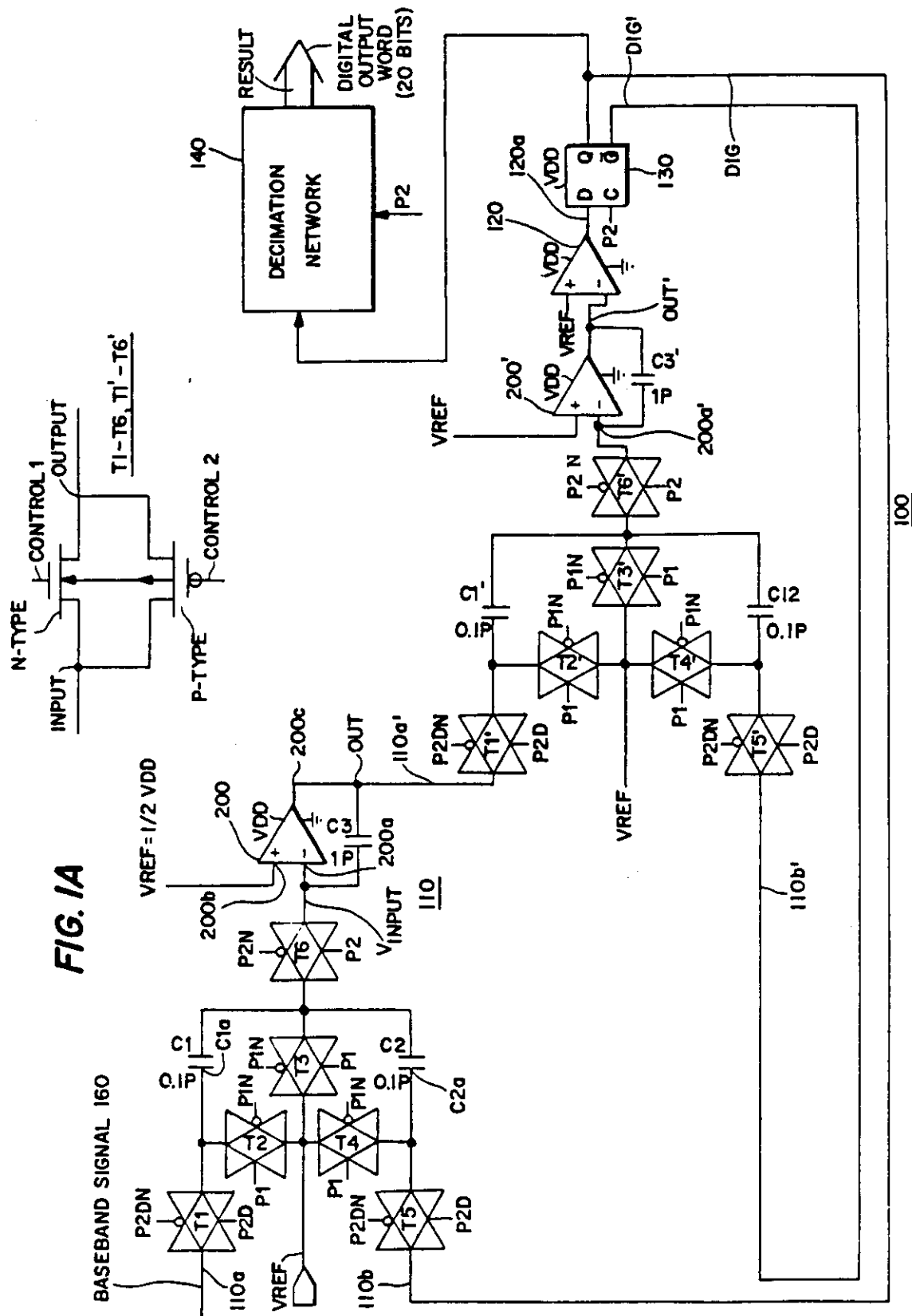
(74) Agent and/or
Address for Service
R W Pratt/T I M Smith
Burdett House
15-16 Buckingham Street
London
WC2N 6DU
United Kingdom

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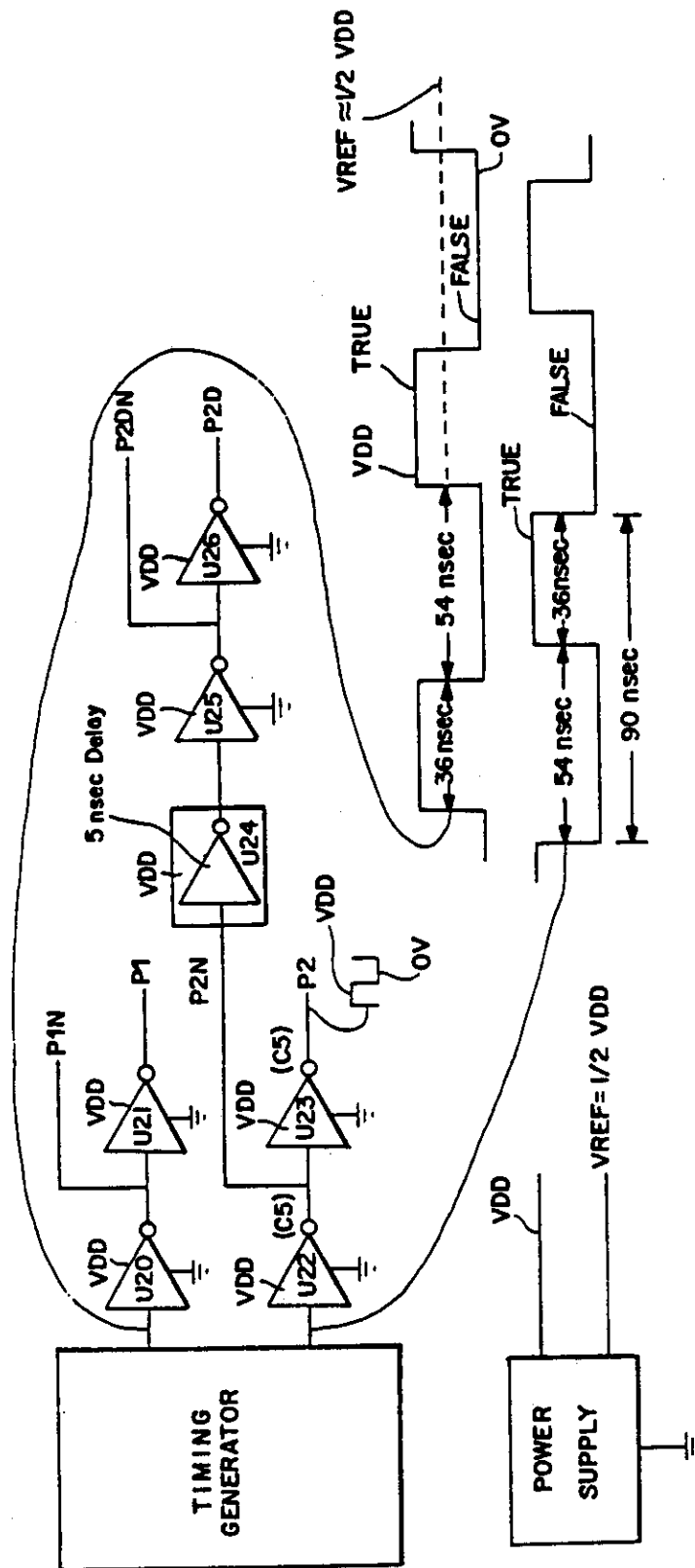
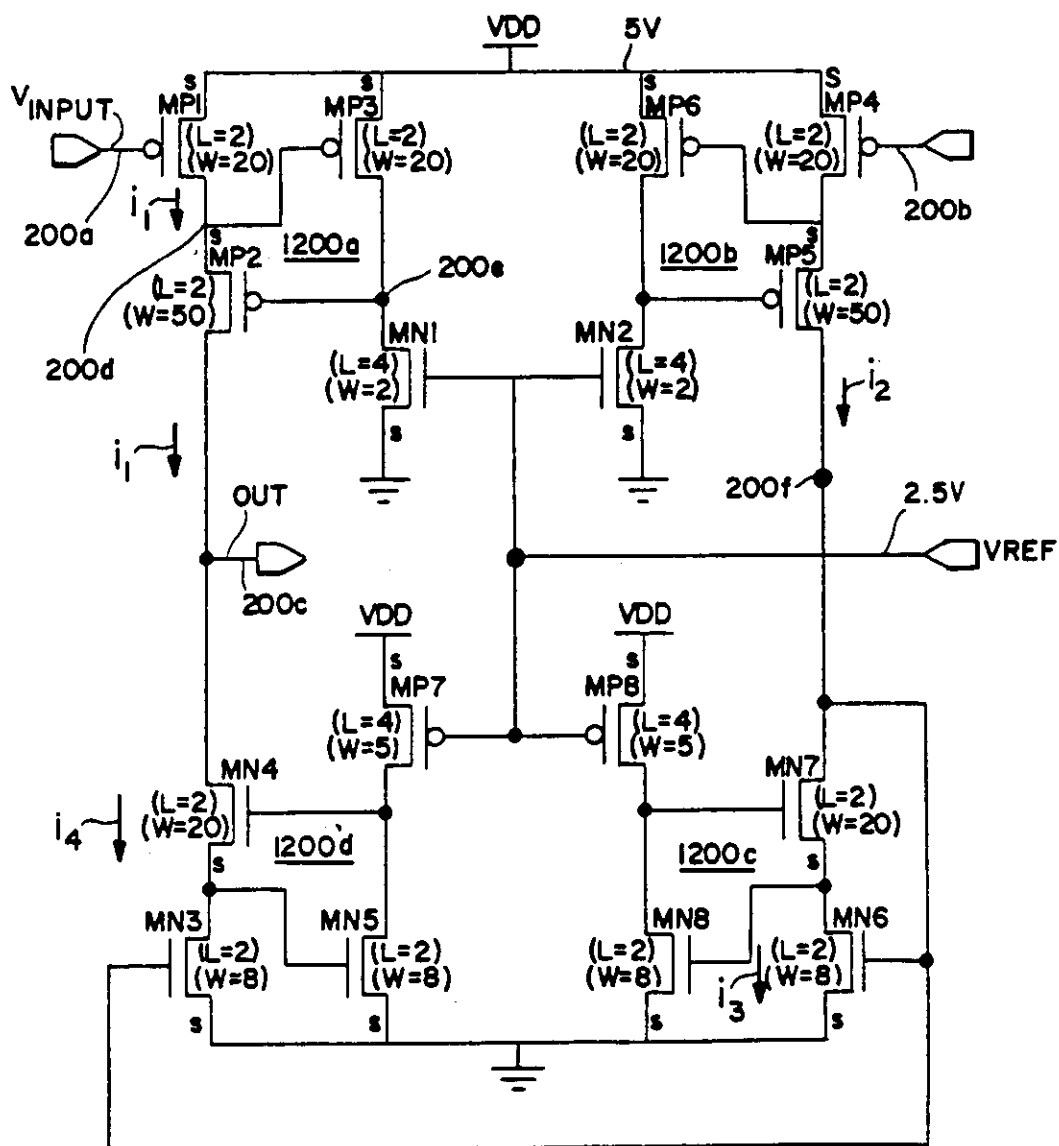


FIG. 1B

FIG. 2



200

L = CHANNEL LENGTH IN MICRONS
W = CHANNEL WIDTH IN MICRONS

A MODIFIED CASCODE AMPLIFIER

The invention relates to amplifier circuitry for use in, for example, a signal integrator of a Sigma-Delta ($\Sigma\Delta$) modulator.

5 In, for example, a stereo decoder that utilizes digital techniques, an analog-to-digital (A/D) converter is used for converting an analog, baseband stereo signal to a digital output signal. The digital output signal is processed in the stereo decoder to form a pair of decoded
10 audio signals that are, generally, referred to as the left channel audio signal and the right channel audio signal, respectively.

A baseband stereo signal that is in accordance with, for example, the BTSC standard, may have a bandwidth
15 of 75 KHz. Therefore, the A/D conversion rate required has to be higher than the minimum required by the Nyquist sampling criteria such as, for example, 200KHz. In order to obtain a minimum predetermined signal-to-noise ratio the quantization resolution in the output word of the A/D
20 converter may have to be, for example, 20 bits.

In an arrangement embodying the invention, the A/D converter operates as a $\Sigma\Delta$ A/D converter that utilizes, advantageously, the metal-oxide-semiconductor (MOS) technology such as, for example, the CMOS technology. The
25 CMOS technology provides, advantageously, relatively high speed operation with low power consumption.

A typical $\Sigma\Delta$ A/D converter includes a signal integrator stage responsive to a sum signal. The sum signal is formed by the summation of an analog input signal
30 and an internally generated bilevel analog signal. An output signal of the signal integrator is coupled to an input terminal of a threshold detector that generates a bilevel digital signal having a first state when the output signal of the integrator is smaller than a first
35 predetermined level and having a second state, otherwise. The signal generated by the threshold detector is stored in a flip-flop at a predetermined rate. The output signal from

the flip-flop is used for generating the bilevel analog signal portion of the sum signal.

5 A signal integrator is constructed using a switched capacitor network operating at a given frequency. The signal integrator includes an amplifier, embodying an aspect of the invention, and a signal integrating capacitor coupled between an inverting input terminal and an output terminal of the amplifier. The external load coupled to the output terminal of the amplifier that includes the
10 integrating capacitor forms a high impedance.

In order to obtain low harmonic distortions, or high linearity that is better than, for example, 0.1%, the steady state or DC gain of the amplifier has to exceed a
15 minimum predetermined value. Because the external load that is coupled to the amplifier forms a high impedance, high DC open loop gain may be obtained by maintaining the internal output impedance of the amplifier high.

An interelectrode capacitance that is developed
20 at the input to the amplifier may be nonlinear, and may adversely affect the linearity of the amplifier. Therefore, it is desirable to reduce the so-called Miller effect on the input capacitance of the amplifier so as to maintain the effect of the input capacitance small.

25 According to an aspect of the invention, there is provided an amplifier being responsive to an input signal for generating an output signal in accordance with said input signal, comprising:

a first transistor having first and second main
30 current conducting electrodes and having a control electrode that is coupled to said input signal such that input signal changes cause a first current to flow in said first main conducting electrode;

a second transistor having a first main current
35 conducting electrode for generating therein an output current and having a second main current conducting electrode that is coupled to said first main current conducting electrode of said first transistor, said second

transistor having a control electrode in which a first voltage is developed for controlling a second voltage formed at said first main current conducting electrode of said first transistor and wherein said first and second
5 transistors form a cascode-like arrangement;

voltage amplifying means coupled to said first and second transistors and responsive to said second voltage for generating said first voltage by amplifying said second voltage in accordance with a voltage gain of
10 said voltage amplifying means, said amplified first voltage being coupled back to said first main current conducting electrode of said first transistor via said second transistor in a negative feedback manner to maintain said second voltage substantially constant when changes occur in
15 said first current that flows in said first transistor such that by maintaining said second voltage substantially constant, said voltage amplifying means prevents an output signal, that is developed at said first main current
conducting electrode of said second transistor, from
20 substantially affecting said first current that, in turn, causes an output impedance at said first main current conducting electrode of said second transistor to increase in accordance with said voltage gain of said voltage
amplifying means; and

25 temperature compensated means coupled to said first main current conducting electrode of said second transistor and responsive to an input, third voltage for conducting at least a portion of an output current that flows in said first main current conducting electrode of
30 said second transistor such that in a closed-loop, configuration of said amplifier, that occurs when said output signal is coupled back to said control electrode of said first transistor in a negative feedback manner, the voltage at said first control electrode of said first
35 transistor is established at a predetermined level that is in accordance with said input, third voltage.

FIGURES 1A and 1B that form FIGURE 1 illustrate a schematic diagram of a Sigma-Delta A/D converter that includes a signal integrator, embodying an aspect of the invention; and

5 FIGURE 2 illustrates the detailed schematic of an amplifier, embodying another aspect of the invention, that is included in the signal integrator of FIGURE 1.

FIGURE 1 illustrates a $\Sigma\Delta$ A/D converter 100. A/D converter 100 includes a signal integrator 110 that
10 utilizes the switched capacitor circuit technique. Signal integrator 110 receives, at an input terminal 110a, an analog input signal 160 that is to be converted to its digital equivalent and receives an internally generated bilevel signal DIG at a terminal 110b. Integrator 110
15 provides a signal OUT at an output terminal 200c of an amplifier 200. Input signal 160 may be, for example, a baseband stereo signal generated by, for example, an FM decoder of a television receiver, not shown in the FIGURES, that is in accordance with, for example, the BTSC standard.
20 Amplifier 200 has an inverting input terminal 200a. An integrating capacitor C3 is coupled between terminals 200c and 200a. A noninverting input terminal 200b is coupled to a DC voltage VREF. The closed loop response of the amplifier and feedback capacitor tends to establish the
25 potential at the inverting input 200a of amplifier 200 at the level of voltage VREF.

Input signal 160 at terminal 110a is coupled to a first terminal C1a of a capacitor C1 via, for example, a conventional complementary transistor transmission gate T1.
30 Transmission gate T1, which utilizes the CMOS technology, is controlled by complementary clock signals P2D and P2DN causing the corresponding pair of transistors of transmission gate T1 to be conductive when signal P2D is

TRUE, or high. The other terminal of capacitor C1 is coupled through a transmission gate T6 to the inverting input terminal 200a of amplifier 200. Transmission gate T6 is controlled by complementary clock signals P2 and P2N causing it to be conductive when signal P2 is TRUE, or high. Transmission gates T1 and T6 are conductive simultaneously during a first portion of each period of, for example, signal P2D, and are both nonconductive during a second portion of it. Thus, transmission gates T1 and T6 operate at the frequency of signal P2D, that is, for example, 11 MHz.

Terminal C1a of capacitor C1 is also coupled to voltage VREF through a transmission gate T2, when transmission gate T2 is conductive. The other terminal of capacitor C1 is coupled to voltage VREF through a transmission gate T3, when transmission gate T3 is conductive. Transmission gates T2 and T3 are controlled by clock signals P1 and P1N and operate at the same frequency as signal P2D. When transmission gates T2 and T3 are conductive, transmission gates T1 and T6 are not, and vice versa.

Timing generator 180 of FIGURE 1B produces a pair of timing signals, and applies them to respective branches of circuitry comprising inverters U20-U23, a delay unit U24, and further inverters U25 and U26, for ultimate production of timing signals P1, P1N, P2, P2N, P2D and P2DN.

Bilevel signal DIG, generated in a manner that is described later on, is coupled to terminal 110b of integrator 110. Terminal 110b is coupled via a transmission gate T5 to a terminal C2a of a capacitor C2. Transmission gate T5 is controlled by complementary clock signals P2D and P2DN causing it to be conductive when clock signal P2D is high. The other terminal of capacitor C2 is coupled to a junction terminal between transmission gates T6 and T3. Terminal C2a is coupled to voltage VREF via a transmission gate T4 when it is conductive. Transmission gate T4 is controlled by clock signals P1 and P1N. Transmission gates T4 and T5 operate similarly to, and

simultaneously with, transmission gates T2 and T1, respectively.

Clock signals P2D and P2DN that control transmission gates T1 and T5 are similar to, but delayed by approximately 5 nsec from, clock signals P2 and P2N, respectively. Each of signals P1, P2 and P2D is a bilevel signal having a waveform of, for example, 40% duty cycle and a period of, for example, approximately 90 nsec. When signal P1 is at a TRUE or high state, signal P2 is always at a FALSE or low state such that signals P1 and P2 are nonoverlapping signals. The result is that when transmission gates T1, T5 and T6 are conductive, transmission gates T2, T3 and T4 are not, and vice versa.

In operation, transmission gates T2, T3 and T4 are simultaneously rendered conductive, during a first portion of each period of, for example, clock signal P1, to discharge capacitors C1 and C2. The potential on the respective electrodes of capacitors C1 and C2 is established at that of voltage VREF, which is substantially equal to the potential at the inverting input terminal 200a of amplifier 200 (+ the amplifier input offset potential). Transmission gates T2, T3 and T4 are then rendered non-conductive and transmission gates T1, T5 and T6 conductive. Input terminal 200a is maintained at a virtual AC ground because of the amplifier feedback connection. Thus capacitors C1 and C2 charge to the respective input voltages at terminals 110a and 110b. The charging current is integrated in capacitor C3, producing an output signal OUT that is proportional to the time integral of the sum of the two input signals at terminals 110a and 110b.

The N-channel and P-channel MOS transistors of a given transmission gate such as shown in FIGURE 1A are coupled in parallel and require opposing clock signals. Signal feedthrough to an output terminal OUTPUT of such transmission gate due to the clock will be reduced as a result of cancellation. However, the cancellation is not complete.

Moreover, disadvantageously, the level of the uncanceled feedthrough signal is nonlinearly dependent on the voltages at the signal terminals INPUT and OUTPUT of such transmission gate. The voltage dependency is caused because, for example, the charge stored in the inversion layer of each of the MOS transistors of such transmission gate, when the transmission gate is conductive, is nonlinearly dependent on the voltages at terminals INPUT and OUTPUT. A voltage change in a given direction in, for example, input terminal INPUT may cause the charge in the inversion layer of one of the complementary transistors to increase by a corresponding amount and in the other one to decrease by a different amount such that the difference between the charge increase and decrease is nonlinearly dependent on the voltage at terminal INPUT.

A corresponding portion of the charge stored in the inversion layer in each of the complementary transistors is coupled to terminal OUTPUT during the turn-off transition of the transmission gate. Thus, a net charge, that is equal to the difference between the corresponding portions of the charges in each of the complementary transistors of, for example, transmission gate T1, is coupled to the corresponding terminal OUTPUT. In the operation of transmission gate T1, the net charge may be transferred to capacitor C1 during the transition edges of clock signals P2D and P2DN that cause transmission gate T1 to be turned off. Such net charge is nonlinearly dependent on the voltage at its input terminal INPUT that is equal to input signal 160. If such net charge is permitted to be coupled to integrating capacitance C3, it will cause, disadvantageously, linearity degradation in the operation of, for example, signal integrator 110.

To prevent such linearity degradation, transmission gate T6 that is controlled by clock signals P2 and P2N is, advantageously, turned off approximately 5 nanoseconds prior to the time transmission gates T1 and T5 are turned off. Thus, advantageously, such net charge transfer in, for example, transmission gate T1 will be

prevented by transmission gate T6, that is then already non-conductive, from affecting signal OUT.

5 If the steady state gain of amplifier 200 is high and if integrator 110 achieves steady state operation prior to the turn-off transition of transmission gate T6, the net charge coupled by transmission gate T6 during its turn-off transition will not degrade the linearity of integrator 110. This is so, because such net charge will not be dependent on the level of signal 160 since corresponding
10 voltages at each of the signal terminals of transmission gate T6 are at the same constant level that is approximately equal to voltage VREF.

On the other hand, as a result of, for example, a relatively high rate of change of input signal 160, steady
15 state operation may not occur immediately prior to the turn-off of transmission gate T6. Therefore, the voltages at the signal terminals of transmission gate T6, immediately prior to its turn-off time, may be different in accordance with the level of input signal 160 that exists
20 at such turn-off time. In such situation, the net charge that is coupled to terminal OUTPUT of transmission gate T6 may be, disadvantageously, nonlinearly dependent on input signal 160. It is desirable to reduce the nonlinear voltage dependent effect on the net charge in transmission gate T6.

25 The nonlinearity in the voltage dependency of the net charge is reduced by operating the two transistors in a symmetrical manner. Symmetrical operation of the transistors of transmission gate T6 means that each of the complementary transistors of the transmission gate contains
30 substantially the same charge at least immediately before gate turn-off.

Symmetrical operation is accomplished by biasing the circuitry so that the input and output terminals of the transmission gate tend to be biased midway between the
35 complementary potentials of the clock signals that are applied to the gate electrodes.

To accomplish the symmetrical operation, voltage VREF that is coupled to noninverting terminal 200b is

established at a level that is equal to the midpoint of the two levels of, for example, clock signal P2. In this way, voltage V_{input} , that is developed at output terminal OUTPUT of transmission gate T6, is also established at the level of voltage VREF as a result of the feedback. The input terminal of transmission gate T6 follows the potential at its output terminal because it is operating as a relatively low impedance switch.

Since the two transistors of transmission gate T6 operate symmetrically and have similar characteristics, a change in the net charge that is produced by a given change in the voltage at, for example, its output terminal OUTPUT will be, advantageously, smaller than if they did not operate symmetrically. The net change will also be, advantageously, less nonlinearly dependent on the level of input signal 160.

A signal DIG', having an inverted waveform of that of signal DIG, and signal OUT are coupled to input terminals 110b' and 110a' of a second signal integrator 110' that operates similarly to integrator 110. Similar items and functions in integrators 110 and 110' are depicted by similar numerals and symbols. Integrator 110' generates an output signal OUT' that is proportional to the time integral of a sum of signal OUT from integrator 110 and of signal DIG'.

Signal OUT' is coupled to an input terminal of a comparator 120 that generates a digital, bilevel signal 120a. Signal 120a is at a TRUE state when signal OUT' is below a predetermined threshold level that is substantially equal to voltage VREF and at a FALSE state, otherwise. Bilevel signal 120a is clocked into a "D" type or data flip-flop 130 by the falling edge of clock signal P2. Flip-flop 130 produces complementary signals DIG and DIG' at its corresponding output terminals at states that correspond with the state of signal 120a. Because the falling edge of signal P2 simultaneously causes both the clocking of flip-flop 130 and the turn-off of transmission gates T6 and T6', the transient perturbations that may be

associated with the turning-off of transmission gates T6 and T6', advantageously, are prevented from affecting signals DIG and DIG'. Signal DIG is coupled to integrator 110 in a negative feedback manner; similarly, signal DIG' is coupled to integrator 110' in a negative feedback manner.

Signal DIG may be at one of its TRUE and FALSE states in each period of, for example, signal P2. When signal DIG is at the TRUE or high state, it is larger than voltage VREF. On the other hand, when it is at the FALSE or low state it is smaller than voltage VREF. Thus, in a given period of signal P2, if signal DIG is at the TRUE state, it causes signal OUT to decrease. On the other hand, if signal DIG is at the FALSE state, it causes signal OUT to increase. Thus, signals DIG provides negative feedback in such a way so as to form a first portion of the current in capacitor C2 that has an average value that is equal to, but of the opposite polarity of, a second portion of the current in capacitor C2 that is caused by signal 160. Consequently, when input signal 160 causes signal OUT of integrator 110, for example, to increase, signal DIG causes it to decrease, and vice versa, in a negative feedback manner. Similarly, in integrator 110', when signal OUT causes signal OUT', for example, to increase, signal DIG' causes it to decrease, and vice versa, in a negative feedback manner. The advantages in using double integration such as formed by integrators 110 and 110' is described in, for example, an article entitled, A USE OF DOUBLE INTEGRATION IN SIGMA DELTA MODULATION, in the name of James C. Candy, published in IEEE TRANSACTIONS ON COMMUNICATIONS Vol. COM-33, No. 3, March 1985.

Signal DIG is coupled to a decimation network 140 that generates a parallel word RESULT, providing the digital representation of analog input signal 160. An example of such decimation network is described in, for example, an article entitled A Sigma-Delta Modulator As An A/D Converter, in the name of Rudy J. Van De Plassche, published in IEEE TRANSACTION ON CIRCUIT AND SYSTEMS, Vol.

CAS-25, No. 7, July 1978. Parallel word RESULT of decimation network 140, may be formed, in accordance with the teaching of Van De Plassche, by computing a difference between the number of periods of, for example, signal P2, occurring during a predetermined interval N, when signal DIG is at the TRUE state and the number of such periods of signal P2, during interval N, when signal DIG is at the FALSE state. Interval N is selected in accordance with the bit resolution of word RESULT that is required. The longer interval N is, the higher is the bit resolution.

In order to obtain high accuracy, and, in particular, high linearity in A/D converter 100, it is desirable to have the steady state or DC gain of amplifier 200 high. The steady state or DC gain determines the level of voltage V_{input} immediately prior to transmission gate T6 becoming nonconductive in each period of signal P2. The large DC gain will cause input voltage V_{input} at input terminal 200a of amplifier 200 to remain substantially constant irrespective of the level of analog input signal 160. Also, it is desirable to reduce the Miller effect on the input capacitance at, for example, terminal 200a which capacitance may in fact be non-linear.

FIGURE 2 illustrates a detailed schematic diagram of amplifier 200, embodying another aspect of the invention, that is included in, for example, signal integrator 110 of FIGURE 1. Similar numerals and symbols in FIGURES 1 and 2 indicate similar items or functions. The circuit of FIGURE 2 is constructed using MOS technology that, advantageously, provides high frequency capability with relatively low power consumption.

Input voltage V_{input} at inverting input terminal 200a of amplifier 200 of FIGURE 2 is coupled to a gate electrode of a P-type field effect, or PMOS transistor MP1 operating as a an inverting, common source amplifier. The drain electrode of transistor MP1 is coupled to the source electrode of a PMOS transistor MP2 via a junction terminal 200d.

In carrying out an aspect of the invention, junction terminal 200d is coupled to a gate electrode of a PMOS transistor MP3 operating as an inverting, common source amplifier. The drain electrode of transistor MP3 is coupled, at a terminal 200e, to the gate electrode of transistor MP2 for varying the gate voltage of transistor MP2. A drain electrode of an N-type field effect, or NMOS transistor MN1, operating as a current source, is coupled to terminal 200e to form a load impedance that determines the voltage gain of transistor MP3. The gate electrode of transistor MN1 is coupled to voltage VREF. Transistors MP1, MP2, MP3 and MN1 form a modified cascode-like arrangement 1200a, embodying an aspect of the invention. Output signal OUT is developed at the drain electrode of transistor MP2. Terminal 200a is the inverting input terminal and terminal 200c is the output terminal of arrangement 1200a.

A change in input voltage V_{input} causes a corresponding change in current i_1 flowing through transistors MP1 and MP2 and causes a voltage change at terminal 200e. The signal at terminal 200e that is the amplified signal developed at terminal 200d is fed back via transistor MP2 to terminal 200d. Because of such negative feedback, variations of current i_1 caused by changes in voltage V_{input} , create significantly smaller voltage variations at terminal 200d than would be created if the gate of transistor MP2 had been maintained constant. In contrast, in, for example, a well known conventional cascode arrangement such negative feedback arrangement is not utilized. The factor by which the voltage variations at terminal 200d become smaller is equal, approximately, to the voltage gain of the common source amplifier comprised of transistors MP3 and MN1. Because the response time of transistors MP2 and of the closed-loop arrangement formed by transistors MP2 and MP3 is fast, the voltage at terminal 200d remains, advantageously, relatively unchanged immediately after an abrupt change occurs in current i_1 flowing in transistor MP1.

Because the drain voltage of transistor MP1 at terminal 200d undergoes only slight changes, its drain current i_1 is substantially unmodulated by changes in drain voltage of transistor MP2 at terminal 200c. Consequently current i_1 that flows also in transistor MP2 is substantially unmodulated by changes in signal OUT at the drain of transistor MP2. Thus, advantageously, the output impedance at terminal 200c is increased by an amount that is proportional to the voltage gain of transistor MP3.

In accordance with a feature of the invention, because of the feedback arrangement formed by transistor MP3 that reduces the variation in the voltage at terminal 200d, the Miller effect on the input capacitance at terminal 200a is, advantageously, even further reduced relative to what it would have been had such negative feedback arrangement not been used. By reducing the Miller effect on the input capacitance, the effective input capacitance is maintained small. Consequently, the effect of any nonlinearity of the input capacitance that may, otherwise, adversely affect the linearity of, for example, integrator 110 of FIGURE 1 is, advantageously, reduced.

As explained before, arrangement 1200a of FIGURE 2 that is included in amplifier 200 having input terminal 200a and output terminal 200c is formed by transistors MP1, MP2, MP3 and MN1. In addition to arrangement 1200a, amplifier 200 also includes arrangements 1200b, 1200c and 1200d, each being formed by corresponding four MOS transistors in a similar manner by which arrangement 1200a is formed. The differences between those arrangements and arrangement 1200a are explained below.

Arrangement 1200b includes transistors MP4, MP5, MP6 and MN2 that correspond with transistors MP1, MP2, MP3 and MN1, respectively, of arrangement 1200a. An input terminal 200b of arrangement 1200b that is coupled to the gate of transistor MP4 is at the voltage level of voltage VREF. An output terminal 200f of arrangement 1200b is coupled to the drain electrode of transistor MP5. Because circuits 1200a and 1200b are identical circuit arrangements

a current i_2 that flows in transistor MP5 is equal to current i_1 that flows in transistor MP2 when the voltages at terminals 200a and 200b are equal. Moreover, currents i_1 and i_2 remain equal when the ambient temperature changes.

Arrangement 1200c includes transistors MN6, MN7, MN8 and MP8 that correspond with transistors MP1, MP2, MP3 and MN1, respectively, of arrangement 1200a; however, each PMOS type transistor in arrangement 1200a, is replaced in arrangement 1200c by an NMOS transistor, and vice versa. Terminal 200f of arrangement 1200b is coupled to the drain electrode of transistor MN7 and to the gate electrode of transistor MN6. Consequently, the gate voltage of transistor MN6 is established at such a level that a current i_3 flowing in transistor MN6 becomes equal to current i_2 . Thus, when the input voltages at terminals 200a and 200b are equal, current i_3 is equal to current i_1 and, advantageously, tracks temperature caused variations of current i_1 .

Arrangement 1200d includes transistors MN3, MN4, MN5 and MP7 that correspond with transistors MP1, MP2, MP3 and MN1, respectively, of arrangement 1200a. As in the case of arrangement 1200c, each PMOS type transistor in arrangement 1200a is replaced in arrangement 1200c by an NMOS type transistor, and vice versa. The gate electrode of transistor MN3 is coupled to terminal 200f of arrangement 1200b and 1200c and the drain electrode of transistor MN4 is coupled to output terminal 200c of arrangement 1200a. Consequently, current i_3 that flows in transistor MN6 of arrangement 1200c is mirrored in transistor MN3 and is equal to current i_1 when the voltages at input terminals 200a and 200b are equal, and advantageously, tracks temperature caused variations of current i_1 . It follows that arrangements 1200b, 1200c and 1200d cause the offset voltage of amplifier 200 to be approximately or nominally zero in a way that is, advantageously, temperature compensated. Thus, in the closed-loop configuration of amplifier 200, such as shown

in FIGURE 1, voltage V_{input} is equal to voltage V_{REF} , during steady state operation.

In accordance with another aspect of the invention, cascode-like arrangement 1200d exhibits high
5 output impedance at terminal 200c that maintains the open loop DC gain of arrangement 1200a, advantageously, high.

Voltage V_{REF} is at a level that provides a sufficient dynamic range to signal OUT of arrangement 1200a of FIGURE 2, and a required DC voltage across transistor
10 MP1.

CLAIMS:

1. An amplifier being responsive to an input signal for generating an output signal in accordance with said input signal, comprising:
 - 5 a first transistor having first and second main current conducting electrodes and having a control electrode that is coupled to said input signal such that input signal changes cause a first current to flow in said first main conducting electrode;
 - 10 a second transistor having a first main current conducting electrode for generating therein an output current and having a second main current conducting electrode that is coupled to said first main current conducting electrode of said first transistor, said second
 - 15 transistor having a control electrode in which a first voltage is developed for controlling a second voltage formed at said first main current conducting electrode of said first transistor and wherein said first and second transistors form a cascode-like arrangement;
 - 20 voltage amplifying means coupled to said first and second transistors and responsive to said second voltage for generating said first voltage by amplifying said second voltage in accordance with a voltage gain of said voltage amplifying means, said amplified first voltage
 - 25 being coupled back to said first main current conducting electrode of said first transistor via said second transistor in a negative feedback manner to maintain said second voltage substantially constant when changes occur in said first current that flows in said first transistor such
 - 30 that by maintaining said second voltage substantially constant, said voltage amplifying means prevents an output signal, that is developed at said first main current conducting electrode of said second transistor, from substantially affecting said first current that, in turn,
 - 35 causes an output impedance at said first main current conducting electrode of said second transistor to increase in accordance with said voltage gain of said voltage amplifying means; and

temperature compensated means coupled to said first main current conducting electrode of said second transistor and responsive to an input, third voltage for conducting at least a portion of an output current that
5 flows in said first main current conducting electrode of said second transistor such that in a closed-loop, configuration of said amplifier, that occurs when said output signal is coupled back to said control electrode of said first transistor in a negative feedback manner, the
10 voltage at said first control electrode of said first transistor is established at a predetermined level that is in accordance with said input, third voltage.

2. An amplifier according to Claim 1 wherein said temperature compensated means comprises a source of
15 current for generating a second current that is equal in magnitude to, and at the same polarity of said output current when said input, third voltage is substantially equal to the voltage at said control electrode of said first transistor and current mirror means responsive to
20 said second current and coupled to said first main current conducting electrode of said second transistor for conducting said portion of said output current that is substantially equal in magnitude to said second current.

3. An amplifier according to Claim 2 wherein
25 said source of current comprises third and fourth transistors and second voltage amplifying means, said fourth transistor being coupled to said third transistor and to said second voltage amplifying means in a way that is similar to the way said second transistor is coupled to
30 said first transistor and to said first voltage amplifying means.

4. An amplifier according to Claim 1 further comprising, a transmission gate that is controlled by a pair of binary signals such that one of said binary signals of said pair of signals is inverted relative to the other one of said pair of binary signals, said transmission gate having a pair of main current conducting terminals such that one of said pair is coupled to said control electrode of said first transistor for coupling said input signal thereto, wherein said input, third voltage is established at a level that is determined in accordance with the two levels of a given one of said pair of binary signals that causes a portion of one of said pair of binary signals that is capacitively coupled through a stray capacitance of said transmission gate to one of said pair of main current conducting terminals of said transmission gate to be substantially cancelled by a portion of the other one of said pair of binary signals.

5. An amplifier according to Claim 4 wherein said level of said input, third voltage is established at the midpoint of the two levels of said given one of the binary signals that control said transmission gate.

6. An amplifier according to Claim 4 wherein said transmission gate comprises a pair of complementary MOS transistors.

7. Amplifier according to Claim 4 further comprising, a capacitance coupled between said first main current conducting electrode of said second transistor and said control electrode of said first transistor to form said closed-loop configuration, wherein said transmission gate is included in a switched capacitor network, responsive to said input signal that couples said input signal to said first transistor such that said amplifier, said capacitance and said switched capacitor network form a signal integrator for generating said output signal by integrating said input signal.

8. An amplifier substantially as hereinbefore described with reference to Figure 2 optionally together with Figures 1A and 1B of the accompanying drawings.

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Title A MODIFIED CASCODE AMPLIFIER

Applicant/Proprietor

RCA LICENSING CORPORATION, Incorporated in USA - Delaware, 2 Independence Way, Princeton, New Jersey 08540, United States of America

[ADP No. 00697326001]

Inventors

DONALD JON SAUER, 8 Twain Drive, Allentown, New Jersey, United States of America

[ADP No. 00282426002]

TODD J CHRISTOPHER, 1402 South Kitley Avenue,, Indianapolis,, Indiana,, United States of America

[ADP No. 02268563001]

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Address for Service

RICHARD W PRATT, GENERAL ELECTRIC TECHNICAL SERVICES COMPANY INC, London Patent Operation, Burdett House, 15-16 Buckingham Street, LONDON, WC2N 6DU, United Kingdom

[ADP No. 00003954004]

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RICHARD W PRATT, GENERAL ELECTRIC TECHNICAL SERVICES COMPANY INC, London Patent Operation, Burdett House, 15-16 Buckingham Street, LONDON, WC2N 6DU, United Kingdom

[ADP No. 00003954004]

to

RICHARD W PRATT, GENERAL ELECTRIC TECHNICAL SERVICES COMPANY INC, London Patent Operation, Essex House, 12-13 Essex Street, LONDON, WC2R 3AA, United Kingdom

[ADP No. 00003954005]

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RCA LICENSING CORPORATION, Incorporated in USA - Delaware, 2
Independence Way, Princeton, New Jersey 08540, United States of
America [ADP No. 00697326001]
to
RCA THOMSON LICENSING CORPORATION, Incorporated in USA - Delaware,
2 Independence Way, Princeton, New Jersey 08540, United States of
America [ADP No. 05964408001]
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2 Independence Way, Princeton, New Jersey 08540, United States of
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