United States Patent [19]

Kafafian

[11] **3,831,147**

[45] **Aug. 20, 1974**

[54] **COMMUNICATION SYSTEM FOR THE HANDICAPPED**

[76] Inventor: **Haig Kafafian,** 4201 Cathedral Ave., Washington, D.C. 20016

[22] Filed: **Jan. 26, 1972**

[21] Appl. No.: **220,995**

[52] **U.S. Cl.** ..... **340/166 R**
[51] **Int. Cl.** **H04q 3/00**
[58] **Field of Search** ..... 340/166 R

[56] **References Cited**

UNITED STATES PATENTS

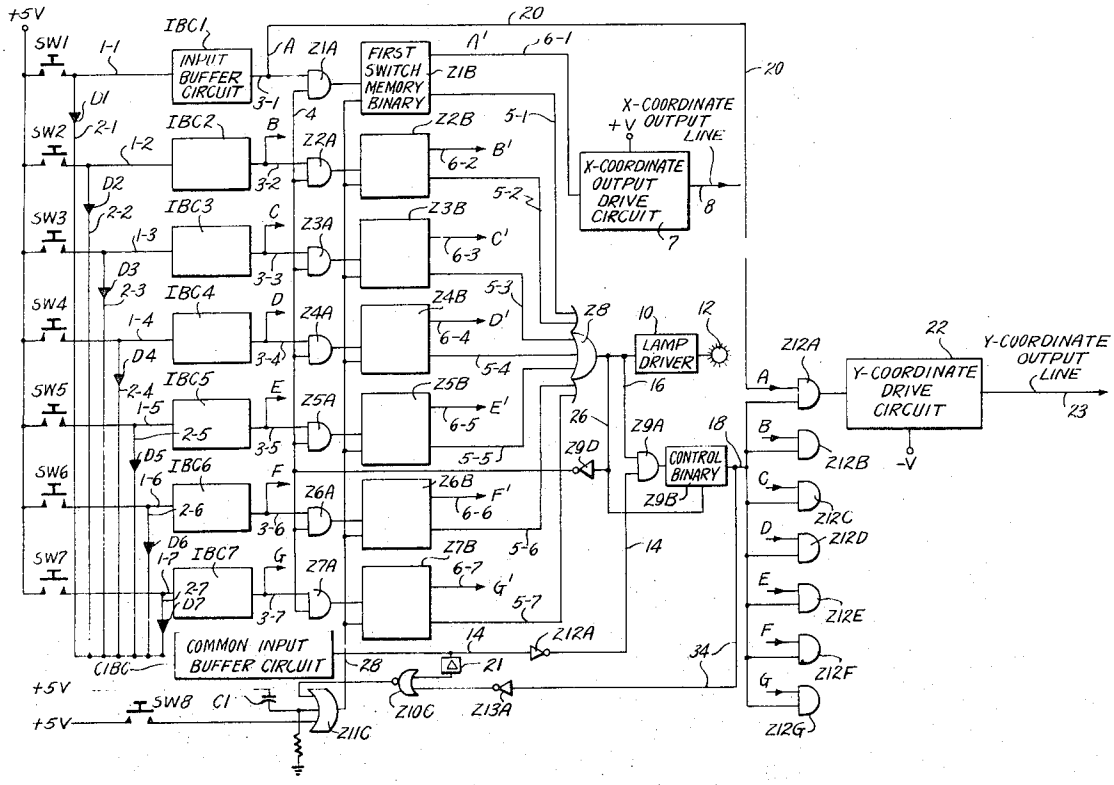
3,220,000	11/1965	Lesage	340/166 UX
3,317,783	5/1967	Neumeister	340/166 UX
3,480,945	11/1969	Nelson	340/166 UX
3,541,541	11/1970	Engelbart	340/166 UX
3,551,888	12/1970	Balugani	340/166 R
3,573,388	4/1971	Pagnall	340/166 R
3,582,892	6/1971	Juliusburger	340/166 R
3,593,289	7/1971	Lerch	340/166 X
3,597,737	8/1971	Wallace	340/166 R

Primary Examiner—Harold I. Pitts
Attorney, Agent, or Firm—Bacon & Thomas

[57] **ABSTRACT**

A seven-key hard wire controller with a dual-sequence operation is used to provide an output signal for producing a typed symbol or the like. When used in a matrix arrangement, the first actuation of one of the switches will provide an X-coordinate, and the second actuation of one of the switches will provide the Y-coordinate. Circuitry is provided to store the X-coordinate signal until the second switch actuation occurs. Upon release of the second switch of the actuated pair, the symbol is typed or the desired function is activated, and the system is reset to accept another pair of inputs. The system is compatible with most types of electric typewriters, adding machines and punched and magnetic tape devices, as well as almost any machine where data or information is to be stored, printed, displayed or otherwise used.

7 Claims, 3 Drawing Figures



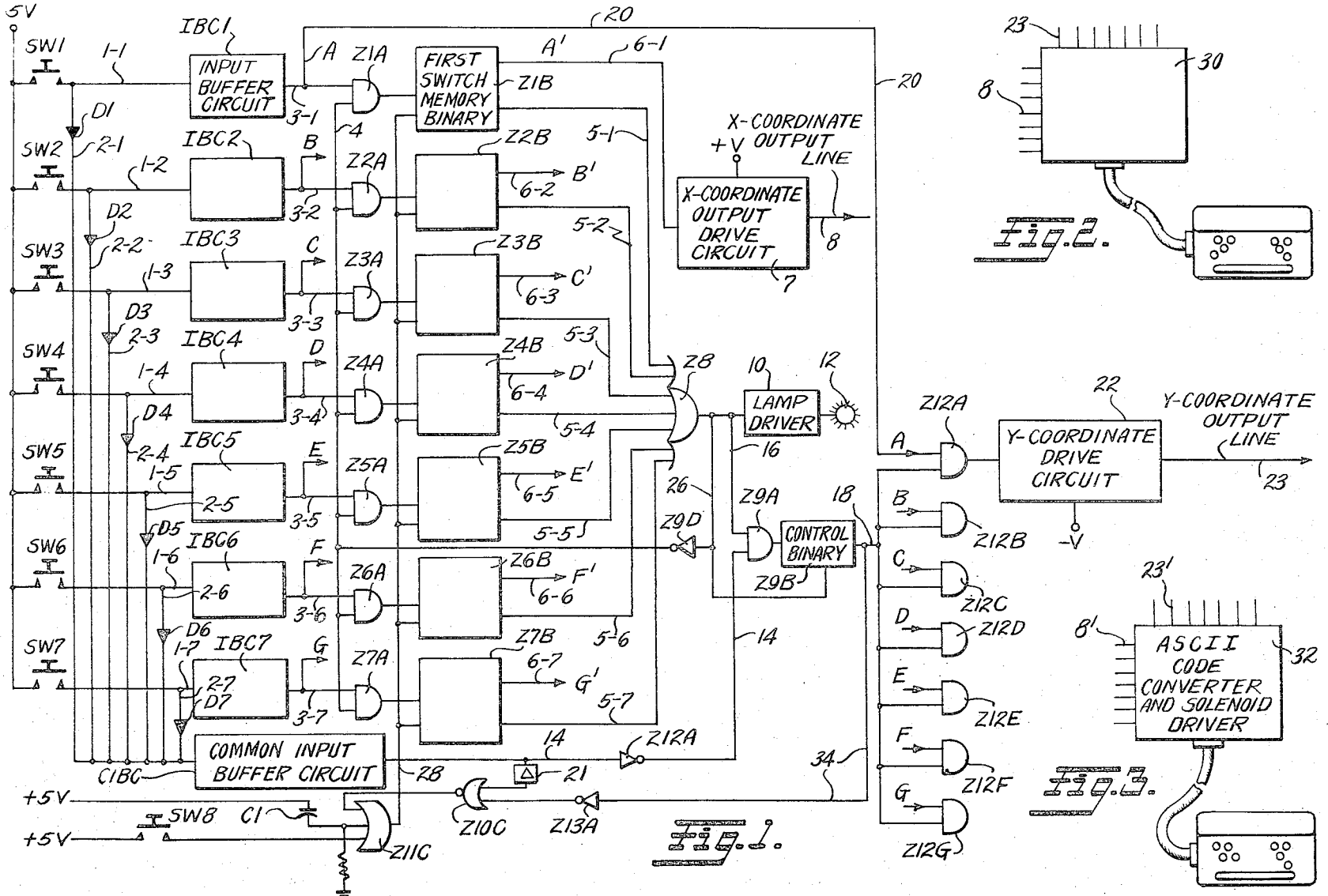


Fig. 1.

Fig. 2.

Fig. 3.

COMMUNICATION SYSTEM FOR THE HANDICAPPED

BACKGROUND OF THE INVENTION

The present invention relates to an improvement in systems for operating typewriters and other program-controlled machines which are particularly adapted for use by the blind, amputees, and those afflicted with debilitating diseases such as multiple sclerosis and cerebral palsy. Reference is made here to the extensive introductory portion in my previous U.S. Pat. No. 3,507,376 which will provide additional background information upon which that invention, as well as the instant invention, is based.

The operation of the system set out in my previous patent required a greater amount of manual dexterity than is often possessed by some handicapped persons. Also, due to certain disabilities in some persons, a system is needed having easier methods of actuation. At the same time it is desirable that the operator be required to exert as much movement as he is capable of, where required for therapeutic purposes.

In addition to my earlier patent, several others are worthy of note. Tevis, U.S. Pat. No. 2,031,017, illustrates a device having a number of input keys equivalent to the number of digits on a person's hand used to provide the X- and Y-coordinate inputs to actuate a plurality of solenoids representative of the keys on a typewriter, but their nature limits its utility.

Another communication device is illustrated in Seibel et al., U.S. Pat. No. **3,022,878,** which discloses a machine control system designed especially for aerospace applications wherein the operator is equipped with a three-position transducer for each finger and is required to perform small movements of his fingers in order to actuate the controls of the machine.

The high degree of manual dexterity in the above-mentioned systems and the high costs of manufacturing and of maintenance are the principal shortcoming thereof. The same is true of much of the other prior art, such as U.S. Pat. Nos. 2,532,228; 2,573,370; 2,613,797; 2,924,321; 3,166,856; 3,239,664 and 3,241,115.

SUMMARY OF THE INVENTION

The present system is of the hard wire type, and a seven-key controller or logic box contains the electronic circuitry required to convert a seven-key dual-sequential input to a 7 × 7 dual-concurrent output or other known input/output devices for the ultimate control of a typewriter, other business machines, or the like, or other programmable machines. The sequential momentary actuation of any two of the seven interface key-operated coding switches, which can include a repeat actuation of the very same switch, will produce an output from the controller.

A signal resulting from the actuation of the first interface switch of the sequentially operated pair is stored or time delayed, and is the X-coordinate of a 7 × 7 matrix. When the second switch is actuated, a Y-coordinate signal of the 7 × 7 matrix and the X-coordinate retrieved from storage are provided as outputs from the seven-key logic box. Upon release of the second switch of the actuated pair the logic circuitry is reset, the memory is cleared, and the logic box is ready to accept another sequentially paired input. The circuitry in the matrix can control a typewriter, or the X, Y-coordinates can be fed into a converter which will in turn control a ball typewriter such as manufactured by IBM under the trademark "SELECTRIC," or a teleprinter or the like, e.g., input/output typwriter, or display.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features of the invention are set forth in the appended claims. The invention itself, both as to its construction and manner of operation, together with additional objects and advantages thereof, will be understood from the following description of the preferred embodiments when read in conjunction with the accompanying drawing wherein:

FIG. **1** is a schematic diagram of a seven-key controller;

FIG. **2** is a block schematic showing the output from FIG. **2** feeding into a matrix arrangement which in turn controls a typewriter; and

FIG. **3** is a block schematic showing the outputs from FIG. **1** feeding into an ASCII code converter and solenoid driver, which in turn controls a typewriter.

DETAILED DESCRIPTION OF THE INVENTION

Reference is now made to FIG. **1** wherein there are illustrated seven interface coding switching means or transducers **SW1–SW7.** Energization of each switch feeds a signal over lines **1–1** to **1–7** into respective input buffer circuits ICB1–ICB7. Likewise, the energization of any of the switches SW1–SW7 also connects the potential to a common input buffer CIBC through a plurality of lines **2–1** to **2–7** and diodes D1–D7. As will be seen below, CIBC changes state prior to ICB1–ICB7 on actuation of the switch and reverts to the static state after ICB1-ICB7 on switch release. The outputs from the input buffer circuits ICB1–ICB7 are fed over lines **3–1** to **3–7** to respective X-coordinate input drive gates Z1A through Z7A. It will be noted that lines **3–1** through **3–7** are connected to one of the terminals of the input AND gates Z1A–Z7A. The other terminal of input AND gate is connected by a common line **4** as will be discussed below. The output of each input gate Z1A through Z7A is connected to one of the inputs of a respective number of first switch memory binaries Z1B through Z7B. One output, **5–1** through **5–7,** from each of the first switch memory binaries Z1B thorugh Z7B is connected to a logic element **Z8.** The logic element **Z8** changes state the instant a first bit representing a first switch actuation is loaded in one of the memories Z1B–Z7B. Each of the memories Z1B–Z7B have a second output **6–1** through **6–7** (also labeled A′–G′) connected to a respective X-coordinate output drive circuit **7** (only one of which is seen). The drive circuits are in turn directly connected to X-coordinate output lines, one of which is seen at **8.**

One output from logic element **Z8** is connected to a lamp driver circuit **10** which will illuminate a first bit indicator **12** which may be placed adjacent the interface panel to provide the operator with feedback to the effect that the first bit has been accepted and is stored in the memory. The output of element **Z8** is also connected via a line **26** to line **4** through an inverter **29D** which in turn is connected to the second of the input terminals of drive gates Z1A–Z7A, closing them. Line **26** is also connected to control binary **Z9B.**

When any one of the switches SW1–SW7 is released, an output from the common input buffer circuit CIBC places a signal on line **14** through an inverter Z12A to a logic AND gate element Z9A. There will also be an output from logic element Z8 over line **16** into AND gate Z9A. When the switch is released, therefor, there will be outputs over lines **14** and **16,** thus gating logic element Z9A "on," which in turn will gate "on" a control binary labeled Z9B. The output of the control binary Z9B will be fed over a line **18** to one terminal of a plurality of Y-coordinate driver gates Z12A–Z12G. The other input terminal of each of the logic elements Z12A–Z12G will be connected to respective output lines A–G of the input buffer circuit, one of which is seen as line **20.** Each of the Y-coordinate drive gates when gated "on" will transmit a signal to the appropriate Y-coordinate driver circuit, one of which is seen as **22.** The output of the Y-coordinate driver circuit is connected directly to a Y-coordinate output line **23.**

As will be discussed more fully below in the "OPERATION" section, it will be seen that actuation of the second switch of the sequential pair produces an output from its associated input buffer circuit IBC1–IBC7 which is transmitted to the appropriate Y-coordinate output driver circuit (for example **22**) through the enabled drive Y-coordinate driver gate Z12A-Z12G.

The X and Y coordinate output lines may be connected to matrix **30** such as that shown in my previous U.S. Pat No. 3,507,376. This is schematically shown in FIG. **2.** Thus, a dual-sequential input is converted to a dual-concurrent output. Alternatively, as seen in FIG. **3,** outputs **8'** and **23'** may be connected to a code converter, such as an ASCII code converter, and a solenoid driver—or some other logic conversion system—to operate a typewriter, such as the IBM "SELECTRIC" brand typewriter.

Upon release of the second switch of the sequentially operated pair, the transition of the output from CIBC to its static state is differentiated by the network **21** at the input of logic element Z10C. The other terminal of Z10C is connected to the output of control binary **29B** via line **34** through an inverter Z13A. The pulse output from Z10C is connected to one of the terminals of logic OR element Z11C. The output from Z11C resets the first switch memory binaries Z1B–Z7B. With the first binaries reset, Z8 reverts to its initial static state, and the "first-bit" light **12** is extinguished. Also, the static state of Z8 through line **26** is used to reset the control binary Z9B. Thus, the controller is ready to accept another dual sequential input.

Also, the binaries Z1B–Z7B, and thus the control binary Z9B, are intially reset when the device is turned "on" through element Z11C via line **28.** This is accomplished from the +5 volt potential which is delayed through the charging action of C1.

Also, the first switch memory binaries can be reset through Z11C upon actuation of SW8 in the event the operator recognizes that his first input switch selection was an error.

OPERATION OF THE INVENTION

For ease in explanation it is assumed that the operator presses switch SW1 for his first sequential pair energization, which will provide the X-coordinate, and then also presses SW1 to provide the Y-coordinate. The present system operates in real-time, and features direct memory access.

When the device is turned "on" the binaries Z1B–Z7B are initially reset through element Z11C. The closing of switch SW1 will feed the signal into input buffer circuit IBC1 over line **1–1.** The output from input buffer circuit IBC1 will go over the line **3–1** into the X-coordinate drive input gate Z1A at its first terminal. The signal will also appear on the common input buffer circuit CIBC over line **2–1** through D1.

Now assuming that the drive gate Z1A is enabled by the signal coming over line **4,** the signal from SW1 will be impressed upon the first switch memory binary Z1B. The signal will be generated over line **5–1** to logic element Z8 which will change its state the instant the bit of information is loaded into memory binary Z1B.

The output from Z8 over line **26** through element Z9D will then gate "off" the various elements Z1A–Z7A. The Z8 output, which, is also connected to the lamp driver **10,** will illuminate the "first bit" indicator **12** to advise the operator that the X-coordinate has been established.

The establishment of the X-coordinate is accomplished by the transmission of a signal over line **6–1** (also labeled A') to the X-coordinate output drive circuit **7** and then on to the X-coordinate output line **8.**

Upon release of the switch SW1 an output signal from the common input buffer circuit CIBC places an input signal over line **14** to one terminal of the logic element Z9A. The other terminal of element Z9A is energized via line **16** from logic element Z8. Therefore, when the switch is released there will be outputs over lines **14** and **16,** thus gating logic element Z9A "on." Because of the timing relationship between the output of ICB1 and CIBC, the switching "on" of Z9A is assured of occuring after ICB1. This in turn will latch the control binary Z9B. Since the output of control binary Z9B is connected to one of the terminals of logic elements Z12A–Z12G, one terminal will be gated "on" for each of the elements which are the Y-coordinate drive gates. When the switch is depressed for the second time (again assuming it is the switch SW1), the signal will follow over lines **1–1** to the input buffer circuit IBC1 and line **3–1** to line **20** (also labeled A). Since the Y-coordinate drive gates have been enabled via line **18,** the output from line **20** will thus gate on the logic element Z12A. This in turn will energize the Y-coordinate driver circuit **22** and provide an output on the Y-coordinate output line **23.**

Now upon release of the second switch the reversion to the initial static state of the output over line **14** from the common input buffer circuit CIBC will be differentiated by element **21** and energize logic gate Z10C, which has been enabled by the control binary Z9B. This signal is utilized to clear the memory binaries Z1B–Z7B through logic element Z11C, which will output a reset signal to the memory binaries over line **28.**

With the first switch binaries reset, Z8 reverts to its initial static state, and the "first bit" light **12** is extinguished. Also, the static state of Z8 through line Z6 is used to reset the control binary Z9B.

Reset switch SW8 can also be used in conjunction with logic element Z11C to reset the first switch memory binaries Z1B–Z7B when an error is made in actuation of the first switch.

The output from X- and Y-coordinate lines **8** and **23** are connected to matrix **30** or code converter **32** for

energization of the approximate letter on a typewriter, for example.

The hard wire control system of invention is thus seen to utilize direct access to the memory, and to operate in real-time. It is to be understood that the number of input switches can be varied in the system, according to a formula whereby the number of resultant signals is equal to S^n, wherein S is the number of input switches and n is the number of successive sequential actuations.

While a specific form of the invention has been described herein, it is to be understood that the same is merely illustrative of the principles involved and that other forms may be resorted to within the scope of the appended claims.

I claim:

1. In a hard wire direct access control operating in real time:

a. a single set of at least two input switching means;

b. logic means for providing single X and Y outputs registering successive, sequential actuations of said single set of switching means, said logic means including means for first storing a signal commensurate with a first actuation, and means for generating a Y output signal commensurate with a second actuation together with an X output signal commensurate with the first stored signal only after initiating the second actuation; and

c. utilization means connected to said outputs for providing a single resultant indication representative of the combination of the successive actuations of said switching means in real time.

2. In a control as defined in claim **1,** wherein said utilization means is a typewriter.

3. In a control as defined by claim **1,** wherein the number of resultant indications is equal to S^n, wherein S is the number of input switching means and n is the number of successive sequential actuations.

4 In a control as defined in claim **3,** including means for resetting said logic means prior to the nth switch actuation whereby no output will occur until said switching means receives n switch actuations.

5. In a control as defined in claim **1,** in means for indicating the occurrence of a first switch actuation.

6. In a control as defined in claim **1** including:

a. an input buffer circuit connected to each of said switching means;

b. an X-coordinate input drive gate connected to each of said input buffer circuits;

c. a first switch memory connected to each of said X-coordinate input gates;

d. an X-coordinate output drive circuit connected to each of said first switch memory;

e. a utilization circuit having X and Y inputs thereto;

f. an X-coordinate output line for each of said X-coordinate output drive circuits connected to an X input of said utilization circuit;

g. a Y-coordinate input drive gate also connected to each of said input buffer circuits;

h. a Y-coordinate output drive circuit connected to each of said Y-coordinate input drive gates;

i. a Y-coordinate output line for each of said Y-coordinate output drive circuits connected to a Y input of said utilization circuit;

j. means for enabling said X-coordinate drive gate for passing therethrough a first switch actuation signal, and means for disabling said X-coordinate drive gate after said first switch actuation is stored in said first switch memory; and

k. means for disabling said Y-coordinate drive gate during said first switch actuation and means for enabling said Y-coordinate drive gate after said first switch actuation.

7. In a control as defined in claim **1,** wherein there are seven input switching means.

* * * * *