

[54] **SOLID STATE, CONTROLLABLE
ELECTRIC SWITCH**

3,543,103 11/1970 Pinckaers..... 317/155.5

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[57] **ABSTRACT**

[21] Appl. No.: **423,229**

An electrical switch which can be remotely conditioned to an ON or OFF state by the use of solid state circuitry, but which can also be controlled at the switch location, if desired. The conditioning of the switch is controlled by means of a solid state monostable multivibrator, a bistable electromechanical relay, and a pair of silicon controlled rectifiers.

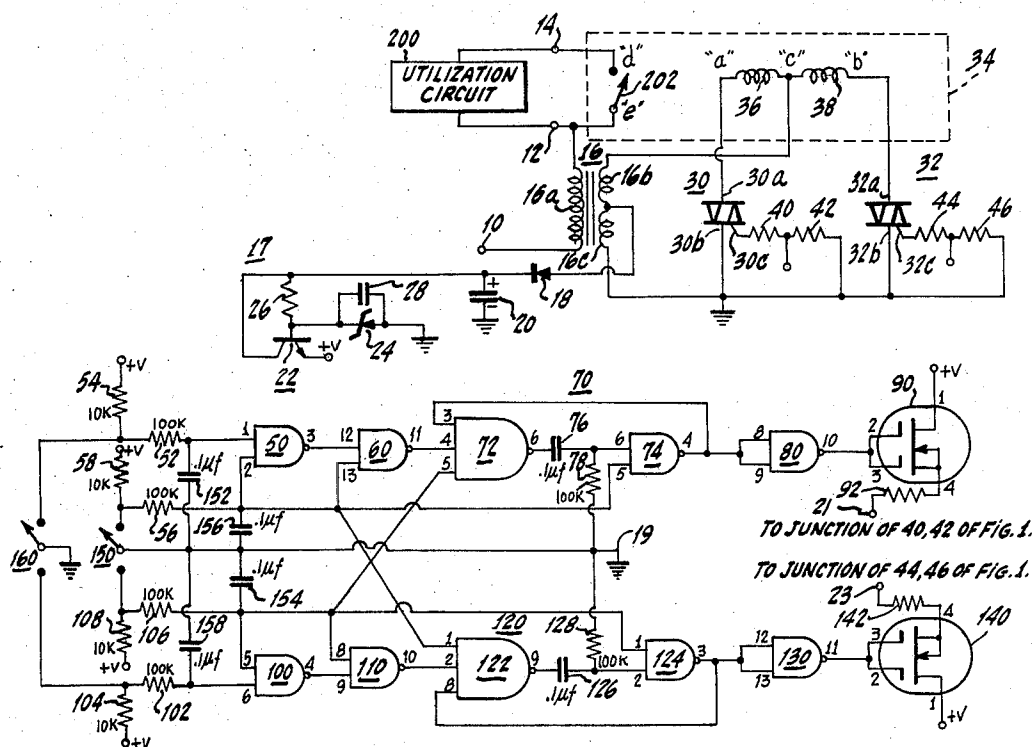
[52] U.S. Cl. 317/155.5, 317/148.5 B
[51] Int. Cl. H01h 47/32
[58] Field of Search..... 317/155.5, 148.5

[56] **References Cited**

UNITED STATES PATENTS

3,349,373 10/1967 Kleist et al. 317/155.5

7 Claims, 2 Drawing Figures



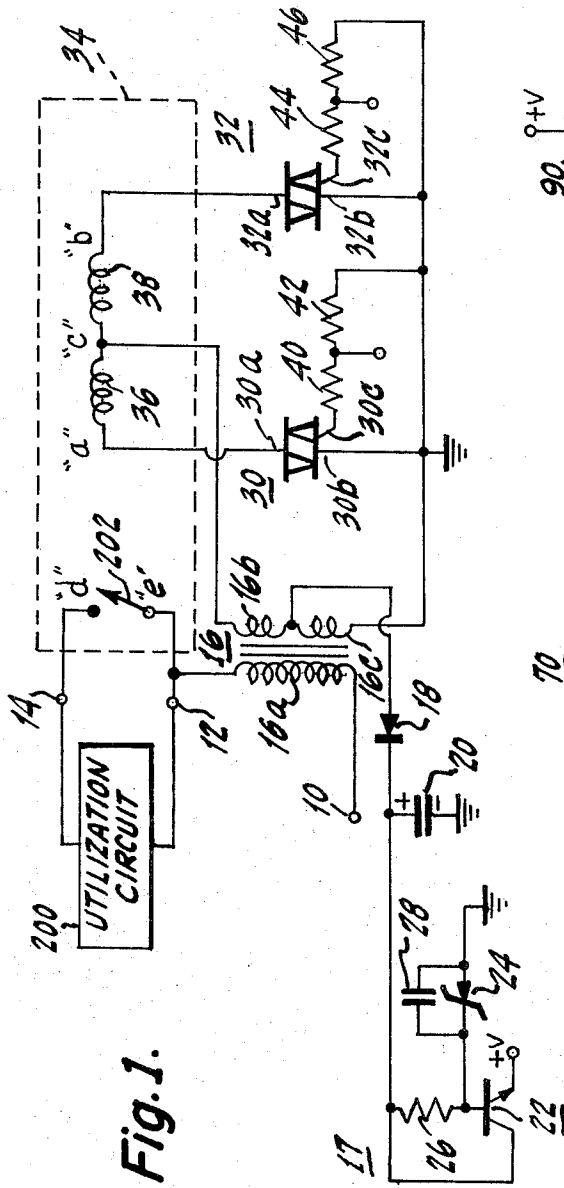


Fig. 1.

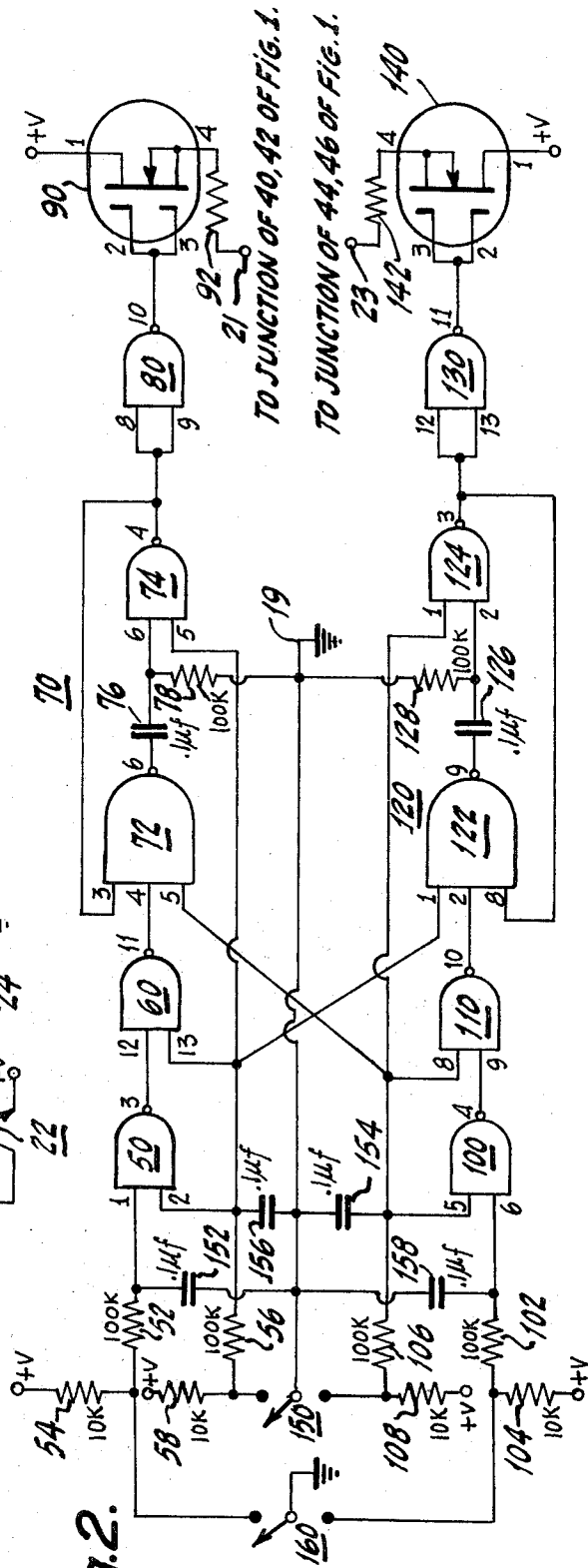


Fig. 2.

TO JUNCTION OF 40, 42 OF FIG. 1.

TO JUNCTION OF 44, 46 OF FIG. 1.

SOLID STATE, CONTROLLABLE ELECTRIC SWITCH

FIELD OF THE INVENTION

This invention relates to electrical make and break switches, in general, and to such switches which can be remotely conditioned to an ON or OFF state for office buildings, schools, and manufacturing facilities where computer control of light switches, for example, is employed as a means to reduce costs of electricity.

SUMMARY OF THE INVENTION

As will become clear hereinafter, the construction of the present invention is similar to that described in pending United States Patent Application Ser. No. 390,532, now U.S. Pat. No. 3,829,683, assigned to the same assignee as is this invention, in its use of a bistable electromechanical relay and a pair of silicon controlled rectifiers to provide local and remote controls in energizing and deenergizing electrical devices. As with the constructions there described, the embodiments of this invention are designed to interface with computer, low voltage systems, so that the switches of the invention can be connected to the computer control center by low voltage, low current carrying conductors.

The arrangements described below are thus also especially attractive for use where the switches are employed in the control of lighting in office buildings, schools, and manufacturing plants, for example. Computer control signals could be coupled, as with the configurations of U.S. Pat. No. 3,829,683 to turn "off" all lights in a particular part of the facility automatically after the work day has ended. Correspondingly, control signals can be sent to those switches at the beginning of the work day, to automatically turn all lights "on." In those installations where personnel periodically make security checks, the computer can transmit control signals to turn the lights "on" just before the guard makes his rounds, and to turn them "off" after they are completed. Conversely, all lights in a different part of a facility can be controlled to their temporary ON condition at the end of a work day, to be later turned "off" by a person working in that area at that time. Similarly, the computer control signal can be such as to place all lights in their temporary OFF mode just before the work day begins, to be individually turned "on" by employees as they appear for work.

As will be seen below, the methods of optical multiplexing with light sensitive photocells, as were used in the U.S. Pat. No. 3,829,683, are omitted from the switch constructions of the present invention. In particular, solid state circuitry in the form of gates, inverters and monostable multivibrators are employed in place of the illuminating lamps and photocell devices therein employed, in providing a package which, with available integrated circuit techniques, is more economical in cost and more compact in size. With the high reliability inherent with an integrated device, moreover, the switch of the invention should have a longer operating life, and make necessary servicing cheaper in the replacement of less expensive integrated circuits for more costly illuminating lamps and photocells.

BRIEF DESCRIPTION OF THE DRAWING

These and other features of the present invention will be more readily understood from a consideration of the following description taken in connection with the accompanying drawing in which:

FIG. 1 is a schematic diagram of a portion of the electrical switch embodying the invention, showing the bistable electromechanical relay and silicon controlled rectifiers employed; and

FIG. 2 is a schematic diagram of the solid state circuitry employed to control the switch functions both from local and remote locations.

DETAILED DESCRIPTION OF THE DRAWING

In FIG. 1, three terminals 10, 12, and 14 are shown. Terminal 10 serves as a ground or reference terminal while terminal 12 serves to supply the operating voltage for the system. Such voltage as is supplied between terminals 10, 12 may be of the order of 120 volts alternating line voltage, but in a specific embodiment of the invention was of 277 volts rms magnitude as that represents the lateral voltage which is oftentimes employed in large office buildings in order to save copper costs. The primary winding 16a of a transformer 16 is coupled between terminals 10 and 12, while a pair of secondary windings 16b, 16c are serially coupled to step this 277 volts down to an amplitude suitable for powering the circuits of the construction.

A regulated power supply circuit 17 is included, having a transistor 22 and a zener diode 24 to develop an operating potential for the solid state circuitry illustrated in FIG. 2. The collector electrode of the transistor 22 is shown connected to the cathode electrode of a semiconductor rectifier 18, while the base electrode of that transistor is coupled first, by a resistor 26 to that electrode and second, to the cathode electrode of the zener 24. The anode electrode of the zener diode 24 is connected to a point of reference or ground potential, and a capacitor 28 is connected in parallel across the zener element. With an electrolytic capacitor 20 being coupled between the cathode electrode of diode 18 and ground, the component values and the turns ratios for the transformer 16 are selected so that a direct potential of substantially +15 volts is developed at the emitter electrode of transistor 22. This potential is illustrated in the drawing by the reference notation +V and is applied at the six indicated points in FIG. 2.

A pair of silicon controlled rectifiers 30, 32 and a bistable electromechanical relay 34 are also shown. As indicated, one power electrode 30a of rectifier 30 is connected to one end a of a relay coil 36 in the bistable unit 30, while a second power electrode 30b of rectifier 30 is coupled to the reference potential point. In corresponding manner, one power electrode 32a of rectifier 32 is coupled to one end b of a second relay coil 38 in the bistable unit 34 while a second power electrode 32b of rectifier 32 is coupled to the ground point. The opposite end of the relay coil 36 and the opposite end of the relay coil 38 are joined together at c, to which point is coupled the terminal of the transformer winding 16b which is remote from the winding 16c. As will be understood, current flowing through the relay coil 36 constitutes the "make" condition for the electrical switch, in which case a closed circuit path will exist between the supply terminal 12 and the third terminal of the drawing 14, between which terminals a utilization cir-

cuit 200 is connected. It will also be understood that current flowing through the relay coil 38 will "break" the switch connection, and open the circuit path between the terminals 12 and 14. The switch connection is particularly illustrated by the contact arm 202, joining points *d* and *e* of the relay 34 when closed.

Four resistors 40, 42, 44, and 46 are also shown. The resistors 40, 42 are serially connected between the gate electrode 30c of the rectifier 30 and the ground potential point. Similarly, the resistors 44, 46 are serially connected between the gate electrode 32c of the rectifier 32 and ground. Control signals, when applied at the junction of resistors 40, 42 energize the silicon device 30 to produce a resulting current flow through the relay coil 36 — the current path comprising the two secondary windings 16b, 16c, the relay coil 36 and the rectifier 30. Control signals applied to the junction of resistors 44, 46, on the other hand, energize the silicon device 32, producing a resulting current flow through the relay coil 38 — the current path this time comprising the two secondary windings 16b, 16c, the relay coil 38 and the rectifier 32.

With this arrangement, a current flow through the relay coil 36 energizes the electromechanical switch contact arm 202 to connect the load 200 between the terminals 12 and 14 while a current flow through the relay coil 38 de-energizes that contact arm and disconnects the load 200 from between those two terminals. With an RR7 type relay, as manufactured by the General Electric Company, only a momentary application of a control signal to the junction of resistors 40, 42 is needed as the electromechanical relay 34 is bistable in its operation and will maintain contact arm 202 closed even though the control signal is removed from that resistor junction. With an RR8 type relay, also manufactured by the General Electric Company, a second contact arm (not shown) will be energized when a current flows through the relay coil 38, for use in providing a remote indication of the state of the relay 34. Such an added feature is more particularly described in the U.S. Pat. No. 3,829,683, the description of which is herein incorporated by reference thereto.

Considering, now, the solid state circuitry of FIG. 2, it will first be appreciated that the upper and lower half portions, centered around the ground bus 19, are substantially identical. It will also be appreciated that the output terminal 21 of the upper half portion is to be coupled to the junction of resistors 40, 42 of FIG. 1, to control the switch to its "make" condition. It will likewise be appreciated that the output terminal 23 of the lower half portion is to be coupled to the junction of resistors 44, 46 of FIG. 1, to control the switch to its "break" condition. A pair of single pole, double throw switches 150, 160 are additionally shown, with the switch 150 being understood as being controllable by the computer at the remote location and with the switch 160 being controllable by the user at the local station. Before describing the construction of these two half portions, it should be noted and understood that throwing the switch 150 to its upper-most position will remotely place the switch of FIG. 1 in its "permanent OFF" state, while throwing the switch 150 to its lower-most position remotely places the switch of FIG. 1 in its "permanent ON" state, independent of the positioning of the switch 160. It will also be understood that with the switch 150 open-circuited, throwing the switch 160 to its upper-most position places the switch of FIG.

1 in its "temporary ON" state, while throwing switch 160 to its lower-most position places the switch of FIG. 1 in its "temporary OFF" state.

To be more specific, each half of the FIG. 2 configuration includes a pair of two input NAND gates, a monostable multivibrator, an inverter, and a field effect transistor amplifier. The first NAND gate 50 has its input terminal 1 coupled by a pair of resistors 52, 54 to the +V potential developed by transistor 22 in FIG. 1, and has its input terminal 2 similarly coupled to receive that voltage by a second pair of resistors 56, 58. The second NAND gate 60 has one input terminal 12 connected to the output terminal 3 of NAND gate 50 and a second input terminal 13 connected to terminal 2 of the NAND gate 50. The monostable multivibrator 70, in actuality, comprises a three-input NAND gate 72 and a two-input NAND gate 74 arranged in appropriate combination, with one input terminal 3 of NAND gate 72 connected to the output terminal 4 of NAND gate 74. A second input terminal 4 of NAND gate 72 is connected to the output terminal 11 of NAND 60, with its own output terminal 6 being coupled in turn first, by a capacitor 76 to an input terminal 6 of NAND 74 and second, by that capacitor 76 and a resistor 78 in series to the ground bus 19. The input terminal 5 of NAND gate 72 is coupled via a third pair of resistors 106 and 108 to the +V supply terminal while the input terminal 5 of NAND gate 74 is connected to input terminal 2 of NAND gate 50.

The upper half portion of the solid state circuitry of FIG. 2 is completed by utilizing a fourth, two input NAND gate 80, arranged as an inverter by connecting both its input terminals 8 and 9 to the output terminal 4 of NAND 74 and by connecting its output terminal 10, in turn, to the field effect transistor amplifier 90. Such unit is shown as being of dual gate construction, in which the input gate terminals 2 and 3 are connected together, the drain electrode is coupled to the +V operating voltage, and the source and substrate electrodes are connected together, and coupled by means of a resistor 92 to the output terminal 21. As indicated, the drain electrode is represented by the terminal reference notation "1," while the source electrode is represented by the terminal notation "4."

Corresponding components in the lower half portion of the solid state circuitry of FIG. 2 are represented by corresponding reference notations, except higher by "50." In these respects, it will be appreciated that NAND gates 50, 60, 100 and 110 may comprise the four dual input NAND circuits found on a type 4011 integrated circuit manufactured by the Solid State Division of the RCA Corporation. The NAND gates 74, 80, 124 and 130 also may comprise the four circuits of such an integrated device, while the two three-input NAND gates 72, 122 may be from a type 4023 integrated circuit also manufactured by the RCA Corporation's Solid State Division. The dual gate field effect transistor amplifiers 90, 140 may be of the type found on a 40841 integrated chip, with all the input and output terminals indicated corresponding to terminal notations as present on the integrated circuit fabrications of those devices. Except for the two switches 150 and 160 previously noted, the solid state circuitry of FIG. 2 is completed by coupling individual capacitors 152, 154, 156, and 158 between the ground bus 19 and the four input terminals of the NAND gates 50 and 100.

In considering the operation of the switch construction of FIGS. 1 and 2, it will first be appreciated that the NAND gates 50, 60, 100 and 110 develop an output voltage, digitally construed as "low" only when all input voltages are digitally "high" and develop an output which is of digitally "high" potential when either or both inputs are of "low" potential. It will also be appreciated that the monostable multivibrators 70, 120 are triggerable only when a digital "high" potential is applied to terminal 5 of the NAND gate 74, in the first case, or to the input terminal 1 of the NAND gate 124, in the second case.

With the computer priority switch 150 in its "open-circuit" position, i.e., not remotely controlled, moving the user switch 160 to its upper-most position places a digitally "low" voltage on input terminal 1 of NAND 50 while a digitally "high" voltage is applied at terminal 2 of NAND 50, terminal 13 of NAND 60 and terminal 5 of NAND 74. The digitally "low" voltage developed at output terminal 3 of NAND 50 cooperates with the digitally "high" voltage on terminal 13 of NAND 60 to provide a digitally "low" potential at terminal 11 of NAND 60. The resulting digitally "low" potential at terminal 4 of NAND 72 cooperates, on the other hand, with the digitally "high" potential applied to terminal 5 of NAND 72 to trigger the monostable multivibrator 70 and develop, in this case, a one half second pulse at the output terminal 4 of NAND 74. After inversion by the stage 80, this pulse drives the amplifier 90 to provide an output pulse at terminal 21 to fire the gate 30c of rectifier 30 and provide a current through relay coil 36 to close the contact arm 202 and place the utilization circuit 200 between the terminals 12 and 14. If switch 160 were moved to its lower-most position, on the other hand, a digitally "low" potential would be placed on input terminal 6 of NAND 100, to cooperate with the digitally "high" potential at its input terminal 5 to develop a digitally "low" voltage at terminal 4 of NAND 100. This potential will be seen to cooperate with the digitally "high" potential applied to terminal 8 of NAND 110 to provide a digitally "low" voltage at output terminal 10 of NAND 110. With a digitally "high" potential applied at terminal 1 of NAND 122, this digitally "low" voltage developed by NAND 110 will be seen to trigger the monostable multivibrator 120 to provide a one half second pulse at output terminal 3 of NAND 124. This pulse is inverted by the stage 130 to drive the field effect transistor amplifier 140 to provide an output pulse at terminal 23, which is coupled to drive the silicon controlled rectifier 32. The resulting current flow through relay coil 38 thus becomes sufficient to disconnect the contact arm 202 and uncouple the utilization circuit from between the terminals 12 and 14.

In other words, alternatively adjusting the single pole, double throw switch 160 upwards and downwards, as shown in the drawing, operates as the local, user control for closing the contact 202 and for opening this contact, respectively. Because the relay unit 34 is a bistable device, this single pole, double throw switch need operate only momentarily to insure the correct state of the electromechanical switch. Similar analysis of the construction of FIG. 2 will show that an output pulse will be developed at the terminal 23 of the field effect amplifier 140 when the priority control switch 150, only, is moved to its upper most position. Conversely, an output pulse will be developed at terminal 21 of the

field effect transistor amplifier 90 when the remote control switch 150 is moved to its lower most position. Such development of output pulses will be seen to occur in this latter manner for those cases where the customer control switch 160 is unconnected, with the output pulse being developed at output terminal 23 arising as well for the case where the remote control switch 150 is actuated upward after the customer control switch 160 was moved to its upper-most position. Correspondingly, the output pulse will be developed at terminal 21 when the remote control switch 150 is moved to its lower-most position after the customer control switch 160 is placed in its lower-most condition.

As was previously mentioned, the priority switch 150 is intended for computer control such that when it is thrown to either of its two possible positions, subsequent attempts by the local user to "make" or "break" the switch condition will be ineffective. In this event, the condition of the controllable switch will be regulated at the remote location, and thereafter immunized from local user control. For example, consider the case where the switch 150 is moved to its upper-most position in order to develop an output pulse at terminal 23, in the direction to disconnect the contact arm 202 and the utilization circuit 200 from between the terminals 12 and 14. Assume further that the customer, or local user, then seeks to energize that utilization circuit 200 by throwing the switch 160 to its upper-most position. It will readily be seen that the placing of switch 150 in its up most condition places a digital "low" voltage at terminal 5 of NAND circuit 74, to prevent any output pulse from being developed at terminal 4 of NAND 74. Thus, moving the switch 160 upwards at the local station has no effect. On the other hand, if the switch 150 is thrown to its lower-most position, to develop an output pulse at the amplifier terminal 21 so as to fire the control rectifier 30 to cause a current to flow through relay coil 36, thereby closing the contact arm 202 and connecting the utilization circuit between the terminals 12 and 14, movement of the local control switch 160 to its lower most condition similarly has no effect as a digitally "low" potential is provided at input terminal 1 of NAND 124. Any tendency for the throwing of switch 160 to provide a pulse output to the inverter 130 is thus offset by the digital conditioning of NAND 124 to prevent this switch-over from occurring. In other words, throwing switch 150 will be seen to take priority in circuit operation over any attempted changes made by the throwing of switch 160. Once the control by switch 150 is removed, it will be seen that local user control can once again be made to provide an output pulse at output terminal 21, or 23, as the case may be, to either place the utilization circuit 200 into operation or remove it from the energized terminal.

Such control operations will be readily apparent to those skilled in the art as being particularly desirable in controlling office lighting, as previously mentioned. Thus, at the end of the work day, the switch 150 can be computer regulated to its upper-most position to permanently turn "off" all lighting in a specified portion of a facility. If security checks are then to be made, the switch 150 can be placed to its lower-most position and all lighting will then be illuminating. After the guard completes his rounds, the switch 150 can be moved to its disconnect position, thereby removing all priority control over the office lighting. At the begin-

ning of the work day, workers can individually illuminate their work area as they come on the job, by throwing the switch 160 to its up-most position. At the end of a work day, they can individually turn off the lighting in their area, by throwing the switch 160 to the lower-most position, prior to the computer being activated to throw switch 150 to its upper most position, thereby assuring "turn-off" of all lighting. It will be readily understandable and appreciated that this manner of electricity control can serve to greatly lessen electricity costs in factories, office buildings, schools and the like.

While there have been described what are considered to be preferred embodiments of the present invention, it will be apparent to those skilled in the art that other bistable switch configurations can be devised without departing from the scope of the teachings herein of utilizing both remote control and local switching in making and breaking electrical connections through the use of solid state digital circuitry. It will also be apparent that the digital blocks of the type referred to are available as integrated circuit, and are thus simple to package and economical in costs. In the constructions described in the U.S. Patent No. 3,829,683, on the other hand, each of the illuminating lamps and photocell devices employed require both additional space for their employment and added expense for their constructions. With the present configurations, on the other hand, readily available building blocks can be utilized, without the criticality of design which might be required in offsetting the variations with age of the photosensitivity characteristics of the photocells employed, and assuring that illumination from any one lamp is constrained so as to only illuminate its associated photocell.

What is claimed is:

1. A controllable electrical switch comprising;
first and second terminals; and

actuating means for making electrical connection between said terminals when closing said switch and for breaking said electrical connection when opening said switch;

said actuating means including:

- a. a bistable electromechanical relay having an input electrode coupled to said first terminal and an output electrode coupled to said second terminal and conditionable to one of a low and high impedance state between its input and output electrodes as a function of current flow therein;
- b. a pair of semiconductor control devices, each having an input circuit and each having an output circuit respectively coupled to said electromechanical relay such that a conductivity condition in one of said devices produces a current flow in said relay as to place it in its low impedance state and such that a conductivity condition in the other of said devices produces a current flow in said relay as to place it in its high impedance state; and
- c. solid state control means for signal pulsing the input circuits of said semiconductor control devices to change the conductivities thereof, with said changes in conductivity conditions serving to change the current flow through the output circuits of said control devices to change the impedance state of said bistable relay in actuating said electrical switch from a make to a break condition and vice versa;

said solid state control means including a pair of pulse triggering circuits, one of which is controllable to first voltage condition for enabling the development of said signal pulses to change the conductivity of said one semiconductor device and controllable to a second voltage condition for inhibiting the development of said signal pulses therefor, and the other of which is controllable to said first voltage condition for enabling the development of said signal pulses to change the conductivity of said other semiconductor device and controllable to said second voltage condition for inhibiting the development of said signal pulses for said other device, and with only one of said pulse triggering circuits being controllable to said first voltage condition at any given instant of time.

2. The controllable switch of claim 1 wherein each of said pulse triggering circuits includes a monostable multivibrator having an input terminal controllable to a first voltage condition to enable the development of said signal pulses to change the conductivities of said semiconductor devices and controllable to a second voltage condition to inhibit the development of said signal pulses to change the conductivities of said semiconductor devices.

3. The controllable switch of claim 2 wherein said solid state control means also includes a pair of actuatable switches, one of which is actuatable to a first position to control one of said multivibrators to enable the development of said signal pulses to change the conductivity of said one semiconductor device and actuatable to a second position to control the other of said multivibrators to enable the development of said signal pulses to change the conductivity of said other semiconductor device.

4. The controllable switch of claim 3 wherein the other of said pair of actuatable switches is actuatable to a first position to control said other of said multivibrators to enable the development of said signal pulses to change the conductivity of said other semiconductor device and actuatable to a second position to control said one multivibrator to enable the development of said signal pulses to change the conductivity of said one semiconductor device, irrespective of the actuation of said one of said pair of actuatable switches.

5. The controllable switch of claim 3 wherein said one of said pair of actuatable switches is actuatable to provide signal pulses to change the conductivities of said semiconductor devices substantially only when said other actuatable switch is in a third, open-circuit position.

6. The controllable switch of claim 5 wherein said bistable electromechanical relay includes a first relay coil responsive to current flow through the output circuit of said one semiconductor control device to place said relay in its low impedance state and a second relay coil responsive to current flow through the output circuit of said other semiconductor control device to place said relay in its high impedance state.

7. The controllable switch of claim 6 wherein there is also included means responsive to the current flow in said second relay coil to provide an indication of the impedance state of said bistable electromechanical relay and the conditioning of said electrical switch to make and break electrical connections.

* * * * *

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,869,651 Dated March 4, 1975

Inventor(s) Donald C. Long, et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 1, Line 50	"eht" should read -- the --
Column 3, Line 40	"the" should be deleted
Column 7, Line 21	"constructions" should be inserted after "circuit" and before the comma (,)
Column 7, Line 22	"constructions" should be deleted (one occurrence)
Column 7, Line 23	"the" should be deleted

Signed and sealed this 6th day of May 1975.

(SEAL)
Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents
and Trademarks

UNITED STATES PATENT OFFICE
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