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Helbig et al.

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[54] BOWLING SPLIT DETECTOR

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[52] **U.S. Cl.** .....**273/54 C**, 273/54 E, 340/323

[51] **Int. Cl.** **A63d 5/04**

[58] **Field of Search** .....273/54 C, 54 D, 54, 54 E; 235/92 GA; 340/323

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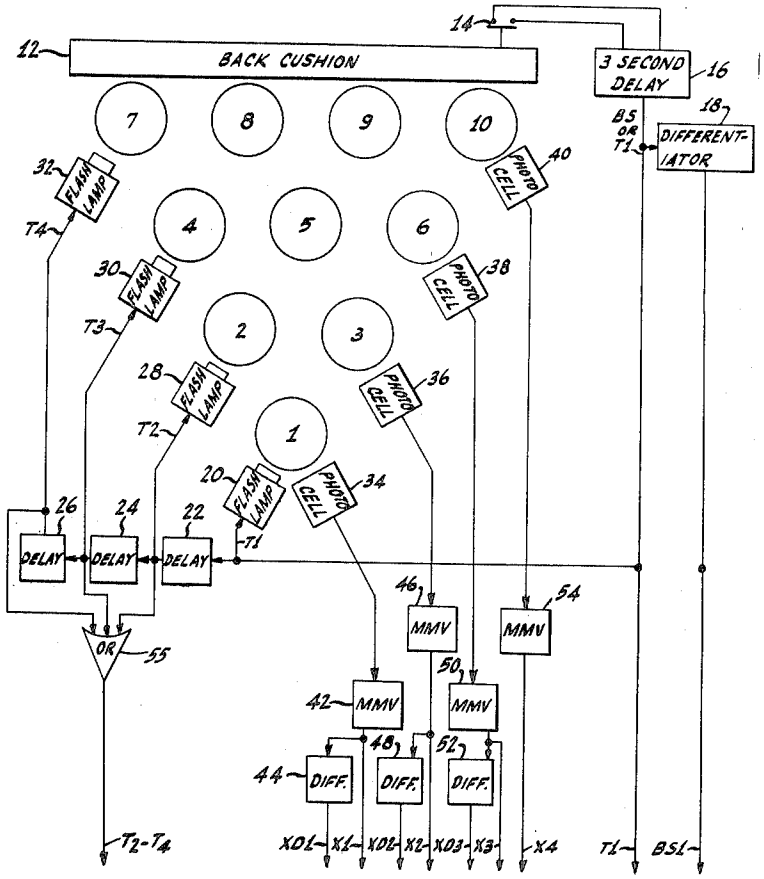
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[57] **ABSTRACT**

A bowling "split" indicator in which signals are provided to indicate which pins are still standing after the first ball is rolled, and in which means are provided to determine whether the formation of the standing pins comprises a split, and to indicate the appearance of a split, and to disable the indicator if the headpin is still standing.

7 Claims, 3 Drawing Figures



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SHEET 1 OF 3

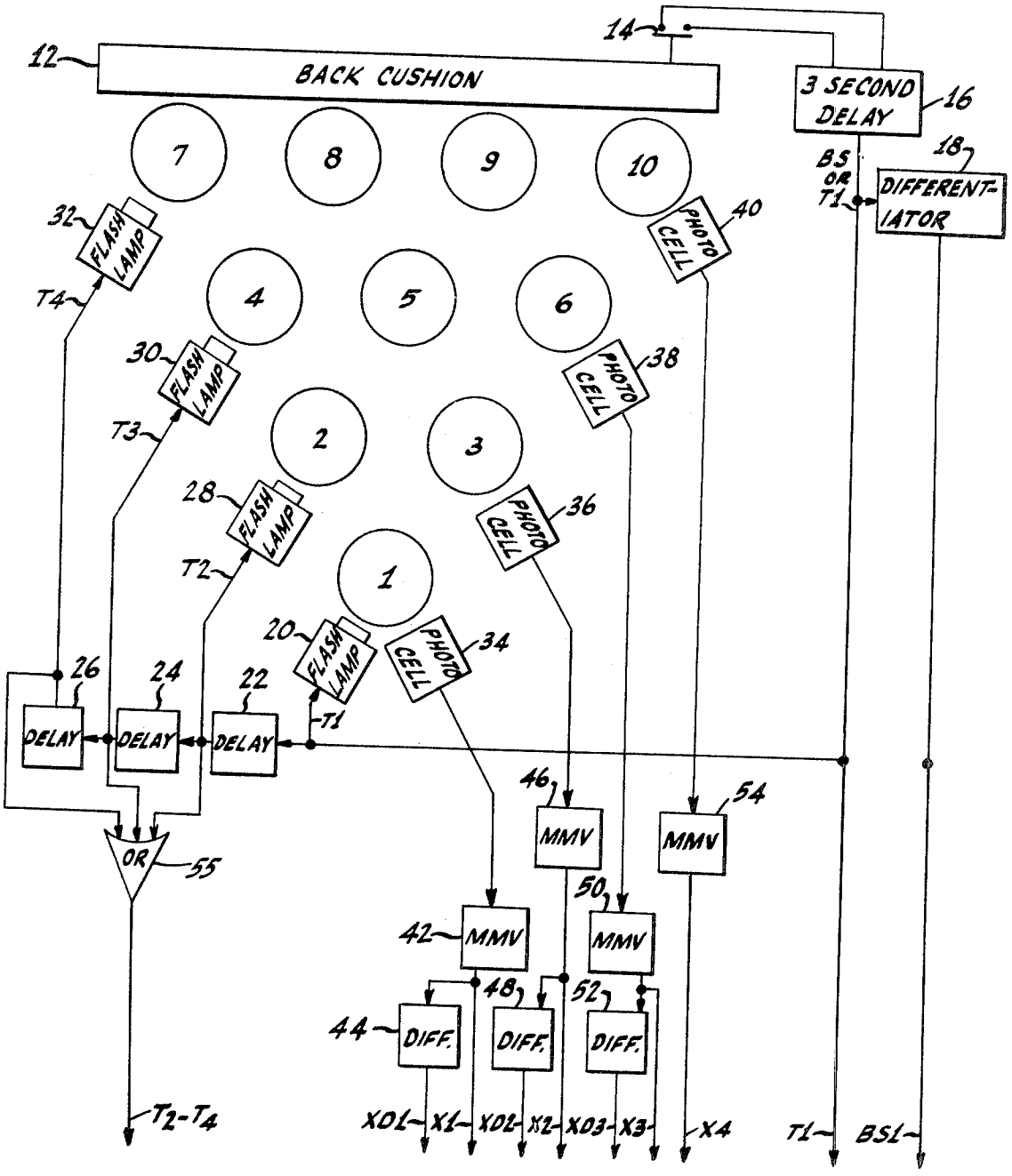


Fig. 1A.

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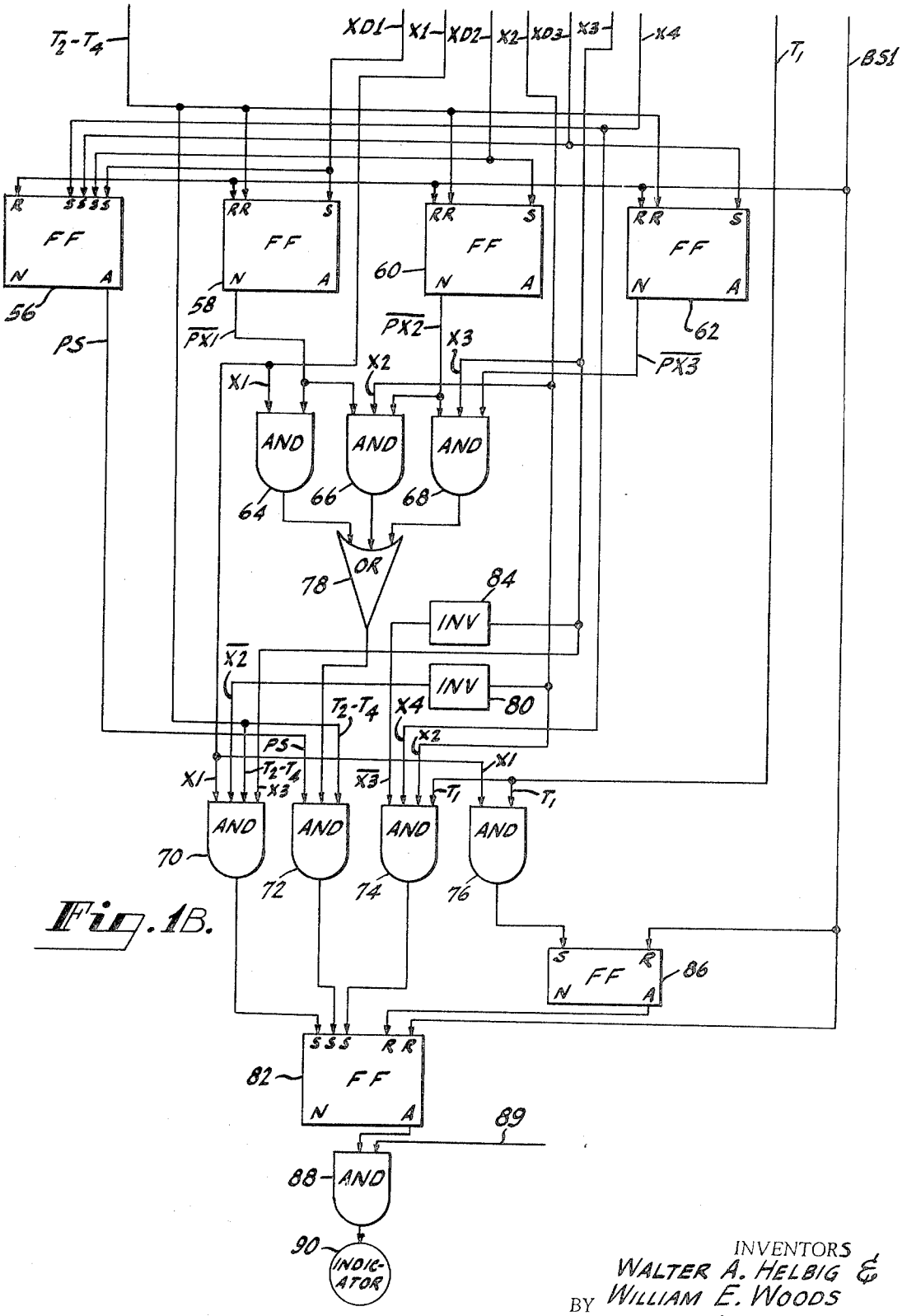


Fig. 1B.

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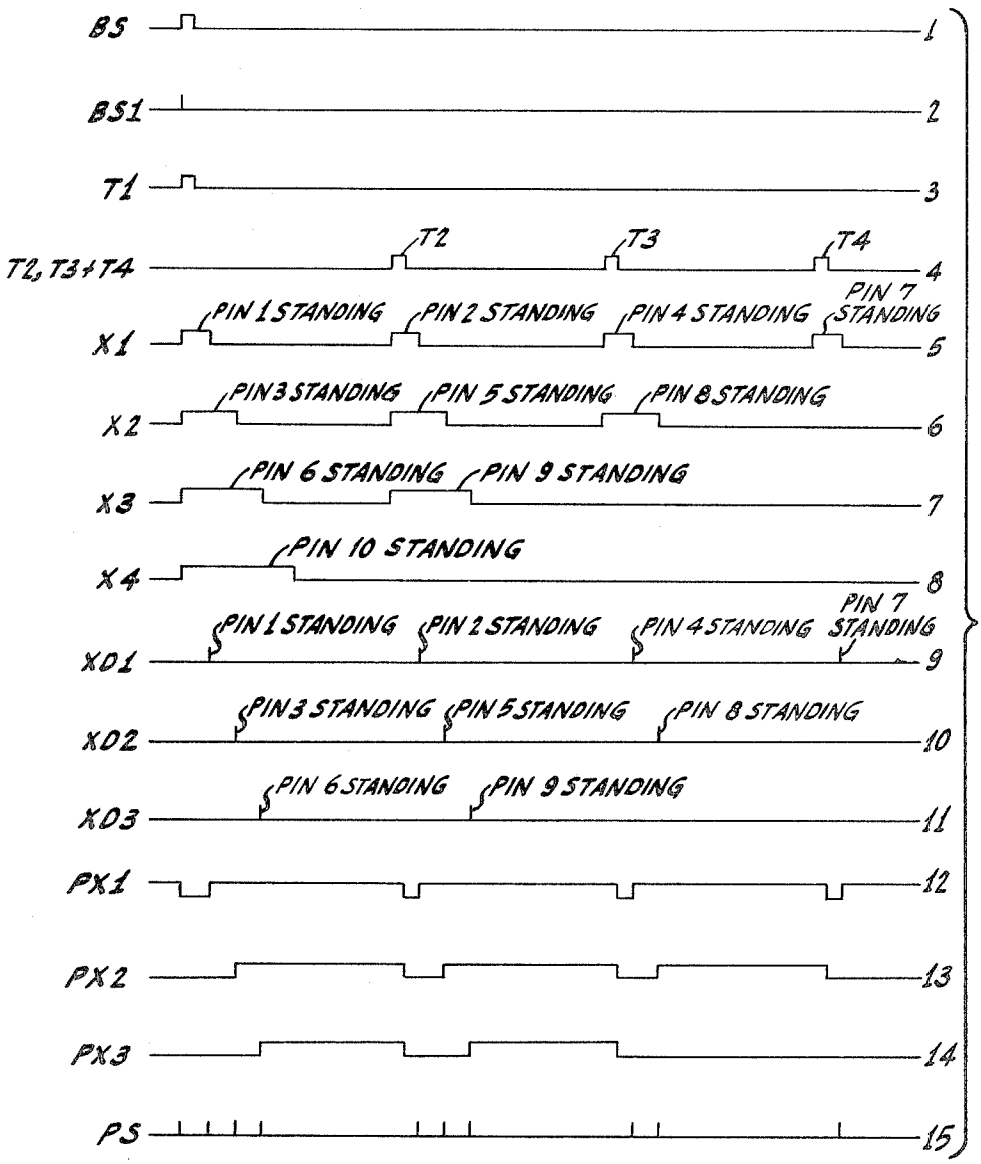


Fig. 2.

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BOWLING SPLIT DETECTOR

This invention relates to an improved apparatus for detecting splits in bowling.

The pins that remain standing, if any, after legal delivery of the first ball in each frame of a bowling game, consisting of 10 frames, may present one of a number of formations known as a split. These formations, as defined by Rule No. 7 of the American Bowling Congress are as follows:

A split shall be a setup of pins remaining standing after the first ball has been legally delivered provided the headpin is down, and

1. At least one pin is down between two or more pins which remain standing, as for example: 7–9, or 3–10.

2. At least one pin is down immediately ahead of two or more pins which remain standing, as for example: 5–6.

In scoring a bowling game, a split may be indicated by a circle on the score pad at the positions where the number of pins knocked down by the first ball of each frame is entered. In a complete bowling scoring apparatus, means must be provided to indicate the occurrence of a split.

It is an object of this invention to provide an apparatus for indicating in bowling scoring the occurrence of a split.

It is another object of this invention to provide apparatus having a minimum number of parts and including electronic logic elements for indicating a split in scoring a bowling game.

It is still a further object of this invention to provide an apparatus consisting substantially only of solid-state electronic devices for indicating a bowling split.

Yet another object of this invention is to provide a split indicator that can be included in a bowling score indicator.

Apparatus for detecting which pins are standing after delivery of the first ball in each frame of a bowling game are well known. Operation of a pin detecting apparatus is normally started after impact of the bowling ball with a ball-stopping cushion at the back of the pit for receiving fallen pins. While many standing pin detecting apparatuses are known, the split detector of this invention is described in cooperation with a known zone-type of standing pin detectors. However, as will become evident, the split detector of this invention is independent of the described standing pin detector and can be applied to any known standing pin detector. According to this invention, pulses, indicating which pins are standing after delivery of the first ball in each frame of a bowling game, are applied to an electronic circuit which includes an output indicator having two conditions. One condition of the indicator indicates a split and the other condition indicates absence of a split. Since a split cannot occur if the headpin (the number 1 pin) is standing no matter what other pins are still standing, a pulse that indicates that the headpin is standing is so applied to the indicator as to prevent it from indicating a split. Similarly, since a split cannot occur after the second ball in a frame, the indicator is prevented from indicating a split after rolling the second ball of a frame.

The novel features of the invention, both as to its organization and methods of operation as well as additional objects and advantages will be understood more readily from the following description, when read in conjunction with the accompanying drawing, in which:

FIGS. 1A and 1B together are a block diagram of one embodiment of a split indicating apparatus according to this invention and

FIG. 2 is a timing chart which is useful in explaining the apparatus of FIGS. 1A and 1B.

The position, before the first ball is rolled, of the tenpins used in a bowling game is indicated by the circles labeled 1–10 in FIG. 1. As is understood, a bowling ball is rolled towards the pins along a direction generally parallel to a line through pins 1–5. The ball may knock down one or more of the pins and it hits the cushion 12. When the ball hits the cushion 12, a microswitch 14 is closed momentarily to energize a 3-second delay device 16. The 3-second delay is necessary, in accordance with the ABC rules, to permit the pins to become stabilized in position before the standing pins are detected. A ball signal pulse BS appears at the output of the delay device 16 3 seconds after the microswitch 14 is closed. This pulse is indicated on the top or No. 1 curve of the timing chart of FIG. 2. The pulse BS is applied to a differentiator 18 to produce a pulse BS1 coincident with the leading edge of the pulse BS, this pulse BS1 being shown in the No. 2 curve of the timing chart. The purpose of pulse BS1 will be described below.

The pulse BS is applied to a flashlamp 20 to cause it to become illuminated during a time T1 (curve 3 of FIG. 2) to illuminate the top of any or all of pins 1, 3, 6 and 10 that remain standing after the first ball in a frame. Since the BS and the T1 pulses coincide in time, the BS pulse is used as the T1 pulse. The pulse BS is also applied to a delay circuit 22, the output of which is fed to another delay circuit 24, the output of which is fed to still another delay circuit 26.

The output of delay circuits 22, 24 and 26 respectively comprise T2, T3 and T4 pulses and are fed respectively to flashlamps 28, 30 and 32. Lamp 28 illuminates the top of any and all of pins 2, 5 and 9 that remain standing after the first ball has been rolled. Lamp 30 illuminates the top of any and all of pins 4 and 8 that remain standing after the first ball has been rolled, and lamp 32 illuminates the top of pin 7 if it remains standing after the first ball has been rolled. Each delay circuit 22, 24 and 26 delays the pulse applied thereto for a short while, a few milliseconds for example, so that no two lamps are illuminated at the same time. Curve 3 of FIG. 2 illustrates time pulse T1 and curve 4 of FIG. 2 illustrates time pulses T2, T3 and T4.

A light-sensitive device or photocell 34 is positioned to be energized by light reflected from the top of any or all of pins 1, 2, 4 and 7 that remain standing after a ball is rolled. A photocell 36 is positioned to be energized by light reflected from the top of any or all of pins 3, 5 and 8. A photocell 38 is positioned to be energized by light reflected from the top of either or both of pins 6 and 9 that remain standing and a photocell 40 is positioned to be energized by light reflected from the top of pin 10 if it remains standing after the ball has been rolled. Therefore, during time T1, photocells 34, 36, 38 and 40 respectively detect which, if any, of pins 1, 3, 6 and 10 are still standing; during time T2, photocells 34, 36 and 38 respectively detect which, if any, of pins 2, 5 and 9 are still standing; during time T3 photocells 34 and 36 respectively determine which, if any, of pins 4 and 8 are still standing and at time T4 photocell 34 determines if pin 7 is still standing.

The output of photocell 34 is applied to a monostable multivibrator (MMV) 42 to produce successive X1 pulses. The successive X1 pulses start coincidentally with timing pulses T1, T2, T3 and T4 and are a little longer than the timing pulses. The occurrence of an X1 pulse during time T1 indicates that the 1 pin is standing. The X1 pulse during time T2 indicates that the 2 pin is standing, and the X1 pulse during time T3 indicates that the 4 pin is standing, and the X1 pulse during time T4 indicates that the 7 pin is standing. Absence of X1 pulses indicate the corresponding pin is down. These pulses are shown in curve 5 of FIG. 2. It will be noted that if all of pins 1, 2, 4 and 7 are down, no X1 pulse will be produced. Similarly, if only pin 1 is standing, only the X1 pulse during time T1 will occur. The output of the MMV 42 is applied to a differentiator 44 which produces a pulse XD1 (curve 9 of FIG. 2) at the end of each X1 pulse, if there be one, after the expiration of the corresponding T1–T4 pulses.

The output of photocell 36 is applied to an MMV 46. The MMV 46 is adjusted to provide an output pulse X2 (Curve 6 of FIG. 2) which starts coincidentally with the successive T1–T3 pulses and which is longer than the X1 pulses, each time the MMV 46 is energized by the output of photocell 36. Therefore, successive X2 pulses occur during times T1–T3 whenever one or more of pins 3, 5 and 8 is standing. The X2 pulse during time T1 indicates that the 3 pin is standing. The X2 pulse during time T2 indicates that the 5 pin is standing. The X2 pulse during time T3 indicates that the 8 pin is standing. The output of MMV 46 is applied to a differentiator 48 which produces an XD2 pulse at the end of each X2 pulse, if any, and after the XD1 pulses. The XD2 pulses are shown in curve 10 of FIG. 2.

Similarly, the output of the photocell **38** is applied to an MMV **50** which produces X3 pulses during times T1, and T2 respectively, to indicate that pins **6** and **9** are standing. While the X3 pulses start respectively at the beginnings of times T1 and T2, and X3 pulses are longer than the X2 pulses. The output of the MMV **50** is applied to a differentiator **52** which produces a pulse at the end of each X3 pulse, if any, and after the XD2 pulses. The XD3 pulses are shown in curve **11** of FIG. 2.

Also, the output of photocell **40** is applied to MMV **54** to produce an X4 pulse during time T1 is pin **10** is standing. This X4 pulse starts with the T1 pulse and is longer than an X3 pulse.

Since the occurrence of an X pulse indicates a pin is standing, the X pulses may be called pin pulses or signals. Since the XD pulses are applied to memory devices, as will be shown, the XD pulses are called memory pulses or signals.

The output of delay circuits **22**, **24** and **26** are applied to an OR-circuit **55** which applies the timing pulses T2, T3 and T4, shown at curve **4** of FIG. **2**, to its output terminal.

Turning now to FIG. **1B**, a plurality of flip-flop circuits (FF) **56**, **58**, **60**, **62**, **82** and **86** are provided. Each FF has at least one reset or R input, at least one set or S input, at least one negative or N output and at least one affirmative or A output. These FF's **56–62**, **82** and **86** each respond to a pulse of the proper polarity applied to its R input to produce a high, or positive voltage at its N output and a low or nega,ive voltage at its A output. These flip-flops each also respond to a pulse of the proper polarity applied to its S input to produce a high or positive voltage on its A output and a low or negative voltage at its N output. Pulses of the wrong polarity produce no change in the output of the FF's. Similarly the second and successive pulses applied to an R or an S input of a FF does not produce a change in the output of the FF in the absence of an intervening pulse applied to the S or the R input of the FF.

The BS1 pulses are applied to a R input of all the FF's **56–62**, **82**, and **86**. Since this BS1 signal occurs at the beginning of time T1, all the FF's are put into their reset conditions before any information is fed to them.

X4, XD1, XD2 and XD3 informations are fed to respective S inputs of FF **56**. Therefore, FF **56** acts as a memory device in that it produces a positive output voltage at its A output whenever, during the time interval between the end of T1 and the beginning of T2, any one or more pins **1**, **3**, **6** and **10** is standing. Furthermore, FF **56** provides a positive output at its A output, during the time between the end of time T2 and the beginning of time T3, if any one or more of pins **1**, **3**, **6**, **10**, **2**, **5** or **9** is standing. Furthermore, FF **56** produces a positive voltage at its A input, if, during the time interval between the end of T3 and the beginning of T4, any one or more of pins **1**, **2**, **3**, **4**, **5**, **6**, **8**, **9**, or **10** is standing. The curve **15** of FIG. **2** marked PS indicates when the FF **56** can be made to produce a positive output at its A output terminal. The FF **56** continues to provide a positive output at its A terminal until reset by the next BS1 pulse.

As noted above, BS1 information is fed to FF **58** to reset it when a ball is rolled. Also, it is reset at the ends of times T2, T3 and T4 due to application to an R terminal thereof of T2–T4 timing information. XD1 information, which has different meaning when it occurs during different ones of times T1–T4, is fed to the set terminal of FF **58**. Therefore, if the one pin is standing after time T1 and before T2, the FF **58** is set to indicate this fact, and the FF **58** continues to indicate this fact until it is reset at the end of the T2 time. Similarly, if an XD1 pulse occurs after T2 and before T3, the FF **58** is set to indicate that the **2** pin is standing and it continues to indicate this fact until the end of the T3 time, and if an XD1 pulse occurs after T3 and before T4, the FF **58** is set to indicate that the **4** pin is standing and it continues to indicate this fact until the end of time T4. Also, the occurrence of an XD1 pulse after T4 and before the next BS1 pulse sets the FF **58** to indicate that the **7** pin is standing. Therefore, the FF **58** remembers whether the **1** pin is standing when the T2 occurs, whether the **2** pin is standing when the T3 pulse occurs and whether the **4** pin is standing when the T4 pulse occurs. (It also remembers if the **7** pin is standing when the next BS1 pulse occurs, but this information is not used.) Therefore, a reset condition of FF **58** during which a positive output appears at the N terminal of FF **58** indicates that the **1** pin, or the **2** pin, or the **4** pin, or the **7** pin is not standing when the reset condition occurs during the T2, or T3, or T4 and the BS1 times respectively. The output at the A terminal of FF **58** when pins **1**, **2**, **4** and **7** are standing is shown at curve **12** of FIG. **2**. The output at the N terminal of FF **58** is not shown but it is the converse of curve **12**.

As noted above, BS1 information is fed to an R terminal of FF **60**. Also, T2, T3 and T4 information is fed to another R terminal of FF **60**, and, XD2 information is fed to an S terminal thereof. Therefore, FF **60** remembers and indicates at times T2 whether or not the **3** pin is standing. It also remembers and indicates at time T3 whether or not the **5** pin is standing, and it remembers and indicates at time T4 whether or not the **8** pin is standing. The FF **60** gives no indications as to any other pin or pins. The A output of FF **60** when pins **3**, **5** and **8** are standing is shown at the 13th or PX2 curve of FIG. **2**. The N output is not shown but it is the converse of the PX2 curve.

As noted above, BS1 information is fed to an R terminal of FF **62**. T2, T3 and T4 information is also fed to another R terminal of FF **62**. Since XD3 information is fed to the S input of FF **62**, FF **62** remembers at time T2 whether or not the **6** pin is standing and at time T3 whether or not the **9** pin is standing. No information about any other pin is given by FF **62**. The A output of FF **62** when the **6** and the **9** pin are standing is shown at curve **14** of FIG. **2**. The N output is not shown but it is the converse of the A output.

The A outputs of each of the FF's **56**, **58**, **60** and **62** are conveniently called PS, PX1, PX2 and PX3 and their converses, at the N outputs of the FF's are called $\overline{PS}$, $\overline{PX1}$, $\overline{PX2}$, and $\overline{PX3}$, each respectively,

A plurality of AND-circuits **64**, **66**, **68**, **70**, **72**, **74** and **76** are provided. The AND-circuits **64** and **76** have two inputs. The AND-circuits **66**, **68** and **72** have three inputs and the AND-circuits **70** and **74** have four inputs. All the AND circuits are similar in that no output is produced at the output circuit of any AND circuit unless all the inputs to that AND circuit are simultaneously the same potential, positive, for example.

X1 and $\overline{X1}$ information from FF **58** are applied to the AND-circuit **64** whereby AND-circuit **64** produces an output when and only when, during the occurrence of an X1 pulse FF **58** produces positive output on its N terminal. That is, if the **1** pin is standing during the first X1 interval, that is during T1, a positive output is produced by the AND-circuit **64**. If the **1** pin is not standing during the second X1 interval, that is, during T2, and the **2** pin is standing, a positive output is provided by the AND-circuit **64**. Similarly, if the **2** pin is not standing during the third X1 interval, that is during T3, and the **4** pin is standing, a positive signal is provided at the output of AND-circuit **64** and finally if the **4** pin is not standing and the **7** pin is standing during its fourth X1 or T4 interval, a positive output is produced by the AND-circuit **64**. That is, the AND-circuit **64** gives information (if such be the case) that (a) the **1** pin is standing, (b) the **2** pin is standing and the **1** pin is not standing, (c) the **4** pin is standing and the **2** pin is not standing, and (d) the **7** pin is standing and the **4** pin is not standing respectively in the four successive time intervals, T1–T4. As will be noted, the (a) information is not used.

$\overline{PX1}$, X2 and $\overline{PX2}$ informations are applied to the AND-gate **66**. Therefore, if AND-gate **66** provides an output during the first X2 interval, that is during T1, it indicates that pin **3** is standing. If AND-gate **66** provides an output during the second X2 or T2 interval it indicates that pin **5** is standing and that neither of pins **1** or **3** is standing. If AND-gate **66** provides an output during the third X2 or T3 interval, it indicates that pin **8** is standing and that neither of pins **2** or **5** is standing. AND-circuit **66** has no output during time T4 and its output during time T1 is not used.

$\overline{PX2}$, X3 and $\overline{PX3}$ informations are applied to the AND-gate 68. Therefore if the AND-gate 68 provides an output during the first X3 or the T1 interval, it indicates that pin 6 is standing. If AND-gate 68 provides an output during the second X3 or T2 interval, it provides an indication the pin 9 is standing and that neither of the 3 and 6 pins is standing. There is no output from AND-circuit 68 during times T3 and T4 and its T1 output is not used.

The outputs of each of the AND-circuits 64, 66 and 68 are applied to the input of an OR-circuit 78, which applies a positive voltage to the AND-circuit 72 whenever any input to the OR-circuit 78 is positive.

X2 information is applied to an invertor 80 and inverted X2 information ($\overline{X2}$) is applied to the AND-circuit 70. X1 and X3 information and T2–T4 timing pulses are also applied to AND-circuit 70. Therefore, during interval T2, when pins 2 and 9 are standing and pin 5 is not standing, AND-circuit 70 applies a positive output to the FF-circuit 82. Since no timing pulse is applied thereto during time T1 and since, during intervals T3 and T4, there can be no X3 input to AND-circuit 70, AND-circuit 70 has no output during intervals T1, T3 and T4.

PS information, the output from OR-circuit 78 and T2–T4 are applied to the inputs of AND-circuit 72. Therefore, if any one or more of pins 1, 3, 6 and 10 is up and if there is an output from any one or more of AND-circuits 64, 66 and 68 during time T2, the AND-circuit 72 will apply a pulse to a set input terminal of FF 82. Furthermore, if any one or more of pins 1, 2, 3, 5, 6, 9 or 10 is up and if there is an output from any one or more of AND-circuits 64, 66 and 68, during time T3, the AND-circuit 72 will apply a pulse to FF 82. Similarly, of any one of pins 1, 2, 3, 4, 5, 6, 8, 9 or 10 is up and if any one of any circuits 64, 66 and 68 provides an output at time T4, AND-circuit 72 will apply a set pulse to FF 82.

X2 and X4 information and T1 timing pulses are applied to AND-circuit 74. Also X3 information is inverted in inverter 84 and $\overline{X3}$ information is applied to AND-gate 74. Therefore, if during time T1, pin 3 is standing, pin 6 is down and pin 10 is standing, AND-gate 74 applies a S pulse of FF 82. AND-circuit 74 does not produce an output at times T2–T4.

X1 information and T1 timing pulses are applied to the AND-gate 76. If therefore, at time T1, the 1 or headpin is standing, the AND-gate 76 applies a pulse to the S terminal of the FF 86, which applies an output voltage to an R terminal of the FF 82 until the FF 86 is reset, preventing the setting of FF 82 while FF 86 is set. This action prevents indication of a split as long as the headpin is up. The BS1 signal is also applied to the R terminal of the FF 86 and to an R terminal of the FF 82 to reset them when a ball is rolled. The A output of the FF 82 is applied to the AND-circuit 88. The output of AND-circuit 88 is applied to the input of the indicator 90 to cause it to indicate the occurrence of a split, as will be explained. During the period between the time when the pinsetter sets all the pins and the second ball in the frame is rolled, a positive voltage is applied to the second input of the AND-circuit 88 over a lead 89 by means not shown. This means may comprise a source of positive voltage in series with a switch which is closed when the pinsetter sets up all the pins and which is opened when the second ball of a frame is rolled. The purpose of the AND-circuit 88 is to prevent indications of a split after the second ball is rolled. As understood, no split can occur after the second ball is rolled in a frame.

In explaining the operations of the described split detector, a general explanation will be given and then the response of the split detector to three situations will be described and the descriptions will terminate when a split is indicated. For simplicity, only one reason why an AND circuit will produce no response will be given even though several reasons may exist.

A previous indication of a split is cleared by the pulse BS1, which is produced as a result of a ball hitting the cushion 12. The BS1 pulse is applied to all the FF's 56, 58, 60, 62, 82 and 86 to reset them.

If the 1 pin is standing, a split cannot occur. As explained above, the AND-circuit 76 indicates that the 1 pin is standing at time T1. The output of AND-circuit 76 causes setting of the FF 86 and the A output of the FF 86 is applied to reset the FF 82 and to keep it reset until the next BS1 pulse resets the split detector. Also, since the arrangement of standing pins after the second ball is not considered a split, no matter what it is, the indicator 90 may be effectively disconnected from the FF 82 during the period after the second ball in a frame is rolled and the pins are reset for the next frame by the AND-circuit 88 as mentioned above.

In general, the described split detector is set up to perform the following functions:

a. At time T1 if the 1 pin is up, reset the FF 82 and hold it reset to prevent any split indication.

b. If the 1 pin is down, set the FF 82 to cause a split indication if

1. At time T1, and subsequently, the 6 pin is down and the 3 and the 10 pins are standing. With the 6 pin down and pins 3 and 10 standing, whether the other pins are standing or not, a split exists.
2. At time T2, and subsequently, the 2 and the 9 pins are up and the 5 pin is down. Again, whether the other pins are standing or not, a split exists.
3. At time T2, and subsequently, the 2 pin is up and one or more of 3, 6 and 10 are up.
4. At time T2, and subsequently, the 3 pin is down and one or both of the 6 and the 10 are up and the 5 pin is up. A split exists no matter whether the other pins are up or down.
5. At time T2, and subsequently, the 6 pin is down, the 9 and 10 pins are up. A split exists here no matter whether the other pins are up or down.
6. At time T3, and subsequently, the 2 pin is down, the 4 pin is up and any one or more of the 3, 5, 6, 9 and 10 pins are up. Again, a split exists no matter whether the other pins are up or down.
7. At time T3, and subsequently, the 2 and the 5 pins are down, the 8 pin is up and any one or more of the 3, 6, 9 and 10 pins are up. A split exists no matter whether the other pins are up or down.
8. At time T4, the 4 pin is down, the 7 pin is up and any one or more of the 2, 3, 5, 6, 8, 9 and 10 pins are up.

A generalized statement of the operation of the split detector is as follows:

a. at T1, hold FF 82 reset if X1

b. otherwise, set FF 82 if

1. at T1, $X2 \cdot \overline{X3} \cdot X4 = 1$
2. at T2–T4, $X1 \cdot \overline{X2} \cdot X3 = 1$
   or $\overline{PX1} \cdot X1 \cdot PS = 1$
   or $\overline{PX1} \cdot \overline{PX2} \cdot X2 \cdot PS = 1$
   or $\overline{PX2} \cdot \overline{PX3} \cdot X3 \cdot PS = 1$

It will be noted that if only the 2, 4, 5, 7 and 9 pins are standing, or if only the 3, 5, 6, 8 and 10 are standing, no split will be indicated, since these formations are not considered to be splits in spite of the fact that these formations fit the ABC definition of a split. It will be noted that the ABC requirements for a split are fulfilled in that the headpin is down and a pin is down between two pins which are up, (for example between the 7 and the 9 or between the 8 and the 10 pins) in these two formations.

Let it first be assumed that the first ball has been rolled and the only pin to fall is the head or one pin. Three seconds after the ball has hit the back cushion 12, a BS pulse is applied to the flashlamp 20 during a time interval T1 to energize it. At the same time, the BS pulse is applied to the differentiator 18 to cause a BS1 pulse to appear at its output. The BS1 pulse resets the split indicator as explained above. During the time T1, light shines on the top of pins 3, 6 and 10 (pin 1 being down) and photocells 36, 38 and 40, receiving light from the tops of pins 3, 6 and 10 respectively, apply pulses to MMV's 46, 50 and 54 respectively to provide the X2, X3 and X4 pulses of curves 6, 7, and 8 of FIG. 2 during time T1. However, since the headpin is down, MMV 42 is not pulsed and whereby no X1 pulse is produced during time T1 by MMV 42. THe dif-

ferentiators 48 and 52 provide respectively the XD2 and XD3 pulses of curves 10 and 11 of FIG. 2, also as explained above. Since there is no X1 pulse during the time T1, there is no output from the AND-circuit 76 to which X1 and T1 pulses are applied, and FF 86 remains reset and no reset voltage is applied by FF 86 to FF 82. Therefore, if a split exists, the FF 82 remains in condition to cause indications thereof. AND-circuits 70 and 72 can have no output during time T1 for the reason that no T1 timing input is applied to the timing input connections thereof. Since the outputs of AND-circuits 64, 66 and 68, if any, are applied through the OR-circuit 78 to the AND-circuit 72 which cannot produce an output during time T1, whether or not AND-circuits 64, 66 and 68 produce and output during time T1 is unimportant and the inputs to AND-circuits 64, 66 and 68 during time T1 will not be further considered. AND-circuit 74 can have no output during time T1 since the X3 pulse is applied thereto in inverted condition that is negatively, due to the fact that pin 6 is standing during time T1. Therefore at the end of time T1, with only the headpin so far being indicated as being down, a split may or may not be present and the split indicator is in condition to later indicate a split, if there be one. In this case, between the times T1 and T2, the FF 56 is set by the first one of the XD2, the XD3 and the X4 pulse that it receives and it remains set until another BS1 pulse is produced when the next ball is rolled. The XD2 and the XD3 pulses set the FF 60 and the FF 62 respectively, and FF's 60 and 62 stay set until the end of the T2 pulse. As explained above, the FF 56 indicates that a pin is standing, but not which one or how many. The FF 60 indicates until reset at the end of time T2 that the 3 pin is up and the FF 62 indicates until reset at the end of time T2 that the 6 pin is up.

During the time T2, the light 28 is on and, since pins 2, 5 and 9 are up, the photocells 34, 36 and 38 will respectively see the tops of these pins. There will, therefore, be an X1, an X2 and an X3 pulse, produced by MMV's 42, 46 and 50 respectively, during the time T2. Since an inverted X2 pulse is applied to AND-circuit 70, there is no output from it, at time T2. The X1 pulse is applied to the AND-circuit 64 with a N voltage from the FF 58. As noted above, the FF 58 was in its reset condition, since during the interval between times T1 and T2, no set pulse was applied thereto since no XD1 pulse was produced. Therefore, a positive voltage is applied at the input of AND-circuit 64 from the FF 58 and the AND-circuit 64 produces an output which is applied the the OR-circuit 78. Since the three AND-circuits 64, 66 and 68 feed the OR-circuit 78, it has become immaterial whether the AND-circuits 66 and 68 produce an output during the time T2, and they will not be considered further during time T2.

A positive voltage is applied to one of the inputs of the AND-circuit 72 from the OR-circuit 78. A positive pulse is applied to the AND-circuit 72 from the FF 56, which has previously been set. Therefore, at the time T2, a positive timing pulse is applied to three inputs of the AND-circuit 72 and the AND-circuit 72 applies a set pulse to the FF 82 to cause it to energize the indicator 90 by way of the AND-circuit 88. Since a split has been indicated, no further operation of the split detector can change this indication until the next ball is rolled. Therefore, the operating of the split detector with only the one pin down will be pursued no further.

Let it be assumed that only the 7, 8, 9 and 10 pins are standing after delivery of the first ball. Then at the time T1, there will be only an X4 pulse, which is applied to set FF 56. Since AND-circuits 70 and 72 have no timing pulse applied thereto at the time T1, they have no outputs. Since there is no X2 pulse at this time, AND-circuit 74 has no output. Since there is no X1 pulse at this time, AND-circuits 76 has no output. Therefore, at the end of time T1, the FF 82 has not been set, however FF 56 is in its set condition.

Since pins 2 and 5 are down and the 9 pin is up, at time T2, only an X3 pulse is produced, AND-circuits 64 and 70 have no output at time T2 since there is no X1 pulse. AND-circuit 76 provides no output during times T2–T4. AND-circuits 66 and 74 have no output at time T2 since there is no X2 pulse. However, a positive voltage is applied to all three inputs of AND-circuit 68, one due to the existence of the X3 pulse during time T2 and the other due to the fact that, since FF's 60 and 62 are in reset condition, their N outputs applied to AND-circuit 68 are positive. The output from the AND-circuit 68 is applied at time T2 through the OR-circuit 78 to the AND-circuit 72. The T2 pulse is applied to the AND-circuits 72 and a positive pulse from the FF 56 (which has been set by the X4 pulse during the time T1) is also applied to the AND-circuit 72. AND-circuit 72 therefore causes setting of FF 82 to indicate a split. As is understood, if pins 1, 2, 3, 5 and 6 are down and pins 9 and 10 are up, a split exists whether or not pins 4, 7 and 8 are up. Therefore, the indication by FF 82 is correct.

Let it be assumed that after the first ball is rolled the 7 and 10 pins are the only ones up. At the time of the BS1 pulse, all FF's 56, 58, 60, 62, 82 and 86 are reset thereby. At time T1, the only pulse produced is the X4 pulse. At time T1, AND-circuits 70 and 72 can have no output so it is immaterial whether AND-circuits 64, 66 and 68 have outputs at time T1. Since there is no X1 pulse at the time T1, and AND-circuit 76 provides no output and the FF 86 remains reset whereby the FF 86 applies no voltage to hold the FF 82 reset, that is the FF 82 can respond to a set pulse that would indicate a split. Therefore, at the end of time T1, no set pulse is applied to FF 82. The X4 pulse is applied to set the FF 56 and since FF 56 is reset only at the occurrence of a BS1 pulse, FF 56 remains set throughout times T2, T3 and T4.

At times T2 and T3, no X1, X2, X3, or X4 pulse is produced and no AND circuit has an output and no set pulse is applied to FF 82, or to FF's 56–62.

At time T4, an X1 pulse is produced to indicate that the 7 pin is standing. There is an output from AND-circuit 64 since it has a positive voltage applied to both its inputs. Therefore, the outputs of circuits 66 and 68 are immaterial. There is no output from AND-circuit 70 since no X3 pulse is produced and there is no output from AND-circuit 74 and 76 since no T4 pulse is applied thereto. HOwever, positive pulses are applied to all the inputs of AND-circuit 72 at time T4, one from set FF 56, and one from AND-circuit 64 by way of OR-circuit 78, and the T4 timing pulse. AND-circuit 72 sets the FF 82 and FF 82 applies a positive voltage to one input of the AND-circuit 88. If the second ball has not been rolled, a positive voltage is applied to the other input of the AND-circuit 88 and a positive voltage is applied to the indicator 90 to indicate occurrence of a split.

Indications of others of the great number of pin configurations does not appear necessary for the understanding of the disclosed split detector.

While the described split detector has been disclosed in connection with a zone-type of standing pin detector, it is evident that the split detector may be used with other types of standing pin detectors. For example, all standing pins may be detected in any manner and stored by setting flip-flop circuits which are individual to each respective pin. Then at a time T1, after all the standing pins have been detected, the flip-flop circuits storing information concerning pins 1, 3, 6 and 10 will be caused to produce $\overline{X1}$, $\overline{X2}$, $\overline{X3}$ and $\overline{X4}$ pulses or signals respectively at their A outputs if these pins are standing, The storage flip-flop circuits will produce X1, X2, X3 and X4 pulses or signals at their N outputs if the corresponding pin is down whereby separate inverters such as 80 and 84 are not necessary when using such storing flip-flop circuits. The storing flip-flop circuits in effect have built-in inverters. Similarly, at a subsequent time T2, the flip-flop circuits storing information concerning pins 2, 5 and 9 will be caused to produce none, one or more of X1, X2 and X3 pulses corresponding to which of these pins is standing, if any. At a time T3, later than time T2, the flip-flop circuits storing information concerning pins 4 and 8 will be caused to produce none or one or more of X1 and X2 pulses corresponding to which of these pins are standing if any. Finally, at a still later time T4, the remaining flip-flop circuit may be caused to give an X1 indication if the 7

pin is standing. In each time T2–T4, use of storage flip-flop circuits will make separate inverters such as 80 and 82 unnecessary. Therefore, the above-described split detector is not in any way dependent on the disclosed standing pin detector, which is described for the sake of convenience only. If desired, apparatus may be provided to print at the appropriate place on the bowling sheet, a circle to indicate that a split has occurred.

Although only a single bowling split indicator has been described, variations thereof are possible within the spirit of this invention. Hence, it should be understood that the foregoing description is to be considered as illustrative and not in a limiting sense.

What is claimed is:

1. A split detector comprising

means responsive to the presence of a bowling ball in the alley pit to produce a succession of at least four delayed timing signals,

means responsive to the first one of said timing signals to provide a respective pin signal for each pin standing of a first group of pins, said pin signals indicating by their occurrence that corresponding pins of said first group of pins are standing and indicating by their absence that corresponding pins of said first group of pins are down,

means responsive to the second one of said timing signals to provide a respective second pin signal for each pin standing of a second group of pins, said second pin signals indicating by their absence that corresponding pins of said second group of pins are down,

means responsive to the third of said timing signals to provide a respective third pin signal for each of a third group of pins, said third pin signals indicating by their occurrence that corresponding pins of said third group are standing and indicating by their absence that corresponding pins of said third group are down,

means responsive to the fourth of said timing signals to provide a fourth pin signal to indicate that a predetermined pin is standing, absence of said fourth pin signal indicating that said predetermined pin is down,

memory means to indicate through successive time signals after the first thereof whether any pin signals have been produced,

additional memory means to indicate after each timing signal and through a next timing signal whether or not certain pin signals have been produced during the timing signal just previous to said next timing signal,

means responsive to the occurrence of a signal indicating that the headpin is standing to prevent indication of a split, and

means responsive to said pin signal and to the indications of each of said memory means to indicate a split when one occurs.

2. A bowling split indicator comprising

means to provide a succession of timing signals,

means responsive to a first timing signal to provide a pin pulse of a given length for each pin standing of a first group of pins during a first time period,

means responsive to a second timing signal to provide a pin pulse of a length greater than said given length for each pin standing of a second group of pins during a second time period,

means responsive to a third timing signal to provide a pin pulse of a length still greater than said greater length for each pin standing of a third group of pins during a third time period,

means responsive to a fourth timing signal to provide a pin pulse of the greatest length to indicate that a further pin is standing during a fourth time period,

lack of occurrence of a pin pulse in each time period indicating that corresponding pins are down,

means to provide memory signals at the end of each of the pin pulses of given length, of greater length and of still greater length,

a plurality of flip-flop circuits each having at least one reset input terminal and at least one set input terminal and a negative output terminal and an affirmative output terminal, said flip-flop circuits providing one polarity of output at their negative terminals and the other polarity of output at the affirmative terminals in response to a pulse applied to the reset terminals and the opposite output potentials of their negative and affirmative terminals in response to a pulse applied to their set terminals,

a plurality of AND circuits, said AND circuits each having a plurality of input terminals and an output terminal, each AND circuit providing an output at its output terminal only when pulses of the proper polarity are applied together to all its input terminals,

means responsive to the first of said timing signals to provide a reset signal at the beginning of said first timing signal,

means to apply said reset signals to a reset terminal of all of said flip-flop circuits,

means to apply said pin pulses of the greatest length to a set input terminal of the first one of said flip-flop circuits,

means to apply said memory signals at the end of said pin pulses of given length to a set terminal of said first flip-flop circuit and to a set terminal of a second of said flip-flop circuits,

means to apply said memory signals at the end of said pin pulses of greater length to a set terminal of said first flip-flop circuit and also to a set terminal of a third of said flip-flop circuits,

means to apply said memory signals at the end of said pin pulses of still greater length to a set terminal of said first flip-flop circuit and also to a set terminal of a fourth of said flip-flop circuits,

means to apply said second, third and fourth timing signals to a reset terminal of said second, third and fourth flip-flop circuits,

means to apply said pin pulses of given length and the negative output of said second flip-flop circuit to respective input terminals of a first AND circuit,

means to apply said pin pulses of greater length and the negative outputs of said second and third flip-flop circuits to respective input terminals of a second AND circuit,

means to apply said pin pulses of still greater length and the negative output of said third and fourth flip-flop circuits to respective input terminals of a third AND circuit,

means to apply the affirmative output of said first flip-flop circuit, the outputs of said first, second and third AND circuits, and the second, third and fourth timing signals to input terminals of a fourth AND circuit,

a plurality of inverter circuits each having an input and an output terminal and each of which provides an inverted version of the voltage applied to its input terminal at its output terminal,

means to apply the pin pulses of given length, the pin pulses of greater length through one of said inverters, the pin pulses of still greater length and the second, third and fourth timing pulses to input terminals of a fifth AND circuit,

means to apply said pin pulses of still greater length through another of said inverters, the pin pulses of greatest length, the pin pulses of greater length and the first timing pulse to respective input terminals of the sixth of said AND circuits,

means to apply said pin pulses of said given length and said first timing signals to respective input terminals of a seventh of said AND circuits,

means to apply the output of said seventh AND circuit to a set terminal of a fifth of said flip-flop circuits,

means to apply the affirmative output of said fifth flip-flop circuit to a reset terminal of a sixth of said flip-flop circuits, and

means to apply the outputs of said fourth, fifth and sixth AND circuits to set inputs of said sixth flip-flop circuits,

whereby a predetermined voltage at the affirmative output terminal of said sixth flip-flop circuit shows that a split has occurred.

3. An apparatus for use in a bowling game wherein a plurality of pins are set in a predetermined array headed by a particular pin, said apparatus indicating the presence during a certain given time interval of a split in said array when certain of said pins are down during said time interval, said apparatus comprising:

means for providing a discrete timing signal during the occurrence of said time interval,

means for providing a plurality of pin signals, each pin signal manifesting a separate, different set pin, the occurrence of a pin signal during said time interval indicating that the corresponding pin is standing and lack of occurrence of a pin signal during said time interval indicating that said corresponding pin is down,

means responsive to that pin signal manifesting a set headpin occurring in time coincidence with said timing signal for preventing the indication of a split, and

means responsive to the time coincidence occurrence of certain of said pin signals and said timing signal and absence of occurrence of certain others of said pin signals during the occurrence of said timing signal to provide a split indication.

4. An apparatus for use in a bowling game wherein a plurality of pins are set in a predetermined array headed by a particular pin, said apparatus indicating the presence during a plurality of separate, different certain given time intervals of a split in said array when certain of said pins are down during said time intervals, said apparatus comprising:

means for providing a plurality of discrete, separate timing signals each occurring during a different, separate one of said time intervals,

means for providing a plurality of pin signals, each pin signal manifesting a separate, different set pin, said pin signals occurring in separate, discrete groups, each signal group manifesting a different portion of said array and corresponding to a separate, different one of said timing signals, the occurrence of a pin signal during the corresponding time interval indicating that the corresponding pin is standing and lack of occurrence of a pin signal during the corresponding time interval indicating that said corresponding pin is down,

means responsive to that pin signal manifesting a set headpin occurring in time coincidence with one of said timing signals for preventing the indication of a split, and

means responsive to the time coincidence occurrence of certain of said pin signals in any of said groups with the timing signal corresponding to that group and absence of occurrence of certain others of said pin signals in any of the other groups during the occurrence of that timing signal corresponding to the respective one of the other groups for providing a split indication.

5. The apparatus of claim 4 wherein there are provided four separate timing signals and wherein each group includes a different number of pins.

6. The apparatus of claim 4 wherein said timing signal means further include means responsive to the presence of a bowling ball rolled past said array to produce said timing signals sequentially,

means responsive to the first occurring of said timing signals to provide a reset signal, and

means responsive to said reset signals to reset said apparatus.

7. The apparatus of claim 4 wherein said means for providing a plurality of pin signals including means responsive to said timing signals for scanning said array in a given sequence,

each of said groups of pin signals being generated in response to a different, separate one of said timing signals, the pins in each of said groups being scanned substantially simultaneously in time coincidence with the corresponding timing signal.

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