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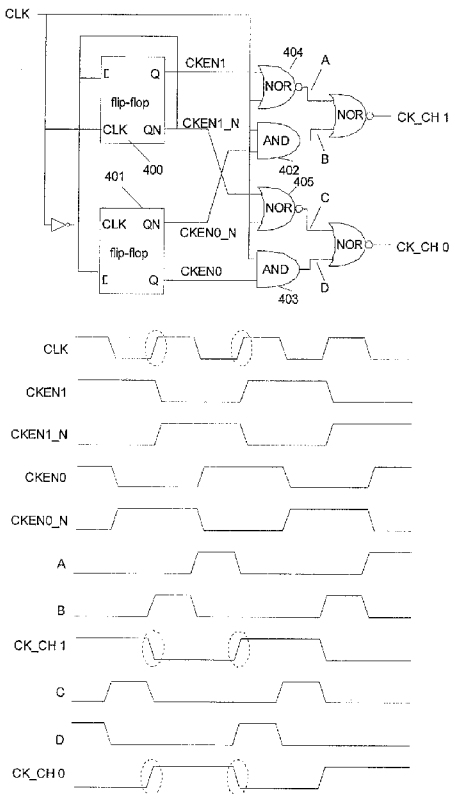
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*[Continued on next page]*

(54) Title: ANALOG-TO-DIGITAL CONVERTER TIMING CIRCUITS

FIG. 4




(57) Abstract: An analog-to-digital converter timing circuit disclosed herein uses a clock generation circuit that makes the analog-to-digital converter insensitive to input clock duty cycle. Minimum clock jitter is added to the clock signal while propagating through the disclosed circuit. A method and system are also disclosed to clock an interleaved pipelined ADC such that the operation is insensitive to input clock duty cycle and such that the clock jitter on the sampling clock edges is minimized.

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MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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A. CLASSIFICATION OF SUBJECT MATTER
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B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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| A | figures 3A, 3B | 1-5 |
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☒ See patent family annex.

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| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040,<br>Fax: (+31-70) 340-3016 | Martínez Martínez, J |

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# INTERNATIONAL SEARCH REPORT

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