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(71) Applicant: TEXAS INSTRUMENTS INCORPORATED [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant (for JP only): TEXAS INSTRUMENTS JAPAN LIMITED [JP/JP]; 24-1, Nishi-shinjuku 9-chome, Shinjuku-ku Tokyo 160-8366 (JP).

(72) Inventors: CHANDRASEKARAN, Ramesh; 8808 Canyonlands Dr., Plano, TX 75025 (US). KAYA, Cetin; 604 Nelson Ct., Plano, TX 74025 (US).

(74) Agents: DAVIS, Michael, A., Jr. et al.; Texas Instruments Incorporated, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

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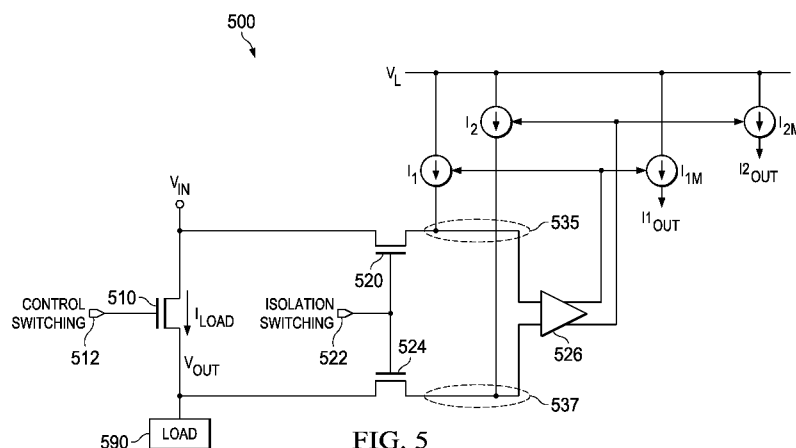


FIG. 5

(57) Abstract: Described examples include current sensing through a power semiconductor device with reduced sensitivity to temperature and process variations. An example arrangement (500) includes: a power switch (510) coupled between a voltage input and an output voltage terminal supplying current to a load (LOAD); a first isolation switch (520) coupled between the voltage input and a first node (535); a comparator amplifier (526) having a pair of differential inputs coupled to the first node (535) and a second node (537) to output a voltage in response to the difference at the differential inputs; and a first current source (I₁) coupled between a positive supply voltage and the first node (535) to output a first current responsive to the voltage output from the comparator amplifier (526). The first current is proportional to the current through the power switch (510) and the on resistance of the first isolation switch (520).

METHOD AND APPARATUS FOR SENSING CURRENT

[0001] This relates generally to electronic circuits, and more particularly to a method and circuitry for a sensing load currents over a wide temperature range in power semiconductor devices.

BACKGROUND

[0002] Field effect transistors (FETs) have been a staple for low resistance electronic switches since their introduction to the market. In a common application, a power FET or switch that is implemented using a FET is used to couple a supply voltage to a load at an output voltage terminal. Measuring the current flow through a FET is a common requirement by control circuits designed to keep the system (of which the FET and the control circuits are a part) within its operational parameters, and especially as a safety to effect current limiting during high load conditions to prevent device damage or failure of the FET. The maximum current flow occurs in the conduction mode when the FET is on and the resistance between the drain and source ($R_{DS(on)}$) is low. Traditional current sensing methods of adding a series resistor in the current path can generate a current measurement point, but this approach poses a tradeoff between power dissipation and peak measurement voltage. The series resistor value must be large enough for the sensed signal (a voltage corresponding to current through the resistor is measured) to be above the signal noise floor, yet as small as possible to reduce power dissipation. Also, the power dissipation of the shunt resistor will be proportional to the square of the load current, which negatively affects the system's efficiency. Furthermore, the parasitic inductance of such series resistance elements has an important detrimental role in determining circuit behavior when switching large currents in short time, causing voltage overshoots that overstress the circuits. Another conventional method is to use the voltage across parasitic resistance of an inductor, which is a part of the load, to approximate the load current.

[0003] FIG. 1 shows a circuit diagram 100 of a conventional circuit for estimating load current from a power FET. In an example circuit 100 from Patent No. US 5,982,160 to Walters et al.,

the load current is approximated by reconstructing the voltage from a series inductor 110 across a resistor–capacitor (RC) network 120. The inductor 110 variation, which is attributed to the mechanical amount of wire used and the intrinsic temperature sensitivity, will have a noticeable effect on the sensing accuracy across a wide temperature range. In further work, as illustrated in FIG. 1 of Patent No. US 6,870,352 by Walters et. al., a temperature compensated resistor was used in the RC network 120 to help contain the temperature variance issue. Using such temperature compensated resistors is typically more expensive than resistors integrated within the semiconductor package.

[0004] In the conduction mode, a FET has a somewhat linear R_{DSon} , which entices one to sense the voltage across the FET and use the appropriate R_{DSon} value to estimate the approximate load current. However, the resistance R_{DSon} could have a thermal coefficient as large as 8000ppm/°C, equaling about 80% in a typical operating range of 25°C to 125°C. To combat the large variance due to thermal changes, various arrangements of components with matching thermal coefficients (TC) have been employed to counteract the variations due to the intrinsic TC of the power FET.

[0005] FIG. 2 shows a circuit diagram 200 of another conventional solution for temperature compensated load current sensing. In FIG. 2, a schematic from FIG. 2 of Patent No. US 6,870,352 by Walters et al. shows the use of another thermally compensated sense resistor 220 (RSEN) is arranged and substantially matched to the thermal variation of the R_{DSon} of power FET 210.

[0006] FIG. 3 shows another conventional load current sensing arrangement 300, which uses a “current branch” methodology to estimate the load current. The primary power FET 310 is switched by a PWM switching arrangement and, as the load current flows through the load, part of the current is diverted to the sensing FET 330. Sense FET 330 is a smaller FET with a higher on resistance than the power FET 310. A sample of the load current will create a voltage V_s across resistor R_s that is proportional to the load current. Use of the sense FET 330 provides a simple method to approximate the load current, but it has some drawbacks. One concern is the achievable current accuracy and noise tolerance, which are limited by the voltage developed on the resistor. This also trades off with the ability to match the drain to source voltage of the two FETs; a mismatch is translated to nonlinearity in the current measurement. Also, because the voltage across the resistor R_s is small in comparison to other methods, amplifier 332 is typically

required to drive external (to the IC) loads, which causes tradeoffs on the circuit response speed, range and accuracy.

[0007] In each of those conventional solutions, temperature compensated resistors are needed with the best match available at the time of manufacture. These temperature compensated resistors are external to the integrated circuit of the FETs, and are expensive. Accordingly, more solutions have been attempted to exclude them.

[0008] FIG. 4 shows a circuit schematic 400 of another conventional current sensing topology excluding TC matched resistors. In FIG. 4, the power FET 410 is switched by a PWM switching circuit. The load current ILOAD flows through the load 490. V_{in} is typically a voltage higher than the breakdown voltage of the sensing circuitry. To protect the sensing circuits from the high voltage of V_{in} , another isolation FET 420 is used to block the high voltage when power FET 410 is in the off condition. When the power FET 410 is switched on, the voltage across it drops to a safe level, at which point the sensing switching circuitry will turn on the isolation FET 420 and turn off the protection FET 430. At this time, voltage V_s is proportional to the on resistance R_{DSon} of the power FET 410 and the current through it. The circuit has a fast following capability and also a reasonable V to I linearity at a given temperature. Also, in a typical application, the peak sense voltage V_s could be in the range of 1 volt, providing good range, resolution and noise immunity compared to the few tens of mV in other architectures. This conventional arrangement falls short because of its nonlinearity due to temperature dependence of R_{DSon} of FET 410, which can be a large value as described hereinabove. Temperature variation, which is also dependent on load applied, will produce a large variation, even for a given current through the FET 410. A complex system may implement methods of calibration to reduce the error, but that process adds unwanted complexity and more cost.

[0009] Continuing improvements are desirable for methods and apparatus to provide current sensing in a power FET over a range of temperatures at a relatively low cost.

SUMMARY

[0010] In described examples, power FET is switched by a control circuit for implementing systems, such as power management or motor control systems. The power FET supplies current from an input voltage to a load that is coupled to an output terminal. At least a first isolation FET is coupled to the power FET and to a comparator amplifier. At least one current source is also connected to one of the comparator amplifier inputs and supplies a current in response to the

output of the comparator, creating a current output that fluctuates with the current in the power FET. The output current is related to the load current by a temperature independent proportion of ratio of the on resistances of the power FET and the at least one isolation FET. Co-locating the isolation FET on the same substrate as the power FET minimizes the differences due to any temperature mismatch. If the isolation FET is, in addition, of the same type as the power FET, mismatch effects due to process variations are also minimized.

[0011] In an example, an apparatus includes a power switch having a switch control input and having a current conduction path coupled between a voltage input and an output voltage terminal, configured for supplying current to a load responsive to a switch control signal coupled to the switch control input; a first isolation switch having a current conduction path coupled between the voltage input a first node, and having a control terminal coupled to an isolation switching control circuit; a comparator amplifier having a pair of differential inputs coupled to the first node and to a second node, and having at least one output, the comparator amplifier configured to output a voltage in response to the difference at the differential inputs; and a first current source coupled between a positive supply voltage and the first node, and configured to output a first current responsive to the voltage output from the comparator amplifier. The first current is proportional to the current through the power switch and to a ratio of the on resistance of the power switch and the on resistance of the first isolation switch.

[0012] In a further arrangement, the apparatus further includes a second isolation switch coupled between the output voltage terminal and the second node; and a second current source coupled between the positive supply voltage and the second node.

[0013] In yet another arrangement, the comparator amplifier further includes a second output voltage and the second current source supplies a current to the second node responsive to the second output voltage.

[0014] In still another arrangement, a difference between the first current and the second current is proportional to a current supplied through the power switch.

[0015] In still another arrangement, the power switch, the first isolation switch and the second isolation switch each include a field effect transistor (FET) formed of a common semiconductor material. In yet a further arrangement, the semiconductor material includes gallium nitride. In still another alternative arrangement, the semiconductor material includes silicon. In another alternative arrangement, the semiconductor material is one selected from the group consisting

essentially of silicon, silicon carbide, gallium arsenide, gallium nitride, indium arsenide, germanium, and silicon germanium. In yet a further arrangement, the power switch, the first isolation switch, and the second isolation switch each consist of GaN FET devices.

[0016] In another alternative arrangement, the first isolation switch and the second isolation switch includes transistors that are a same size. In still another arrangement, the apparatus further includes a second current source coupled between the first node and a negative power supply and supplying a second current from the first node. The second node of the comparator amplifier is coupled to the output voltage terminal, and a difference between the first current and the second current is proportional to the current through the power switch. In yet another alternative arrangement, the proportion is equal to a ratio of the on resistance of the power switch and the on resistance of the first isolation switch.

[0017] In another example, a method includes coupling a current conduction path of a power switch between an input voltage terminal and an output voltage terminal for supplying current to a load at the output voltage terminal, responsive to a switching control circuit; coupling a current conduction path of a first isolation switch between the input voltage terminal and a first node, and coupling a first current source between a positive voltage power supply and the first node, the first current source having a control input; coupling a comparator amplifier to the first node and to a second node, and coupling the output of the comparator amplifier to the control input of the first current source; operating the power switch to supply current to a load coupled to the voltage output terminal; operating the comparator to control the first current from the first current source; and using the first current, computing a load current through the power switch.

[0018] In a further method arrangement, the above-described method further includes coupling a second isolation switch between the voltage output terminal and the second node, and coupling a second current source between the positive voltage supply and the second node; coupling a second output of the comparator amplifier to control a second current supplied by the second current source to the second node; operating the power switch to supply current to a load coupled to the voltage output terminal; operating the comparator to control the first current and the second current; and computing a load current through the power switch by determining a difference between the first current and the second current. In still another example, the above-described method further includes coupling a second current source to the first node to supply a second current from the first node to a negative voltage supply; coupling the output

voltage terminal to the second node; operating the power switch to supply current to a load coupled to the output voltage terminal; operating the comparator to control the first current; and computing a load current through the power switch by determining a difference between the first current and the second current. In still a further arrangement, in the above-described method, the power switch and the first isolation switch are FET devices formed on a common semiconductor substrate.

[0019] In yet another example, an integrated circuit includes a semiconductor substrate; a power FET formed on the semiconductor substrate and having an input voltage terminal, a gate terminal coupled to a switch control circuit, and an output voltage terminal, the power FET configured to supply current to a load at the voltage output terminal; a first isolation FET formed on the semiconductor substrate and coupled between the input voltage terminal and a first node, and having a gate terminal coupled to an isolation control circuit; a comparator amplifier having a first differential input coupled to the first node and a second differential input, and configured to output a voltage corresponding to a difference between the voltages at the first differential input and the second differential input; and a first current source coupled between a positive voltage supply and the first node, configured to output a current responsive to the output voltage from the comparator amplifier. The current output from the first current source is proportional to the current through the power FET and a ratio of an on resistance of the power FET and an on resistance of the first isolation FET.

[0020] In still another arrangement, the integrated circuit includes a second isolation FET formed on the semiconductor substrate and coupled between the output voltage terminal and a second node; and a second current source coupled between the positive voltage supply and the second node to supply a second current to the second node; the second node coupled to the second differential input, and the comparator having a second output controlling the second current source. A difference between the first current and the second current is proportional to the current through the power switch multiplied by a ratio of the on resistance of the power FET and an on resistance of the first isolation FET.

[0021] In another alternative arrangement, the integrated circuit further includes a second current source coupled between the first node and a negative voltage supply and configured to supply a second current from the first node to the negative voltage supply; and the second differential input is coupled to the output voltage terminal. The difference between the first

current and the second current is proportional to the current through the power FET multiplied by a ratio of the on resistance of the power FET to an on resistance of the first isolation FET.

[0022] In yet another further arrangement, in the above-described integrated circuit, the semiconductor substrate is one of materials used for power devices, such as silicon, germanium, silicon carbide, gallium arsenide, silicon germanium, and gallium nitride.

[0023] Example embodiments enable sensing current through a power switch to a load with little temperature dependence.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] FIG. 1 is a circuit diagram of a conventional circuit for estimating load current from a power FET.

[0025] FIG. 2 is another circuit diagram of another conventional solution for temperature compensated load current sensing.

[0026] FIG. 3 is another circuit diagram of yet another conventional load current sensing arrangement.

[0027] FIG. 4 is a circuit diagram of a conventional current sensing topology.

[0028] FIG. 5 is a circuit schematic of an example arrangement using an aspect of example embodiments.

[0029] FIG. 6 is a graph of a power FET voltage V_{DSon} at 3 temperatures.

[0030] FIG. 7 is a graph illustrating the load current estimate of a power FET obtained using an example arrangement across a temperature range.

[0031] FIG. 8 is a circuit schematic that illustrates an alternative arrangement using another aspect of example embodiments.

[0032] FIG. 9 is a graph of the load current estimate of a power FET operated using an example arrangement across a temperature range.

[0033] FIG. 10 is a flow diagram depicting a method arrangement forming an aspect of example embodiments.

[0034] FIG. 11 is a second flow diagram depicting an alternative method arrangement forming another aspect of example embodiments.

[0035] FIG. 12 is a third flow diagram depicting another alternative method arrangement forming another aspect of example embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0036] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated.

[0037] When the term “coupled” is used herein to describe the relationships between elements, the term “coupled” includes “connected” or “directly connected,” and further includes connections made with intervening elements, so more elements and various connections may exist between any elements that are described as “coupled.”

[0038] In an aspect of example embodiments, an architecture reduces the temperature dependence current estimation from the drain to source voltage of a power transistor. Also, the example architecture and methods minimize effects of temperature and process variations to achieve a more accurate current ISENSE that is stable across a wide temperature range.

[0039] FIG. 5 shows a circuit schematic 500 of an arrangement using an aspect of example embodiments. In FIG. 5, power FET 510 is switched by control switching circuitry 512. Various forms of construction and operation are possible for the PWM/PFM switching circuitry. Power FET 510 is supplied by V_{in} and provides a load current I_{LOAD} to the load 590 at an output terminal V_{out} . Coupled to the drain/source terminals of power FET 510 are a pair of isolation FETs 520 and 524. The isolation FETs are switched by the isolation switching circuitry 522, shown as a circuit block. At node 535, isolation FET 520 is coupled to current source I_1 which is supplied by a positive voltage supply V_L . At node 537, isolation FET 524 is coupled to current source I_2 which is also supplied by voltage V_L . A comparator amplifier, which can be implemented using a differential operational amplifier (op amp) 526 has its inputs coupled to node 535 and 537. The differential outputs of the op amp 526 are coupled to the control inputs of current sources I_1 and I_2 . Current mirrors for I_1 and I_2 are coupled by their control and are designated as I_{1M} and I_{2M} and output currents I_{1out} , I_{2out} .

[0040] In circuit 500, isolation FETs 520 and 524 are assumed to be of the same size and located on the same substrate. In an example, circuit 500 can be a single integrated circuit including all of the circuit elements of FIG. 5; however, in more alternative arrangements, the FET devices 510, 520, 524 can be formed on an integrated circuit while other portions of the circuit 500 could be fabricated on a second integrated circuit. In one particular example, the power FET 510 and the isolation FETs 520 and 524 can be formed from Gallium Nitride (GaN) semiconductor material. In another alternative arrangement, the isolation FETs 520, 524 and

power FET 510 can be fabricated using silicon carbide (SiC) material. FET devices fabricated from GaN and/or SiC material are increasingly used in power applications because the material provides FETs allowing high-voltage hard-switched and soft switched converters to operate at higher frequencies. The material also provides converters with faster switching speeds and may enable reducing or eliminating heat sinks in some applications. In an example fabrication arrangement, GaN FETs can be formed in a semiconductor substrate implemented as an epitaxial layer of AlGaN material formed over a silicon or other substrate. For example, the circuit 500 can also be fabricated using FETs manufactured using silicon substrates, or other semiconductor materials and III-V material combinations such as gallium arsenide (GaAs), silicon germanium (SiGe), silicon carbide, germanium or other materials known for use in transistor manufacture. Epitaxial layers can be used to form the semiconductor material for the FET devices. The co-location of the FETs on a single substrate or semiconductor layer normalizes the processing variation and the thermal conditions that each of these components experiences regardless of the thermal constant of the device package. V_{in} is assumed to be greater than the breakdown voltage of the sense circuitry so the isolation switching ensures that the isolation FETs are only ON when the power FET 510 is ON. When the power FET is on, the voltage across the power FET's drain-source, V_{DSon} , is within the voltage tolerance of the sense circuitry. Various forms of construction and operation of the isolation switching circuitry are possible.

[0041] Analyzing the voltage V_{dson} across the power FET 510 yields the following relationships:

$$I_1 \times R_{ON} (520) + V_{DSon}(510) = I_2 \times R_{ON} (524) \quad \text{Equation 1}$$

$$V_{DSon}(510) = I_2 \times R_{ON} (524) - I_1 \times R_{ON} (520) \quad \text{Equation 1.1}$$

and because all the two isolation FETs are the same size and are co-located, R_{ON} can be assumed to be the same for FETs 520 and 524; and for $I_1, I_2 \ll I_{LOAD}$: $V_{DSon} (510) = R_{DSon} (510) \times I_{LOAD}$, so:

$$R_{DSon} (510) \times I_{LOAD} = I_2 \times R_{ON} - I_1 \times R_{ON} \quad \text{Equation 1.2}$$

rearranged as:

$$R_{DSon} (510) \times I_{LOAD} = (I_2 - I_1) \times R_{ON} \quad \text{Equation 1.3}$$

and solving for the load current:

$$I_{LOAD} = (I_2 - I_1) \times (R_{ON} \div R_{DSon}) \quad \text{Equation 1.4}$$

where the sense current $I_{SENSE} = (I_2 - I_1)$

$$I_{LOAD} = I_{SENSE} \times (R_{ON} \div R_{DSon}). \quad \text{Equation 1.5}$$

[0042] With the 3 FETs 510, 520 and 524, being co-located on a common semiconductor substrate, the on resistances change factor for the devices should be well matched across the temperature range. The change factor can be expressed as change from a nominal value, R_{nom} , as follows:

$$R_{nom} \times (1 + TC \times (T - T_{nom})) \quad \text{Equation 1.6}$$

[0043] In an example, the isolation transistors 520, 524 can be the same size as the power FET 510, because these isolation transistors are used only as sensing elements. In another example, these transistors will be smaller and perhaps much smaller than the power FET. The ratio of on resistances used in the arrangements divides quantities with an approximately equal or common temperature coefficient. When the ratio is taken as in Equation 1.5, the term $(R_{ON} \div R_{DSon})$ therefore cancels out the individual temperature coefficients and makes the estimate of the load current through the power FET independent of temperature, and proportional to the difference in the currents I_2 and I_1 . The current mirrors I_{2M} and I_{1M} can be used by the circuit designer to output these currents as currents I_{1out} and I_{2out} , so the circuitry can compute the load current and use the I_{LOAD} information as needed. An example use of the outputs is to determine the load current and feedback the information to the Control Switching block, so as to limit the amount of load current to a current value the power FET 510 can safely handle. However, the arrangements are not limited to this example application, and the current sensed through the FET 510 is useful for other purposes.

[0044] FIG. 6 presents a graph 600 of a power FET voltage V_{DSon} at 3 temperatures. Illustrated in FIG. 6 is a graph 600 with the FET voltage V_{DSon} plotted on the vertical axis and time plotted on the horizontal axis. In a simulated test of a power FET 510 such as shown in FIG. 5, two step loads were applied at 3 different temperatures in the time periods designated by 602 and 604. The lowest data line, 610 was simulated at 27C, the middle line 612 was simulated at 85C and the top line 614 was simulated at 125C. Because the FET has a positive TC, line 614 is expected to have a higher reading than the room temperature data line 610. The first test load varies across the time span 602 starting approximately at 1.5A and increasing to 5A. Looking at the 27C data line 610, V_{DSon} begins by dropping to approximately 0.2V then steadily rises to approximately 0.9V. The rising V_{DSon} voltage is illustrative of an increasing load current. During the second test, the test load is constant cross the time period 604 at approximately 5A.

Examining the 27C data line 610, the voltage V_{DSon} is pretty constant at approximately 0.9V. In 604, the high temperature data line 614 is steady at approximately 1.7V. Span 620 illustrates the approximately 90% rise in V_{DSon} over the approximate 100 degrees C temperature range. This high change in V_{DSon} over temperature illustrates why using the voltage V_{DSon} directly for an estimate of load current in the FET is an unreliable approach.

[0045] FIG. 7 is a graph of the load current estimate obtained using the arrangements for a power FET across a temperature range. In FIG. 7, a graph 700 presents increasing milliamp current on the Y axis and time on the X axis. Graph 700 illustrates the sensed current I_{SENSE} results using the same load test as shown in FIG. 6. The room temperature line 710 (27C) falls below the 85C data line 712 which falls below the 125C data line 714. During the first variable load pulse, shown in time span 702 corresponding to time span 602 in FIG. 6, the I_{SENSE} current between the 3 different temperatures is hardly distinguishable. However, the sloping line from approximately 1.5mA to 5mA is consistent with the increasing load current and corresponds to the increasing voltage V_{DSon} shown in time span 602 of FIG. 6. Looking at time span 704, which corresponds to time span 604 from FIG. 6, the data lines separate with the room temperature data 710 being the lowest at approximately 5.0mA and the high temperature at the highest level of approximately 5.2mA. The I_{SENSE} change due to temperature change is between 4% and 5% (which is a vast improvement to the 90% delta shown in V_{DSon}).

[0046] As shown by the graphs described hereinabove, by using the resistances of intrinsic circuit elements as in example embodiments, and in sharp contrast to the conventional approaches, no extra sensing resistors are required that reduce efficiency and which could introduce more temperature dependence.

[0047] In another arrangement that forms another aspect of example embodiments, a different amplifier was used in simulation. Substituting a higher gain and slower op amp results in an I_{SENSE} change of less than 0.1%. However, a higher gain op amp takes longer to settle and results in a slower response time, which limits the frequency response to the load current. Various amplifiers are useful to implement the comparator amplifiers of the arrangements according to the needs of a particular application.

[0048] FIG. 8 shows another circuit schematic of a circuit 800 using another aspect of example embodiments. In a system with a negative power supply available, a simplified circuit arrangement can be employed that requires only two FETs, the power FET and a single isolation

FET. In FIG. 8, a power FET 810 is switched by Control Switching circuitry 812, shown as a circuit block. Various forms of construction and operation of the control/PWM switching circuitry are possible. When switched on, power FET 810 is supplied by input voltage V_{in} and provides load current I_{LOAD} 814 to the load 890 at an output voltage terminal V_{out} . Coupled to the source terminal of power FET 810 is an isolation transistor FET 820. The isolation FET is switched by the isolation switching circuitry 822, shown as a circuit block. At node 835, isolation FET 820 is coupled to current source I_1 which is supplied by a positive voltage supply V_L . An op amp 826 has its inputs coupled to node 835 and the output voltage terminal V_{out} . V_{out} is a node between the power FET 810 and the Load 890. A second current source I_2 is connected to node 835 and to a negative voltage supply terminal V_{NEG} . The output of the op amp 826 is coupled to the control line of current source I_1 and the mirror current source I_{1M} . In this arrangement, the second current source does not require a control terminal but provides a predetermined current I_2 from the first node to the negative power supply.

[0049] In FIG. 8, in circuit 800, the power FET 810 and isolation FET 820 are assumed to be of the same transistor type and are formed and located on the same semiconductor substrate. In one arrangement, all of the circuit components of circuit 800 can be provided on a single integrated circuit. However, in alternative arrangements, the FETs 810 and 820 can be formed on an integrated circuit, while other components of circuit 800 can be formed on other integrated circuits or provided as discrete components. The co-location of the FETs 810, 820 on a common semiconductor substrate or layer normalizes processing variations and the thermal conditions that each of these components experiences. The input voltage V_{in} is assumed to exceed the breakdown voltage of the sense circuitry, so the isolation switching ensures that the isolation FET 820 is ON only when the power FET 810 is ON. Also, as another feature of the arrangements, the isolation switching can be used to turn off FET 820 when current sensing is not required, to save power. When the power FET 810 is on, the voltage across the power FET's drain-source current conduction path, V_{DSon} , is within the voltage tolerance of the sense circuitry. Various forms of construction and operation of the isolation switching circuitry are possible.

[0050] Analyzing the voltage across the power FET 810 yields the following relationships :

$$(I_1 - I_2) \times R_{ON}(820) = -V_{DSon}(810) \quad \text{Equation 2}$$

$$V_{DSon}(810) = (I_2 - I_1) \times R_{ON}(820) \quad \text{Equation 2.1}$$

and for $I_1, I_2 \ll I_{LOAD}$: $V_{DSon} (810) = R_{DSon} (810) \times I_{LOAD}$, so:

$$R_{DSon} (810) \times I_{LOAD} = (I_2 - I_1) \times R_{ON} (820)) \quad \text{Equation 2.3}$$

and solving for the load current:

$$I_{LOAD} = (I_2 - I_1) \times (R_{ON} \div R_{DSon}) \quad \text{Equation 2.4}$$

where the differential sense current $I_{SENSE} = (I_2 - I_1)$,

$$I_{LOAD} = I_{SENSE} \times (R_{ON} \div R_{DSon}) \quad \text{Equation 2.5}$$

which is the same relationship that results from circuit 500 in a conventional arrangement.

[0051] With FETs 810 and 820 being the same type and co-located, the R_{DSon} change factor as shown in Equation 1.6 hereinabove for the two devices will be well matched across the temperature range. The term $(R_{ON} \div R_{DSon})$ therefore cancels out the temperature coefficients for the on resistances of the transistors and makes the estimate of the load current independent of temperature, and proportional to a difference in the currents I_2 and I_1 . The current mirror I1M can be used by the designer to output I_1 . Because the current I_2 in circuit 800 is known, the difference $I_1 - I_2$ can be computed and used for calculating I_{LOAD} . In at least one example, I_{LOAD} information is useful as feedback to the Control/PWM Switching block 812, so as to limit the amount of load current to a value that the power FET 810 can safely handle. Also, more applications can also be formed.

[0052] FIG. 9 is a graph of the load current estimate obtained using the example arrangement of FIG. 8 for a power FET across a temperature range. Using the same test loads at the same test temperatures as shown in FIG. 6, FIG. 9 illustrates the stability of the sensed current I_{SENSE} across the temperature range of the tests from 27C to 125C. In FIG. 9, graph 900 is shown with increasing current in milliamps on the vertical or Y axis and time on the horizontal or X axis, and illustrates the I_{SENSE} measurement results of the load test shown in FIG. 6. The room temperature line 910 (27C) falls below the 85C data line 912 which falls below the 125C data line 914. In this simulated test, a standard Op Amp with high open loop gain (OLG) of approximately 50,000 was used as the comparator amplifier. During the first variable load pulse, shown in time span 902 which corresponds to the time span 602 in FIG. 6, the current differential between the 3 temperatures is hardly distinguishable, except in the settling period following time span 902. However, the sloping line from approximately -4.0mA to 1mA is consistent with the increasing load and corresponds to the increasing voltage V_{DSon} shown in time span 602 of FIG. 6. Looking at time span 904, which corresponds to time span 604 from

FIG. 6, the data lines again are nearly indistinguishable except in the settling period following time span 904. The ISENSE change due to temperature is less than 0.05% (which is a vast improvement to the 90% delta shown in VDSon).

[0053] Graph 900 illustrates that by using the resistances of intrinsic circuit elements as in the example arrangements, the load current can be accurately sensed, and no extra resistors are required that reduce efficiency and which could reintroduce more temperature dependence.

[0054] FIG. 10 is a flow diagram illustrating a method arrangement 1000 for operating a power FET and sensing the load current. In the method arrangement, the method begins at step 1001. In step 1003, a power FET is switched on to supply current to a load from an input voltage. In step 1005, an isolation transistor is coupled between an input voltage and a first node. In step 1007, a first current source is coupled to the first node. In step 1009, a comparator amplifier is coupled to the first node and the output of the comparator is coupled to control the first current source. In step 1011, the comparator is operated to control the first current. In step 1013, the load current through the power FET can be determined using the first current and a ratio of the on resistance of the power FET and the on resistance of the first isolation transistor. Because the ratio is used, temperature dependence of the transistor is removed from the calculation.

[0055] FIG. 11 is a flow diagram of the steps for an alternative method arrangement 1100. The method begins at block 1101, start. In step 1103, a power FET is coupled to supply current to a load from an input voltage. In step 1105, a first isolation transistor is coupled between the input voltage and the first node, and a first current source coupled between the power supply and the first node. In step 1107, a second isolation FET is coupled between the load and a second node, and a second current source is coupled between a power supply and the second node. In step 1109, the two current sources are controlled by the differential outputs from a comparator coupled to the first node and the second node. In step 1111, the current through the power FET is determined using the difference between the two currents and a ratio of the on resistance of the FET and the on resistance of one of the isolation FETs, as described hereinabove.

[0056] FIG. 12 depicts still another method arrangement 1200. In this method a negative power supply is available. The method 1200 begins at step 1201, start. At step 1203, the power FET is coupled between an input voltage terminal and an output voltage terminal to supply current to a load at the output terminal. At step 1205, a first isolation FET is coupled between the input voltage and a first node, and a first current source is coupled between a positive power

supply and the first node. In step 1207, a second current source is coupled between the first node and a negative voltage supply. At step 1209, a comparator amplifier is coupled to the first node and the output voltage terminal that supplies the load is coupled to the second differential input of the comparator amplifier. The power FET is switched on to supply current to a load. At step 1209 the comparator amplifier is operated to control the first current. At step 1211, the current through the power FET can be calculated using a difference between the first current and second current and a ratio of the on resistance of the power FET and the on resistance of the first isolation transistor, as described hereinabove.

[0057] Various modifications can also be made in the order of steps and in the number of steps to form more arrangements.

[0058] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

a power switch having a switch control input and having a current conduction path coupled between a voltage input and an output voltage terminal, configured for supplying current to a load responsive to a switch control signal coupled to the switch control input;

a first isolation switch having a current conduction path coupled between the voltage input a first node, and having a control terminal coupled to an isolation switching control circuit;

a comparator amplifier having a pair of differential inputs coupled to the first node and to a second node, and having at least one output, the comparator amplifier configured to output a voltage in response to the difference at the differential inputs; and

a first current source coupled between a positive supply voltage and the first node, and configured to output a first current responsive to the voltage output from the comparator amplifier;

wherein the first current is proportional to the current through the power switch and to a ratio of the on resistance of the power switch and the on resistance of the first isolation switch.

2. The apparatus of claim 1, further comprising:

a second isolation switch coupled between the output voltage terminal and the second node; and

a second current source coupled between the positive supply voltage and the second node.

3. The apparatus of claim 2, wherein the comparator amplifier further comprises a second output voltage, and the second current source supplies a current to the second node responsive to the second output voltage.

4. The apparatus of claim 3, wherein a difference between the first current and the second current is proportional to a current supplied through the power switch.

5. The apparatus of claim 2, wherein the power switch, the first isolation switch and the second isolation switch each comprise a field effect transistor (FET) formed of a common semiconductor material.

6. The apparatus of claim 5, wherein the semiconductor material comprises gallium nitride.

7. The apparatus of claim 5, wherein the semiconductor material is one selected from the

group consisting essentially of silicon, silicon carbide, gallium arsenide, gallium nitride, indium arsenide, germanium, and silicon germanium.

8. The apparatus of claim 2, wherein the power switch, the first isolation switch, and the second isolation switch each comprise GaN FET devices.

9. The apparatus of claim 2, wherein the first isolation switch and the second isolation switch comprise transistors that have a same size.

10. The apparatus of claim 1, further comprising:

a second current source coupled between the first node and a negative power supply and supplying a second current from the first node;

wherein the second node of the comparator amplifier is coupled to the output voltage terminal, and a difference between the first current and the second current is proportional to the current through the power switch.

11. The apparatus of claim 10, wherein the first current is proportional to the current through the power switch multiplied by a ratio of the on resistance of the power switch and the on resistance of the first isolation switch.

12. A method, comprising:

coupling a current conduction path of a power switch between an input voltage terminal and an output voltage terminal for supplying current to a load at the output voltage terminal, responsive to a switching control circuit;

coupling a current conduction path of a first isolation switch between the input voltage terminal and a first node, and coupling a first current source between a positive voltage power supply and the first node, the first current source having a control input;

coupling a comparator amplifier to the first node and to a second node, and coupling the output of the comparator amplifier to the control input of the first current source;

operating the power switch to supply current to a load coupled to the voltage output terminal;

operating the comparator to control the first current from the first current source; and

using the first current, computing a load current through the power switch, where the first current is proportional to the load current through the power switch and a ratio of an on resistance of the power switch and an on resistance of the first isolation switch.

13. The method of claim 12, further comprising:

coupling a second isolation switch between the voltage output terminal and the second node, and coupling a second current source between the positive voltage supply and the second node;

coupling a second output of the comparator amplifier to control a second current supplied by the second current source to the second node;

operating the power switch to supply current to a load coupled to the voltage output terminal;

operating the comparator to control the first current and the second current; and

computing a load current through the power switch by determining a difference between the first current and the second current. .

14. The method of claim 12, further comprising:

coupling a second current source to the first node to supply a second current from the first node to a negative voltage supply;

coupling the output voltage terminal to the second node;

operating the power switch to supply current to a load coupled to the output voltage terminal;

operating the comparator to control the first current; and

computing a load current through the power switch by determining a difference between the first current and the second current and multiplying the difference by a ratio of the on resistance of the power switch and the on resistance of the first isolation switch.

15. The method of claim 12, wherein the power switch and the first isolation switch are FET devices formed on a common semiconductor substrate.

16. The method of claim 15, wherein the common semiconductor substrate is formed from one selected from the group consisting essentially of silicon, silicon carbide, silicon germanium, germanium, gallium, gallium nitride, and gallium arsenide.

17. An integrated circuit, comprising:

a semiconductor substrate;

a power FET formed on the semiconductor substrate and having an input voltage terminal, a gate terminal coupled to a switch control circuit, and an output voltage terminal, the power FET configured to supply current to a load at the voltage output terminal;

a first isolation FET formed on the semiconductor substrate and coupled between the

input voltage terminal and a first node, and having a gate terminal coupled to an isolation control circuit;

a comparator amplifier having a first differential input coupled to the first node and a second differential input, and configured to output a voltage corresponding to a difference between the voltages at the first differential input and the second differential input; and

a first current source coupled between a positive voltage supply and the first node, configured to output a current responsive to the output voltage from the comparator amplifier;

wherein the current output from the first current source is proportional to the current through the power FET and a ratio of an on resistance of the power FET and an on resistance of the first isolation FET.

18. The integrated circuit of claim 17, further comprising:

a second isolation FET formed on the semiconductor substrate and coupled between the output voltage terminal and a second node; and

a second current source coupled between the positive voltage supply and the second node to supply a second current to the second node;

the second node coupled to the second differential input, and the comparator having a second output controlling the second current source;

wherein a difference between the first current and the second current is proportional to the current through the power switch multiplied by a ratio of the on resistance of the power FET and an on resistance of the first isolation FET.

19. The integrated circuit of claim 17, further comprising:

a second current source coupled between the first node and a negative voltage supply and configured to supply a second current from the first node to the negative voltage supply; and

the second differential input is coupled to the output voltage terminal;

wherein a the difference between the first current and the second current is proportional to the current through the power FET multiplied by a ratio of the on resistance of the power FET to an on resistance of the first isolation FET.

20. The integrated circuit of claim 17 wherein the semiconductor substrate is one selected from the group consisting essentially of silicon, silicon carbide, germanium, gallium arsenide, silicon germanium, and gallium nitride.

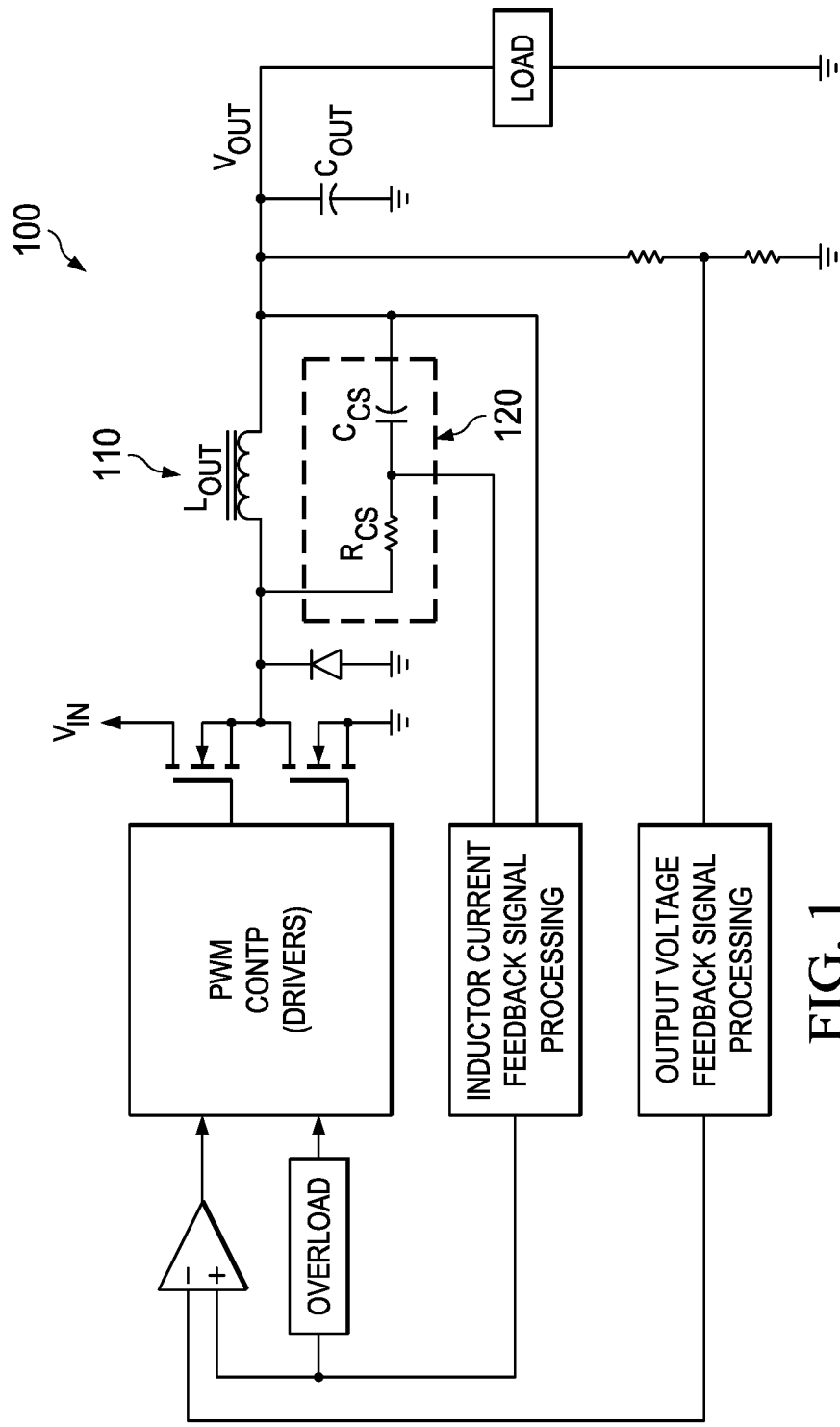


FIG. 1
(PRIOR ART)

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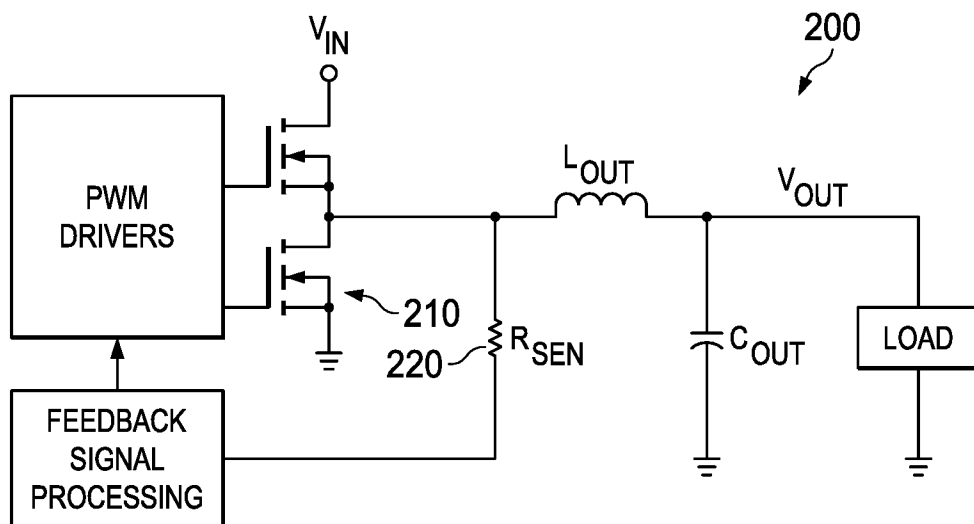


FIG. 2
(PRIOR ART)

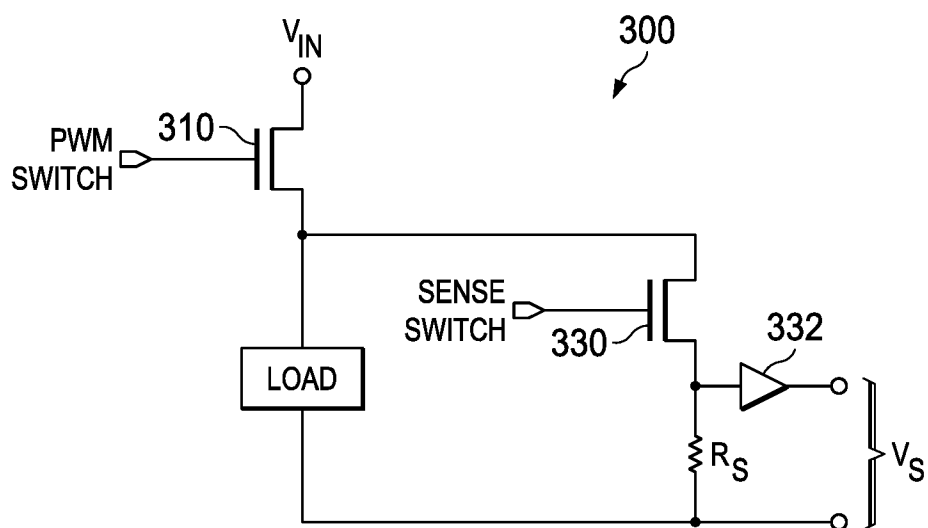


FIG. 3
(PRIOR ART)

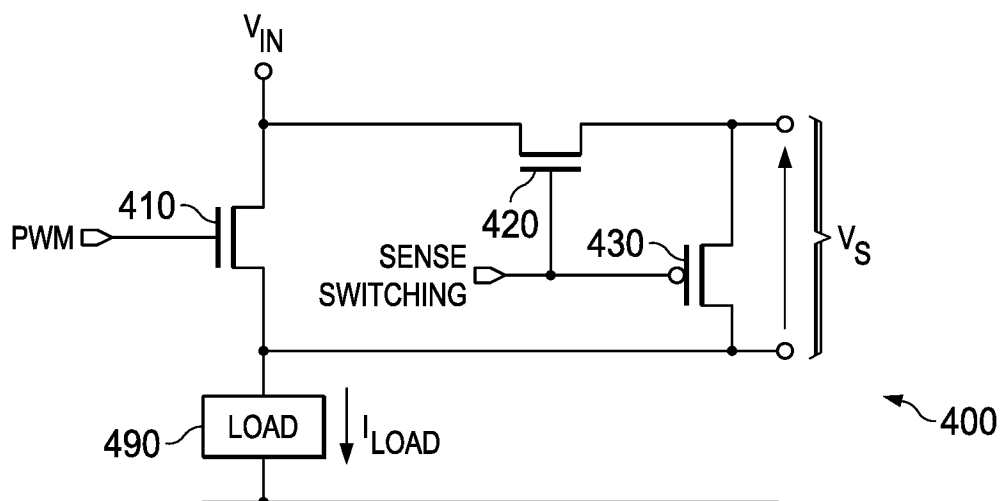
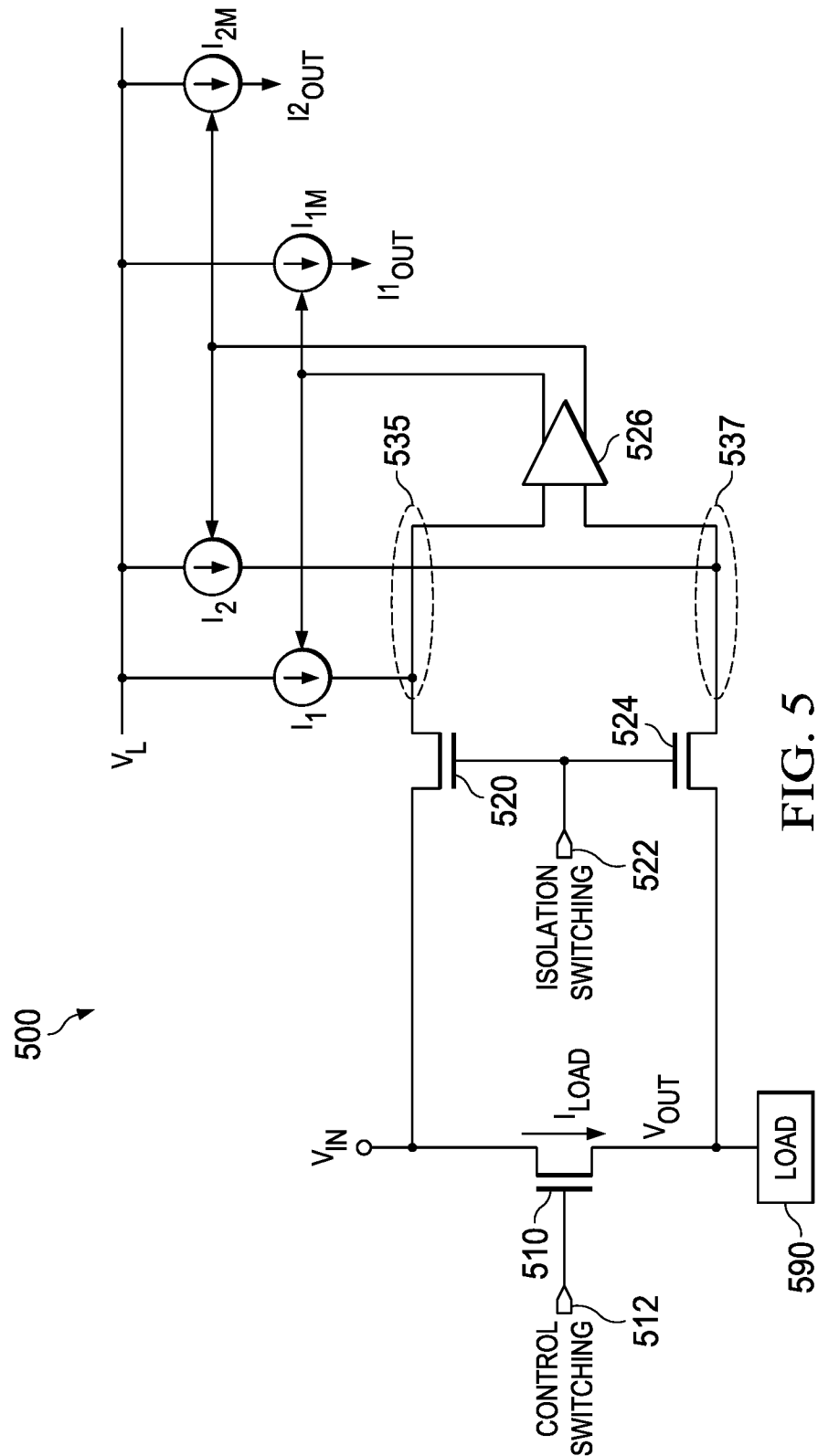


FIG. 4
(PRIOR ART)



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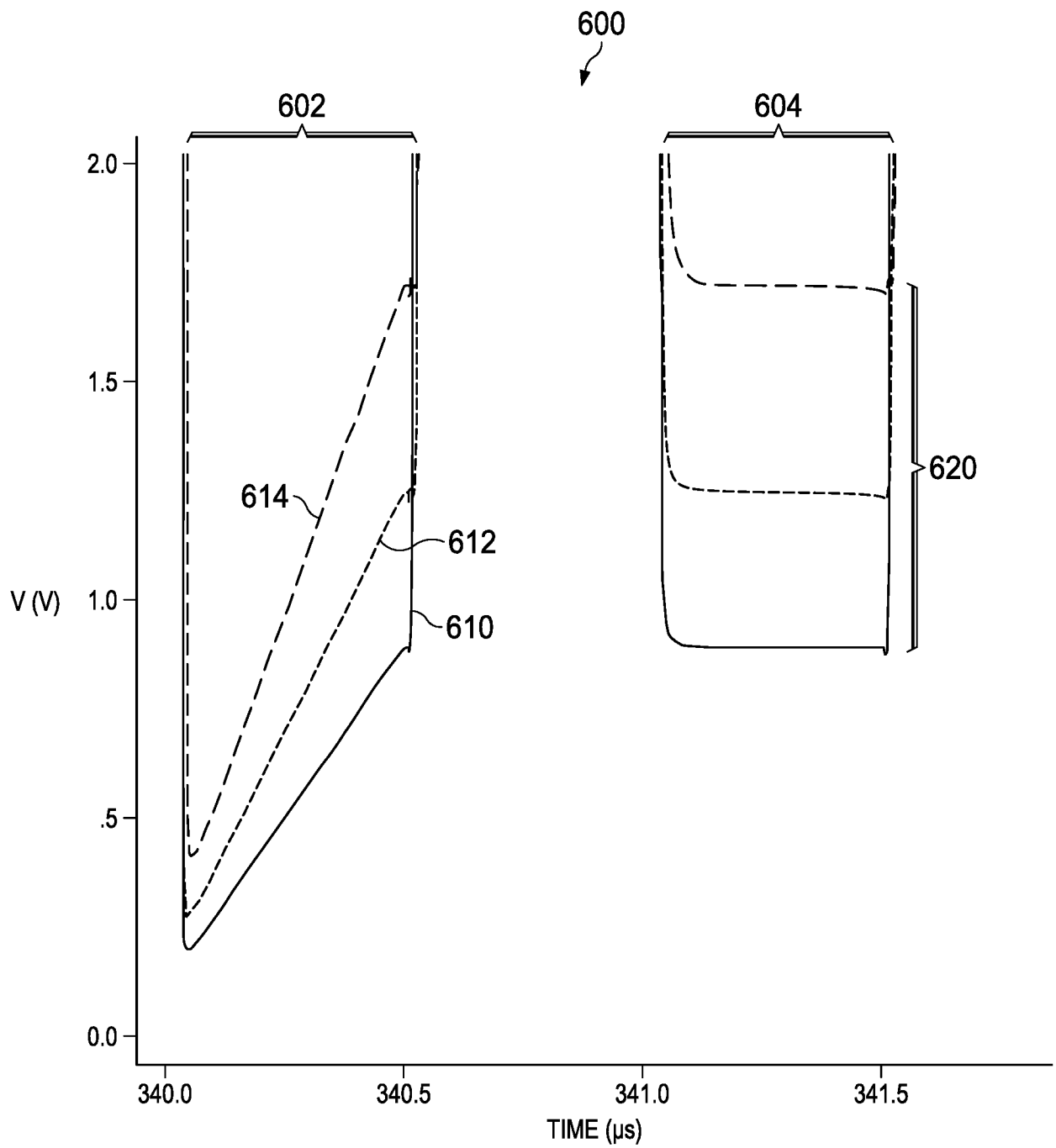


FIG. 6

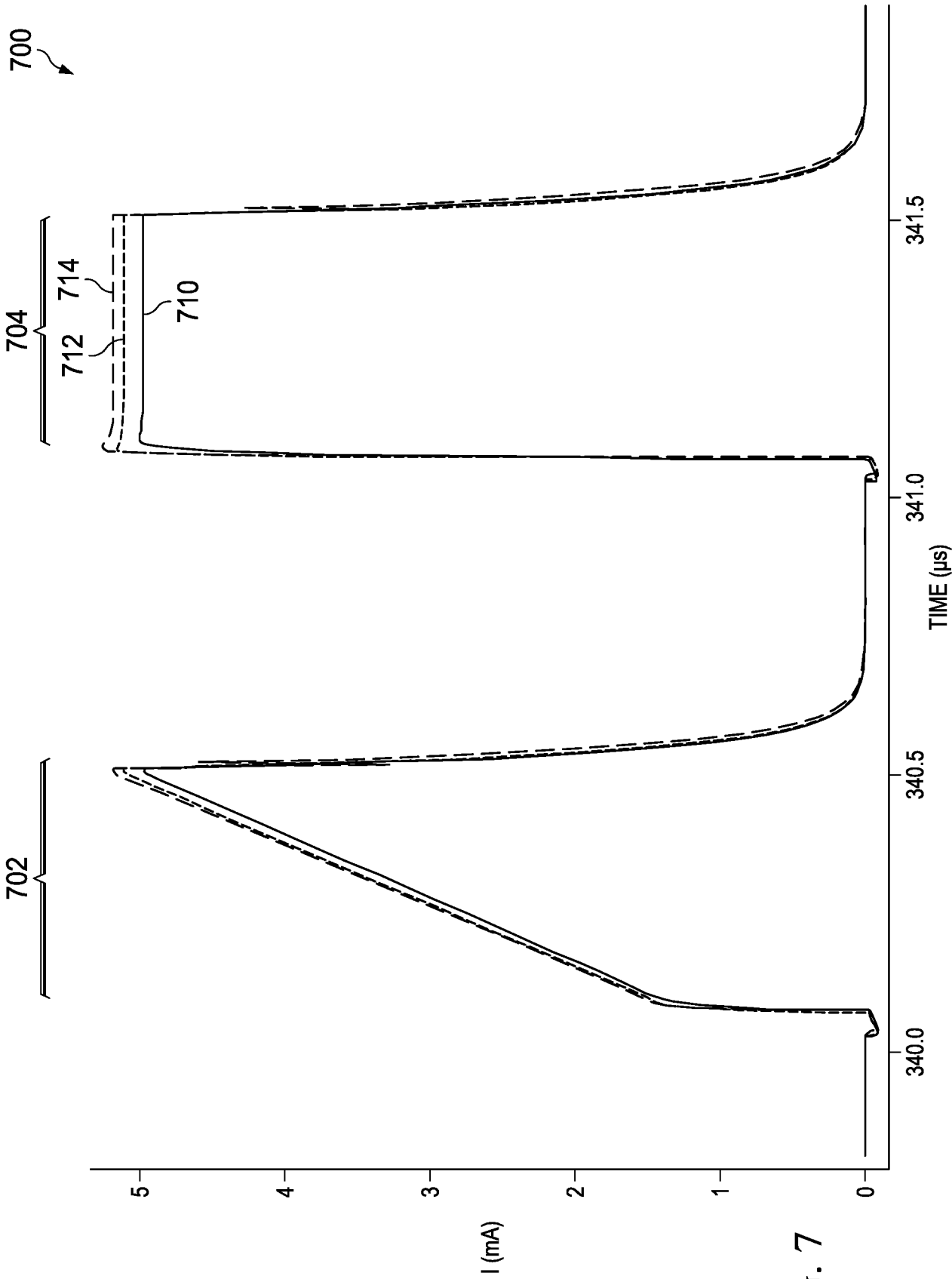
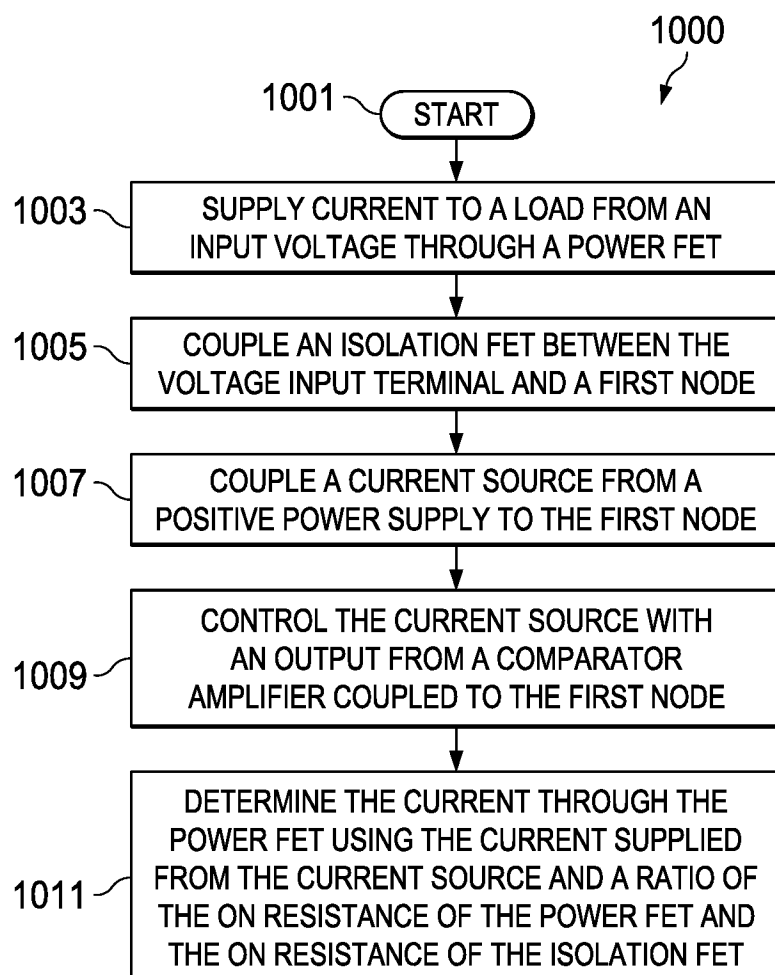
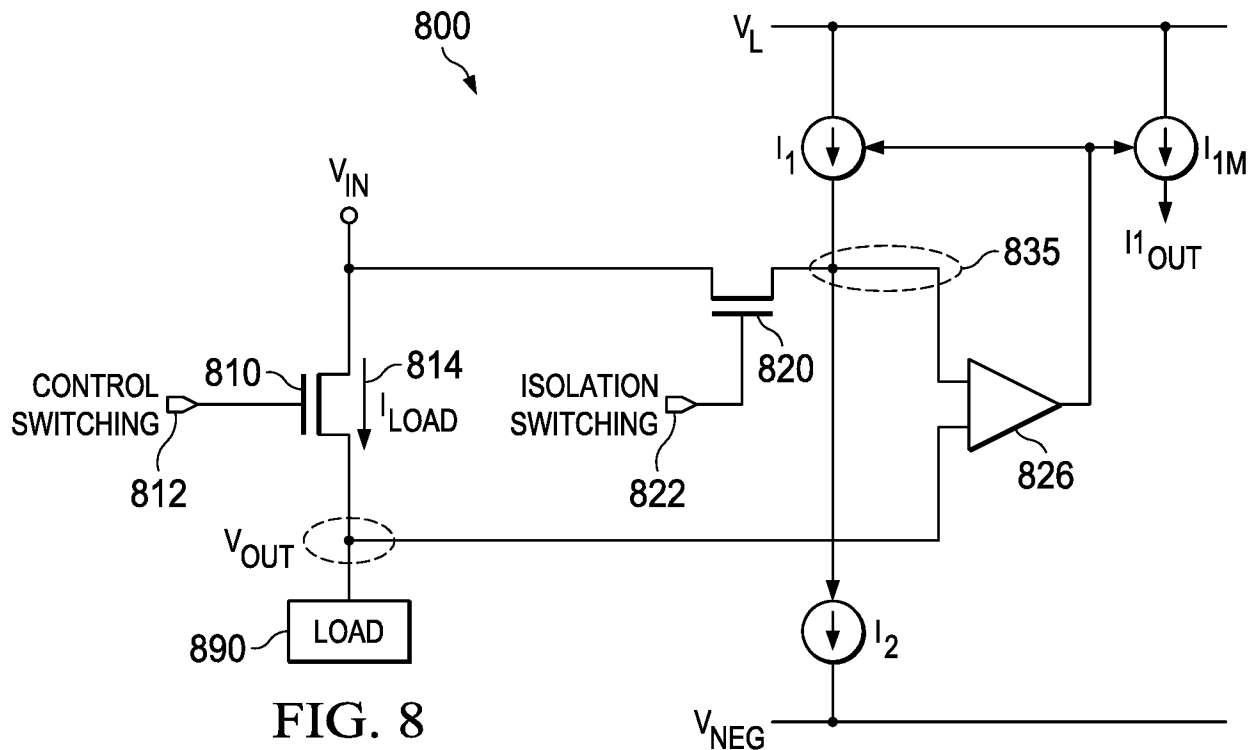


FIG. 7

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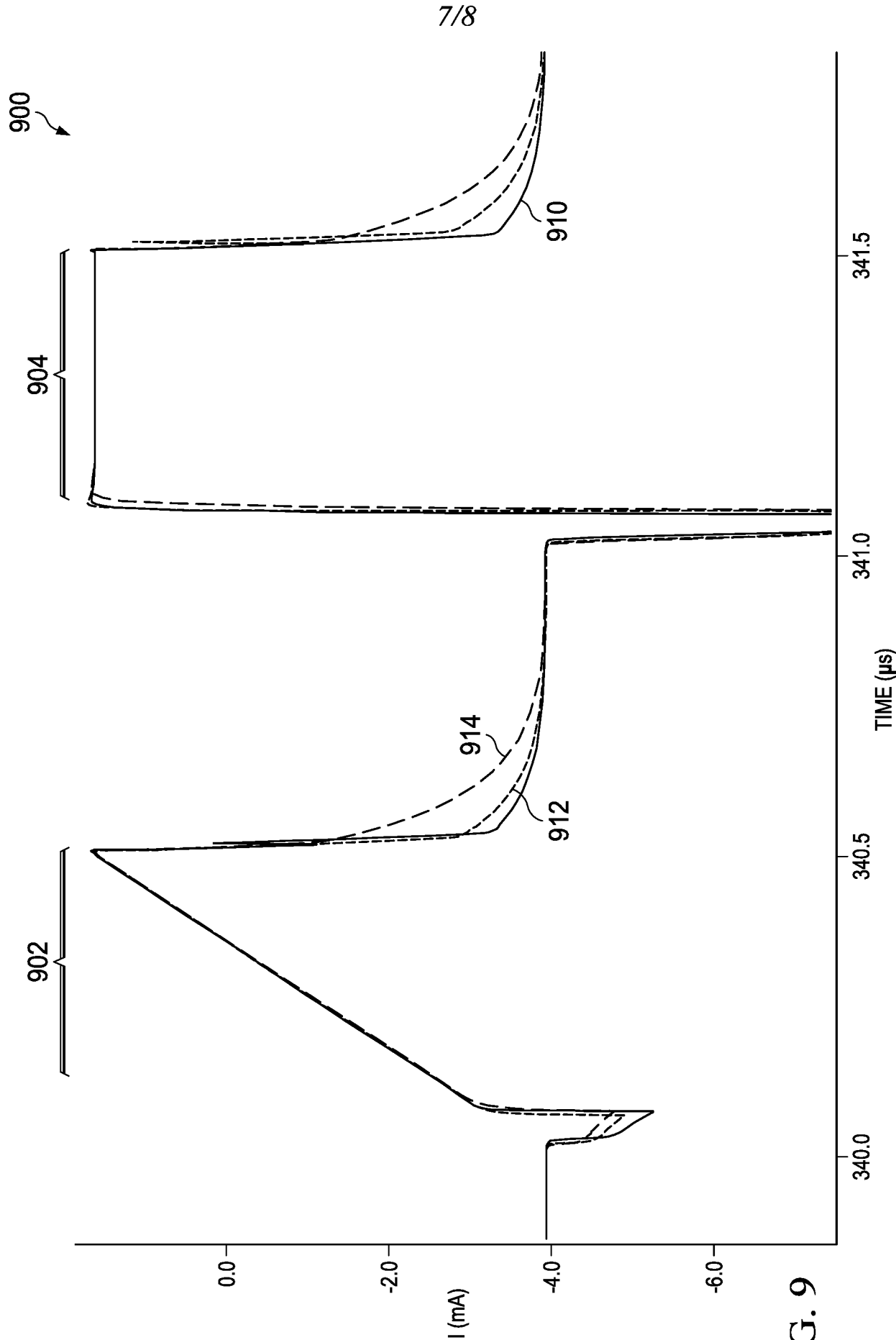


FIG. 9

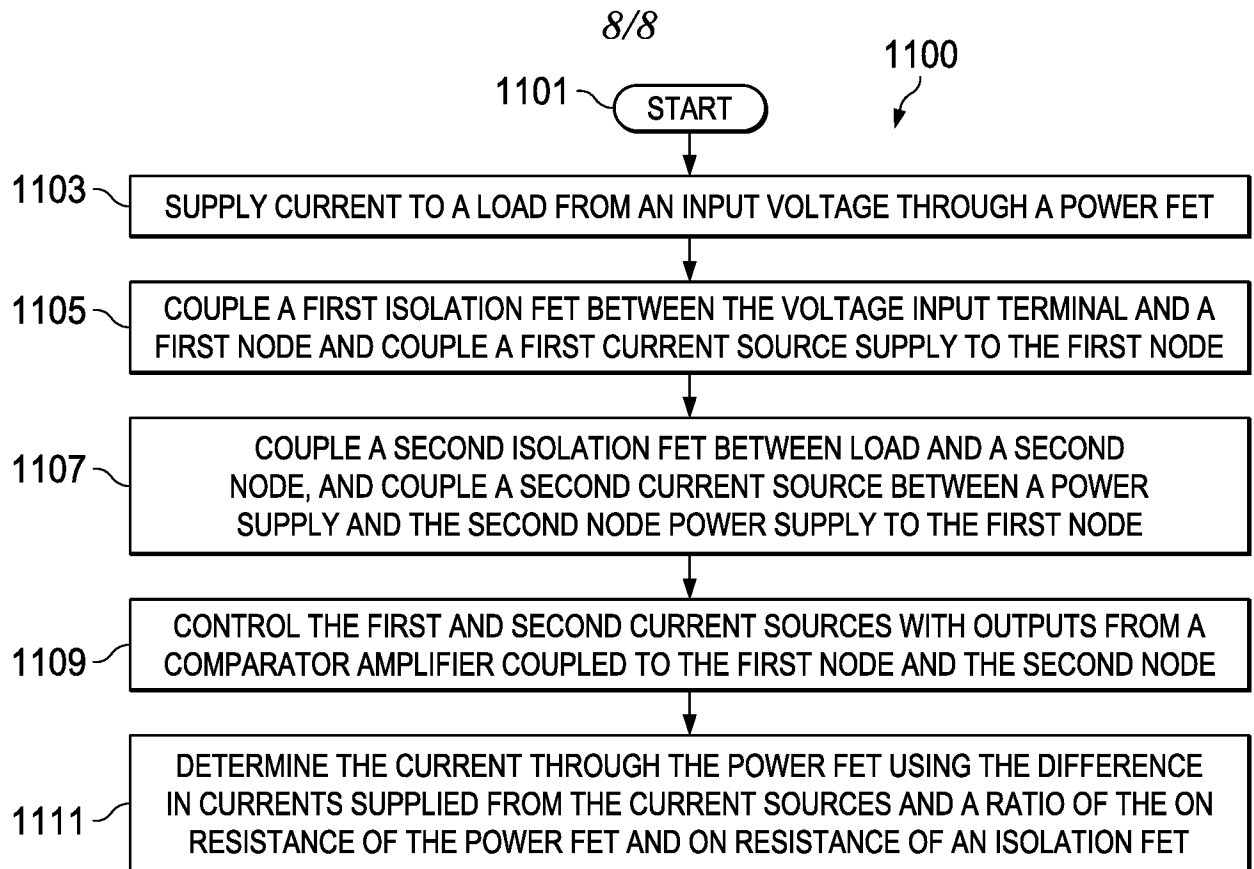


FIG. 11

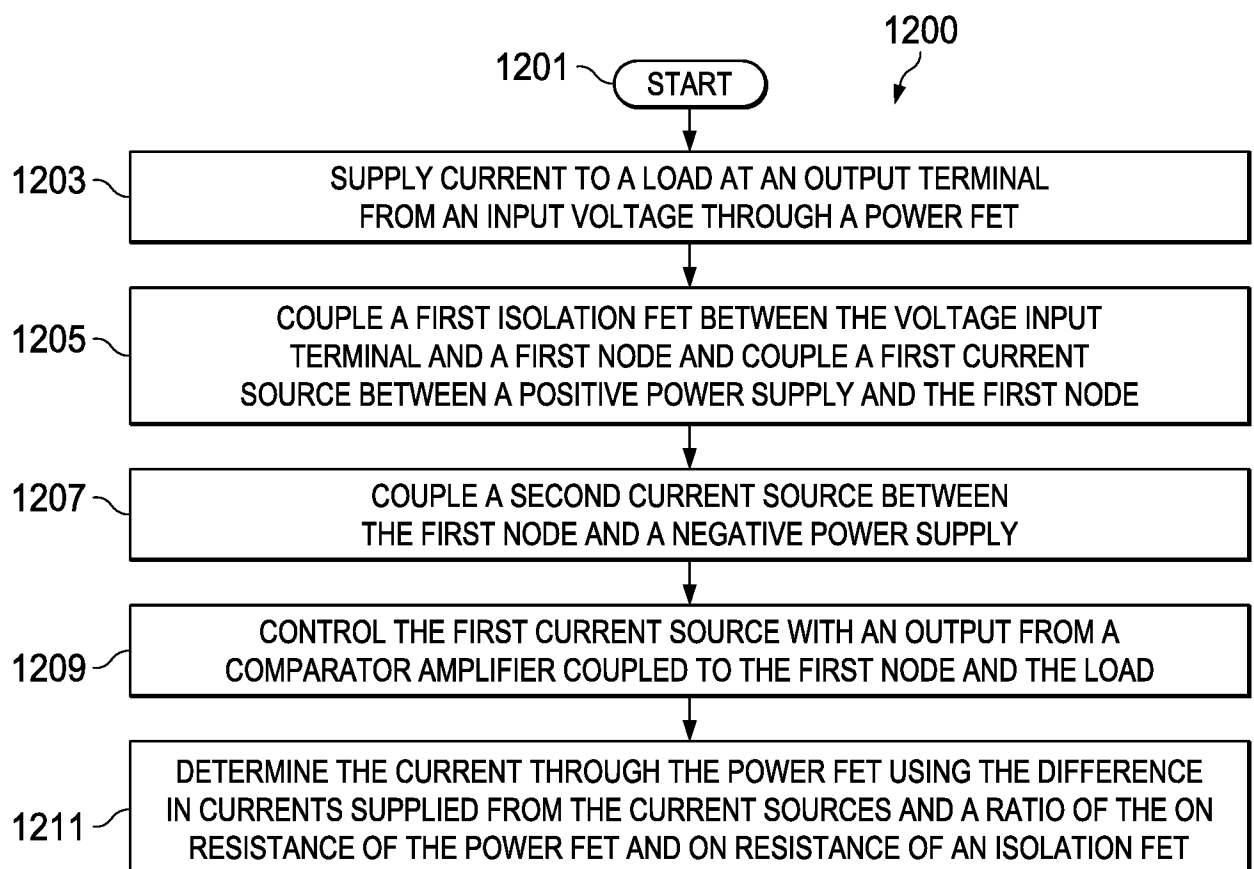


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2017/013503

A. CLASSIFICATION OF SUBJECT MATTER		
<i>G01R 19/00 (2006.01)</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
G01R 19/00, G05F 1/10, H02M 3/156, 3/155, H02M 1/08		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
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C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2015/195717 A1 (ENDURA TECHNOLOGIES LLC) 23.12.2015	1-20
A	US 5654880 A1 (CALIFORNIA INSTITUTE OF TECHNOLOGY) 05.08.1997	1-20
A	US 2008/0018387 A1 (TAKASHI RYU) 24.01.2008	1-20
A	US 2012/0119715 A1 (MIKKO T.LOIKKANEN) 17.05.2012	1-20
A	SU 1597874 A1 (V.I.ANISIMOV et al.) 07.10.1990	1-20
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"O" document referring to an oral disclosure, use, exhibition or other means		
"P" document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search	Date of mailing of the international search report	
15 March 2017 (15.03.2017)	06 April 2017 (06.04.2017)	
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer M. Markov Telephone No. (499) 240-25-91	