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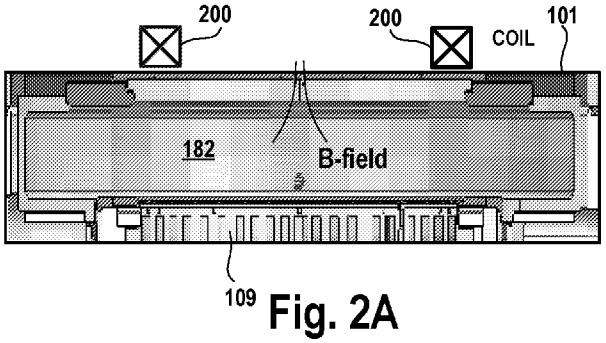

Fig. 2A

(57) **Abstract:** A system for performing a plasma process on a wafer is provided, including: a chamber configured to receive a wafer for plasma processing and having an interior defining a plasma processing region in which a plasma is provided for the plasma processing of the wafer; a first magnetic coil disposed above the chamber and centered about an axis perpendicular to a surface plane of the wafer and through an approximate center of the wafer; a first DC power supply configured to apply a first DC current to the first magnetic coil during the plasma processing, the applied first DC current producing a magnetic field in the plasma processing region that reduces non-uniformity of the plasma.

WO 2022/108753 A1

Plasma Uniformity Control Using a Static Magnetic Field

Background

1. Field of the Disclosure

[0001] The present disclosure relates to semiconductor device fabrication.

2. Description of the Related Art

[0002] Plasma etching processes are often used in the manufacture of semiconductor devices on semiconductor wafers. In the plasma etching process, a semiconductor wafer that includes semiconductor devices under manufacture is exposed to a plasma generated within a plasma processing volume. The plasma interacts with material(s) on the semiconductor wafer so as to remove material(s) from the semiconductor wafer and/or modify material(s) to enable their subsequent removal from the semiconductor wafer. The plasma can be generated using specific reactant gases that will cause constituents of the plasma to interact with the material(s) to be removed/modified from the semiconductor wafer, without significantly interacting with other materials on the wafer that are not to be removed/modified. The plasma is generated by using radiofrequency signals to energize the specific reactant gases. These radiofrequency signals are transmitted through the plasma processing volume that contains the reactant gases, with the semiconductor wafer held in exposure to the plasma processing volume. The transmission paths of the radiofrequency signals through the plasma processing volume can affect how the plasma is generated within the plasma processing volume. For example, the reactant gases may be energized to a greater extent in regions of the plasma processing volume where larger amounts of radiofrequency signal power is transmitted, thereby causing spatial non-uniformities in the plasma characteristics throughout the plasma processing volume. The spatial non-uniformities in plasma characteristics can manifest as spatial non-uniformity in ion density, ion energy, and/or reactive constituent density, among other plasma characteristics. The spatial non-uniformities in plasma characteristics can correspondingly cause spatial non-uniformities in plasma processing results on the semiconductor wafer. Therefore, the manner in which radiofrequency signals are transmitted through the plasma processing volume can have an effect on the uniformity of plasma processing results on the semiconductor wafer. It is within this context that the present disclosure arises.

Summary

[0003] Broadly speaking, embodiments of the present disclosure provide methods and systems for plasma uniformity control using a static magnetic field.

[0004] In some implementations, a system for performing a plasma process on a wafer is provided, including: a chamber configured to receive a wafer for plasma processing and having an interior defining a plasma processing region in which a plasma is provided for the plasma

processing of the wafer; a first magnetic coil disposed above the chamber and centered about an axis perpendicular to a surface plane of the wafer and through an approximate center of the wafer; a first DC power supply configured to apply a first DC current to the first magnetic coil during the plasma processing, the applied first DC current producing a magnetic field in the plasma processing region that reduces non-uniformity of the plasma.

[0005] In some implementations, the magnetic field is configured to be substantially vertical through a central region of the plasma processing region.

[0006] In some implementations, the magnetic field through the central region of the plasma processing region has a strength that is less than approximately 10 Gauss.

[0007] In some implementations, the magnetic field is configured to reduce a radial non-uniformity of etching that is performed by the plasma processing.

[0008] In some implementations, the first magnetic coil is substantially annular in shape.

[0009] In some implementations, the first magnetic coil is oriented along a horizontal plane parallel to the surface plane of the wafer.

[0010] In some implementations, an inner diameter of the first magnetic coil is in the range of approximately 15 to 20 inches.

[0011] In some implementations, the first magnetic coil includes a plurality of turns of magnet wire.

[0012] In some implementations, the system further includes: a second magnetic coil disposed above the chamber, the second magnetic coil being concentric with the first magnetic coil; a second DC power supply configured to apply a second DC current to the second magnetic coil during the plasma processing, the applied second DC current contributing to producing the magnetic field in the plasma processing region that reduces non-uniformity of the plasma.

[0013] In some implementations, the second magnetic coil is substantially oriented along a same horizontal plane as the first magnetic coil.

[0014] In some implementations, the first DC current and the second DC current are configured to have a same magnitude or a different magnitude.

[0015] In some implementations, the first DC current and the second DC current are configured to be applied in a same direction or in opposite directions.

[0016] In some implementations, an inner diameter of the first magnetic coil is in the range of approximately 10 to 15 inches; and, an inner diameter of the second magnetic coil is in the range of approximately 15 to 25 inches.

[0017] In some implementations, the system further includes: a second magnetic coil configured to laterally surround the plasma processing region; a second DC power supply configured to apply a second DC current to the second magnetic coil during the plasma processing, the applied

second DC current contributing to producing the magnetic field in the plasma processing region that reduces non-uniformity of the plasma.

[0018] In some implementations, the system further includes: a second magnetic coil disposed below the plasma processing region; a second DC power supply configured to apply a second DC current to the second magnetic coil during the plasma processing, the applied second DC current contributing to producing the magnetic field in the plasma processing region that reduces non-uniformity of the plasma.

[0019] In some implementations, a method for performing a plasma process on a wafer is provided, including: moving a wafer into a chamber configured for plasma processing, an interior of the chamber defining a plasma processing region; providing a plasma in the plasma processing region for the plasma processing of the wafer; and applying a DC current to a magnetic coil during the plasma processing, the applied DC current producing a magnetic field in the plasma processing region that reduces non-uniformity of the plasma;

[0020] wherein the magnetic coil is disposed above the chamber and centered about an axis perpendicular to a surface plane of the wafer and through an approximate center of the wafer.

[0021] In some implementations, the magnetic field is configured to be substantially vertical through a central region of the plasma processing region.

[0022] In some implementations, the magnetic field through the central region of the plasma processing region has a strength that is less than approximately 10 Gauss.

[0023] In some implementations, the magnetic field is configured to reduce a radial non-uniformity of etching that is performed by the plasma processing.

[0024] In some implementations, the magnetic coil is substantially annular in shape.

[0025] In some implementations, the magnetic coil is oriented along a horizontal plane parallel to the surface plane of the wafer.

[0026] In some implementations, an inner diameter of the first magnetic coil is in the range of approximately 15 to 20 inches.

Brief Description of the Drawings

[0027] Figure 1 shows a vertical cross-section view through a plasma processing system for use in semiconductor chip manufacturing, in accordance with some embodiments.

[0028] Figure 2A conceptually illustrates a cross-section of a process chamber having a single magnetic coil for applying a magnetic field during plasma processing, in accordance with implementations of the disclosure.

[0029] Figure 2B conceptually illustrates a cross-section of a process chamber having two magnetic coils for applying a magnetic field during plasma processing, in accordance with implementations of the disclosure.

[0030] Figure 2C conceptually illustrates a cross-section of a process chamber having three magnetic coils for applying a magnetic field during plasma processing, in accordance with implementations of the disclosure.

[0031] Figure 2D conceptually illustrates a cross-section of a process chamber having four magnetic coils for applying a magnetic field during plasma processing, in accordance with implementations of the disclosure.

[0032] Figure 3A is a graph illustrating etch rate results for a continuous wave plasma under different applied B-fields, in accordance with implementations of the disclosure.

[0033] Figure 3B is a graph illustrating the change in etch rate that is effected by the applied B-field, in accordance with the implementation of Figure 3A.

[0034] Figure 4A is a graph illustrating etch rate as a function of wafer radius for a plasma process with different applied B-fields, in accordance with implementations of the disclosure.

[0035] Figure 4B is a graph showing the change in etch rate as a result of applied B-fields, in accordance with the implementation of Figure 4A.

[0036] Figure 5 shows cross-section images of portions of wafers having etched features thereon, demonstrating the effect of an applied B-field on feature tilting, in accordance with implementations of the disclosure.

[0037] Figure 6A illustrates magnetic field strength at the wafer level in the z-direction (vertical direction, or perpendicular to the wafer surface) versus radial position along a 300mm diameter wafer, for various single coil current configurations, in accordance with implementations of the disclosure.

[0038] Figure 6B illustrates magnetic field strength at the wafer level in the radial direction (in Gauss) versus radial position along a 300mm diameter wafer, for various single coil current configurations, in accordance with the implementations of Figure 6A.

[0039] Figure 7A is a graph illustrating thermal oxide etch rate versus radial position along a 300mm wafer, for various positive currents (counterclockwise) applied to single coils A (12”), B (14”), C (17”), and D (23”), in accordance with implementations of the disclosure.

[0040] Figure 7B is a graph illustrating thermal oxide etch rate versus radial position along a 300mm wafer, for various negative currents (clockwise) applied to single coils A (12”), B (14”), C (17”), and D (23”), in accordance with implementations of the disclosure.

[0041] Figure 8A illustrates magnetic field strength at the wafer level in the z-direction (vertical direction, or perpendicular to the wafer surface) versus radial position along a 300mm diameter wafer, for various two-coil current configurations, in accordance with implementations of the disclosure.

[0042] Figure 8B illustrates magnetic field strength at the wafer level in the radial direction (in

Gauss) versus radial position along a 300mm diameter wafer, for various two-coil current configurations, in accordance with the implementations of Figure 8A.

[0043] Figure 9A illustrates magnetic field strength at the wafer level in the z-direction (vertical direction, or perpendicular to the wafer surface) versus radial position along a 300mm diameter wafer, for various three-coil current configurations, in accordance with implementations of the disclosure.

[0044] Figure 9B illustrates magnetic field strength at the wafer level in the radial direction (in Gauss) versus radial position along a 300mm diameter wafer, for various three-coil current configurations, in accordance with the implementations of Figure 9A.

[0045] Figure 10A is a graph illustrating etch rate as a function of radial position along a 300 mm wafer, for a two coil combination, in accordance with implementations of the disclosure.

[0046] Figure 10B is a graph illustrating the etch rate delta as compared to a zero current condition, in accordance with the implementations of Figure 10A.

[0047] Figure 11 is a conceptual schematic diagram of a system for controlling power to multiple magnetic coils, in accordance with implementations of the disclosure.

[0048] Figure 12 shows an example schematic of the control system of Figure 1, in accordance with some embodiments.

Detailed Description

[0049] In the following description, numerous specific details are set forth in order to provide an understanding of embodiments of the present disclosure. It will be apparent, however, to one skilled in the art that the present disclosure may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present disclosure.

[0050] In plasma etching systems for semiconductor wafer fabrication, spatial variation of etching results across the semiconductor wafer can be characterized by radial etch uniformity and azimuthal etch uniformity. Radial etch uniformity can be characterized by the variation in etch rate as a function of radial position on the semiconductor wafer, extending outward from the center of the semiconductor wafer to the edge of the semiconductor wafer at a given azimuthal position on the semiconductor wafer. And, azimuthal etch uniformity can be characterized by the variation in etch rate as a function of azimuthal position on the semiconductor wafer, about the center of the semiconductor wafer, at a given radial position on the semiconductor wafer. In some plasma processing systems, such as in the system described herein, the semiconductor wafer is positioned on an electrode from which radiofrequency signals emanate to generate a plasma within a plasma generation region overlying the semiconductor wafer, with the plasma having characteristics controlled to cause a prescribed etching process to

occur on the semiconductor wafer.

[0051] In capacitive coupled plasma (CCP) systems, there is a tendency to exhibit center plasma non-uniformity due to standing waves and localized accumulation of positive and negative ions. This results in radial non-uniformity of etch rate. For example, many CCP tools may exhibit dramatic increases in etch rate towards the center of the wafer.

[0052] Furthermore, there is tool-to-tool variation with respect to radial non-uniformity. Some tools may exhibit significant spikes in etch rate at the center, whereas other tools may not. Often this is correlated to the presence or absence of magnetic fields, as the flux from chamber parts, which may vary in configuration from tool to tool, differs. Further, the local environment or specific location of a given tool, and surrounding hardware, may affect the local magnetic fields which are present, and which in turn affect etch radial non-uniformity.

[0053] In view of the foregoing problems in existing CCP systems, some implementations of the disclosure provide for the application of a static B-field to the plasma to minimize localized charged species accumulation and improve plasma/etch uniformity across the wafer.

[0054] In some implementations, a pulsed magnetic field is applied to create a time-varying radial gradient of B-field to control radial electron diffusion, and, therefore, radial negative and positive ion acoustic waves.

[0055] Figure 1 shows a vertical cross-section view through a plasma processing system 100 for use in semiconductor chip manufacturing, in accordance with some embodiments. The system 100 includes a chamber 101 formed by walls 101A, a top member 101B, and a bottom member 101C. The walls 101A, top member 101B, and bottom member 101C collectively form an interior region 103 within the chamber 101. The bottom member 101C includes an exhaust port 105 through which exhaust gases from plasma processing operations are directed. In some embodiments, during operation, a suction force is applied at the exhaust port 105, such as by a turbo pump or other vacuum device, to draw process exhaust gases out of the interior region 103 of the chamber 101. In some embodiments, the chamber 101 is formed of aluminum. However, in various embodiments, the chamber 101 can be formed of essentially any material that provides sufficient mechanical strength, acceptable thermal performance, and is chemically compatible with the other materials to which it interfaces and to which it is exposed during plasma processing operations within the chamber 101, such as stainless steel, among others. At least one wall 101A of the chamber 101 includes a door 107 through which a semiconductor wafer W is transferred into and out of the chamber 101. In some embodiments, the door 107 is configured as a slit-valve door.

[0056] In some embodiments, the semiconductor wafer W is a semiconductor wafer undergoing a fabrication procedure. For ease of discussion, the semiconductor wafer W is referred to as

wafer W hereafter. However, it should be understood that in various embodiments, the wafer W can be essentially any type of substrate that is subjected to a plasma-based fabrication process. For example, in some embodiments, the wafer W as referred to herein can be a substrate formed of silicon, sapphire, GaN, GaAs or SiC, or other substrate materials, and can include glass panels/substrates, metal foils, metal sheets, polymer materials, or the like. Also, in various embodiments, the wafer W as referred to herein may vary in form, shape, and/or size. For example, in some embodiments, the wafer W referred to herein may correspond to a circular-shaped semiconductor wafer on which integrated circuit devices are manufactured. In various embodiments, the circular-shaped wafer W can have a diameter of 200 mm (millimeters), 300 mm, 450 mm, or of another size. Also, in some embodiments, the wafer W referred to herein may correspond to a non-circular substrate, such as a rectangular substrate for a flat panel display, or the like, among other shapes.

[0057] The plasma processing system 100 includes an electrode 109 positioned on a facilities plate 111. In some embodiments, the electrode 109 and the facilities plate 111 are formed of aluminum. However, in other embodiments, the electrode 109 and the facilities plate 111 can be formed of another electrically conductive material that has sufficient mechanical strength and that has compatible thermal and chemical performance characteristics. A ceramic layer 110 is formed on a top surface of the electrode 109. The ceramic layer 110 is configured to receive and support the wafer W during performance of plasma processing operations on the wafer W. In some embodiments, the top surface of the electrode 190 that is located radially outside of the ceramic layer 110 and the peripheral side surfaces of the electrode 109 are covered with a spray coat of ceramic.

[0058] The ceramic layer 110 includes an arrangement of one or more clamp electrodes 112 for generating an electrostatic force to hold the wafer W to the top surface of the ceramic layer 110. In some embodiments, the ceramic layer 110 includes an arrangement of two clamp electrodes 112 that operate in a bipolar manner to provide a clamping force to the wafer W. The clamp electrodes 112 are connected to a direct current (DC) supply 117 that generates a controlled clamping voltage to hold the wafer W against the top surface of the ceramic layer 110. Electrical wires 119A, 119B are connected between the DC supply 117 and the facilities plate 111. Electrical wires/conductors are routed through the facilities plate 111 and the electrode 109 to electrically connect the wires 119A, 119B to the clamp electrodes 112. The DC supply 117 is connected to a control system 120 through one or more signal conductors 121.

[0059] The electrode 109 also includes an arrangement of temperature control fluid channels 123 through which a temperature control fluid is flowed to control a temperature of the electrode 109 and in turn control a temperature of the wafer W. The temperature control fluid channels

123 are plumbed (fluidly connected) to ports on the facilities plate 111. Temperature control fluid supply and return lines are connected to these ports on the facilities plate 111 and to a temperature control fluid circulation system 125, as indicated by arrow 126. The temperature control fluid circulation system 125 includes a temperature control fluid supply, a temperature control fluid pump, and a heat exchanger, among other devices, to provide a controlled flow of temperature control fluid through the electrode 109 in order to obtain and maintain a prescribed wafer W temperature. The temperature control fluid circulation system 125 is connected to the control system 120 through one or more signal conductors 127. In various embodiments, various types of temperature control fluid can be used, such as water or a refrigerant liquid/gas. Also, in some embodiments, the temperature control fluid channels 123 are configured to enable spatially varying control of the temperature of the wafer W, such as in two dimensions (x and y) across the wafer W.

[0060] The ceramic layer 110 also includes an arrangement of backside gas supply ports (not shown) that are fluidly connected to corresponding backside gas supply channels within the electrode 109. The backside gas supply channels within the electrode 109 are routed through the electrode 109 to the interface between the electrode 109 and the facilities plate 111. One or more backside gas supply line(s) are connected to ports on the facilities plate 111 and to a backside gas supply system 129, as indicated by arrow 130. The facilities plate 111 is configured to supply the backside gas(es) from the one or more backside gas supply line(s) to the backside gas supply channels within the electrode 109. The backside gas supply system 129 includes a backside gas supply, a mass flow controller, and a flow control valve, among other devices, to provide a controlled flow of backside gas through the arrangement of backside gas supply ports in the ceramic layer 110. In some embodiments, the backside gas supply system 129 also includes one or more components for controlling a temperature of the backside gas. In some embodiments, the backside gas is helium. Also, in some embodiments, the backside gas supply system 129 can be used to supply clean dry air (CDA) to the arrangement of backside gas supply ports in the ceramic layer 110. The backside gas supply system 129 is connected to the control system 120 through one or more signal conductors 131.

[0061] Three lift pins 132 extend through the facilities plate 111, the electrode 109, and the ceramic layer 110 to provide for vertical movement of the wafer W relative to the top surface of the ceramic layer 110. In some embodiments, vertical movement of the lift pins 132 is controlled by a respective electromechanical and/or pneumatic lifting device 133 connected to the facilities plate 111. The three lifting devices 133 are connected to the control system 120 through one or more signal conductors 134. In some embodiments, the three lift pins 132 are positioned to have a substantially equal azimuthal spacing about a vertical centerline of the electrode 109/ceramic

layer 110 that extends perpendicular to the top surface of the ceramic layer 110. It should be understood that the lift pins 132 are raised to receive the wafer W into the chamber 101 and to remove the wafer W from the chamber 101. Also, the lift pins 132 are lowered to allow the wafer W to rest on the top surface of the ceramic layer 110 during processing of the wafer W.

[0062] Also, in various embodiments, one or more of the electrode 109, the facilities plate 111, the ceramic layer 110, the clamp electrodes 112, the lift pins 132, or essentially any other component associated therewith can be equipped to include one or more sensors, such as sensors for temperature measurement, electrical voltage measurement, and electrical current measurement, among others. Any sensor disposed within the electrode 109, the facilities plate 111, the ceramic layer 110, the clamp electrodes 112, the lift pins 132, or essentially any other component associated therewith is connected to the control system 120 by way of electrical wire, optical fiber, or through a wireless connection.

[0063] The facilities plate 111 is set within an opening of a ceramic support 113, and is supported by the ceramic support 113. The ceramic support 113 is positioned on a supporting surface 114 of a cantilever arm assembly 115. In some embodiments, the ceramic support 113 has a substantially annular shape, such that the ceramic support 113 substantially circumscribes the outer radial perimeter of the facilities plate 111, while also providing a supporting surface 116 upon which a bottom outer peripheral surface of the facilities plate 111 rests. The cantilever arm assembly 115 extends through the wall 101A of the chamber 101. In some embodiments, a sealing mechanism 135 is provided within the wall 101A of the chamber 101 where the cantilever arm assembly 115 is located to provide for sealing of the interior region 103 of the chamber 101, while also enabling the cantilever arm assembly 115 to move upward and downward in the z-direction in a controlled manner.

[0064] The cantilever arm assembly 115 has an open region 118 through which various devices, wires, cables, and tubing is routed to support operations of the system 100. The open region 118 within the cantilever arm assembly is exposed to ambient atmospheric conditions outside of the chamber 101, e.g. air composition, temperature, pressure, and relative humidity. Also, a radiofrequency signal supply rod 137 is positioned inside of the cantilever arm assembly 115. More specifically, the radiofrequency signal supply rod 137 is positioned inside of an electrically conductive tube 139, such that the radiofrequency signal supply rod 137 is spaced apart from the inner wall of the tube 139. The sizes of the radiofrequency signal supply rod 137 and the tube 139 may vary. The region inside of the tube 139 between the inner wall of the tube 139 and the radiofrequency signal supply rod 137 is occupied by air along the full length of the tube 139.

[0065] In some embodiments, the radiofrequency signal supply rod 137 is substantially centered

within the tube 139, such that a substantially uniform radial thickness of air exists between the radiofrequency signal supply rod 137 and the inner wall of the tube 139, along the length of tube 139. However, in some embodiments, the radiofrequency signal supply rod 137 is not centered within the tube 139, but the air gap within the tube 139 exists at all locations between the radiofrequency signal supply rod 137 and the inner wall of the tube 139, along the length of the tube 139. A delivery end of the radiofrequency signal supply rod 137 is electrically and physically connected to a lower end of a radiofrequency signal supply shaft 141. In some embodiments, the delivery end of the radiofrequency signal supply rod 137 is bolted to a lower end of a radiofrequency signal supply shaft 141. An upper end of the radiofrequency signal supply shaft 141 is electrically and physically connected to the bottom of the facilities plate 111. In some embodiments, the upper end of the radiofrequency signal supply shaft 141 is bolted to the bottom of the facilities plate 111. In some embodiments, both the radiofrequency signal supply rod 137 and the radiofrequency signal supply shaft 141 are formed of copper. In some embodiments, the radiofrequency signal supply rod 137 is formed of copper, or aluminum, or anodized aluminum. In some embodiments, the radiofrequency signal supply shaft 141 is formed of copper, or aluminum, or anodized aluminum. In other embodiments, the radiofrequency signal supply rod 137 and/or the radiofrequency signal supply shaft 141 is formed of another electrically conductive material that provides for transmission of radiofrequency electrical signals. In some embodiments, the radiofrequency signal supply rod 137 and/or the radiofrequency signal supply shaft 141 is coated with an electrically conductive material (such as silver or another electrically conductive material) that provides for transmission of radiofrequency electrical signals. Also, in some embodiments, the radiofrequency signal supply rod 137 is a solid rod. However, in other embodiments, the radiofrequency signal supply rod 137 is a tube. Also, it should be understood that a region 140 surrounding the connection between the radiofrequency signal supply rod 137 and the radiofrequency signal supply shaft 141 is occupied by air.

[0066] A supply end of the radiofrequency signal supply rod 137 is connected electrically and physically to an impedance matching system 143. The impedance matching system 143 is connected to a first radiofrequency signal generator 147 and a second radiofrequency signal generator 149. The impedance matching system 143 is also connected to the control system 120 through one or more signal conductors 144. The first radiofrequency signal generator 147 is also connected to the control system 120 through one or more signal conductors 148. The second radiofrequency signal generator 149 is also connected to the control system 120 through one or more signal conductors 150. The impedance matching system 143 includes an arrangement of inductors and capacitors sized and connected to provide for impedance matching so that

radiofrequency power can be transmitted along the radiofrequency signal supply rod 137, along the radiofrequency signal supply shaft 141, through the facilities plate 111, through the electrode 109, and into a plasma processing region 182 above the ceramic layer 110. In some embodiments, the first radiofrequency signal generator 147 is a high frequency radiofrequency signal generator, and the second radiofrequency signal generator 149 is a low frequency radiofrequency signal generator. In some embodiments, the first radiofrequency signal generator 147 generates radiofrequency signals within a range extending from about 50 MegaHertz (MHz) to about 70 MHz, or within a range extending from about 54 MHz to about 63 MHz, or at about 60 MHz. In some embodiments, the first radiofrequency signal generator 147 supplies radiofrequency power within a range extending from about 5 kiloWatts (kW) to about 25 kW, or within a range extending from about 10 kW to about 20 kW, or within a range extending from about 15 kW to about 20 kW, or of about 10 kW, or of about 16 kW. In some embodiments, the second radiofrequency signal generator 149 generates radiofrequency signals within a range extending from about 50 kiloHertz (kHz) to about 500 kHz, or within a range extending from about 330 kHz to about 440 kHz, or at about 400 kHz. In some embodiments, the second radiofrequency signal generator 149 supplies radiofrequency power within a range extending from about 15 kW to about 100 kW, or within a range extending from about 30 kW to about 50 kW, or of about 34 kW, or of about 50 kW. In an example embodiment, the first radiofrequency signal generator 147 is set to generate radiofrequency signals having a frequency of about 60 MHz, and the second radiofrequency signal generator 149 is set to generate radiofrequency signals having a frequency of about 400 kHz.

[0067] A coupling ring 161 is configured and positioned to extend around the outer radial perimeter of the electrode 109. In some embodiments, the coupling ring 161 is formed of a ceramic material. A quartz ring 163 is configured and positioned to extend around the outer radial perimeters of both the coupling ring 161 and the ceramic support 113. In some embodiments, the coupling ring 161 and the quartz ring 163 are configured to have substantially aligned top surfaces when the quartz ring 163 is positioned around both the coupling ring 161 and the ceramic support 113. Also, in some embodiments, the substantially aligned top surfaces of the coupling ring 161 and the quartz ring 163 are substantially aligned with a top surface of the electrode 109, said top surface being present outside of the radial perimeter of the ceramic layer 110. Also, in some embodiments, a cover ring 165 is configured and positioned to extend around the outer radial perimeter of the top surface of the quartz ring 163. In some embodiments, the cover ring 165 is formed of quartz. In some embodiments, the cover ring 165 is configured to extend vertically above the top surface of the quartz ring 163. In this manner, the cover ring 165 provides a peripheral boundary within which an edge ring 167 is positioned.

[0068] The edge ring 167 is configured to facilitate extension of the plasma sheath radially outward beyond the peripheral edge of the wafer W to provide improvement in process results near the periphery of the wafer W. In various embodiments, the edge ring 167 is formed of a conductive material, such as crystalline silicon, polycrystalline silicon (polysilicon), boron doped single crystalline silicon, aluminum oxide, quartz, aluminum nitride, silicon nitride, silicon carbide, or a silicon carbide layer on top of an aluminum oxide layer, or an alloy of silicon, or a combination thereof, among other materials. It should be understood that the edge ring 167 is formed as an annular-shaped structure, e.g. as a ring-shaped structure. The edge ring 167 can perform many functions, including shielding components underlying the edge ring 167 from being damaged by ions of a plasma 180 formed within a plasma processing region 182. Also, the edge ring 167 improves uniformity of the plasma 180 at and along the outer peripheral region of the wafer W.

[0069] A fixed outer support flange 169 is attached to the cantilever arm assembly 115. The fixed outer support flange 169 is configured to extend around an outer vertical side surface of the ceramic support 113, and around an outer vertical side surface of the quartz ring 163, and around a lower outer vertical side surface of the cover ring 165. The fixed outer support flange 169 has an annular shape that circumscribes the assembly of the ceramic support 113, the quartz ring 163, and the cover ring 165. The fixed outer support flange 169 has an L-shaped vertical cross-section that includes a vertical portion and a horizontal portion. The vertical portion of the L-shaped cross-section of the fixed outer support flange 169 has an inner vertical surface that is positioned against the outer vertical side surface of the ceramic support 113, and against the outer vertical side surface of the quartz ring 163, and against the lower outer vertical side surface of the cover ring 165. In some embodiments, the vertical portion of the L-shaped cross-section of the fixed outer support flange 169 extends over an entirety of the outer vertical side surface of the ceramic support 113, and over an entirety of the outer vertical side surface of the quartz ring 163, and over the lower outer vertical side surface of the cover ring 165. In some embodiments, the cover ring 165 extends radially outward above a top surface of the vertical portion of the L-shaped cross-section of the fixed outer support flange 169. And, in some embodiments, an upper outer vertical side surface of the cover ring 165 (located above the top surface of the vertical portion of the L-shaped cross-section of the fixed outer support flange 169) is substantially vertically aligned with an outer vertical surface of the vertical portion of the L-shaped cross-section of the fixed outer support flange 169. The horizontal portion of the L-shaped cross-section of the fixed outer support flange 169 is positioned on and fastened to the supporting surface 114 of a cantilever arm assembly 115. The fixed outer support flange 169 is formed of an electrically conductive material. In some embodiments, the fixed outer support flange 169 is

formed of aluminum or anodized aluminum. However, in other embodiments, the fixed outer support flange 169 can be formed of another electrically conductive material, such as copper or stainless steel. In some embodiments, the horizontal portion of the L-shaped cross-section of the fixed outer support flange 169 is bolted to the supporting surface 114 of a cantilever arm assembly 115.

[0070] An articulating outer support flange 171 is configured and positioned to extend around the outer vertical surface 169D of the vertical portion of the L-shaped cross-section of the fixed outer support flange 169, and to extend around the upper outer vertical side surface of the cover ring 165. The articulating outer support flange 171 has an annular shape that circumscribes both the vertical portion of the L-shaped vertical cross-section of the fixed outer support flange 169 and the upper outer vertical side surface of the cover ring 165. The articulating outer support flange 171 has an L-shaped vertical cross-section that includes a vertical portion and a horizontal portion. The vertical portion of the L-shaped cross-section of the articulating outer support flange 171 has an inner vertical surface that is positioned proximate to and spaced apart from both the outer vertical side surface of the vertical portion of the L-shaped cross-section of the fixed outer support flange 169 and the upper outer vertical side surface of the cover ring 165. In this manner, the articulating outer support flange 171 is moveable in the vertical direction (z-direction) along both the vertical portion of the L-shaped vertical cross-section of the fixed outer support flange 169 and the upper outer vertical side surface of the cover ring 165. The articulating outer support flange 171 is formed of an electrically conductive material. In some embodiments, the articulating outer support flange 171 is formed of aluminum or anodized aluminum. However, in other embodiments, the articulating outer support flange 171 can be formed of another electrically conductive material, such as copper or stainless steel.

[0071] A number of electrically conductive straps 173 are connected between the articulating outer support flange 171 and the fixed outer support flange 169, around the outer radial perimeters of both the articulating outer support flange 171 and the fixed outer support flange 169. In the example embodiment, the electrically conductive straps 173 are shown to have an "outward" configuration, in that the electrically conductive straps 173 bend outward away from the fixed outer support flange 169. In some embodiments, the electrically conductive straps 173 are formed of stainless steel. However, in other embodiments, the electrically conductive straps 173 can be formed of another electrically conductive material, such as aluminum or copper, among others.

[0072] In some embodiments, forty-eight (48) electrically conductive straps 173 are distributed in a substantially equally spaced manner around the outer radial perimeters of the articulating outer support flange 171 and the fixed outer support flange 169. It should be understood,

however, that the number of electrically conductive straps 173 can vary in different embodiments. In some embodiments, the number of electrically conductive straps 173 is within a range extending from about 24 to about 80, or within a range extending from about 36 to about 60, or within a range extending from about 40 to about 56. In some embodiments, the number of electrically conductive straps 173 is less than 24. In some embodiments, the number of electrically conductive straps 173 is greater than 80. Because the number of electrically conductive straps 173 has an effect on the ground return paths for the radiofrequency signals around the perimeter of the plasma processing region 182, the number of electrically conductive straps 173 can have an effect on the uniformity of process results across the wafer W. Also, the size of the electrically conductive straps 173 can vary in different embodiments.

[0073] In some embodiments, the electrically conductive straps 173 are connected to the fixed outer support flange 169 by a clamping force applied by securing a clamp ring 175 to a top surface of the horizontal portion of the L-shaped cross-section of the fixed outer support flange 169. In some embodiments, the clamp ring 175 is bolted to the fixed outer support flange 169. In some embodiments, the bolts that secure the clamp ring 175 to the fixed outer support flange 169 are positioned at locations between the electrically conductive straps 173. However, in some embodiments, one or more bolts that secure the clamp ring 175 to the fixed outer support flange 169 can be positioned to extend through electrically conductive straps 173. In some embodiments, the clamp ring 175 is formed of a same material as the fixed outer support flange 169. However, in other embodiments, the clamp ring 175 and the fixed outer support flange 169 can be formed of different materials.

[0074] In some embodiments, the electrically conductive straps 173 are connected to the articulating outer support flange 171 by a clamping force applied by securing a clamp ring 177 to a bottom surface of the horizontal portion of the L-shaped cross-section of the articulating outer support flange 171. Alternatively, in some embodiments, the first end portion of each of the plurality of electrically conductive straps 173 is connected to the upper surface of the horizontal portion of the articulating outer support flange 171 by the clamp ring 177. In some embodiments, the clamp ring 177 is bolted to the articulating outer support flange 171. In some embodiments, the bolts that secure the clamp ring 177 to the articulating outer support flange 171 are positioned at locations between the electrically conductive straps 173. However, in some embodiments, one or more bolts that secure the clamp ring 177 to the articulating outer support flange 171 can be positioned to extend through electrically conductive straps 173. In some embodiments, the clamp ring 177 is formed of a same material as the articulating outer support flange 171. However, in other embodiments, the clamp ring 177 and the articulating outer support flange 171 can be formed of different materials.

[0075] A set of support rods 201 are positioned around the cantilever arm assembly 115 to extend vertically through the horizontal portion 169B of the L-shaped cross-section of the fixed outer support flange 169. The upper end of the support rods 201 are configured to engage with the bottom surface of the horizontal portion of the L-shaped cross-section of the articulating outer support flange 171. In some embodiments, a lower end of each of the support rods 201 is engaged with a resistance mechanism 203. The resistance mechanism 203 is configured to provide an upward force to the corresponding support rod 201 that will resist downward movement of the support rod 201, while allowing some downward movement of the support rod 201. In some embodiments, the resistance mechanism 203 includes a spring to provide the upward force to the corresponding support rod 201. In some embodiments, the resistance mechanism 203 includes a material, e.g. spring and/or rubber, that has a sufficient spring constant to provide the upward force to the corresponding support rod 201. It should be understood that as the articulating outer support flange 171 moves downward to engage the set of support rods 201, the set of support rods 201 and corresponding resistance mechanisms 203 provide an upward force to the articulating outer support flange 171. In some embodiments, the set of support rods 201 includes three support rods 201 and corresponding resistance mechanisms 203. In some embodiments, the support rods 201 are positioned to have a substantially equal azimuthal spacing relative to a vertical centerline of the electrode 109. However, in other embodiments, the support rods 201 are positioned to have a non-equal azimuthal spacing relative to a vertical centerline of the electrode 109. Also, in some embodiments, more than three support rods 201 and corresponding resistance mechanisms 203 are provided to support the articulating outer support flange 171.

[0076] With continued reference back Figure 1, the plasma processing system 100 further includes a C-shroud member 185 positioned above the electrode 109. The C-shroud member 185 is configured to interface with the articulating outer support flange 171. Specifically, a seal 179 is disposed on the top surface of the horizontal portion of the L-shaped cross-section of the articulating outer support flange 171, such that the seal 179 is engaged by the C-shroud member 185 when the articulating outer support flange 171 is moved upward toward the C-shroud member 185. In some embodiments, the seal 179 is electrically conductive to assist with establishing electrical conduction between the C-shroud member 185 and the articulating outer support flange 171. In some embodiments, the C-shroud member 185 is formed of polysilicon. However, in other embodiments, the C-shroud member 185 is formed of another type of electrically conductive material that is chemically compatible with the processes to be formed in the plasma processing region 182, and that has sufficient mechanical strength.

[0077] The C-shroud is configured to extend around the plasma processing region 182 and

provide a radial extension of the plasma processing region 182 volume into the region defined within the C-shroud member 185. The C-shroud member 185 includes a lower wall 185A, an outer vertical wall 185B, and an upper wall 185C. In some embodiments, the outer vertical wall 185B and the upper wall 185C of the C-shroud member 185 are solid, non-perforated members, and the lower wall 185A of the C-shroud member 185 includes a number of vents 186 through which process gases flow from within the plasma processing region 182. In some embodiments, a throttle member 196 is disposed below the vents 186 of the C-shroud member 185 to control a flow of process gas through the vents 186. More specifically, in some embodiments, the throttle member 196 is configured to move up and down vertically in the z-direction relative to the C-shroud member 185 to control the flow of process gas through the vents 186. In some embodiments, the throttle member 196 is configured to engage with and/or enter the vents 186.

[0078] The upper wall 185C of the C-shroud member 185 is configured to support an upper electrode 187A/187B. In some embodiments, the upper electrode 187A/187B includes an inner upper electrode 187A and an outer upper electrode 187B. Alternatively, in some embodiments, the inner upper electrode 187A is present and the outer upper electrode 187B is not present, with the inner upper electrode 187A extending radially to cover the location that would be occupied by the outer upper electrode 187B. In some embodiments, the inner upper electrode 187A is formed of single crystal silicon and the outer upper electrode 187B is formed of polysilicon. However, in other embodiments, the inner upper electrode 187A and the outer upper electrode 187B can be formed of other materials that are structurally, chemically, electrically, and mechanically compatible with the processes to be performed within the plasma processing region 182. The inner upper electrode 187A includes a number of throughports 197 defined as holes extending through an entire vertical thickness of the inner upper electrode 187A. The throughports 197 are distributed across the inner upper electrode 187A, relative to the x-y plane, to provide for flow of process gas(es) from a plenum region 188 above the upper electrode 187A/187B to the plasma processing region 182 below the upper electrode 187A/187B.

[0079] It should be understood that the distribution of throughports 197 across the inner upper electrode 187A can be configured in different ways for different embodiments. For example, a total number of throughports 197 within the inner upper electrode 187A and/or a spatial distribution of throughports 197 within the inner upper electrode 187A can vary between different embodiments. Also, a diameter of the throughports 197 can vary between different embodiments. In general, it is of interest to reduce the diameter of the throughports 197 to a size small enough to prevent intrusion of the plasma 180 into the throughports 197 from the plasma processing region 182. In some embodiments, as the diameter of the throughports 197 is reduced, the total number of throughports 197 within the inner upper electrode 187A is increased

to maintain a prescribed overall flowrate of process gas(es) from the process gas plenum region 188 through the inner upper electrode 187A to the plasma processing region 182. Also, in some embodiments, the upper electrode 187A/187B is electrically connected to a reference ground potential. However, in other embodiments, the inner upper electrode 187A and/or the outer upper electrode 187B is/are electrically connected to either a respective direct current (DC) electrical supply or a respective radiofrequency power supply by way of a corresponding impedance matching circuit.

[0080] The plenum region 188 is defined by an upper member 189. One or more gas supply ports 192 are formed through the chamber 101 and the upper member 189 to be in fluid communication with the plenum region 188. The one or more gas supply ports 192 are fluidly connected (plumbed) to a process gas supply system 191. The process gas supply system 191 includes one or process gas supplies, one or more mass flow controller(s), one or more flow control valve(s), among other devices, to provide controlled flow of one or more process gas(es) through the one or more gas supply ports 192 to the plenum region 188, as indicated by arrow 193. In some embodiments, the process gas supply system 191 also includes one or more components for controlling a temperature of the process gas(es). The process gas supply system 191 is connected to the control system 120 through one or more signal conductors 194.

[0081] A processing gap (g1) is defined as the vertical (z-direction) distance as measured between the top surface of the ceramic layer 110 and the bottom surface of the inner upper electrode 187A. The size of the processing gap (g1) can be adjusted by moving the cantilever arm assembly 115 in the vertical direction (z-direction). As the cantilever arm assembly 115 moves upward, the articulating outer support flange 171 eventually engages the lower wall 185A of the C-shroud member 185, at which point the articulating outer support flange 171 moves along the fixed outer support flange 169 as the cantilever arm assembly 115 continues to move upward until the set of support rods 201 engage the articulating outer support flange 171 and the prescribed processing gap (g1) size is achieved. Then, to reverse this movement for removal of the wafer W from the chamber, the cantilever arm assembly 115 is moved downward until the articulating outer support flange 171 moves away from the lower wall 185A of the C-shroud member 185. It should be understood that Figure 1 shows the system 100 in a closed configuration with the wafer W position on the ceramic layer 110 for plasma processing.

[0082] During plasma processing operations within the plasma processing system 100, the one or more process gas(es) are supplied to the plasma processing region 182 by way of the process gas supply system 191, plenum region 188, and throughports 197 within the inner upper electrode 187A. Also, radiofrequency signals are transmitted into the plasma processing region 182, by way of the first and second radiofrequency signal generators 147, 149, the impedance

matching system 143, the radiofrequency signal supply rod 137, the radiofrequency signal supply shaft 141, the facilities plate 111, the electrode 109, and through the ceramic layer 110. The radiofrequency signals transform the process gas(es) into the plasma 180 within the plasma processing region 182. Ions and/or reactive constituents of the plasma interact with one or more materials on the wafer W to cause a change in composition and/or shape of particular material(s) present on the wafer W. The exhaust gases from the plasma processing region 182 flow through the vents 186 in the C-shroud member 185 and through the interior region 103 within the chamber 101 to the exhaust port 105 under the influence of a suction force applied at the exhaust port 105, as indicated by arrows 195.

[0083] In various embodiments, the electrode 109 can be configured to have different diameters. However, in some embodiments, to increase the surface of the electrode 109 upon which the edge ring 167 rests, the diameter of the electrode 109 is extended. In some embodiments, an electrically conductive gel 226 is disposed between a bottom of the edge ring 167 and the top of the electrode 109 and/or between the bottom of the edge ring 167 and the top of the coupling ring 161. In these embodiments, the increased diameter of the electrode 109 provides more surface area upon which the conductive gel is disposed between the edge ring 167 and the electrode 109.

[0084] It should be understood that the combination of the articulating outer support flange 171, the electrically conductive straps 173, and the fixed outer support flange 169 are electrically at a reference ground potential, and collectively form a ground return path for radiofrequency signals transmitted from the electrode 109 through the ceramic layer 110 into the plasma processing region 182. The azimuthal uniformity of this ground return path around the perimeter of the electrode 109 can have an effect on uniformity of process results on the wafer W. For example, in some embodiments, the uniformity of etch rate across the wafer W can be affected by the azimuthal uniformity of the ground return path around the perimeter of the electrode 109. To this end, it should be understood that the number, configuration, and arrangement of the electrically conductive straps 173 around the perimeter of the electrode 109 can affect the uniformity of process results across the wafer W.

[0085] With reference back to Figure 1, a Tunable Edge Sheath (TES) system is implemented to include a TES electrode 225 disposed (embedded) within the coupling ring 161. The TES system also includes a number of TES radiofrequency signal supply pins 223 in physical and electrical connection with the TES electrode 225. Each TES radiofrequency signal supply pin 223 extends through a corresponding insulator feedthrough member 231 configured to electrically separate the TES radiofrequency signal supply pin 223 from surrounding structures, such as from the ceramic support 113 and the cantilever arm assembly 115 structure. In some embodiments, o-

rings 227 and 229 are disposed to ensure that the region inside of the insulator feedthrough member 231 is not exposed to any materials/gases present within the plasma processing region 182. In some embodiments, the TES radiofrequency signal supply pins 223 are formed of copper, or aluminum, or anodized aluminum, among others.

[0086] The TES radiofrequency signal supply pins 223 extend into the open region 118 inside of the cantilever arm assembly 115, where each of the TES radiofrequency signal supply pins 223 is electrically connected to a TES radiofrequency signal supply conductor 219 through a corresponding TES radiofrequency signal filter 221. In some embodiments, three TES radiofrequency signal supply pins 223 are positioned to physically and electrically connect with the TES electrode 225 at substantially equally spaced azimuthal locations about the centerline of the electrode 109. It should be understood, however, that other embodiments can have more than three TES radiofrequency signal supply pins 223 in physical and electrical connection with the TES electrode 225. Also, some embodiments can have either one or two TES radiofrequency signal supply pins 223 in physical and electrical connection with the TES electrode 225. Each TES radiofrequency signal supply pin 223 is electrically connected to a corresponding TES radiofrequency signal filter 221, with each TES radiofrequency signal filter 221 electrically connected to the TES radiofrequency signal supply conductor 219. In some embodiments, each TES radiofrequency signal filter 221 is configured as an inductor. For example, in some embodiments, each TES radiofrequency signal filter 221 is configured as a coiled conductor, such as a metal coil wrapped around a dielectric core structure. In various embodiments, the metal coil can be formed of solid copper rod, copper tubing, aluminum rod, or aluminum tubing, among others. Also, in some embodiments, each TES radiofrequency signal filter 221 can be configured as a combination of inductive and capacitive structures. In the interest of improving plasma processing result uniformity across the wafer W, each of the TES radiofrequency signal filters 221 has a substantially same configuration.

[0087] In some embodiments, the TES radiofrequency signal supply conductor 219 is formed as a ring-shaped (annular-shaped) structure, so as to extend around the open region 118 inside of the cantilever arm assembly 115 to enable physical and electrical connection of the azimuthally distributed TES radiofrequency signal filters 221 with the TES radiofrequency signal supply conductor 219. In some embodiments, the TES radiofrequency signal supply conductor 219 is formed as a solid (non-tubular) structure. Alternatively, in some embodiments, the TES radiofrequency signal supply conductor 219 is formed as a tubular structure. In some embodiments, the TES radiofrequency signal supply conductor 219 is formed of copper, or aluminum, or anodized aluminum, among others.

[0088] The TES radiofrequency signal supply conductor 219 is electrically connected to a TES

radiofrequency supply cable 217. Also, a capacitor 218 is connected between the TES radiofrequency signal supply conductor 219 and a reference ground potential, such as the structure of the cantilever arm assembly 115. More specifically, the capacitor 218 has a first terminal electrically connected to both the TES radiofrequency supply cable 217 and the TES radiofrequency signal supply conductor 219, and the capacitor 218 has a second terminal electrically connected to the reference ground potential. In some embodiments, the capacitor 218 is a variable capacitor. In some embodiments, the capacitor 218 is a fixed capacitor. In some embodiments, the capacitor 218 is set to have a capacitance within a range extending from about 10 picoFarads to about 100 picoFarads. The TES radiofrequency supply cable 217 is connected to a TES impedance matching system 211. The TES impedance matching system 211 is connected to a TES radiofrequency signal generator 213. Radiofrequency signals generated by the TES radiofrequency signal generator 213 are transmitted through the TES impedance matching system 211 to the TES radiofrequency supply cable 217, then to the TES radiofrequency signal supply conductor 219, then through the TES radiofrequency signal filters 221 to the respective TES radiofrequency signal supply pins 223, and to the TES electrode 225 within the coupling ring 161. In some embodiments, the TES radiofrequency signal generator 213 is configured and operated to generate radiofrequency signals within a frequency range extending from about 50 kiloHertz to about 27 MHz. In some embodiments, the TES radiofrequency signal generator 213 supplies radiofrequency power within a range extending from about 50 Watts to about 10 kiloWatts. The TES radiofrequency signal generator 213 is also connected to the control system 120 through one or more signal conductors 215.

[0089] The TES impedance matching system 211 includes an arrangement of inductors and capacitors sized and connected to provide for impedance matching so that radiofrequency power can be transmitted from the TES radiofrequency signal generator 213 along the TES radiofrequency supply cable 217, along the TES radiofrequency signal supply conductor 219, through the TES radiofrequency signal filters 221, through the respective TES radiofrequency signal supply pins 223, to the TES electrode 225 within the coupling ring 161, and into the plasma processing region 182 above the edge ring 167. The TES impedance matching system 211 is also connected to the control system 120 through one or more signal conductors 214.

[0090] By transmitting radiofrequency signals/power through the TES electrode 225 disposed (embedded) within the coupling ring 161, the TES system is capable of controlling characteristics of the plasma 180 near the peripheral edge of the wafer W. For example, in some embodiments, the TES system is operated to control the plasma 180 sheath properties near the edge ring 167, such as by controlling a shape of the plasma 180 sheath and/or by controlling a size (either increase in sheath thickness or decrease in sheath thickness). Also, in some

embodiments, by controlling the shape of the plasma 180 sheath near the edge ring 167, it is possible to control various properties of the bulk plasma 180 over the wafer W. Also, in some embodiments, the TES system is operated to control a density of the plasma 180 near the edge ring 167. For example, in some embodiments, the TES system is operated to either increase or decrease the density of the plasma 180 near the edge ring 167. Also, in some embodiments, the TES system is operated to control a bias voltage present on the edge ring 167, which in turn controls/influences movement of ions and other charged constituents within the plasma 180 near the edge ring 167. For example, in some embodiments, the TES system is operated to control a bias voltage present on the edge ring 167 to attract more ions from the plasma 180 toward the edge of the wafer W. And, in some embodiments, the TES system is operated to control a bias voltage present on the edge ring 167 to repel ions from the plasma 180 away from the edge of the wafer W. It should be understood that the TES system can be operated to perform a variety of different functions, such as those mentioned above, among others, either separately or in combination.

[0091] In some embodiments, the coupling ring 161 is formed of a dielectric material, such as quartz, or ceramic, or alumina (Al_2O_3), or a polymer, among others.

[0092] A bottom surface of the edge ring 167 has a portion that is coupled to the upper surface of the coupling ring 161 through a layer of thermally and electrically conductive gel to thermally sink the coupling ring 161 to the edge ring 167. Also, the bottom surface of the edge ring 167 has another portion that is coupled to an upper surface of the electrode 109 through a layer of thermally and electrically conductive gel. Examples of the thermally and electrically conductive gel include polyimide, polyketone, polyetherketone, polyether sulfone, polyethylene terephthalate, fluoroethylene propylene copolymers, cellulose, triacetates, and silicone, among others. In some embodiments, the thermally and electrically conductive gel is formed as a double-sided tape. In some embodiments, the edge ring 167 has an inner diameter sized to be proximate to the outer diameter of the ceramic layer 110.

[0093] In various embodiments, the TES electrode 225 is formed of an electrically conductive material, such as platinum, steel, aluminum, or copper, among others. During operation, capacitive coupling occurs between the TES electrode 225 and the edge ring 167, such that the edge ring 167 is electrically powered to influence processing of the wafer W near the outer perimeter of the wafer W.

[0094] Broadly speaking, implementations of the disclosure provide for a CCP chamber having at least one magnetic coil positioned outside the chamber. In some implementations, a single magnetic coil or multiple magnetic coils are positioned above or on top of the chamber. A DC current is applied to the magnetic coil to generate a magnetic field (B-field). With the B-field

from these currents, control over center non-uniformity is achieved. In some implementations, using a combination of different coils provides for different magnetic fields to enable more control over overall uniformity.

[0095] Standard plasma systems are prone to non-uniformities where there is accumulation of positive and negative ions, as their densities are at least partially controlled by electron density and further based on temperature. To address such non-uniformities, implementations of the disclosure contemplate the application of a static B-field to the plasma to minimize localized charged species accumulation and thereby improve uniformity.

[0096] Without being bound by any particular theory of operation, it is believed that in accordance with implementations of the disclosure, the B-field is configured to be relatively weak, so that it does not completely magnetize the plasma. However, electrons which are sensitive to the B-field are affected. Thus, it is believed that the B-field is used to change the direction of diffusion of the electrons so that the electrons travel approximately along the field lines. In this manner, the B-field can be utilized to affect and control the amount of electrons in the middle that discharge. By providing an approximately vertical B-field in the central portion of the plasma, from top to bottom, then electrons that tend to collect in the middle can magnetize so that the electrons move approximately along the B-field lines. Hence, there will be more losses to the upper and lower electrons, and therefore a consequent reduction in the amount of electrons in the center portion.

[0097] Figure 2A conceptually illustrates a cross-section of a process chamber having a single magnetic coil for applying a magnetic field during plasma processing, in accordance with implementations of the disclosure. As shown, a single magnetic coil 200 is disposed over the chamber 101. It will be appreciated that the magnetic coil 200 is substantially circular in shape or ring-shaped or annular in shape. Further, the magnetic coil 200 is disposed along a plane that is parallel to the surface plane of the wafer. That is, the windings/turns of the magnetic coil are substantially along a horizontal plane that is parallel to the plane of the wafer, so that the magnetic coil itself is horizontally oriented, and centered about an axis perpendicular through the center of the wafer. In some implementations, the magnetic coil 200 has a diameter (center to center diameter, or inner diameter, or outer diameter) in the range of approximately 15 to 20 inches (approximately 38 to 51 cm) for a chamber configured to process a 300mm wafer; in some implementations, the diameter is in the range of approximately 16 to 18 inches (approximately 41 to 46 cm).

[0098] In some implementations, the height of the magnetic coil 200 above the surface level of the wafer is in the range of approximately 3 to 15 inches (approximately 8 to 38 cm); in some implementations, in the range of approximately 5 to 12 inches (approximately 13 to 30 cm); in

some implementations, approximately 7 to 8 inches (approximately 18 to 20 cm).

[0099] In accordance with implementations of the disclosure, a DC current is applied to the magnetic coil 200 to produce a static B-field in the chamber 101.

[0100] Figure 2B conceptually illustrates a cross-section of a process chamber having two magnetic coils for applying a magnetic field during plasma processing, in accordance with implementations of the disclosure. As shown, a first magnetic coil 200 and a second magnetic coil 202 are concentric coils disposed over the chamber 101. In some implementations, the first and second magnetic coils 200 and 202 are approximately coplanar. In some implementations, the first and second magnetic coils 200 and 202 are not coplanar, but positioned in parallel planes, while being concentric about the same central axis. In some implementations, the first magnetic coil 200 has a diameter as described above with respect to Figure 2A.

[0101] In some implementations, the second magnetic coil 202 has a diameter (center to center diameter, or inner diameter, or outer diameter) in the range of approximately 20 to 25 inches (approximately 51 to 63 cm) for a chamber configured to process a 300 mm wafer; in some implementations, the diameter of the second magnetic coil 202 is in the range of approximately 22 to 24 inches (approximately 56 to 61 cm).

[0102] In accordance with implementations of the disclosure, DC currents are applied to the magnetic coils 200 and 202 to produce a static B-field in the chamber 101. In various implementations, the DC currents applied to each of the coils can be approximately the same or different, and in the same direction or opposite directions.

[0103] Though not specifically shown, it will be appreciated that in other implementations, there can be additional magnetic coils disposed over the chamber 101. For example, in some implementations, a third magnetic coil is provided, also disposed over the chamber 101, and having a diameter smaller than the first magnetic coil 200. In some implementations, such a third magnetic coil has a diameter in the range of approximately 10 to 15 inches (approximately 25 to 38 cm) for a chamber configured to process a 300mm wafer; in some implementations, the third magnetic coil has a diameter in the range of approximately 11 to 13 inches (approximately 28 to 33 cm).

[0104] In some implementations, the first, second and third magnetic coils are approximately coplanar. In some implementations, the first, second, and third magnetic coils are not coplanar, but positioned in parallel planes, while being concentric about the same central axis. In some implementations, two of the magnetic coils are coplanar, while the other magnetic coil is not coplanar with either of the two that are coplanar.

[0105] In some implementations, there can be additional magnetic coils disposed over the chamber 101.

[0106] Figure 2C conceptually illustrates a cross-section of a process chamber having three magnetic coils for applying a magnetic field during plasma processing, in accordance with implementations of the disclosure. As shown in the illustrated implementation, two magnetic coils 200 and 202 are disposed over the chamber 101. In some implementations, the magnetic coils 200 and 202 are configured similar to the implementation of Figure 2B. Furthermore, a bottom magnetic coil 204 is disposed below the electrode 109, so as to be below the plasma processing region 182. In some implementations, the bottom magnetic coil 204 has a diameter (center to center diameter, or inner diameter, or outer diameter) in the range of approximately 10 to 25 inches (approximately 25 to 63 cm). In accordance with implementations of the disclosure, a DC current is applied to the magnetic coil 204, alone or in combination with DC current applied to other magnetic coils, to produce a static B-field in the chamber 101.

[0107] Though a single bottom magnetic coil 204 is shown and described in the illustrated implementation, in other implementations, there can be more than one bottom magnetic coil. In the case of multiple bottom magnetic coils, such bottom magnetic coils can be coplanar or not coplanar with each other.

[0108] Figure 2D conceptually illustrates a cross-section of a process chamber having four magnetic coils for applying a magnetic field during plasma processing, in accordance with implementations of the disclosure. As shown in the illustrated implementation, similar to the configuration of Figure 2C, there are two magnetic coils 200 and 202 disposed over the chamber 101, and a bottom magnetic coil 104 disposed below the electrode 109. Furthermore, a side magnetic coil 206 is positioned so as to laterally surround the plasma processing region 182. In some implementations, the side magnetic coil 206 is positioned adjacent to the C-shroud member 185. In some implementations, the side magnetic coil 206 is positioned adjacent to the walls 101a of the chamber 101. In some implementations, the side magnetic coil 206 is vertically positioned so as to be approximately at the height of at least a portion of the plasma processing region 182. In some implementations, the side magnetic coil 206 has a diameter (center to center diameter, or inner diameter, or outer diameter) in the range of approximately 25 to 30 inches (approximately 63 to 76 cm) for a chamber configured to process a 300 mm wafer. In accordance with implementations of the disclosure, a DC current is applied to the magnetic coil 206, alone or in combination with DC currents applied to other magnetic coils, to produce a static B-field in the chamber 101.

[0109] Though a single side magnetic coil 206 is shown and described in the illustrated implementation, in other implementations, there can be more than one side magnetic coil. In some implementations, multiple side magnetic coils are provided and configured to have the same diameter and are vertically aligned with one another. In some implementations, multiple

side magnetic coils can have different diameters and may be coplanar or non-coplanar with one another.

[0110] As described, in various implementations, there can be one or more magnetic coils positioned above, below, and/or surrounding the plasma processing region 182. Each magnetic coil is supplied with a DC current to generate a static B-field in the plasma processing region 182. Broadly speaking, in some implementations, the B-field is created substantially in the z-direction in the central portion of the plasma processing region 182, so as to effect suppression of the center etch rate. Thus, if a given CCP chamber exhibits a peak in etch rate at the center portion of the wafer, then the B-field can be applied to the plasma to suppress the center peak.

[0111] In some implementations, a magnetic coil in accordance with implementations of the disclosure is formed from insulated copper wire, or magnet wire. In some implementations, the magnet wire is approximately 16 to 10 AWG magnet wire. In some implementations, the coiling of the magnet wire is configured to have approximately 30 to 60 turns for a given magnetic coil. In some implementations, the coiling is configured to have approximately 40 to 50 turns. In some implementations, the magnetic coil has a cross sectional width or height of approximately 1 to 3 cm.

[0112] In some implementations, a magnetic coil in accordance with implementations of the disclosure is supported by a support structure formed from an insulating material (e.g. plastic insulator), so as to further insulate the magnetic coil from other components or hardware.

[0113] By comparison to other applications of magnetic fields in the context of plasma processing, the B-field generated in accordance with implementations of the disclosure is a low strength field, so that there is minimal effect on other components. However, electrons in the plasma are affected by the B-field in such a manner as to promote reduced localized accumulation of charged species and therefore improve plasma and etch uniformity. In some implementations, the strength of the generated B-field is configured to be less than approximately 10 Gauss (measured at the wafer level and approximately in the center); in some implementations, less than approximately 5 Gauss.

[0114] It will be appreciated that correspondingly low current levels are applied to produce the weak magnetic fields in accordance with implementations of the disclosure. In some implementations, the applied current to a given magnetic coil is approximately 10 amps or less; in some implementations, approximately 7 amps or less; in some implementations, approximately 5 amps or less; in some implementations, approximately 3 amps or less.

[0115] Though a low strength magnetic field is provided, the chamber walls are typically constructed from an aluminum and/or silicon-containing material, and therefore the B-field penetrates the chamber.

[0116] Still, even a low strength magnetic field may interfere with nearby devices. Hence, in some implementations, a cover constructed from a nickel-containing material is provided, to shield nearby devices from the magnetic field.

[0117] Previous applications of a magnetic field in plasma processing have employed a much stronger magnetic field, where the direction of the field is parallel to the wafer. This promoted electron movement along B-field lines parallel to the surface of the wafer, and was performed as a way to control overall uniformity. However, such applications were prone to device damage, as there was also charge accumulation on the device, and the interaction of the strong B-field tended to produce device damage.

[0118] However, in contrast to these prior uses of a strong magnetic field, implementations of this disclosure employ a very low strength B-field by comparison. It has been observed that B-fields generated by magnetized steel parts, and even very weak electric fields, can have an effect on uniformity at the center. Further, as device sizes shrink and the tolerance for non-uniformity is reduced (e.g. significantly below 1%), so changes in ion density can have a significant impact on uniformity. Generally, in accordance with implementations of the disclosure, the greater the strength of the B-field that is applied, the greater the suppression of etch rate in the center portion of the wafer.

[0119] Figure 3A is a graph illustrating etch rate results for a continuous wave plasma under different applied B-fields, in accordance with implementations of the disclosure. In the illustrated implementation, etch rate as a function of radius is shown for a continuous wave plasma process carried out on a blanket oxide wafer. The curve 300 is a plot showing etch rate results with zero applied current to a magnetic coil as described in the above implementations. The curve 302 is a plot showing etch rate results with a 5 Amp current applied to the magnetic coil. The curve 304 is a plot showing etch rate results with a 10 Amp current applied to the magnetic coil. As can be seen from the results, with zero current applied to the magnetic coil as shown by curve 300), there is significant peaking of the etch rate in the central portion of the wafer. However, as current in the magnetic coil is increased to 5 Amps (curve 302) and to 10 Amps (curve 304), so the etch rate in the central portion of the wafer is reduced. This result demonstrates the effectiveness of increasing the B-field to reduce center etch rate peaking, and thereby reduce the non-uniformity of etch rate.

[0120] Figure 3B is a graph illustrating the change in etch rate that is effected by the applied B-field, in accordance with the implementation of Figure 3A. As indicated in Figure 3B, the curve 306 is a plot showing the change (or delta) in etch rate of the continuous wave plasma process performed with the 5 Amp current applied to the magnetic coil (as previously indicated by curve 302) versus the zero current condition (as previously indicated by curve 300). The curve 308 is a

plot showing the change in etch rate of the continuous wave plasma process performed with the 10 Amp current applied to the magnetic coil (as previously indicated by curve 304) versus the zero current condition.

[0121] As shown by the etch rate delta results, the application of a B-field, in accordance with implementations of the disclosure, provides a significant reduction in etch rate principally in the central portion of the wafer (e.g. within an approximate 50 mm radius). Also, the reduction in etch rate is greater with a stronger applied B-field.

[0122] Figure 4A is a graph illustrating etch rate as a function of wafer radius for a plasma process with different applied B-fields, in accordance with implementations of the disclosure. In the illustrated implementation, etch rate on a blanket oxide wafer is shown for a pulsed plasma process. In the illustrated implementation, the curve 400 illustrates etch rate as a function of wafer radius for a pulsed plasma process with zero current applied to a magnetic coil, as described above in accordance with implementations of the disclosure. The curve 402 illustrates etch rate as a function of wafer radius for the pulsed plasma process with 5 Amps current applied to the magnetic coil. The curve 404 illustrates etch rate as a function of wafer radius for the pulsed plasma process with 10 Amps current applied to the magnetic coil. As shown, in the zero current condition, such that no additional B-field is applied (other than existing ambient fields), there is a significant peak in etch rate towards the center of the wafer. However, as current is applied to the magnetic coil at 5 Amps, so the center peak in etch rate is reduced. And as current is applied to the magnetic coil at 10 Amps, the center etch rate is further reduced. This, as the applied B-field is increased, the etch rate in the center portion of the wafer becomes more diminished, thereby reducing non-uniformity across the center of the wafer.

[0123] Figure 4B is a graph showing the change in etch rate as a result of applied B-fields, in accordance with the implementation of Figure 4A. The curve 406 illustrates the change in etch rate for the pulsed plasma process with the 5 Amp current applied to the magnetic coil as compared to the zero current condition. The curve 408 illustrates the change in etch rate for the pulsed plasma process with the 10 Amp current applied to the magnetic coil as compared to the zero current condition. As can be seen, the effect of the applied B-field primarily reduces etch rate in the center portion of the wafer (e.g. within approximately a 50 mm radius of the center).

[0124] Figure 5 shows cross-section images of portions of wafers having etched features thereon, demonstrating the effect of an applied B-field on feature tilting, in accordance with implementations of the disclosure. The upper images provide cross-sectional views of wafer portions having etched features which were processed without an applied B-field. Whereas the lower images provide cross-sectional views of wafer portions having etched features which were processed with an applied B-field (resulting from application of a 1 Amp current to a magnetic

coil). As can be seen, features etched under an applied B-field exhibit less tilting and are more vertical than features etched in the absence of the applied B-field. Applying the B-field improves tilt because the applied B-field changes the shape of the plasma sheath at the wafer. Non-uniform plasma results in tilting at some radiuses, and therefore applying a magnetic field to the plasma that reduces non-uniformity also can reduce tilting and enable more vertical etching.

[0125] In accordance with some implementations, a system having four magnetic coils disposed above the chamber is provided. The four magnetic coils are substantially coplanar, and concentric about the same axis, which is substantially perpendicular through the center of the wafer. The four magnetic coils are referenced as coil "A", "B", "C", and "D". Coil A has an inner diameter of approximately 12 inches (approximately 30 cm); coil B has an inner diameter of approximately 14 inches (approximately 36 cm); coil C has an inner diameter of approximately 17 inches (approximately 43 cm); and coil D has an inner diameter of approximately 23 inches (approximately 58 cm). By varying which coils receive current, the amount of current applied to a given coil, and the direction of current applied to a given coil, various magnetic profiles can be achieved, which can be tuned, for example, to reduce radial etch non-uniformity.

[0126] Figure 6A illustrates magnetic field strength at the wafer level in the z-direction (vertical direction, or perpendicular to the wafer surface) versus radial position along a 300mm diameter wafer, for various single coil current configurations, in accordance with implementations of the disclosure. That is, currents were applied to a single one of coils A, B, C, and D, and the strength of the magnetic field in the z-direction was measured in Gauss.

[0127] A positive current indicates current applied in a counterclockwise direction, when considered from an overhead view of the coil. Accordingly, a negative current indicates current applied in a clockwise direction.

[0128] In the illustrated implementation, the legend for the graph is of the following form: (coil#)(current)_(coil#)(current)_(coil#)(current)_(coil#)(current). Thus, the curve indicated as "A5_B0_C0_D0" can be understood as the result for a 5 Amp current applied to coil A, and zero currents applied to coils B, C, and D. The curve indicated as "A-5_B0_C0_D0" can be understood as the result for a -5 Amp current applied to coil A, and zero currents applied to coils B, C, and D. The curve indicated as "A0_B5_C0_D0" can be understood as the result for a 5 Amp current applied to coil B, and zero currents applied to coils A, C, and D, and so forth.

[0129] Figure 6B illustrates magnetic field strength at the wafer level in the radial direction (in Gauss) versus radial position along a 300mm diameter wafer, for various single coil current configurations, in accordance with the implementations of Figure 6A. As can be seen from these results, radial B-field strength at the wafer edge is comparable to z-direction B-field strength.

[0130] In some implementations, it will be appreciated that magnetic field strength at the wafer level is approximately one-third of the magnetic field strength at the level of the magnetic coils.

[0131] Figure 7A is a graph illustrating thermal oxide etch rate versus radial position along a 300mm wafer, for various positive currents (counterclockwise) applied to single coils A (12"), B (14"), C (17"), and D (23"), in accordance with implementations of the disclosure.

[0132] Figure 7B is a graph illustrating thermal oxide etch rate versus radial position along a 300mm wafer, for various negative currents (clockwise) applied to single coils A (12"), B (14"), C (17"), and D (23"), in accordance with implementations of the disclosure.

[0133] As the results of Figures 7A and 7B demonstrate, different coil sizes and currents can have different impacts on oxide etch rates. For the same coil, opposite current directions can have different impacts on oxide etch rates, especially at lower current magnitudes. This can be understood, as when the coil induced B-field is lower, then the ambient B-field offset has a more significant effect.

[0134] Figure 8A illustrates magnetic field strength at the wafer level in the z-direction (vertical direction, or perpendicular to the wafer surface) versus radial position along a 300mm diameter wafer, for various two-coil current configurations, in accordance with implementations of the disclosure. That is, currents were applied to two of coils A, B, C, and D, and the strength of the magnetic field in the z-direction was measured in Gauss.

[0135] Figure 8B illustrates magnetic field strength at the wafer level in the radial direction (in Gauss) versus radial position along a 300mm diameter wafer, for various two-coil current configurations, in accordance with the implementations of Figure 8A.

[0136] As these results demonstrate, by combining different coil currents with the same or different directions, it is possible to create different B-field profiles along the wafer radius, and thereby achieve different effects on plasma and etch profiles.

[0137] Figure 9A illustrates magnetic field strength at the wafer level in the z-direction (vertical direction, or perpendicular to the wafer surface) versus radial position along a 300mm diameter wafer, for various three-coil current configurations, in accordance with implementations of the disclosure. That is, currents were applied to three of coils A, B, C, and D, and the strength of the magnetic field in the z-direction was measured in Gauss.

[0138] Figure 9B illustrates magnetic field strength at the wafer level in the radial direction (in Gauss) versus radial position along a 300mm diameter wafer, for various three-coil current configurations, in accordance with the implementations of Figure 9A.

[0139] As these results demonstrate, by combining different coil currents with the same or different directions, it is possible to create different B-field profiles along the wafer radius, and thereby achieve different effects on plasma and etch profiles.

[0140] Figure 10A is a graph illustrating etch rate as a function of radial position along a 300 mm wafer, for a two coil combination, in accordance with implementations of the disclosure. In the illustrated implementation, the specific two-coil combination includes coil A (12" diameter) and coil D (23" diameter).

[0141] Figure 10B is a graph illustrating the etch rate delta as compared to a zero current condition, in accordance with the implementations of Figure 10A.

[0142] As shown, different current combinations between the 12" and 23" coils can provide adjustability affecting the etch rate uniformity.

[0143] Figure 11 is a conceptual schematic diagram of a system for controlling power to multiple magnetic coils, in accordance with implementations of the disclosure. In the illustrated implementation, the control system 120 is operatively connected to, and controls the operation of, several DC power supplies 1100, 1102, 1104, and 1106. The DC power supplies respectively apply a DC current to magnetic coils 1108, 1110, 1112, and 1114. The control system 120 can control the magnitude/strength of the DC current (e.g. Amperage) and the polarity (e.g. positive or negative; or, counterclockwise or clockwise) of the DC current supplied by a given one of the DC power supplies.

[0144] In some implementations, the magnetic coils 1108, 1110, 1112, and 1114 are the coils A, B, C, and D described above. In some implementations, the magnetic coils 1108, 1110, 1112, and 1114 can be any of the magnetic coils described in accordance with the various implementations of the disclosure. Though four magnetic coils and four corresponding DC power supplies are shown, it will be appreciated that there can be additional magnetic coils and DC power supplies in other implementations.

[0145] In some implementations, a user interface is provided to enable an operator to adjust the parameters of the DC power supplies, such as by providing settings for adjustment of the DC current magnitude, and its polarity, for any given DC power supply.

[0146] As has been discussed, in some implementations, application of a B-field during plasma processing can be used to reduce plasma non-uniformity, and thereby reduce etch non-uniformity. Furthermore, in some implementations, application of the B-field can be used for chamber matching, to compensate for variation between tools due to environmental magnetic fields. Ambient magnetic fields can vary from tool to tool, and therefore an applied B-field can be used to counter/offset such ambient environmental fields, and thereby provide consistency from tool to tool.

[0147] It will be appreciated that any of the methods described in the present disclosure can be implemented to run automatically by the control system 120.

[0148] Figure 12 shows an example schematic of the control system 120 of Figure 1, in

accordance with some embodiments. In some embodiments, the control system 120 is configured as a process controller for controlling the semiconductor fabrication process performed in plasma processing system 100. In various embodiments, the control system 120 includes a processor 1401, a storage hardware unit (HU) 1403 (e.g. memory), an input HU 1405, an output HU 1407, an input/output (I/O) interface 1409, an I/O interface 1411, a network interface controller (NIC) 1413, and a data communication bus 1415. The processor 1401, the storage HU 1403, the input HU 1405, the output HU 1407, the I/O interface 1409, the I/O interface 1411, and the NIC 1413 are in data communication with each other by way of the data communication bus 1415. The input HU 1405 is configured to receive data communication from a number of external devices. Examples of the input HU 1405 include a data acquisition system, a data acquisition card, etc. The output HU 1407 is configured to transmit data to a number of external devices. An examples of the output HU 1407 is a device controller. Examples of the NIC 1413 include a network interface card, a network adapter, etc. Each of the I/O interfaces 1409 and 1411 is defined to provide compatibility between different hardware units coupled to the I/O interface. For example, the I/O interface 1409 can be defined to convert a signal received from the input HU 1405 into a form, amplitude, and/or speed compatible with the data communication bus 1415. Also, the I/O interface 1407 can be defined to convert a signal received from the data communication bus 1415 into a form, amplitude, and/or speed compatible with the output HU 1407. Although various operations are described herein as being performed by the processor 1401 of the control system 120, it should be understood that in some embodiments various operations can be performed by multiple processors of the control system 120 and/or by multiple processors of multiple computing systems in data communication with the control system 120.

[0149] In some embodiments, the control system 120 is employed to control devices in various wafer fabrication systems based in-part on sensed values. For example, the control system 120 may control one or more of valves 1417, filter heaters 1419, wafer support structure heaters 1421, pumps 1423, and other devices 1425 based on the sensed values and other control parameters. The valves 1417 can include valves associated with control of the backside gas supply system 129, the process gas supply system 191, and the temperature control fluid circulation system 125. The control system 120 receives the sensed values from, for example, pressure manometers 1427, flow meters 1429, temperature sensors 1431, and/or other sensors 1433, e.g. voltage sensors, current sensors, etc. The control system 120 may also be employed to control process conditions within the plasma processing system 100 during performance of plasma processing operations on the wafer W. For example, the control system 120 can control the type and amounts of process gas(es) supplied from the process gas supply system 191 to the

plasma processing region 182. Also, the control system 120 can control operation of the first radiofrequency signal generator 147, the second radiofrequency signal generator 149, the impedance matching system 143, the TES radiofrequency signal generator 213, and the TES impedance matching system 211. Also, the control system 120 can control operation of the DC supply 117 for the clamping electrode(s) 112. The control system 120 can also control operation of the lifting devices 133 for the lift pins 132 and operation of the door 107. The control system 120 also controls operation of the backside gas supply system 129 and the temperature control fluid circulation system 125. The control system 120 also control vertical movement of the cantilever arm assembly 115. The control system 120 also controls operation of the throttle member 196 and the pump that controls suction at the exhaust port 105. The control system 120 also controls operation of the hold-down control mechanisms 913 of the hold-down rods 911 of the TES system 1000. The control system 120 also receives input from the temperature probe of the TES system 1000. It should be understood that the control system 120 is equipped to provide for programmed and/or manual control any function within the plasma processing system 100.

[0150] In some embodiments, the control system 120 is configured to execute computer programs including sets of instructions for controlling process timing, process gas delivery system temperature, and pressure differentials, valve positions, mixture of process gases, process gas flow rate, backside cooling gas flow rate, chamber pressure, chamber temperature, wafer support structure temperature (wafer temperature), RF power levels, RF frequencies, RF pulsing, impedance matching system 143 settings, cantilever arm assembly position, bias power, and other parameters of a particular process. Other computer programs stored on memory devices associated with the control system 120 may be employed in some embodiments. In some embodiments, there is a user interface associated with the control system 120. The user interface include a display 1435 (e.g. a display screen and/or graphical software displays of the apparatus and/or process conditions), and user input devices 1437 such as pointing devices, keyboards, touch screens, microphones, etc.

[0151] Software for directing operation of the control system 120 may be designed or configured in many different ways. Computer programs for directing operation of the control system 120 to execute various wafer fabrication processes in a process sequence can be written in any conventional computer readable programming language: for example, assembly language, C, C++, Pascal, Fortran or others. Compiled object code or script is executed by the processor 1401 to perform the tasks identified in the program. The control system 120 can be programmed to control various process control parameters related to process conditions such as, for example, filter pressure differentials, process gas composition and flow rates, backside cooling gas composition and flow rates, temperature, pressure, plasma conditions, such as RF power levels

and RF frequencies, bias voltage, cooling gas/fluid pressure, and chamber wall temperature, among others. Examples of sensors that may be monitored during the wafer fabrication process include, but are not limited to, mass flow control modules, pressure sensors, such as the pressure manometers 1427 and the temperature sensors 1431. Appropriately programmed feedback and control algorithms may be used with data from these sensors to control/adjust one or more process control parameters to maintain desired process conditions.

[0152] In some implementations, the control system 120 is part of a broader fabrication control system. Such fabrication control systems can include semiconductor processing equipment, including a processing tools, chambers, and/or platforms for wafer processing, and/or specific processing components, such as a wafer pedestal, a gas flow system, etc. These fabrication control systems may be integrated with electronics for controlling their operation before, during, and after processing of the wafer. The control system 120 may control various components or subparts of the fabrication control system. The control system 120, depending on the wafer processing requirements, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, the delivery of backside cooling gases, temperature settings (e.g. heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0153] Broadly speaking, the control system 120 may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable wafer processing operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g. software). Program instructions may be instructions communicated to the control system 120 in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on the wafer W within system 100. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0154] The control system 120, in some implementations, may be a part of or coupled to a computer that is integrated with, coupled to the plasma processing system 100, or otherwise

networked to the system 100, or a combination thereof. For example, the control system 120 may be in the "cloud" of all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system 100 to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to the system 100 over a network, which may include a local network or the Internet.

[0155] The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system 100 from the remote computer. In some examples, the control system 120 receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed within the plasma processing system 100. Thus as described above, the control system 120 may be distributed, such as by comprising one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on the plasma processing system 100 in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process performed on the plasma processing system 100.

[0156] Without limitation, example systems that the control system 120 can interface with may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an atomic layer deposition (ALD) chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers. As noted above, depending on the process step or steps to be performed by the tool, the control system 120 might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0157] Embodiments described herein may also be implemented in conjunction with various computer system configurations including hand-held hardware units, microprocessor systems, microprocessor-based or programmable consumer electronics, minicomputers, mainframe computers and the like. Embodiments described herein can also be implemented in conjunction with distributed computing environments where tasks are performed by remote processing hardware units that are linked through a network. It should be understood that the embodiments described herein, particularly those associated with the control system 120, can employ various computer-implemented operations involving data stored in computer systems. These operations are those requiring physical manipulation of physical quantities. Any of the operations described herein that form part of the embodiments are useful machine operations. The embodiments also relate to a hardware unit or an apparatus for performing these operations. The apparatus may be specially constructed for a special purpose computer. When defined as a special purpose computer, the computer can also perform other processing, program execution or routines that are not part of the special purpose, while still being capable of operating for the special purpose. In some embodiments, the operations may be processed by a general purpose computer selectively activated or configured by one or more computer programs stored in the computer memory, cache, or obtained over a network. When data is obtained over a network, the data may be processed by other computers on the network, e.g. a cloud of computing resources.

[0158] Various embodiments described herein can be implemented through process control instructions instantiated as computer-readable code on a non-transitory computer-readable medium. The non-transitory computer-readable medium is any data storage hardware unit that can store data, which can be thereafter be read by a computer system. Examples of the non-transitory computer-readable medium include hard drives, network attached storage (NAS), ROM, RAM, compact disc-ROMs (CD-ROMs), CD-recordables (CD-Rs), CD-rewritables (CD-RWs), magnetic tapes, and other optical and non-optical data storage hardware units. The non-transitory computer-readable medium can include computer-readable tangible medium distributed over a network-coupled computer system so that the computer-readable code is stored and executed in a distributed fashion.

[0159] Although the foregoing disclosure includes some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications can be practiced within the scope of the appended claims. For example, it should be understood that one or more features from any embodiment disclosed herein may be combined with one or more features of any other embodiment disclosed herein. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and what is claimed is not to be limited to the details given herein, but may be modified within the scope and equivalents of the described

embodiments.

Claims

1. A system for performing a plasma process on a wafer, comprising:

a chamber configured to receive a wafer for plasma processing and having an interior defining a plasma processing region in which a plasma is provided for the plasma processing of the wafer;

a first magnetic coil disposed above the chamber and centered about an axis perpendicular to a surface plane of the wafer and through an approximate center of the wafer;

a first DC power supply configured to apply a first DC current to the first magnetic coil during the plasma processing, the applied first DC current producing a magnetic field in the plasma processing region that reduces non-uniformity of the plasma.

2. The system of claim 1, wherein the magnetic field is configured to be substantially vertical through a central region of the plasma processing region.

3. The system of claim 2, wherein the magnetic field through the central region of the plasma processing region has a strength that is less than approximately 10 Gauss.

4. The system of claim 1, wherein the magnetic field is configured to reduce a radial non-uniformity of etching that is performed by the plasma processing.

5. The system of claim 1, wherein the first magnetic coil is substantially annular in shape.

6. The system of claim 1, wherein the first magnetic coil is oriented along a horizontal plane parallel to the surface plane of the wafer.

7. The system of claim 1, wherein an inner diameter of the first magnetic coil is in the range of approximately 15 to 20 inches.

8. The system of claim 1, wherein the first magnetic coil includes a plurality of turns of magnet wire.

9. The system of claim 1, further comprising:

a second magnetic coil disposed above the chamber, the second magnetic coil being concentric with the first magnetic coil;

a second DC power supply configured to apply a second DC current to the second magnetic coil during the plasma processing, the applied second DC current contributing to producing the magnetic field in the plasma processing region that reduces non-uniformity of the plasma.

10. The system of claim 9, wherein the second magnetic coil is substantially oriented along a same horizontal plane as the first magnetic coil.

11. The system of claim 9, wherein the first DC current and the second DC current are configured to have a same magnitude or a different magnitude.

12. The system of claim 9, wherein the first DC current and the second DC current are configured to be applied in a same direction or in opposite directions.

13. The system of claim 9,

wherein an inner diameter of the first magnetic coil is in the range of approximately 10 to 15 inches; and,

wherein an inner diameter of the second magnetic coil is in the range of approximately 15 to 25 inches.

14. The system of claim 1, further comprising:

a second magnetic coil configured to laterally surround the plasma processing region;

a second DC power supply configured to apply a second DC current to the second magnetic coil during the plasma processing, the applied second DC current contributing to producing the magnetic field in the plasma processing region that reduces non-uniformity of the plasma.

15. The system of claim 1, further comprising:

a second magnetic coil disposed below the plasma processing region;

a second DC power supply configured to apply a second DC current to the second magnetic coil during the plasma processing, the applied second DC current contributing to producing the magnetic field in the plasma processing region that reduces non-uniformity of the plasma.

16. A method for performing a plasma process on a wafer, comprising:

moving a wafer into a chamber configured for plasma processing, an interior of the chamber defining a plasma processing region;

providing a plasma in the plasma processing region for the plasma processing of the wafer; and

applying a DC current to a magnetic coil during the plasma processing, the applied DC current producing a magnetic field in the plasma processing region that reduces non-uniformity of the plasma;

wherein the magnetic coil is disposed above the chamber and centered about an axis perpendicular to a surface plane of the wafer and through an approximate center of the wafer.

17. The method of claim 16, wherein the magnetic field is configured to be substantially vertical through a central region of the plasma processing region.

18. The method of claim 17, wherein the magnetic field through the central region of the plasma processing region has a strength that is less than approximately 10 Gauss.

19. The method of claim 16, wherein the magnetic field is configured to reduce a radial non-uniformity of etching that is performed by the plasma processing.

20. The method of claim 16, wherein the magnetic coil is substantially annular in shape.

21. The method of claim 16, wherein the magnetic coil is oriented along a horizontal plane parallel to the surface plane of the wafer.

22. The method of claim 16, wherein an inner diameter of the first magnetic coil is in the range of approximately 15 to 20 inches.

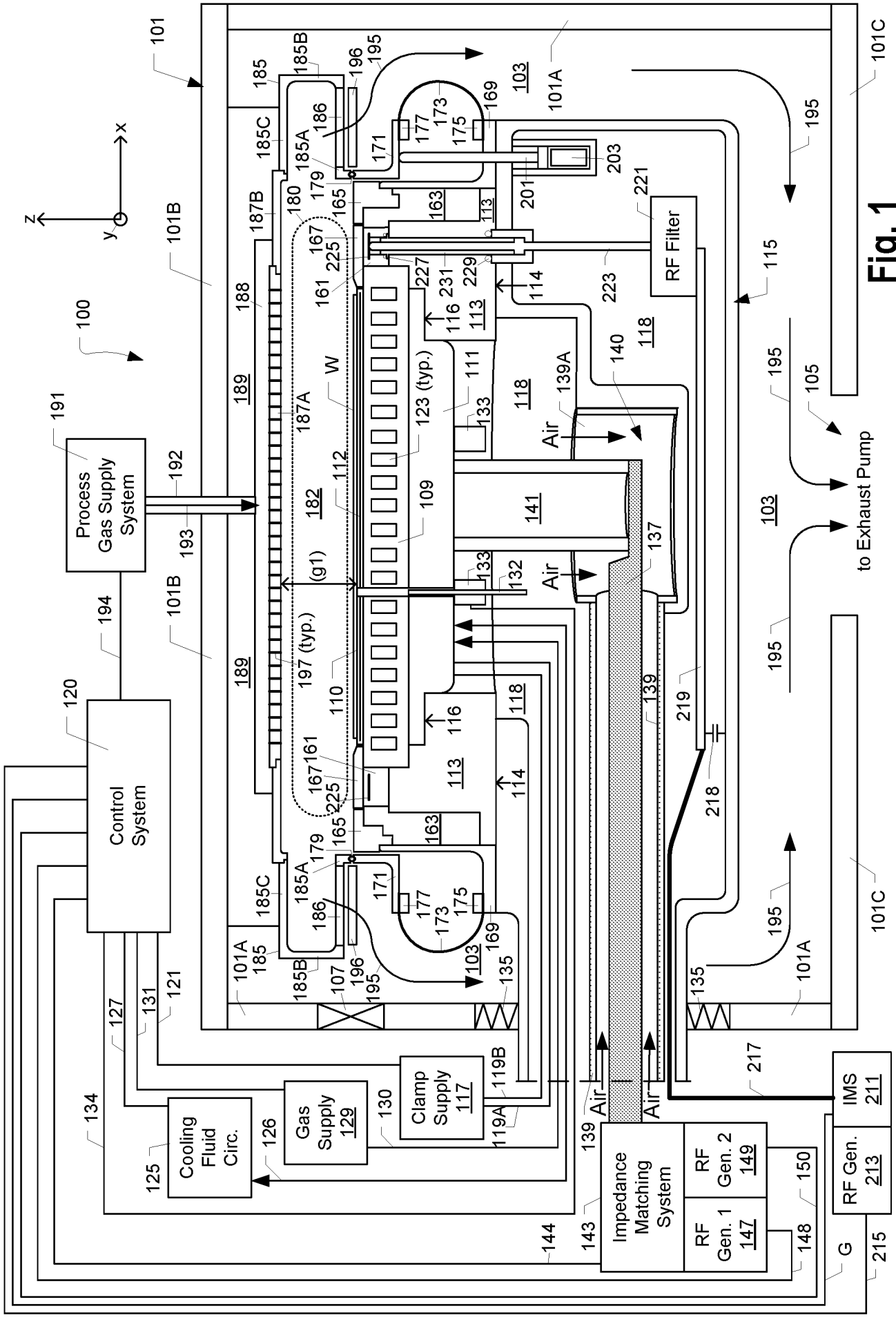
Process Gas Supply System
Control System
Cooling Fluid Circ.
Gas Supply 129
Clamp Supply 117
Impedance Matching System
RF Gen. 1 147
RF Gen. 2 149
RF Gen. 213
IMS 211
RF Filter
to Exhaust Pump
Air
W
(g1)
(typ.)
x
y
z

Fig. 1

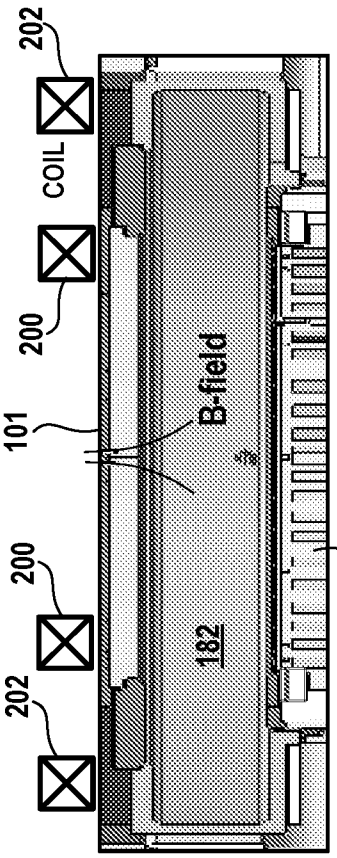

Fig. 2B

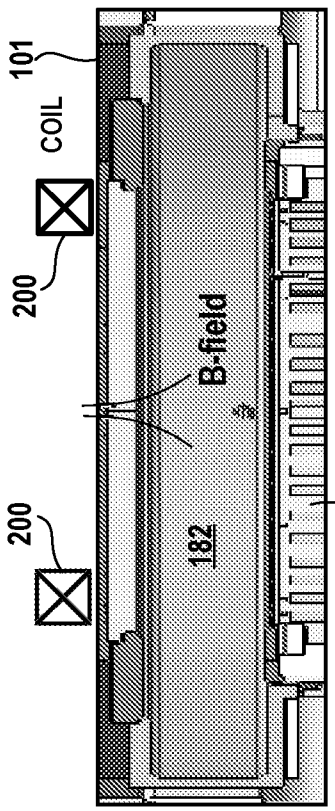

Fig. 2A

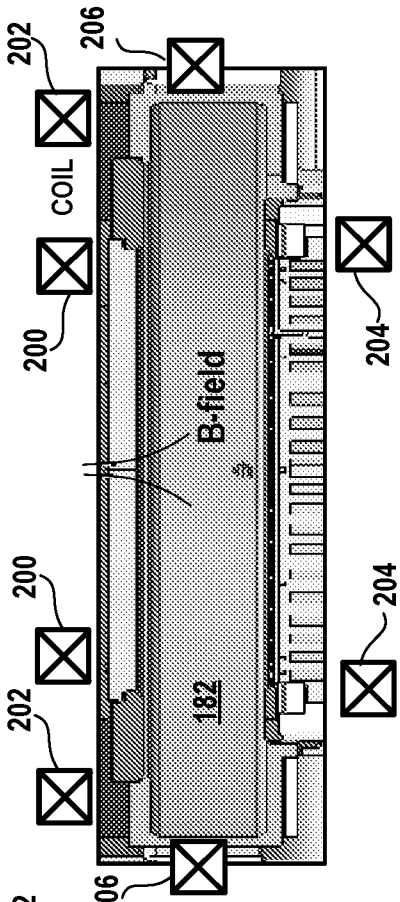

Fig. 2D

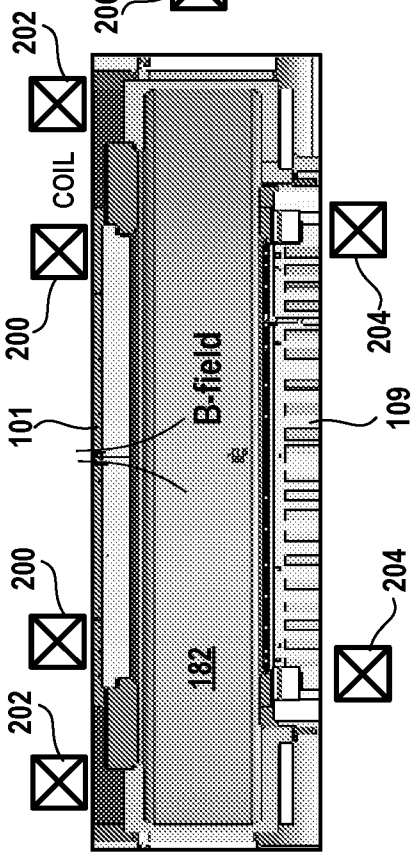

Fig. 2C

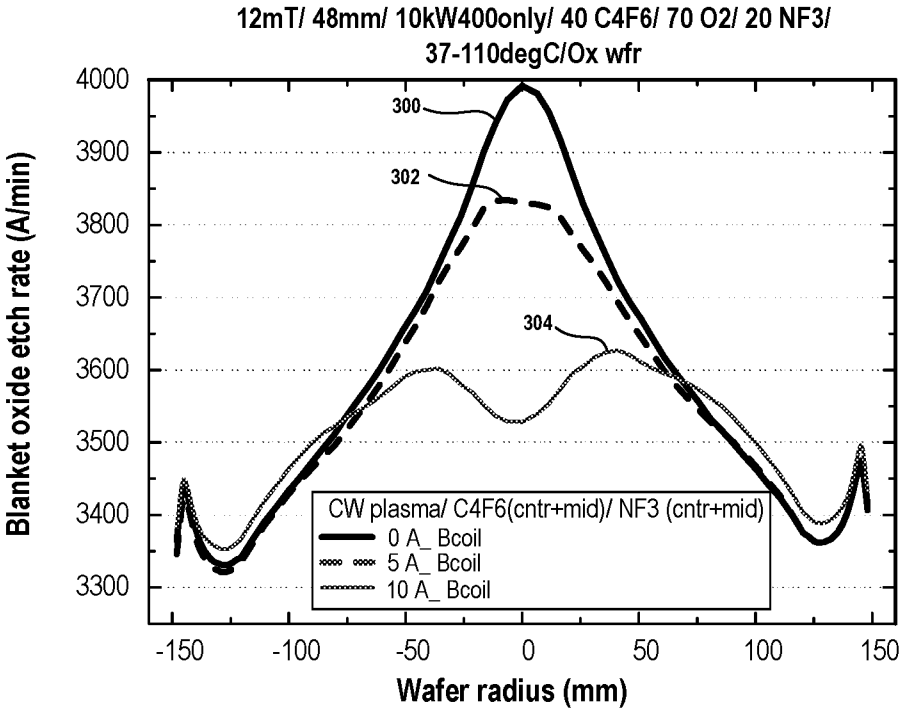
12mT/ 48mm/ 10kW400only/ 40 C4F6/ 70 O2/ 20 NF3/
37-110degC/Ox wfr
Blanket oxide etch rate (A/min)
4000
3900
3800
3700
3600
3500
3400
3300
300
302
304
CW plasma/ C4F6(cntr+mid)/ NF3 (cntr+mid)
0 A_ Bcoil
5 A_ Bcoil
10 A_ Bcoil
-150
-100
-50
0
50
100
150
Wafer radius (mm)

Fig. 3A

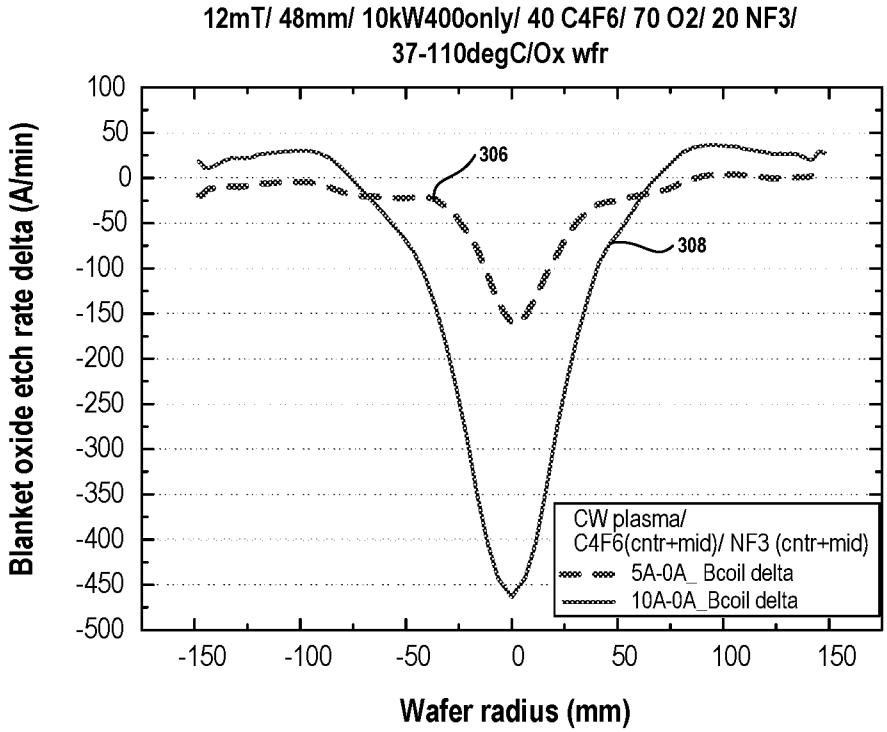
12mT/ 48mm/ 10kW400only/ 40 C4F6/ 70 O2/ 20 NF3/
37-110degC/Ox wfr
Blanket oxide etch rate delta (A/min)
100
50
0
-50
-100
-150
-200
-250
-300
-350
-400
-450
-500
306
308
CW plasma/
C4F6(cntr+mid)/ NF3 (cntr+mid)
5A-0A_ Bcoil delta
10A-0A_Bcoil delta
-150
-100
-50
0
50
100
150
Wafer radius (mm)

Fig. 3B

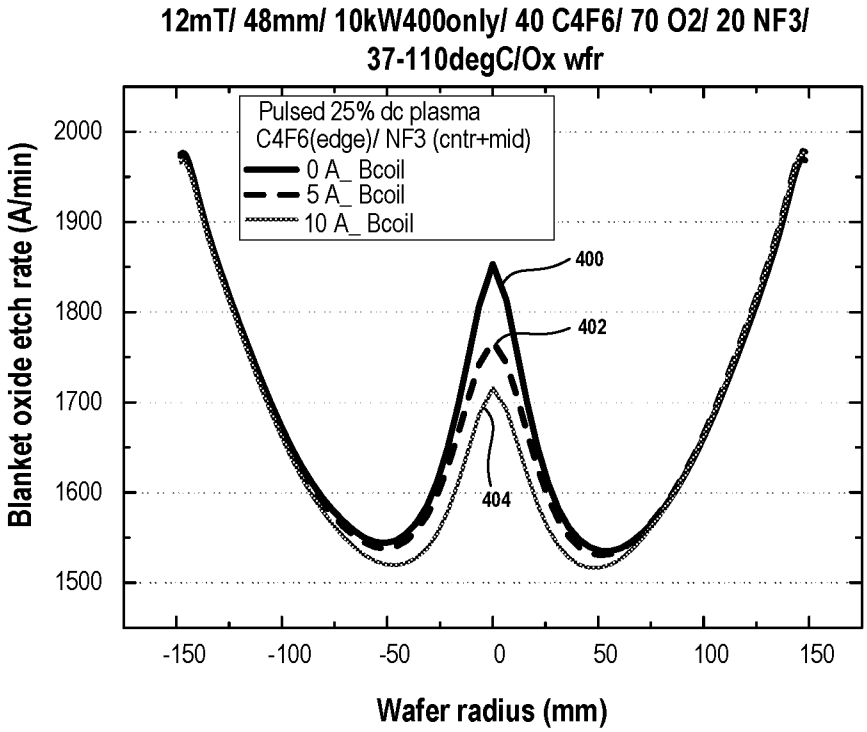
12mT/ 48mm/ 10kW400only/ 40 C4F6/ 70 O2/ 20 NF3/
37-110degC/Ox wfr
Pulsed 25% dc plasma
C4F6(edge)/ NF3 (cntr+mid)
0 A_ Bcoil
5 A_ Bcoil
10 A_ Bcoil
400
402
404
Blanket oxide etch rate (A/min)
2000
1900
1800
1700
1600
1500
-150
-100
-50
0
50
100
150
Wafer radius (mm)

Fig. 4A

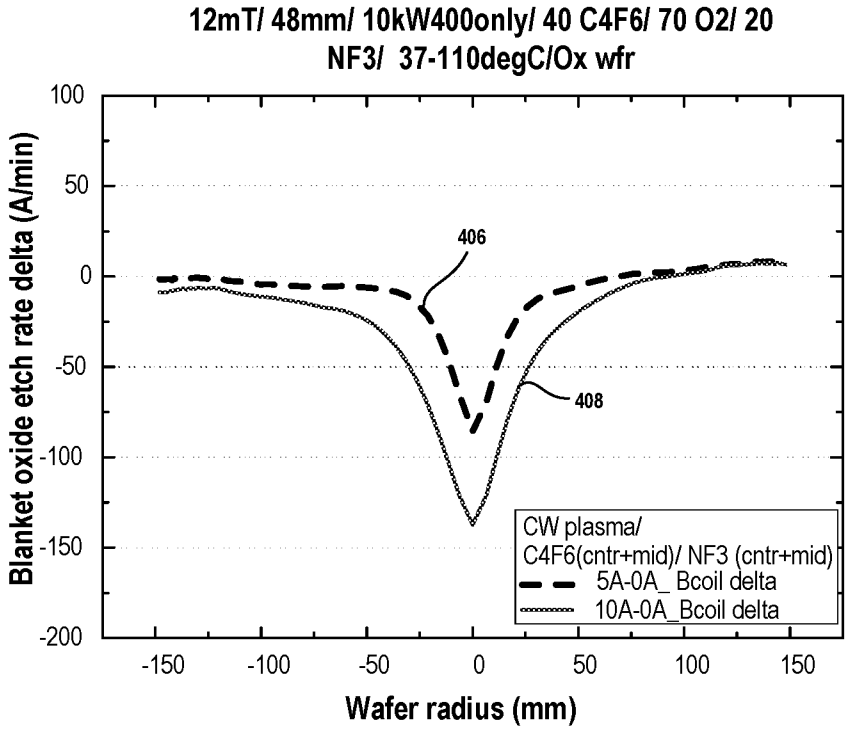
12mT/ 48mm/ 10kW400only/ 40 C4F6/ 70 O2/ 20
NF3/ 37-110degC/Ox wfr
406
408
CW plasma/
C4F6(cntr+mid)/ NF3 (cntr+mid)
5A-0A_ Bcoil delta
10A-0A_Bcoil delta
Blanket oxide etch rate delta (A/min)
100
50
0
-50
-100
-150
-200
-150
-100
-50
0
50
100
150
Wafer radius (mm)

Fig. 4B

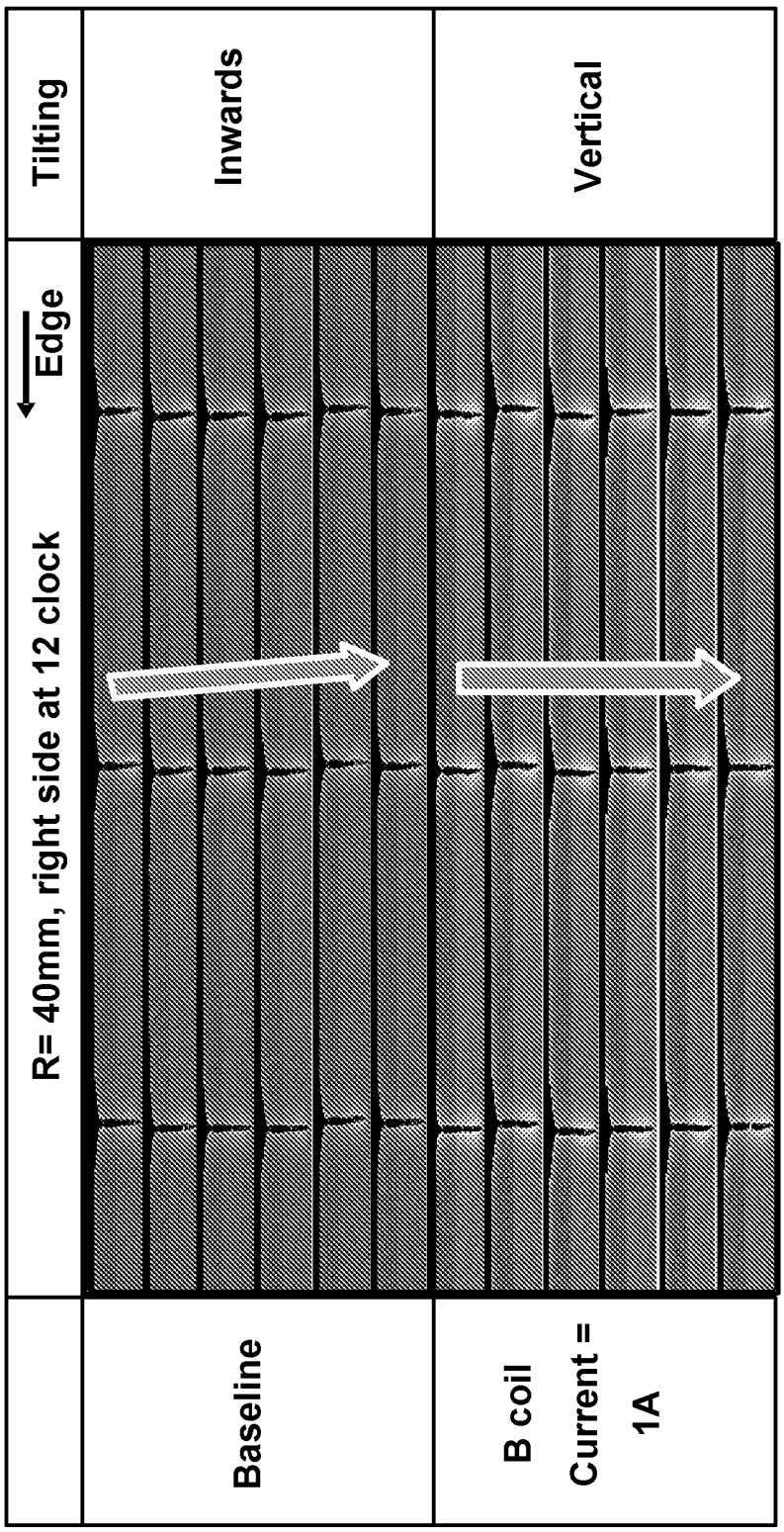
Tilting
Inwards
Vertical
Edge
R= 40mm, right side at 12 clock
Baseline
B coil
Current =
1A

Fig. 5

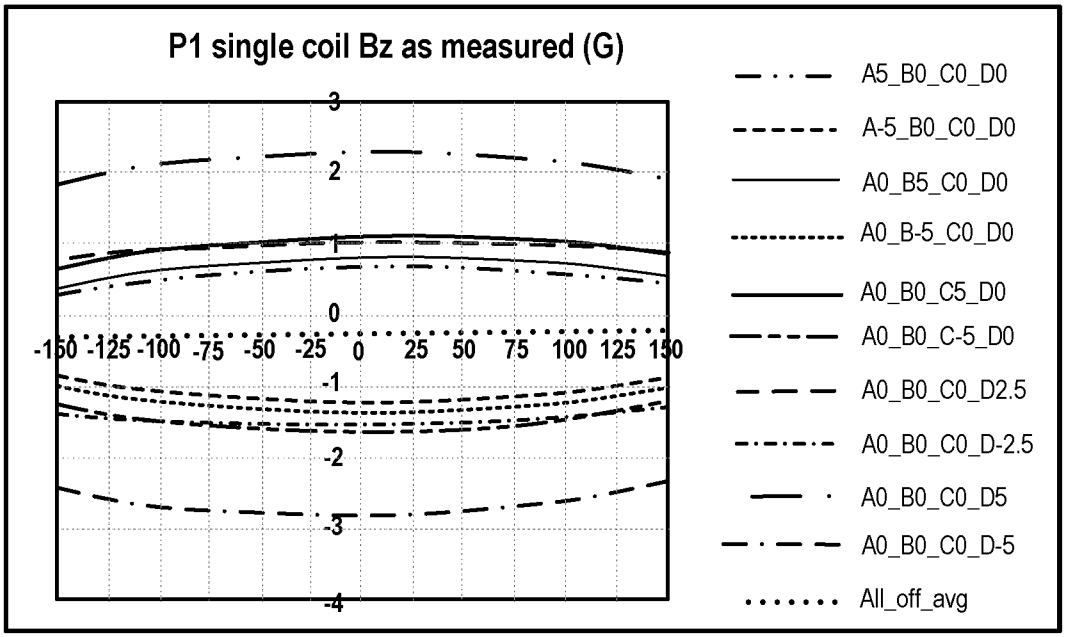
P1 single coil Bz as measured (G)
3
2
1
0
-1
-2
-3
-4
-150 -125 -100 -75 -50 -25 0 25 50 75 100 125 150
A5_B0_C0_D0
A-5_B0_C0_D0
A0_B5_C0_D0
A0_B-5_C0_D0
A0_B0_C5_D0
A0_B0_C-5_D0
A0_B0_C0_D2.5
A0_B0_C0_D-2.5
A0_B0_C0_D5
A0_B0_C0_D-5
All_off_avg

Fig. 6A

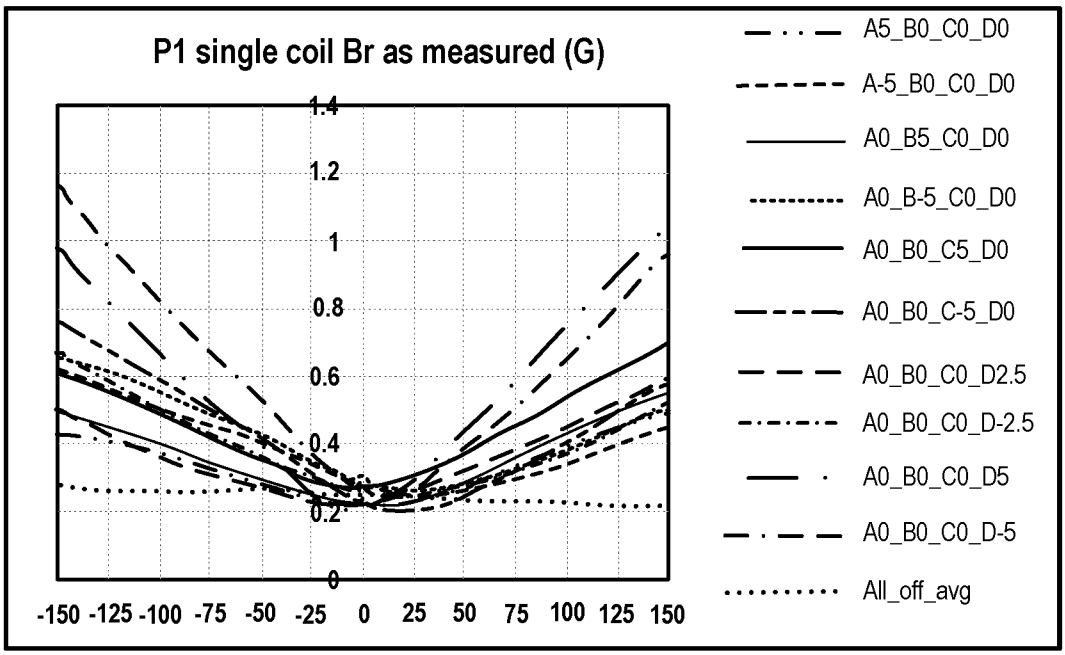
P1 single coil Br as measured (G)
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-150 -125 -100 -75 -50 -25 0 25 50 75 100 125 150
A5_B0_C0_D0
A-5_B0_C0_D0
A0_B5_C0_D0
A0_B-5_C0_D0
A0_B0_C5_D0
A0_B0_C-5_D0
A0_B0_C0_D2.5
A0_B0_C0_D-2.5
A0_B0_C0_D5
A0_B0_C0_D-5
All_off_avg

Fig. 6B

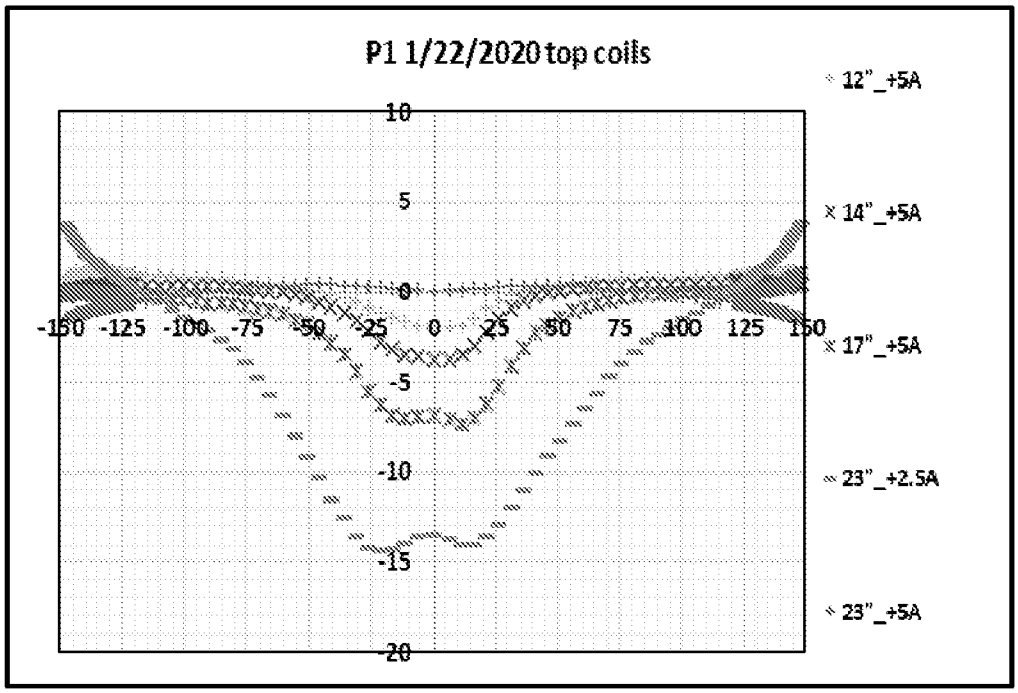
P1 1/22/2020 top coils
12"_+5A
14"_+5A
17"_+5A
23"_+2.5A
23"_+5A
10
5
0
-5
-10
-15
-20
-150 -125 -100 -75 -50 -25 0 25 50 75 100 125 150

Fig. 7A

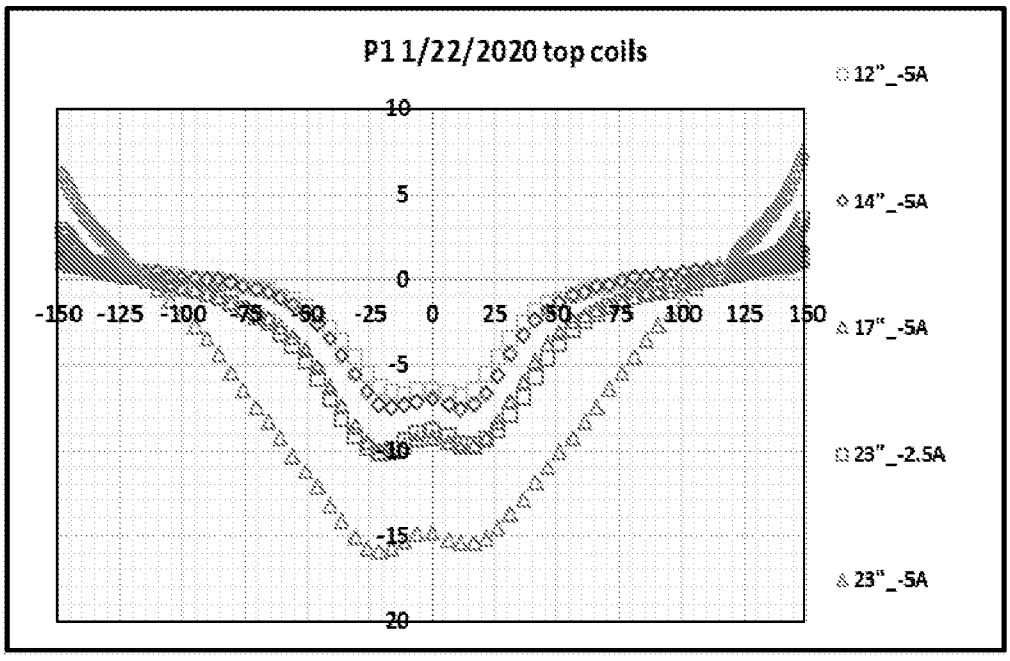
P1 1/22/2020 top coils
12"_-5A
14"_-5A
17"_-5A
23"_-2.5A
23"_-5A
10
5
0
-5
-10
-15
-20
-150 -125 -100 -75 -50 -25 0 25 50 75 100 125 150

Fig. 7B

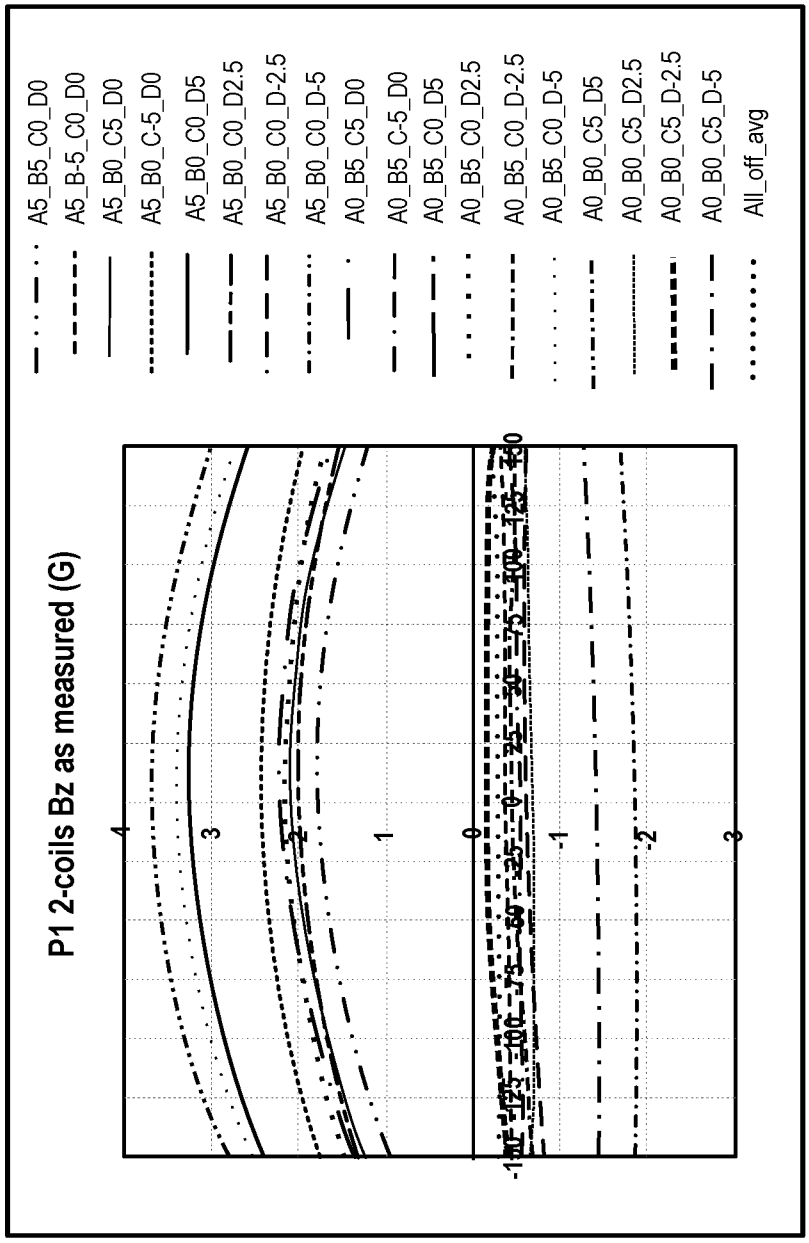
P1 2-coils Bz as measured (G)
A5_B5_C0_D0
A5_B-5_C0_D0
A5_B0_C5_D0
A5_B0_C-5_D0
A5_B0_C0_D5
A5_B0_C0_D2.5
A5_B0_C0_D-2.5
A5_B0_C0_D-5
A0_B5_C5_D0
A0_B5_C-5_D0
A0_B5_C0_D5
A0_B5_C0_D2.5
A0_B5_C0_D-2.5
A0_B5_C0_D-5
A0_B0_C5_D5
A0_B0_C5_D2.5
A0_B0_C5_D-2.5
A0_B0_C5_D-5
All_off_avg
4
3
2
1
0
-1
-2
3

Fig. 8A

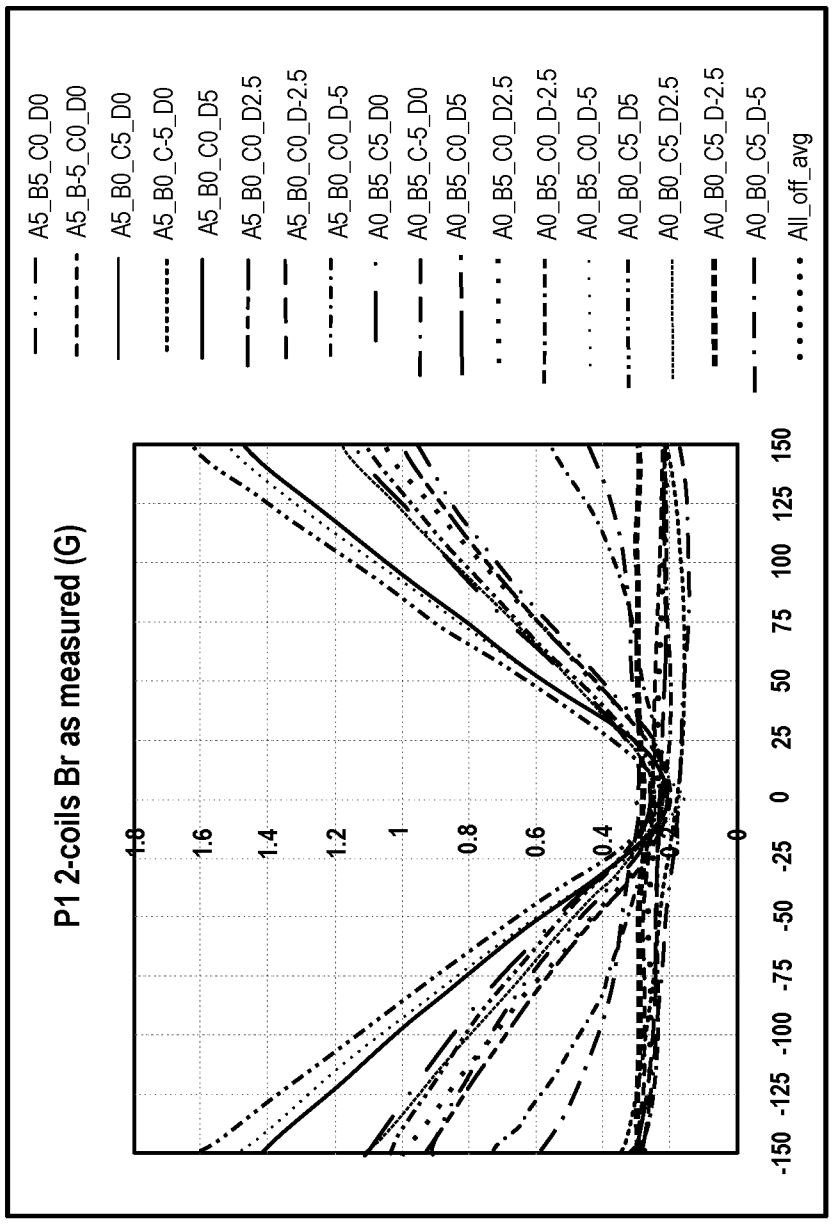
P1 2-coils Br as measured (G)
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-150 -125 -100 -75 -50 -25 0 25 50 75 100 125 150
A5_B5_C0_D0
A5_B-5_C0_D0
A5_B0_C5_D0
A5_B0_C-5_D0
A5_B0_C0_D5
A5_B0_C0_D2.5
A5_B0_C0_D-2.5
A5_B0_C0_D-5
A0_B5_C5_D0
A0_B5_C-5_D0
A0_B5_C0_D5
A0_B5_C0_D2.5
A0_B5_C0_D-2.5
A0_B5_C0_D-5
A0_B0_C5_D5
A0_B0_C5_D2.5
A0_B0_C5_D-2.5
A0_B0_C5_D-5
All_off_avg

Fig. 8B

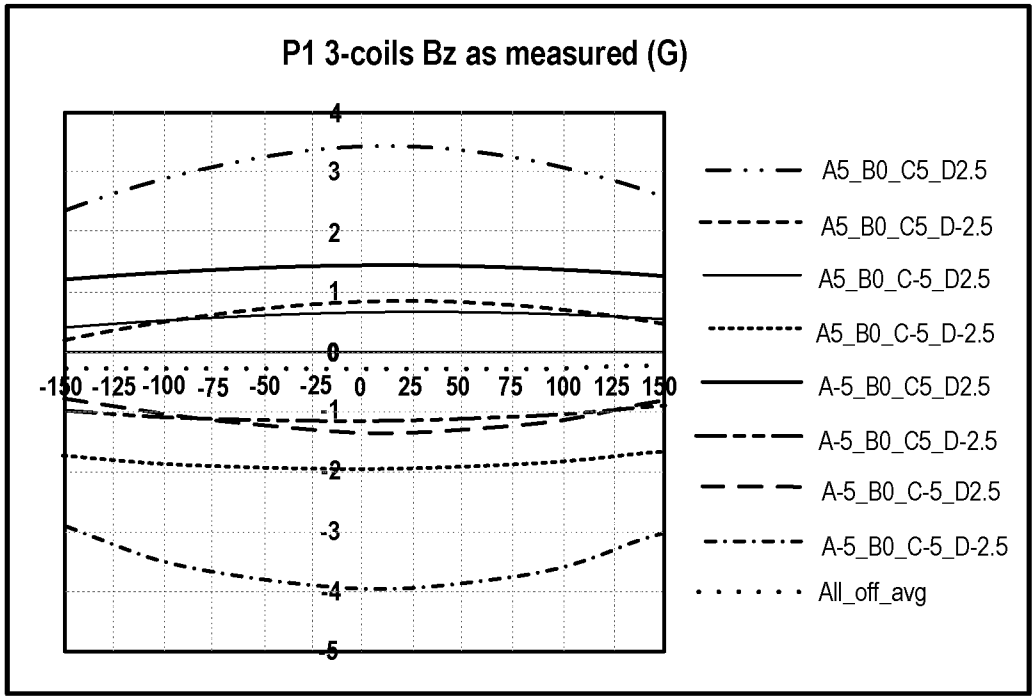
P1 3-coils Bz as measured (G)
4
3
2
1
0
-1
-2
-3
-4
-5
-150 -125 -100 -75 -50 -25 0 25 50 75 100 125 150
A5_B0_C5_D2.5
A5_B0_C5_D-2.5
A5_B0_C-5_D2.5
A5_B0_C-5_D-2.5
A-5_B0_C5_D2.5
A-5_B0_C5_D-2.5
A-5_B0_C-5_D2.5
A-5_B0_C-5_D-2.5
All_off_avg

Fig. 9A

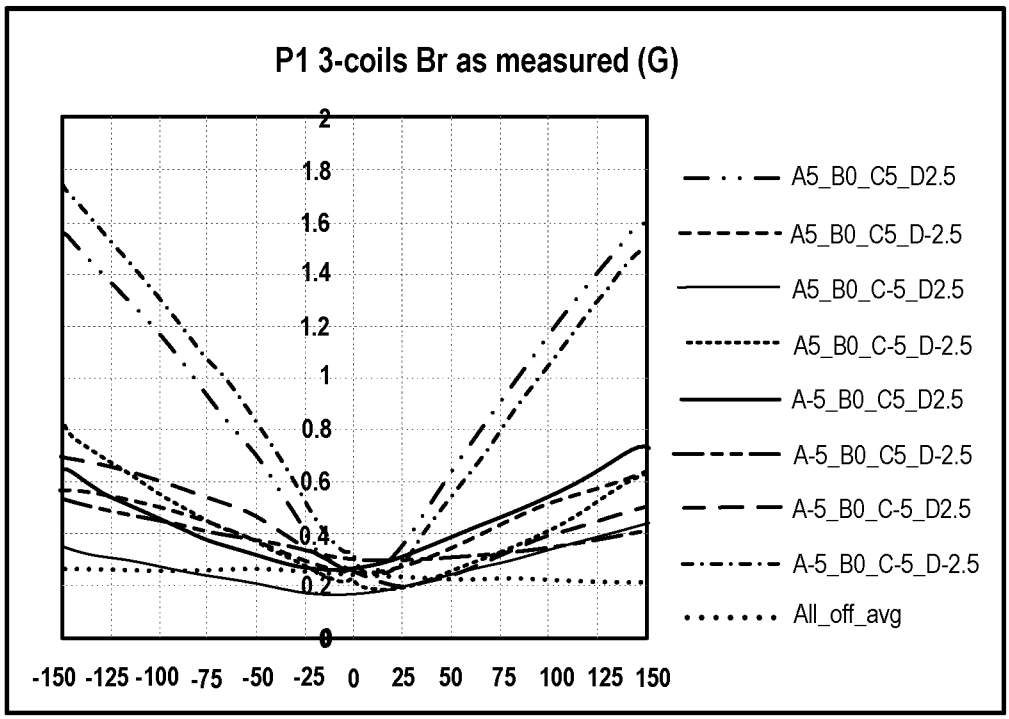
P1 3-coils Br as measured (G)
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-150 -125 -100 -75 -50 -25 0 25 50 75 100 125 150
A5_B0_C5_D2.5
A5_B0_C5_D-2.5
A5_B0_C-5_D2.5
A5_B0_C-5_D-2.5
A-5_B0_C5_D2.5
A-5_B0_C5_D-2.5
A-5_B0_C-5_D2.5
A-5_B0_C-5_D-2.5
All_off_avg

Fig. 9B

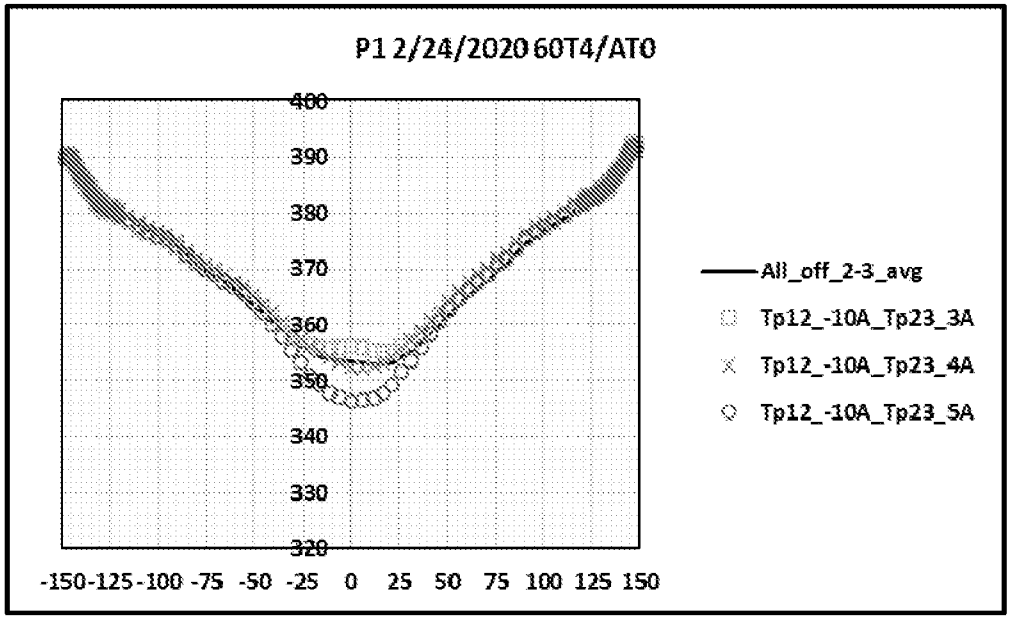

Fig. 10A

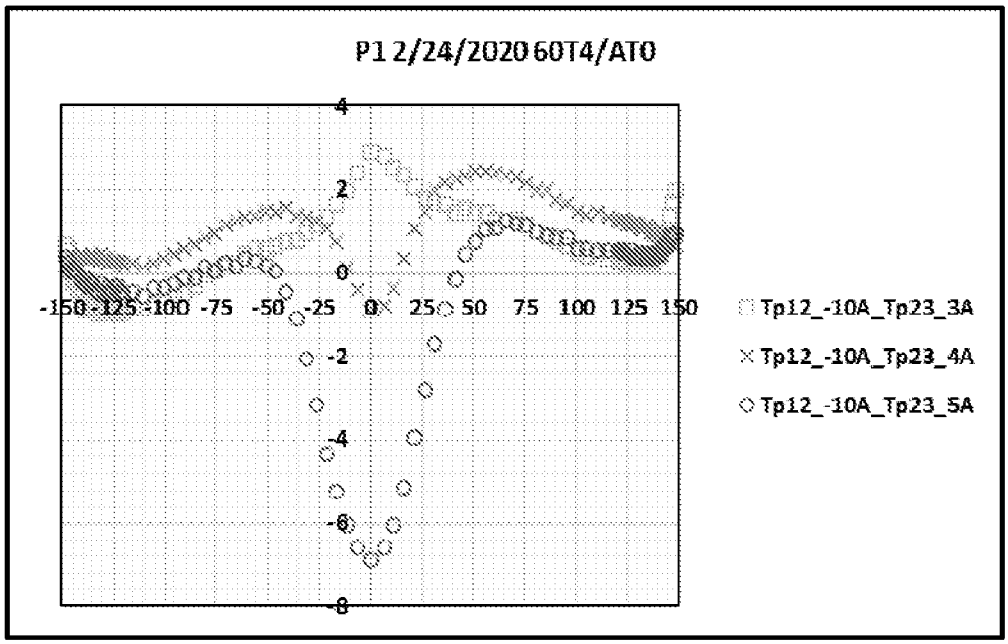

Fig. 10B

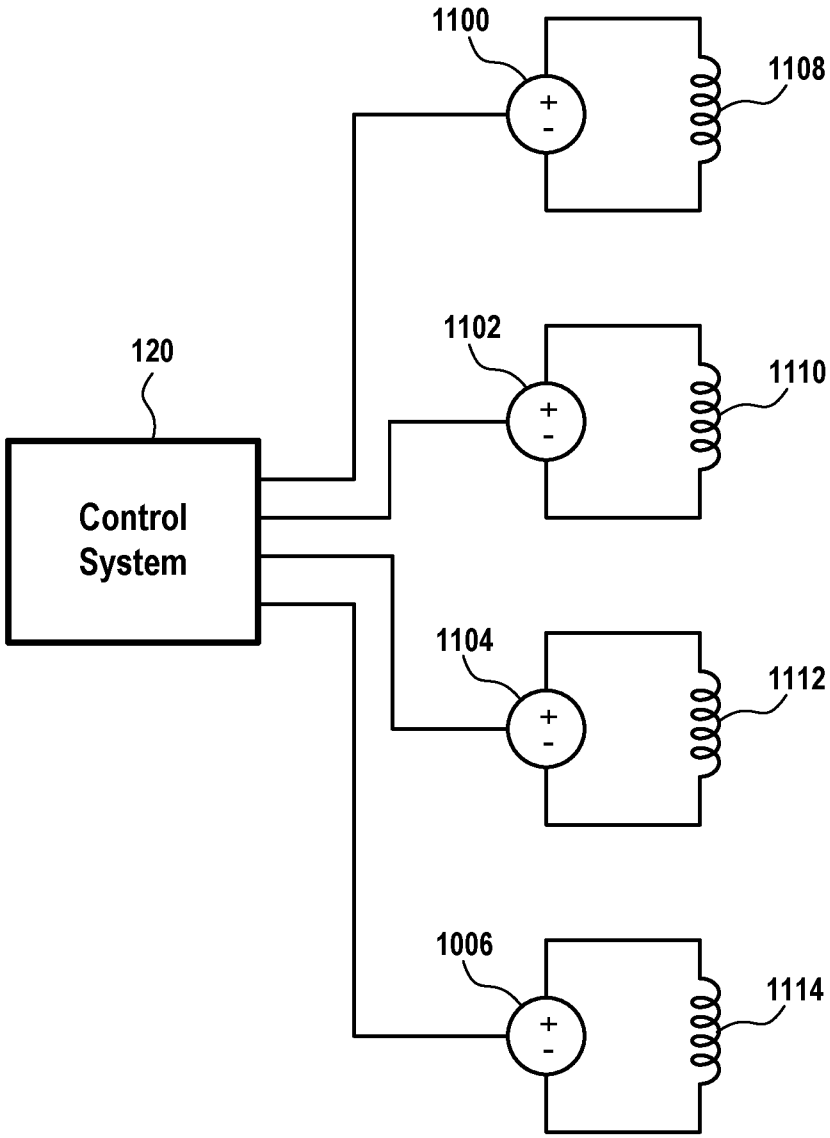

Fig. 11

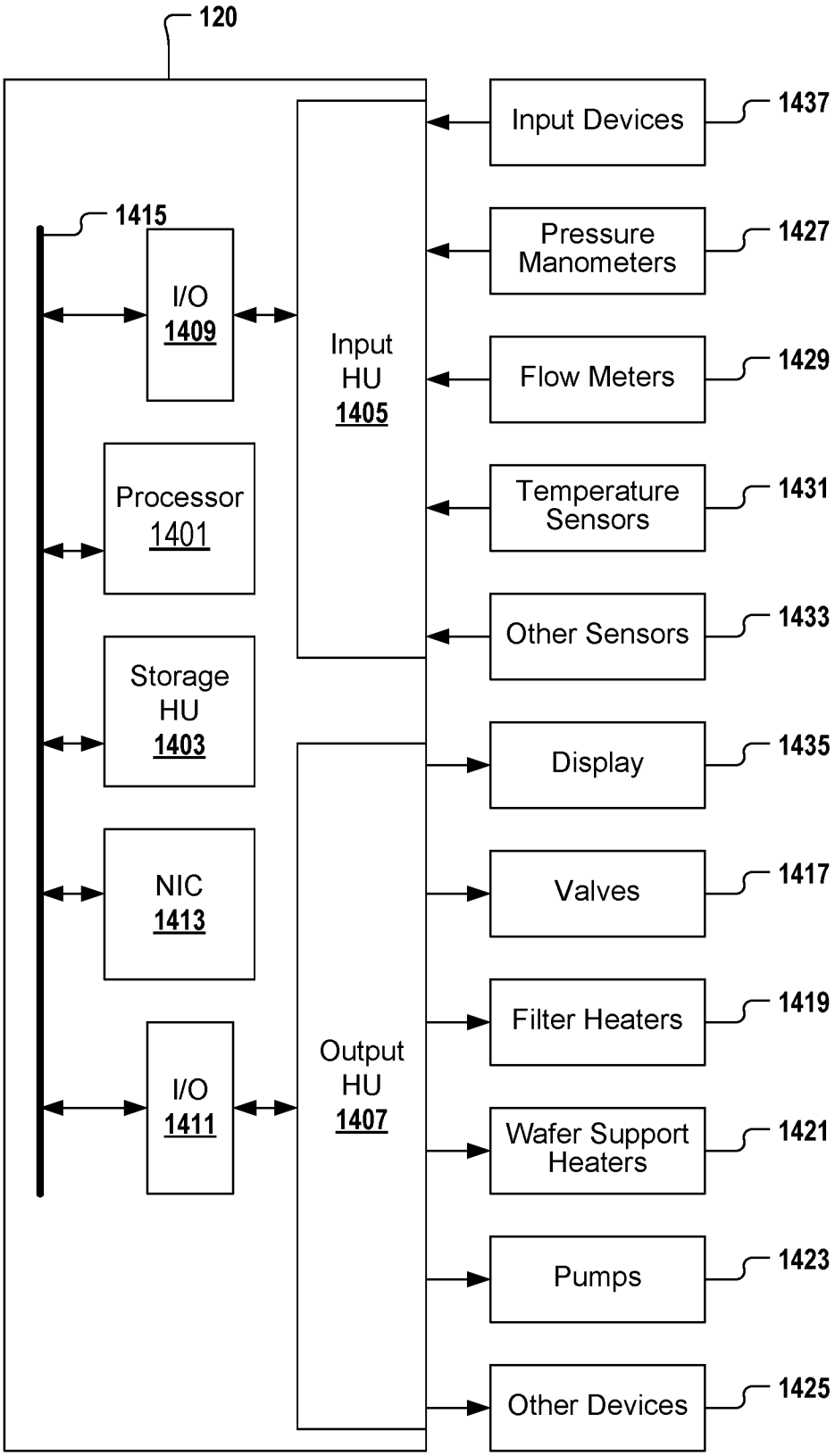
120
1415
I/O
1409
Processor
1401
Storage
HU
1403
NIC
1413
I/O
1411
Input
HU
1405
Output
HU
1407
Input Devices
1437
Pressure
Manometers
1427
Flow Meters
1429
Temperature
Sensors
1431
Other Sensors
1433
Display
1435
Valves
1417
Filter Heaters
1419
Wafer Support
Heaters
1421
Pumps
1423
Other Devices
1425

Fig. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2021/057786

A. CLASSIFICATION OF SUBJECT MATTER

H01J 37/32(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01J 37/32(2006.01); C23C 16/50(2006.01); H01L 21/3065(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: plasma, uniformity, control, magnetic field, chamber, coil

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2019-0006153 A1 (HITACHI HIGH-TECHNOLOGIES CORPORATION) 03 January 2019 (2019-01-03) See paragraphs 37-55, 140; and figure 1.	1-22
Y	US 6245190 B1 (TOSHIO MASUDA et al.) 12 June 2001 (2001-06-12) See column 12, lines 21-41, column 23, lines 40-59; and figure 1.	1-22
A	US 2003-0006008 A1 (KEIJI HORIOKA et al.) 09 January 2003 (2003-01-09) See the entire document.	1-22
A	JP 2003-523483 A (EURPOEAN COMMUNITY(EC)) 05 August 2003 (2003-08-05) See the entire document.	1-22
A	KR 10-1997-0015781 A (CANON KABUSHIKI KAISHA) 28 April 1997 (1997-04-28) See the entire document.	1-22

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
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"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 February 2022	**28 February 2022**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office **189 Cheongsa-ro, Seo-gu, Daejeon** **35208, Republic of Korea**	**PARK, Hye Lyun**
Facsimile No. **+82-42-481-8578**	Telephone No. **+82-42-481-3463**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2021/057786

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
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		EP 0764969 A3	12 November 1997
		EP 0764969 B1	04 December 2002
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		US 5985091 A	16 November 1999