

(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
13 March 2008 (13.03.2008)

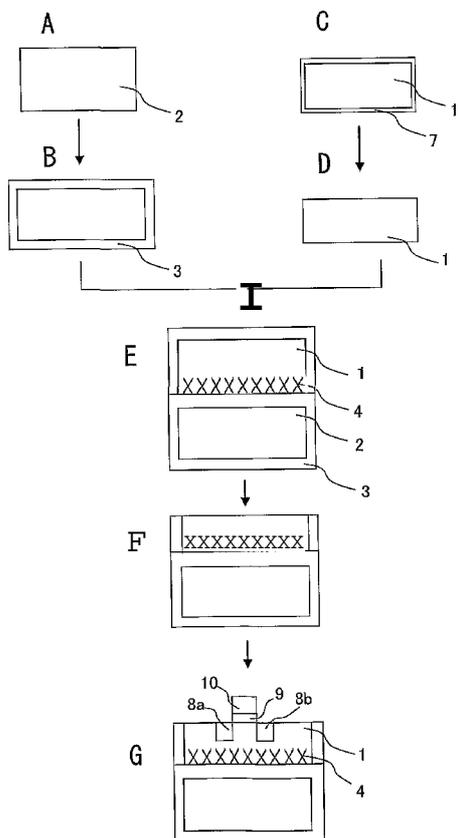
PCT

(10) International Publication Number  
**WO 2008/029607 A1**

- (51) **International Patent Classification:**  
*HOIL 21/762 (2006.01) HOIL 21/322 (2006.01)*
- (21) **International Application Number:**  
**PCT/JP2007/066075**
- (22) **International Filing Date:** 13 August 2007 (13.08.2007)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**  
2006-242670 7 September 2006 (07.09.2006) **JP**
- (71) **Applicant (for all designated States except US):** **NEC Electronics Corporation** [JP/JP]; 1753 Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 2118668 (**JP**).
- (72) **Inventor; and**
- (75) **Inventor/Applicant (for US only):** **KATO, Hiroaki** [JP/JP]; c/o NEC Electronics Corporation, 1753 Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 2118668 (**JP**).
- (74) **Agent:** **IEIRI, Takeshi; HIBIKI IP** Law Firm, Asahi Bldg. 10th Floor, 3-33-8, Tsuruya-cho, Kanagawa-ku, Yokohama-shi, Kanagawa 2210835 (**JP**).
- (81) **Designated States (unless otherwise indicated, for every kind of national protection available):** AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW
- (84) **Designated States (unless otherwise indicated, for every kind of regional protection available):** ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL,

[Continued on next page]

(54) **Title:** MANUFACTURING METHOD OF SEMICONDUCTOR SUBSTRATE AND MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE



(57) **Abstract:** To provide a manufacturing method of a semiconductor substrate and a manufacturing method of a semiconductor device, which prevent reduction in breakdown voltage of a gate oxide film of a device formed in a semiconductor substrate to improve a reliability of the gate oxide film. A manufacturing method of a semiconductor substrate according to the present invention includes: exposing a silicon surface of an active layer substrate 1 made of single-crystal silicon, to which a semiconductor device is formed; forming an oxide film on a support substrate 2 made of single-crystal silicon; and bonding the silicon surface of the active layer substrate 1 to the oxide film formed on the support substrate 2. The silicon surface of the active layer substrate 1 is exposed by removing a spontaneous oxidation film 7 formed on the surface.

WO 2008/029607 A1



---

PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM,  
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**  
— *with international search report*

**DESCRIPTION**

MANUFACTURING METHOD OF SEMICONDUCTOR SUBSTRATE AND  
MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

5

**Technical Field**

[0001]

The present invention relates to a manufacturing method of a semiconductor substrate and a manufacturing method of a semiconductor device. In particular, the invention relates to a manufacturing method of a bonding SOI substrate, and a manufacturing method of a semiconductor device using a bonding SOI substrate .

15 **Background Art**

[0002]

High-speed operations have been required of a large scale integrated circuit. Reduction of a parasitic capacitance is indispensable for higher-speed operations of the large scale integrated circuit. An SOI (Silicon on Insulator) substrate technique has been expected as a promising technique for reducing this parasitic capacitance. Fig. H A is a schematic diagram of a semiconductor device 90 (hereinafter referred to as "SOI device 90") where a transistor and the like are formed in an SOI substrate. Fig.

25

11B is a schematic diagram of a semiconductor device 100 (hereinafter referred to as "Si substrate device 100") where a transistor and the like are formed in an Si substrate. As shown in Fig. HA, the SOI substrate is constituted of an Si-made active layer substrate (SOI layer) 91, a support substrate 92 supporting the SOI layer 91 from the rear side, and a buried oxide film ( $\text{SiO}_2$ ) 93 having the thickness of several  $\mu\text{m}$  and formed between the two substrates. A device 101 such as a transistor is formed in the active layer substrate 91 of the SOI substrate to thereby complete the SOI device 90. The SOI device 90 is separated into the SOI layer 91 and the support substrate 92 across the buried oxide film 93. Therefore, a transistor or the like can be formed in the thin SOI layer 91 in the SOI device 90, and a parasitic capacitance of source/drain regions can be reduced to thereby enable higher-speed operations than the Si substrate device 100 of the related art, in which a transistor or the like is directly formed in the Si substrate 94 as shown in Fig. HB.

[0003]

20 However, the SOI device 90 has a problem that defects are likely to occur in a gate oxide film of the device due to metal impurities generated in production facility or the like at the time of manufacturing a device. As shown in Fig. HB, the Si substrate device 100 of the related art includes  
25 gettering sites enough to trap metal impurities 95, in the Si

substrate 94. The gettering sites trap the metal impurities  
95 or the like. Thus, even if metal impurities are mixed in  
the Si substrate 94 during a manufacturing process of the Si  
substrate device 100, the gettering sites trap the metal  
5 impurities 95 or the like. As a result, defects of the gate  
oxide film 96 in the device due to the metal impurities 95 or  
the like can be suppressed.

[0004]

On the other hand, in the SOI device 90 of Fig. HA,  
10 the SOI layer 91 is thin, so the number of gettering sites  
that trap the metal impurities 95 is small. Further, SiO<sub>2</sub>  
for forming the buried oxide film 93 is interposed between  
the Si-made SOI layer 91 and the support substrate 92. Since  
a diffusion coefficient of metal is lower in SiO<sub>2</sub> than in Si,  
15 the metal impurities 95 cannot pass through the SiO<sub>2</sub> with  
ease. As a result, the metal impurities 95 are accumulated  
in the SOI layer 91. That is, the metal impurities 95 are  
accumulated in the SOI layer 91, with the result that the  
metal impurities 95 are more likely to adversely affect a  
20 device formed in the SOI layer substrate 91. The  
contamination with the metal impurities 95 might cause  
junction leak or reduction in breakdown voltage of a gate  
oxide film.

[0005]

25 As a method of suppressing defects of the gate oxide

film due to metal impurities, there is a gettering technique that forming a crystal defect in a substrate and capturing metal impurities with the crystal defect. The gettering technique is disclosed in Patent Document 1. Referring to 5 Figs. 12A to 12H, a manufacturing method of an SOI device with gettering sites as disclosed in Patent Document 1 is described. As shown in Fig. 12A, a support substrate 92 is first prepared. As shown in Fig. 12B, a buried oxide film 93 is then formed to surround the support substrate 92.

10 [0006]

As shown in Fig. 12C, an active layer substrate 91 is prepared, and a predetermined amount of dopant such as arsenic or antimony or the like is selectively doped to the active layer substrate 91. At this time, the surface portion 15 of the Si-made active layer substrate 91 is turned amorphous through the dopant injection to form an amorphous layer 98. As shown in Fig. 12D, the active layer substrate 91 is subjected to heat treatment next to diffuse the dopant. At this time, the amorphous layer 98 is recrystallized. Here, 20 the heat treatment for diffusing the dopant is carried out under an oxygen atmosphere, so oxygen, silicon, and the like are supplied to the amorphous layer 98 to hinder the amorphous layer 98 from recrystallizing, and crystal defects 97 are formed. At this time, a silicon oxide film 99 is 25 formed around the active layer substrate 91. After that, as

shown in Fig. 12E, the active layer substrate 91 is treated with SC1 cleaning and SC2 cleaning prior to bonding for the purpose of removing contaminants. As shown in Fig. 12F, the support substrate 92 with the buried oxide film 93 is then bonded to the active layer substrate 91 on the crystal defect 97 side, followed by heat treatment. As shown in Fig. 12G, the active layer substrate 91 is ground or polished. As shown in Fig. 12H, a device 101 such as a transistor or the like is formed in the ground or polished surface of the active layer substrate 91 to thereby complete an SOI device.

[Patent Document 1]

Japanese Unexamined Patent Application Publication No. 2006-5341

## 15 Disclosure of the Invention

[0007]

However, in the above technique as disclosed in Patent Document 1, the crystal defects 97 cannot be formed unless a dopant is injected and then heat treatment is carried out, so a dopant injection step and a heat treatment step cannot be omitted. That is, there arises a problem in that the number of manufacturing steps for an SOI device is increased. There is another problem that a breakdown voltage is lowered in such a device that a depletion layer reaches where a dopant is injected.

[0008]

In one embodiment of the present invention, a manufacturing method of a semiconductor substrate includes: exposing a silicon surface of an active layer substrate made of single-crystal silicon, to which a semiconductor device is formed; forming an oxide film on a support substrate made of single-crystal silicon; and bonding the silicon surface of the active layer substrate to the oxide film formed on the support substrate.

[0009]

According to the one embodiment of the present invention, the exposed surface of the active layer substrate made of single-crystal silicon is bonded to the support substrate made of single-crystal silicon with the oxide film formed thereon. Hence, crystal defects are formed in the silicon surface as a bonding surface between the silicon surface of the active layer substrate and the oxide film formed on the support substrate.

[0010]

According to a manufacturing method of a semiconductor substrate of the present invention, crystal defects formed in an active layer substrate trap metal impurities to prevent reduction in breakdown voltage of a gate oxide film of a device formed in a semiconductor substrate to improve a

reliability of the gate oxide film.

### Brief Description of the Drawings

[0011]

5 Figs. 1A to 1D are schematic diagrams showing a manufacturing process of a manufacturing method of an SOI substrate with an oxide film on an active layer substrate side;

Figs. 2A to 2D are schematic diagrams showing a  
10 manufacturing process of a manufacturing method of an SOI substrate with an oxide film on a support substrate side;

Figs. 3A and 3B are schematic diagrams of an SOI device where crystal defects are formed on an upper side of a bonding surface between a support substrate and an active  
15 layer substrate;

Fig. 4 shows a pre-bonding cleaning method of an SOI substrate and its effects;

Fig. 5 shows a rate of destruction of a gate oxide film of an SOI device at an intrinsic breakdown voltage in Samples  
20 1 and 2, and whether or not crystal defects are formed;

Fig. 6 shows trace plots of a TEM image of an SOI substrate with an oxide film on a support substrate side in Sample 1;

Figs. 7A to 7C are schematic diagrams of three types of  
25 SOI substrates that reflect considerations of the inventor of

the present invention;

Fig. 8 shows in-plane distribution of a breakdown voltage of a gate oxide film of an SOI device under different pre-bonding cleaning conditions, and whether or not crystal  
5 defects are formed;

Fig. 9 is distribution chart of a breakdown voltage of a gate oxide film of an SOI device in the case of using a substrate with an oxide film on a support substrate side and a substrate with an oxide film on an active layer substrate  
10 side, which are washed with SCl as pre-bonding treatment;

Figs. 10A to 10G are schematic diagrams of a manufacturing process of an SOI device according to an embodiment of the present invention;

Fig. H A is a schematic diagram of a semiconductor  
15 device where a transistor and the like are formed in an SOI substrate;

Fig. H B is a schematic diagram of a semiconductor device of the related art where a transistor and the like are formed in an Si substrate; and

20 Figs. 12A to 12H are schematic diagrams of a manufacturing process of an SOI device of the related art, in which a dopant is ion-implanted.

#### **Explanation of Reference**

25 [0012]

- 1, 91 ACTIVE LAYER SUBSTRATE
- 2, 92 SUPPORT SUBSTRATE
- 3, 93 BURIED OXIDE FILM
- 4, 97 CRYSTAL DEFECT
- 5 5, 95 METAL IMPURITY
- 6 SiO<sub>2</sub>-MADE OXIDE FILM
- 7 SPONTANEOUS OXIDATION FILM
- 8A SOURCE REGION
- 8B GATE REGION
- 10 9, 96 GATE OXIDE FILM
- 10 GATE ELECTRODE
- 90 SOI DEVICE
- 94 SI SUBSTRATE
- 98 AMORPHOUS LAYER
- 15 99 SILICON OXIDE FILM
- 100 SI SUBSTRATE DEVICE
- 101 DEVICE SUCH AS TRANSISTOR

### **Best Modes for Carrying Out the Invention**

20 [0013]

As described above, a manufacturing method of an SOI substrate of the related art includes a step of injecting a dopant and the like and thus has problems in that a manufacturing process of an SOI substrate is complicated and  
25 a breakdown voltage is lowered in such a device that a

depletion layer reaches where a dopant is injected. The inventor of the subject application has made extensive studies to solve these problems and finally found that crystal defects are formed between an active layer substrate and a buried oxide film only by completely removing a spontaneous oxidation film formed on an active layer substrate to expose an Si surface and then bonding the Si surface to a support substrate with an oxide film, followed by heat treatment.

10 [0014]

According to the present invention, a bonding surface (referred also to as "joint surface") between a support substrate and an active layer substrate is positioned on an oxide film formed on a support substrate. The reason therefor is described below. In general, as a manufacturing method of a bonding SOI substrate, there are two methods: a method of bonding a support substrate onto an active layer substrate having an oxide film formed thereon (hereinafter referred to as "oxide film on an active layer substrate side") and a method of bonding an active layer substrate onto a support substrate having an oxide film formed thereon (hereinafter referred to as "oxide film on a support substrate side"). Referring first to Figs. IA to ID, a manufacturing method of an SOI substrate with an oxide film on an active layer substrate side is described. As shown in

15

20

25

Fig. 1A, a support substrate 2 is prepared first. As shown in Fig. 1B, an active layer substrate 1 is then prepared to form a buried oxide film 3 around the active layer substrate 1. As shown in Fig. 1C, the support substrate 2 is next  
5 bonded to the active layer substrate 1 with the buried oxide film 3, followed by heat treatment. As shown in Fig. 1D, the active layer substrate 1 is then ground or polished to form a device on the active layer substrate 1.

[0015]

10 Referring next to Figs. 2A to 2D, a manufacturing method of an SOI substrate with an oxide film on a support substrate side is described. As shown in Fig. 2A, the buried oxide film 3 is first formed around the support substrate 2. As shown in Fig. 2B, the active layer substrate 1 is prepared  
15 next. Subsequently, as shown in Fig. 2C, the active layer substrate 1 is bonded to the support substrate 2 with the buried oxide film 3, followed by heat treatment. As shown in Fig. 2D, the active layer substrate 1 is then ground or polished to form a device on the active layer substrate 1.

20 [0016]

In this example, it is effective to form crystal defects in the active layer substrate 1 to prevent defects of a gate oxide film. The reason therefor is described below. Fig. 3A is a schematic diagram of an SOI device with an oxide  
25 film on an active layer substrate side where crystal defects

are formed in a support substrate. Fig. 3B is a schematic diagram of an SOI device with an oxide film on a support substrate side where crystal defects are formed in an active layer substrate. As discussed later, the crystal defects are formed between an exposed Si substrate and the buried oxide film 3. Therefore, as shown in Fig. 3A, if the method of the present invention is applied to the device with an oxide film on an active layer substrate side, crystal defects 4 are formed in the support substrate 2 below the buried oxide film 3 in the SOI device with an oxide film on an active layer substrate side. Further, as described above, the SiO<sub>2</sub>-made buried oxide film 3 has a lower diffusion coefficient than that of the Si-made active layer substrate 1, so a diffusion speed of metal impurities 5 is slow in the buried oxide film 3. Therefore, the metal impurities 5 cannot easily pass through the buried oxide film 3. As a result, the crystal defects 4 formed below the buried oxide film 3 cannot trap the metal impurities 5 in the active layer substrate 1, and the metal impurities 5 are accumulated in the active layer substrate 1. That is, the metal impurities 5 accumulated in the active layer substrate 1 cause defects of a gate oxide film.

[0017]

On the other hand, as shown in Fig. 3B, if the method of the present invention is applied to the device with an

oxide film on a support substrate side, the crystal defects 4 are formed in the active layer substrate 1 (silicon surface) on the buried oxide film 3 (bonding surface between the silicon surface of the active layer substrate and the oxide film formed on the support substrate) in the SOI device with an oxide film on a support substrate side. Hence, the metal impurities 5 and the like in the active layer substrate 1 are trapped by the crystal defects 4. That is, the method of the present invention is applied to the SOI device with an oxide film on a support substrate side, making it possible to prevent the metal impurities 5 from causing defects of the gate oxide film. For that reason, according to the present invention, the oxide film on a support substrate side of Fig. 3B is employed.

15 [0018]

Further, the inventor of the subject application has found a technique effective for forming the crystal defects 4 at a bonding surface (silicon surface) of the active layer substrate 1 with reliability. That is, a spontaneous oxidation film on the surface of the active layer substrate 1 is completely removed to expose a clean Si surface and the Si surface is bonded to the support substrate with an oxide film. The reason therefor is described next. To begin with, two cleaning methods are compared. These cleaning methods differ from each other in cleaning conditions of an active layer

substrate prior to bonding of a support substrate with the active layer substrate (hereinafter referred to as pre-bonding treatment) . Fig. 4 shows the cleaning methods and effects thereof. As shown in Fig. 4, a cleaning method 1 using Sample 1 is SCl cleaning with a mixed solution of  $\text{NH}_4$ ,  $\text{H}_2\text{O}_2$ , and  $\text{H}_2\text{O}$ , and an etching rate thereof is about 1 nm/min. That is, SCl is an alkali solution, so  $\text{SiO}_2$  is etched with hydroxide ions ( $\text{OH}^-$ ) functioning as an etchant. Further, SCl cleaning is not so effective for removal of an organic material, that is, removal of a foreign substance larger than a particle, and removal of metal contaminants. On the other hand, a cleaning method 2 using Sample 2 is SC2 cleaning with a mixed solution of  $\text{HCl}$ ,  $\text{H}_2\text{O}_2$ , and  $\text{H}_2\text{O}$ , and Si and  $\text{SiO}_2$  are not etched. Further, SC2 cleaning is not so effective for removal of a particle and removal of an organic material, but is very effective of removal of metal contaminants.

[0019]

The SOI device with an oxide film on a support substrate side was subjected to pre-bonding treatment with the two cleaning methods. Fig. 5 shows results of evaluating distribution of a breakdown voltage of a gate oxide film of an SOI device with Sample 1 subjected to SCl cleaning and Sample 2 subjected to SC2 cleaning, and whether or not crystal defects are formed in an active layer substrate. As for the results of evaluating distribution of a breakdown

voltage of a gate oxide film, a film having a breakdown voltage of 9.5 MV/cm or higher is broken at an intrinsic breakdown voltage and used as a sample, and a rate of destruction is illustrated as the evaluation result. The evaluation results of Fig. 5 show that crystal defects are formed in the SOI device of Sample 1, and crystal defects are not formed in the SOI device of Sample 2. Further, the evaluation result of distribution of a breakdown voltage of a gate oxide film is more satisfactory in Sample 1 than in Sample 2. As shown in Fig. 5, about 93% of Sample 1 is broken at the intrinsic breakdown voltage, and the rest of about 7% of Sample 1 is broken at a lower voltage than the intrinsic breakdown voltage. In contrast, only about 10% of Sample 2 is broken at the intrinsic breakdown voltage, the rest of about 90% of Sample 2 is broken at a lower voltage than the intrinsic breakdown voltage. That is, in Sample 1, crystal defects are formed, and a gettering effect against metal impurities is exercised. Thus, the distribution of a breakdown voltage of a gate oxide film is improved.

20 [0020]

Here, Fig. 6 shows trace plots of a TEM (Transmission Electron Microscope) image of an SOI substrate with an oxide film on a support substrate side in Sample 1, in which crystal defects are formed. Fig. 6 shows trace plots of a portion of the joint surface between the buried oxide film 3

and the active layer substrate 1 with a magnification of  $10^{\delta}$ . As shown in Fig. 6, the crystal defects 4 are formed on the active layer substrate 1 side.

[0021]

5 Considerations made by the inventor from the above are explained with three types of SOI substrates with reference to Figs. 7A to 7C. As shown in Fig. 7A, crystal defects are not formed even if the SiO<sub>2</sub>-made buried oxide films 3 are bonded. On the other hand, as shown in Fig. 7B, the Si-made  
10 active layer substrate 1 is subjected to SCl cleaning to thereby etch Si and SiO<sub>2</sub>. As a result, the spontaneous oxidation film 7 is completely removed. Then, the buried oxide film 3 is bonded and heat treatment is carried out, with the result that the crystal defects 4 are formed.

15 Further, as shown in Fig. 7C, if the Si-made active layer substrate 1 is not well cleaned and the spontaneous oxidation film 7 partially remains on the active layer substrate 1, when the active layer substrate 1 and the SiO<sub>2</sub>-made buried oxide film 3 are bonded, the spontaneous oxidation film 7 is  
20 formed on the active layer substrate 1, so crystal defects are not formed.

[0022]

That is, if pre-bonding treatment is performed with a cleaning solvent capable of etching SiO<sub>2</sub> to remove the  
25 spontaneous oxidation film, followed by bonding, crystal

defects are formed in the active layer substrate.

[0023]

Here, it is desirable to completely remove the spontaneous oxidation film formed on the active layer substrate upon pre-bonding treatment to form crystal defects without fail. The reason therefor is described next. In this example, description is made of a result of evaluating distribution of a breakdown voltage of a gate oxide film under such conditions that pre-bonding treatment is performed with two cleaning solvents different in ability to etch SiO<sub>2</sub>. For this evaluation, SCl cleaning and HF cleaning that has a larger effect of etching Si and SiO<sub>2</sub> than the SCl cleaning are employed. Further, the SOI substrate with an oxide film on an active layer substrate side of Sample 1 with improved distribution of a breakdown voltage of a gate oxide film is used here. Fig. 8 shows a verification test result. In the substrate that underwent SCl cleaning upon pre-bonding treatment, crystal defects are not formed in some portions, and a breakdown voltage of the gate oxide film in these portions is lowered. On the other hand, in the substrate that underwent HF cleaning upon pre-bonding treatment, the crystal defects are formed throughout the substrate, and a breakdown voltage of the gate oxide film is not lowered.

[0024]

Fig. 9 shows distribution of a breakdown voltage of a

gate oxide film of an SOI device with the substrate with an oxide film on a support substrate side and the substrate with an oxide film on an active layer substrate side, which are subjected to SCl cleaning upon pre-bonding treatment. IN

5 this example, the horizontal axis represents a breakdown voltage  $E_{bd}$  [MV/cm] of the gate oxide film, and the vertical axis represents a cumulative fraction defective of the gate oxide film. Further, distribution of a breakdown voltage of the SOI device with an oxide film on an active layer

10 substrate side, which is subjected to SCl cleaning upon pre-bonding treatment is represented by circular plots (Sample 3). In addition, distribution of a breakdown voltage of the SOI device with an oxide film on a support substrate side, which is not cleaned enough with SCl upon pre-bonding treatment and

15 thus has the spontaneous oxidation film partially left on the active layer substrate is represented by rectangular plots (Sample 4). Moreover, distribution of a breakdown voltage of the SOI device with an oxide film on a support substrate side, which is subjected to SCl cleaning upon pre-bonding treatment

20 to thereby completely remove the spontaneous oxidation film formed on the active layer substrate is represented by triangular plots (Sample 5).

[0025]

As shown in Fig. 9, in the SOI device with an oxide

25 film on an active layer substrate side, which includes no

crystal defect on the active layer substrate side (Sample 3), about 11% of the substrate is broken at an intrinsic breakdown voltage (a ratio of the gate oxide film having a breakdown voltage of about 9.5 MV/cm or higher), and the rest of 89% of Sample 3 is broken at a lower voltage than the intrinsic breakdown voltage. In contrast, 93% and 100% of the substrate of the SOI device with an oxide film on a support substrate side, which is subjected to SCl cleaning, are broken at the intrinsic breakdown voltage in Sample 4 and Sample 5, respectively. As understood from this, a rate of destruction of the gate oxide film at the intrinsic breakdown voltage is dramatically improved. Here, in the SOI device where the spontaneous oxidation film is partially left (Sample 4), about 7% of the entire SOI substrate does not have a breakdown voltage of about 9.5 MV/cm. On the other hand, the SOI device from which the spontaneous oxidation film is completely removed (Sample 5) has a breakdown voltage of about 10 MV/cm over the SOI substrate.

[0026]

That is, pre-bonding cleaning is performed with a cleaning method capable of etching Si and SiO<sub>2</sub>. Then, the spontaneous oxidation film formed on the active layer substrate is removed to thereby form crystal defects in the substrate of the SOI device. Owing to the crystal defects, a rate of destruction of the gate oxide film of the SOI device

at the intrinsic breakdown voltage is improved. That is, in the SOI device, a ratio of areas having a gate oxide film breakdown voltage lower than the intrinsic breakdown voltage to the entire substrate is reduced, and reliability is increased. Here, the spontaneous oxidation film is completely removed to thereby form crystal defects throughout the substrate of the SOI device, so a rate of destruction of the gate oxide film of an SOI device at the intrinsic breakdown voltage is further improved.

10 [0027]

As understood from the above, the spontaneous oxidation film formed on the active layer substrate is first removed completely to expose Si of the active layer substrate in order to form crystal defects without fail upon the pre- bonding treatment. Then, the active layer substrate is bonded to the support substrate with the buried oxide film, followed by heat treatment. As a result, crystal defects can be formed throughout the active layer substrate. Thus, a rate of destruction of the gate oxide film of an SOI device at the intrinsic breakdown voltage can be improved, and reliability can be increased.

First Embodiment

[0028]

An embodiment of the present invention will be described in detail below with reference to Figs. 10A to 10G.

Figs. 10A to 10G are schematic diagrams of a manufacturing process for forming an SOI substrate and forming a device to the SOI substrate according to this embodiment. As shown in Fig. 10A, the support substrate 2 made of single-crystal Si is prepared. As shown in Fig. 10B, the support substrate 2 is thermally oxidized to form the SiO<sub>2</sub>-made buried oxide film 3 around the support substrate 2.

[0029]

As shown in Fig. 10C, the active layer substrate 1 made of single-crystal Si is prepared next. As shown in Fig. 10D, pre-bonding treatment is then performed to remove the spontaneous oxidation film 7 formed around the active layer substrate 1. As described above, the spontaneous oxidation film 7 formed on the active layer substrate 1 is removed through pre-bonding treatment to thereby form the crystal defects 4 in the active layer substrate 1. As a result, a rate of destruction of the gate oxide film at the intrinsic breakdown voltage can be improved. Therefore, pre-bonding treatment is performed to remove the spontaneous oxidation film 7 formed around the active layer substrate 1 to expose the surface of the active layer substrate 1. That is, pre-bonding treatment that can remove the spontaneous oxidation film 7 formed around the active layer substrate 1 to expose the Si surface portion of the active layer substrate 1.

25 [0030]

For example, the above SCl cleaning is carried out to etch Si and SiO<sub>2</sub> to remove the spontaneous oxidation film 7 formed on the active layer substrate 1. Here, a mixing ratio of solutions for SCl cleaning is preferably NH<sub>4</sub>OH:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O = 1:1:5, but a mixing ratio of NH<sub>4</sub>OH can be changed as appropriate if the spontaneous oxidation film 7 can be removed. Further, it is preferable to set enough cleaning time to completely remove the spontaneous oxidation film 7. Moreover, Si and SiO<sub>2</sub> can be etched even during HF cleaning. Here, a mixing ratio of solutions for HF cleaning is preferably HF:H<sub>2</sub>O = 1:100, but any mixing ratio can be set insofar as the spontaneous oxidation film 7 can be removed. Further, HF-H<sub>2</sub>O<sub>2</sub> and HF-HCl can be used aside from HF in HF cleaning. Moreover, it is possible to remove the spontaneous oxidation film 7 with CMP (Chemical Mechanical Polishing) as mechanical polishing. As understood from the above, pre-bonding treatment can be performed under the following combinations of conditions for the purpose of removing the spontaneous oxidation film 7. For example, pre-bonding treatment involves SCl cleaning alone, HF cleaning alone, CMP alone, SCl cleaning and HF cleaning.

[0031]

As an example of treatment capable of cleaning the active layer substrate 1 albeit small effect of etching Si and SiO<sub>2</sub>, there are SPM cleaning and SC2 cleaning. For

example, SCl cleaning is performed to etch Si and SiO<sub>2</sub> to thereby remove the spontaneous oxidation film 7 formed on the active layer substrate 1. In addition, SPM cleaning, SC2 cleaning, or the like is performed to suppress contamination of the active layer substrate 1. Here, SPM cleaning uses a mixed solution of H<sub>2</sub>SO<sub>4</sub> and H<sub>2</sub>O<sub>2</sub>, and has a high ability to remove an organic material and a high ability to remove metal contaminants but has a small effect of removing particles. A mixing ratio of solutions for SPM cleaning is preferably H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub> = 4:1. Further, a mixing ratio of solutions for SC2 cleaning is preferably HCl:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O = 1:1:6.

[0032]

Next, as shown in Fig. 10E, the active layer substrate 1 from which the spontaneous oxidation film 7 is removed enough to expose Si, is bonded to the support substrate 2 with the buried oxide film 3, followed by heat treatment. At this time, the crystal defects 4 are formed near the bonding surface on the active layer substrate 1 side. As shown in Fig. 10F, the surface of the active layer substrate 1 opposite to the bonding surface is next ground or polished into a predetermined thickness. At this time, SCl cleaning, and SC2 cleaning, SPM cleaning, and the like, which have an effect of removing metal contaminants may be performed for cleaning.

25 [0033]

As shown in Fig. 10G, a device is formed next to the SOI substrate completed by bonding the active layer substrate 1 to the support substrate 2 with the buried oxide film 3. That is, a source region 8a and a gate region 8b are formed in the active layer substrate 1. Then, a gate electrode 10 is formed on the active layer substrate 1 through the gate oxide film 9 to thereby form the device to the SOI substrate to complete the SOI device.

[0034]

10 In this embodiment, prior to bonding of the active layer substrate 1 to the support substrate 1 with the buried oxide film 3, the spontaneous oxidation film 7 formed on the active layer substrate 1 is removed and the active layer substrate 1 is bonded to the support substrate 2 with the buried oxide film 3. That is, Si of the active layer substrate 1, which is exposed by removing the spontaneous oxidation film 7 is bonded to SiO<sub>2</sub> of the buried oxide film 3, followed by heat treatment to thereby form crystal defects near the bonding surface of the active layer substrate 1.

15 The crystal defects near the bonding surface of the active layer substrate 1 trap metal impurities in the active layer substrate 1. As a result, an influence of metal impurities on the gate oxide film 9 formed on the active layer substrate 1 can be suppressed, making it possible to improve a

20 breakdown voltage of the gate oxide film 9. Then, a rate of

25

destruction of the gate oxide film 9 at the intrinsic breakdown voltage can be improved. Further, in this embodiment, the crystal defects 4 can be formed not through a step of implanting ions to the active layer substrate 1 and a  
5 heat treatment step of the ion-implanted active layer substrate 1, so a manufacturing cost of the substrate can be saved. Further, it is possible to prevent reduction in breakdown voltage in such a device that a depletion layer reaches where a dopant is injected.

10 [0035]

Incidentally, the present invention is not limited to the above embodiments solely but may be variously modified within the scope of the present invention.

## 15 **Industrial Applicability**

[0036]

The present invention provides a manufacturing method of a semiconductor substrate and manufacturing method of a semiconductor device. In particular, the invention is  
20 applicable to a manufacturing method of a bonding SOI substrate, and a manufacturing method of a semiconductor device using a bonding SOI substrate.

## CLAIMS

1. A manufacturing method of a semiconductor substrate, comprising:

5 exposing a silicon surface of an active layer substrate made of single-crystal silicon, to which a semiconductor device is formed;

forming an oxide film on a support substrate made of single-crystal silicon; and

10 bonding the silicon surface of the active layer substrate to the oxide film formed on the support substrate.

2. The manufacturing method of a semiconductor substrate according to claim 1, wherein a spontaneous oxidation film formed on a surface of the active layer substrate is removed to expose the silicon surface.

3. The manufacturing method of a semiconductor substrate according to claim 2, wherein crystal defects are formed in the silicon surface as a bonding surface between the silicon surface of the active layer substrate and the oxide film formed on the support substrate.

4. The manufacturing method of a semiconductor substrate according to claim 1, wherein no dopant remains in the silicon surface as a bonding surface between the silicon surface of the active layer substrate and the oxide film formed on the support substrate .

5. The manufacturing method of a semiconductor substrate according to claim 2, wherein the spontaneous oxidation film on a surface of the active layer substrate is removed through at least one of cleaning and etching.

6. The manufacturing method of a semiconductor substrate according to claim 5, wherein the spontaneous oxidation film is removed through at least one of SCl cleaning, HF cleaning, and mechanical polishing.

7. The manufacturing method of a semiconductor substrate according to claim 5, wherein the spontaneous oxidation film is removed through at least one of SCl cleaning, HF cleaning, and mechanical polishing and in addition, through SC2 cleaning or SPM cleaning.

8. A manufacturing method of a semiconductor device, comprising:

exposing a silicon surface of an active layer substrate made of single-crystal silicon, to which a  
5 semiconductor device is formed;

forming an oxide film on a support substrate made of single-crystal silicon; and

bonding the silicon surface of the active layer substrate to the oxide film formed on the support  
10 substrate to remove a portion of a surface of the active layer substrate opposite to a bonding surface;  
and

forming the semiconductor device to a surface  
15 portion of the active layer substrate opposite to the bonding surface.

9. The manufacturing method of a semiconductor device according to claim 8, wherein a spontaneous  
oxidation film formed on the surface of the active  
20 layer substrate is removed to expose the silicon surface.

10. The manufacturing method of a semiconductor device according to claim 9, wherein crystal defects  
25 are formed in the silicon surface as a bonding surface

between the silicon surface of the active layer substrate and the oxide film formed on the support substrate.

5           11. The manufacturing method of a semiconductor device according to claim 8, wherein no dopant remains in the silicon surface as a bonding surface between the silicon surface of the active layer substrate and the oxide film formed on the support substrate.

10

12. The manufacturing method of a semiconductor device according to claim 9, wherein the spontaneous oxidation film on the surface of the active layer substrate is removed through at least one of cleaning and etching.

15

13. The manufacturing method of a semiconductor device according to claim 12, wherein the spontaneous oxidation film is removed through at least one of SCl cleaning, HF cleaning, and mechanical polishing.

20

14. The manufacturing method of a semiconductor device according to claim 12, wherein the spontaneous oxidation film is removed through at least one of SCl cleaning, HF cleaning, and mechanical polishing and in addition, through SC2

25 cleaning or SPM cleaning.

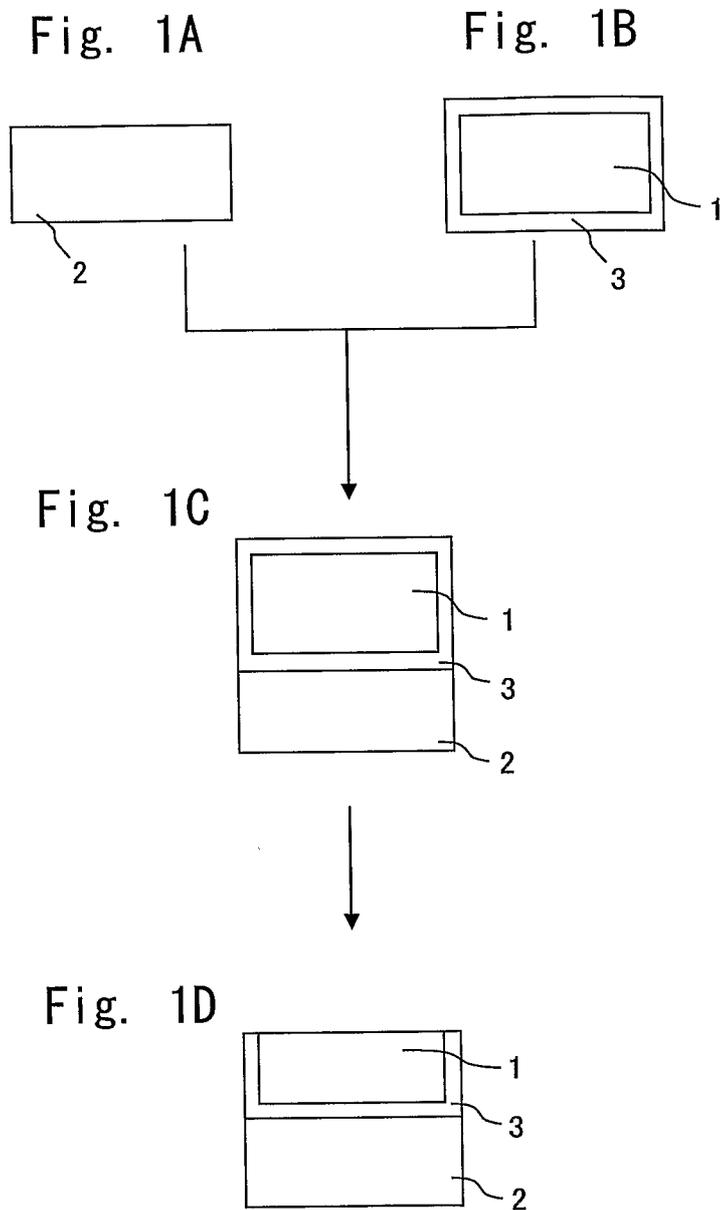


Fig. 2A

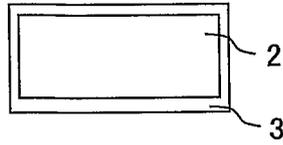


Fig. 2B

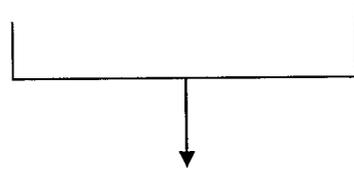
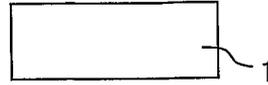


Fig. 2C

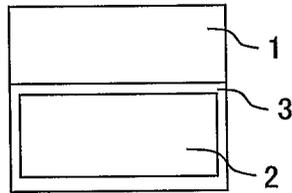
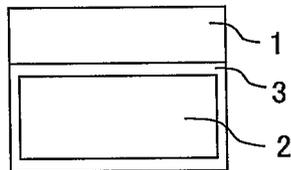


Fig. 2D



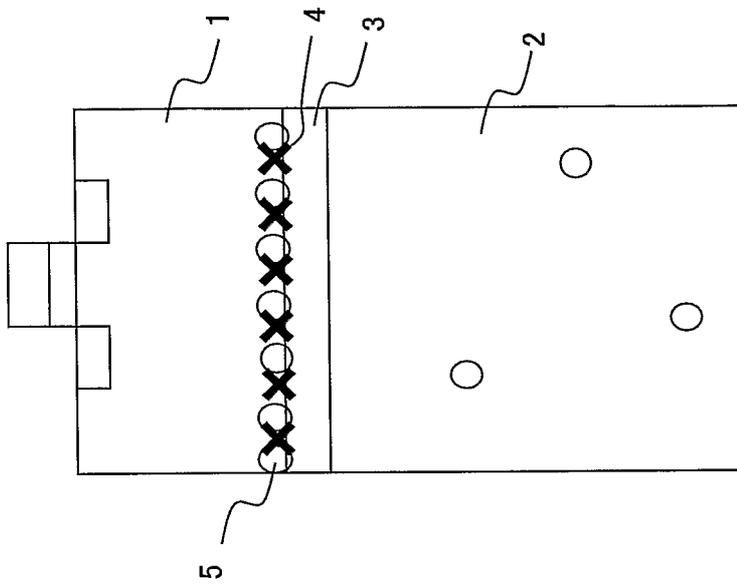


Fig. 3B

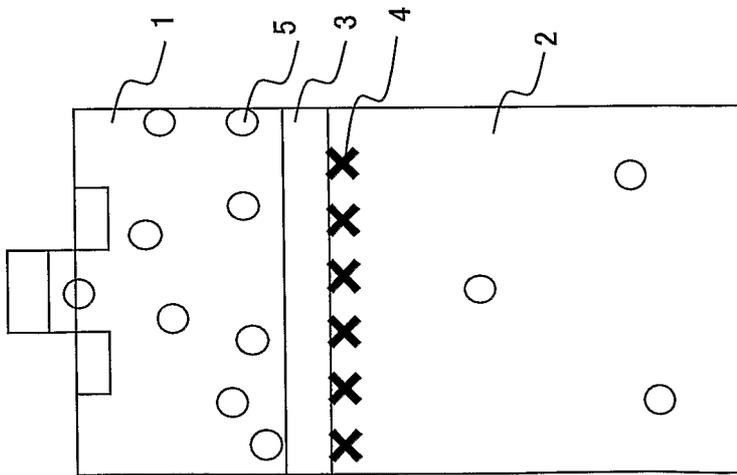


Fig. 3A

CLEANING METHOD	SOLUTION	ABILITY TO REMOVE PARTICLE	ABILITY TO REMOVE ORGANIC MATERIAL	ABILITY TO REMOVE METAL CONTAMINANT	ETCHING OF Si AND SiO <sub>2</sub>
1	NH <sub>4</sub> OH/H <sub>2</sub> O <sub>2</sub> (SC1)	HIGH	MID	LOW	ABOUT 1nm/Min
2	HCl/H <sub>2</sub> O <sub>2</sub> (SC2)	LOW	LOW	HIGH	-

Fig. 4

5/12

SAMPLE	PRE-BONDING CLEANING	RATE OF DESTRUCTION OF GATE OXIDE FILM AT INTRINSIC BREAKDOWN VOLTAGE (%)	CRYSTAL DEFECT
1	NH <sub>4</sub> OH/H <sub>2</sub> O <sub>2</sub> (SC1)	93	CRYSTAL DEFECT FOUND
2	HCl/H <sub>2</sub> O <sub>2</sub> (SC2)	10	NO CRYSTAL DEFECT

Fig. 5

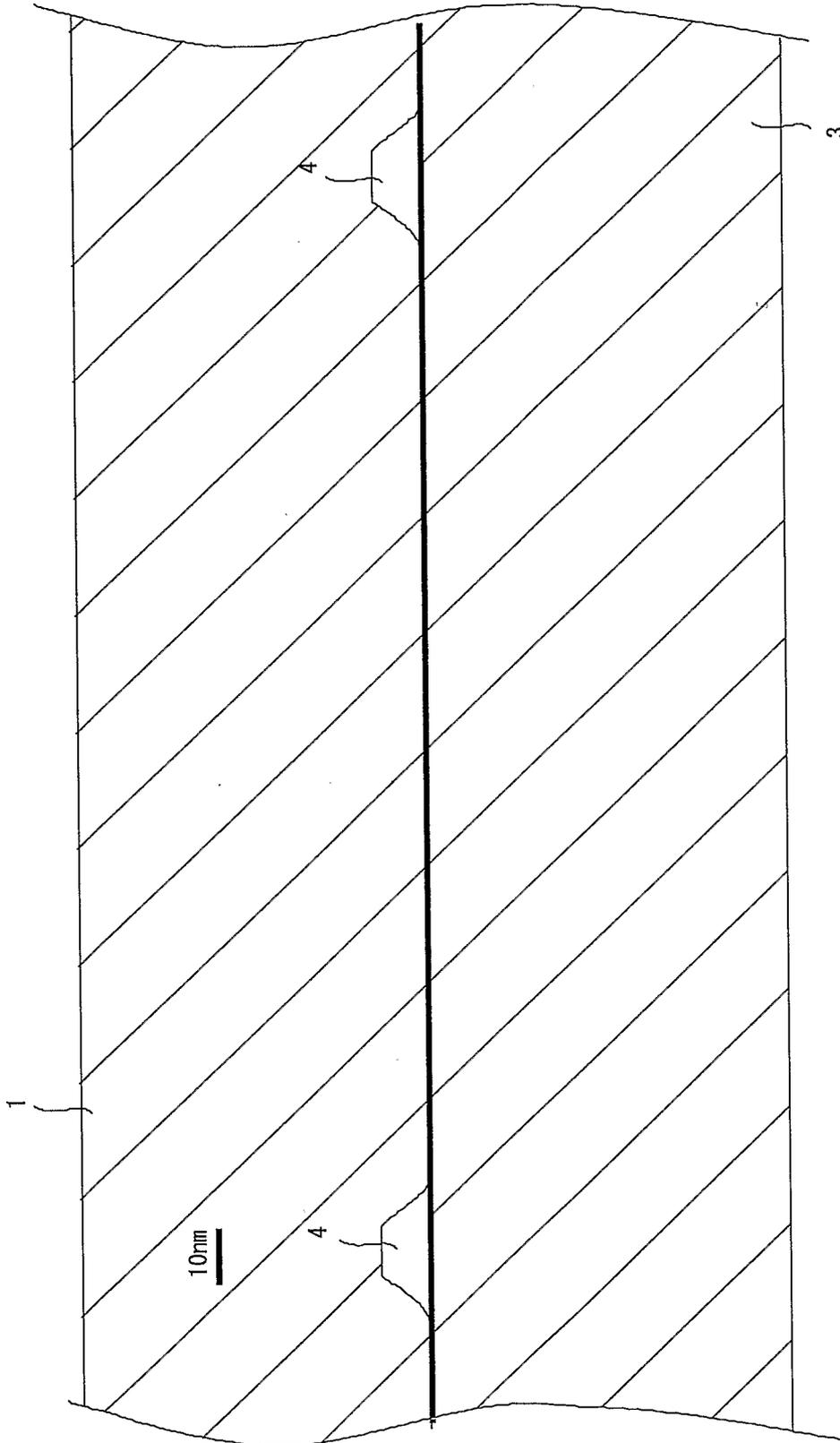


Fig. 6

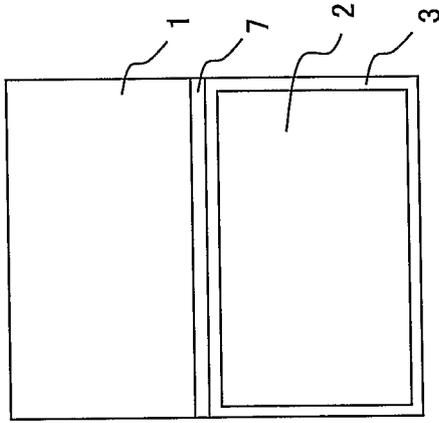


Fig. 7C

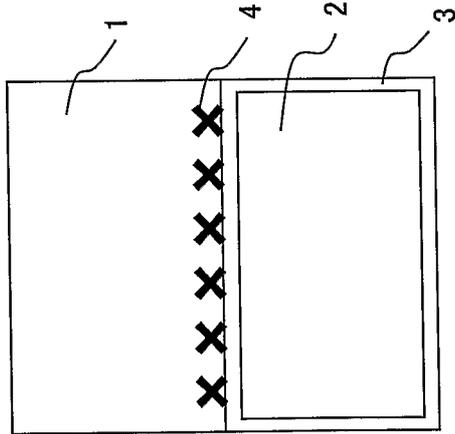


Fig. 7B

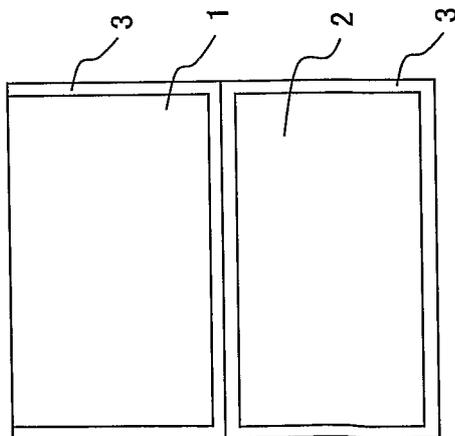


Fig. 7A

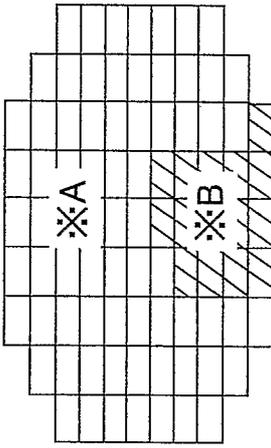
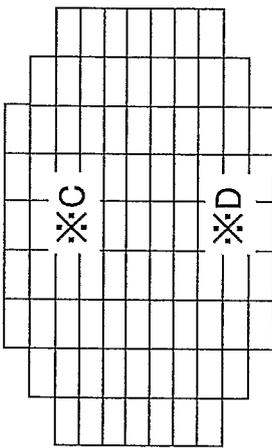
PRE-BONDING TREATMENT	ETCHING OF Si AND SiO <sub>2</sub>	BREAKDOWN VOLTAGE OF GATE OXIDE FILM IN-PLANE DISTRIBUTION	CRYSTAL DEFECT
<p>NH<sub>4</sub>OH/H<sub>2</sub>O<sub>2</sub> (SC1)</p>	<p>ABOUT 1nm/Min</p>	<p>CHIP DESTROYED AT INTRINSIC BREAKDOWN VOLTAGE CHIP DESTROYED AT INTRINSIC BREAKDOWN VOLTAGE OR LESS</p>  <p>※ A, B REPRESENT SITES WHERE CRYSTAL DEFECTS ARE OBSERVED.</p>	<p>※A: DEFECT FOUND</p> <p>※B: NO DEFECT</p>
<p>HF</p>	<p>ABOUT 10nm/sec</p>	<p>CHIP DESTROYED AT INTRINSIC BREAKDOWN VOLTAGE CHIP DESTROYED AT INTRINSIC BREAKDOWN VOLTAGE OR LESS</p>  <p>※ C, D REPRESENT SITES WHERE CRYSTAL DEFECTS ARE OBSERVED.</p>	<p>※C: NO DEFECT</p> <p>※D: DEFECT FOUND</p>

Fig. 8

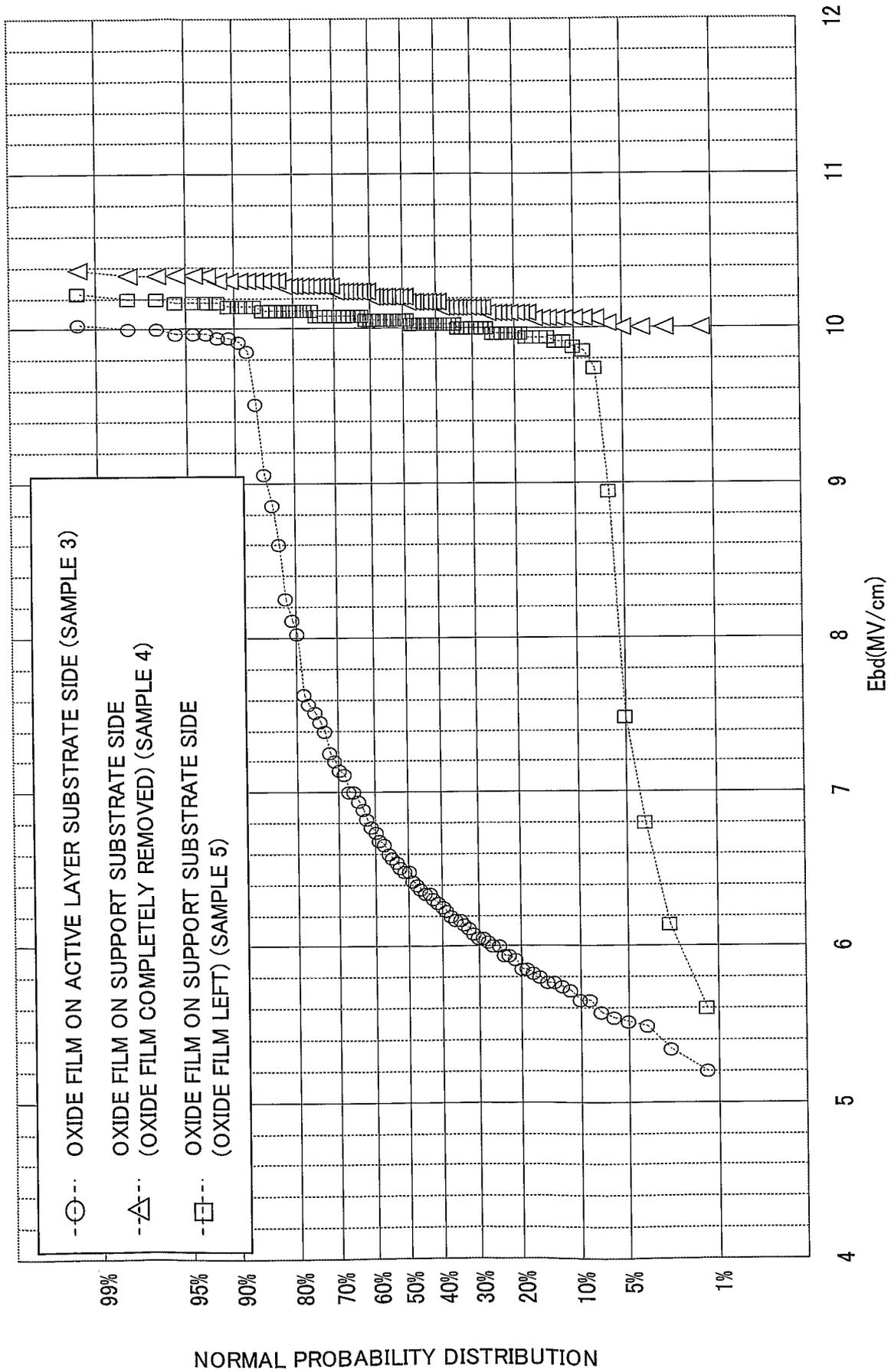


Fig. 9

Fig. 10A

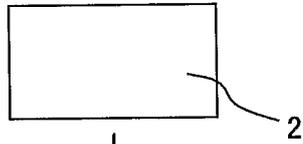


Fig. 10B

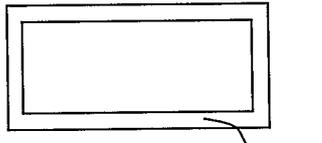


Fig. 10C

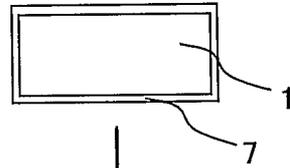


Fig. 10D

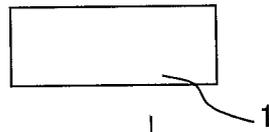


Fig. 10E

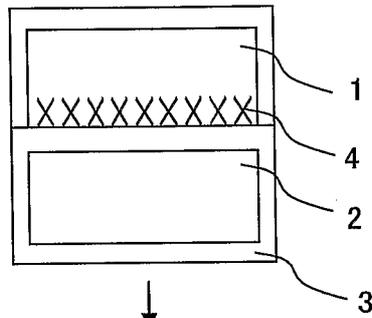


Fig. 10F

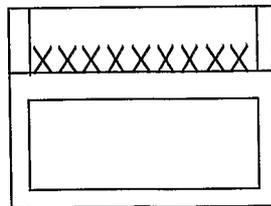
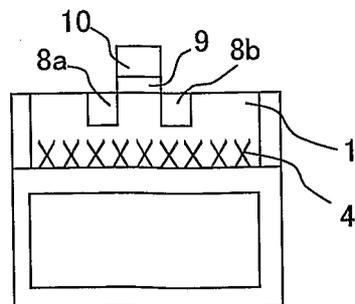


Fig. 10G



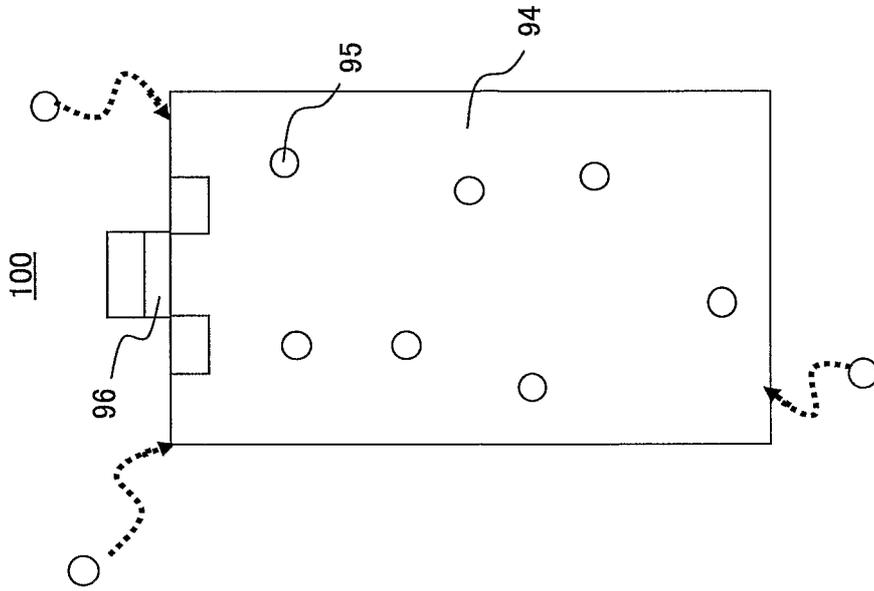


Fig. 11B

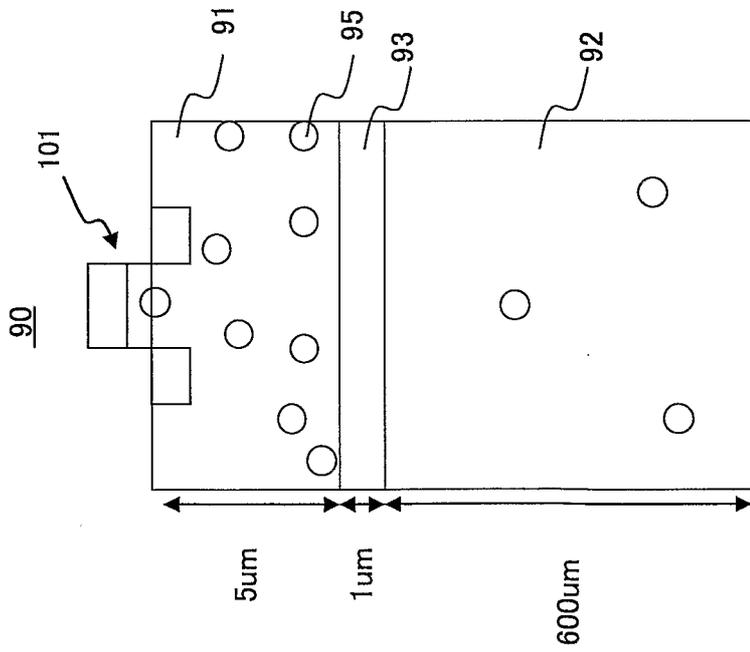
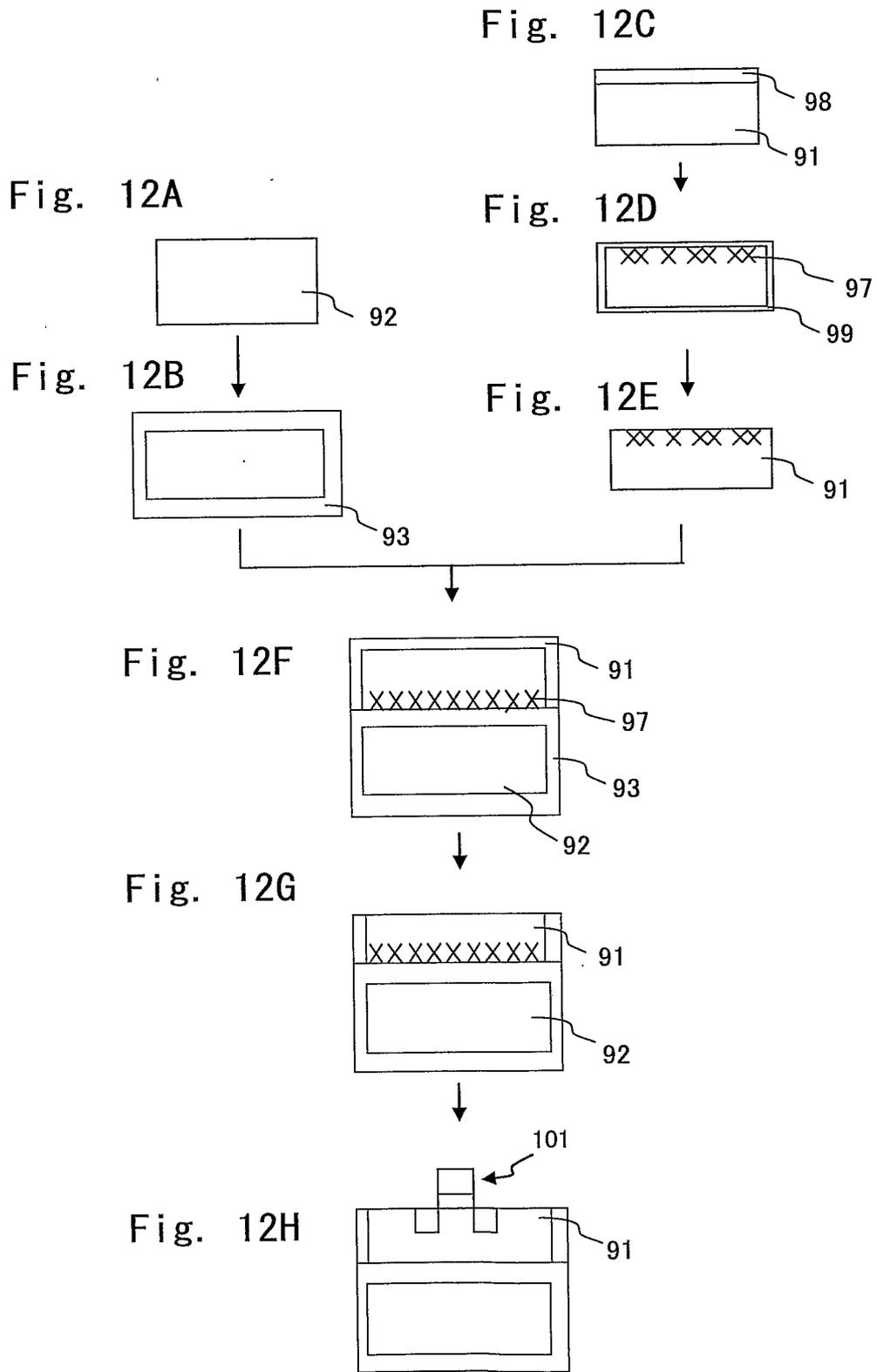


Fig. 11A



**INTERNATIONAL SEARCH REPORT**

International application No  
PCT/JP2007/066075

**A. CLASSIFICATION OF SUBJECT MATTER**  
INV. H01L21/762 H01L21/322

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
HOIL

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal , WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 571 693 A (SHINETSU HANDOTAI KK [JP]) 7 September 2005 (2005-09-07) column 8 , paragraph 34 column 9 , paragraph 40 - column 10, paragraph 45 figure 1	1-14
X	EP 1 187 216 A (SHINETSU HANDOTAI KK [JP]) 13 March 2002 (2002-03-13) page 2 , paragraph 11 page 3 , paragraph 22 - page 4 , paragraph 30 figure IA table 1	1-14

Further documents are listed in the continuation of Box C.

See patent family annex.

\* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the International filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- "&" document member of the same patent family

Date of the actual completion of the international search

10 December 2007

Date of mailing of the international search report

18/12/2007

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,  
Fax: (+31-70) 340-3016

Authorized officer

Ekoue, Adamah

## INTERNATIONAL SEARCH REPORT

International application No

PCT/JP2007/066075

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>EP 1 381 086 A (SHINETSU HANDOTAI KK [JP])  14 January 2004 (2004-01-14)  column 8, paragraph 44 - column 9,  paragraph 50  figure 1</p> <p style="text-align: center;">-----</p>	1-14
X	<p>CHAO ET AL: "Investigation of  silicon-on-insulator (SOI) substrate  preparation using the smart-cut&lt;TM&gt;  process"  NUCLEAR INSTRUMENTS &amp; METHODS IN PHYSICS  RESEARCH, SECTION - B: BEAM INTERACTIONS  WITH MATERIALS AND ATOMS, ELSEVIER,  AMSTERDAM, NL,  vol. 237, no. 1-2, August 2005 (2005-08),  pages 197-202, XP005010134  ISSN: 0168-583X  page 198, left-hand column, paragraph 3  page 199, left-hand column, paragraph 2  figure 1</p> <p style="text-align: center;">-----</p>	1-14
X	<p>US 2006/148208 A1 (POPOV VLADIMIR P [RU]  ET AL) 6 July 2006 (2006-07-06)  page 3, paragraph 44 - page 4, paragraph  48  figure 1</p> <p style="text-align: center;">-----</p>	1-14
X	<p>US 2003/227057 A1 (LOCHTEFELD ANTHONY J  [US] ET AL) 11 December 2003 (2003-12-11)  page 3, paragraph 42  page 4, paragraph 49  figures 3,8</p> <p style="text-align: center;">-----</p>	1-14

## INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/JP2007/066075

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
EP 1571693	A	07-09-2005	WO	2004055871	A1	01-07-2004
			JP	2004193515	A	08-07-2004
			US	2006014330	A1	19-01-2006
EP 1187216	A	13-03-2002	WO	0148825	A1	05-07-2001
			TW	511141	B	21-11-2002
			us	2003040163	A1	27-02-2003
EP 1381086	A	14-01-2004	CN	1461496	A	10-12-2003
			WO	02086975	A1	31-10-2002
			JP	2002313689	A	25-10-2002
			US	2004035525	A1	26-02-2004
US 2006148208	A1	06-07-2006	RU	2217842	C1	27-11-2003
			WO	2004064137	A1	29-07-2004
us 2003227057	A1	11-12-2003	US	2005156246	A1	21-07-2005